TX FIR Equalizer – CM mode

12 Gbps

(Final Report)

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Outline

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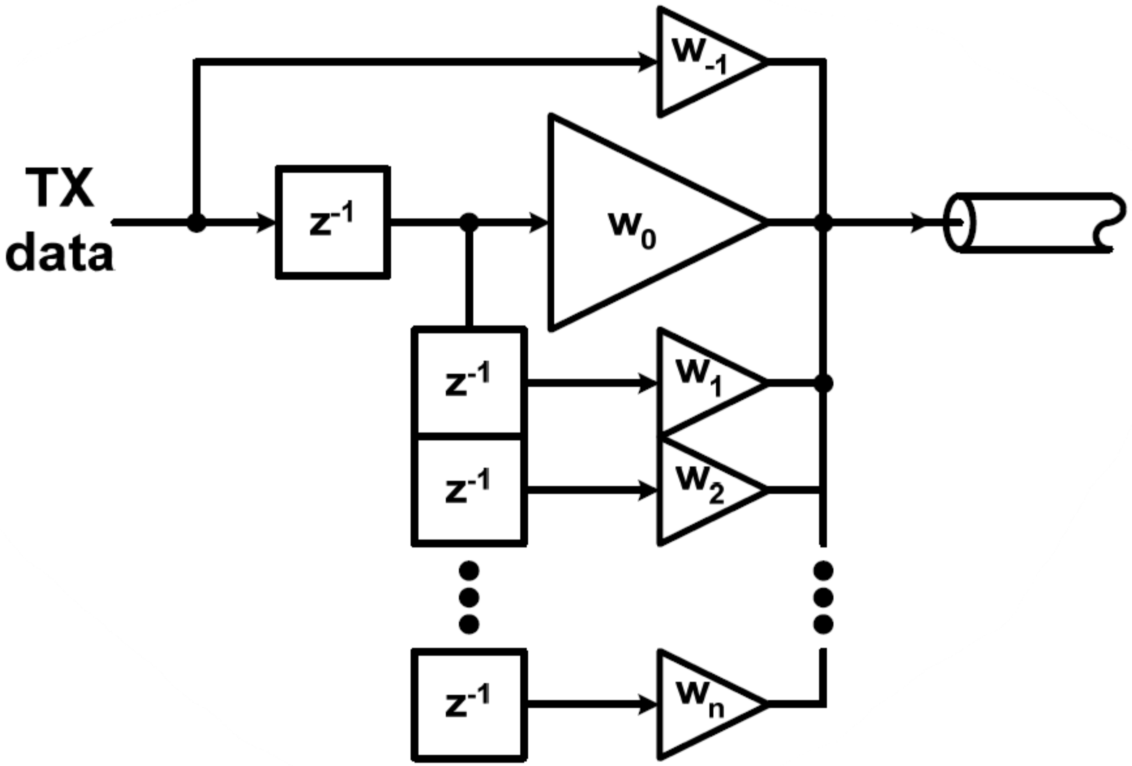
2. Implementation
3. Schematics
4. Simulation Results
    a) Pulse Response
    b) Eye Diagram
    c) Transient Waveforms

Background

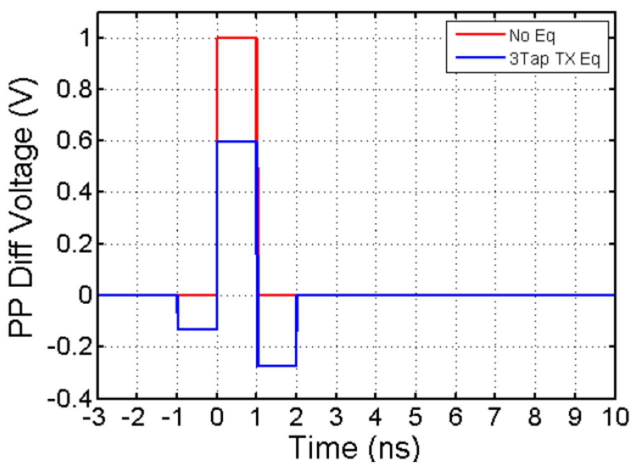
- "TX FIR equalization" is the technique in which a transmitter applies a Finite Impulse Response (FIR) filter to pre-distort the signal before sending it.
- This is to compensate for the distortions introduced by the transmission channel, thus improving signal quality at the receiver by mitigating intersymbol interference (ISI).

Background

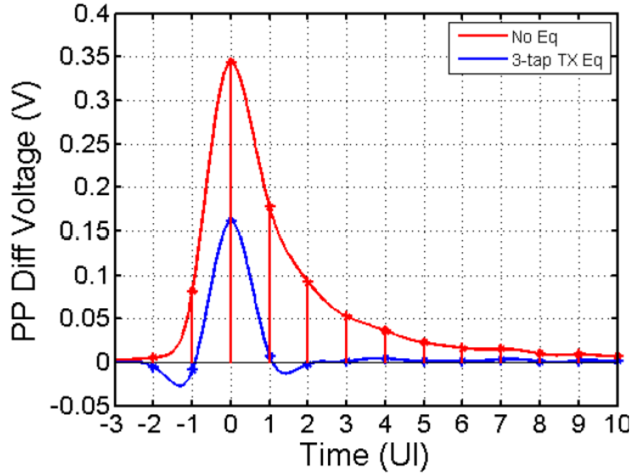


Time Domain

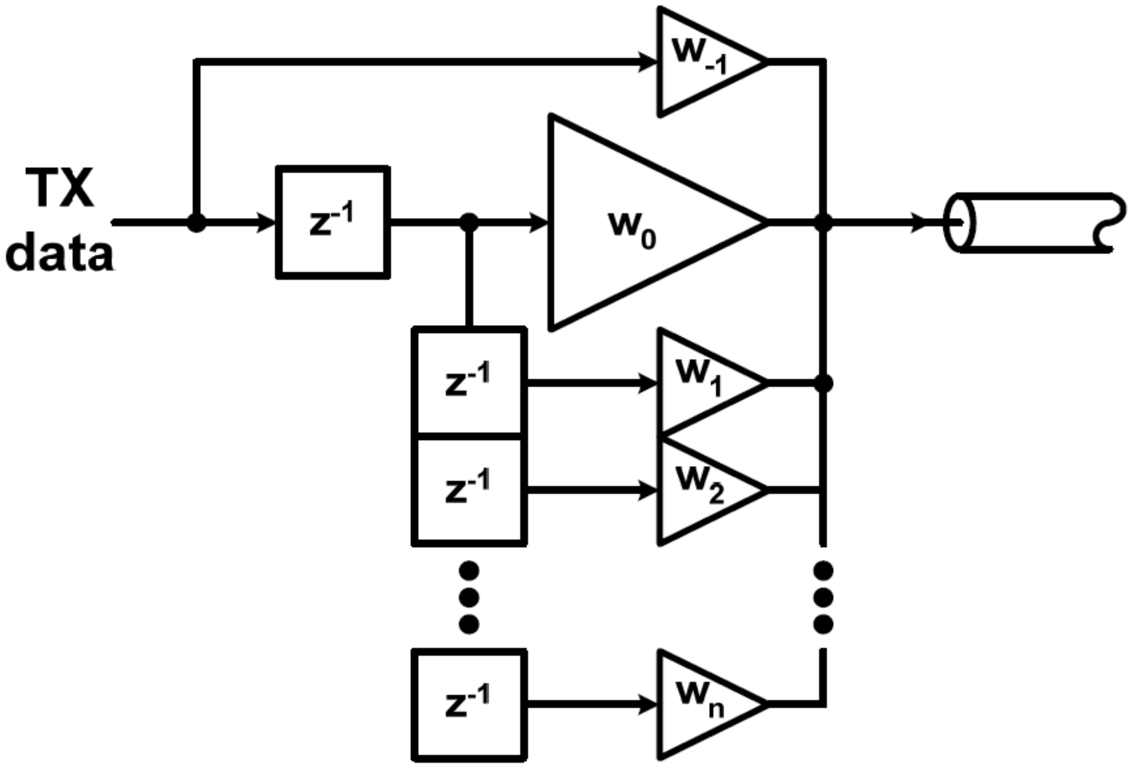
Input Pulse w/ 3-tap TX Eq



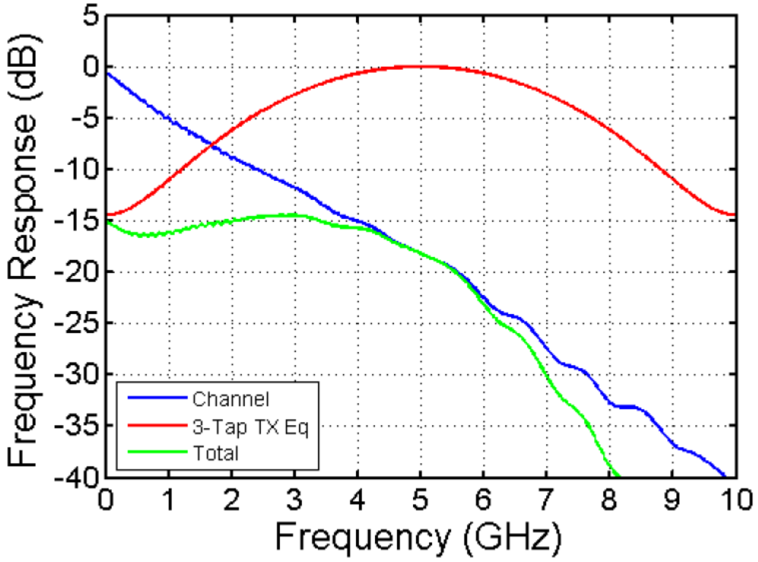
Output Pulse Response



Background

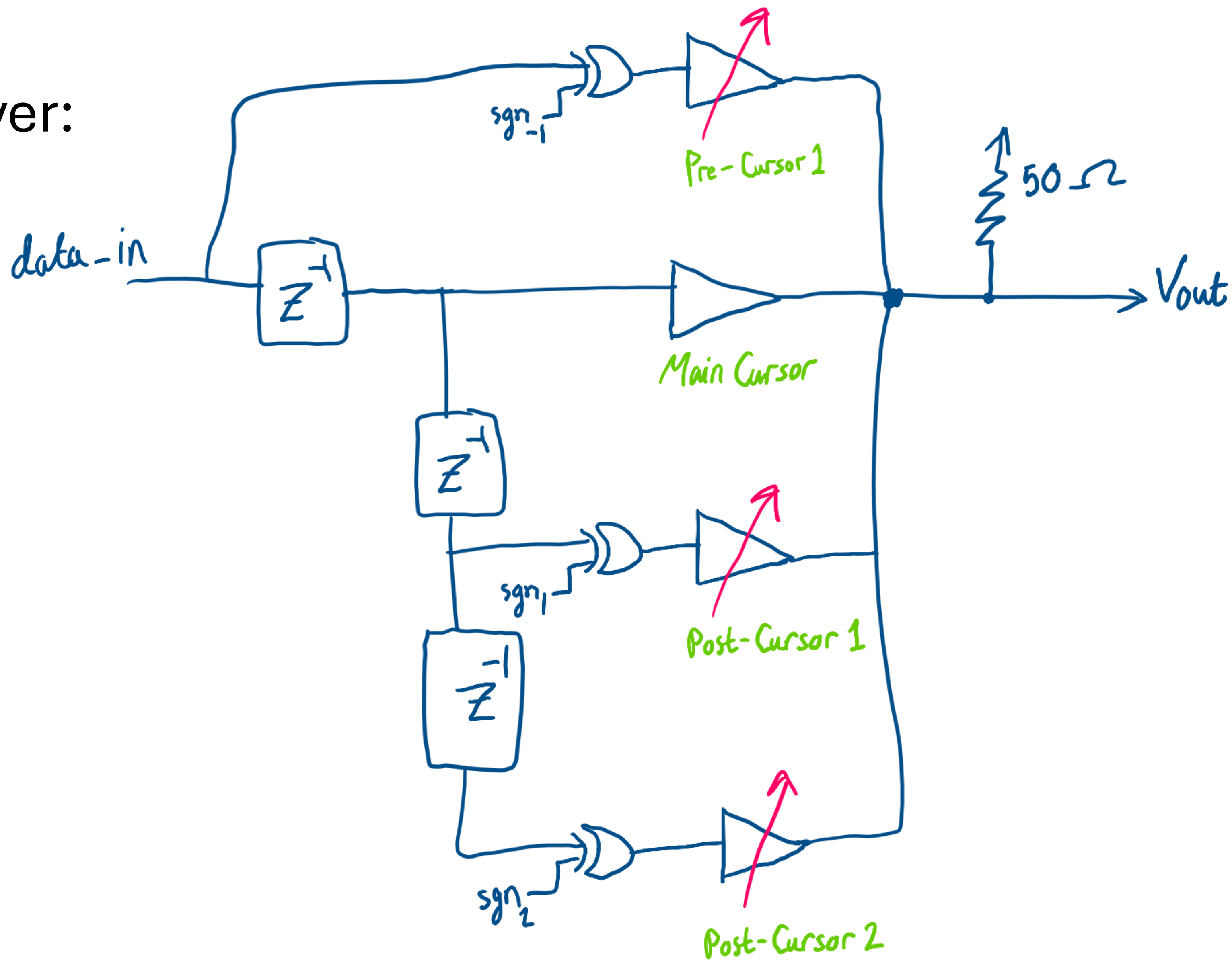


Freq Domain



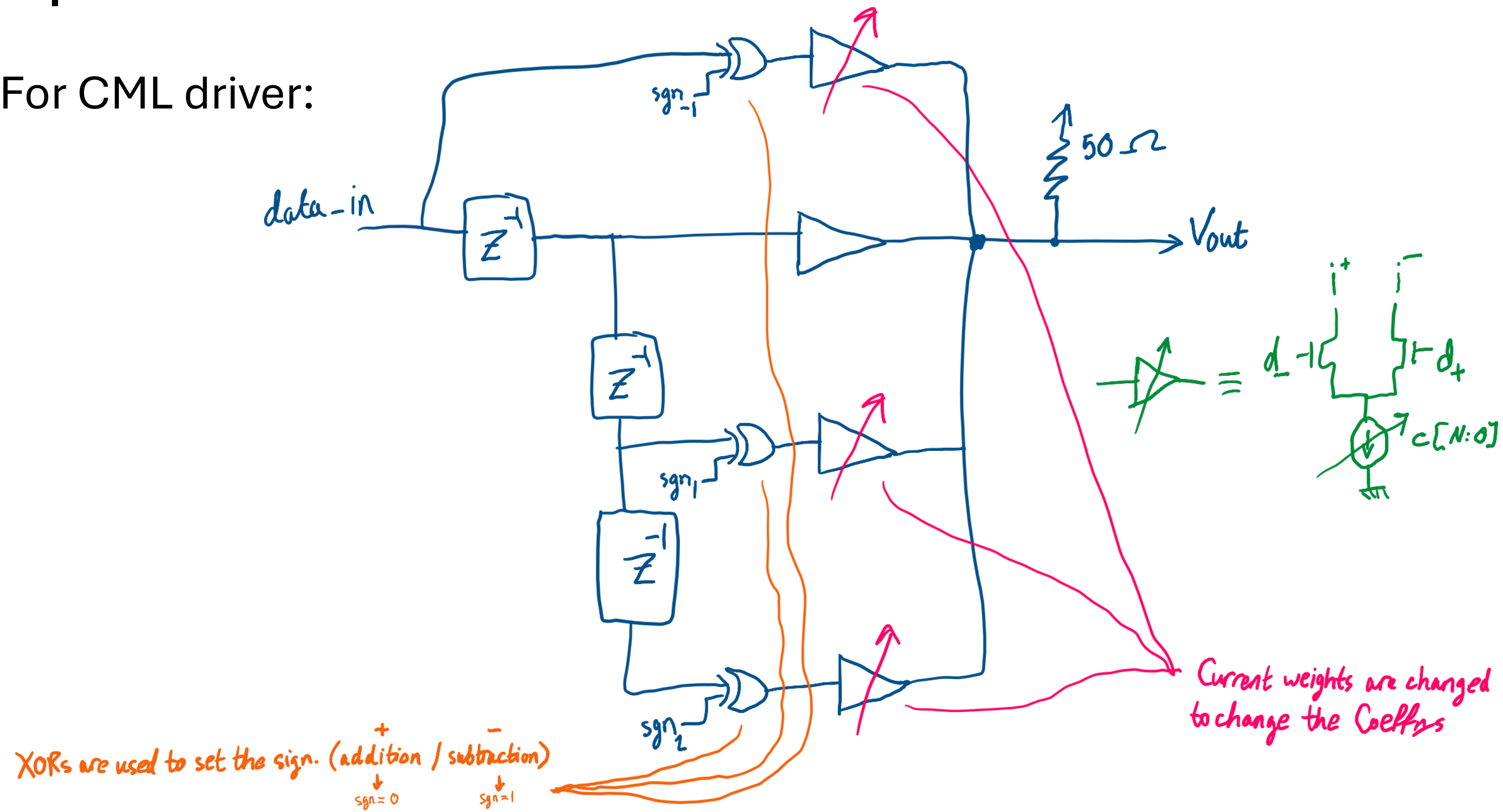
Implementation

- For CML driver:

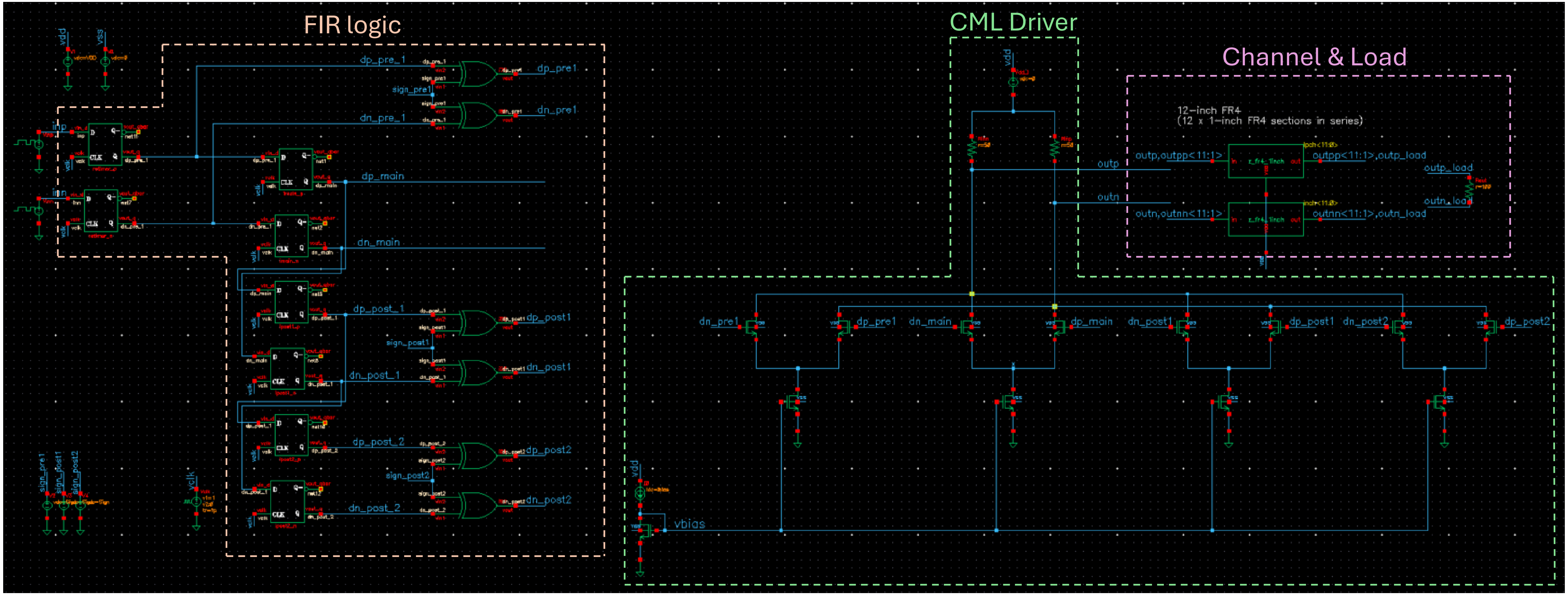


Implementation

- For CML driver:



Schematics

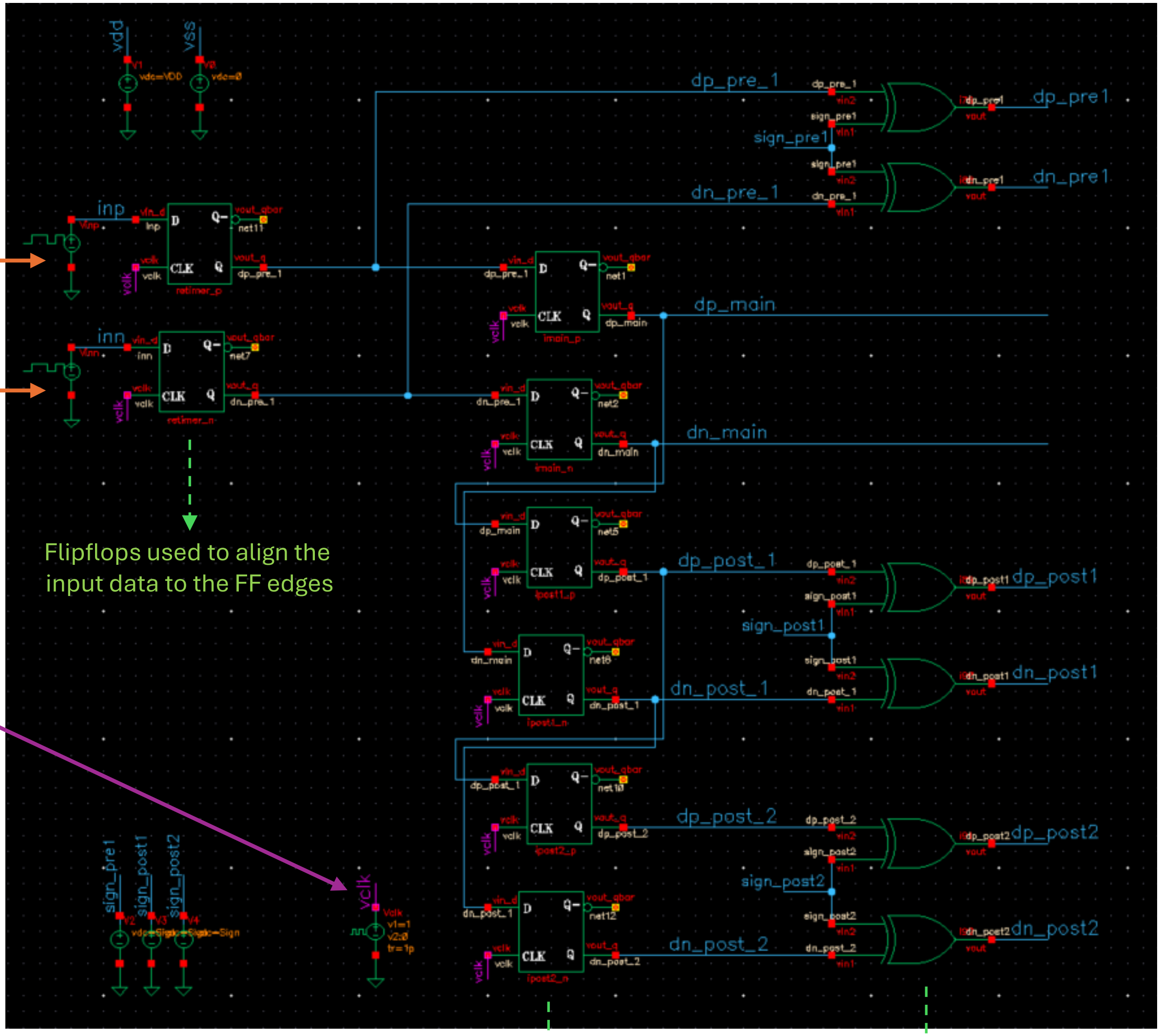

FIR logic
CML Driver
Channel & Load
12-inch FR4
(12 x 1-inch FR4 sections in series)
dp_pre_1
dp_pre1
dn_pre_1
dn_pre1
sign_pre1
dp_main
dn_main
dp_post_1
dp_post1
sign_post1
dn_post_1
dn_post1
dp_post_2
dp_post2
sign_post2
dn_post_2
dn_post2
outp
outn
outp,outpp<11:1>
outpp<11:1>,outp_load
outn,outnn<11:1>
outnn<11:1>,outn_load
outp_load
outn_load
vbias
vdd
vss
vclk
inp
inn

Schematics

A) FIR Logic:

12 Gb/s PRBS Inputs

12 GHz Clock



Pre-Cursor 1

Main-Cursor

Post-Cursor 1

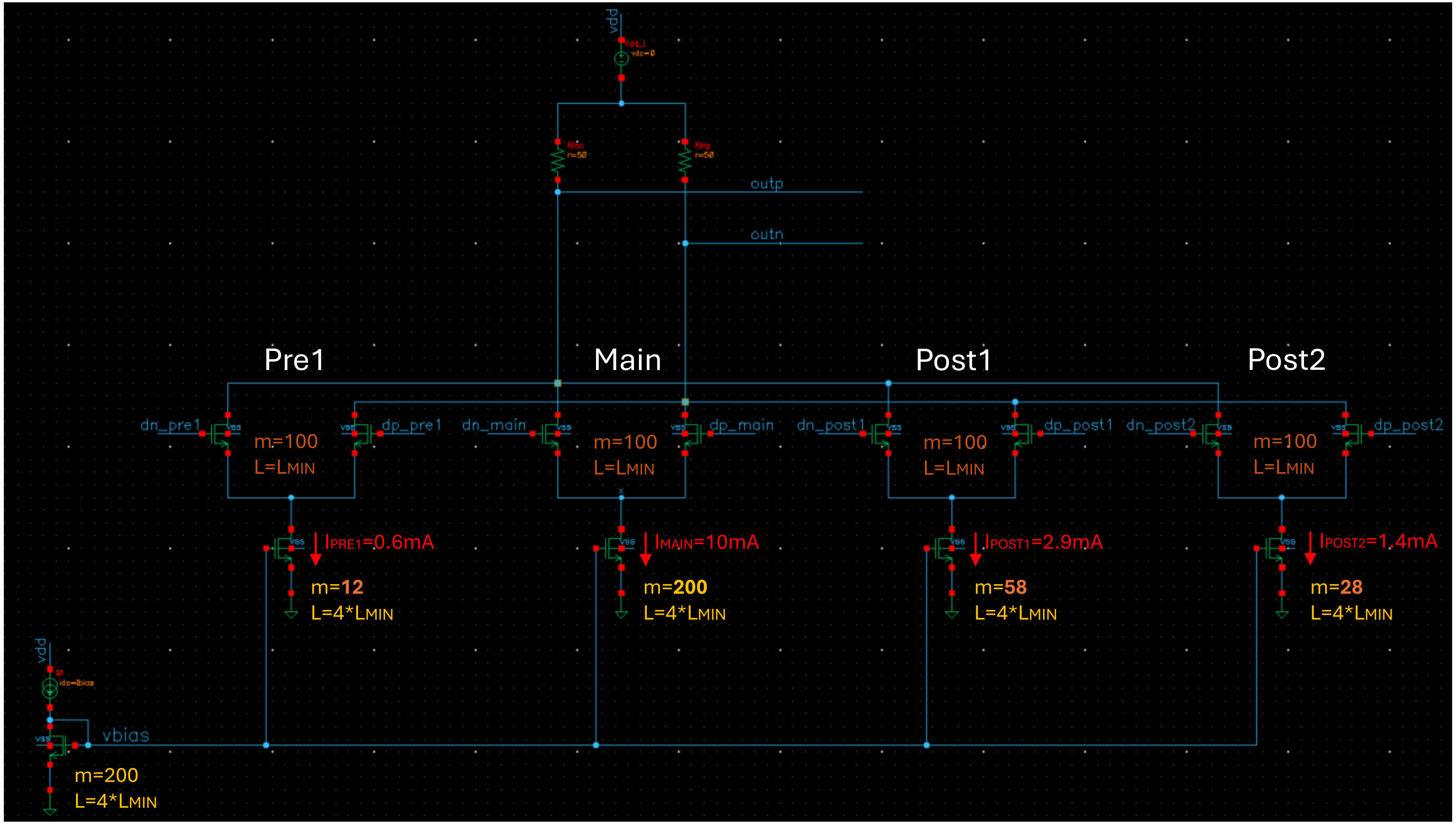
Post-Cursor 2

Flipflops used as delay cells

XOR gates used to apply the sign to the cursor taps

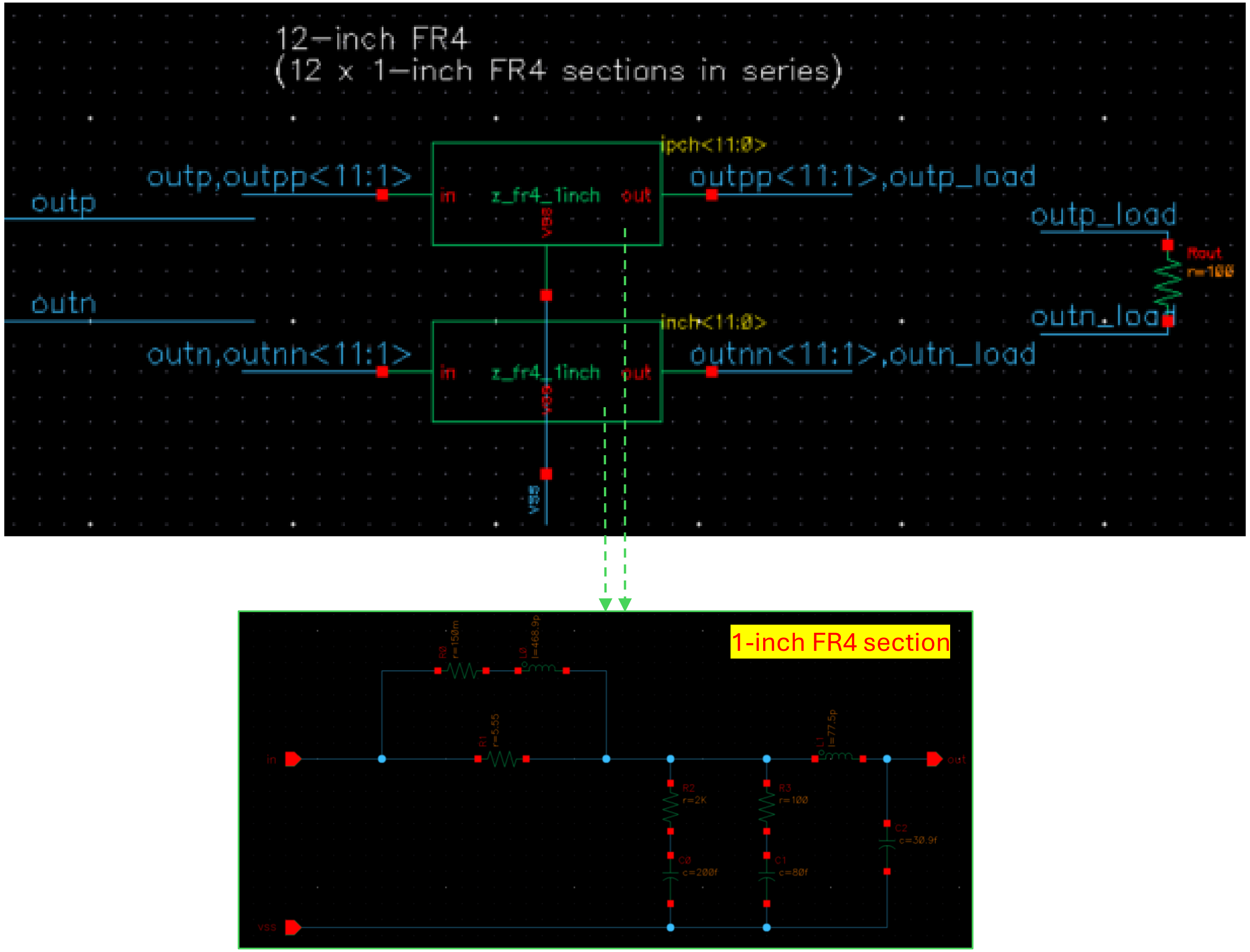
Schematics

B) CML Driver:



Schematics

C) Channel & Load:

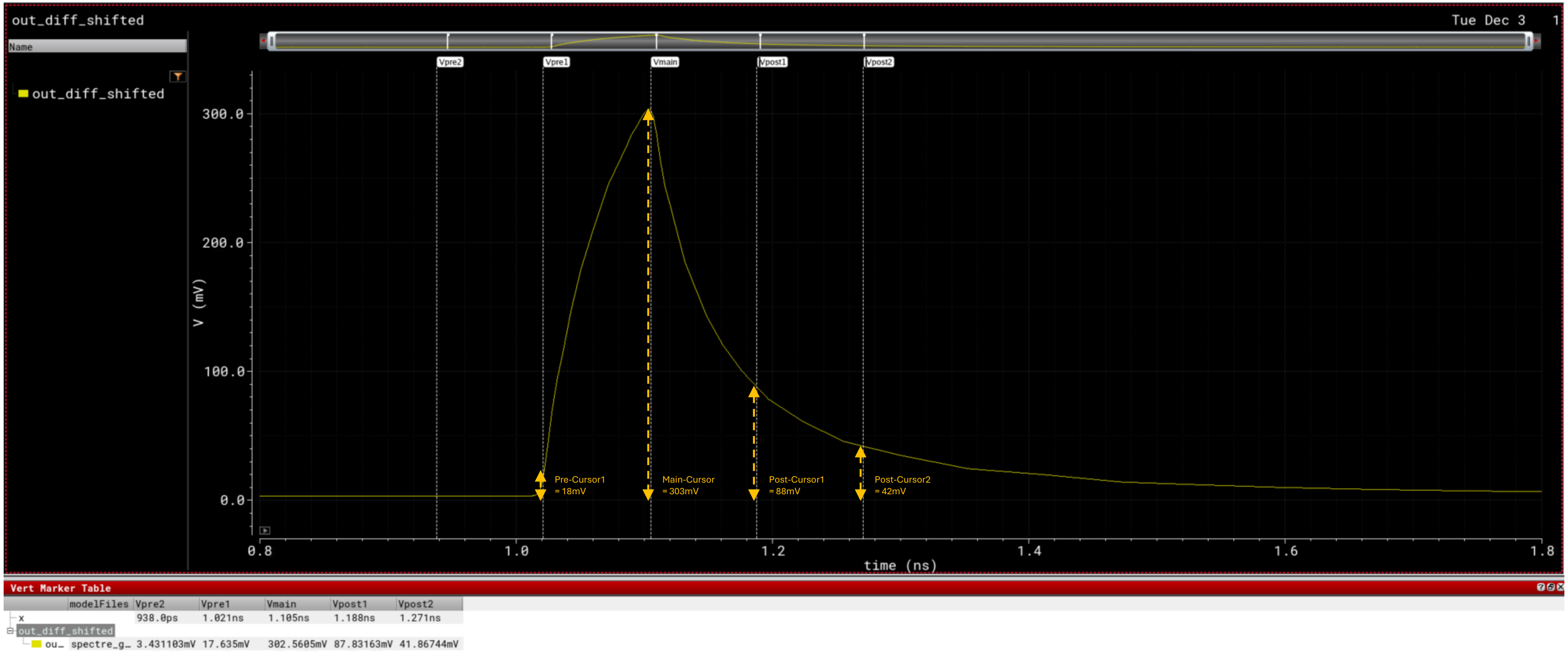


Simulation Results

A) Pulse Response:

(Without Equalization)

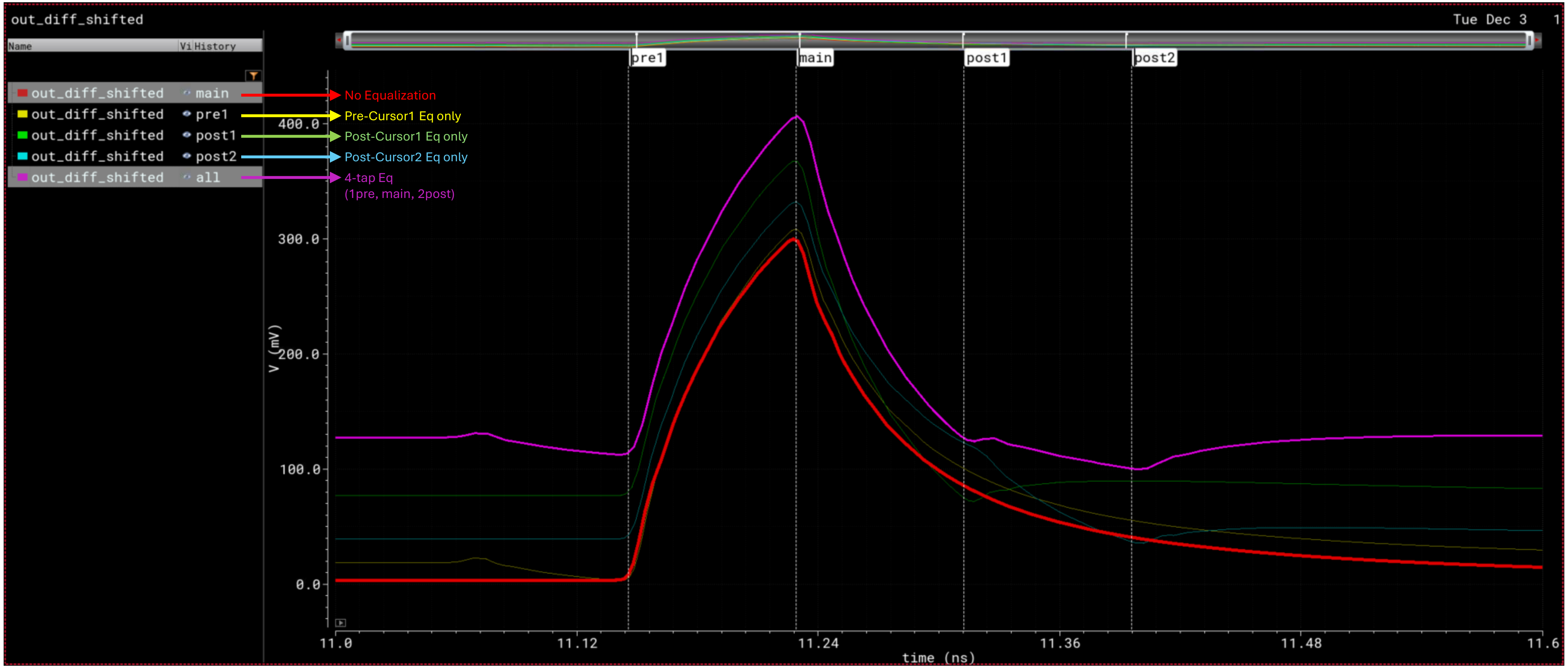
	Pre-Cursor1	Main-Cursor	Post-Cursor1	Post-Cursor2
Adjusted VSWING(PK2PK)	(18 / 303) * 500 mV = **29.7 mV**	(303 / 303) * 500 mV = **500 mV**	(88 / 303) * 500 mV = **145.2 mV**	(42 / 303) * 500 mV = **69.3 mV**
Equivalent IBIAS	29.7 mV / 50 Ohms = **0.6 mA**	500 mV / 50 Ohms = **10 mA**	145.2 mV / 50 Ohms = **2.9 mA**	69.3 mV / 50 Ohms = **1.4 mA**
# of fingers	**(m = 12)**	**(m = 200)**	**(m = 58)**	**(m = 28)**



Simulation Results

A) Pulse Response:

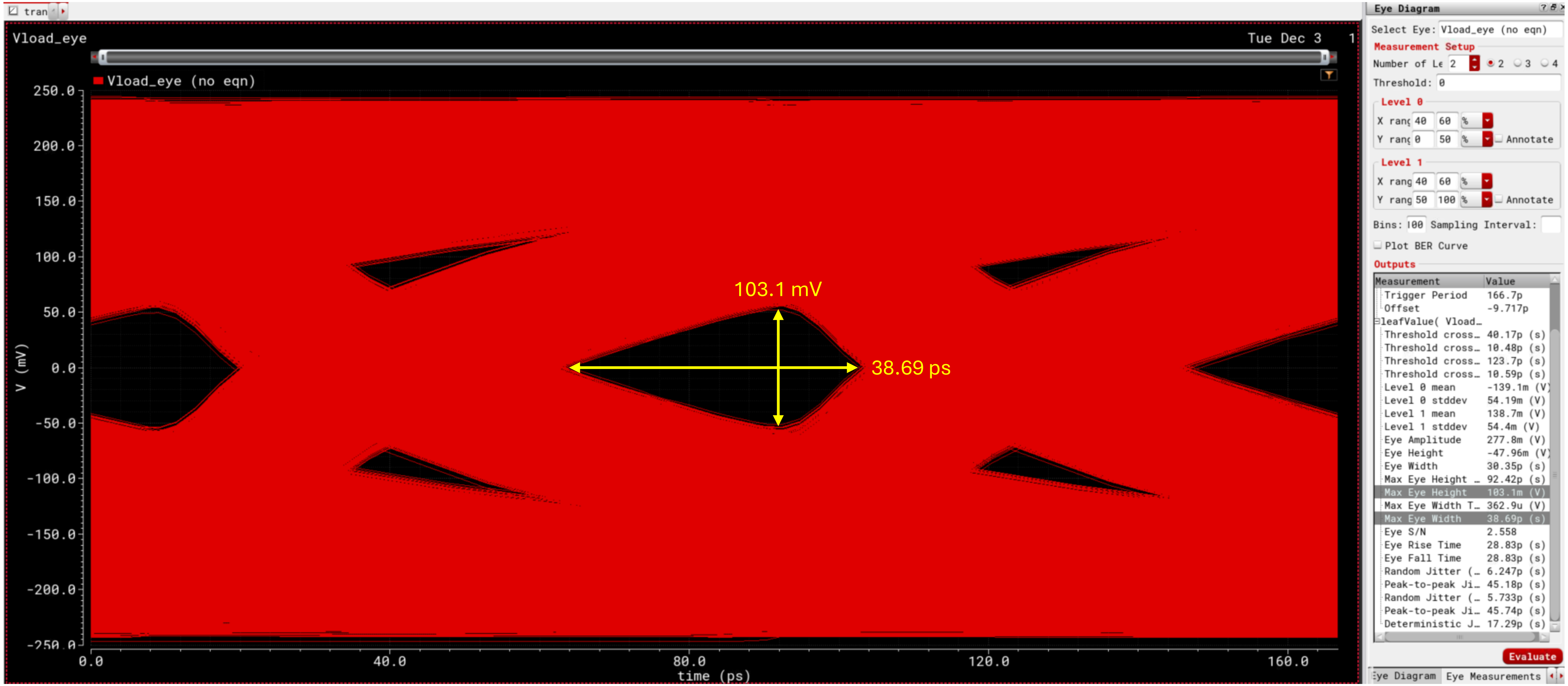
(With Equalization)



Simulation Results

B) Eye Diagram:

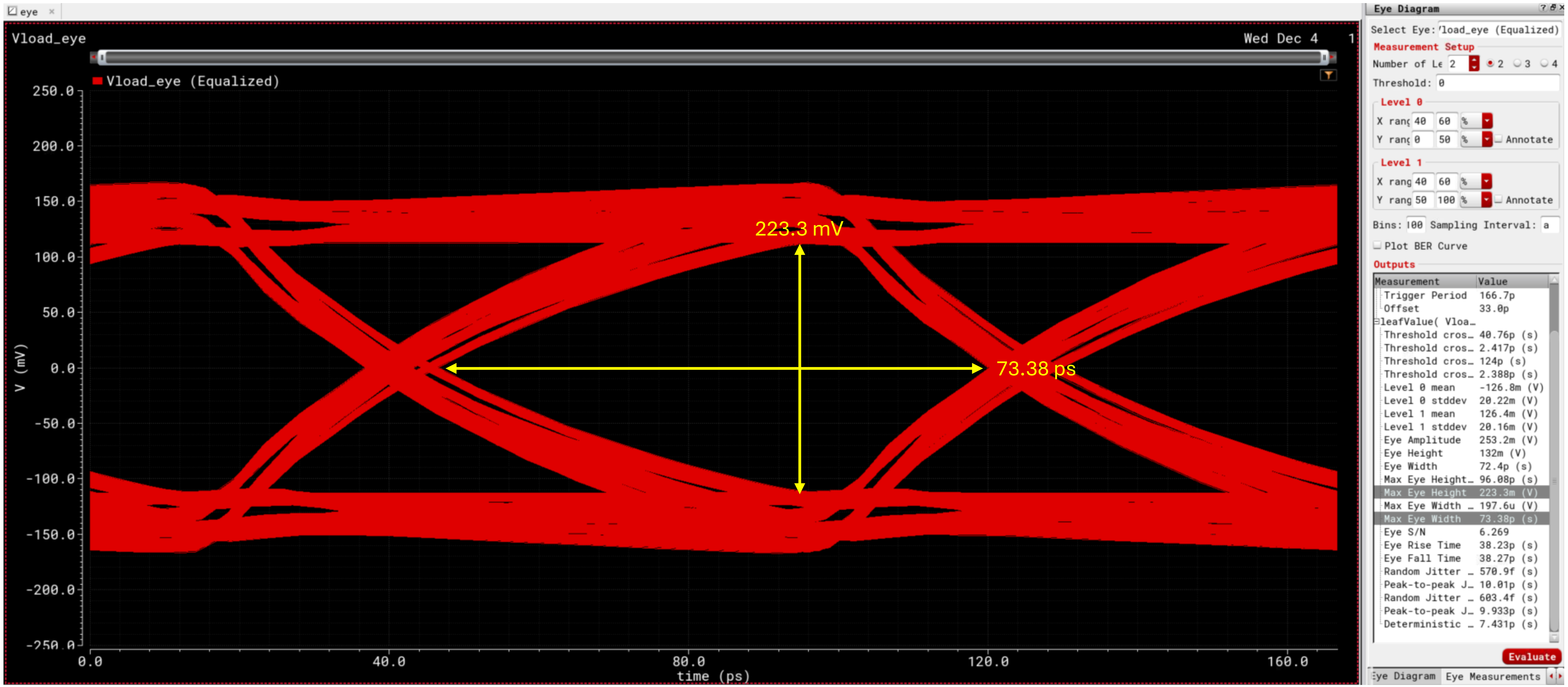
(Without Equalization)



Simulation Results

B) Eye Diagram:

(With Equalization)



Simulation Results

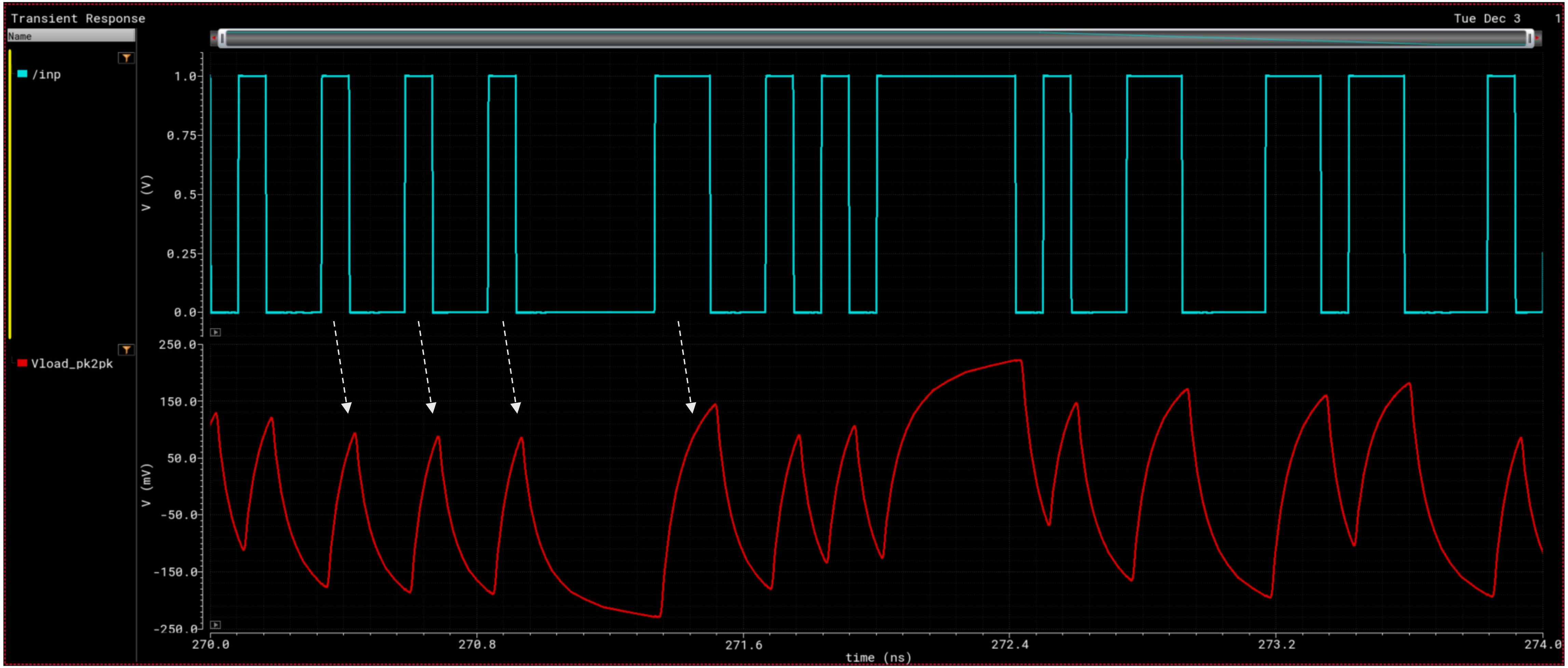
B) Eye Diagram:

	No Equalization	With Equalization (4-tap)
Eye Height (Max)	**103.1 mV**	**223.3 mV**
Eye Width (Max)	**38.69 ps**	**73.38 ps**
Swing (PK2PK)	**500 mV** (–250mV ~ +250mV)	**328 mV** (–164mV ~ +164mV)

Simulation Results

C) Transient Waveforms:

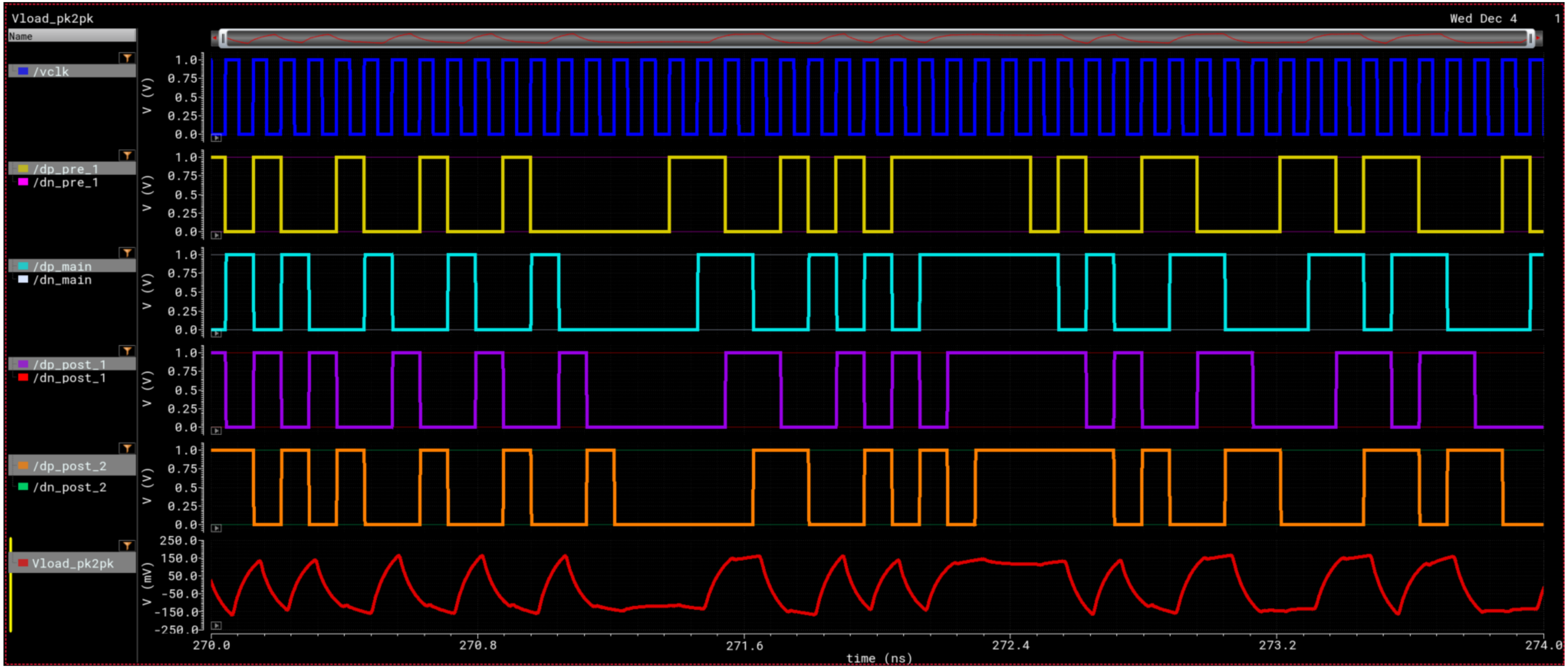
(Without Equalization)



Simulation Results

C) Transient Waveforms:

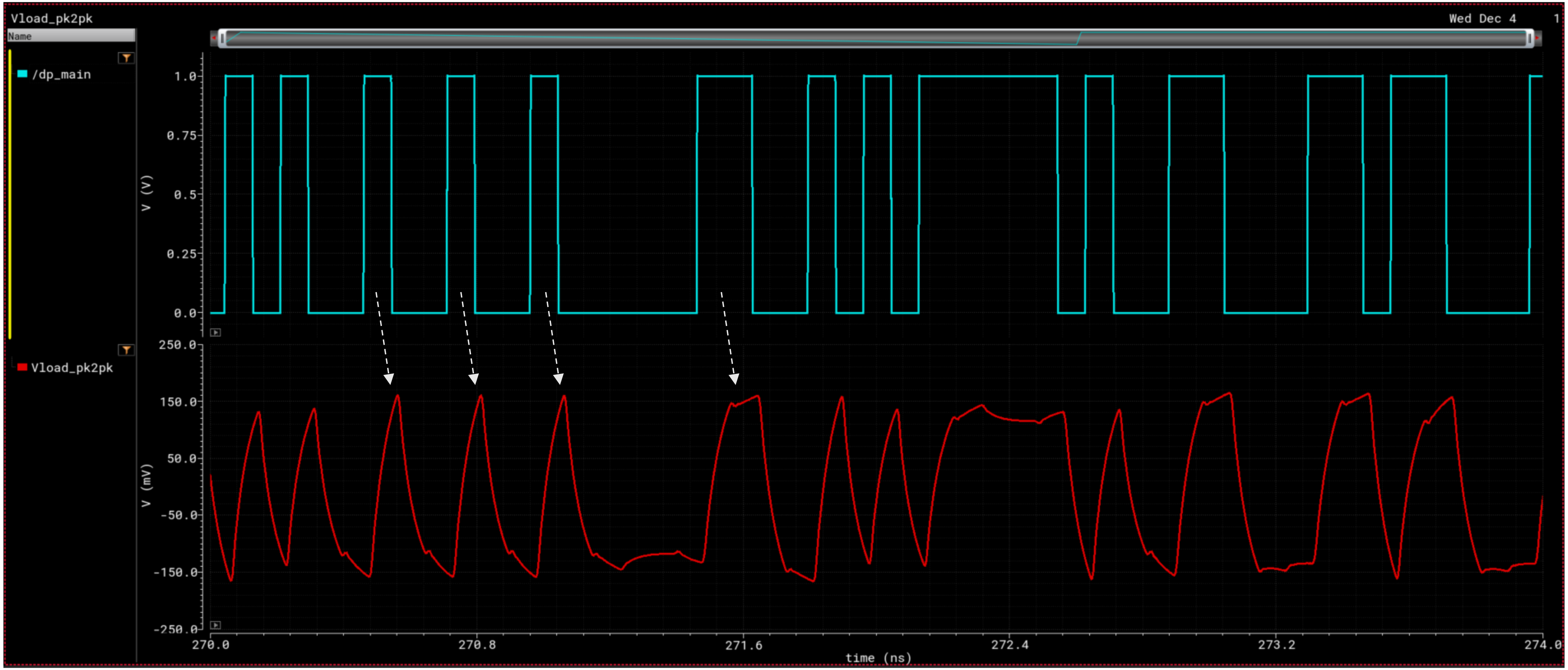
(With Equalization)



Simulation Results

C) Transient Waveforms:

(With Equalization)



Conclusion

- This project shows the design procedure of a TX FIR Equalizer for a 12 Gb/s input & a channel of 12-inch FR4.
- It also shows how the equalization improves the eye opening of the output, while paying the price of lower swing amplitude & increased latency.