TX FIR Equalizer

12 Gbps

(Eye Diagram)

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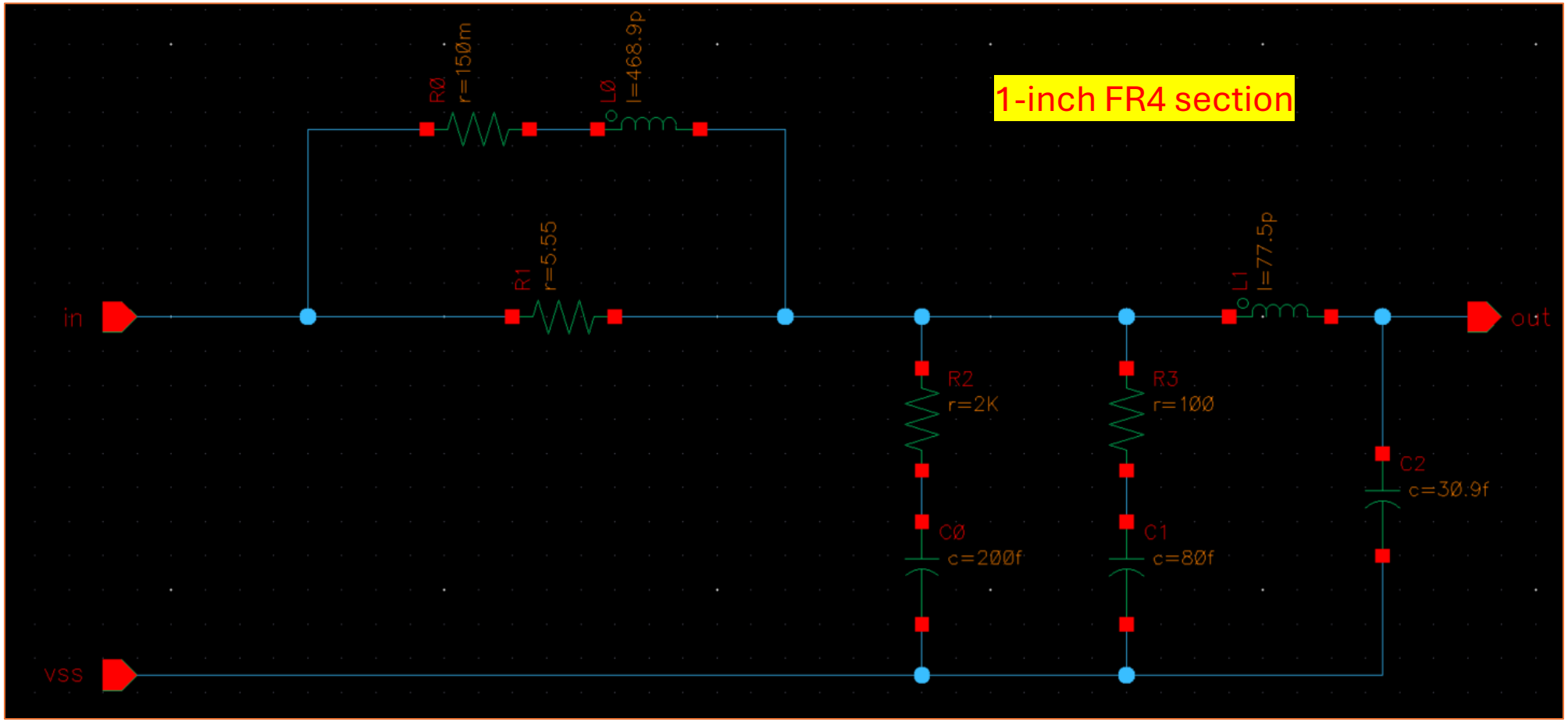
Design Parameters

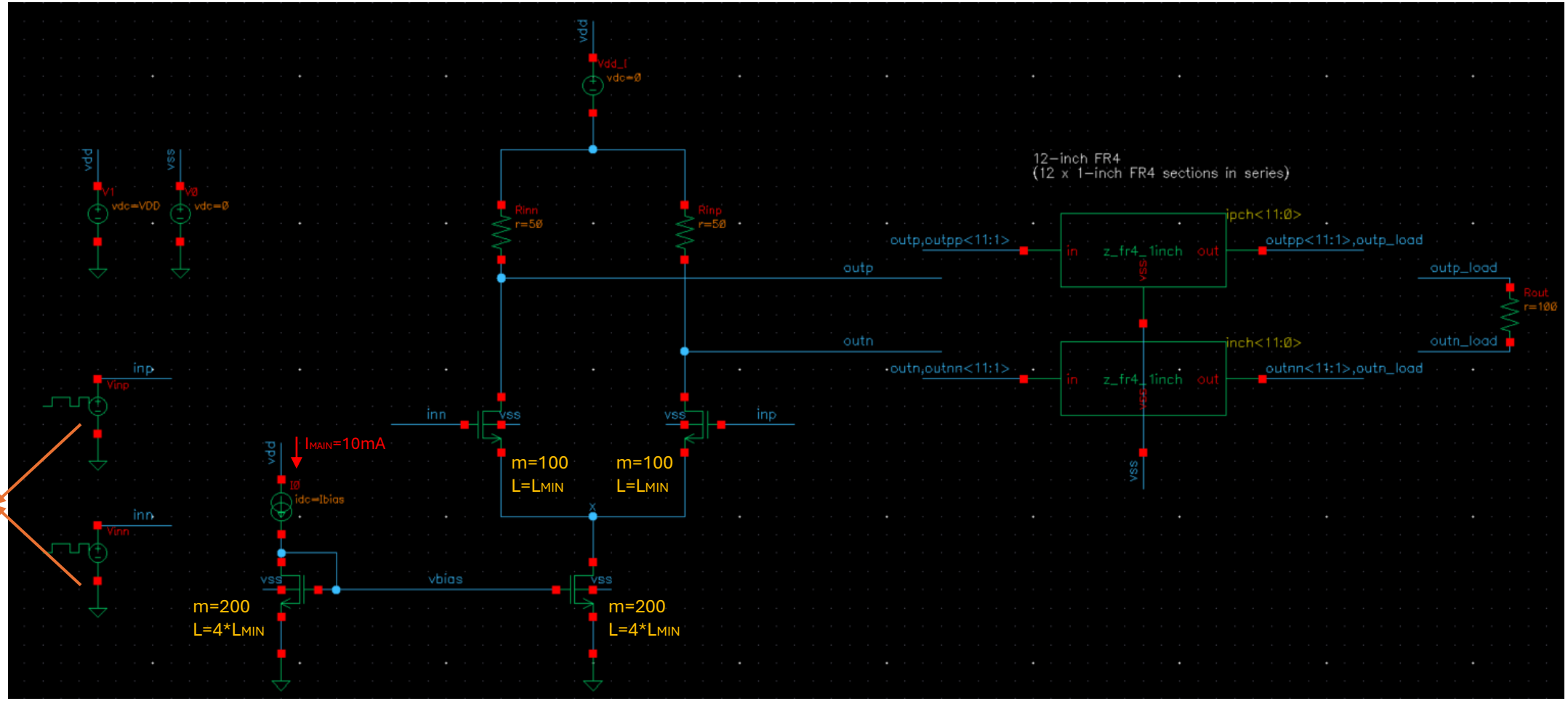
Parameter	Value
Data Rate	12 Gb/s
VDD	1 V
Tx-Driver	Current Mode (CML)
$V_{SWING\ (PK2PK)}$	0.5 V
I_{BIAS}	10mA
Channel	12-inch FR4

Channel = 12 x 1-inch FR4 section



1) Eye Diagram (without Equalization)

TB Schematics



LIB: **analogLib**
CELL: **vprbs**

Zero value: **0 V** / 1 V
One value: **1 V** / 0 V
Bit period: **83.33ps (1/12G)**
Rise/Fall times: **2.5 ps**
Edge type: **linear**
Trigger: **Internal**
LFSR Mode: **PN32**

Analysis Setup

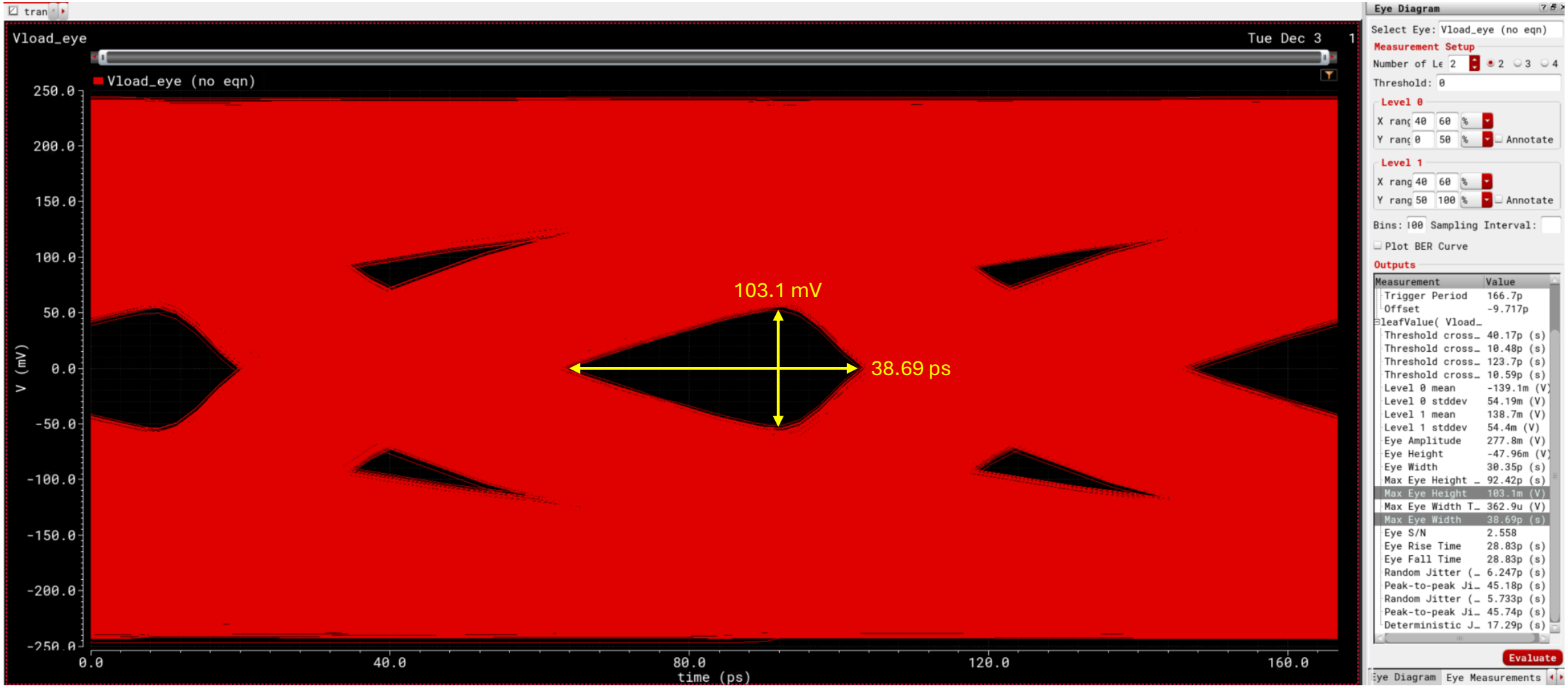
Name	Value
Filter	Filter
Tests	
eye	
Simulator	spectre
Analyses	
tran	0 VAR("sim_time")
Click to add analysis	
Design Variables	
Click to add test	
Global Variables	
sim_time	2000n
VDD	1
Data_rate	12G
Vsw_pk2pk	500m
Ibias	10m

Eye Diagram

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
*** Voltages ***	expr		point
	signal	/inp	point
	signal	/inn	point
	signal	/outp	point
	signal	/outn	point
	signal	/outp_load	point
	signal	/outn_load	point
	signal	/x	point
	signal	/vbias	point
*** Currents ***	expr		point
/Vdd_I/PLUS_I	signal …	/Vdd_I/PLUS	point
/Rout/PLUS_I	signal …	/Rout/PLUS	point
*** Outputs ***	expr		point
Vtxout_pk2pk	expr	(VT("/outp") - VT("/outn"))	point
Vtxout_eye	expr	eyeDiagram(Vtxout_pk2pk 0 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
Vload_pk2pk	expr	(VT("/outp_load") - VT("/outn_load"))	point
Vload_eye	expr	eyeDiagram(Vload_pk2pk 0 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point

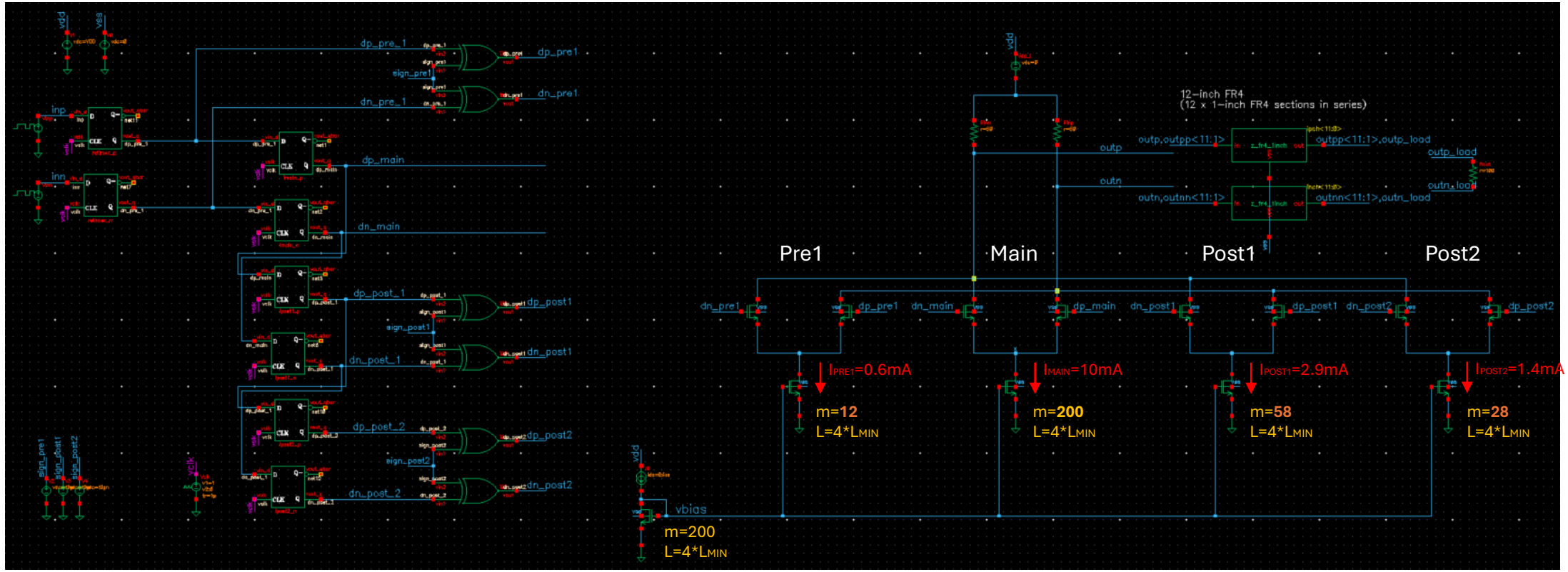
Eye Diagram

Measurements → Eye Diagram



2) Eye Diagram
(with Equalization)

TB Schematics



TB Schematics

$T_{UI} = 83.33ps$
(Datarate = $^{1}/_{UI}$ = 12Gb/s)

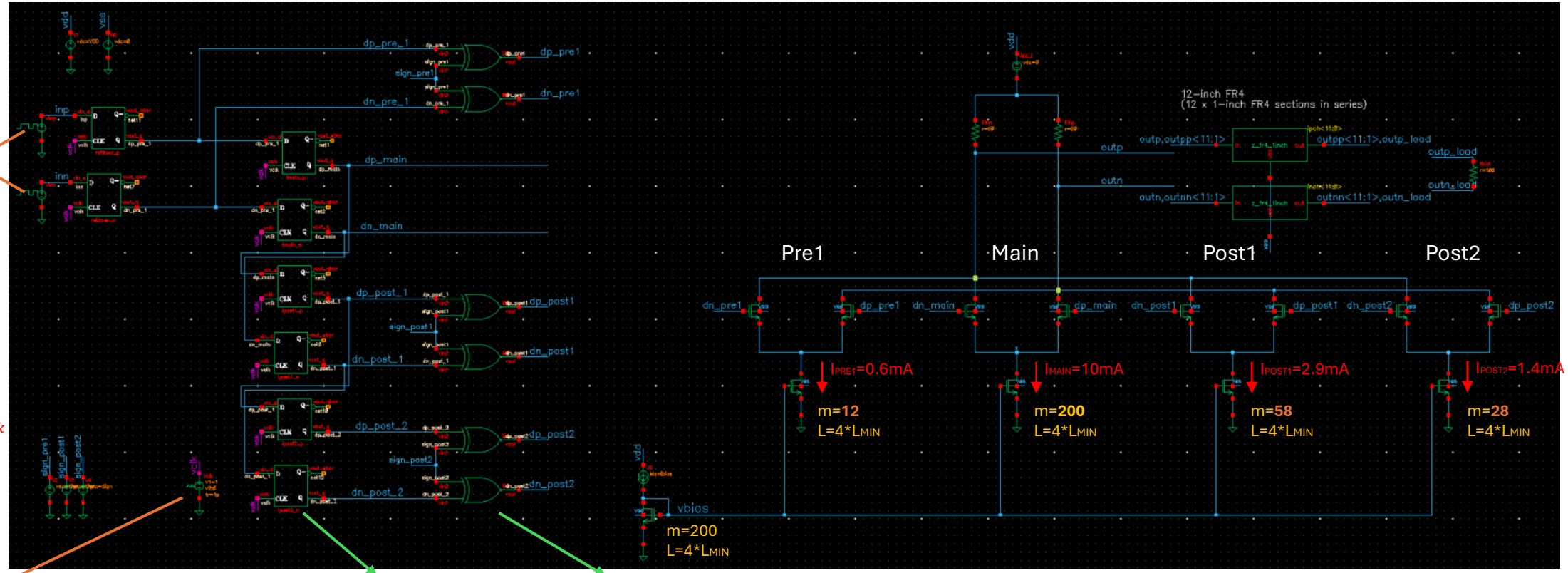
LIB: **analogLib**
CELL: **vprbs**

Zero value: **0 V** / 1 V
One value: **1 V** / 0 V
Bit period: **83.33ps (1/12G)**
Rise/Fall times: **2.5 ps**
Edge type: **linear**
Trigger: **Internal**
LFSR Mode: **PN32**

$T_{clk} = 83.33ps$
(Data is sampled every T_{clk} = every rising edge)

LIB: **analogLib**
CELL: **vpulse**

Voltage1: **1 V**
Voltage2: **0 V**
Period: **83.33ps (1/12G)**
Rise/Fall times: **1 ps**
Pulse width: **41.67ps (0.5/12G)**



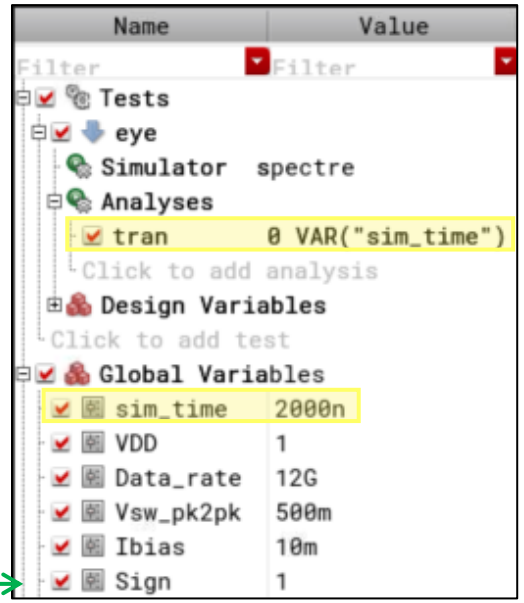
LIB: **ahdlLib**
CELL: **d_ff**

Vlogic_high/low: **1/0**
Vtrans_clk/Vtrans: **0.5**
tdel: 1f
Rise/Fall times: **2.5 ps**

LIB: **ahdlLib**
CELL: **xor_gate**

Vlogic_high/low: **1/0**
Vtrans: **0.5**
tdel: 1f
Rise/Fall times: **2.5 ps**

Analysis Setup



Eye Diagram

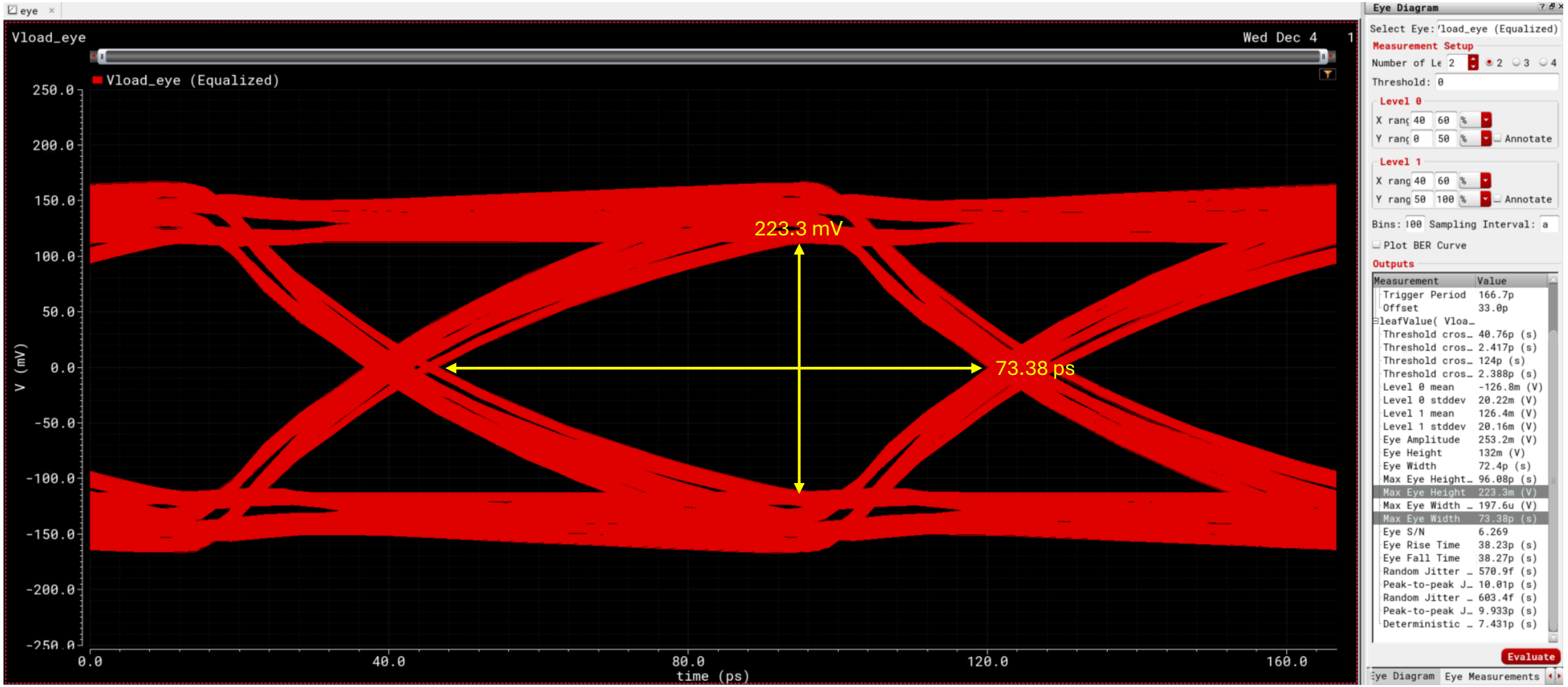
* The Sign bit of the XOR gates is set to 1, to subtract the cursor values from the main waveform.

Name	Type	Details	EvalType
Filter	Filter	Filter	Filter
*** Voltages ***	expr		point
	signal	/inp	point
	signal	/inn	point
	signal	/outp	point
	signal	/outn	point
	signal	/outp_load	point
	signal	/outn_load	point
	signal	/x	point
	signal	/vbias	point
*** Currents ***	expr		point
/Vdd_I/PLUS_I	signal …	/Vdd_I/PLUS	point
/Rout/PLUS_I	signal …	/Rout/PLUS	point
*** Outputs ***	expr		point
Vtxout_pk2pk	expr	(VT("/outp") - VT("/outn"))	point
Vtxout_eye	expr	eyeDiagram(Vtxout_pk2pk 1e-08 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
Vload_pk2pk	expr	(VT("/outp_load") - VT("/outn_load"))	point
Vload_eye	expr	eyeDiagram(Vload_pk2pk 1e-08 VAR("sim_time") (2 * (1 / VAR("Data_rate"))) ?autoCenter t)	point
*** FIR ***	expr		point
	signal	/dp_pre_1	point
	signal	/dn_pre_1	point
	signal	/dp_main	point
	signal	/dn_main	point
	signal	/dp_post_1	point
	signal	/dn_post_1	point
	signal	/dp_post_2	point
	signal	/dn_post_2	point
	signal	/vclk	point

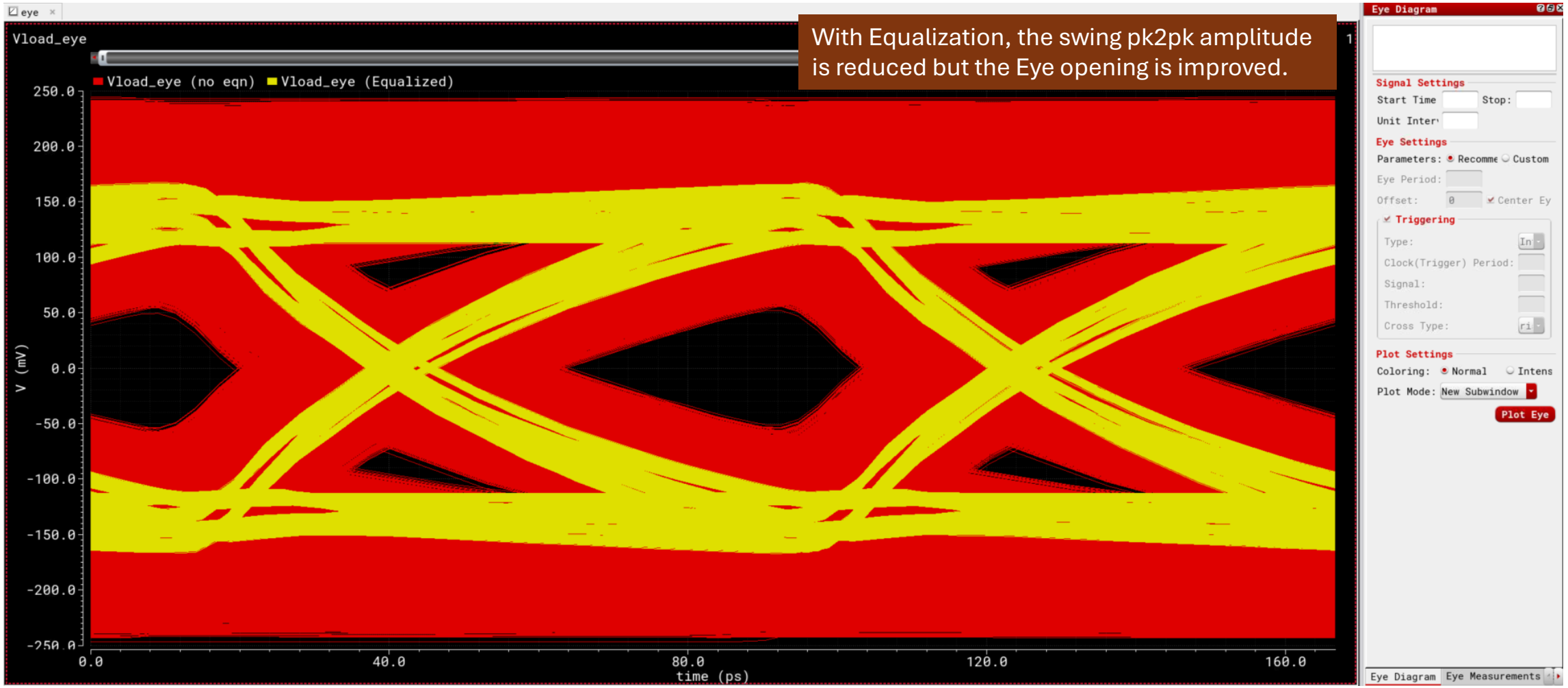
* Delay time of 10ns is added to remove any settling time issues at the beginning of the simulation.

Eye Diagram

Measurements → Eye Diagram



Eye Diagram (Comparison)



Eye Diagram (Comparison)

	No Equalization	With Equalization (4-tap)
Eye Height (Max)	**103.1 mV**	**223.3 mV**
Eye Width (Max)	**38.69 ps**	**73.38 ps**
Swing (PK2PK)	**500 mV** (–250mV ~ +250mV)	**328 mV** (–164mV ~ +164mV)