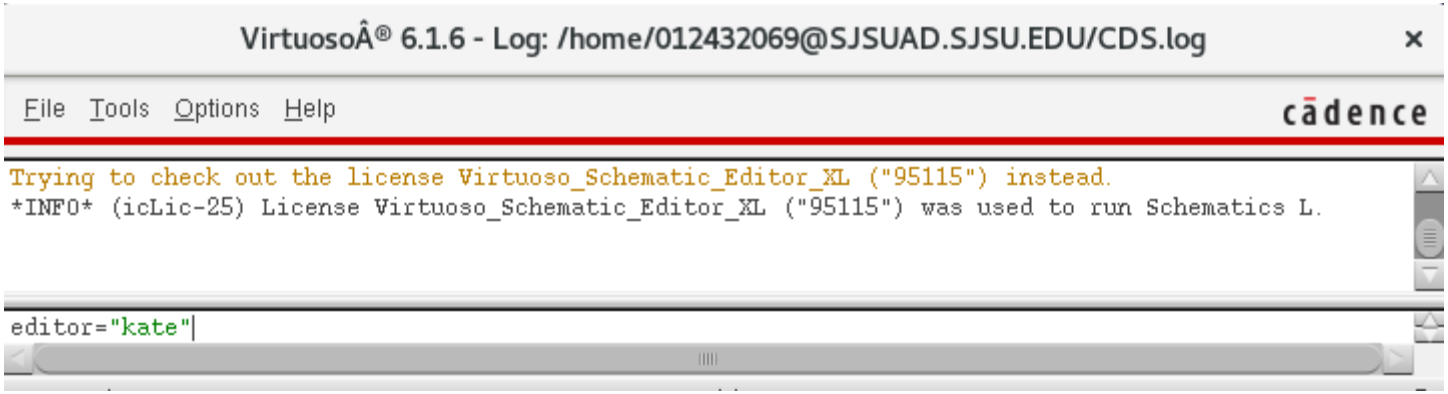
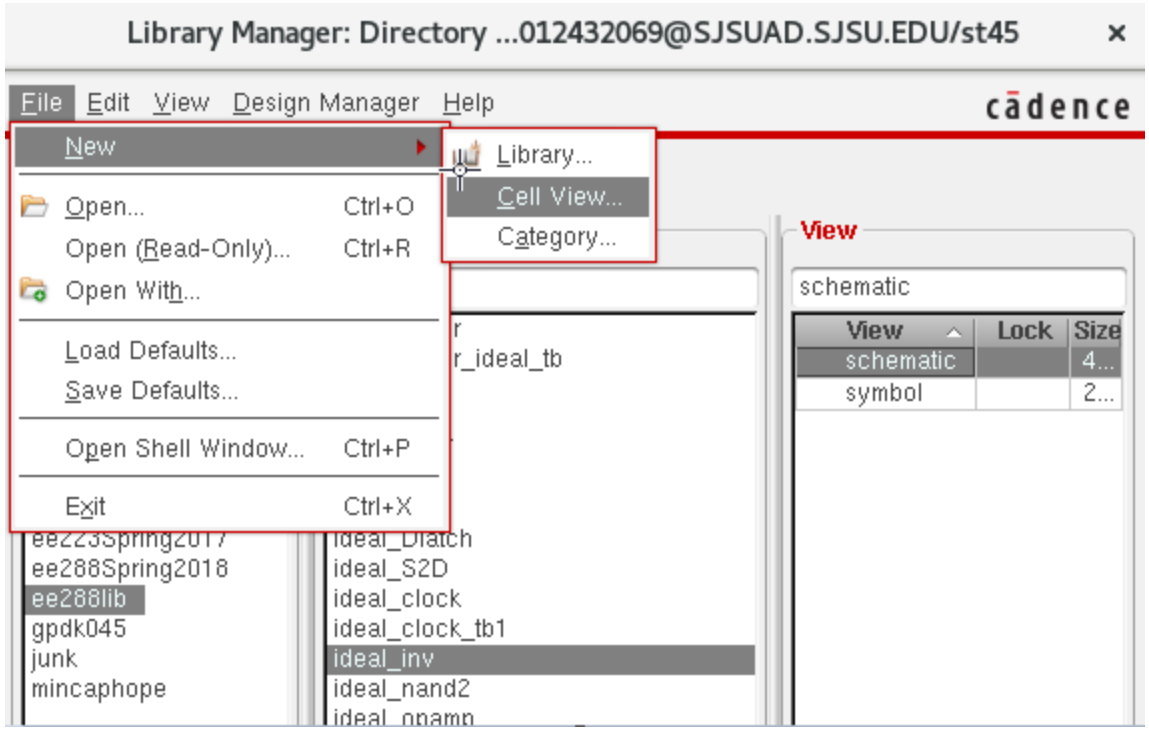
Creating Veriloga View

- In CIW window, type
  editor="kate"



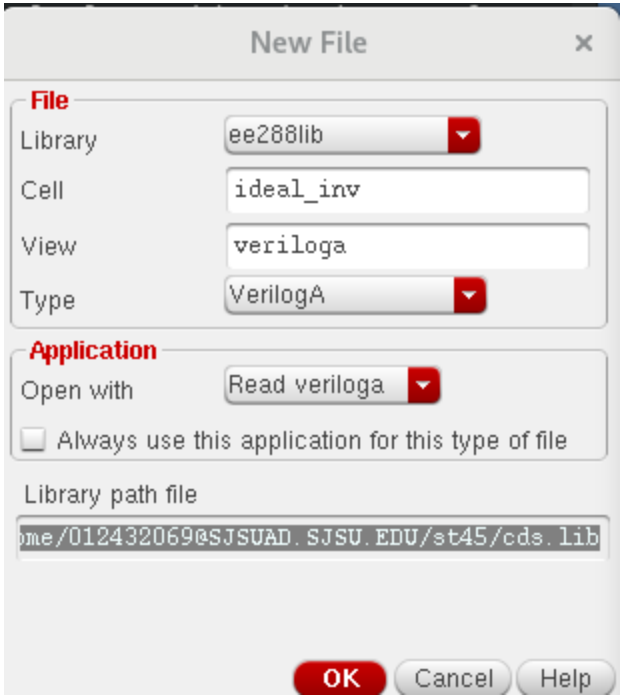
Creating Veriloga View

- From Library Manager, File->New->Cell View



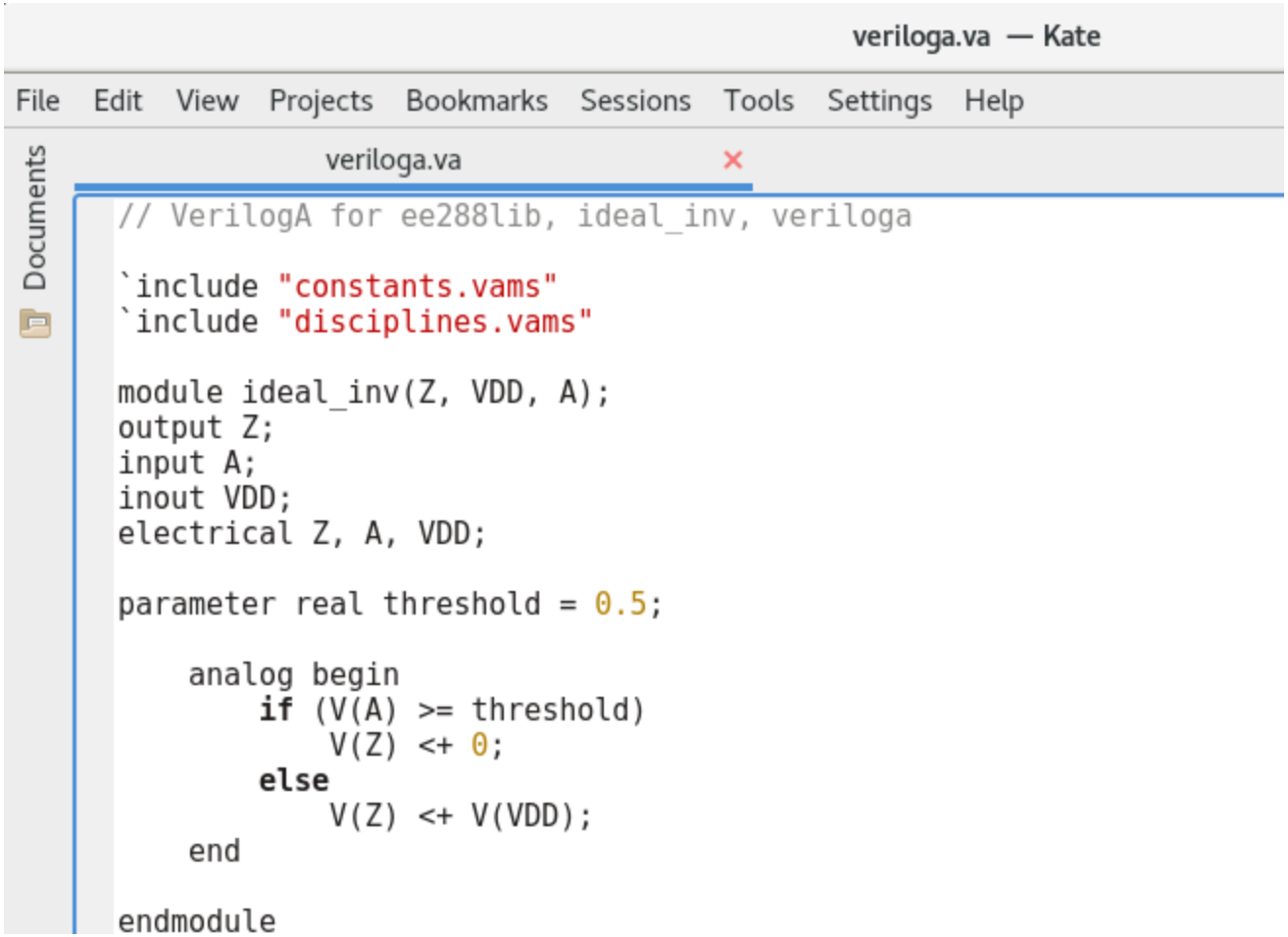
Creating Veriloga View

- Fill out the form like this



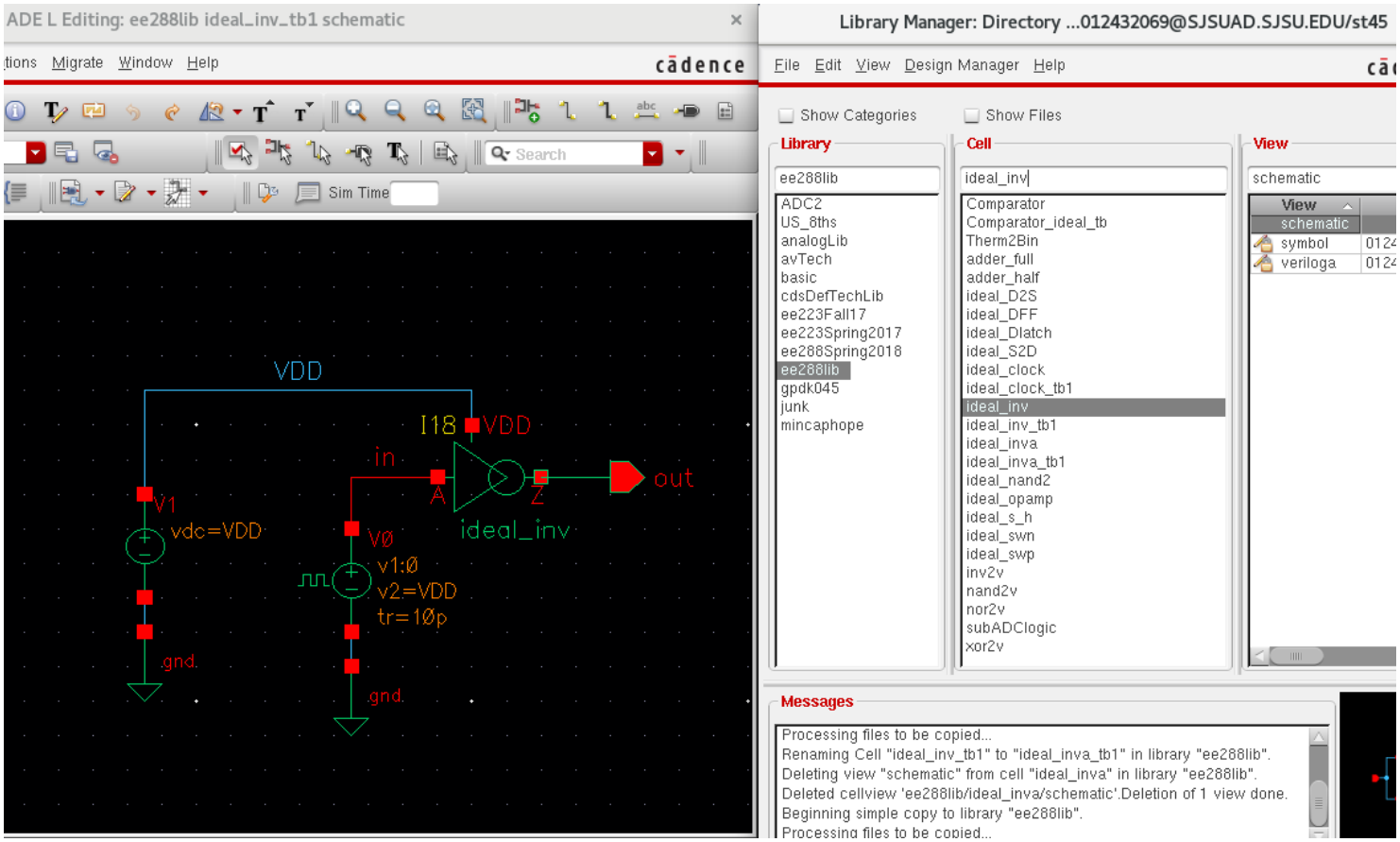
Creating Veriloga View

- In the editor, write a code like below example



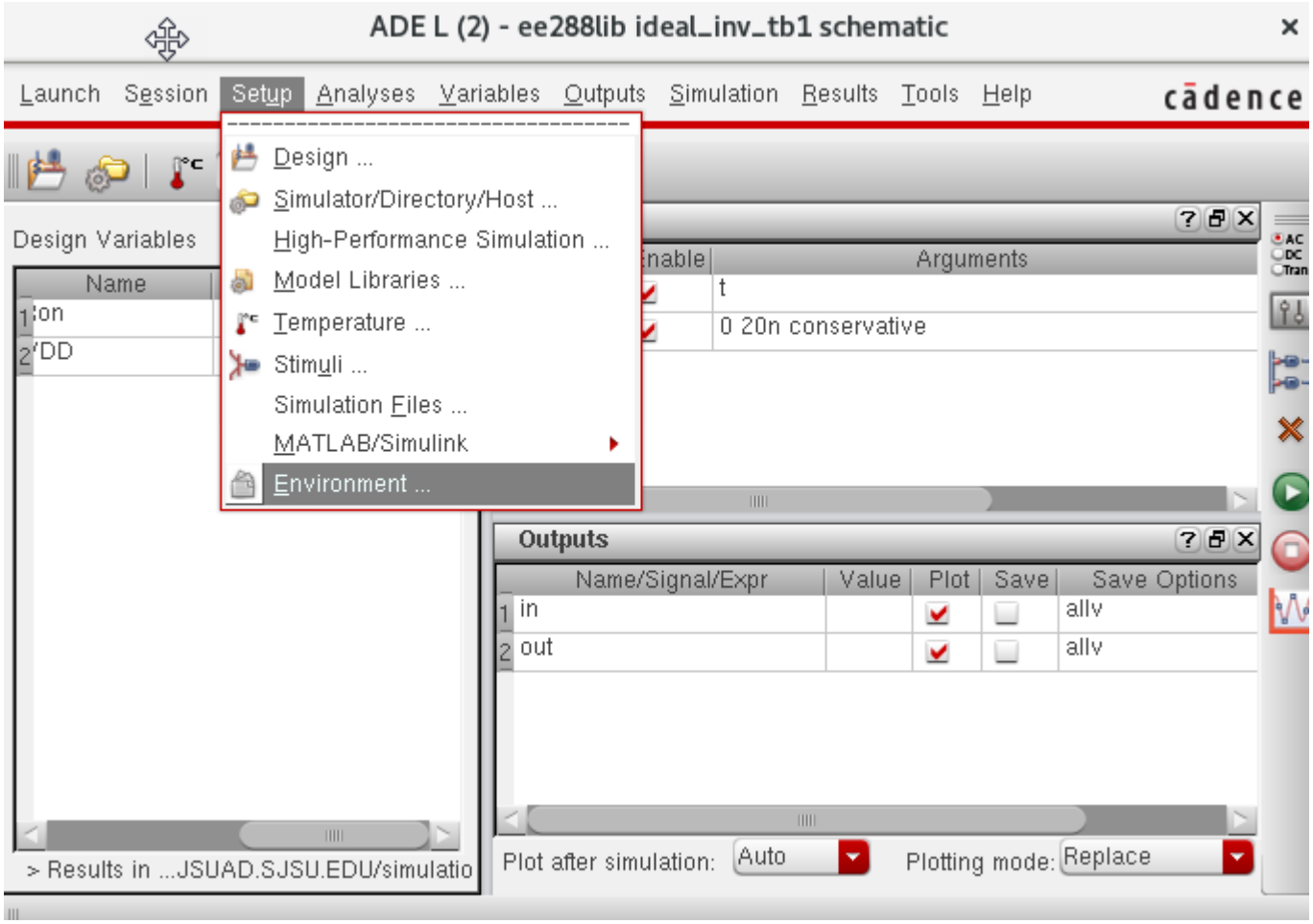
Running Simulation Using Verilog View

- Check the following test bench “ideal_inv_tb1” in ee288lib



Running Simulation Using Verilog View

- In ADL L window, choose Setup->Environment



Running Simulation Using Verilog View

- Rearrange the Switch View List so that veriloga comes before schematic -> verloga view will be used in simulation