

## *EE141-Spring 2010 Digital Integrated Circuits*

### Lecture 28 Perspectives

EECS141

Lecture #28

1

## *Administrivia*

- Hw 8 due Today
- Hw 9 posted
  - Do not turn in, will not be graded
- Project Poster Presentations Next We 1-6pm
  - Signup via Doodle (Friday) – Use the following link:  
<http://www.doodle.com/q6ri23aqub4dywwq>
- Final:
  - Tuesday May 11, 11:30am-2:30pm, 127 Dwinelle
  - Review Session: Monday May 10, 6pm, TBD
- Today: HKN class evaluation

EECS141

Lecture #28

2



## Digital Design - Where does it go from here?

EECS141

Lecture #28

3

## Technology Outlook

High Volume Manufacturing	2008	2010	2012	2014	2016	2018	2020	2022
Technology Node (nm)	45	32	22	16	11	8	6	4
Integration Capacity (BT)	8	16	32	64	128	256	512	1024
Delay Scaling	>0.7				~1?			
Energy Scaling	~0.5				>0.5			
Transistors	Planar				3D, FinFET			
Variability	High				Extreme			
ILD	~3				towards 2			
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	8-9				0.5 to 1 Layer per generation			

## THE OPTIMISTIC PERSPECTIVE

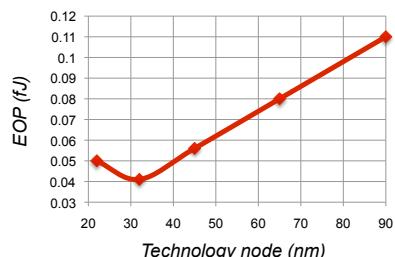
EECS141

Lecture #28

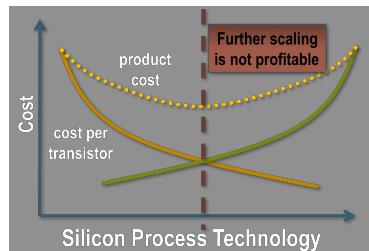
4

**Many good reasons why CMOS may not scale far below 22nm ...**

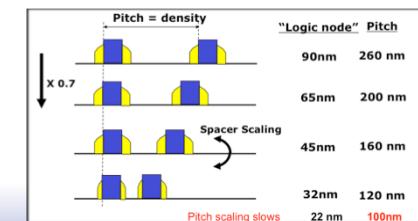
□ Energy!



○ Cost

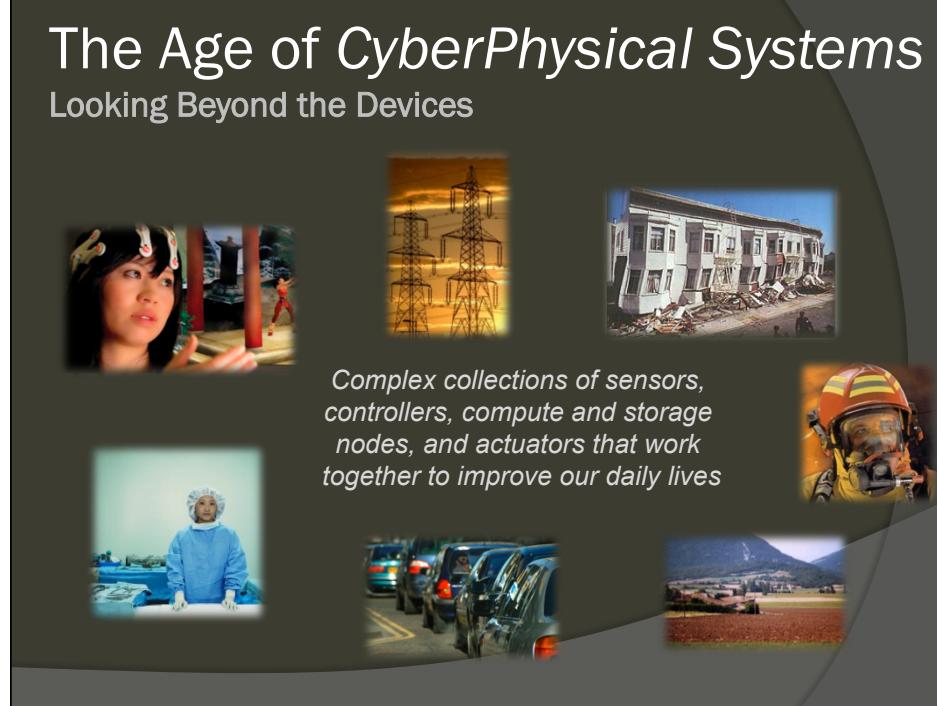


○ Size



**Maybe Moore's law as we know it may end**

**... yet there are plenty of interesting challenges and huge opportunities!!**

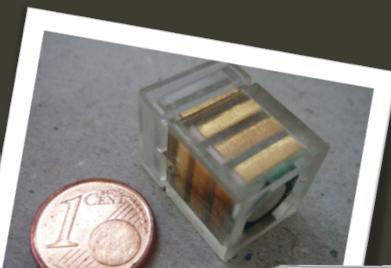


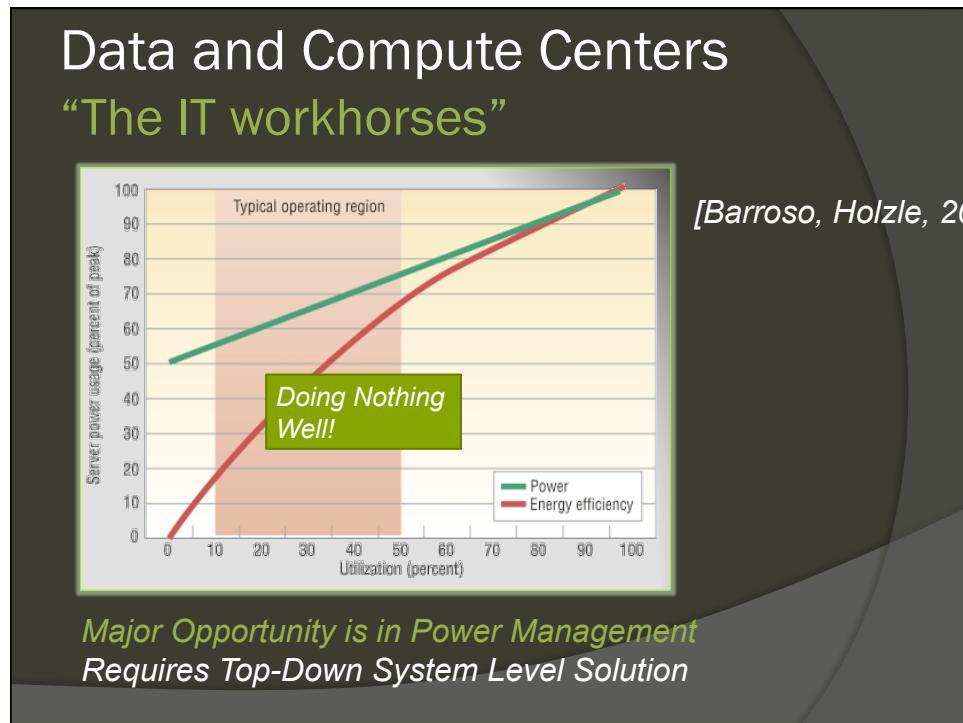
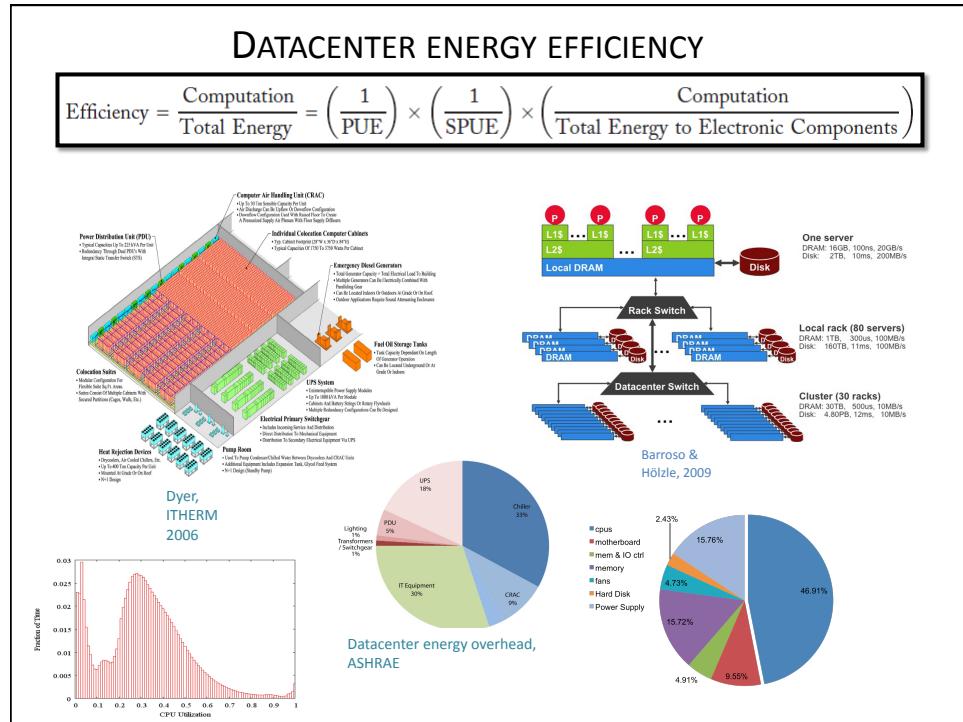
## It's All About Energy



*Energy among the most compelling concerns of distributed IT platform and its applications  
Intelligent energy management at ALL LEVELS AND SCALES offers tremendous opportunity.*

## It Is All About Energy ...

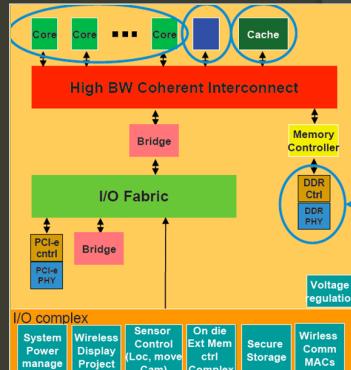




## Mobiles

“The home of the user interface”

- Most “tricks” already in use! (multi-core, heterogeneity, accelerators, SoC, ...)
- Opportunity: system and application considerations
  - Always-connected*
  - Perceptual processing

Mobile  $\mu$ Proc Anno 2015  
[Courtesy A. Peleg, Intel]

## The Sensory Swarm

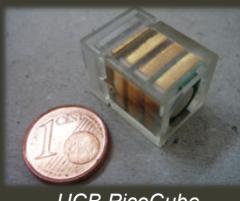
“Adding senses to the Internet”



Philips Sand module



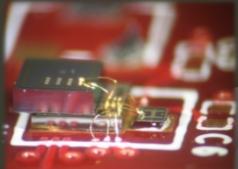
Telos Mote



UCB PicoCube



IMEC e-Cube

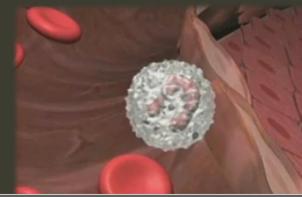
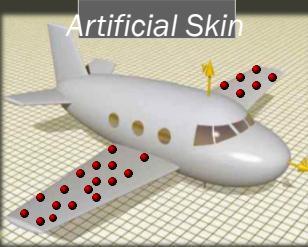


UCB  $mm^3$  radio

*The driver for Ultra-Low Energy design for past decade*

Ref: Ambient Intelligence, W. Weber Ed., 2005]

## Yet ... True Immersion Still Out of Reach Microscopic Wireless



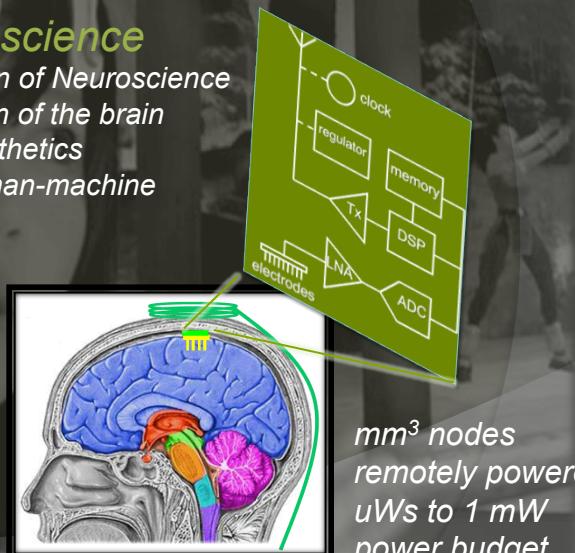
*Another leap in size, cost and energy reduction*

## Example: Microscopic Wireless to Power Brain-Machine Interfaces (BMI)

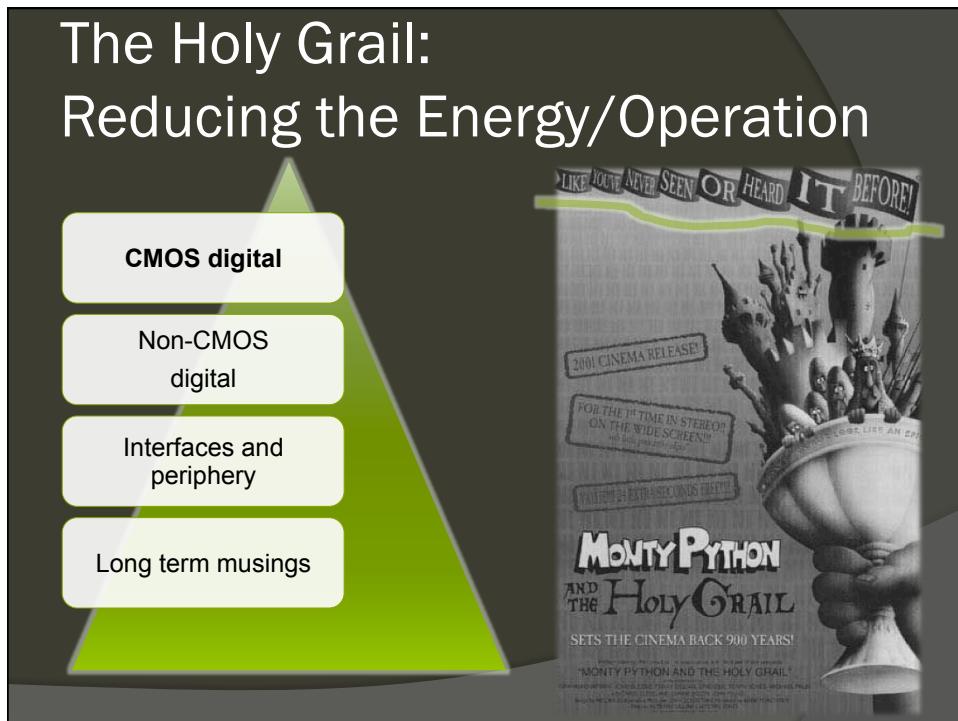
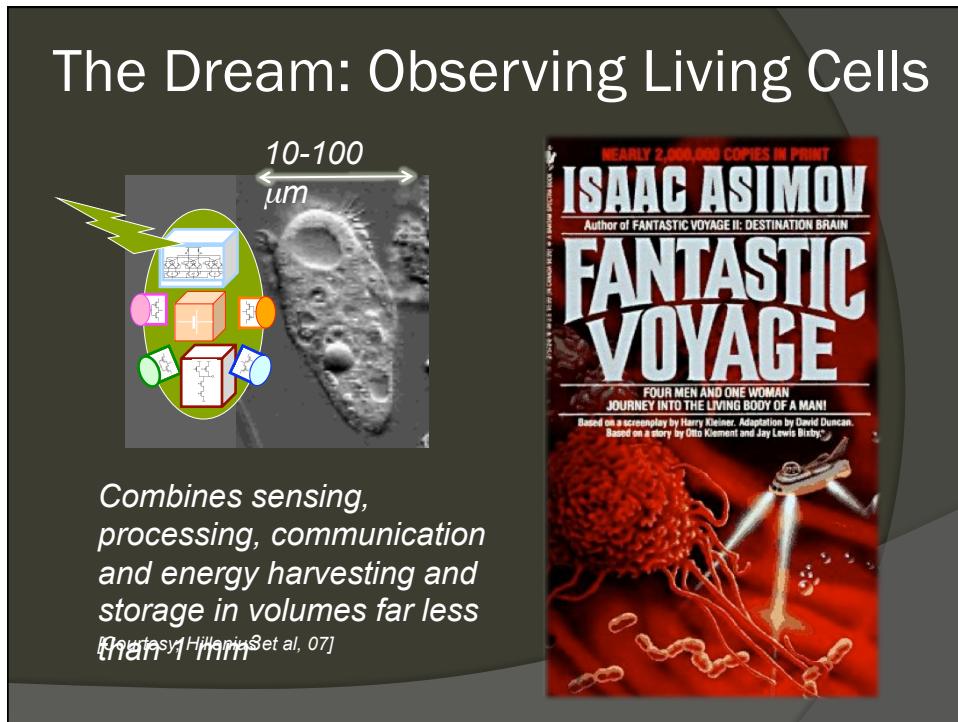
### *The Age of Neuroscience*

*BMI – The Instrumentation of Neuroscience*

- Learning about operation of the brain
- Enabling advanced prosthetics
- Enabling innovative human-machine interfaces



*mm<sup>3</sup> nodes  
remotely powered  
uWs to 1 mW  
power budget*



# Energy Limits in Digital

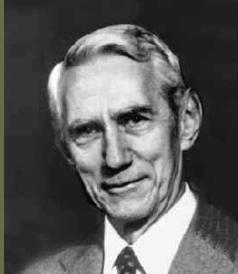


*Shannon-Von Neumann-Landauer Bound:*

*Minimum energy/operation =  $kT\ln(2)$*

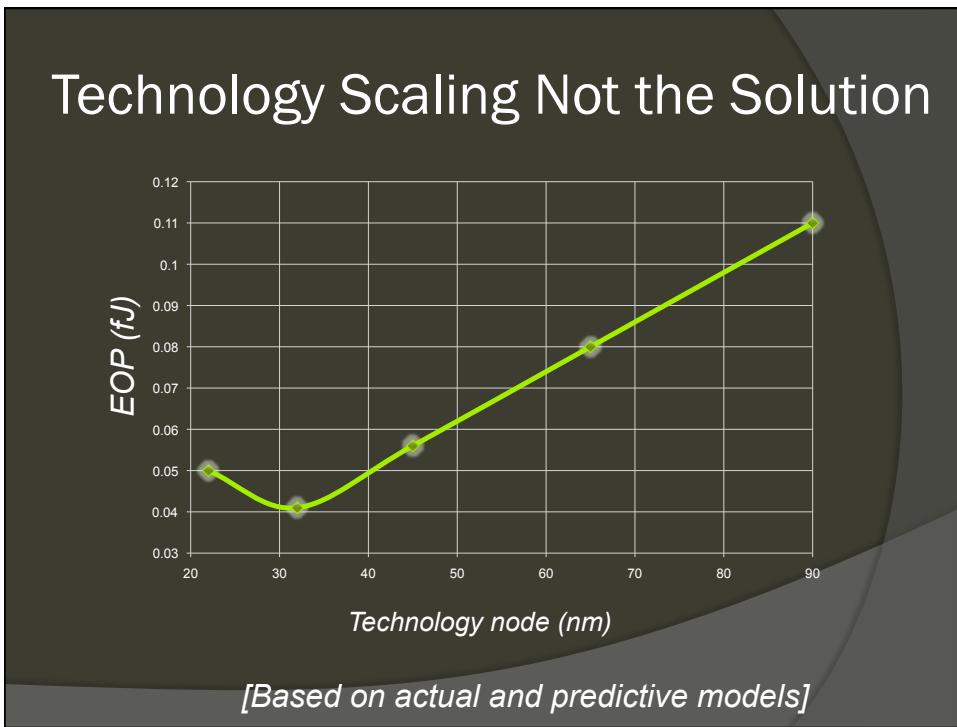
*=  $4 \cdot 10^{-21} \text{ J/bit}$  at room temperature*

*John Von Neumann*



*Claude Shannon*

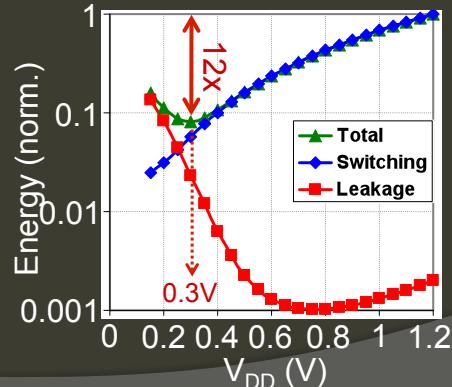
***More than 4 orders of magnitude below current practice (65 nm at 1V)***



## Lowering Supply Voltage Only Option

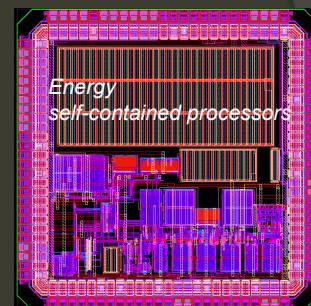
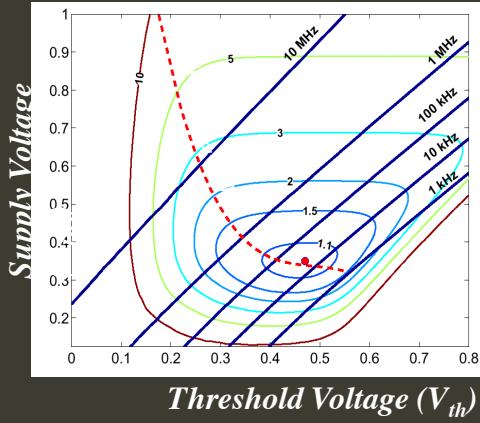
*(recoup performance through parallelism)*

BUT: CMOS Has Minimum Energy Point Set by Leakage



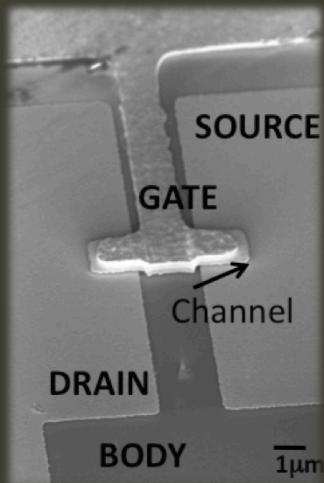
## Sub-Threshold Operation Leads to Minimum Energy/Operation

Energy-Aware FFT Processor  
[Chang, Chandrakasan, 2004]



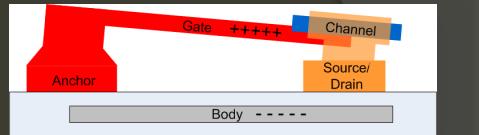
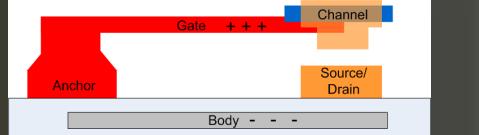
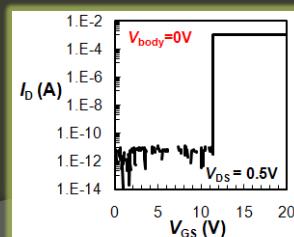
Subliminal  $\mu$ processor for  
retinal implants  
3 pJ/inst @ 350 mV  
[Blaauw, VLSI'07]

## How About Mechanical Computing?

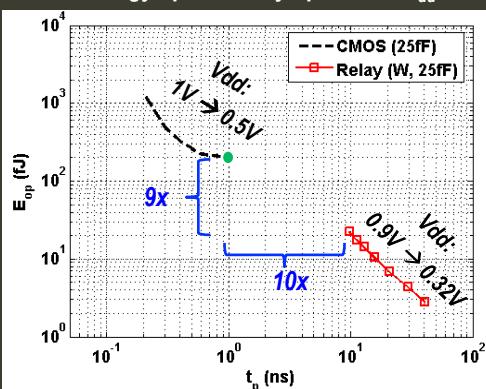


NEMS Relay

[Courtesy: TJ King, E. Alon, UCB]

ON:  $V_{GS} > V_{PI}$  – Low on resistanceOFF:  $V_{GS} < V_{PI}$  – Zero Leakage

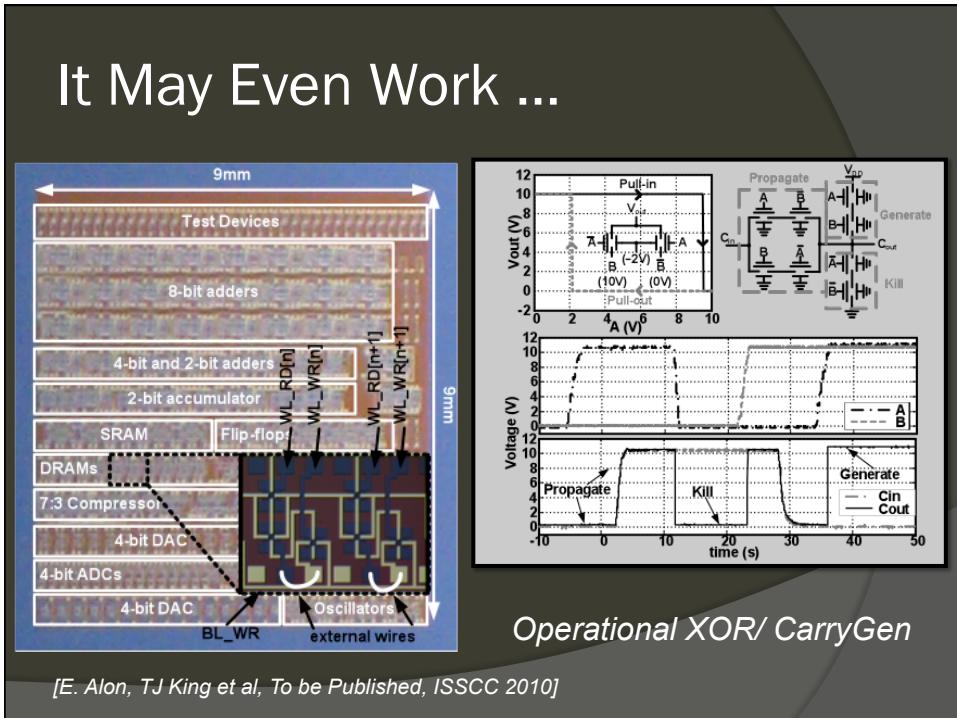
## NEMS Relays Versus CMOS

Energy/op vs. Delay/op across  $V_{dd}$ 

	CMOS	Relay
Supply Voltage	0.5 V	0.32 - 0.9 V
Load Cap per Output	25 fF	25 fF
Total Gate Cap	4.0 pF	125 fF
Area	600 $\mu\text{m}^2$	480 $\mu\text{m}^2$

Enables the parallelism concept anew!

[CMOS Adder: D. Patil, ARITH'07]



## The Lessons from EE141

- ❑ Digital IC Design has been a tremendous success story
  - Fueled by Moore's Law
- ❑ Design complexity has increased accordingly
  - Has been addressed by raising abstraction levels
  - Custom -> ASIC -> IP and System-on-a-Chip
- ❑ Before: Area & Performance
- ❑ Now: Area, Energy and Performance
- ❑ Any successful system designer must have insight in the design trade-off space