UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey *Homework #4* *EECS 141*
Due Monday, February 23, 5pm, box in 240 Cory

1. Given the RC network below:

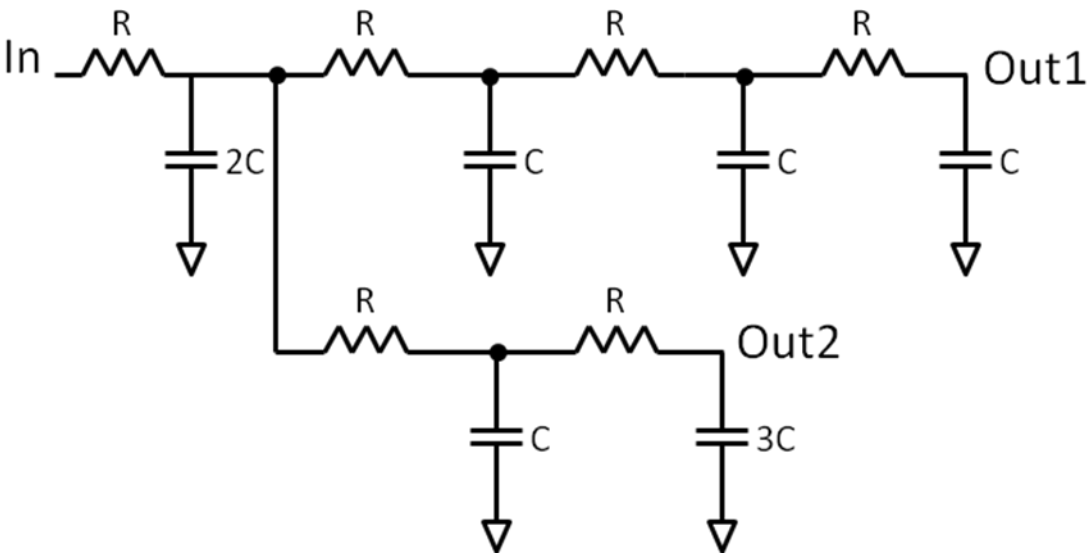


Figure 1 RC network.

(1) Calculate the Elmore delay from In to Out1 and from In to Out2. Which one is critical path? (10 pts)
(2) Assume R = 100Ω and C = 10fF. Calculate the Elmore delay of the critical path you find in part (1) and verify the result using Spectre. (10 pts)

Solution:

(1) From In to Out1:
$\tau_1 = R \cdot (2C + C + 3C) + 2RC + 3RC + 4RC = 15RC$

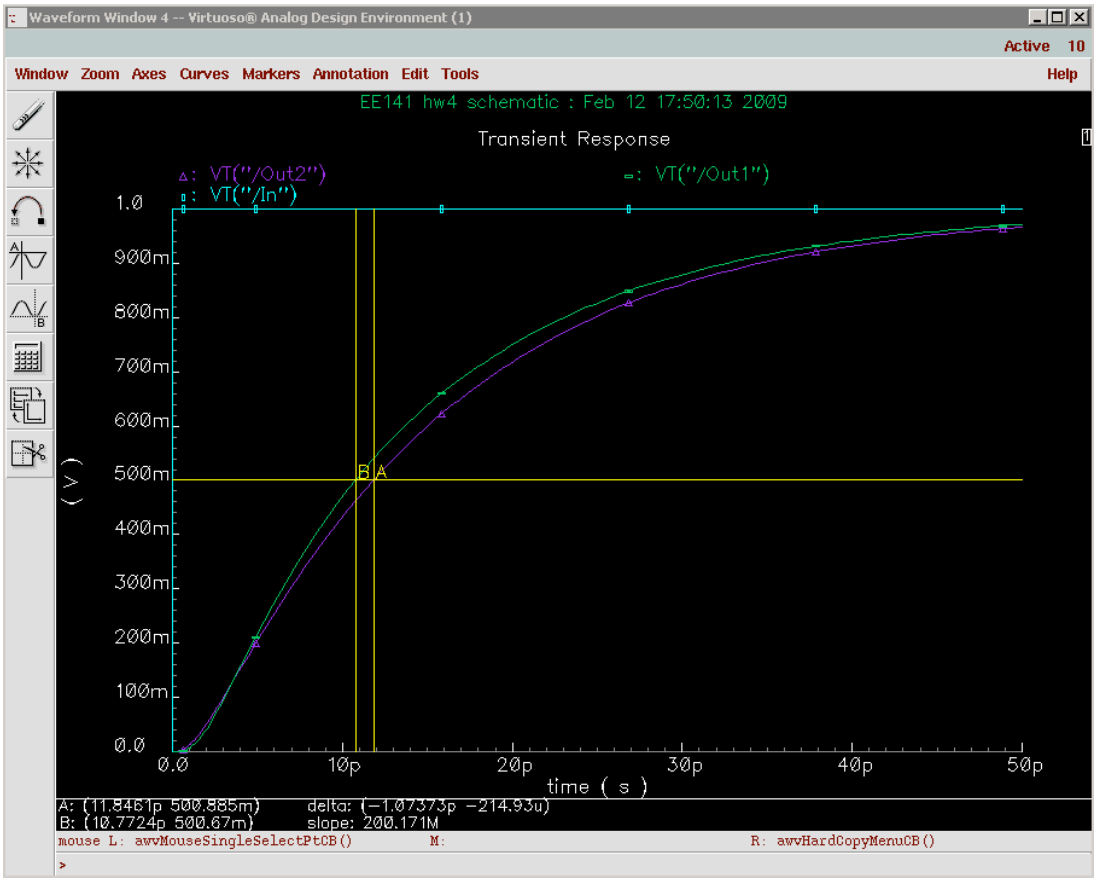
From In to Out2:
$\tau_2 = R \cdot (2C + C + C + C) + 2RC + 3R \cdot 3C + 4RC = 16RC$

The path from In to Out2 is critical path

(2) From In to Out1:
$t_{d1} = 0.69\tau_1 = 0.69 \cdot 15 \cdot 100 \cdot 10 \times 10^{-15} = 10.35ps$

From In to Out1:

$t_{d2} = 0.69\tau_2 = 0.69 \cdot 16 \cdot 100 \cdot 10 \times 10^{-15} = 11.04ps$



From the simulation results, $t_{d1} = 10.77ps$, $t_{d2} = 11.85ps$

2. In the following problem, we will calculate the delay of a NAND2 gate by using two approaches we have learned, logical effort and Elmore delay. The NMOS and PMOS can be modeled as a RC network shown below when the transistor is "ON". When the transistor is "OFF", we use the same model except now the transistor has an infinite off-resistance. Assume $\gamma = 1$.

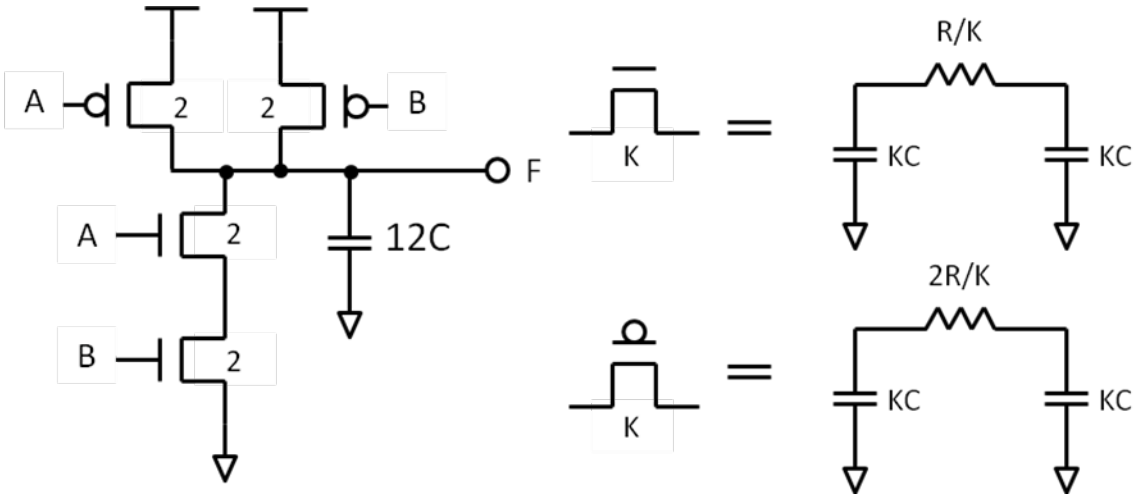


Figure 2 A NAND2 gate and NMOS and PMOS transistor models.

(1) Calculate the T_{pLH} and T_{pHL} of a NAND2 gate shown above using logical effort. (5 pts)
(2) Calculate the T_{pLH} and T_{pHL} of a NAND2 gate shown above using Elmore delay. Do you get different answers in delay between part (1) and (2)? Briefly explain why there is or isn't difference. (15 pts)

Solution:

(1) $T_{pLH} = T_{pHL} = t_{p0}(p + fg) = 0.69 \cdot 3RC(2 + \frac{4}{3} \cdot 3) = 12.42RC$

(2) $T_{pLH} = 0.69 \cdot R \cdot (2C + 2C + 2C + 12C) = 12.42RC$

$T_{pHL} = 0.69 \cdot [0.5R \cdot 4C + R(2C + 2C + 2C + 12C)] = 13.8RC$

We get different T_{pHL} results between part (1) and (2) because the delay calculation using logical effort ignores the internal node capacitances.