EE223 Analog Integrated Circuits
Fall 2018

Lecture 2: Review of Basics

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ENG-259

EE223 Cadence Lab

- ENG 289 Code: 116 0656
- ISA: Ashley Hettick, achettick@gmail.com
- Lab Time: Tuesday 6:00 – 8:00 PM
  Wednesday 3:45 – 5:45 PM
- ISA will help only Cadence setup & simulation related issues

Agenda

- Review of Basics
- Circuit Facts
- Analog Design Philosophy
- Circuits to be covered in the class
- Device Types
  - Passive
  - Active

Standard Prefixes for Multiples

Prefix	Symbol	Multiplying Factor
exa-	E	10^{18} = 1,000,000,000,000,000,000
peta-	P	10^{15} = 1,000,000,000,000,000
tera-	T	10^{12} = 1,000,000,000,000
giga-	G	10^{9} = 1,000,000,000
mega-	M	10^{6} = 1,000,000
kilo-	k	10^{3} = 1,000
hecto-	h	10^{2} = 1000
deca-	da	10 = 10

Standard Prefixes for Fractions

deca-	**da**	**$10 = 10$**
deci-	**d**	**$10^{-1} = 0.1$**
centi-	**c**	**$10^{-2} = 0.01$**
milli-	**m**	**$10^{-3} = 0.001$**
micro-	**μ**	**$10^{-6} = 0.000,001$**
nano-	**n**	**$10^{-9} = 0.000,000,001$**
pico-	**p**	**$10^{-12} = 0.000,000,000,001$**
femto-	**f**	**$10^{-15} = 0.000,000,000,000,001$**
atto-	**a**	**$10^{-18} = 0.000,000,000,000,000,001$**

μm, nm, Å

- 1 um = 10^{-6} m
  = $10^{3} \cdot 10^{-9}$ m
  = 1000 nm
  = 10000 Å

- 0.13 um = 130 nm technology
  - Minimum channel length: L = 0.13 um = 130 nm = 1300 Å
  - Tox ~ L / 50 = 130 nm / 50 = 2.6 nm

Things To Remember

- Speed of light
  - C = 3 x 10^8 m/s
  - C = f λ = frequency x wavelength
- 1 ppm = 10^{-6}
  - 1000 ppm = 10^{-3} = 0.001 = 0.1%
- ε_o = 8.85 x 10^{-12} F/m = 8.85 aF/um
  - ε_{si} = 11.7 ε_{ox} = 3.97 ε_{ni} = 16
- k = 1.38 x 10^{-23} J/K, q = 1.6 x 10^{-19} C
  - kT = 4 x 10^{-21} Joule at 300 K or 4kT = 1.6 x 10^{-20} Joule
  - kT / q = 26 mV at 300 K
  - Capacitor noise $\sqrt{\frac{kT}{C}}$ = 64 μV for 1pF
  - Resistor noise: Noise of 1 kΩ = 4kTR/Hz => 4 nV /√Hz

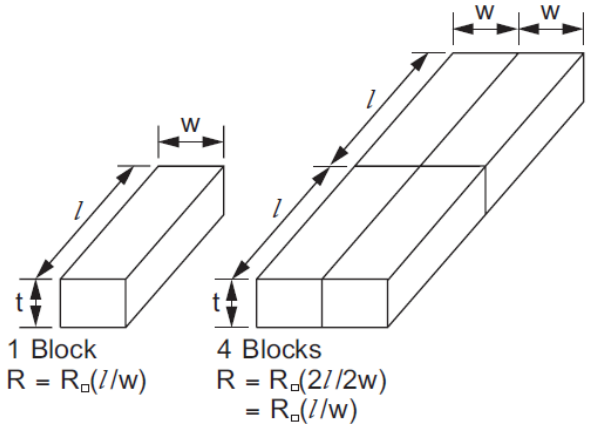
Things To Remember

- Cox = ε / t_{ox} (capacitance per unit area)
  - T_{ox} = 50 Å = 5 nm -> C_{ox} = 3.9 x 8.85 /5 = 7 fF/um^2
  - T_{ox} = 10 Å = 1 nm -> C_{ox} = 3.9 x 8.85 /1 = 35 fF/um^2

- R = ρ L / A = ρ L / (Wt) = (ρ/t) (L/W) = R_{sq} (L/W)
  - If R_{sq} = 300 Ω /sq (resistance per unit area)
  - L/W=10 → R = 3 kΩ
- Angular frequency w = 2πf = 1 / RC
  - R=1 kΩ, C=1pF → f = 160 MHz

- Logarithmic relation: log A B = log A + log B
  - log 2 = 0.3
  - log 4 = 2 x log 2 = 0.6

- Cascade of gain stages
  - Total Gain A = A_1 x A_2 x A_3
  - Input referred offset V_{os} = V_{os1} + V_{os2}/A_1 + $V_{os3}/(A_1A_2)$



Things To Remember

- KVL & KCL
- Ohm's law

  $V = R\,I$ $\qquad\qquad$ $Q = C\,V$
- I-V relationship

  Capacitor: $I = C\,dV/dt \rightarrow$ slew rate $= dV/dt = I / C$

  Inductor: $V = L\,di/dt$
- Power $P = V\,I$

Understanding Power

- $P = V I$
- Total power = Static power + Dynamic power + Leakage power
- Static power = $V I$
- Dynamic power = $\alpha C V^2 f$
- Leakage Types
  - junction leakage
  - gate leakage – watch out for this in 90nm technology and beyond
  - sub-threshold leakage: usually dominant leakage factor
  - Reducing leakage
    - Higher Vt
    - 10% longer gate length reduces leakage by 35%
    - Doubling L reduces leakage by 3X

Decibel

- Signal amplitude can vary orders of magnitude from very small to very large values
  - Use logarithm to handle large dynamic range

- dB = 20 log V
  - If V = 100, then 20 log V = 20 log 100 = 40 dB
  - V2 = 10 x V1 → 20 dB increase
  - 0 dB = 1
  - -3 dB → $10^{(-3/20)}$ = 0.7 → 30% drop in magnitude from 0 dB

- dBm = 10 log (P/1mW) = 10 log $V^2/(0.001R)$
  - If R = 100 ohm, then -160 dBm = 3.26 nV
  - 0 dBm = 1 mW
  - V2 = 10 x V1 → 20 dBm increase

More Things To Remember

- Transistor Vt mismatch A_{vt} = (1~2) mV · μm per nm
  - T_{ox} = 35 Å = 3.5 nm → A_{vt} = (3.5 ~ 7) mV · μm
- DR (ENOB) = 6.02 N + 1.76 in dB
  - 10 bit = 62 dB
  - 1V signal in 10 bit → 1 LSB = 1 mV
- Miller Effect: Y = C · (1 – A)
  - If A is large, $C_{eff} \approx A \cdot C$
  - If A = 0.8, C_{eff} = 0.2 C

Circuit Spec

- Power supplies
  - 1.0V for Core
  - 1.8V for I/O
  - Power dissipation requirement

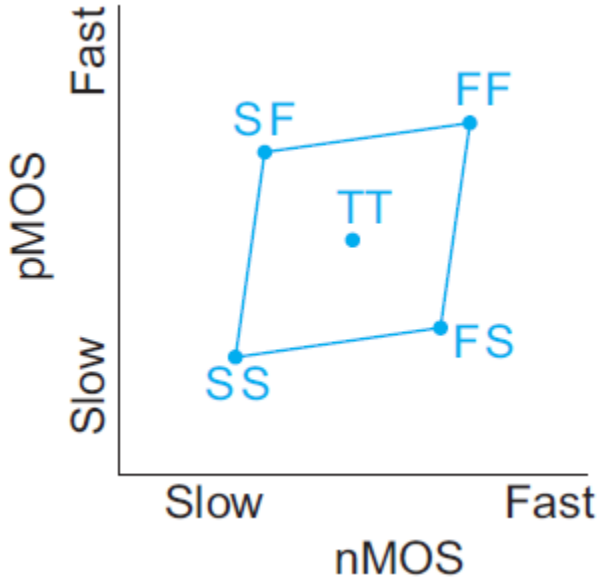
- Temperature Range
  - Commercial: 0 °C ~ 70 °C
  - Industrial: -40 °C ~ 85 °C
  - Automotive: -40 °C ~ 125 °C
  - Military: -55 °C ~ 125 °C

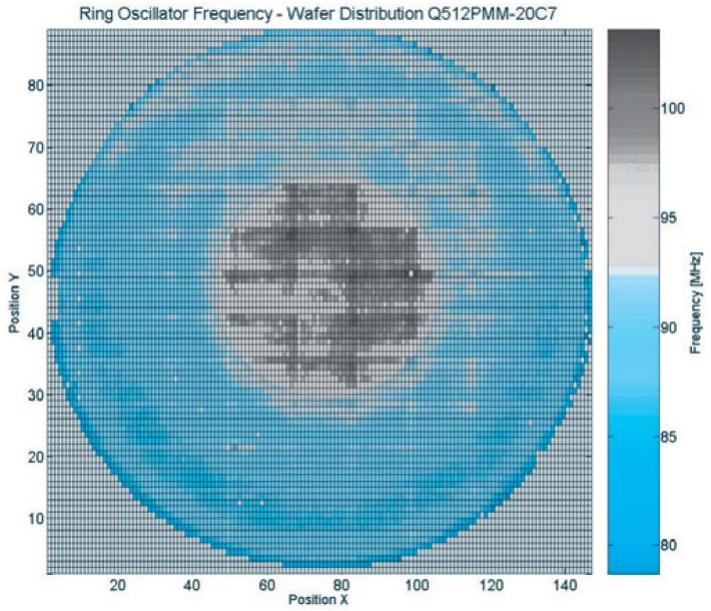
- Signal
  - Frequency of operation
  - Voltage signal swing
  - Current driving capability
  - Linearity (Signal to Noise ratio, Dynamic range, ENOB)

Process Variation

- Variations
  - Lot-to-Lot (L2L)
  - Wafer-to-Wafer (W2W)
  - Die-to-Die (D2D) or within-wafer (WIW)
  - Within-die (WID) or intra-die

- Process Corners
  - TT
  - SS
  - FF
  - SF
  - FS





Corner	Voltage	Temperature
F	1.98	0 °C
T	1.8	70 °C
S	1.62	125 °C

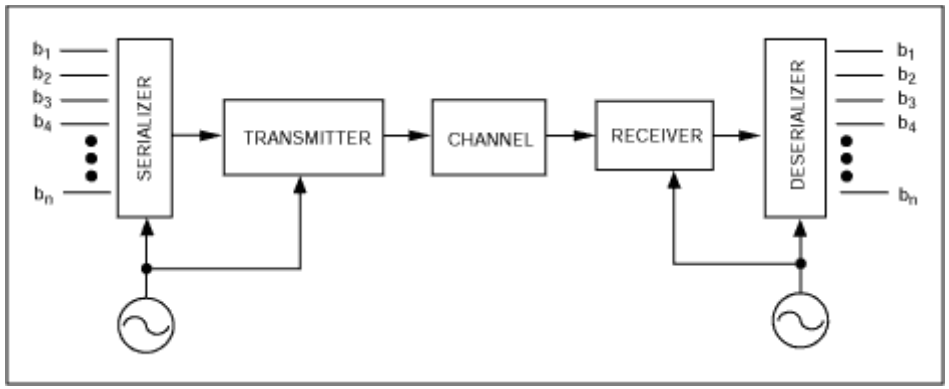
PVT Variation

- Process Variation
  - TT
  - SS
  - FF
  - SF
  - FS
- Voltage (Power Supply) Variation
  - ±10% or ±5%
- Temperature Range
  - Commercial: 0 °C ~ 70 °C
  - Industrial: -40 °C ~ 85 °C
  - Automotive: -40 °C ~ 125 °C
  - Military: -55 °C ~ 125 °C

Circuit Design Goal

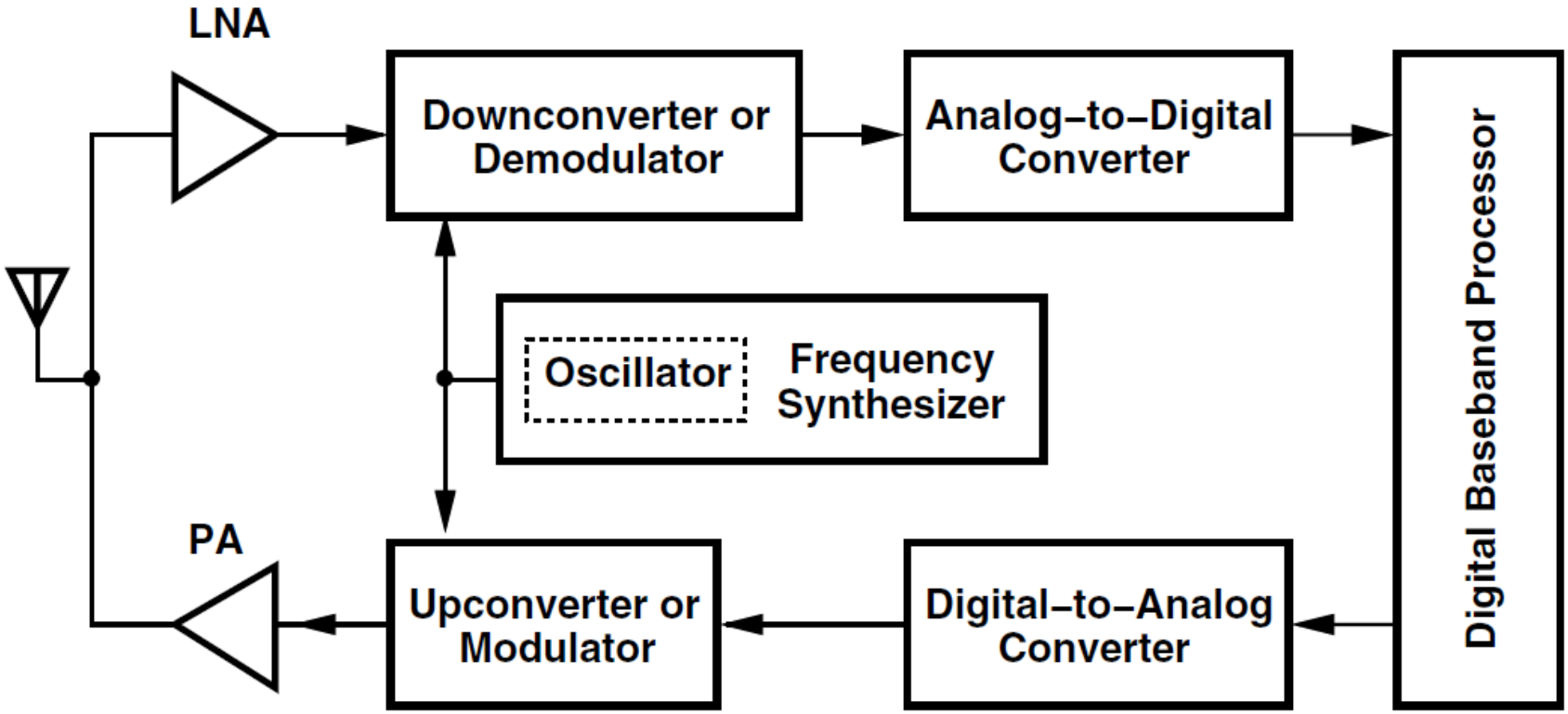
- Meet all the spec required
- Minimize power dissipation
- Minimize circuit area
- Minimize design time
- Minimize re-spin of the design
  - Design review by team members
  - Cost implications
    - 1 or 2 day delay in tape-out
    - Mask re-spin
    - Production recall

Generic Communication Diagram

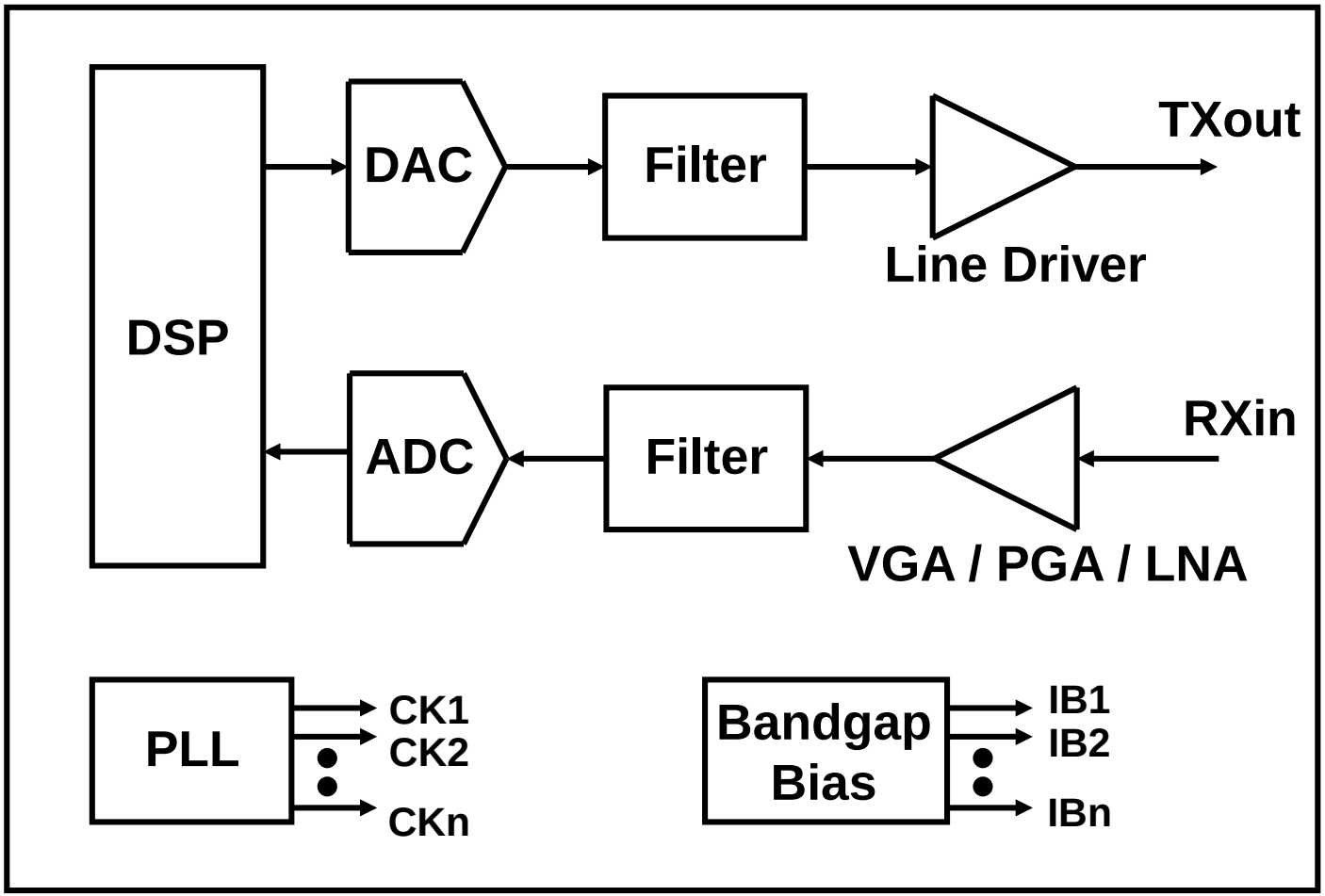


- Serializer + Deserializer = Serdes
- Channel can be either Wireline or Wireless
- Transmitter and Receiver are in a single chip

RF Transceiver



Baseband Transceiver



Basic Circuits

- Bandgap and Bias
- Amplifiers
- Comparators
- Sample & Hold
- References & Regulators

EE223

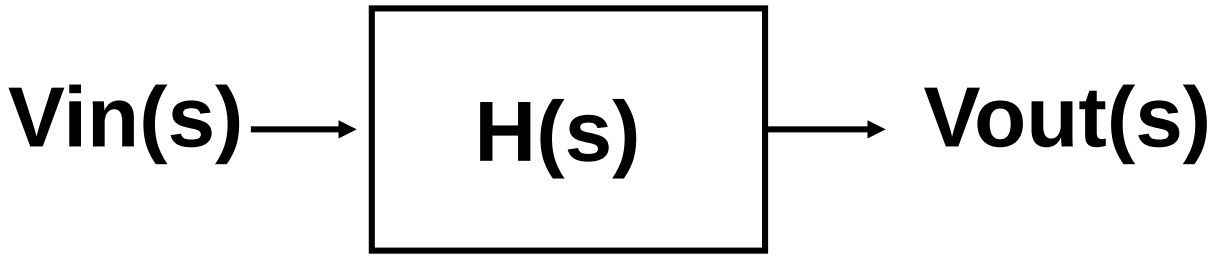
- Filters
- Oscillators
- PLL
- Integrators
- Data converters

Advanced Analog
EE288
EE230
EE227

Circuit Facts

- Structure
  - Circuits consist of a bunch of semiconductor devices such as transistors, resistors, capacitors, and occasionally inductors
- Maxwell's equation
  - Circuit should obey KCL, KVL, and Ohm's law
- Signal path
  - High impedance node in the signal path creates a low frequency pole
  - Low impedance node in the signal path creates a high frequency pole
  - Inverting amplifier creates a right half plane zero
  - Non-inverting amplifier creates a left half plane zero

Circuit Transfer Function



- Transfer function

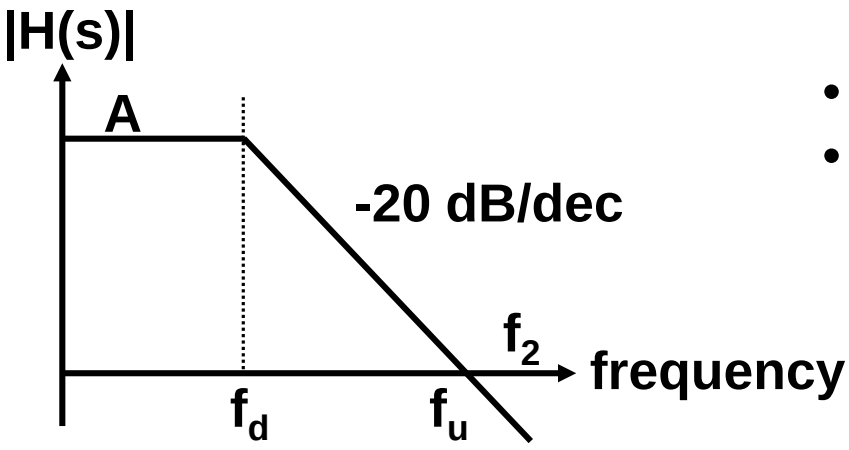
$$H(s) = \frac{Vout(s)}{Vin(s)} = \frac{A(s - z1)(s - z2)}{(s - p1)(s - p2)}$$

Many circuit blocks can be approximated as second order system.

Stability Consideration

- Two poles in the transfer function
  - Useful for checking stability of Amplifiers
  - Filter design
  - PLL design

- Bode Plot



- **$f_u = A\, f_d$**
- **For 70 deg phase margin**
  $f_2 > 3f_u$

Signal-to-Noise Ratio

- SNR = P_{sig} / P_{noise}
  - SNR = 10 log P_{sig}/(kT/C) = f(C)
    - 1 bit → 6 dB → 4x increase in capacitor value for 6 dB
    - Keep bandwidth constant ~ 1/RC ~ gm/C
    - Keep voltage constant: 4 gm → 4 x I_D → 4x Power
    - Thermal noise limited circuit:
      - Each additional bit quadruples power dissipation
      - Over design is very costly