EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 9: Sample and Hold Circuits

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ENG-259

Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	Finish Flash ADC
28-Feb	DAC Architectures - Resistor, R-2R
5-Mar	DAC Architectures - Current steering, Segmented
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

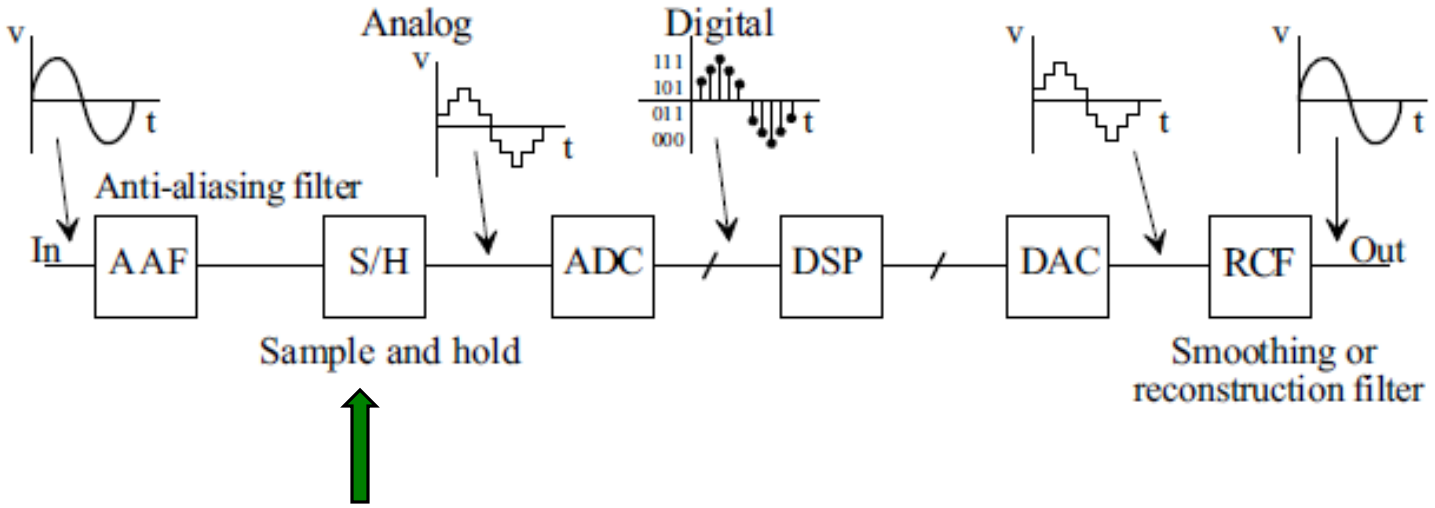
Sample & Hold

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

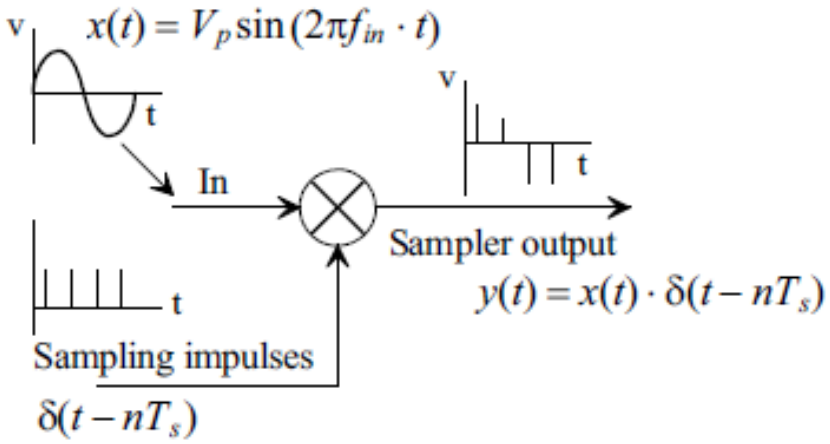
Agenda

- Sample & Hold Circuits

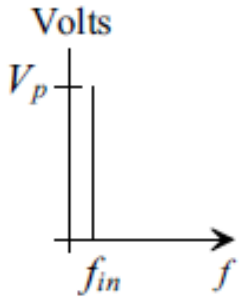
Recap A/D & D/A Signal Path



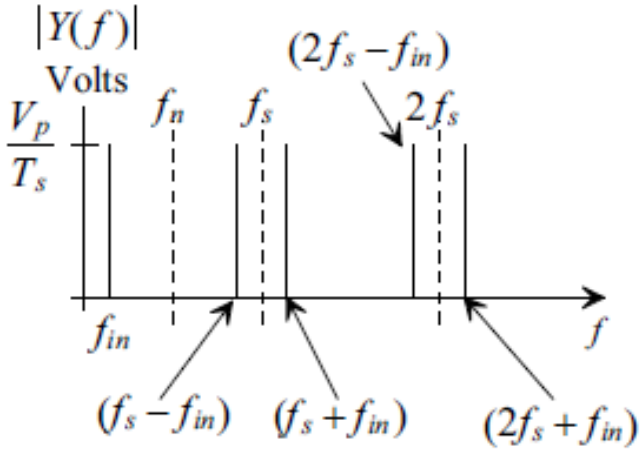
Review: Sampling & Spectrum



$$f_n = \frac{f_s}{2}$$

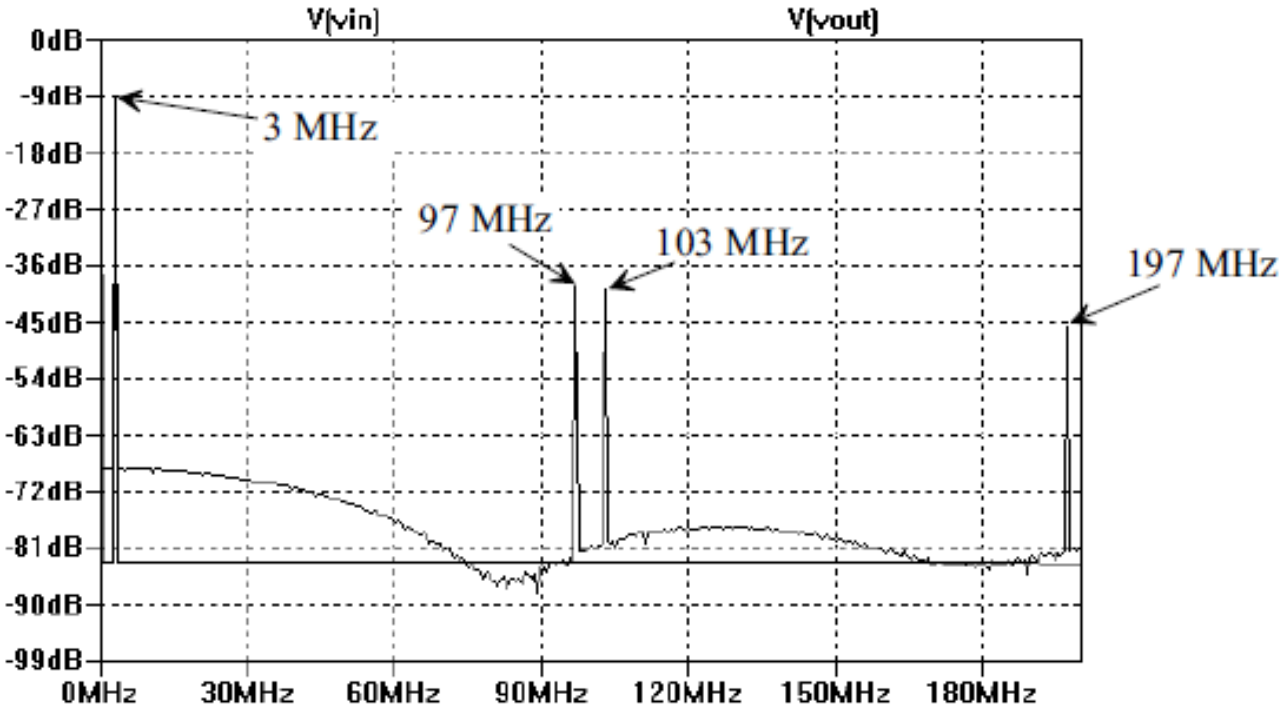


(a) Input spectrum



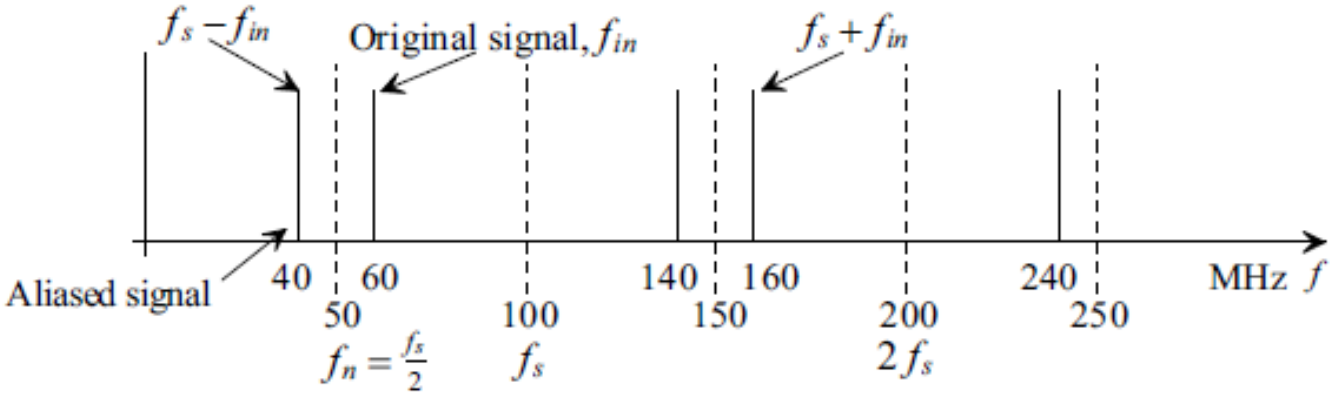
(b) Output spectrum after sampling

Review: Sampling Spectrum

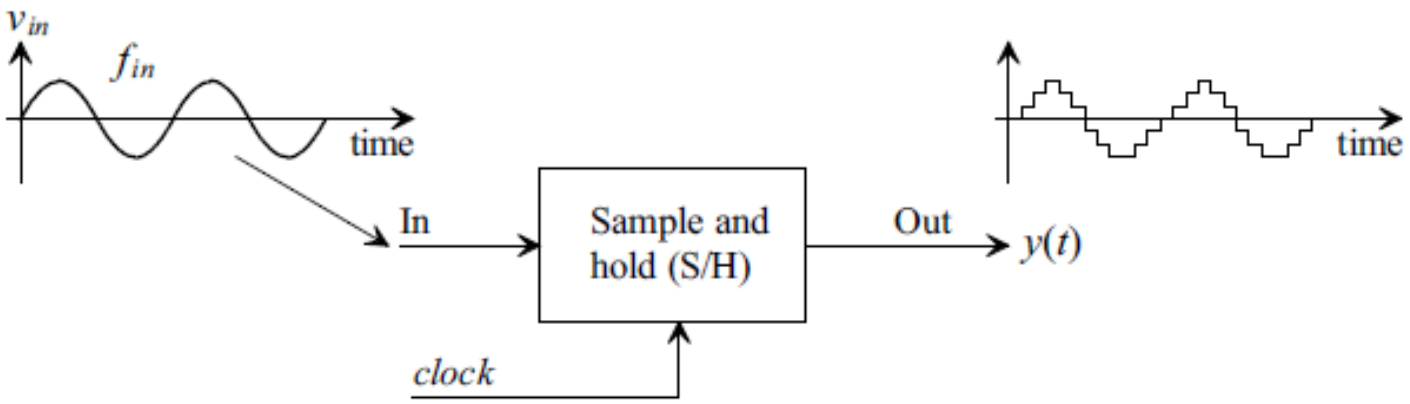


Review: Aliasing

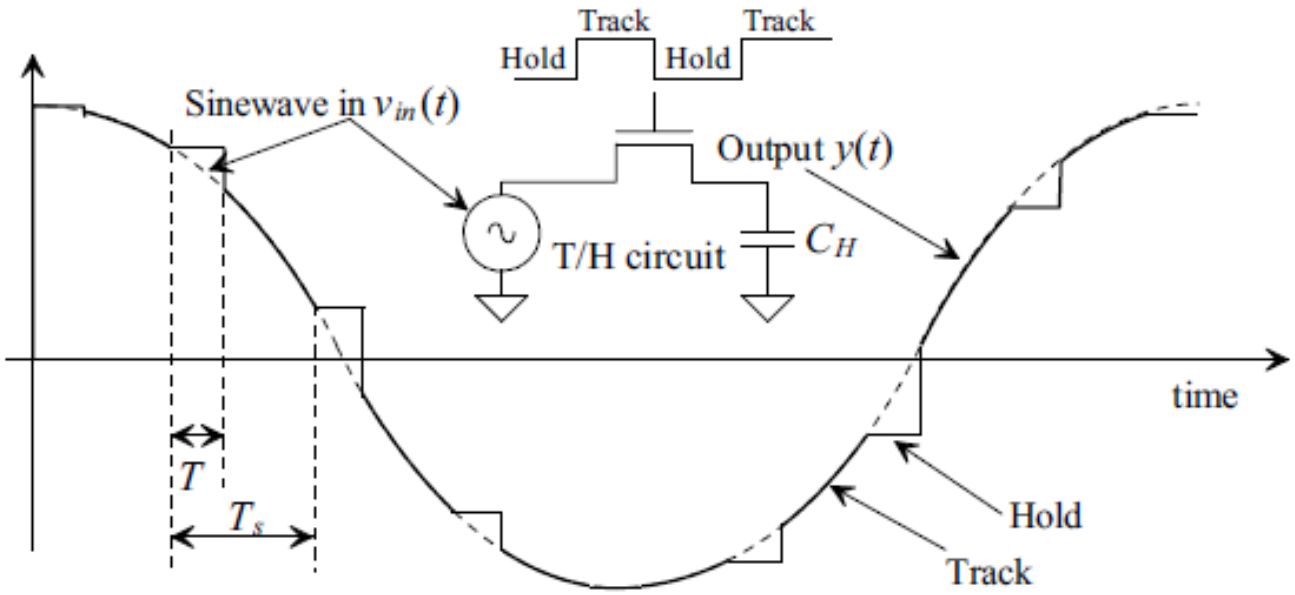
f_{in} = 60 MHz
f_s = 100 MHz



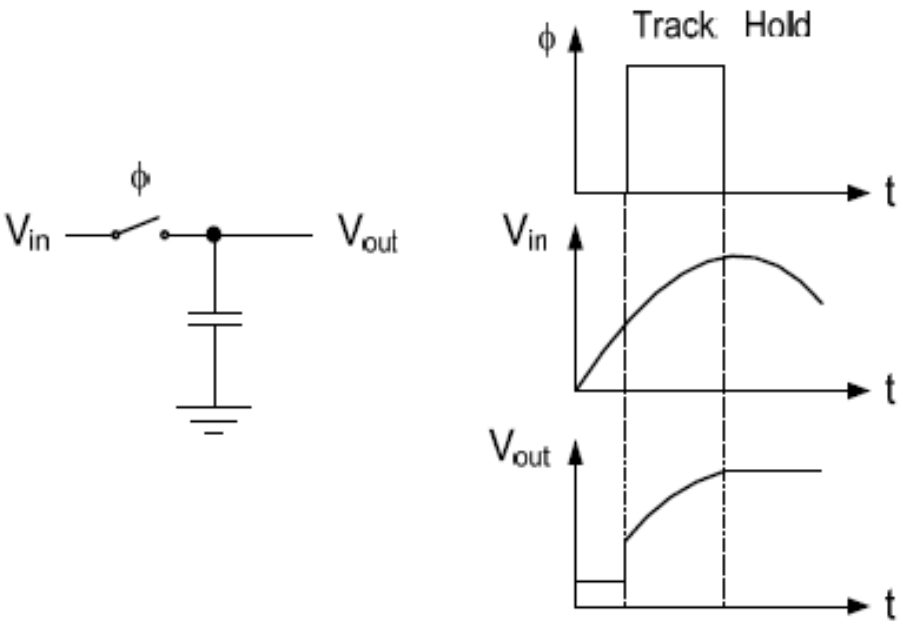
Sample and Hold (S/H)



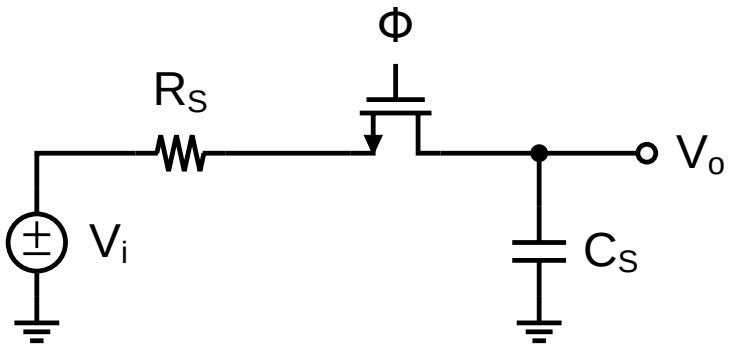
Track and Hold (T/H)



Ideal T/H

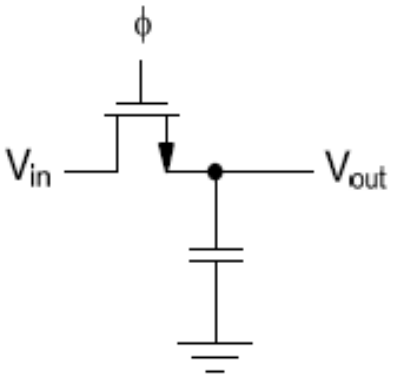


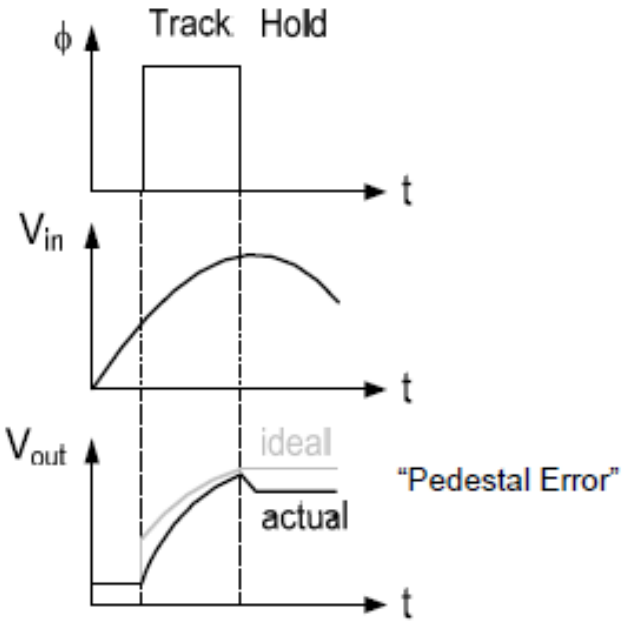
Simple NMOS T/H (or S/H)



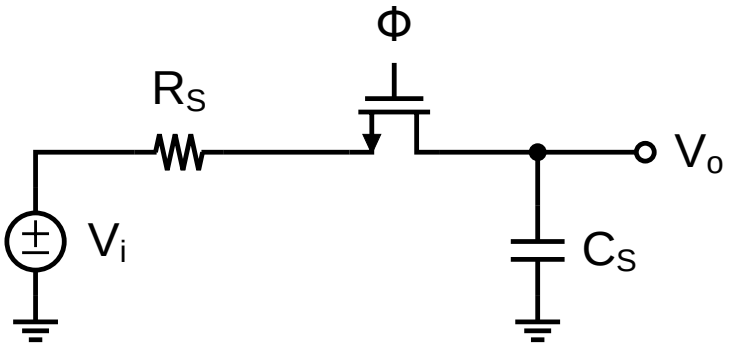
Non-idealities of T/H

- Finite acquisition time
- Thermal noise
- Clock jitter
- Charge injection and clock feedthrough

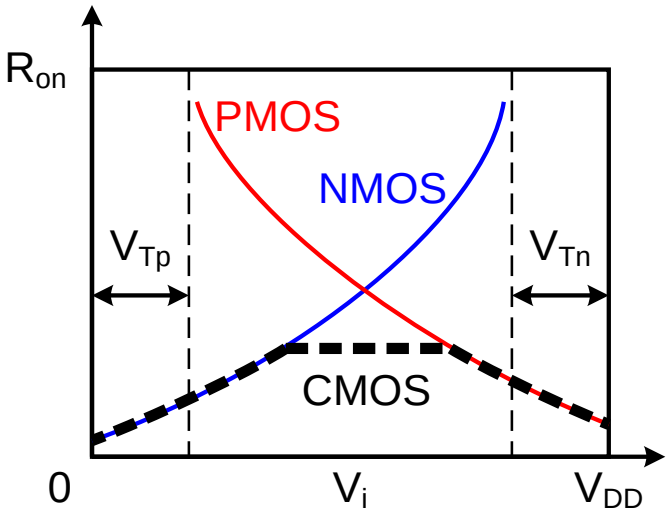




Signal-Dependent R_{on}



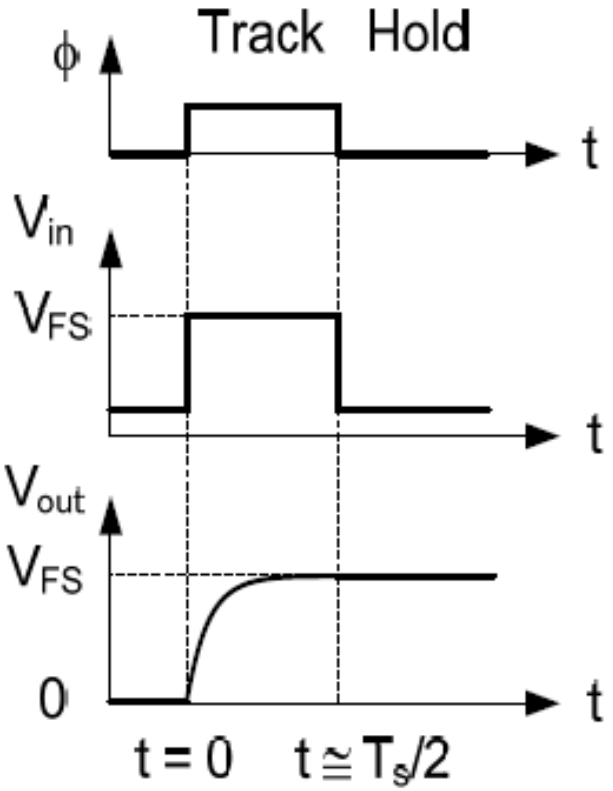
$$R_{on}^{-1} = \mu C_{ox} \frac{W}{L}(V_{DD} - V_{th} - V_i)$$



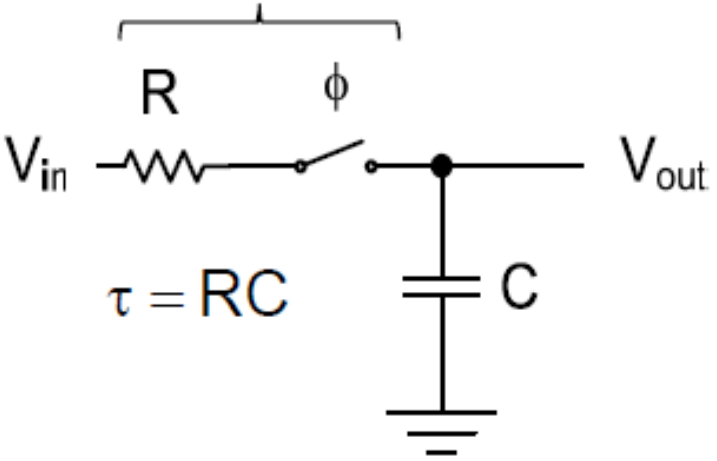
- Signal-dependent R_{on} → signal-dependent TBW → extra waveform distortion
- TBW should be sufficiently large (>> f_{in}, depending on the target accuracy)

Finite Acquisition Time

- For simplicity, neglect finite rise time of the input signal
- Consider worst case – the output is required to settle from 0 to the full-scale voltage of the system (V_{FS})

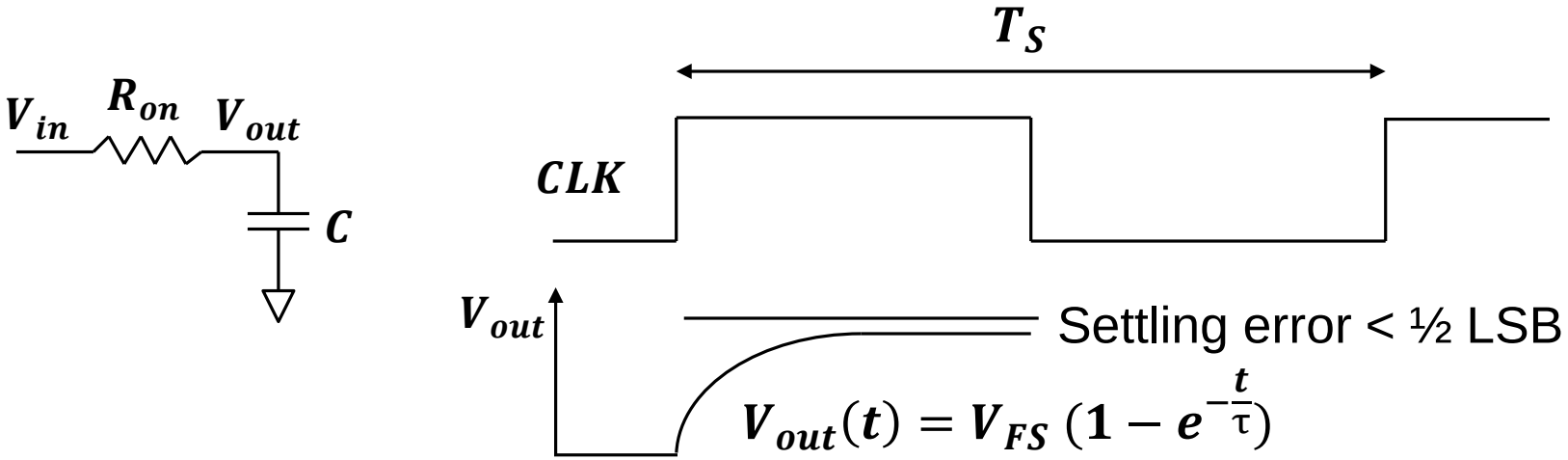


First order MOS switch model



$$\Rightarrow V_{out}(t) = V_{FS}\left(1 - e^{-t/\tau}\right)$$

Finite Acquisition Time



$$\textbf{Want the settling error } < \frac{1}{2} LSB \rightarrow V_{FS}\, e^{-\frac{t}{\tau}} < \frac{1}{2} \cdot \frac{V_{FS}}{2^N}$$

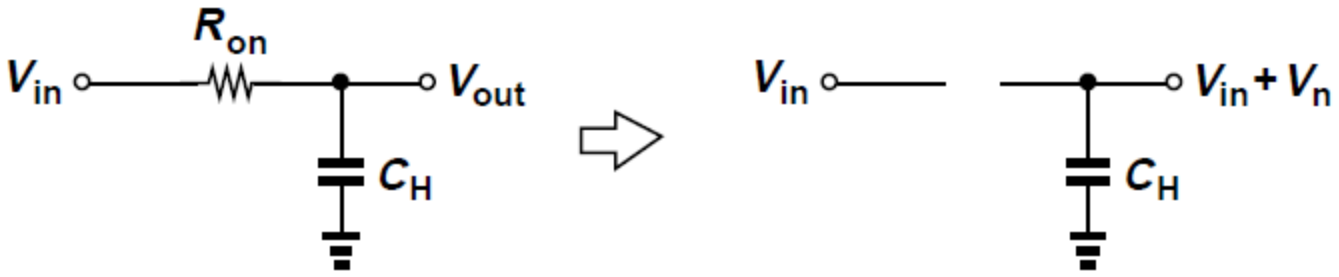
$$\textbf{Assume it takes } n \textbf{ time constants to settle within } \frac{T_S}{2},$$

$$e^{-n} < \frac{1}{2} \cdot \frac{1}{2^N} \quad \rightarrow \quad n > ln(2^{N+1})$$

$$\textbf{For } N = 10 \textbf{bit ADC, you need } 7.6\tau$$

Thermal Noise

- kT/C Noise:
- Resistor charging a capacitor gives a total RMS noise voltage of $\sqrt{kT/C}$.
- On resistance of switch introduces thermal noise at output which is stored on the capacitor when switch turns off
- RMS voltage of sampled noise is still approximately equal to $\sqrt{kT/C}$.



Implication of Thermal Noise

Suppose we make the kT/C noise equal to the quantization noise of a B-bit ADC

$$\frac{kT}{C} = \frac{\Delta^2}{12}, \quad \Delta = \frac{V_{FS}}{2^B} \Rightarrow \quad C = 12kT\left(\frac{2^B}{V_{FS}}\right)^2$$

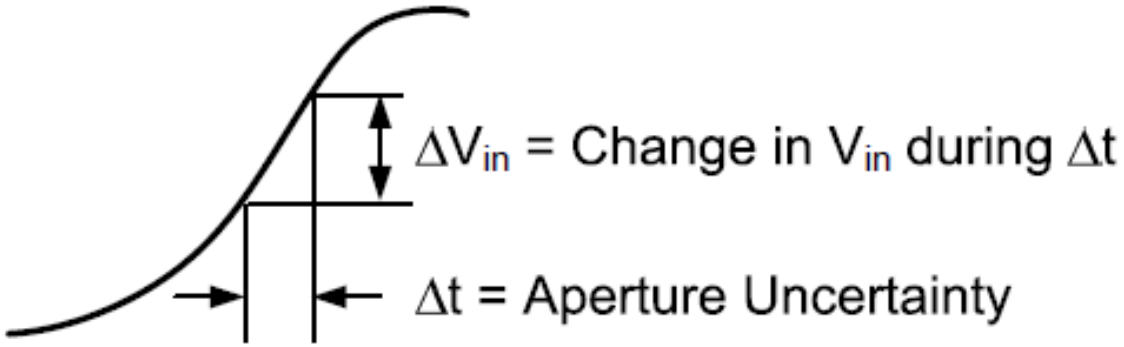
For a given resolution B, both C and R can be determined.

Below table shows example numbers for V_{FS}=1V and f_s=100MHz

B	C [pF]	R [Ω]
8	0.003	246,057
10	0.052	12,582
12	0.834	665
14	13.3	36
16	213	1.99
18	3,416	0.11

Aperture Uncertainty

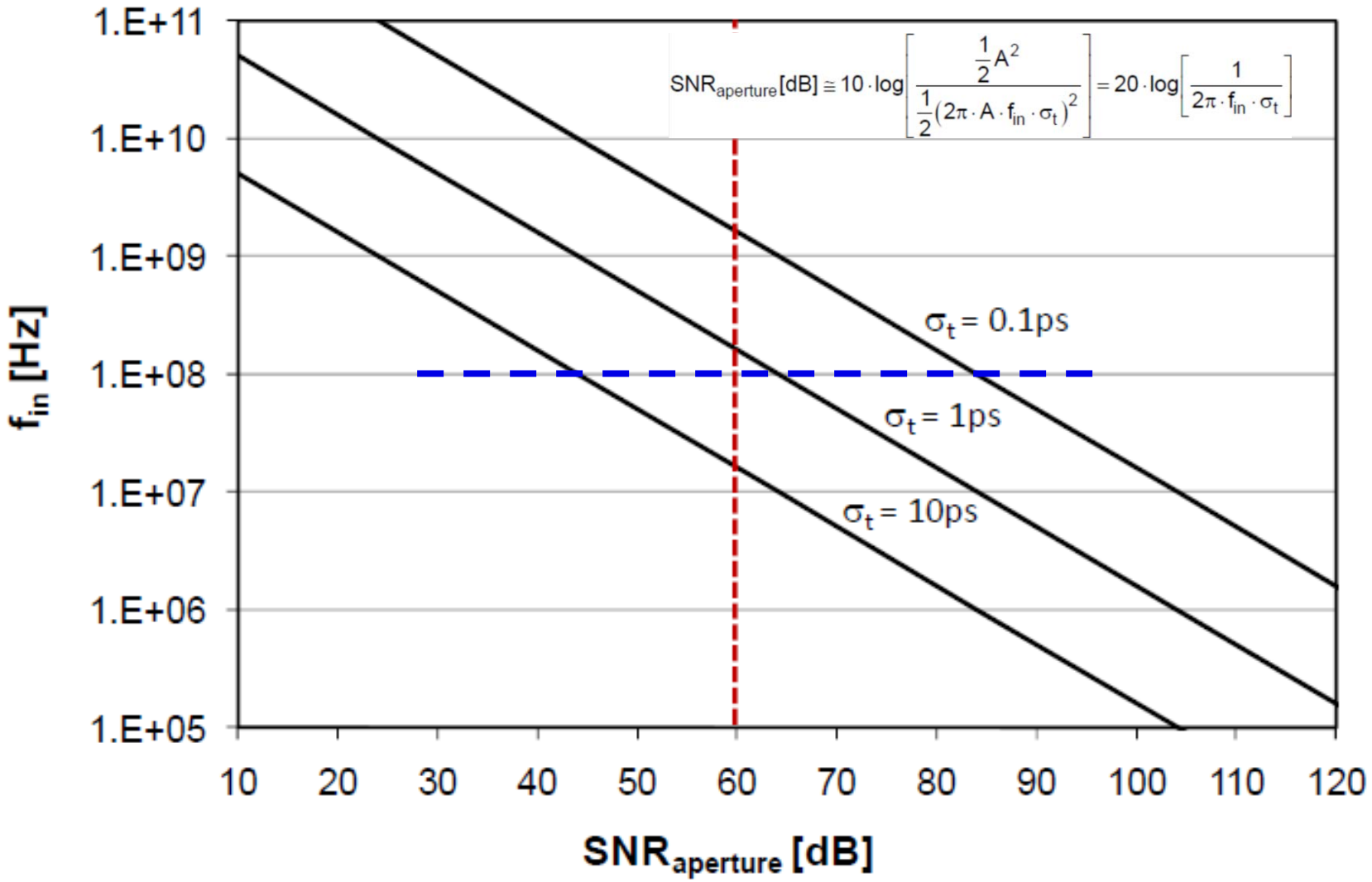
- In any sampling circuit, electronic noise causes random timing variations in the actual sampling clock edge
  - Adds "noise" to samples, especially if dV_{in}/dt is large



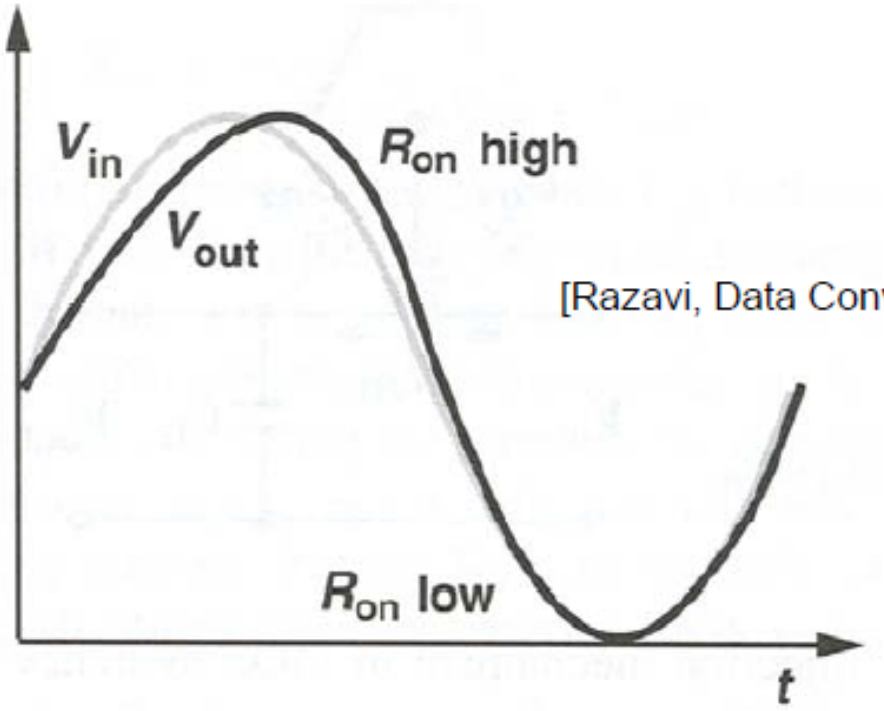
$$\Delta V_{in} \cong \frac{dV_{in}}{dt} \cdot \Delta t$$

- Analysis
  - Consider sine wave input signal
  - Assume Δt is random with zero mean and standard deviation σ_t

Result of Aperture Jitter



Track Mode Nonlinearity



[Razavi, Data Conversion System Design, p.16]

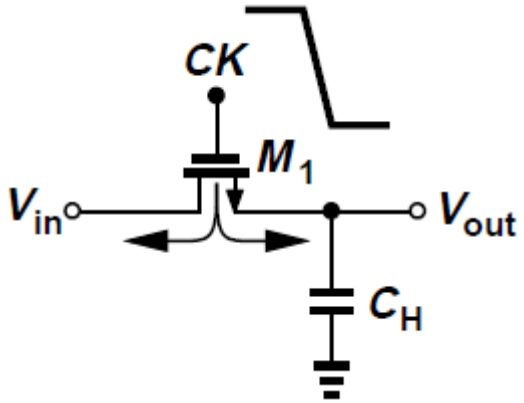
Output tracks well when input voltage is low

– Gets distorted when voltage is high due to increase in R_{ON}

Charge Injection

- For MOSFET to be on, a channel must exist at the oxide-silicon interface
- Assuming $V_{in} \approx V_{out}$, total charge in the inversion layer is

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$



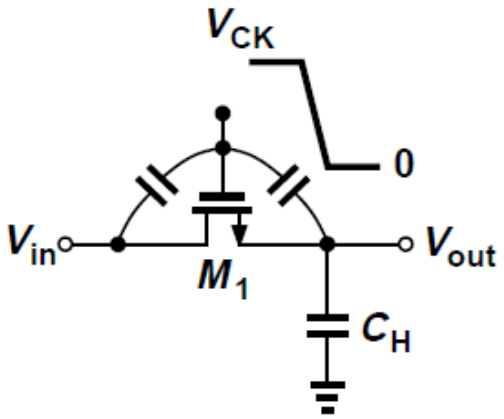
- When switch turns off, Q_{ch} exits through the source and drain terminals ("channel charge injection")

Clock Feedthrough

- MOS switch couples clock transitions through C_{GD} or C_{GS}
- Sampled output voltage has error due to this given by

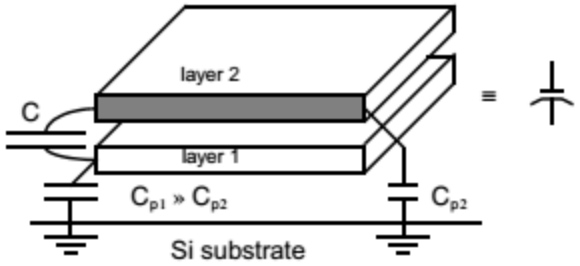
$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_H}$$

- C_{ov} is the overlap capacitance per unit width
- Error ΔV is independent of input level, manifests as constant offset in the input/output characteristic



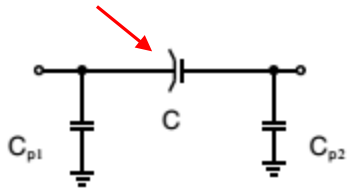
Basic Building Blocks of Switched-Capacitor Circuits

- OPAMP (OTA)
- Capacitor
- Switch
- Clock



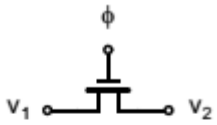
(a)

Bottom Plate

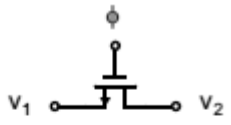


$C_{p1} > C_{p2}$

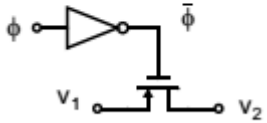
(b)



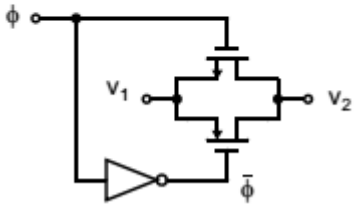
(a)



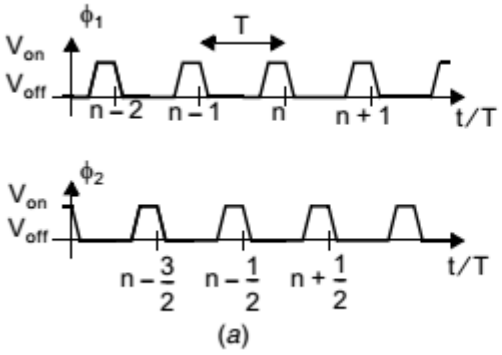
(b)



(c)

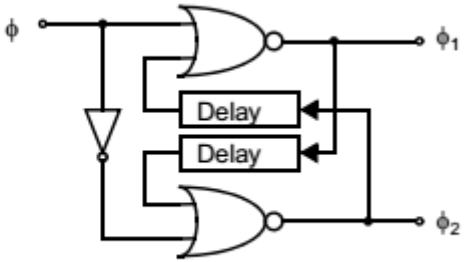


(d)



(a)

$f_s \equiv \frac{1}{T}$



(b)