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8:00-11:00am

EECS 141: FALL 2001—FINAL EXAM

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):
NMOS:
$V_{Tn} = 0.4$, $k'_n = 115$ mA/V^2, $V_{DSAT} = 0.6$V, $\lambda = 0$, $\gamma = 0.4$ V$^{1/2}$, $2\Phi_F = -0.6$V
PMOS:
$V_{Tp} = -0.4$V, $k'_p = -30$ mA/V^2, $V_{DSAT} = -1$V, $\lambda = 0$, $\gamma = -0.4$ V$^{1/2}$, $2\Phi_F = 0.6$V

NAME	Last First

GRAD/UNDERGRAD	

Problem 1: _____/ 6

Problem 2: _____/ 12

Problem 3: _____/ 12

Problem 4: _____/ 10

Problem 5: _____/ 8

Problem 6: _____/ 10

Problem 7: _____/ 6

Total: _____/ 64

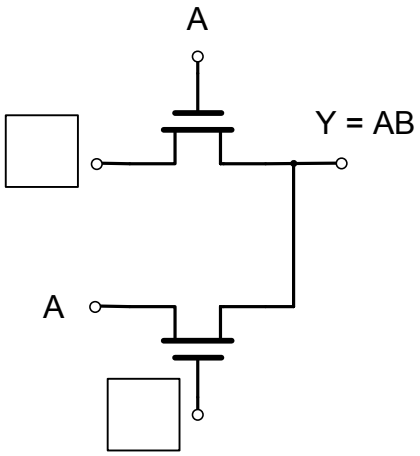
PROBLEM 1. Technology Scaling (6 points)

Assume that the technology scales every two years by a factor of S = 0.7. If a microprocessor in year 2002. is dissipating 100W, consider a scaling scenario in the future, where all the dimensions scale by a factor of 0.7 every technology generation. Technology generation spans 2 years. Assume also that the trends from the past will continue in the future as well: the microprocessor die size continues to increase by 14% every other year, the supply voltage is reduced by a factor 0.85 and frequency doubles every technology generation.

Find the power dissipation of a future microprocessor in year 2010. Please write down all of your assumptions and explain your reasoning.

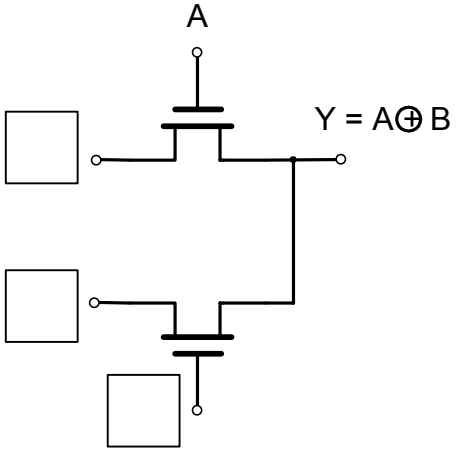
PROBLEM 2: Logic families (12 points)

a) (2 pts) An NMOS-only pass-transistor network is supposed to implement logic AND function Y = AB. Please add appropriate signals in the boxes, such that the circuit works properly.



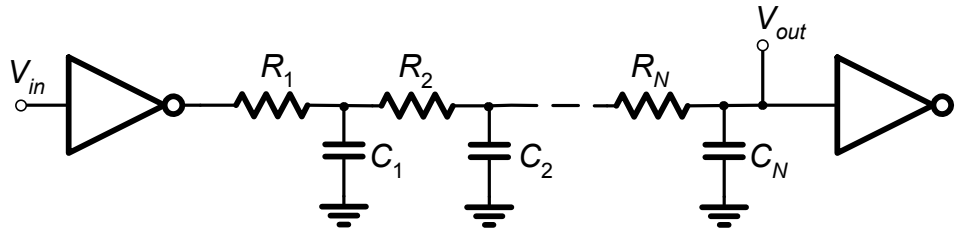
b) (4 pts) Circuit considered in part a) of this problem does not produce full voltage levels at its output. Add **minimum** number of PMOS transistors to it, such that it has a full swing at its output for any combination on its inputs.

c) (6 pts) Repeat parts a) and b) of this problem for the implementation of an XOR.



PROBLEM 3. Wire interconnect. (12 points)

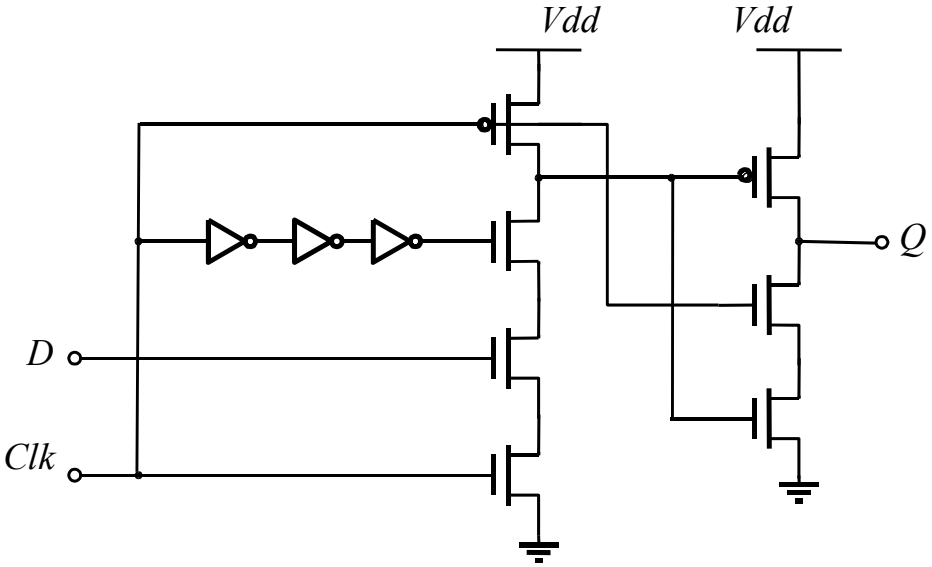
Consider an inverter, driving another identical inverter through a long piece of wire. The wire can be modeled as an RC ladder consisting of $N = 100$ segments, where each $R_i = 10\Omega$ and $C_i = 10$fF, as shown in figure. The inverters have equivalent resistance in low-to-high and high-to-low transitions of $R_{inv} = 1k\Omega$, an input capacitance of $C_{in} = 25$fF and a parasitic output capacitance of $C_{out} = 50$fF.



a) If the wire is initially discharged, and a VDD->0 step is applied to the input V_{in}, find the delay of the signal at the output node, V_{out}.

b) In order to minimize this delay insert one inverter after each *m* segments of wire. Assume that inserted inverters are identical to the one that is driving the wire. Find an optimal value of *m* that minimizes the delay. Ignore the polarity of the signal at the end of the wire (i.e. the number of inserted inverters does not have to be even).

PROBLEM 4. Sequential circuits. (10 pts)



a) (2 pts) Would the sequential circuit from the figure above be considered a latch, a master-slave latch pair or a pulse-triggered latch? Briefly explain your answer.

b) (5pts) All transistors in this circuit are unit-sized, with equivalent resistances R and gate capacitances C (ignore diffusion capacitances). Calculate the propagation delay $t_{Clk\text{-}Q}$ for high-to-low and low-to-high transitions. Load on the output Q is equal $12C$. Ignore the signal slopes in delay calculation.

c) (3pts) This circuit does not strictly follow the rules for designing sequential logic discussed in the class. List three major problems in the operation of this circuit.

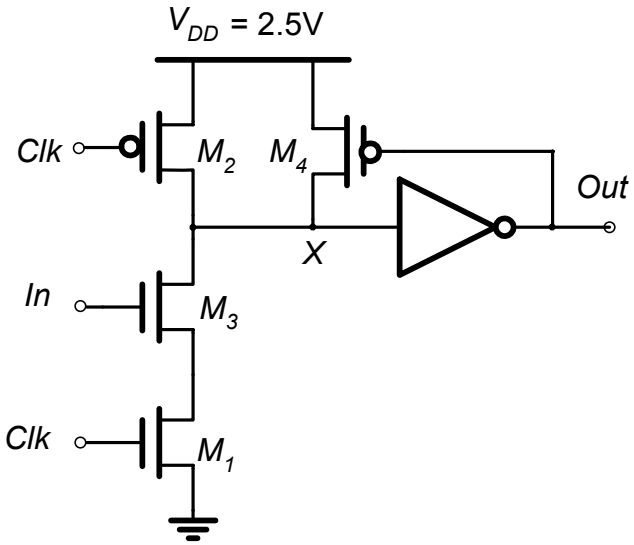
1. _____

2. _____

3. _____

PROBLEM 5: Dynamic Circuits. (8 points)

Keepers are frequently used in dynamic circuits to provide reliable operation.



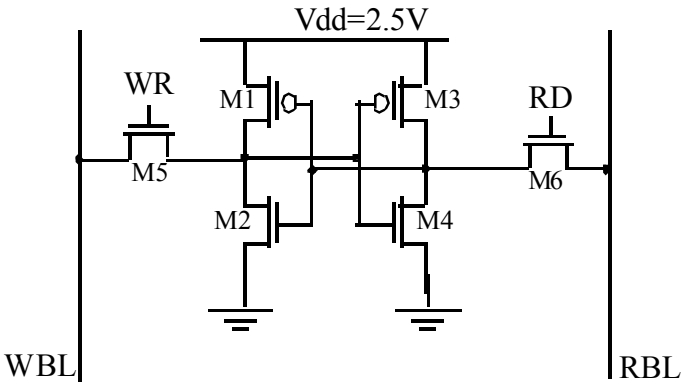
a) If M_1 and M_3 transistor widths are 2μm and M_2 is 1μm wide, there could be a limit on the size of transistor M_4 for proper operation of this dynamic inverter. Find the maximum width of transistor M_4, assuming that the output voltage stays constant during the critical part of transition. The inverter is symmetrically sized.

b) On the same graph, draw the voltage transfer functions (from input node *In* to node *X*, after clock rises) for this gate, for two cases:
   - without the keeper transistor M_4 and
   - when M_4 is largest possible, but the dynamic inverter still performs the function.

   Please label the breakpoints on the graph.

PROBLEM 6. Memory Design (10 points)

The figure below shows an SRAM cell that uses separate bit lines for read and write operations. During the write operation WR=*Vdd*, RD=0V, and during the read operation WR=0V, RD=*Vdd*. The RBL holds the last voltage read out between the read operations (i.e. RBL is not precharged to any value). For the inverters, assume that V_M=Vdd/2 with Vdd = 2.5V. Throughout the question, assume the long-channel transistor model. You may ignore body-effect! Also you may assume the bit-line capacitances are very large. Answer the following questions in terms of the (W/L) ratios of M1, M2, M3, and M4. You can make other reasonable assumptions if necessary.



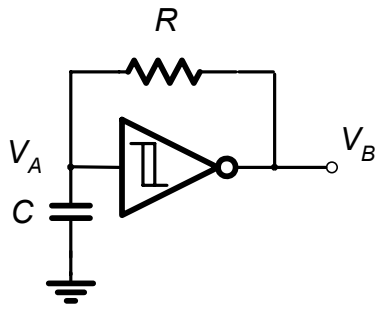
a) Determine the high and low value of the signals on the RBL?

b) Write down the constraints on the sizing of M5 (with respect to M1, M2, M3, and M4) for the memory cell to be functional? Just write the complete constraint equation - you do not need to solve it.

c) Write down the constraints on M6 for the memory cell to be functional? Just write the complete constraint equation - you do not need to solve it.

PROBLEM 7: Multivibrators (6 points)

The circuit from figure below, uses a Schmitt trigger with the following threshold voltages: $V_{M+} = 2V$, $V_{M-} = 1V$.



a) Identify whether the circuit is a monostable, bistable or astable.

b) Draw the waveforms at nodes A and B. Assume that the capacitor is initially discharged. Mark all important voltage levels, and time intervals.