San Jose State University
Department of Electrical Engineering
College of Engineering

Exam 2

EE 224 **Fall 2017**

Closed Book, Closed Notes, No electronic devices

Instructions:

❶ **There are four problems. They are weighted as shown. Interpretation of questions will not be given during the exam. If you are unsure about the meaning of a question, make an assumption, state what it is and continue.**

❷ **Work all four problems. Show all your work. Justify your answer. Partial credit will be granted for an answer but only if the intermediate work is shown.**

❸ **All writing must be on the paper provided (No additional, scratch paper allowed).**

❹ **Candidates guilty of any of following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:**

- **Making use of any books, papers or memoranda, calculators, cellphone, or any memory aid devices.**
- **Speaking or communicating with other candidates.**
- **Purposely exposing written papers with other candidates.**

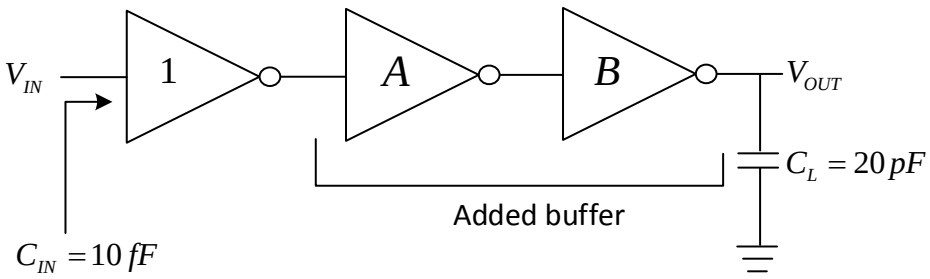
Problem	Possible	Score
1	25	
2	25	
3	25	
4	25	
Total	100	

❺ **Candidate should be prepared to produce, upon request, her/his SJSU identification card.**

❻ **Verify your name and enter your student identification number at the bottom of this page and sign.**

Name **Signature:**

PROBLEM 1: (25 points)



a) A large capacitance $C_L = 20\,pF$ is driven from a minimum size gate (with input capacitance $C_{IN} = 10\,fF$), you decide to introduce a two-stage buffer as shown in Figure. Assume that the intrinsic propagation delay of a minimum size inverter, $t_{INV} = 70\,ps$. Also assume that the input capacitance of a gate is proportional to its size, and there is no diffusion capacitance of inverter, $\gamma = 0$. Determine the sizing of the two additional stages that will minimize the propagation delay. (5 points)

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as f , f^2 , respectively.

$$f = \sqrt[N]{F} = \sqrt[3]{2000} = 12.6$$
$$t_p = Nt_{inv}\left(\gamma + f\right) = 3\left(70\,ps\right)\left(12.6\right) = 2646\,ps$$

b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? Ignore polarity of output, VOUT. (10 points)

From the text, we know that the minimum delay occurs when $f = e$. Therefore,

$$N = \frac{\ln 2000}{\ln e} = 7.6$$

N=7 or 8, both case are right for this question. However, N=7 is better choice since the delay difference is very small amount but power consumption difference is large. If polarity should be concerned, N=8 cannot be right choice.

(i) In case of N=7

$$f = \exp\left[\frac{\ln 2000}{7}\right] = 2.96$$

so new

$$t_p = 7\left(70\,ps\right)\left(2.96\right) = 1450\,ps$$

(ii) In case of N=8

$$f = \exp\left[\frac{\ln 2000}{8}\right] = 2.58$$

so new

$$t_p = 8(70\,ps)(2.58) = 1445\,ps$$

c) Determine a closed form expression for the energy consumption in the circuit of part a) with 3-stage inverter chain. Consider gate capacitances and C_L only in your analysis. What is the energy consumption for a supply voltage of 1.2V? Assume that the activity factor, α, is 1, i.e. there are $0^- > 1$ transition and $1^- > 0$ transition at every cycle. (10 pts)

The energy consumption is determined as follows

If α=1 then there are 0->1 transition and 1->0 transition at every cycle.

i) Including C_{in}

$$E_c = C_{total}V_{DD}^2 = (C_{in} + C_A + C_B + C_L)V_{DD}^2 = \left[C_{in}\left(1 + f + f^2\right) + C_L\right]V_{DD}^2$$

$$E_c = \left[10\,fF\,(1 + 12.6 + 12.62) + 20\,pf\right]1.2^2 = 31.28\,pJ$$

Excluding C_{in}

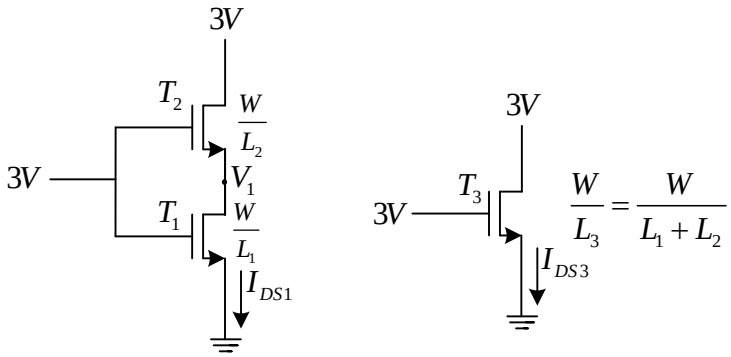
$$E_c = C_{total}V_{DD}^2 = (C_A + C_B + C_L)V_{DD}^2 = \left[C_{in}\left(f + f^2\right) + C_L\right]V_{DD}^2$$

$$E_c = \left[10\,fF\,(12.6 + 12.62) + 20\,pf\right]1.2^2 = 31.27\,pJ$$

Both i) & ii) are right. Actually, there is no big difference.

PROBLEM 2: (45 points)

Prove the transistor equivalency says that 2 transistors in series having the same width is equivalent to a single transistor with that width and the lengths added together as shown below by finding I_{D1} and I_{D3}. Find also V_1 . (Ignore body effect find finite output impedance).



T_3 *Sat* $V_{DS} > V_{GS} - V_{TN}$

$\mu_n = 120\mu A/V_2$

$V_{TN} = 0.4V$

$W = 1\mu m, \quad L_1 = 0.25\mu m, \quad L_2 = 0.5\mu m,$

Solution:

$M_1 \quad Nonsat \quad M_1 \quad Sat$

$$I_{DS1} = \mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[(V_{GS1} - V_{Tn})V_{DS1} - \frac{V_{DS1}^2}{2}\right] = 120\times10^{-6}\left(\frac{1}{0.25}\right)_1\left[(3-0.4)V_1 - \frac{V_1^2}{2}\right]$$

$$I_{DS2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2(V_{GS1} - V_{Tn})^2 = \frac{120\times10^{-6}}{2}\left(\frac{1}{0.5}\right)_2(3-0.4-V_1)^2$$

$$I_{DS1} = I_{DS2} = 120\times10^{-6}\left(\frac{1}{0.25}\right)_1\left[(3-0.4)V_1 - \frac{V_1^2}{2}\right] = \frac{120\times10^{-6}}{2}\left(\frac{1}{0.5}\right)_2(3-0.4-V_1)^2$$

$V_1 = 0.477 \quad \& V_1 = 4.72$

$$I_{DS2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2(V_{GS1} - V_{Tn} - V_1)^2 = \frac{120\times10^{-6}}{2}\left(\frac{1}{0.5}\right)_2(3-0.4-0.477)^2 = 541\mu A$$

$$I_{DS3} = I_{DS2} = I_{DS1} = 541\mu A = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_3(V_{GS1} - V_{Tn})^2 = 120\times10^{-6}\left(\frac{1}{L}\right)_3(3-0.4)^2$$

$L_3 = 0.75 = L_1 + L_2$

PROBLEM 3: (25 points)

A CMOS inverter has the following device parameters:

NMOS: $V_{TN}=0.5V$ $k_n=115\mu A/V^2$ $(W/L)_n=2$

PMOS: $V_{TP}=-0.6V$ $k_p=-30\mu A/V^2$ $(W/L)_p=4$

The power supply voltage is $V_{DD}=2.5V$, and the output load capacitance of 0.5Pf. Assume that CMOS inverter is implemented with long-channel devices, and that channel modulation is neglected.

a) Calculate the low-to-high and high-to-low delay times of the output signal. (10 points)

$$\Delta V = V_{DD} - \frac{V_{DD}}{2} = 1.25V \quad \& \quad C = 0.5\,pF$$

Long channel => no vel. Sat.

$$t_{PHL}: \quad V_{GS}=V_{DD}, \quad V_{DS}=V_{DD} \quad \Rightarrow sat.$$

$$I_{2.5} = \frac{1}{2}k_n\left(\frac{W}{L}\right)_n\left(V_{GS}-V_t\right)^2 = 460\mu A$$

$$V_{GS}=V_{DD}, \quad V_{DS}=\frac{V_{DD}}{2} \quad \Rightarrow linear$$

$$I_{1.25} = k_n\left(\frac{W}{L}\right)_n\left[\left(V_{GS}-V_t\right)V_{DS} - \frac{{V_{DS}}^2}{2}\right] = 395\mu A$$

$$I_{avg} = \frac{1}{2}\left(460+395\right)\mu A = 427.5\mu A$$

$$t_{PHL} = \frac{C\Delta V}{I_{avg}} = 1.46n\sec$$

$$t_{PLH}: \quad V_{GS}=-V_{DD}, \quad V_{DS}=-V_{DD} \quad \Rightarrow sat.$$

$$I_{2.5} = \frac{1}{2}k_p\left(\frac{W}{L}\right)_p\left(V_{GS}-V_t\right)^2 = 216.6\mu A$$

$$V_{GS}=-V_{DD}, \quad V_{DS}=-\frac{V_{DD}}{2} \quad \Rightarrow linear$$

$$I_{1.25} = k_p\left(\frac{W}{L}\right)_p\left[\left(V_{GS}-V_t\right)V_{DS} - \frac{{V_{DS}}^2}{2}\right] = 191.25\mu A$$

$$I_{avg} = \frac{1}{2}(191.25 + 216.6)\,\mu A = 203.925\mu A$$

$$t_{PLH} = \frac{C\Delta V}{I_{avg}} = 3.06n\sec$$

b) Determine the maximum frequency of the output signal. (5 Points)

Solution:

$$t_P = \frac{1}{2}(t_{PLH} + t_{PHL}) = \frac{1}{2}(3.06 + 1.46) = 2.26n\sec$$

$$f_{\max} = \frac{1}{t_p} = 442MHz$$

c) Calculate the dynamic power dissipation at this maximum frequency. Neglect any diffusion capacitance. (5 Points)

Solution:

$$P_{dyn} = \alpha_{0\to T} C V_{DD}^2\ f_{clk}$$

$$= (0.5pF)(2.5V)^2\left(442\times10^6 Hz\right) = 1.38mW$$

d) Assume that the output load capacitance is mainly dominated by fixed fanout components (which are independent of W_n and W_p). We want to re-design the inverter so that the propagation delay times are reduced by 25%. Determine the required channel dimensions of the NMOS and PMOS transistors. How does this re-design influence the dynamic power dissipation? Which of the two designs produces lower Power-Delay-Product? (5 Points)

Solution:

$$t_{pnew} = 0.75 \quad t_{pold} = 1.695n\sec$$

Reduce each,

$$t_{PLH}\ \&\ t_{PHL}\ \text{by } 25\% \ \rightarrow\ \text{increase}\left(\frac{W}{L}\right)\text{ by }\frac{1}{0.75} = \frac{4}{3}$$

So new channel dimensions are

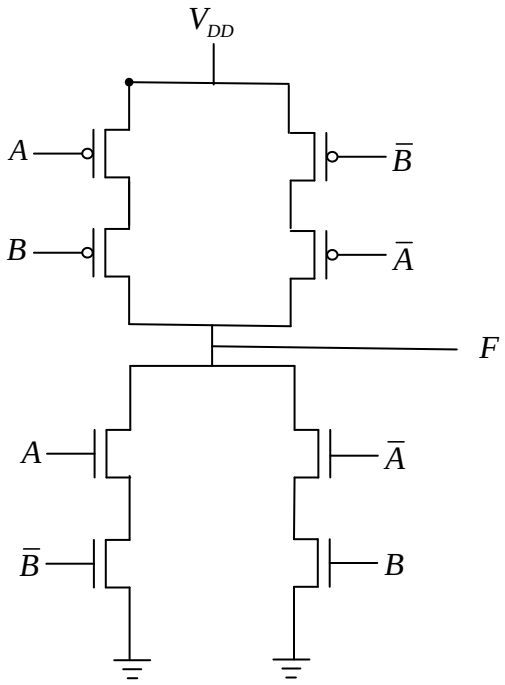
$$\left(\frac{W}{L}\right)_n = \frac{8}{3},\ \left(\frac{W}{L}\right)_p = \frac{16}{3}$$

$$t_{PLH} = 2.295\,n\sec,\quad t_{PHL} = 1.095\,n\sec \quad \rightarrow t_P = 1.695\,n\sec \rightarrow f_{\max} = 590MHz$$

The PDPs are exactly the same since the increase in frequency and power is compensated by same decrease in t_p .
Also there is no considerable change in C due to assumption of large fanout.

PROBLEM 4: (25 points)

Given the complex gate below:



a) Draw the truth table and determine the logic function of the complex gate shown in figure. (10 points).

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

This is an XNOR gate.

This is an XNOR gate.

b) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2/1). What is logical effort of this gate for each input ($\left(A, \bar{A}, B, \bar{B}\right)$? (10 pts)

Solution:
M1=M2=M5=M6=2

M3=M4=M7=M8=4

$$LE_A = \frac{2+4}{3} = 2$$

$$LE_B = \frac{2+4}{3} = 2$$

$$LE_{\bar{A}} = \frac{2+4}{3} = 2$$

$$LE_{\bar{B}} = \frac{2+4}{3} = 2$$

c) Suppose we are only interested in the delay of the falling output transition when input A is pulled high and input B is pulled low. Size the transistor M1 and M2 to make the logical effort of this gate for the input A the same as a unit inverter. For transistors M3-M8, use the sizes you found in (b). (10 pts)

$$\mathrm{LE_A} = \left(\frac{\left(\frac{2}{\mathrm{M2}}\right) \times (4 + \mathrm{M2})}{1 \times 3} \right) = 1$$

$$\Rightarrow \mathrm{M2} = 8$$

$$\mathrm{M2} = \mathrm{M1} = 8$$