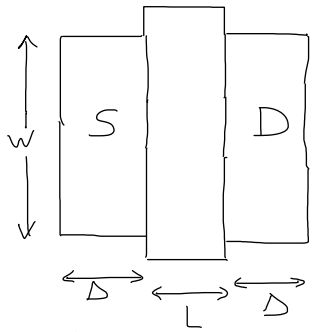
* Summary of Mosfet parasitic capacitors:

	$C_{gse}=C_{gde}$	C_{gb}	C_{gsi}	C_{gdi}	C_{sbi}	C_{dbi}
cutoff	$C_{ox}.W.L_{ov}$	$C_{ox}.W.L_{eff}$	$\emptyset$	$\emptyset$	$\emptyset$	$\emptyset$
triode	$C_{ox}.W.L_{ov}$	$\emptyset$	$\frac{1}{2}C_{ox}WL_{eff}$	$\frac{1}{2}C_{ox}WL_{eff}$	$\frac{1}{2}C_{jLeff}.W$	$\frac{1}{2}C_jL_{eff}.W$
saturation (active)	$C_{ox}.W.L_{ov}$	$\emptyset$	$\frac{2}{3}C_{ox}WL_{eff}$	$\frac{1}{3}C_{ox}WL_{eff}$	$\frac{2}{3}C_{jLeff}W$	$\frac{1}{3}C_jL_{eff}W$

	C_{sbe}	C_{dbe}
cutoff	$A_sC_j+P_sC_{jsw}$	$A_d.C_j+P_d.C_{jsw}$
triode	$A_s.C_j+P_s'C_{jsw}$	$A_dC_j+P_s'.C_{jsw}$
saturation (active)	$A_s.C_j+P_s'C_{jsw}$	$A_d.C_j+P_d'.C_{jsw}$



$C_{ox}\left[\frac{F}{m^2}\right]$, $C_j\left[\frac{F}{m^2}\right]$, $C_{jsw}\left[\frac{F}{m}\right]$

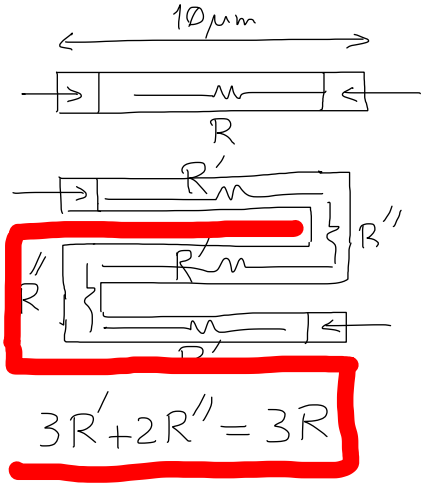
$A_s=\Delta.W$, $P_s=2(\Delta+W)$, $P_s'=2\Delta+W$

$A_d=\Delta.W$, $P_d=2(\Delta+W)$, $P_d'=2\Delta+W$

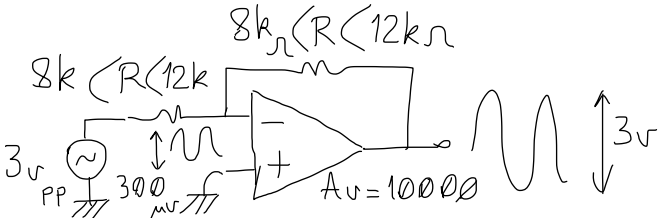
$$C_j=\frac{C_{j\emptyset}\ \left[\frac{F}{m^2}\right]}{\left(1+\frac{V_r}{\phi_0}\right)^n},\qquad C_{jsw}=\frac{C_{jsw\emptyset}\ \left[\frac{F}{m}\right]}{\left(1+\frac{V_r}{n}\right)^n}$$

$C_{jsw}\approx C_j.X_j$

X_j: junction depth



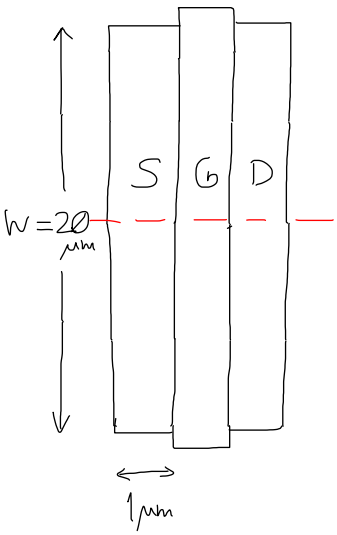
$3R'+2R''=3R$

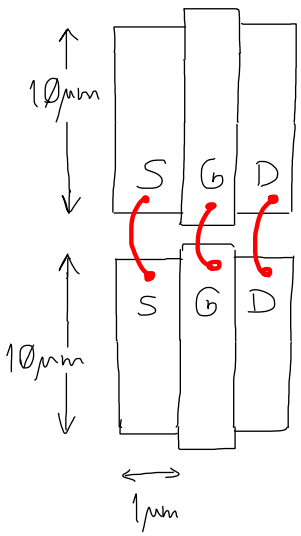


Tolerance of on-chip resistors is 20% (ideally R=10kΩ)

* interdigitated layout minimizes mismatch

* layout :

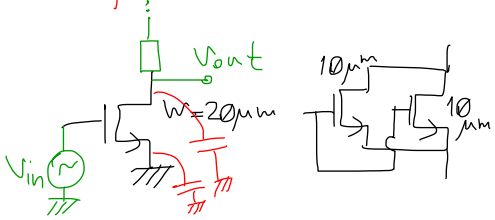




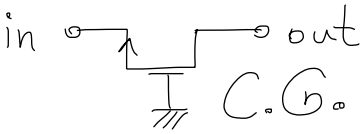
$A_S = 20\mu m \times 1\mu m = A_d$

$P_S = 20\mu + 1\mu m + 1\mu m = P_d$

* In Analog, 99.9% of the time, all transistors must operate in the active

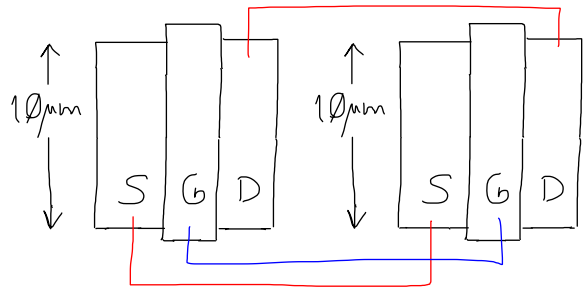


this will be a transistor with 20μm width

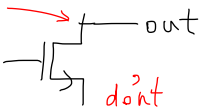


$A_S = (10\mu m \times 1\mu m) + (10\mu m \times 1\mu m) = A_d$

$P_S = (10\mu m + 1\mu m + 1\mu m) + (10\mu m + 1\mu m + 1\mu m) = P_d$



critical node

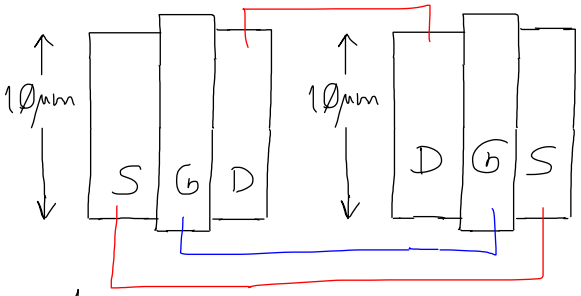


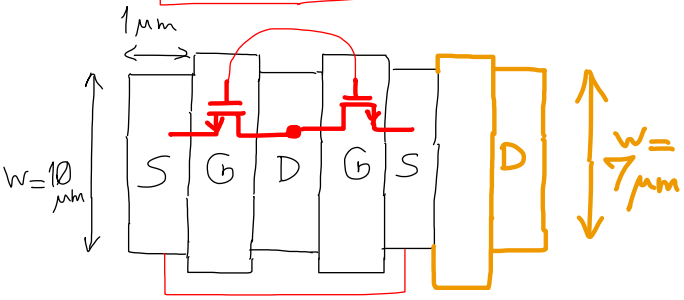
don't care

* Always use interdigitated multiple finger layout

$P_S = (10\mu m + 1\mu m + 1\mu m)2$

$P_d = 1\mu m + 1\mu m$

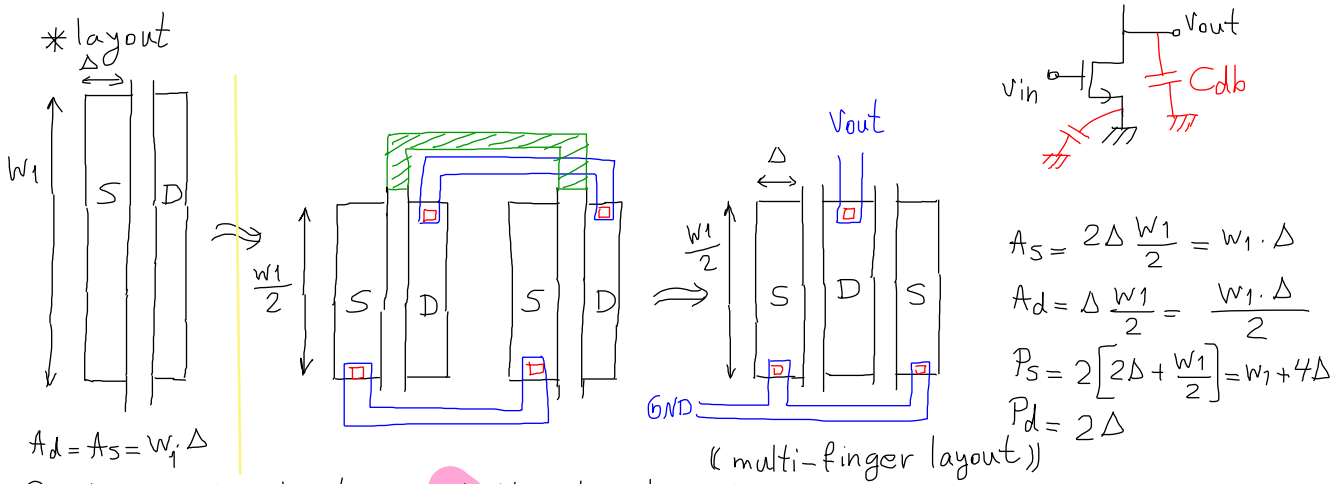




$W = 2\ \text{fingers} \times 10\mu m = 20\mu m$

$A_S = 10\mu m \times 1\mu m \times 2$

$A_d = 10\mu m \times 1\mu m$



$A_d = A_S = W_1 \cdot \Delta$

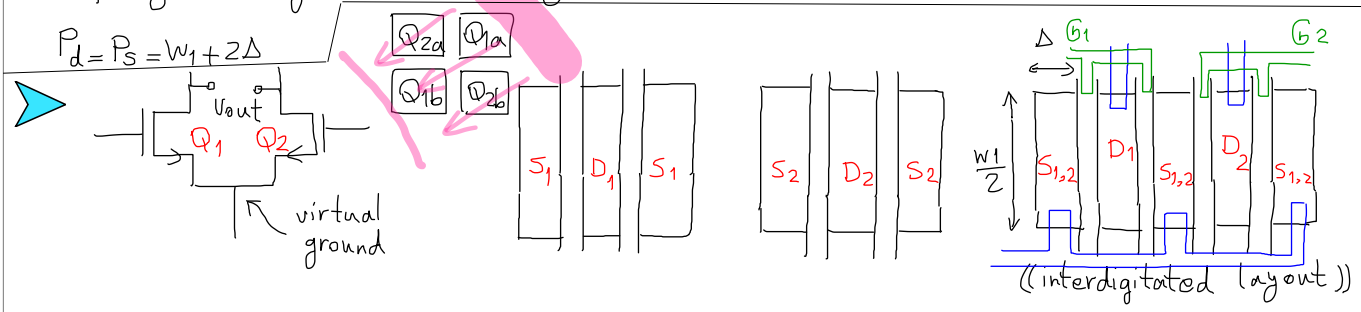
$A_S = 2\Delta \frac{W_1}{2} = W_1 \cdot \Delta$

$A_d = \Delta \frac{W_1}{2} = \frac{W_1 \cdot \Delta}{2}$

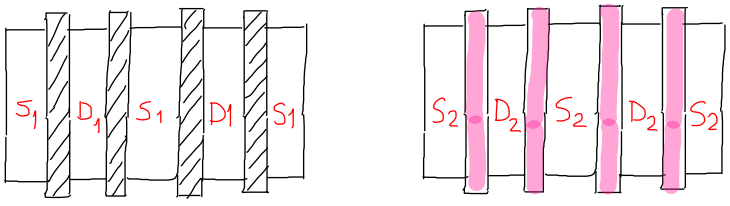
$P_S = 2\left[2\Delta + \frac{W_1}{2}\right] = W_1 + 4\Delta$

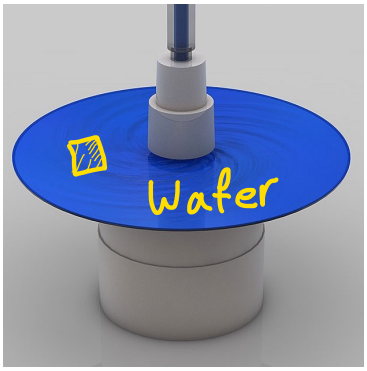
$P_d = 2\Delta$

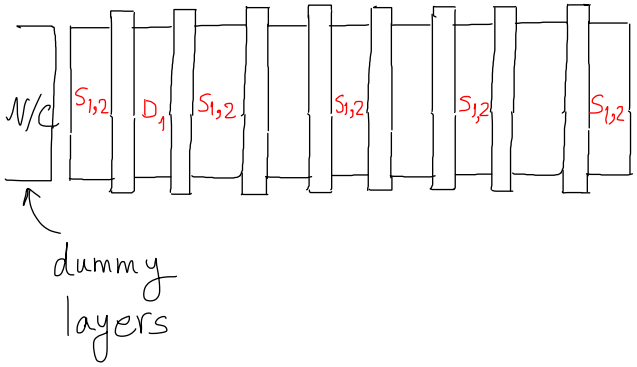
Periphery is the junction excluding the channel

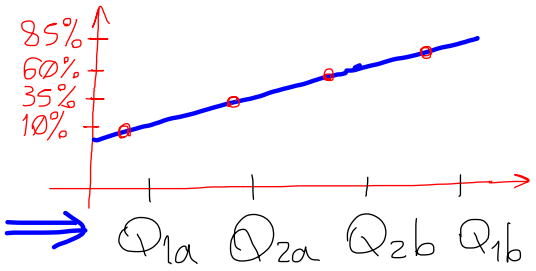


* Example of interdigitated layout with Q_1 and Q_2 designed using 4 fingers

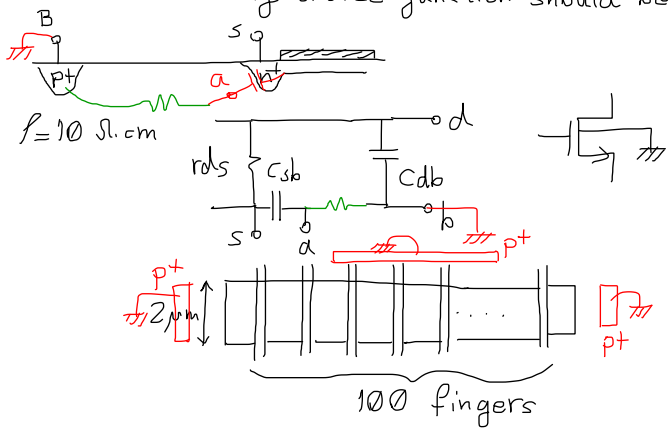








* Bulk rule : the minimum distance between bulk to any source junction should be less than 10μm



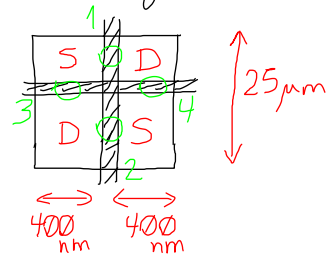
$A_s = 3\frac{W_1}{2}\Delta$

$A_{d_1} = \frac{W_1}{2}\Delta = A_{d_2}$

$P_s = 2\left[2\Delta + \frac{W_1}{2}\right] + 2\Delta$

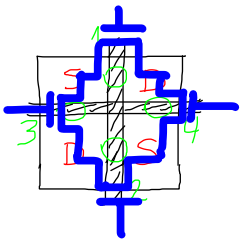
$P_{d_1} = 2\Delta = P_{d_2}$

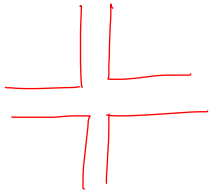
Waffle Layout :



$A_D = A_S = 2 \times \frac{25\mu m}{2} \times 400_{nm}$

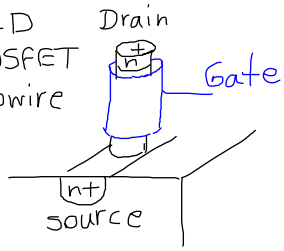
$P_D = P_S = 2\left[400_{nm} + \frac{25\mu m}{2}\right]$





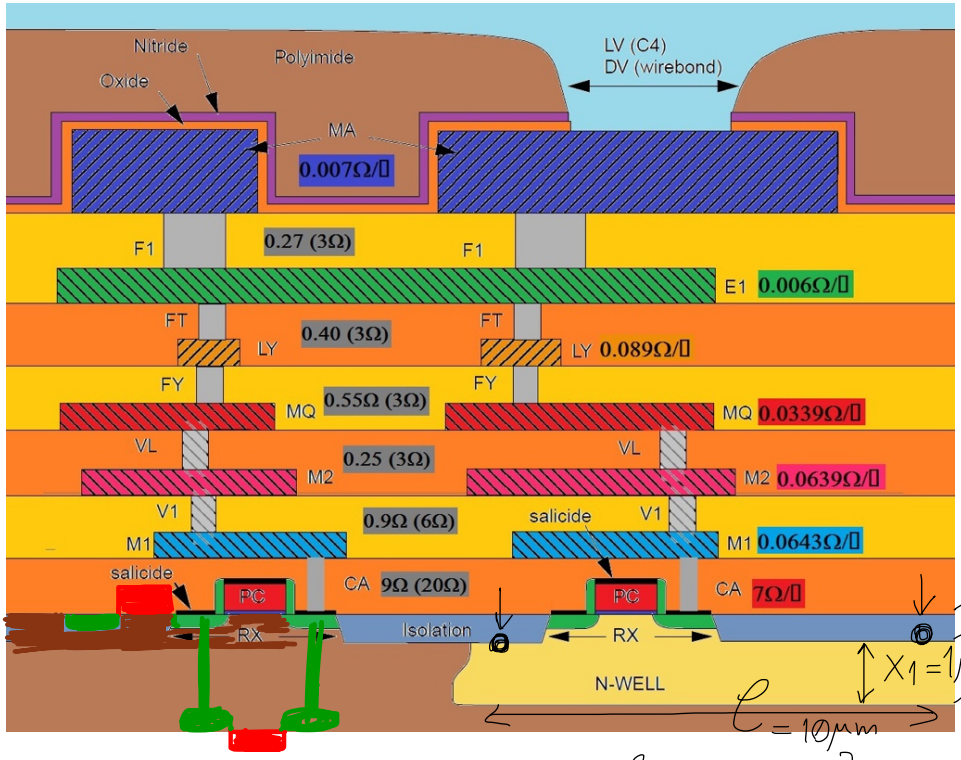
X DRC error

3-D MOSFET nanowire



Also look at FinFets

Electrical Parameter PDF



$\rho = 10\ \Omega.cm$

$R = \rho \cdot \frac{L}{A} = 10 \times 10^{-2} \times \frac{10 \times 10^{-6}}{10^{-6} \times 10^{-6}} = 1M\Omega$