EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 6: Performance Metrics

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Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	~~OPAMP and bias circuits review~~
12-Feb	~~SC circuits review~~
14-Feb	~~Sample and Hold Amplifier - Reading materials~~
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: latch offset, preamp, autozero
26-Feb	Finish Flash ADC
28-Feb	DAC Architectures - Resistor, R-2R
5-Mar	DAC Architectures - Current steering, Segmented
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	$\boxed{\text{Midterm exam}}$
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

Performance Metrics
EE223 Review

No class on Feb 14, Wed.

Read Lecture Note

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

Announcements

- No class this Wednesday
  - ISSCC conference

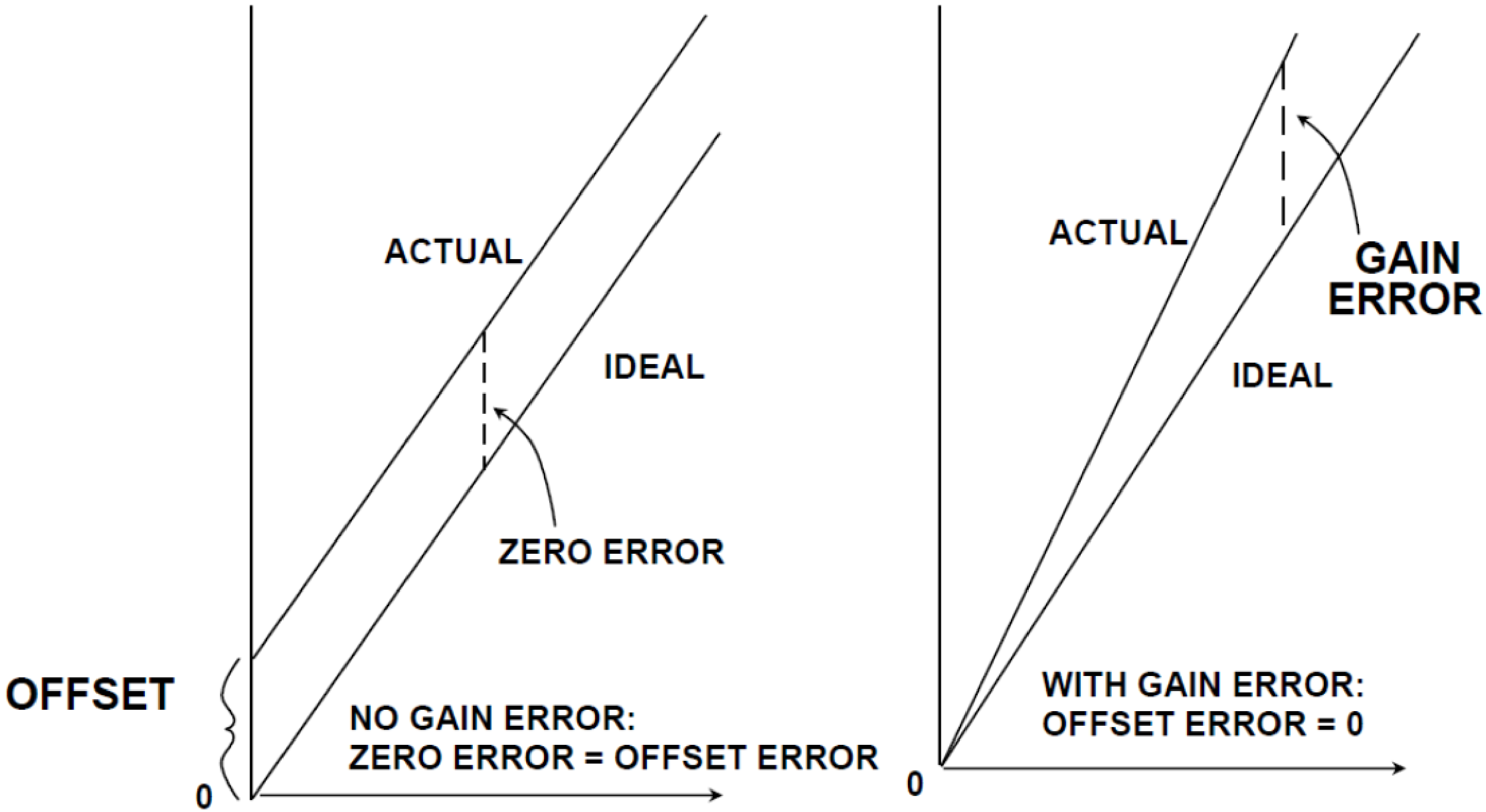
- Reading materials posted in Canvas file section
  - Lecture 7 – EE223 Review

- Homework posted in Canvas – Due Feb 26, Monday
  - 4-bit Flash ADC

Agenda

- ADC Performance Metrics
  - Static
  - Dynamic

Offset and Gain Errors

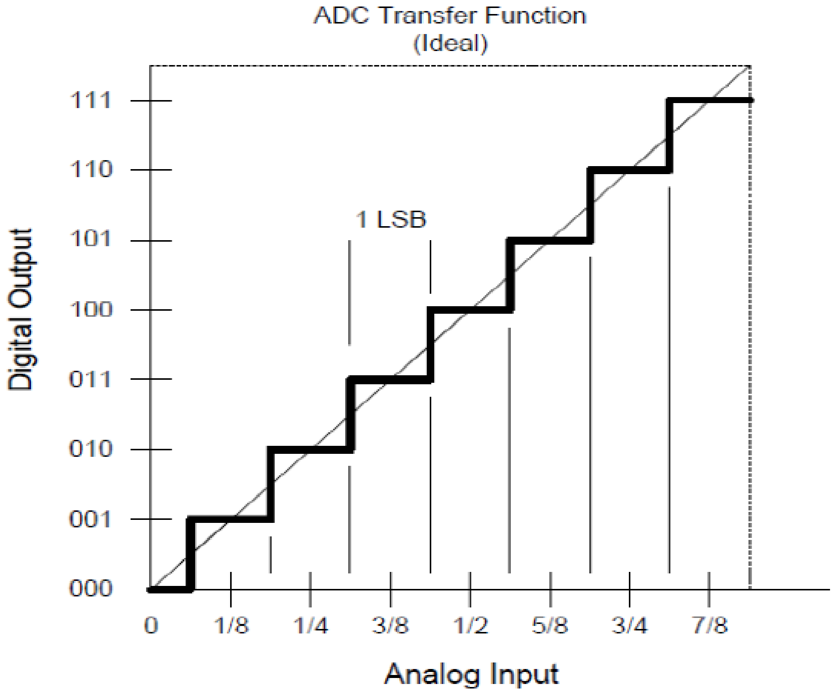


Performance Parameters

- **DC Performance**
  - Differential Non-Linearity (DNL)
  - Integral Non-Linearity (INL)
- **AC Performance**
  - Harmonic Distortion
  - Worst Harmonic
  - Total Harmonic Distortion (THD)
  - Total Harmonic Distortion Plus Noise (THD + N)
  - Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N +D)
  - Effective Number of Bits (ENOB)
  - Signal-to-Noise Ratio (SNR)
  - Analog Bandwidth (Full-Power, Small-Signal)
  - Spurious Free Dynamic Range (SFDR)
  - Two-Tone Intermodulation Distortion
  - Noise Power Ratio (NPR) or Multitone Power Ratio (MPR)

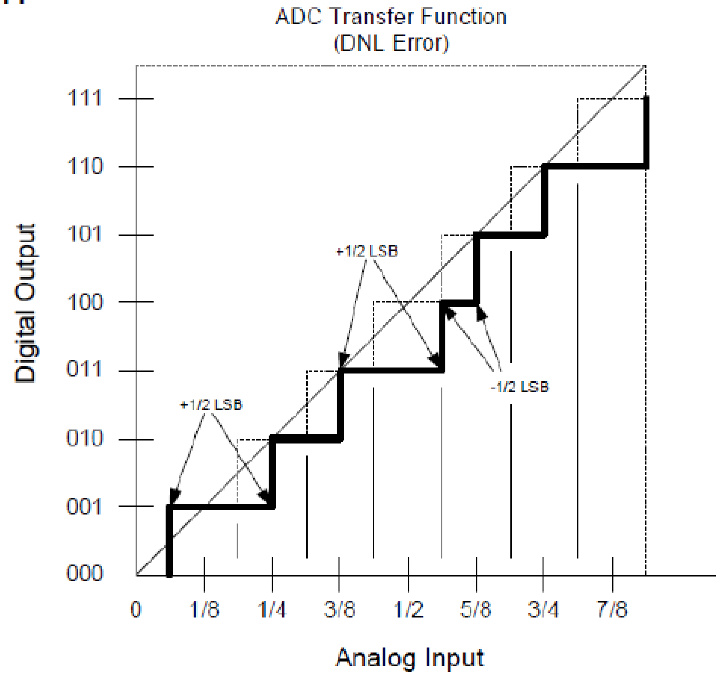
Ideal DC Characteristic

- Ideal ADC code transitions are exactly 1 LSB apart.
- For an N-bit ADC, there are 2^N codes. (1 LSB = $FS/2^N$)
- For this 3-bit ADC, 1 LSB = ($1V/2^3 = 1/8$)
- Each "step" is centered on an eighth of full scale



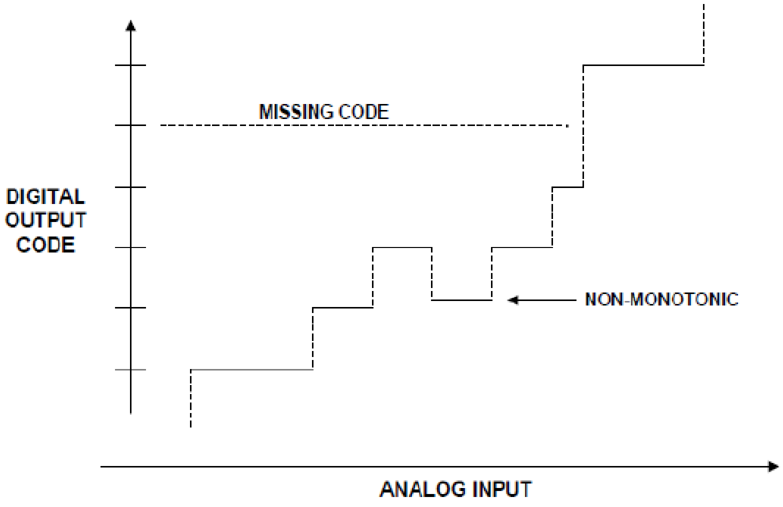
Differential Non Linearity (DNL)

- The deviation of an actual code width from the ideal 1 LSB code
- DNL error is measured in LSBs
- Results in narrow or wider code widths than ideal
- Results in additive noise/spurs beyond the effects of quantization



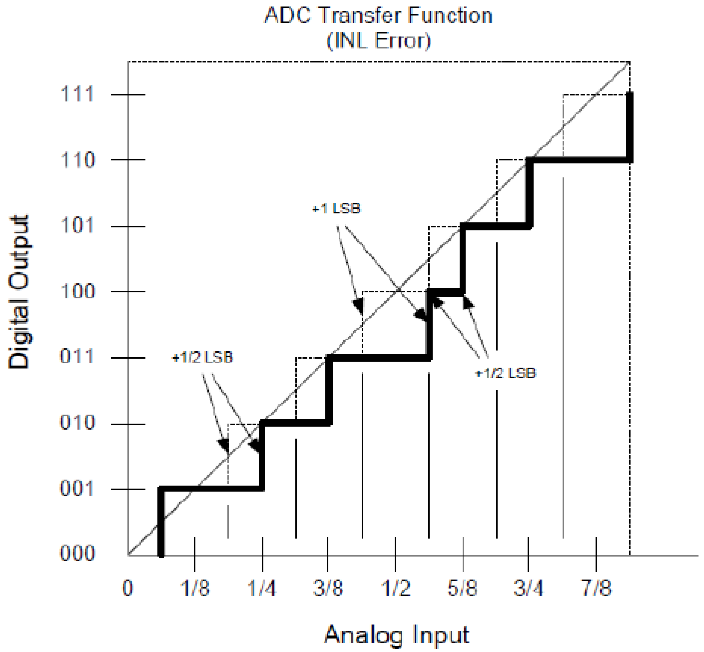
DNL Effects

- *Missing Codes* — An ADC has missing codes if an infinitesimally small change in voltage causes a change in result of two codes, with the intermediate code never being set. A DNL of −1.0 LSB indicates the ADC has missing.
- *Non-Monotonicity* — An ADC is *monotonic* if it continually increases conversion result with an increasing voltage (and vice versa). A non-monotonic ADC may give a lower conversion result for a higher input voltage, which may also mean that the same conversion may result from two separate voltage ranges.



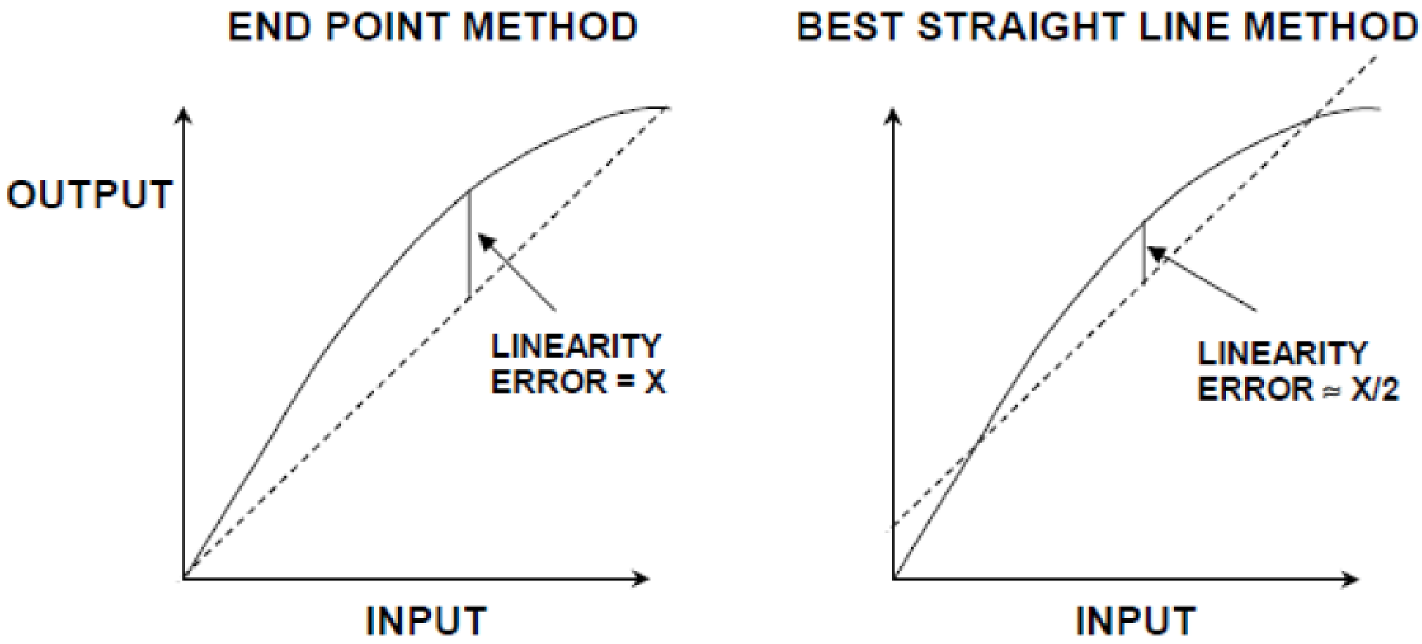
Integral Non Linearity (INL)

- The deviation of an actual code transition point from its ideal position on a straight line drawn between the end points of the transfer function.
- INL is calculated after offset and gain errors are removed
- Results in additive harmonics and spurs



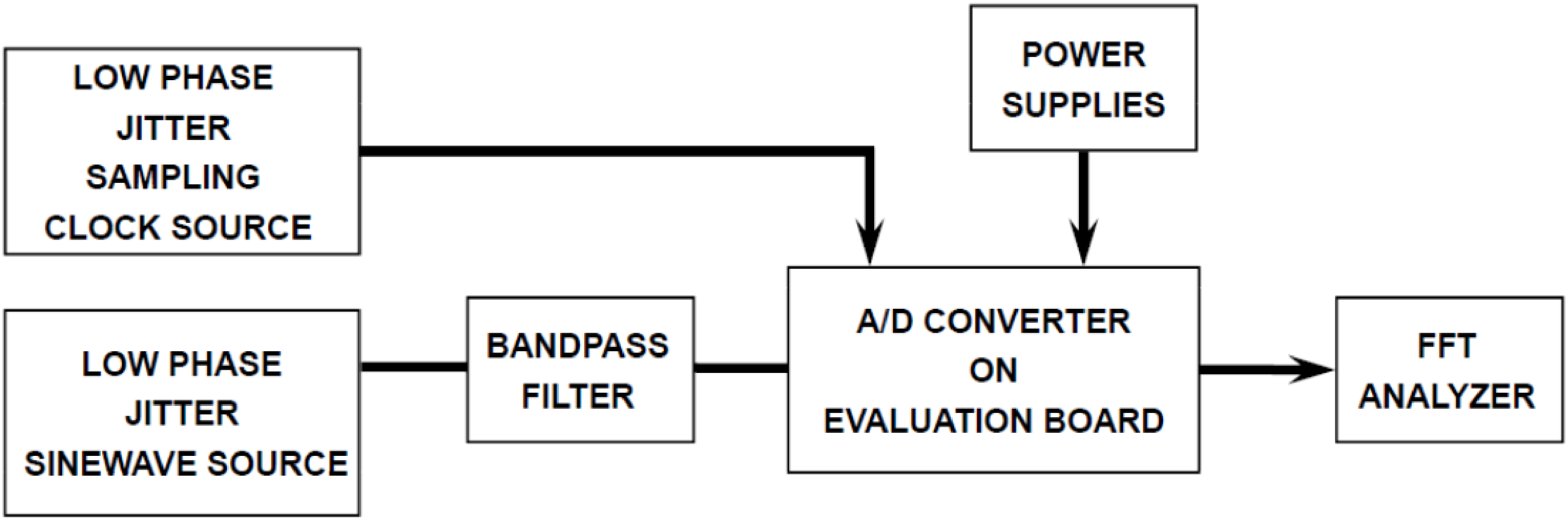
INL Measurement Methods

- *End Point Method* : the deviation is measured from the straight line through the origin and the full-scale point (after gain adjustment)
- *Best Straight Line Method* : the best fit straight line is drawn through the transfer characteristic of the device using standard curve fitting techniques, and the maximum deviation is measured from this line



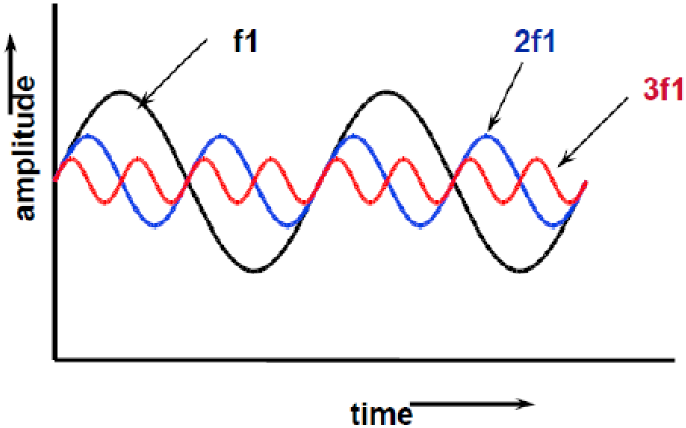
Dynamic Testing of ADC

- A *Fast Fourier Transform* (FFT) analyzer is used to measure dynamic performance

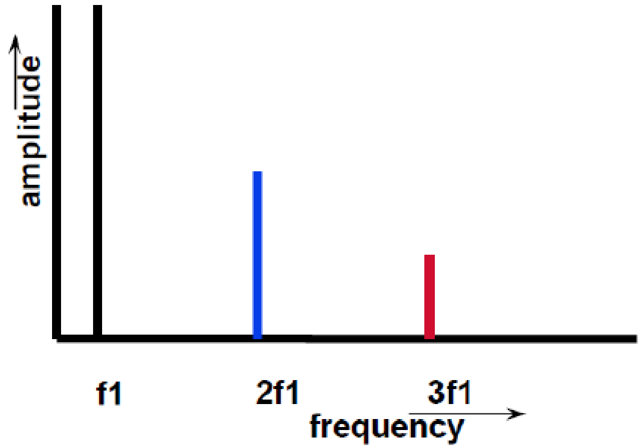


FFT

- The Fast Fourier Transform converts a signal from time domain….



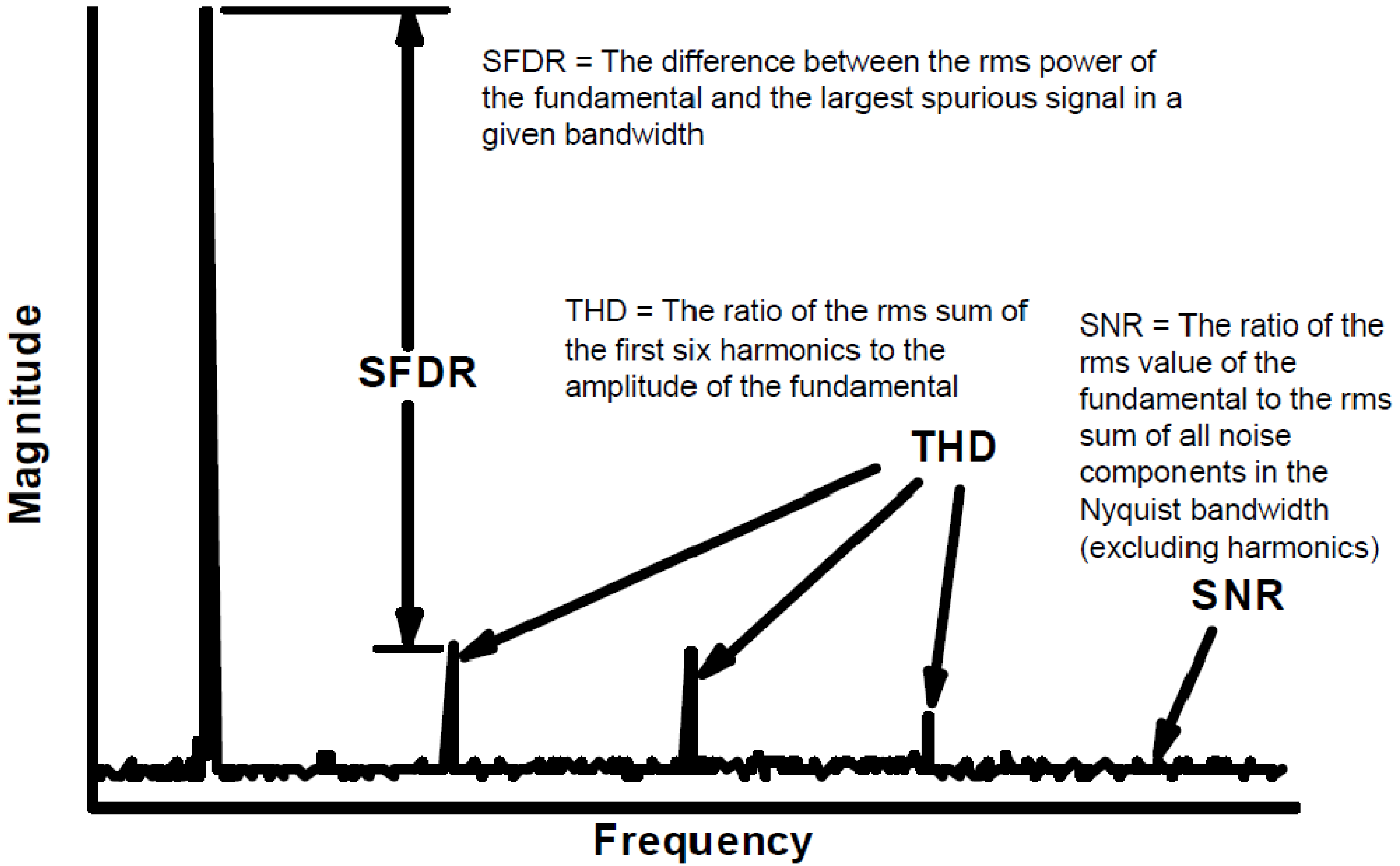
….to frequency domain



SINAD, ENOB, SNR

- **SINAD (Signal to Noise and Distortion Ratio)**
  - The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, including harmonics, but excluding DC
- **ENOB (Effective Number of Bits)**
  - $$ENOB = \frac{SINAD - 1.76\,dB}{6.02}$$
- **SNR (Signal to Noise Ratio)**
  - The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other spectral components, excluding the first five harmonics and DC

SFDR, THD, SNR


SFDR = The difference between the rms power of the fundamental and the largest spurious signal in a given bandwidth
THD = The ratio of the rms sum of the first six harmonics to the amplitude of the fundamental
SNR = The ratio of the rms value of the fundamental to the rms sum of all noise components in the Nyquist bandwidth (excluding harmonics)
SFDR
THD
SNR
Magnitude
Frequency

SQNR

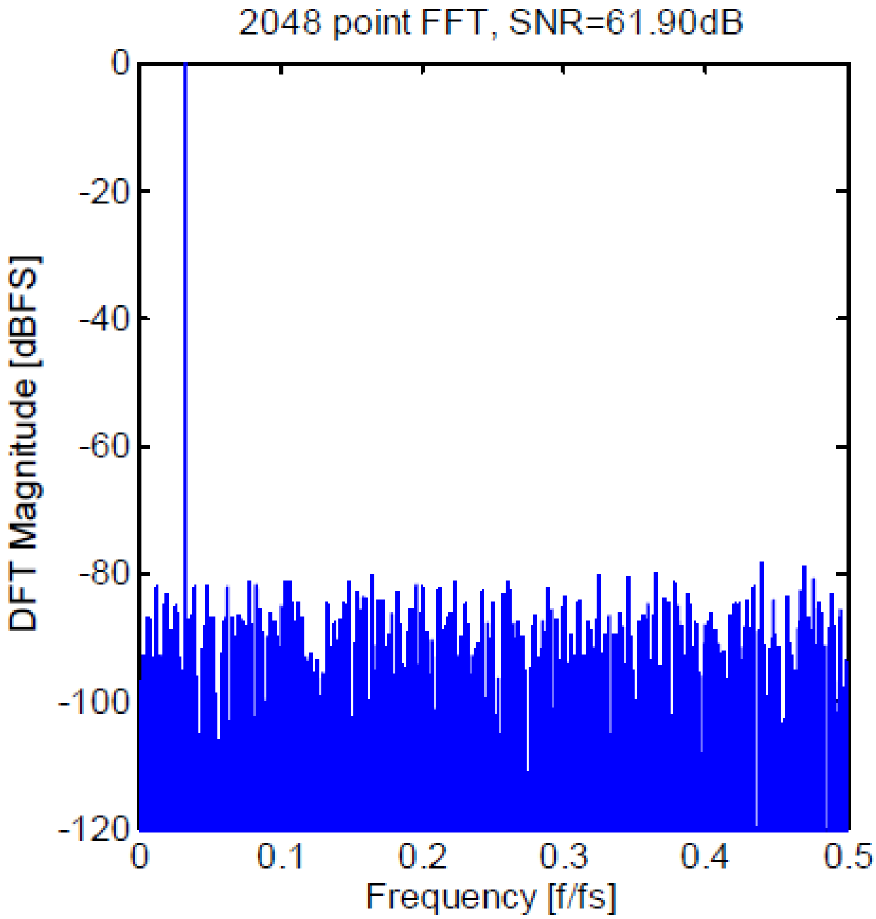
$$\mathrm{SQNR} = \frac{\text{Signal Power}}{\text{Quantization Noise Power}}$$

$$= \frac{\frac{1}{2}\left(\frac{V_{FS}}{2}\right)^2}{\frac{1}{12}\left(\frac{V_{FS}}{2^N}\right)^2} = \frac{3}{2}\cdot 2^{2N}$$

$$= 6.02 \cdot N + 1.76 \text{ [dB]}$$

$$= 6.02 \cdot 10 + 1.76 \text{ [dB]}$$

$$= 61.9 \text{ dB}$$



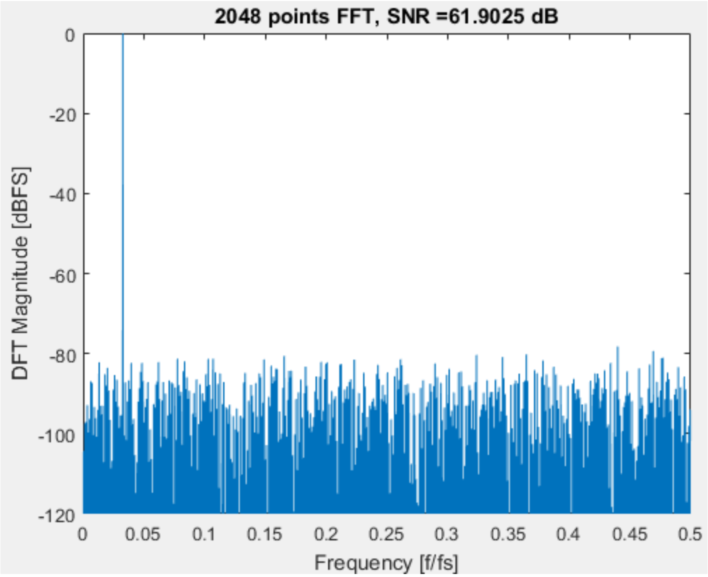
FFT Spectrum of Quantized Signal

```
clear all; clc; close all;
N = 2048;                  % FFT size
cycles = 67;               % Signal bin
fs = 1000;                 % Sampling rate
fx = cycles*fs/N;          % Signal frequency
B = 10;                    % ADC resolution
LSB = 2/2^B;               % LSB size

t = 0:N-1;                 % time sequence
x = cos(2*pi*fx/fs*t);     % Signal sequence
x = round(x/LSB)*LSB;      % Quantized signal
s = abs(fft(x))+ eps;      % Take FFT
s = s(1:end/2)/N*2;        % Take half of the spectrum and normalize

sigbin = cycles + 1;
noise = [s(1:sigbin-1), s(sigbin+1:end)];
SNR = 10*log10( s(sigbin)^2/sum(noise.^2) );
fprintf('SNR = %0.4f\n',SNR);

s = 20*log10(s);           % dB relative to full-scale
f = [0:N/2-1]/N;           % frequency vector
plot(f, s);
axis([0 0.5 -120 0]);
xlabel('Frequency [f/fs]');
ylabel('DFT Magnitude [dBFS]');
title(strcat(num2str(N),' points FFT, SNR = ', num2str(SNR), ' dB'));
```



fft_p55.m

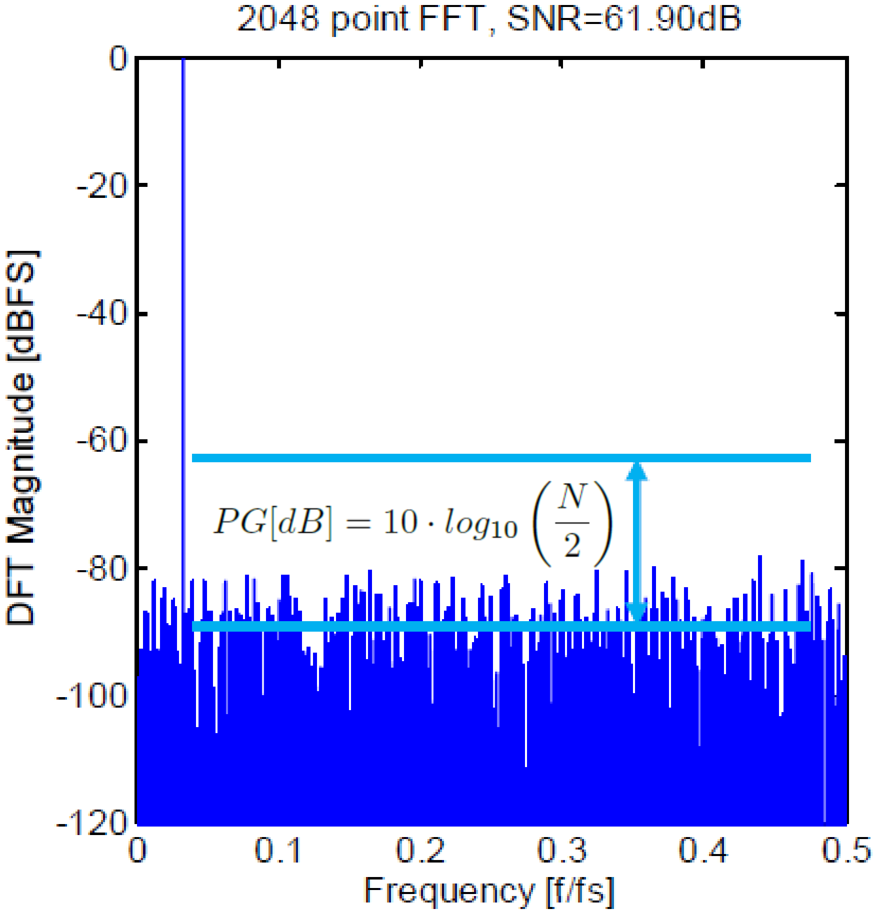
FFT Noise Floor

$$N_{floor} = -61.9\text{ dBc} - 10\log\left(\frac{2048}{2}\right)$$

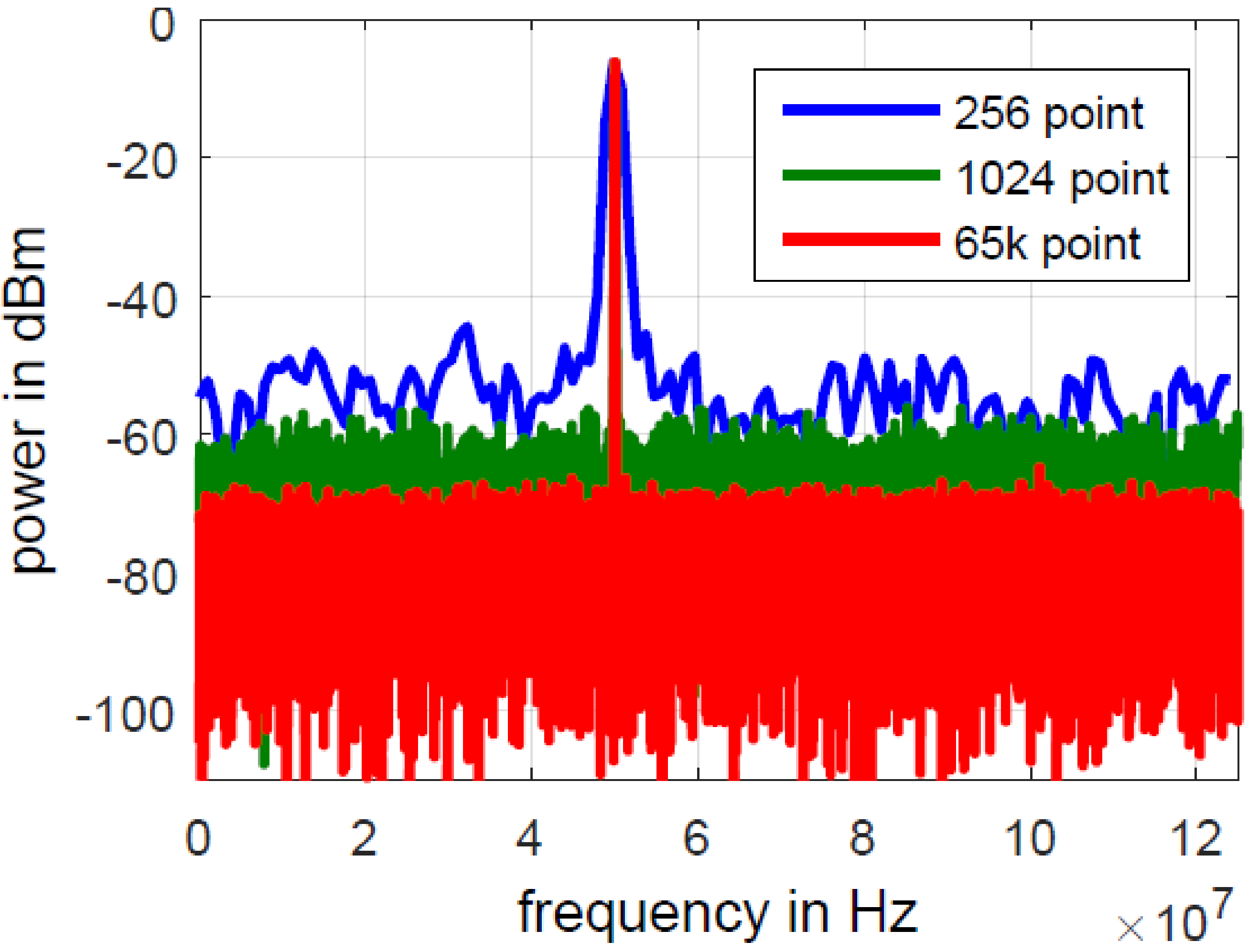
$$= -61.9\text{ dBc} - 30.1\text{ dB}$$

$$= -92\text{ dBc}$$

- Depends on FFT size
- Plot is "useless" if FFT size is not specified



FFT Processing Gain



SNDR and ENOB

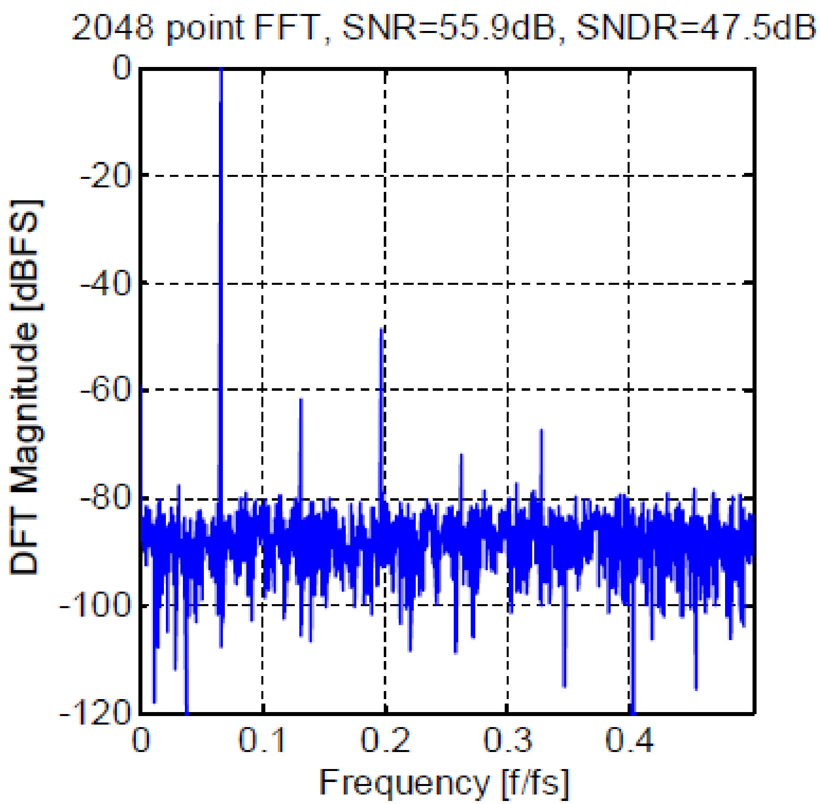
- Definition

$$SNDR = \frac{\text{Signal Power}}{\text{Noise and Distortion Power}}$$

- Noise and distortion power includes all bins except DC and signal

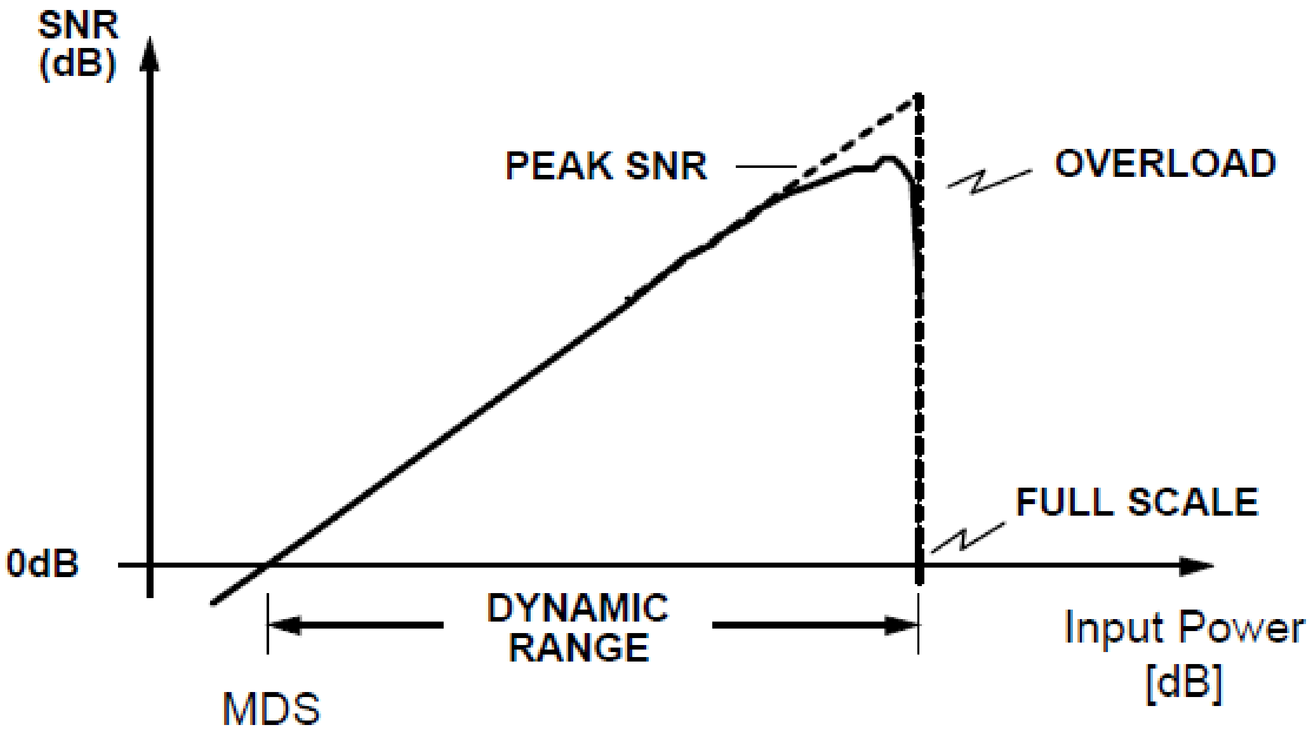
- Effective number of bits

$$ENOB = \frac{\text{SNDR(dB)-1.76dB}}{\text{6.02dB}}$$



Dynamic Range

$$DR = \frac{\text{Maximum Signal Power}}{\text{Minimum Detectable Signal}} \geq SNR_{peak}$$



SDR and THD

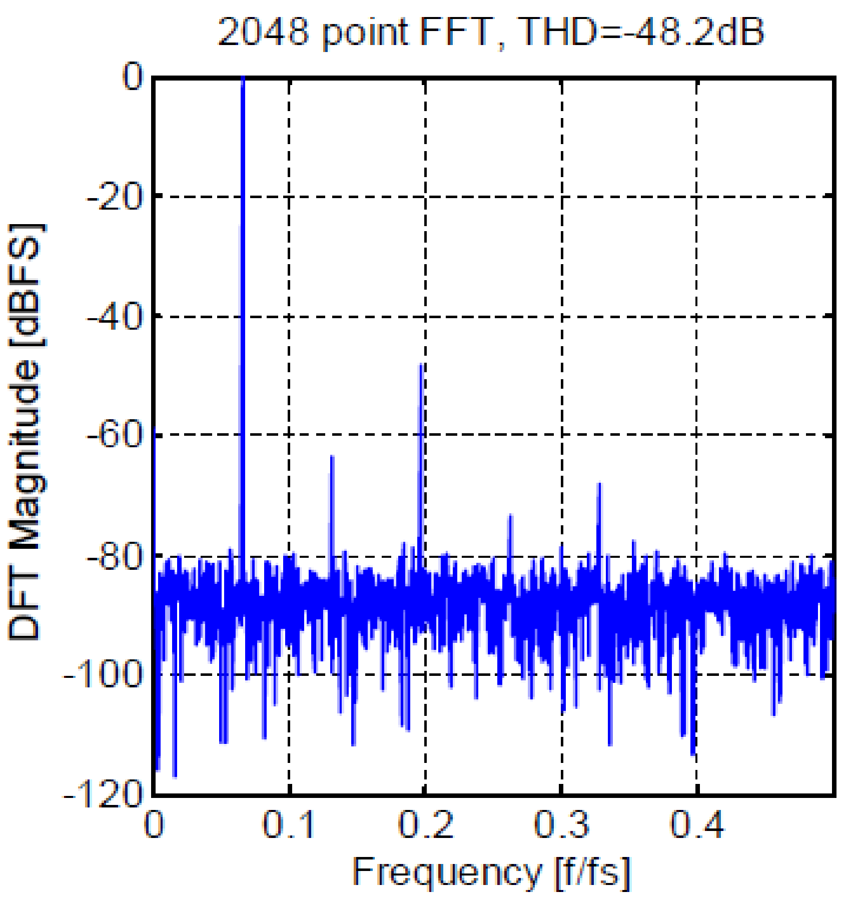
- Signal-to-distortion ratio

$$SDR = \frac{\text{Signal Power}}{\text{Total Distortion Power}}$$

- Total harmonic distortion

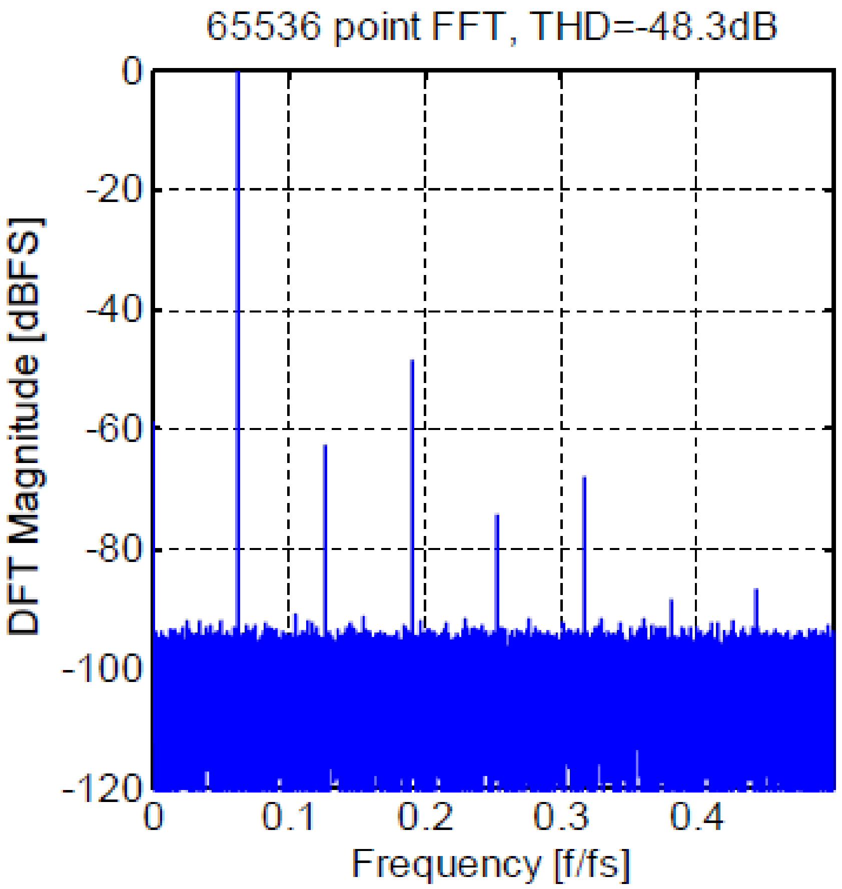
$$THD = \frac{\text{Total Distortion Power}}{\text{Signal Power}} = \frac{1}{SDR}$$

- By convention, total distortion power consists of 2nd through 7th harmonic



Lowering the Noise Floor

- Increasing the FFT size let's us lower the noise floor and reveal low level harmonics



Aliasing

- Harmonics can appear at "arbitrary" frequencies due to aliasing

$f_1 = f_x = 0.3125\ f_s$

$f_2 = 2\ f_1 = 0.6250\ f_s \rightarrow 0.3750\ f_s$

$f_3 = 3\ f_1 = 0.9375\ f_s \rightarrow 0.0625\ f_s$

$f_4 = 4\ f_1 = 1.2500\ f_s \rightarrow 0.2500\ f_s$

$f_5 = 5\ f_1 = 1.5625\ f_s \rightarrow 0.4375\ f_s$