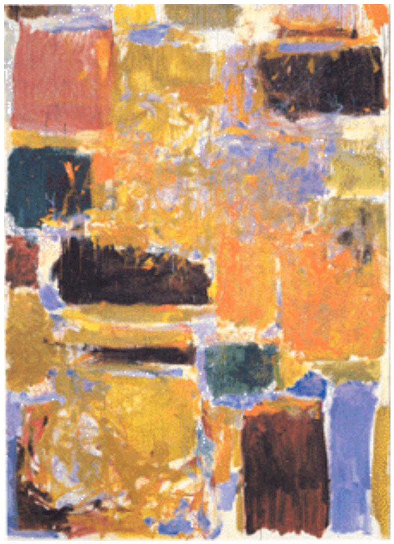


EE141-Spring 2010 Digital Integrated Circuits

Lecture 8
Wires
Transistors

Administrativia

- Hw 3 due today – HW 4 to be posted
- No Lab next week
- Extra review session Th at 6:30pm

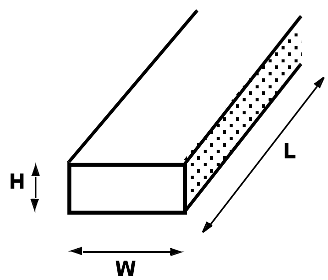
Class Material

- Last lecture
  - Logical Effort + Wires
- Today's lecture
  - Wiring (cntd) – Transistor models
- Reading (Ch 3, 4)

INTERCONNECT

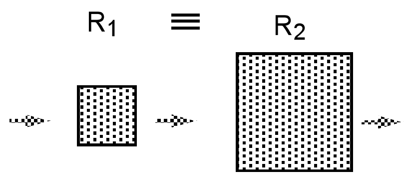
Resistance

Wire Resistance



$$R = \frac{\rho}{H}\frac{L}{W}$$

Sheet Resistance
R_o



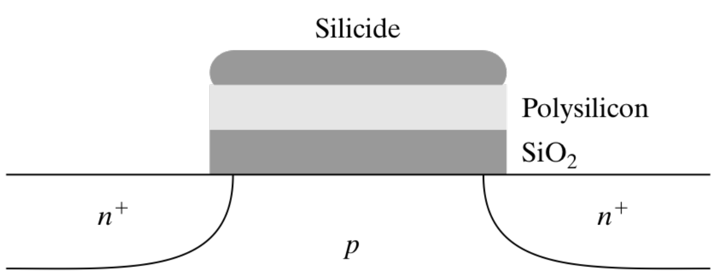
Interconnect Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Dealing with Resistance

- **Use Better Interconnect Materials**
  - e.g. copper, silicides
- **More Interconnect Layers**
  - reduce average wire-length
- **Selective Technology Scaling**
  - (More later)

Polycide Gate MOSFET



Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

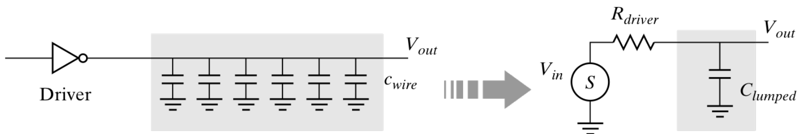
Conductivity: 8-10 times better than Poly

Sheet Resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

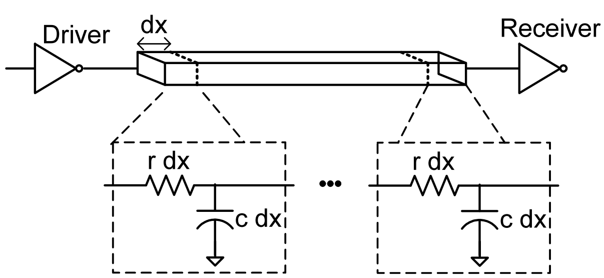
Interconnect Modeling

The Lumped Model



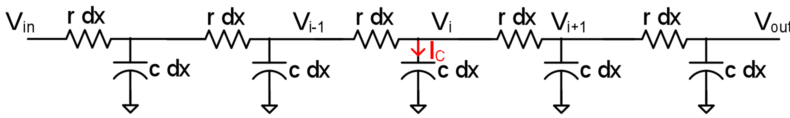
What to do with the resistance?

The Distributed RC-line



- Analysis method:
  - Break the wire up into segments of length dx
  - Each segment has resistance (r dx) and capacitance (c dx)

The Distributed RC-line



$$I_C = c\Delta L \frac{\partial V}{\partial t} = \frac{(V_{i-1} - V_i) - (V_i - V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

The diffusion equation

$$\boxed{\tau = \frac{L^2}{2} rc}$$

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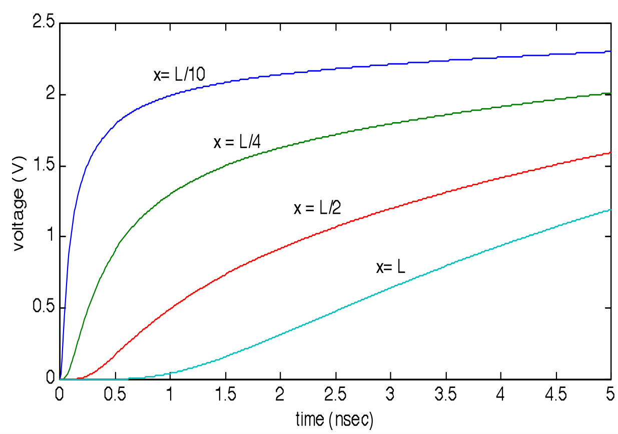
Step-response of RC wire as a function of time and space



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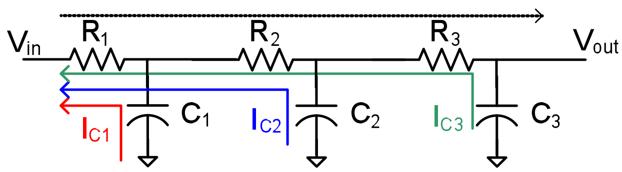
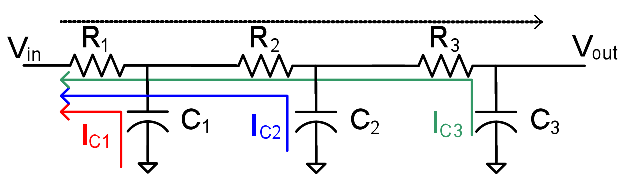
Simplified Model: Elmore Delay



- "Elmore delay": approximation for delay of arbitrary (complex) RC circuits
- To find "Elmore time constant":
  - For each capacitor, draw path of current from cap to input
  - Multiply C by sum of R's on current path that are common with path from V_{in} to V_{out}
  - Add up RC products from all capacitors

Simplified Model: Elmore Delay



$$\boxed{\tau_{Elmore} = R_1C_1 + \left(R_1 + R_2\right)C_2 + \left(R_1 + R_2 + R_3\right)C_3}$$

Wire Model

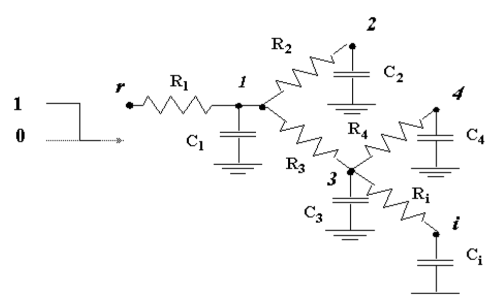
Model the wire with N equal-length segments:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

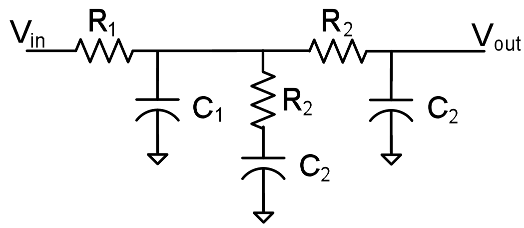
Elmore Delay - Extended



$$R_{ik} = \sum R_j \Rightarrow (R_j \in [path(s \to i) \cap path(s \to k)])$$

$$\tau_{Di} = \sum_{k=1}^{N} C_k R_{ik}$$

Another Elmore Delay Example



$$\tau_{Elmore} =$$

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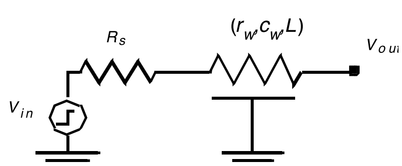
Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$

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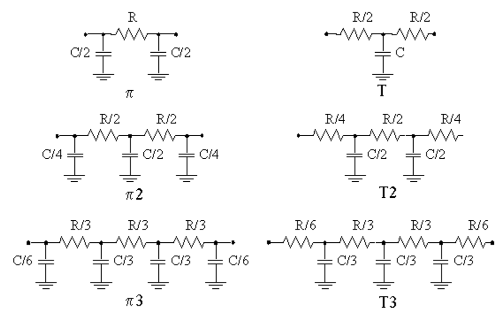
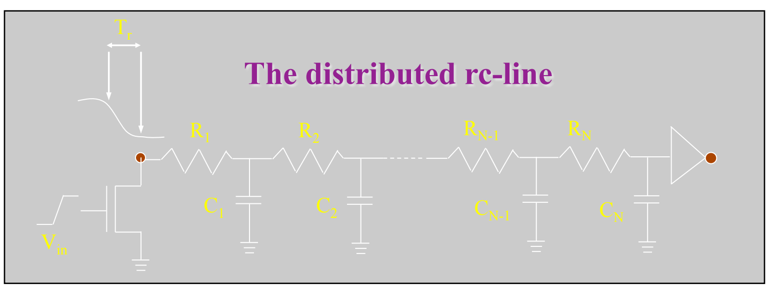
RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
$0 \rightarrow 50\%$ (t_p)	0.69 RC	0.38 RC
$0 \rightarrow 63\%$ (τ)	RC	0.5 RC
$10\% \rightarrow 90\%$ (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.

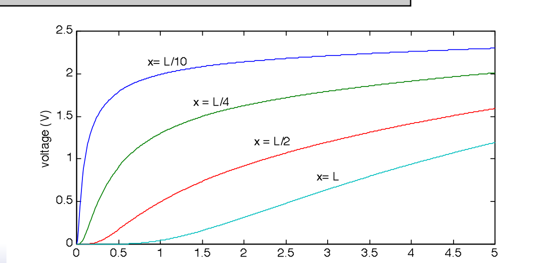


Resistivity and Performance



Diffused signal propagation

Delay ~ L^2



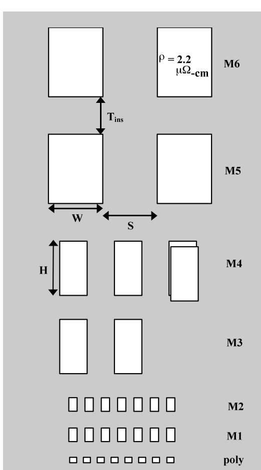
The Global Wire Problem

$$T_d = 0.377 R_w C_w + 0.693\left(R_d C_{out} + R_d C_w + R_w C_{out}\right)$$

Challenges

- No further improvements to be expected after the introduction of Copper (superconducting, optical?)
- Design solutions
  - Use of fat wires
  - Efficient chip floorplanning
  - Insert repeaters

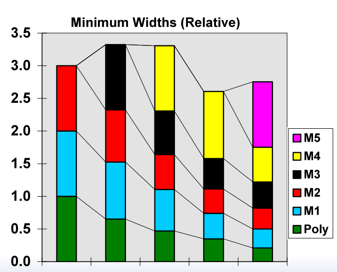
Interconnect: # of Wiring Layers

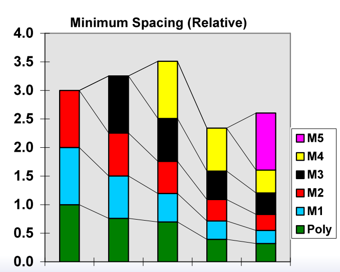


0.25 μm wiring stack

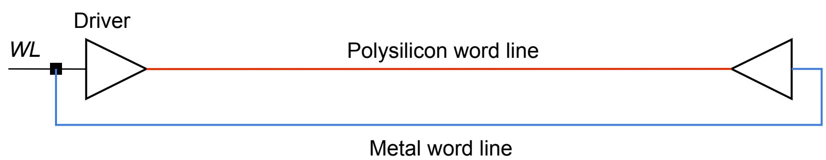
# of metal layers is steadily increasing due to:

- Increasing die size and device count: we need more wires and longer wires to connect everything
- Rising need for a hierarchical wiring network; local wires with high density and global wires with low RC

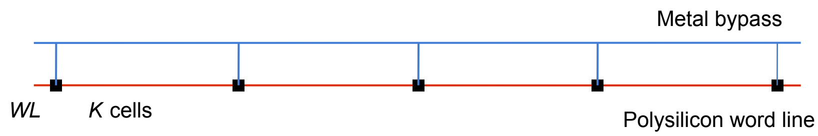




Using Bypasses

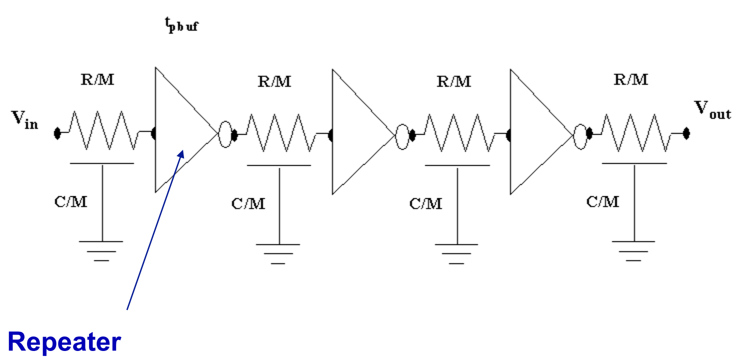


Driving a word line from both sides

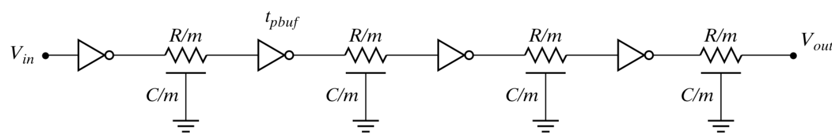


Using a metal bypass

Reducing RC-delay Using Repeaters



Repeaters



$$t_p = m\left(0.69\frac{R_d}{s}\left(s\gamma C_d + \frac{cL}{m} + sC_d\right) + 0.69\left(\frac{rL}{m}\right)(sC_d) + 0.38rc\left(\frac{L}{m}\right)^2\right)$$

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

Repeater Insertion (Revisited)

Taking the repeater loading into account

$$m_{opt} = L\sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma+1)}} = \sqrt{\frac{t_{pwire(unbuffered)}}{t_{p1}}}$$

$$s_{opt} = \sqrt{\frac{R_dc}{rC_d}}$$

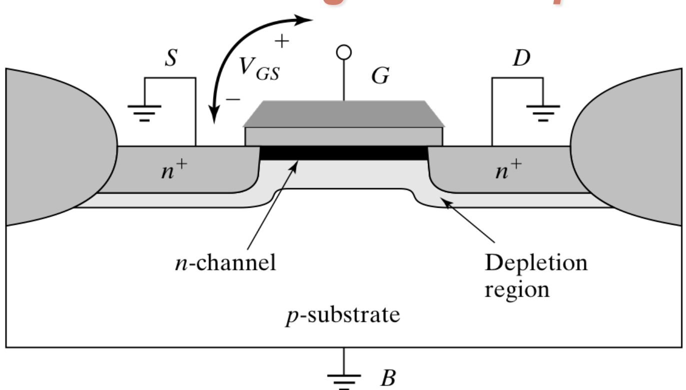
For a given technology and a given interconnect layer, there exists an optimal length of the wire segments between repeaters. The delay of these wire segments is independent of the routing layer!

$$L_{crit} = \frac{L}{m_{opt}} = \sqrt{\frac{t_{p1}}{0.38rc}} \qquad t_{p,crit} = \frac{t_{p,min}}{m_{opt}} = 2\left(1 + \sqrt{\frac{0.69}{0.38(1+\gamma)}}\right)t_{p1}$$

MOS Transistor

What do digital IC designers need to know?

Threshold Voltage: Concept



- With positive gate bias, electrons pulled toward the gate
- With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
- Voltage at which surface inverts: “magic” threshold voltage V_T

The Threshold Voltage

- Threshold

$$V_T = \varphi_{FB} + 2\varphi_F + \frac{Q_B}{C_{ox}}$$ Depletion charge

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{2\varphi_F}\right)$$

- Fermi potential

$$\phi_F = \phi_T \cdot \ln\frac{N_A}{n_i}$$

$2\Phi_F$ is approximately 0.6V for p-type substrates
γ is the body factor
V_{T0} is approximately 0.45V for our process

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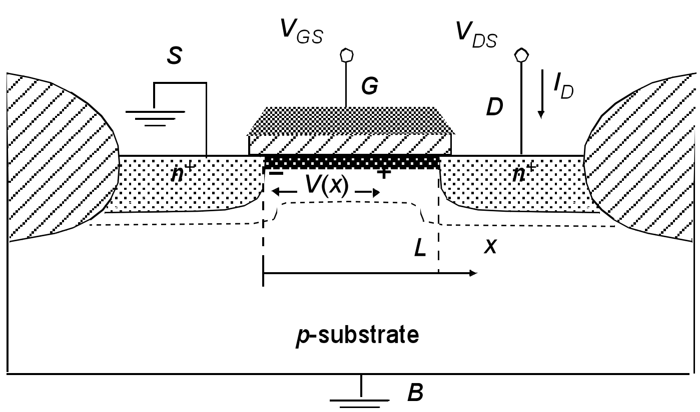
Transistor with Gate and Drain Bias



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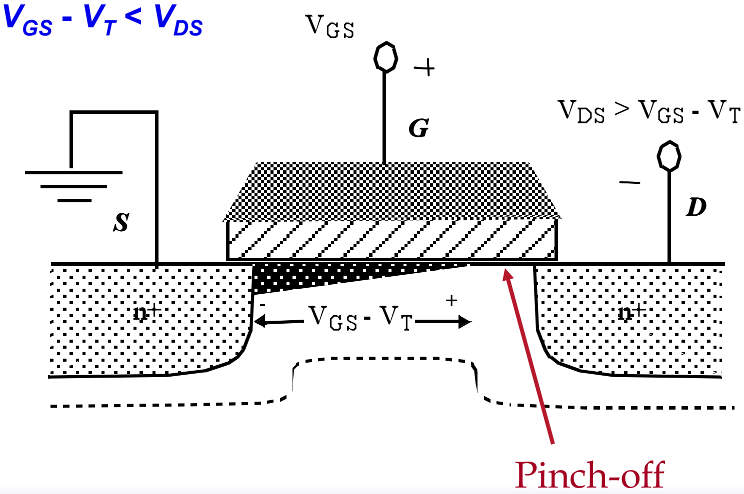
Transistor in Saturation

$0 < V_{GS} - V_T < V_{DS}$



Saturation

- For $(V_{GS} - V_T) < V_{DS}$, the effective drain voltage and current saturate:

$$V_{DS,eff} = (V_{GS} - V_T)$$

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

- Of course, real drain current isn't totally independent of V_{DS}
  - For example, approx. for channel-length modulation:

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

Modes of Operation

Cutoff:

$V_{GS} - V_T < 0$ $\qquad I_D = 0$

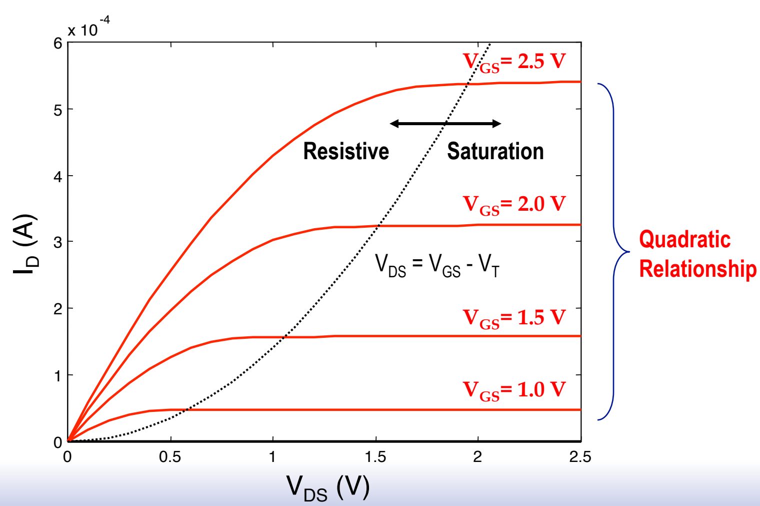
Linear (Resistive):

$V_{GS} - V_T > V_{DS}$ $\qquad I_D = k_n' \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$

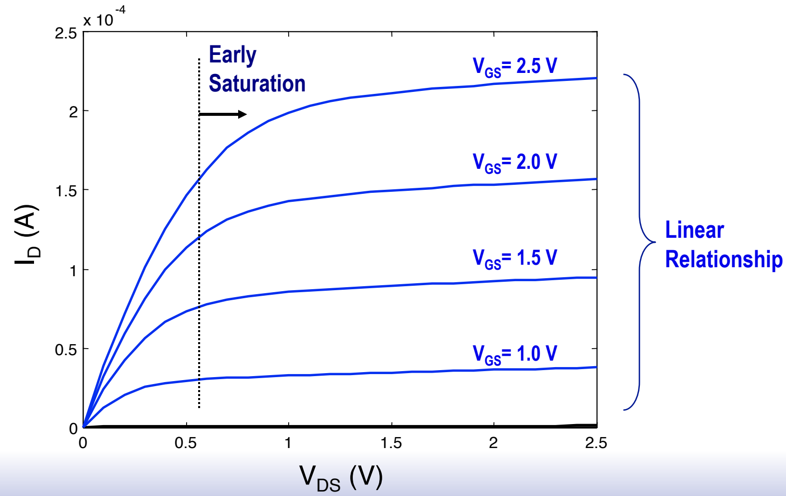
Saturation:

$0 < V_{GS} - V_T < V_{DS}$ $\qquad I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$

Current-Voltage Relations: A Good Ol' Transistor

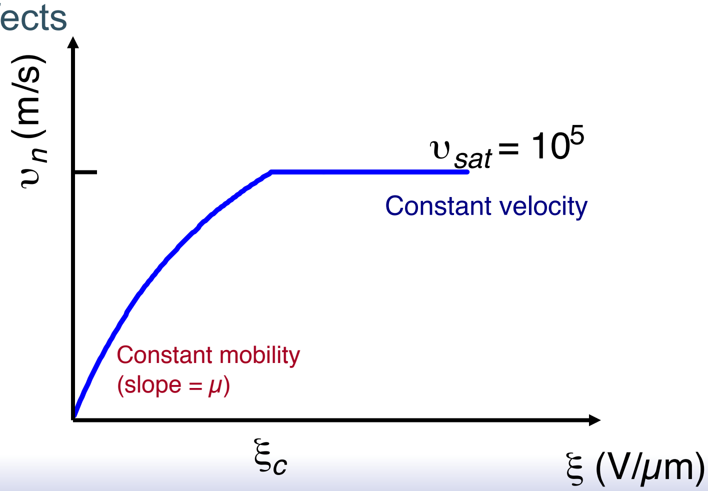


Current-Voltage Relations: The Deep Sub-Micron Transistor

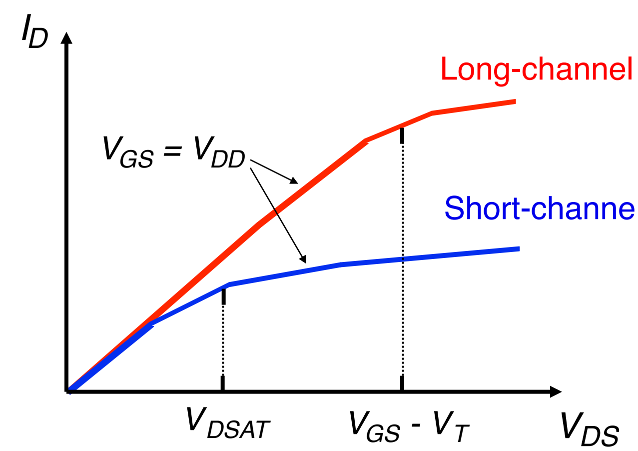


Velocity Saturation

- Velocity saturates due to carrier scattering effects



Velocity Saturation



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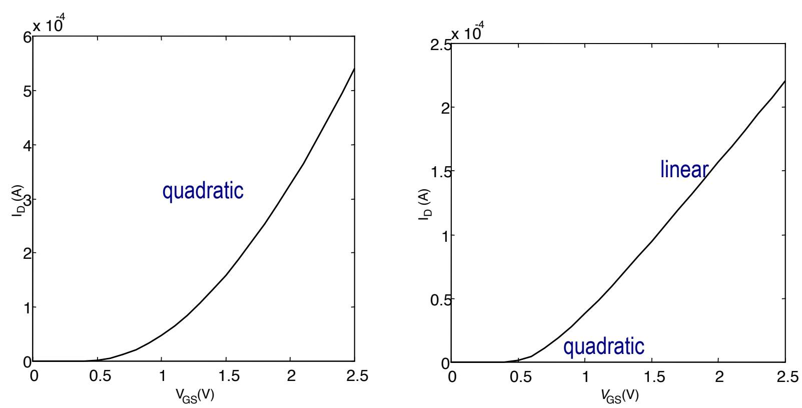
I_D versus V_{GS}



Long Channel (L=2.5μm)

Short Channel (L=0.25μm)

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