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SRAM Column Decoder and Sense Amplifier – Term Project Phase 3

Due Noon, Wednesday, May 6, 2009

Introduction

In Phase 3 of the project, we will design the read-out path of the 4Mb SRAM array, which consists of the column decoder and sense amplifier (Fig. 1). The column decoder decodes the 6-bit address input and enables access to one of the 64 words at a time. The sense amplifier detects small difference between the differential bit lines (BL and $\overline{BL}$) and reports a full-swing output for each bit of the 71-bit word.

Objective of Phase 3 is to minimize the delay time of the read-out path in the face of process variations.

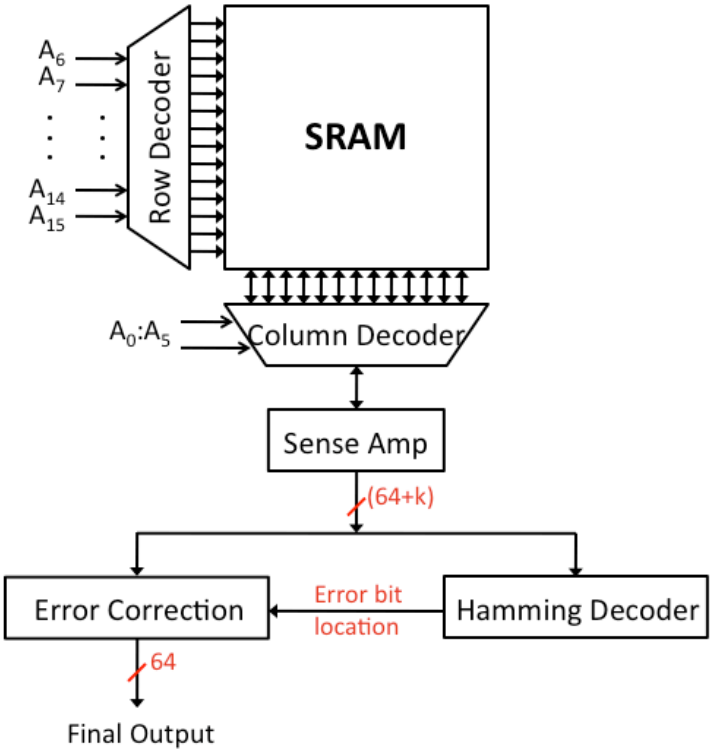

Fig. 1 A 4Mb SRAM Array with Error Correction.

Process Variations

As CMOS marches down the path of scaling, process variations have become increasingly challenging to a circuit designer. Global variations (those that affect all devices on the same wafer, or more precisely on the same fabrication run) are typically modeled as "corner conditions" in the technology library. In the EE141 90nm CMOS technology, there exist five process corners:

- NN: normal NMOS, normal PMOS
- SS: slow NMOS, slow PMOS
- FF: fast NMOS, fast PMOS
- FS: fast NMOS, slow PMOS
- SF: slow NMOS, fast PMOS

Process corners can be specified in the Cadence Analog Design Environment (under "Setup" → "Model Libraries"). After changing the "Section", remember to click "OK" to make the change effective (Fig. 2).

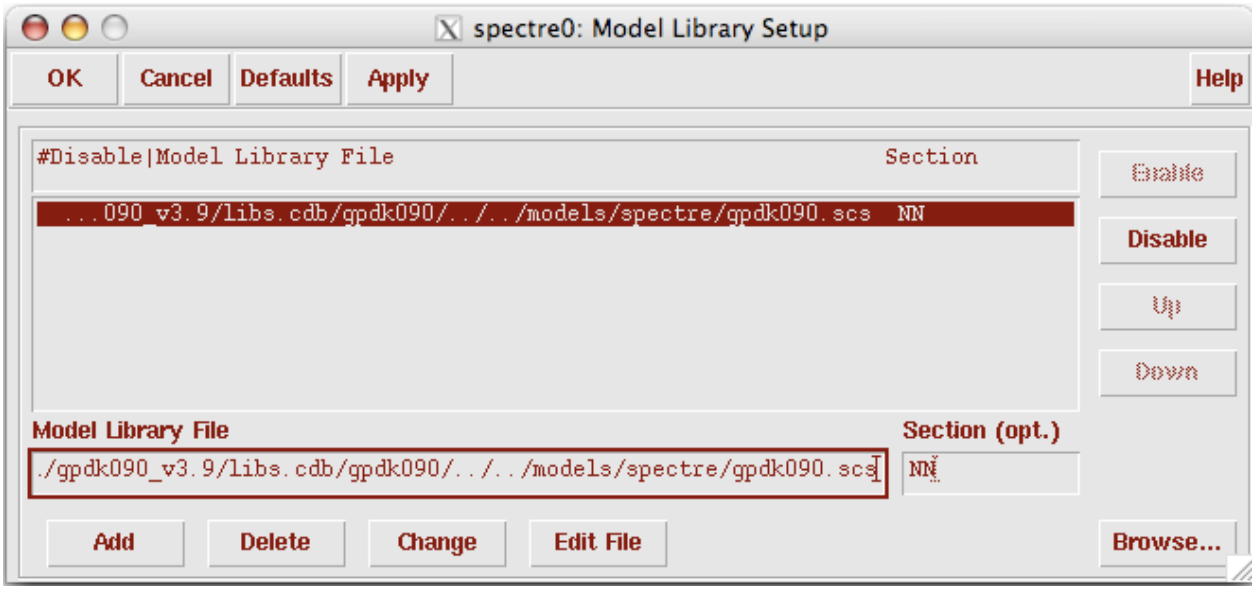

Fig. 2 Specifying Process Corner in Model Library Setup.

Device Mismatch and Sense Amp Offset

While process corners specify global variations affecting all transistors on a circuit, there exists another source of variability: local variation. In this project we will only consider threshold mismatch (ΔV_T) between a pair of identical devices laid out next to each other. Observed widely (reference [1]), device mismatch is inversely proportional to device area:

$$\Delta V_T = \frac{\sigma}{\sqrt{W \times L}} \quad \text{.....(1)}$$

where W and L are the width and length of each transistor, and σ is the process parameter, which is assumed to be 10mV×μm in our technology. (Please note that Eq. (1) above is significantly

simplified from the statistical nature of device matching. It nevertheless captures the "worst-case" mismatch and its dependence on device sizing.)

The circuit to which device mismatch makes significant impact is the sense amplifier in Fig. 1. Input devices of a sense amplifier are typically a differential pair laid out in a common-centroid fashion. **Threshold mismatch manifests as offset voltage at the sense amplifier's input.** A properly designed sense amplifier should be held from reporting an output until its input signal is larger than the offset voltage; otherwise the output will be erroneous. In this project, a design tradeoff needs to be made between device sizing (W and L) and the hold-time of the sense amplifier, both affecting the delay of the read-out path.

While global variation can be simulated through process corners, the worst-case offset needs to be computed from Eq. (1) above. A DC voltage source, representing this offset, can then be added in series with the sense amplifier's input (either single-ended or differential, Fig. 3). Make sure that the polarity of the offset voltage is set in conjunction with the expected values on BL and $\overline{BL}$ so that it represents the worst-case propagation delay. (In practice, noise is another factor that impacts the sense amplifier hold time. In this project however, no consideration for noise is needed.)

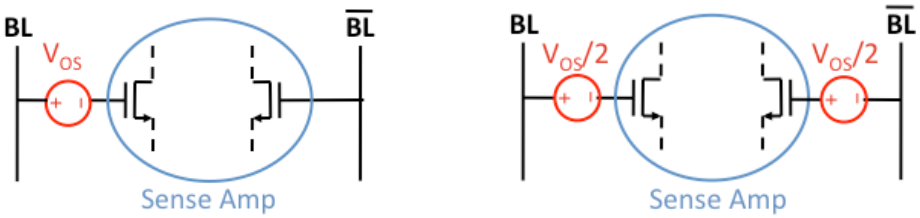

Fig. 3 Modeling of Sense Amplifier Offset: Single-ended and Differential.

Constraints

Supply Voltage: Up to 1V.

Clock: Clock frequency is 100MHz, with 50ps rise and fall time and 50% duty cycle. Clocks exist only in two phases: 0° and 180°. 0° means that the clock's rising edge is synchronized with the rising edge of the word line (WL). Similarly 180° means clock's falling edge synchronized to the WL rising edge. If you need additional phase delays, they need to be generated with your own circuits.

Column Address: Changes on column address A<5:0> are synchronized with the rising edge of word line. Only the true, not the complementary, form of the inputs is available.

Loading: Loading on each sense amplifier's output is 4C, where C is the gate capacitance of a unit-size inverter (NMOS: 120n/100n, PMOS: 240n/100n). Loading on each column address bit cannot exceed 4C either.

Critical Path: Like in previous two phases, you only need to perform analysis and simulation on the critical path. When there are multiple fan-in and fan-out gates however, you need to include 2 stages of off-path in the simulation schematic to characterize propagation delay more accurately. Propagation delay is measured from the rising edge of the word line to the time when sense amplifier produces a valid output. Output of the sense amplifier can change **at most once** after the word line is asserted.

SRAM Model

To simplify simulation, the SRAM column will be modeled as follows. The SRAM cell from which data will be read out is identical to the cell used in Phase 1 and Phase 2 (Fig. 4). No layout extraction is needed for Phase 3. **Remember to set initial conditions on nodes "Q" and "QB" before executing transient simulation.** For the rest of 1,023 cells in the column, represent them with two large access transistors (N1 and N2 in Fig. 5). To model the effect of leakage current however, one of the access transistors needs to be connected to V_{DD} while the other connected to V_{SS}. Again make sure that the initial conditions on Q and QB are set properly with regard to bias levels of the large transistors so that it models the worst-case propagation delay. Finally two lumped capacitors (C1 and C2, of equal value 300fF) are added to the bit lines, representing wiring capacitances. Prior to the read operations, both bit lines are pre-charged to V_{DD}. This is equivalent to setting initial conditions on "BL" and "BLB" to V_{DD}.

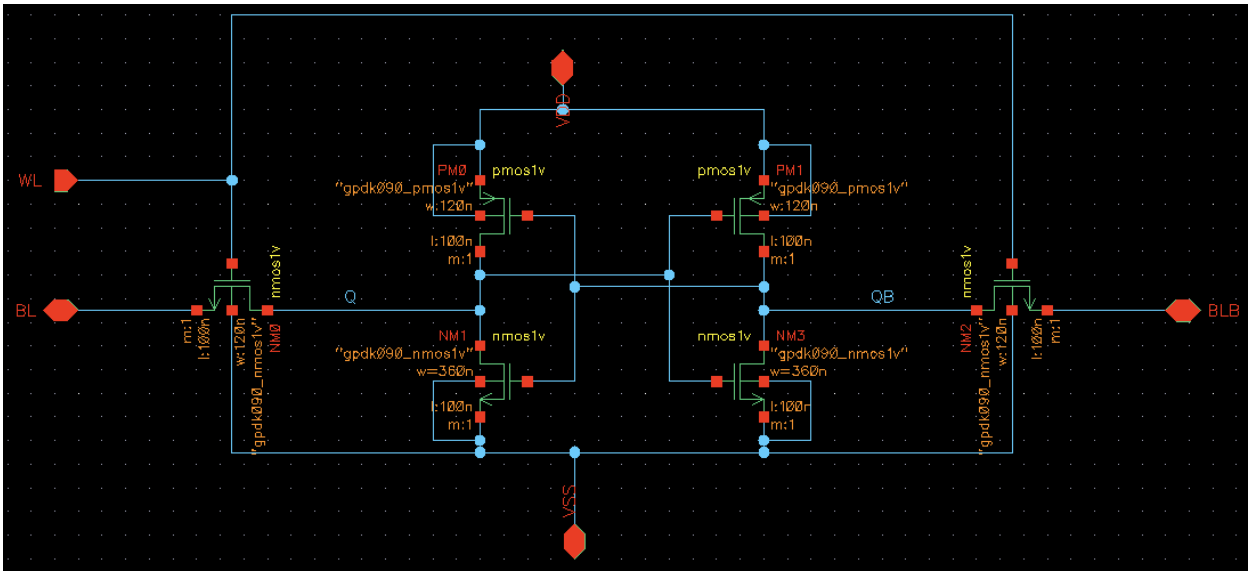

Fig. 4 SRAM Cell Model for Phase 3 Simulation.

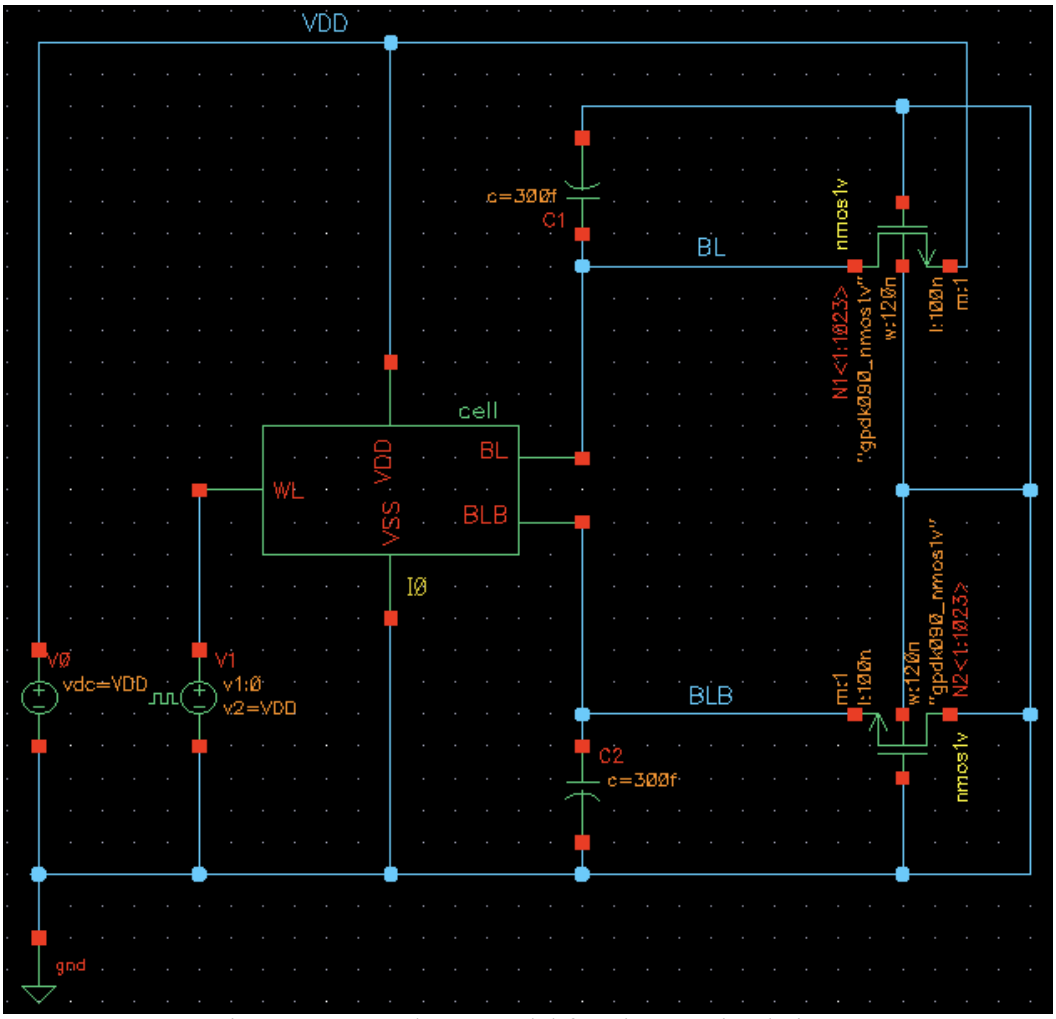

Fig. 5 SRAM Column Model for Phase 3 Simulation.

Objective

Objective of Phase 3 of the project is to **minimize the propagation delay**, under the **worse** global and local variation conditions. Propagation delay is defined as the time from the word line rises to 50% of V_{DD} to sense amplifier's output reaches 50% of V_{DD}. Again no glitches are allowed at the output.

Once the design is optimized for the worse case, you are also asked to set the process corners to "NN", reduce the offset voltage to 0 and simulate the "nominal case" propagation delay. This extra step is only for comparison purposes − don't spend extra time to change anything on your design!

No layout work is required in Phase 3.

Poster

Instead of text report, results of this phase of the project will be presented in a poster session at 2:00~5:00 pm on Wednesday May 6th, 2009. Each team will be given 12 minutes to present the design of the column decoder and sense amplifier, followed by 3 minutes Q&A. Time slot sign-up sheet will be passed around during the lecture on **April 29**. Make sure at least one of the team members will be present.

The poster session will be held at BWRC (Berkeley Wireless Research Center, directions: http://bwrc.eecs.berkeley.edu/Background/directions.htm). Poster template as well as mounting instructions can be found on the course website. Remember to also **email your poster** to ee141@cory.eecs.berkeley.edu by noon, Wednesday, May 6, 2009.

Reference:

[1] M. Pelgrom, A. Duinmaijer and A. Welbers, "Matching Properties of MOS Transistors," *IEEE Journal of Solid-State Circuits,* October 1989