EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 13: Comparator Offset Cancellation
Differential Preamplifier

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Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	~~Finish Flash ADC~~
28-Feb	~~DAC Architectures - Resistor, R-2R~~
5-Mar	~~DAC Architectures - Current steering, Segmented~~
7-Mar	~~DAC Architectures - Capacitor-based~~
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

Latched Comparator

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

Latched Comparator Example 1

Key Point: *Latched comparators typically employ a simple preamplifier to mitigate kickback and reduce the requirements placed upon the latch stage, followed by a latch which alternates between a reset phase and a positive feedback phase that quickly generates full-swing digital signals from the preamplifier output.*

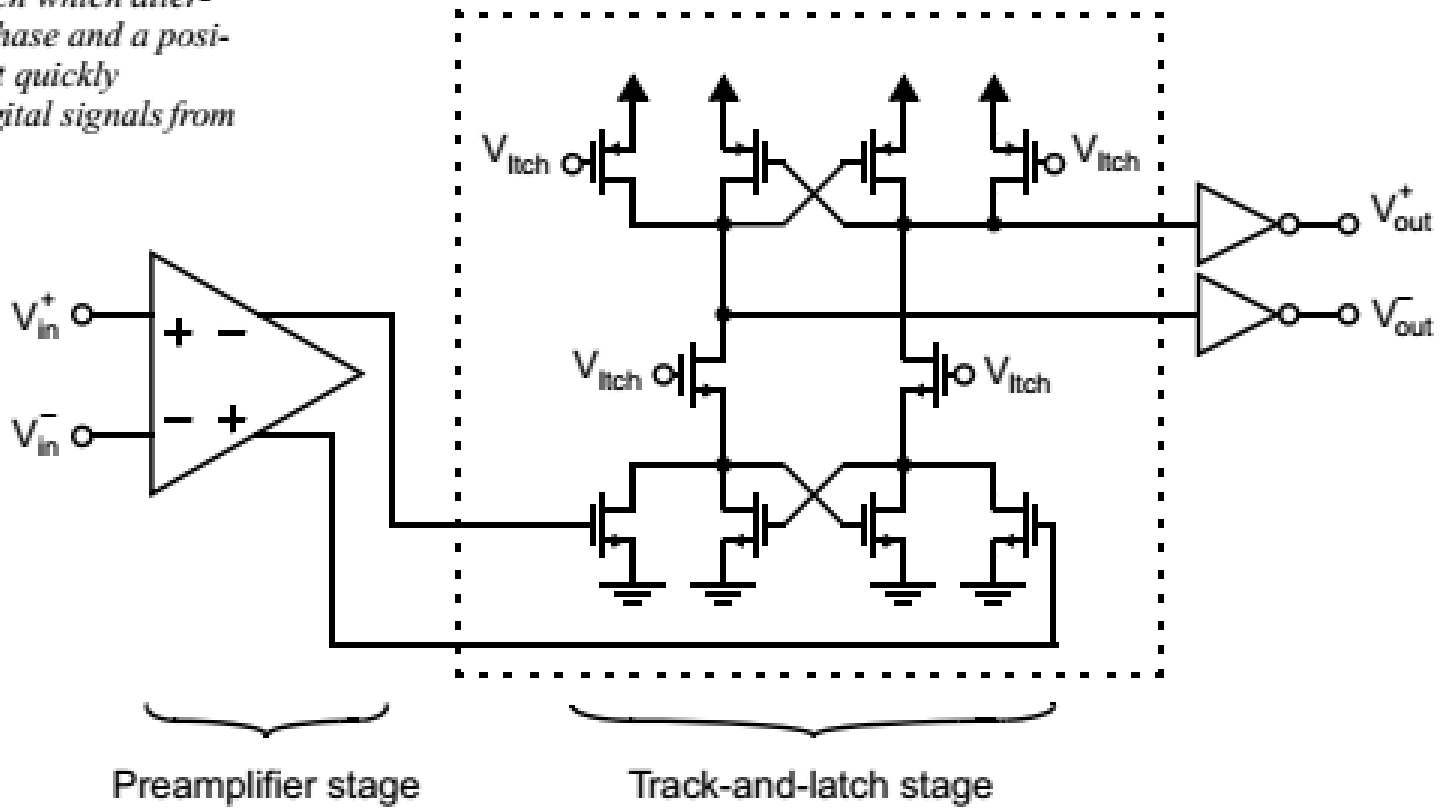
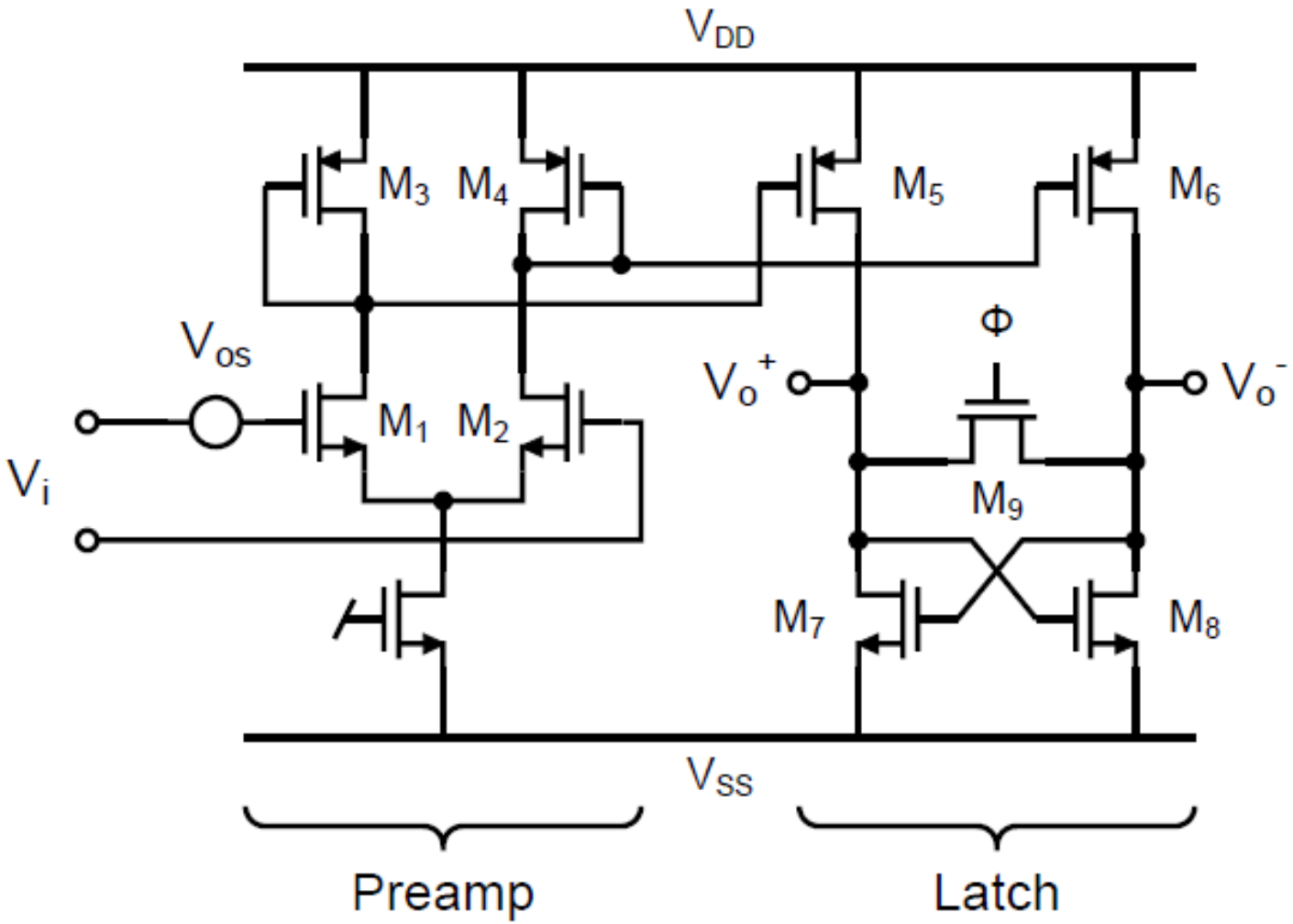
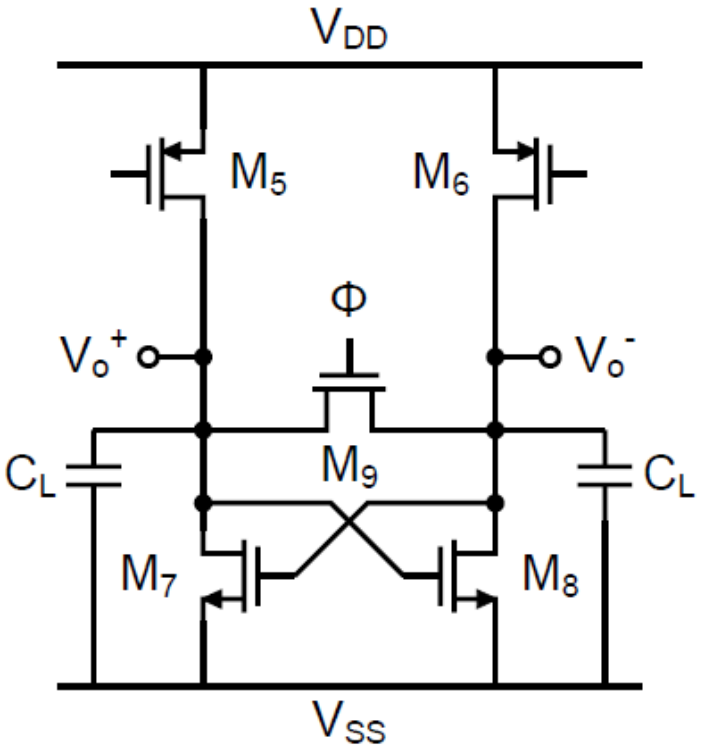


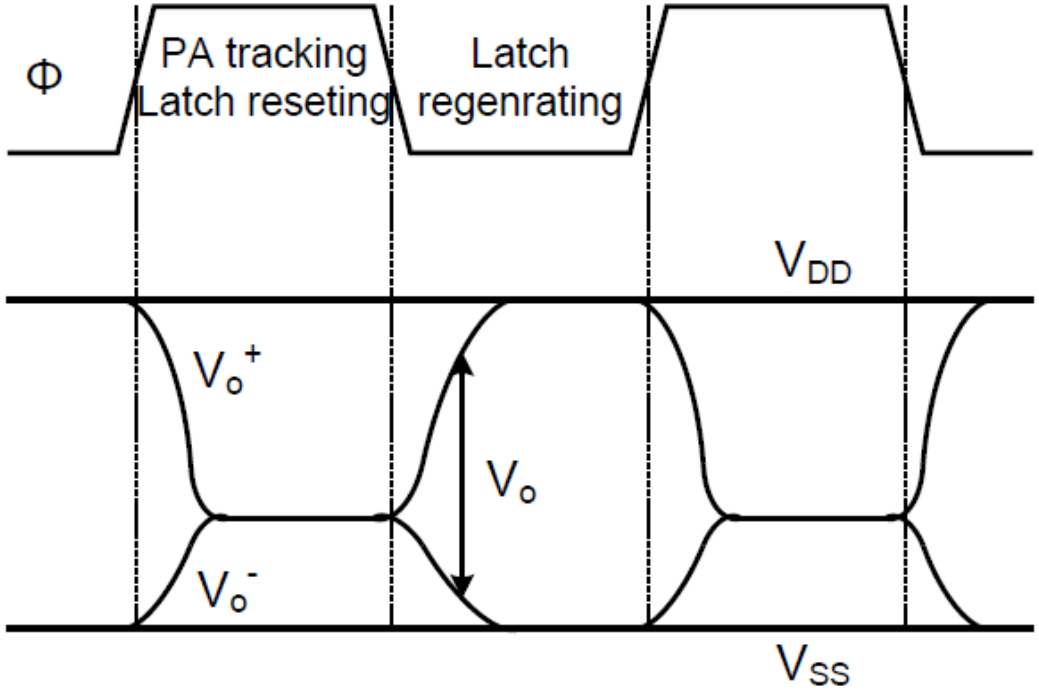
Fig. 10.14 A typical architecture for a high-speed comparator.

Latched Comparator Example 2

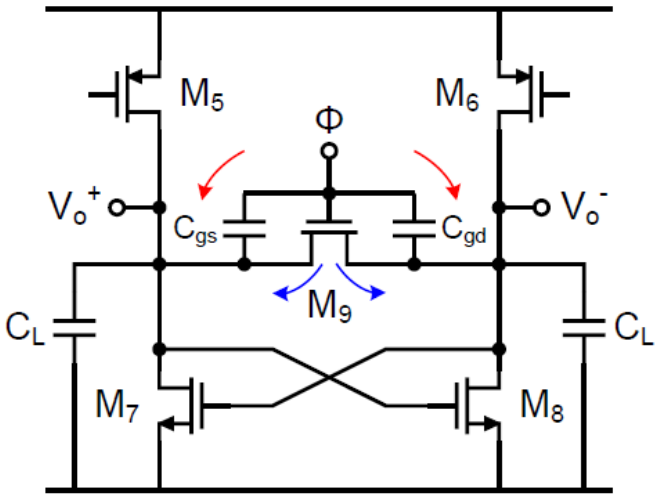


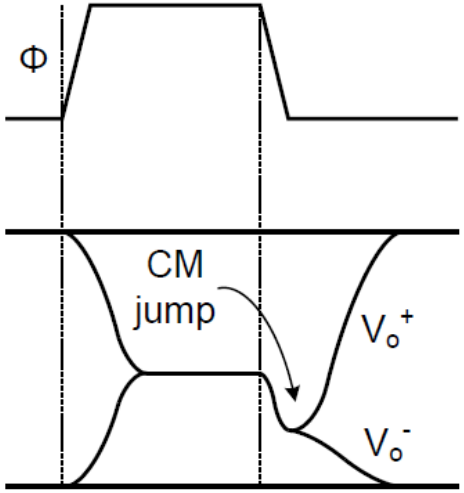
Regeneration in the Comparator





Dynamic Offset in the Comparator

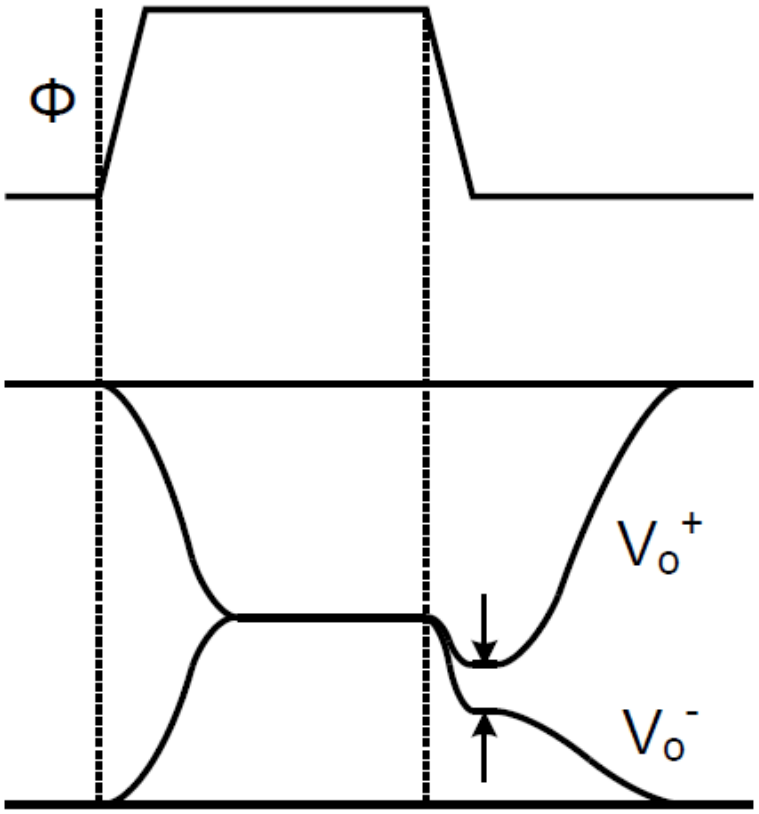




In the above latch, regeneration starts when Φ goes low

- Charge injection (CI) and clock-feedthrough (CF) introduce common-mode jump into V_o^+ and V_o^-
- Mismatch/imbalance in CI and/or CF induces dynamic offset in the latch

Dynamic and Static Offset in the Comparator



Dynamic offset induced due to:

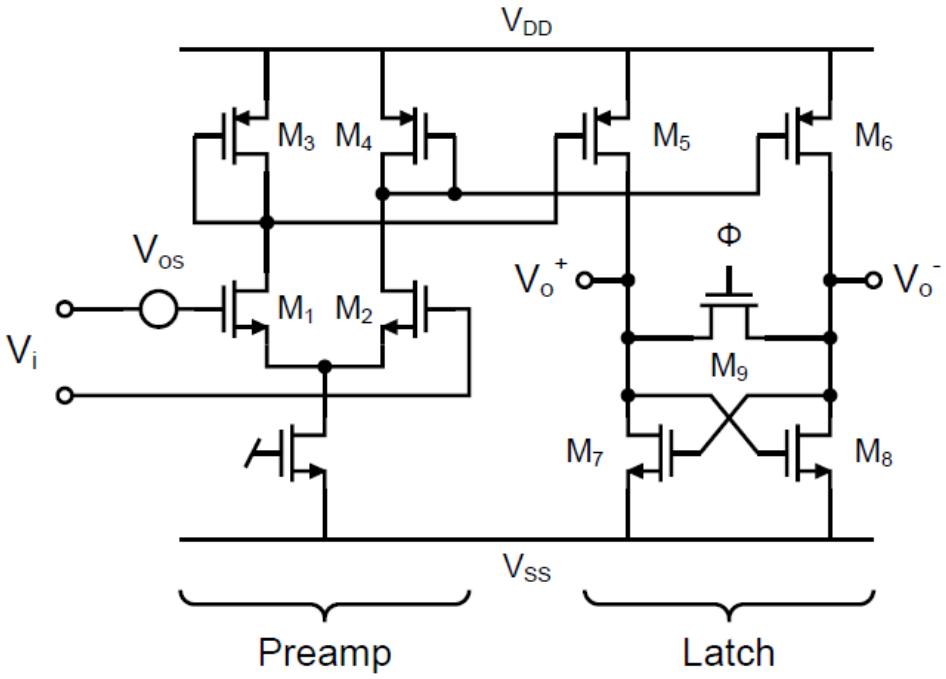
- Imbalanced CI and CF
- Imbalanced load capacitance

0.5V CM jump
10% imbalance
} ⇒ 50mV offset

Static offset induced due to:

- Mismatch in the cross-coupled pairs
- Mismatch in the signal input circuitry

Kickback Noise



- Input-referred latch offset gets divided by the gain of the preamp
- Preamp introduces its own offset (mostly static due to V_{th}, W, and L mismatches)
- Preamp also reduces kickback noise

Rapidly varying regeneration nodes couple kickback noise to the input

Kickback noise disturbs reference voltages, must settle before next sample

Offset of Differential Pair

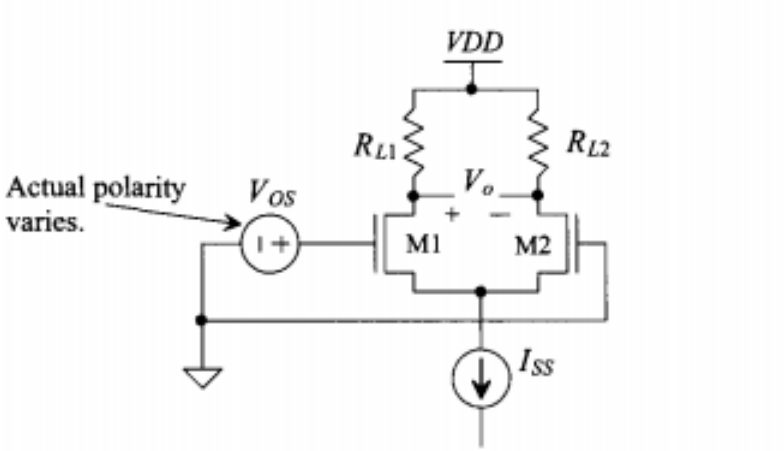


Figure 22.19 Determining diff-amp input offset voltage.

$$V_{OS} = V_{GS1} - V_{GS2} = V_{THN1} + \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{THN2} - \sqrt{\frac{2I_{D2}}{\beta_2}}$$

$$V_{OS} = \Delta V_{THN} + \frac{V_{GS} - V_{THN}}{2} \cdot \left[\frac{-\Delta R_L}{R_L} - \frac{\Delta(W/L)}{(W/L)} \right]$$

To reduce Offset of differential pair,

(1) Reduce ΔVth

(2) Increase gm ($g_m = \frac{2I}{Vgs-Vth}$) for a given bias current

Threshold Voltage Mismatch

$$\sigma_{VT,local} = \frac{\sqrt[4]{4q^3\varepsilon_{Si}\varphi_B}}{2} \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \frac{\sqrt[4]{N_{tot}}}{\sqrt{L_{eff} \cdot W_{eff}}}$$

$$\sigma_{VT,local} = \frac{A_{VT,local}}{\sqrt{L_{eff} \cdot W_{eff}}}$$

$$A_{VT,local} = \frac{\sqrt[4]{4q^3\varepsilon_{Si}\varphi_B}}{2} \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \sqrt[4]{N_{tot}}$$

Threshold Voltage Mismatch

$$\sigma^2_{deltaVT} = \sigma^2_{local,A} + \sigma^2_{local,B} = 2 \cdot \sigma^2_{local}$$

$$A_{VT} = \sqrt{2} \cdot A_{VT,local}$$

Pelgrom Plot

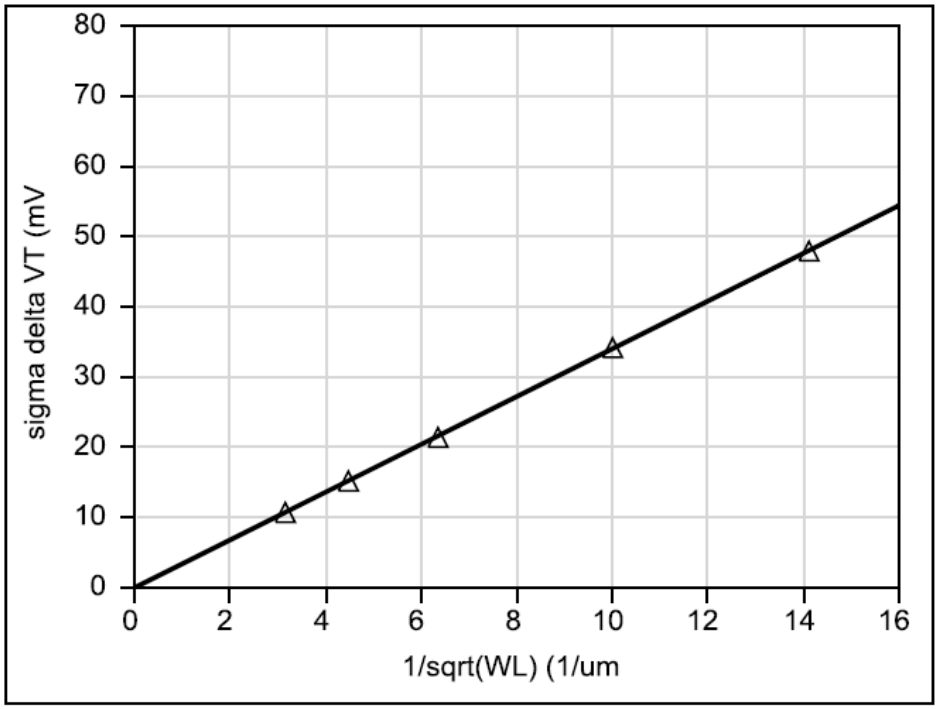
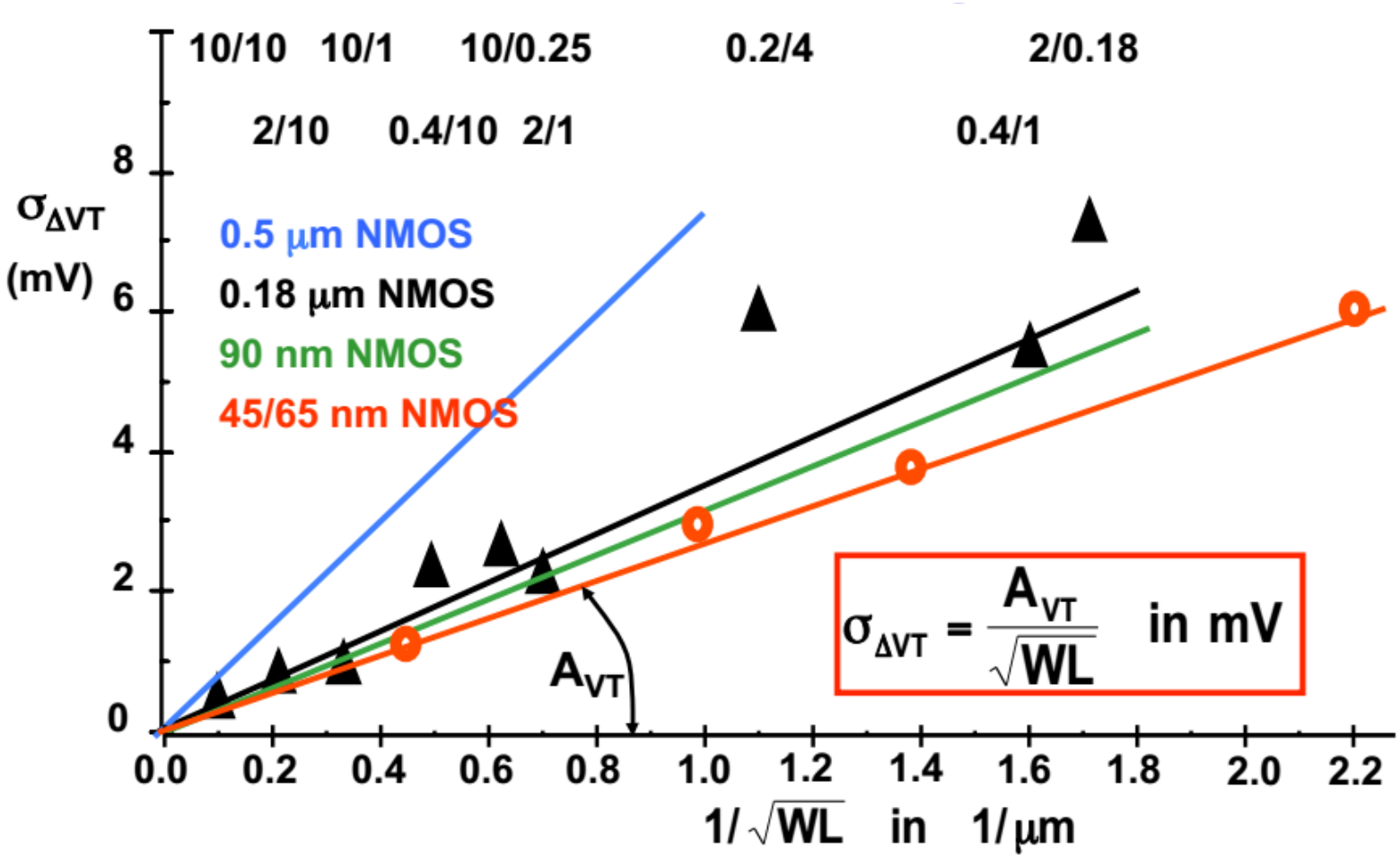


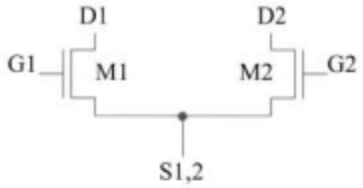
Figure 2. A sample Pelgrom plot showing sigma delta VT plotted against the inverse of the square root of the area for various device geometries with an A_{VT} of 3.4 mV-µm.

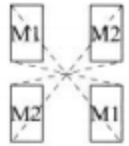
MOSFET Matching and Technology Scaling



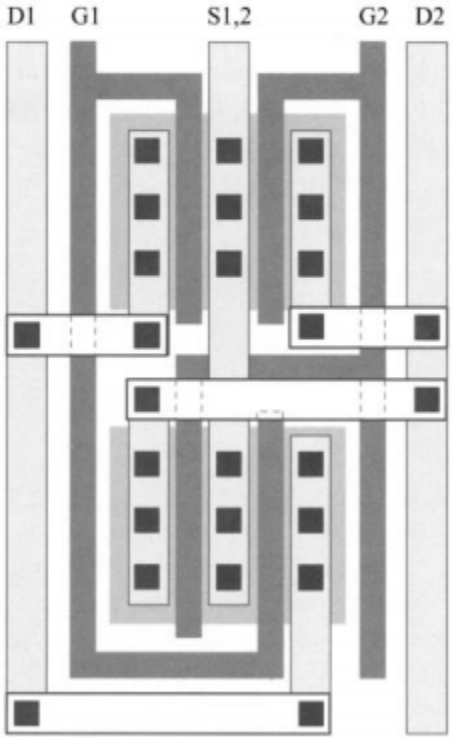
Ref: M. Pelgrom IEEE JSSC 1989 p. 1433, Tuinhout, Wils, and work by many others

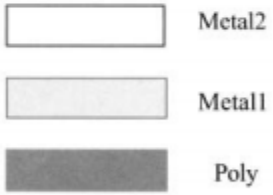
Layout to reduce Threshold Voltage Mismatch





Common-centroid layout





$$V_{os} = \Delta V_{th} + \frac{V_{GS}-V_{th}}{2}\left[\frac{\Delta R_L}{R_L} + \frac{\Delta\left(\frac{W}{L}\right)}{\left(\frac{W}{L}\right)}\right]$$

Input Offset Cancellation

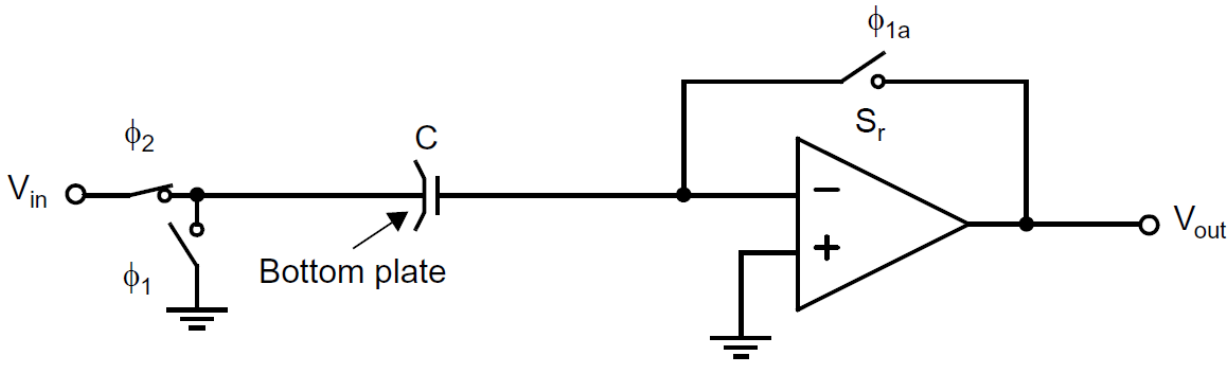
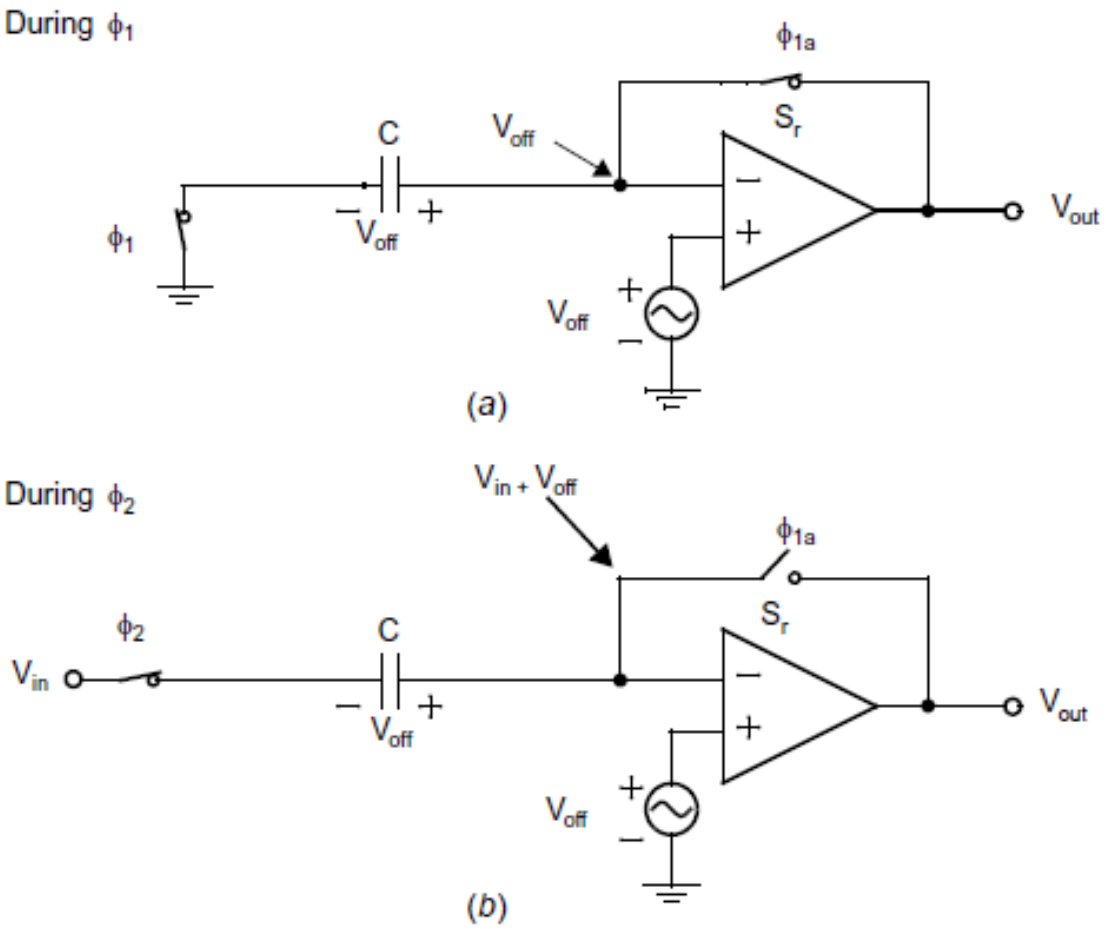
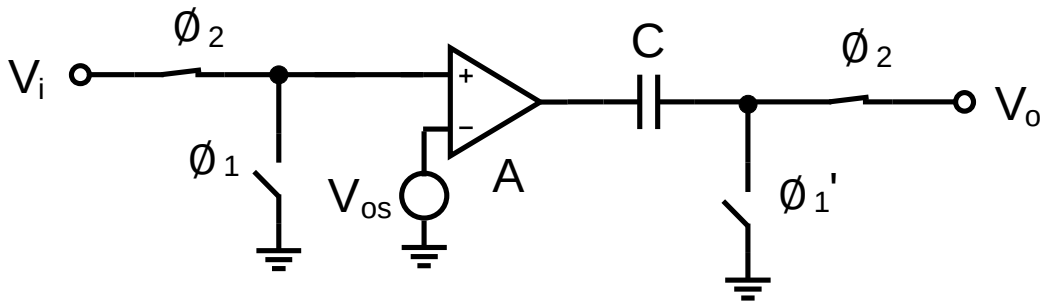


Fig. 10.3 Cancelling the offset voltage of a comparator—the comparator here must be stable, with unity-gain feedback during ϕ_{1a}. (ϕ_{1a} is a slightly advanced version of ϕ_1 so that charge-injection effects are reduced.)

Input Offset Cancellation

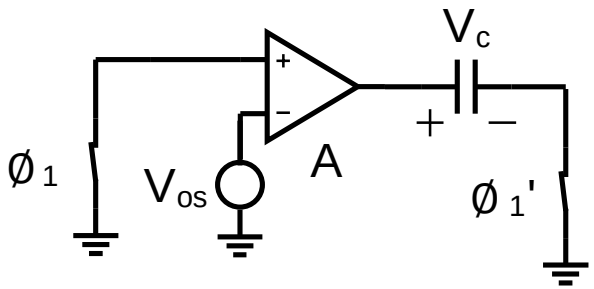


Output Offset Cancellation



- AC coupling at the output with offset stored in C during Φ_1
- A (Amp gain) must be small and well controlled (independent of V_o)
- Does not work for high-gain op-amps

Offset Storage During Φ_1

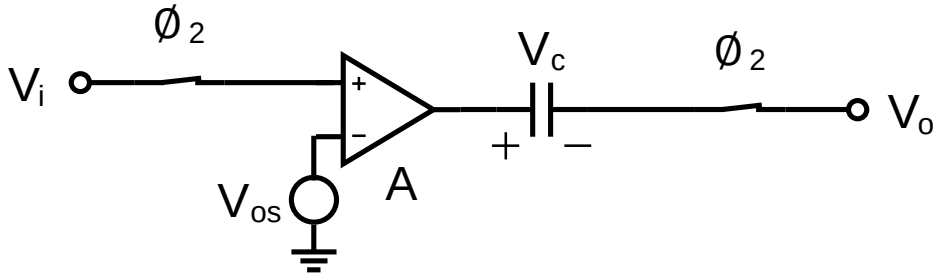


$$V_c = A(-V_{os}) = -AV_{os}$$

- Closed-loop stability is not required
- CF and CI of Φ_1' gets divided by A when referred to input

Ref: R. Poujois and J. Borel, “A low drift fully integrated MOSFET operational amplifier,” *JSSC*, vol. 13, pp. 499-503, issue 4, 1978.

Amplifying Phase During Φ_2



$$V_o = A(V_i - V_{os}) + AV_{os}$$
$$= AV_{in}$$

$\Rightarrow$

Input-referred offset :

$V_{os,in} = 0$

- Cancellation is complete if A is constant (independent of V_o)
- AC coupling at output attenuates signal gain

Multi-Stage Comparator

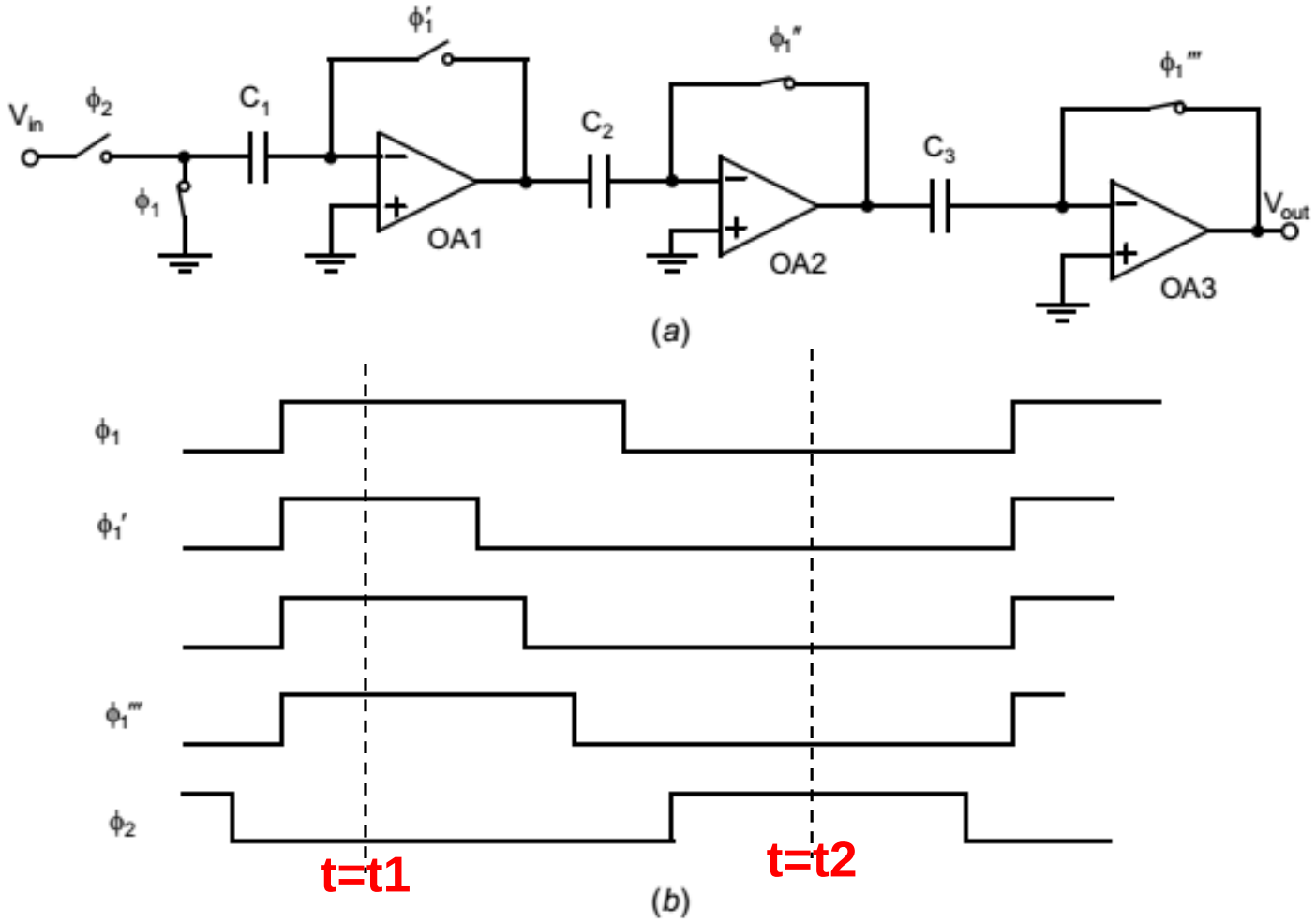


Fig. 10.11 (*a*) A multi-stage comparator used to eliminate clock feedthrough errors, with (*b*) the appropriate clock waveforms.

First-Stage of the Multi-Stage Comparator

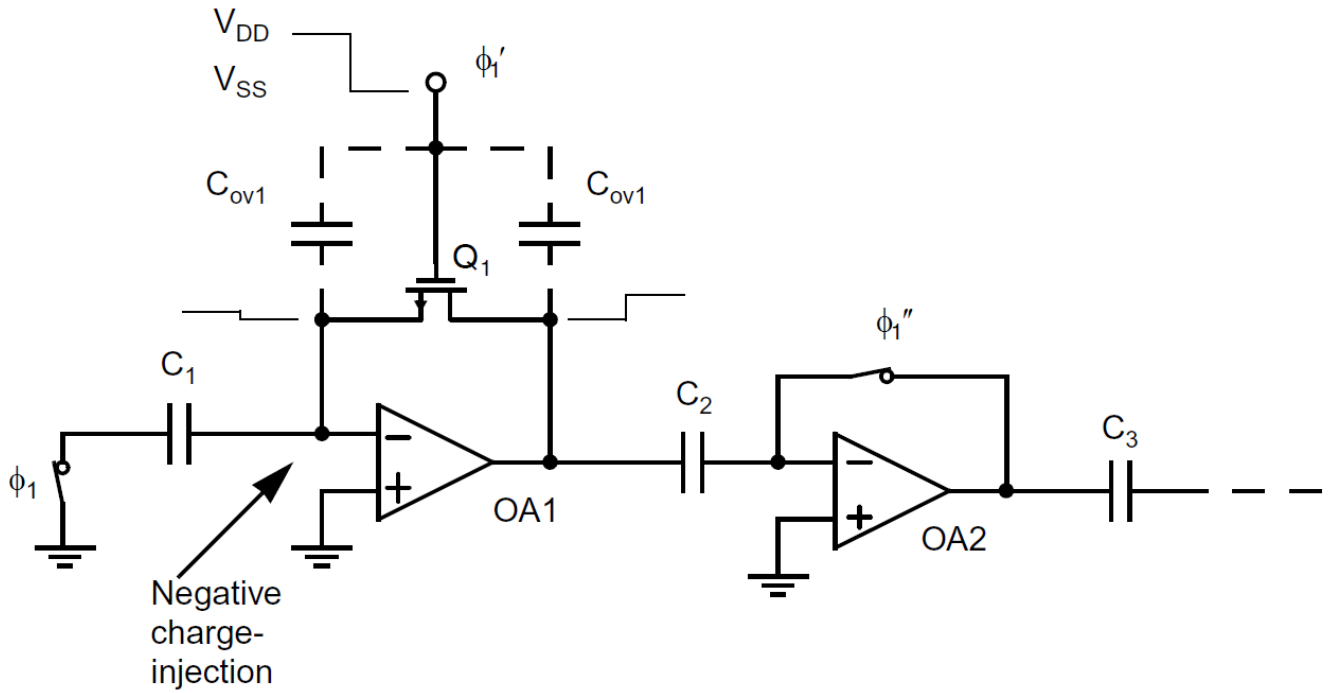
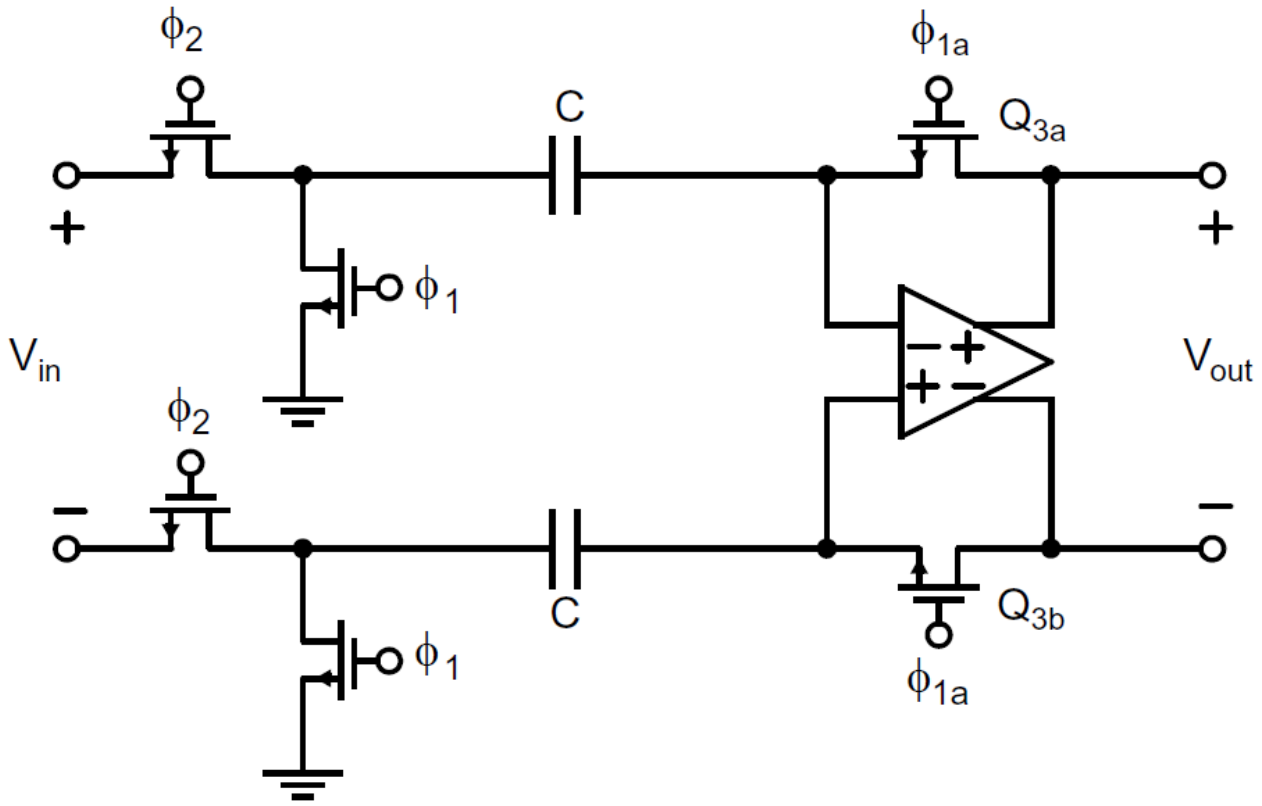
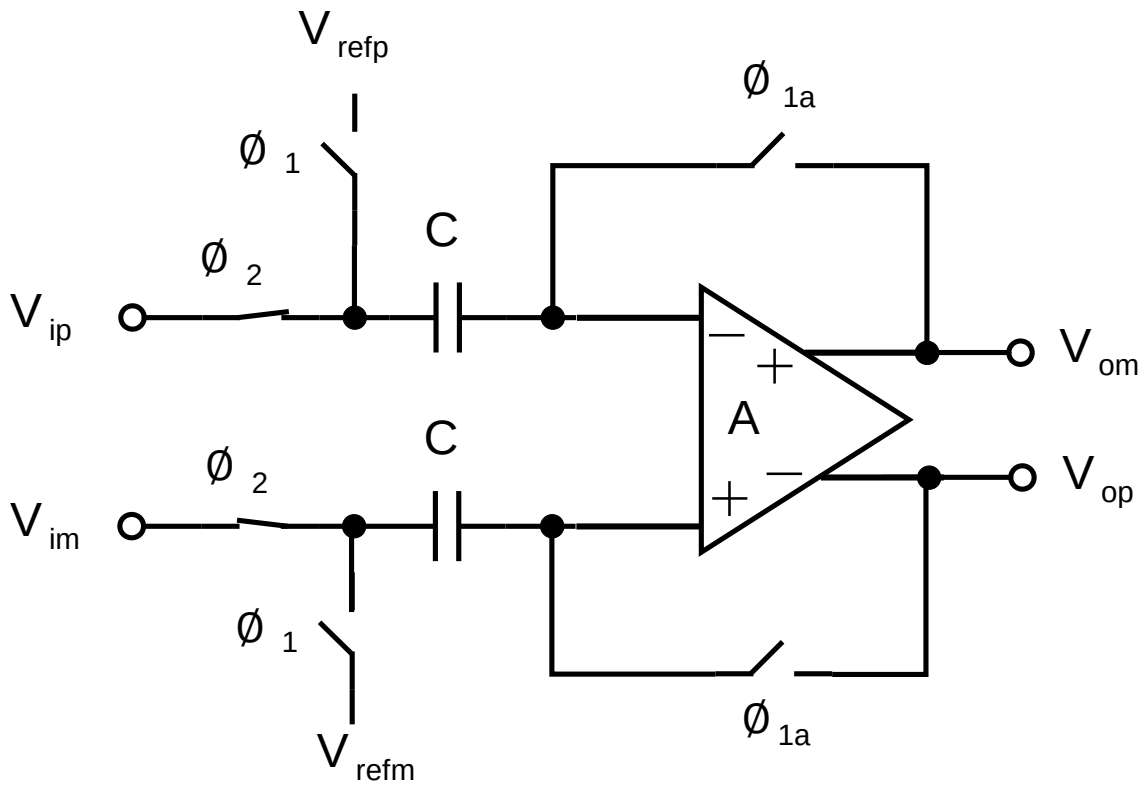


Fig. 10.12 The first stage of the comparator in Fig. 10.11, when the first stage is injecting charge.

Differential Switched-Capacitor Comparator



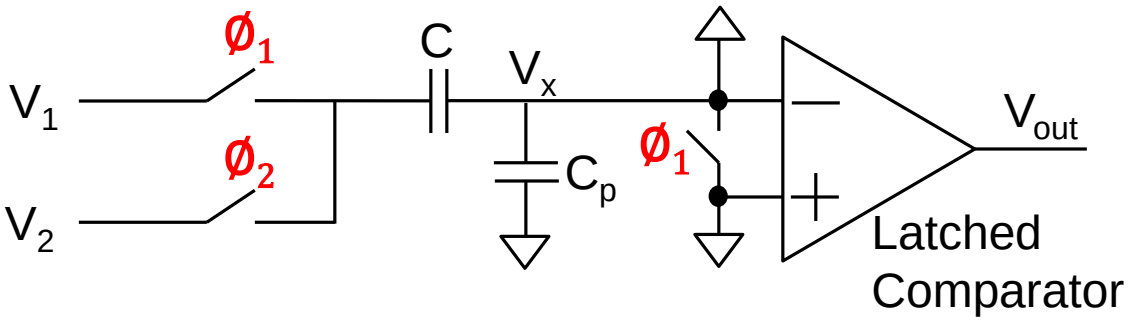
Differential Switched-Capacitor Comparator



$$V_{op} - V_{om} = -A\left[\left(V_{ip} - V_{im}\right) - \left(V_{refp} - V_{refm}\right) - \frac{V_{off}}{A+1}\right]$$

$$\approx -A\left[\left(V_{ip} - V_{im}\right) - \left(V_{refp} - V_{refm}\right)\right]$$

Comparator using Capacitive Coupling



During $\emptyset_1$, the charge at V_x is $Q_1 = C(0-V_1) = -CV_1$

During $\emptyset_2$, the charge at V_x is $Q_2 = C(V_x-V_2) + C_pV_x$

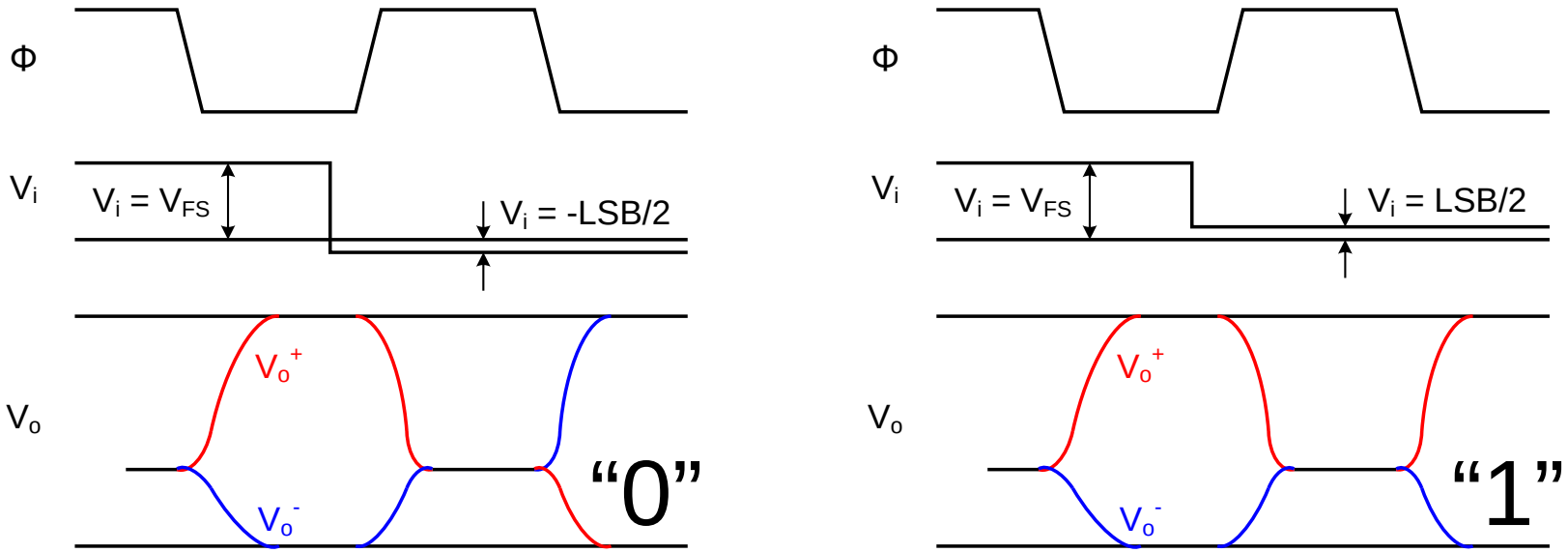
Charge conservation $\rightarrow Q_1 = Q_2$

$-CV_1 = (C+C_p)V_x - CV_2$

$V_x = (V_2-V_1)\cdot C/(C+C_p) \approx (V_2-V_1)$ if $C \gg C_p$

Example: If $V_1 = 1V$, $V_2 = 1.1V$, $V_x \approx 0.1V \rightarrow V_{out} = \text{Low}$

Comparator Test: Overdrive Recovery

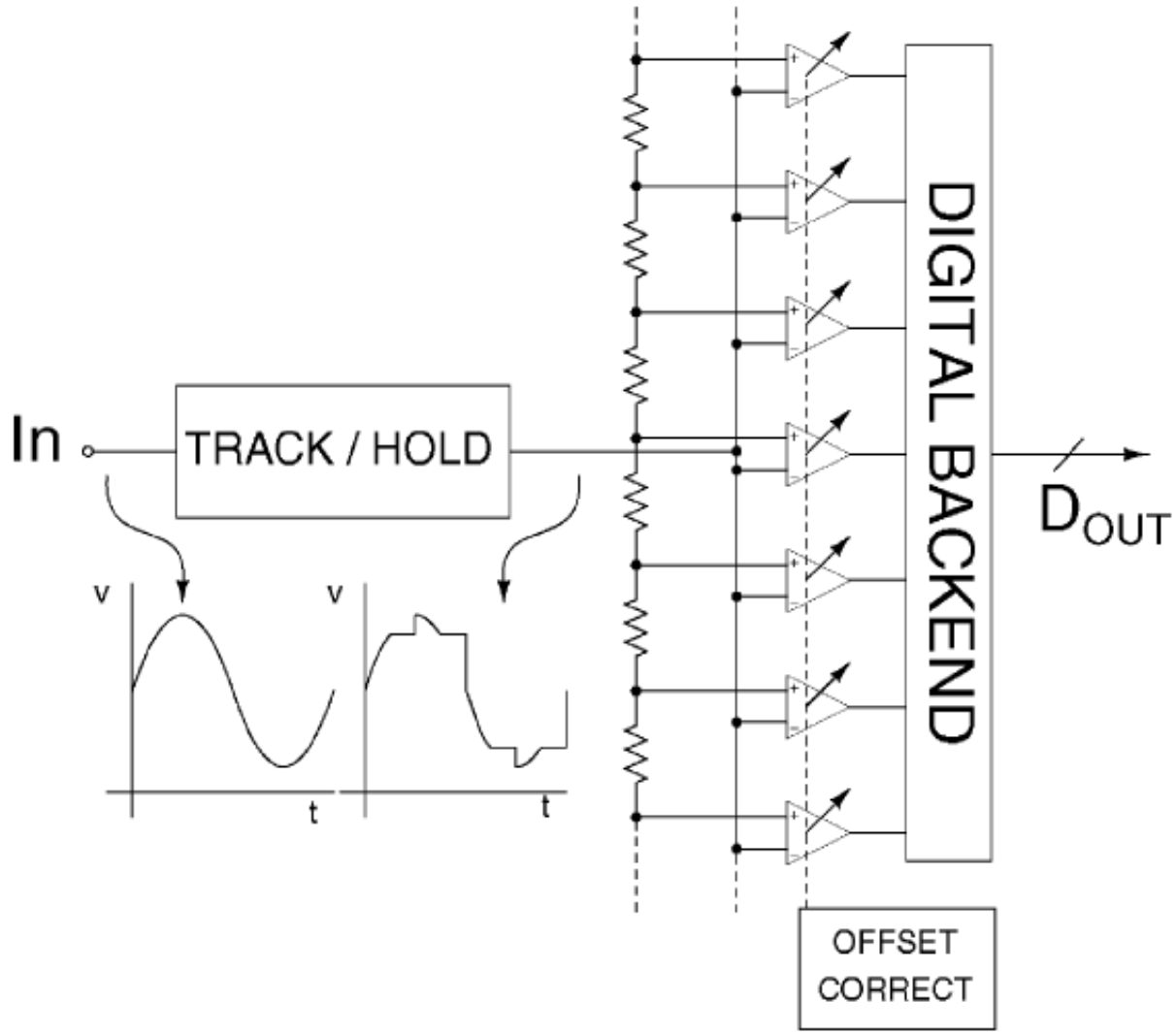


Case I

Case II

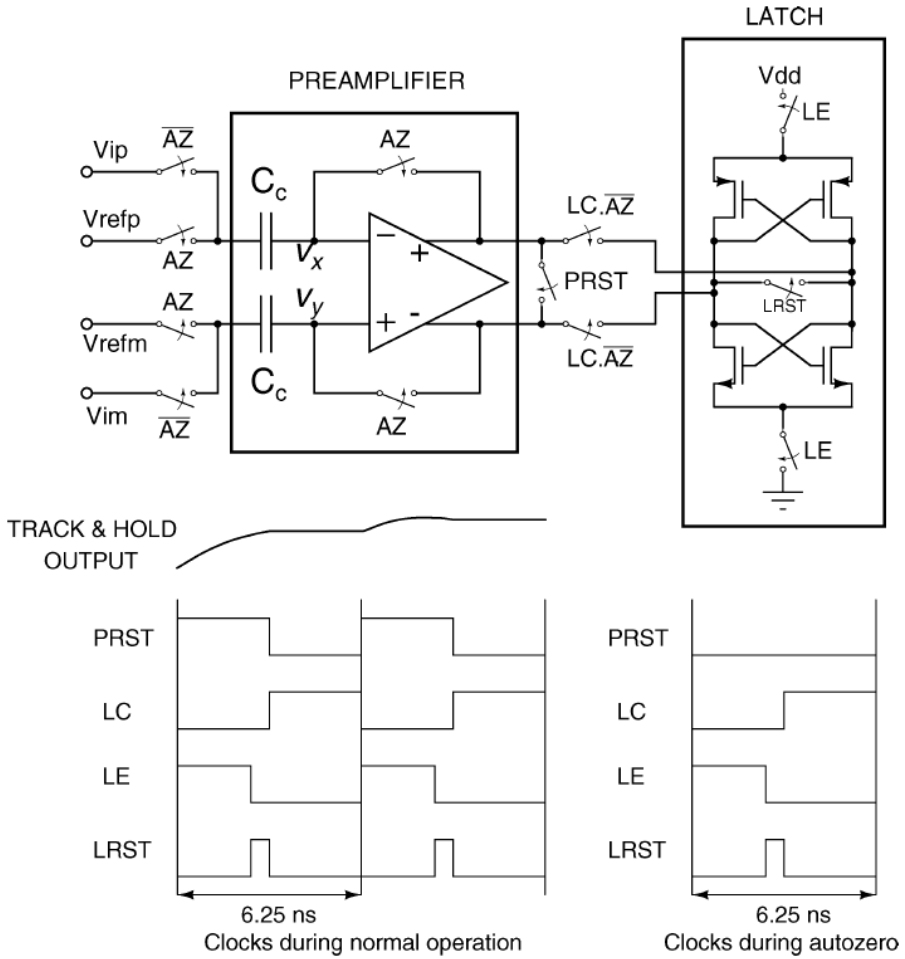
A small input (±0.5 LSB) is applied to the comparator input in a cycle right after a full-scale input is applied; the comparator should be able to resolve to the right output in either case → memoryless

Offset Corrected Comparators in Flash ADC

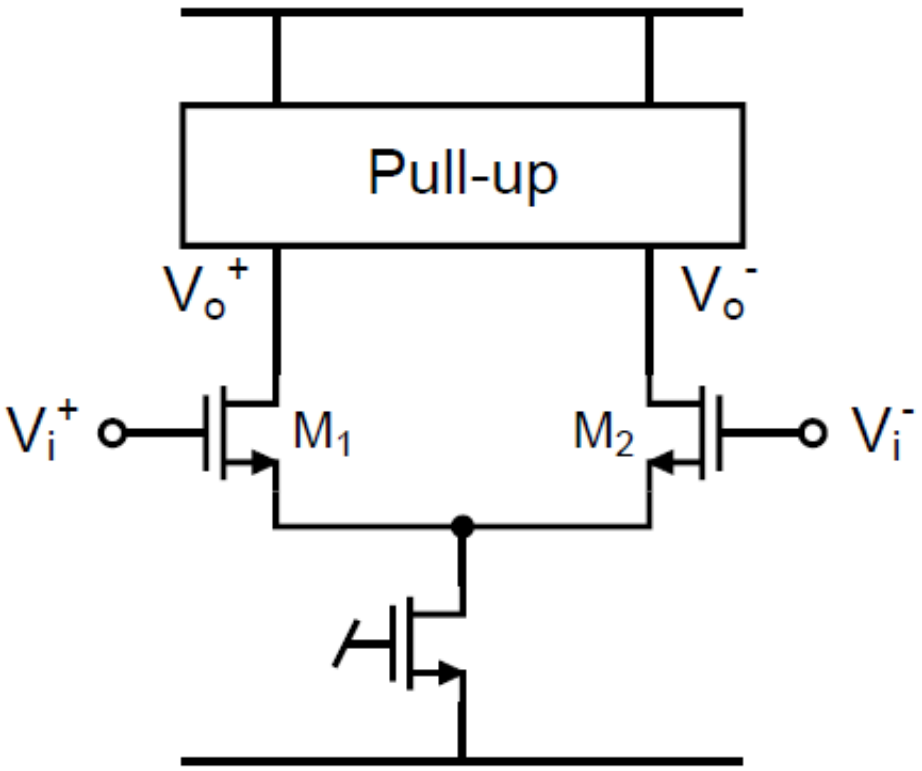


Latched Comparators with Autozero

V. Srinivas, S. Pavan, et al, “A Distortion Compensating Flash Analog-to-Digital Conversion Technique,“ IEEE JSSC, vol. 41, no. 9, pp. 1959-1969, Sep. 2006.



Differential Amplifiers



- NMOS diodepull–up:

$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{(W/L)_1}{(W/L)_L}}$$

- PMOS diodepull–up:

$$A_V = -\frac{g_{m1}}{g_{mL}} = -\sqrt{\frac{\mu_n}{\mu_p}\frac{(W/L)_1}{(W/L)_L}}$$

- Resistorpull–up:

$$A_V = -g_{m1} \cdot R_L$$

Differential Amplifier with Resistor Pull-up