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TuTh11:00-12:30pm

EECS 141: SPRING 04—MIDTERM 2

NAME	Last First

SID	

Problem 1 (on 10):
Problem 2 (on 9):
Problem 3 (on 11):

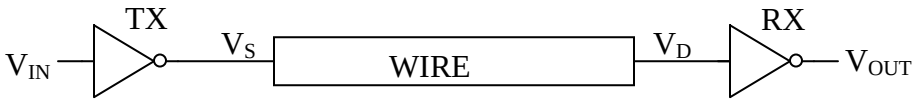
Total	

Problem 1: Interconnect (10 points)

Consider the communication link shown below. The wire is 100 mm long and has some characteristic resistance, capacitance, and inductance per unit length given by

r = 0.02Ω/um c = 133 aF/um l = 333 fH/um

The transmitter and receiver are both CMOS inverters with a 2.5 V supply. However, the transmitter is designed by an inexperienced engineer using the same W/L ratio for the PMOS and NMOS transistors. As a result, the transmitter has an output impedance of 50 Ω when driving a high output, but only 20 Ω when driving a low output.



a. What is the delay from a rising edge at V_{IN} to V_{OUT}? Assume that the inverters have negligible propagation delay (and capacitance), and that the RX inverter switches instantaneously when its input reaches $V_M = V_{DD}/2$ **(3 points)**.

Soln: The wire has

$Z_0 = sqrt(l/c) = 50.0\ \Omega$

$v = 1/sqrt(lc) = 1.50 \times 10^8$ *m/s*

$R = r \times 100{,}000 \mu m = 2\ k\Omega$

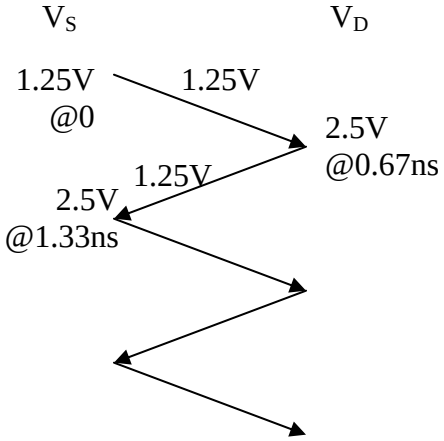
$C = c \times 100{,}000 \mu m = 13.3$ *pF*

Since R >> Z_0, the distributed rc wire model is used. Since R >> TX output impedance, the TX output impedance has negligible effect. Therefore, the delay is determined solely by the wire, and is given by Equation 4.16 (derived from the Elmore delay model)

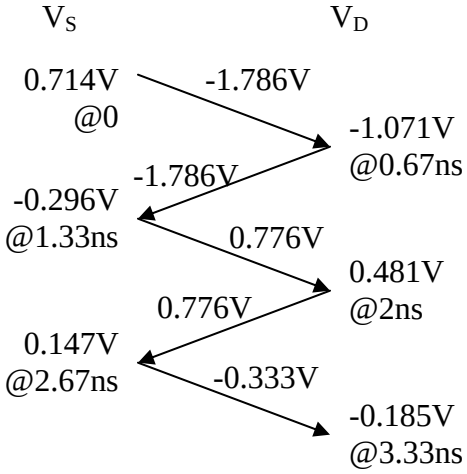
$t_p = 0.69\tau = 0.69\ RC/2 =$ ***9.18 ns***

b. The link designer recognizes that the wiring resistance is slowing down the link. To improve the speed, the wire is redesigned with thicker, lower resistance metal until the resistance is negligible, but with the capacitance and inductance remaining unchanged. Complete the lattice diagrams below for a rising (0 V → 2.5 V) transition at $V_{IN.}$ Stop either at the end of the provided diagrams, or when V_S and V_D are both within 0.1V of their final values. Remember to note the times at which V_S and V_D change. **(4 points)**

<u>VIN: 2.5 V → 0 V</u>



<u>VIN: 0 V → 2.5 V</u>



Soln: This is a lossless lc transmission line with 50 Ω characteristic impedance determined in part (a). The flight time is 100mm/1.50×10^8 m/s = 0.67ns.

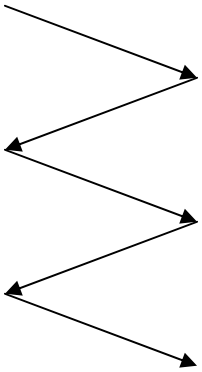
In the case of a falling transition at V_{IN}, TX is driving the wire high and has an output impedance of 50 Ω, which is matched to the line. Thus, $\Gamma_S = (50 - Z_0)/(50 + Z_0) = 0$ and $\Gamma_D = (\infty - Z_0)/(\infty + Z_0) = 1$. Before the transition, all nodes are at 0V. Initial voltage at the TX output leads to $V_S = V_{DD}/2 = 1.25$ V, and a 1.25V wave is launched down the wire. At t = 0.67 ns this wave reaches the RX inverter with infinite input impedance and is reflected with $\Gamma_D = 1$. Thus, the return reflection is 1.25V, and V_D = 0 V + 1.25 V + 1.25 V = 2.5V. When this reflection returns to the TX output at t = 1.33 ns, the reflection coefficient is $\Gamma_S = 0$ so there is no reflection. The wave terminates here and V_S = 2.5V.

*In the case of a rising transition at V_{IN}, TX is driving the line low and has an output impedance of 20 Ω. Thus, $\Gamma_S = (20 - Z_0)/(20 + Z_0) = -0.429$. Note that $V_S = V_D = 2.5$V before the transition, and initial voltage division at the TX output leads to V_S = 2.5 - 2.5*50/(20+50) = 0.714V and a –1.786V wave is launched. This wave reaches the RX inverter at t = 0.67 ns and is reflected with $\Gamma_D = 1$. V_D changes by –1.786 V * 2 and is now -1.071 V. At t = 1.33 ns the reflection reaches the transmitter, and is reflected with coefficient –0.429, resulting in a +0.766 V reflection. V_S changes by –1.786 V + 0.776 V and is now –0.296 V. This process repeats with the numbers shown in the lattice diagram.*

c. Do the same for a falling (2.5 V → 0 V) transition at V_{IN}. **(3 points)**

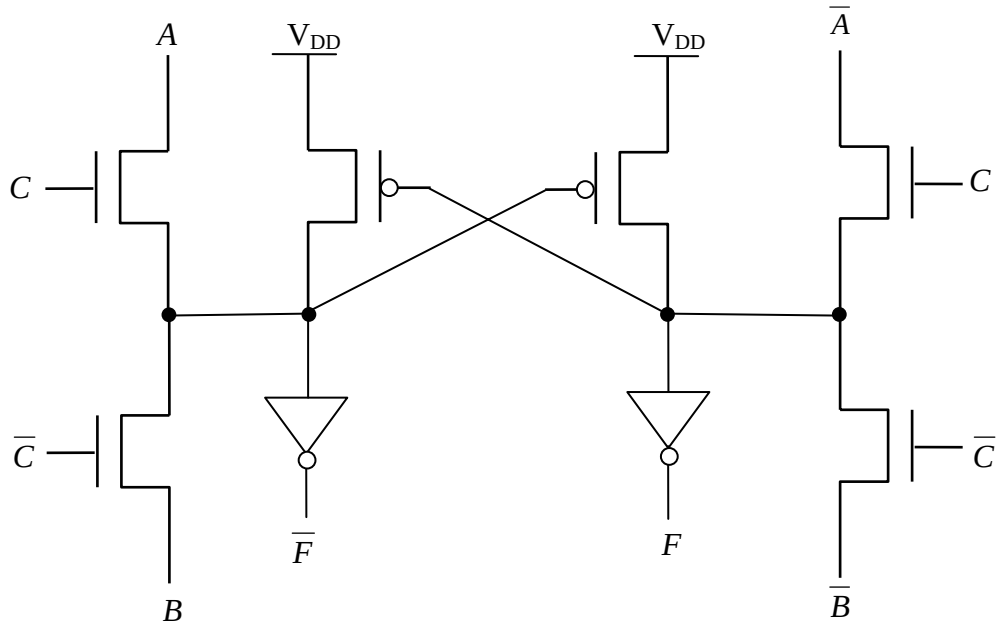
<u>VIN: 2.5 V → 0V</u>

V_S V_D



Problem 2: Complementary Pass-Transistor Logic (9 points)

Consider the complementary pass-transistor logic shown below. It accepts three inputs *A, B, C* and their complements, produces the output *F* and its complement.



a. Fill out the following truth table.

A	B	C	F
0	0	0	*0*
1	0	0	*0*
0	1	0	*1*
1	1	0	*1*
0	0	1	*0*
1	0	1	*1*
0	1	1	*0*
1	1	1	*1*

b. Write down the Boolean function this circuit implements in the given space below. Explain in one sentence the function of this circuit.

The circuit implements the function of a multiplexer which passes A when C is high and B when C is low.

F = $AC + B\overline{C}$

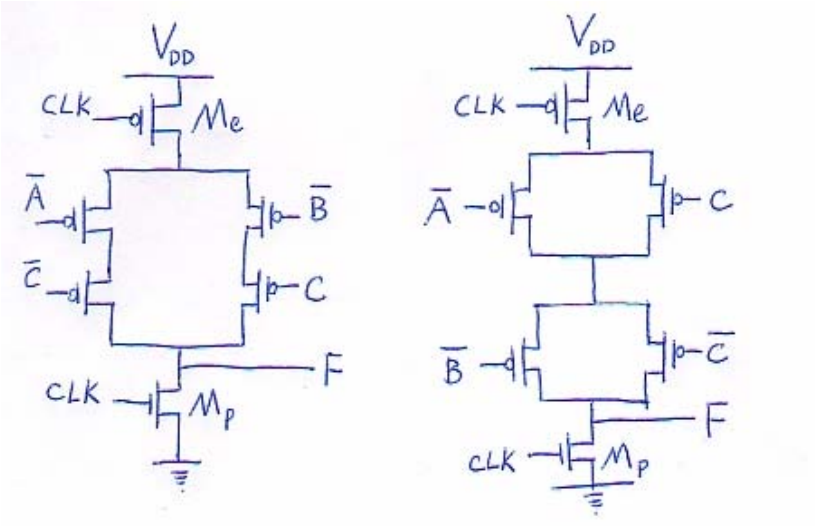
c. Explain the purpose of two PMOS transistors in the circuit.

Two PMOS transistors are a pair of cross coupled level restorers. They help to pull the inputs to both inverters to V_{DD}, thus eliminating static power consumption.

d. Now we want to implement the same function using **dynamic logic** with **PMOS pull up network**. Draw the implementation schematic. You may assume we have inputs in inverted and non-inverted format, however, for the output you are only required to produce *F*.

$$F = \overline{(\overline{A} + \overline{C})(\overline{B} + C)} = \overline{\overline{A}C + \overline{B}\overline{C}}$$

Both implementations should work:



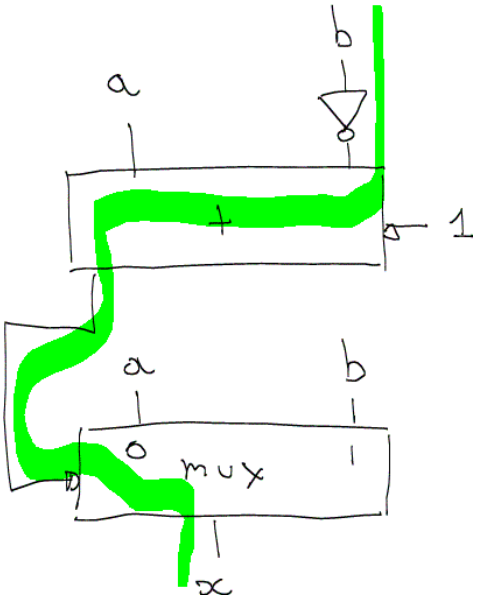
e. Determine the logical effort of the gate you just designed (2 points).
Hint: size the gate first such that a current drive identical to a minimum sized CMOS inverter is obtained.

Size of PMOS transistors, to create an equivalent resistance of 1 is 6 (3 PMOS in series). Hence the logical effort (compared to CMOS inverter) is 6/3 = 2.

Problem 3: Arithmetic (11 points)

Designer Viterbi, working for a famous telecommunications company has to implement a digital hardware module that implements the following logic function:
f = (a>b)? a: b. In other words, the output *f* should be equal to *a* if (*a*>*b*), else it should equal *b*. Both *a* and *b* are N-bit 2's complement numbers.

a. Draw a block diagram of how you think this function should be implemented. Do not show any transistors. Use only gates and higher level modules, such as for instance M x N multipliers (**4 points)**.



Other option: create a real comparator, which ripples from Msb to lsb.

b. Highlight or draw (using arrows) **the longest delay path** on your block diagram. Determine one of the possible set of input values that would trigger that longest path (3 points)

Many different solutions are possible. They have to create a ripple from the lsb to the msb.

A=01111111 and b=111111111

See above

c. Derive an expression for the **worst-case delay of the module as a function of *N* and the delay of the composing gates or modules** (such as t_{carry} of full adder t_{NAND}). Make sure to clearly define each parameter you use in your expression. (2 points)

Tp = tinv + (N-1)tcarry + tsum + tmux

d. Propose one possible way on how you would speed up that design (the faster the better). Redraw your block diagram (2 points).

Use CLA – but maintain only the carry-out generation tree. We are not interested in the intermediate results.
Other option: Logarithmic comparator