EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 2: ADC Architectures

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Course Schedule – Subject to Change

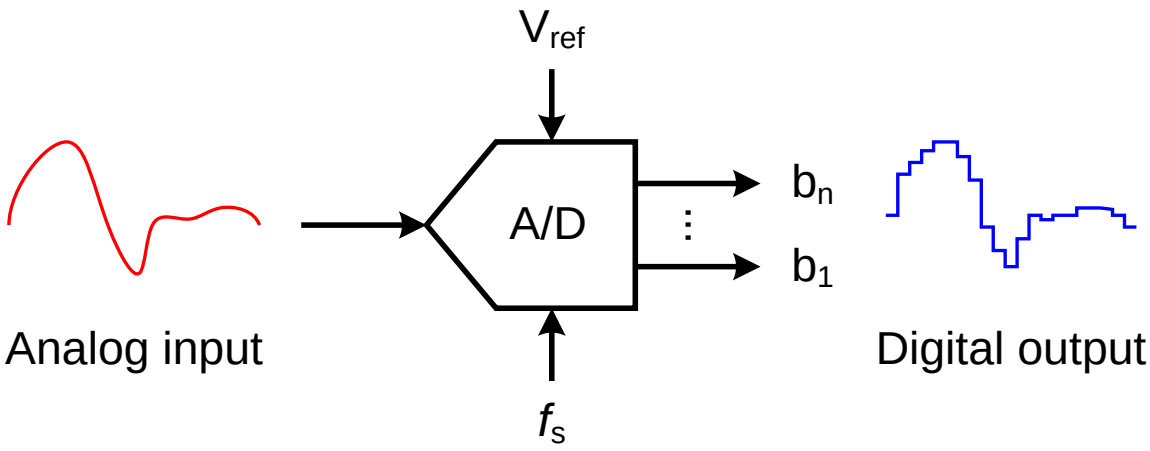
Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	~~Converter basics: AAF, Sampling, Quantization, Reconstruction~~
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	Finish Flash ADC
28-Feb	DAC Architectures - Resistor, R-2R
5-Mar	DAC Architectures - Current steering, Segmented
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

ADC architectures

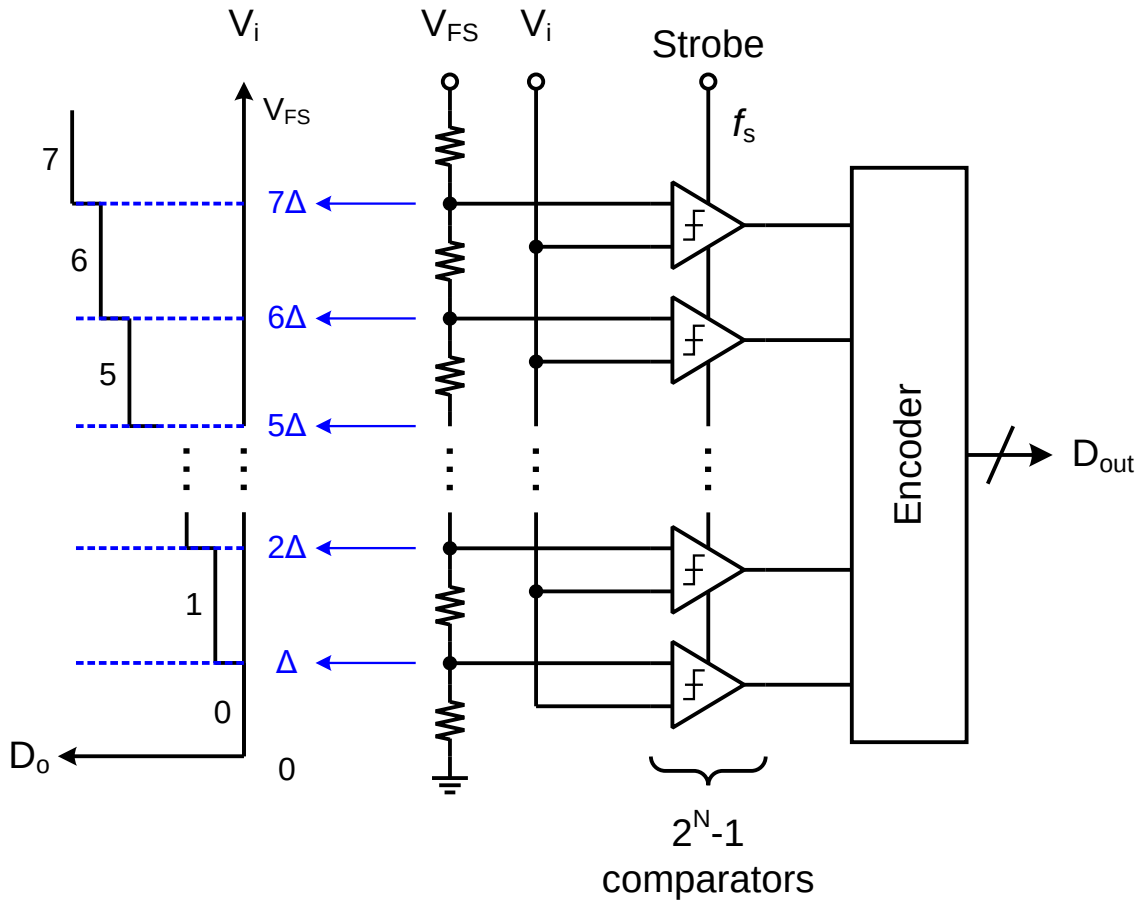
***Midterm Exam dates are approximate and subject to change with reasonable notice.**

ADC

- Digitizes input signal up to Nyquist frequency ($f_N=f_s/2$)
- Sampling rate, f_s should be greater than twice the input bandwidth
- Each sample is digitized to the maximum resolution of converter
- Need good reference and clock



Flash ADC


Vi
VFS
Vi
Strobe
VFS
fs
7
6
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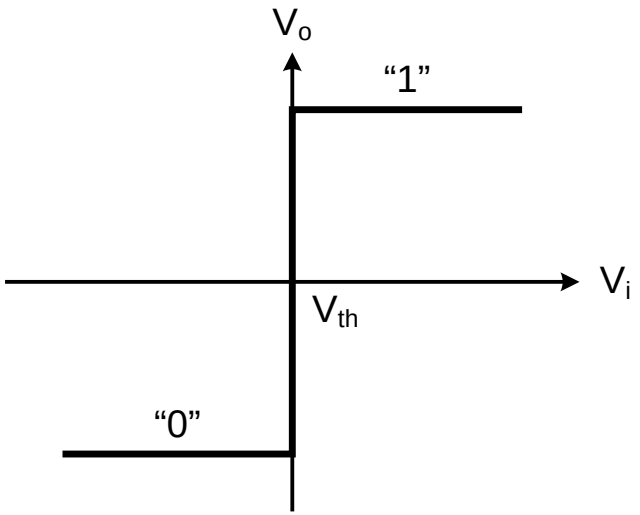
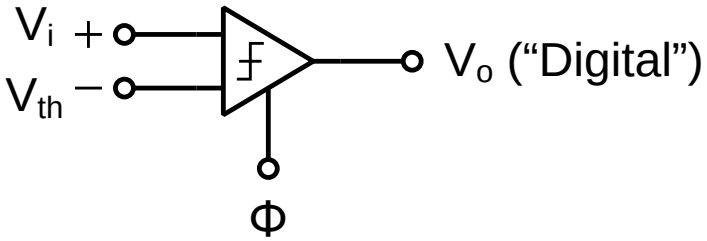
Do
Encoder
Dout
2N-1
comparators

Comparator



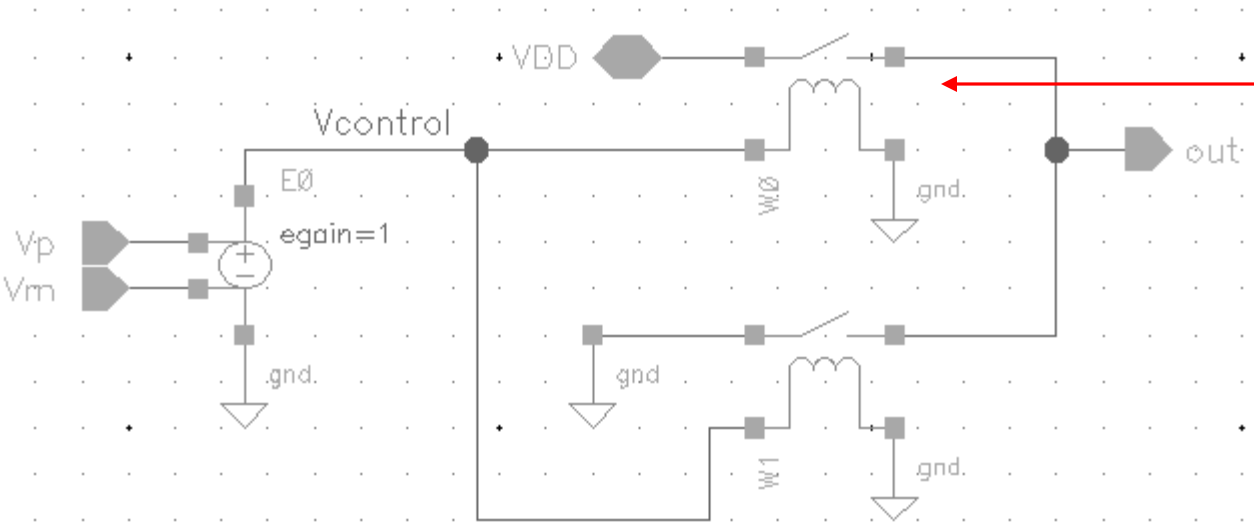
Transfer characteristic (ideal)

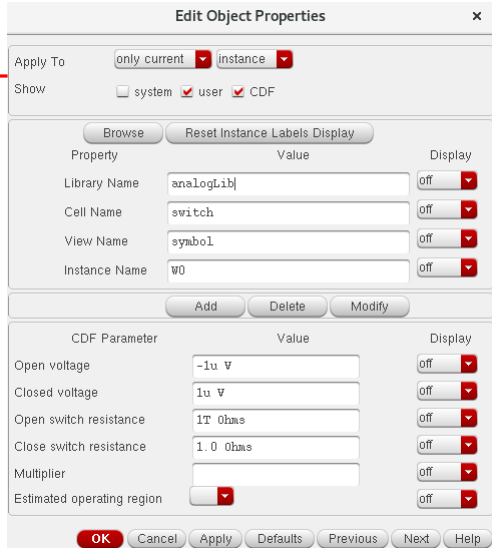


Circuit symbol

Detects the polarity of the analog input signal and produces a digital output (1 or 0) accordingly – threshold-crossing detector

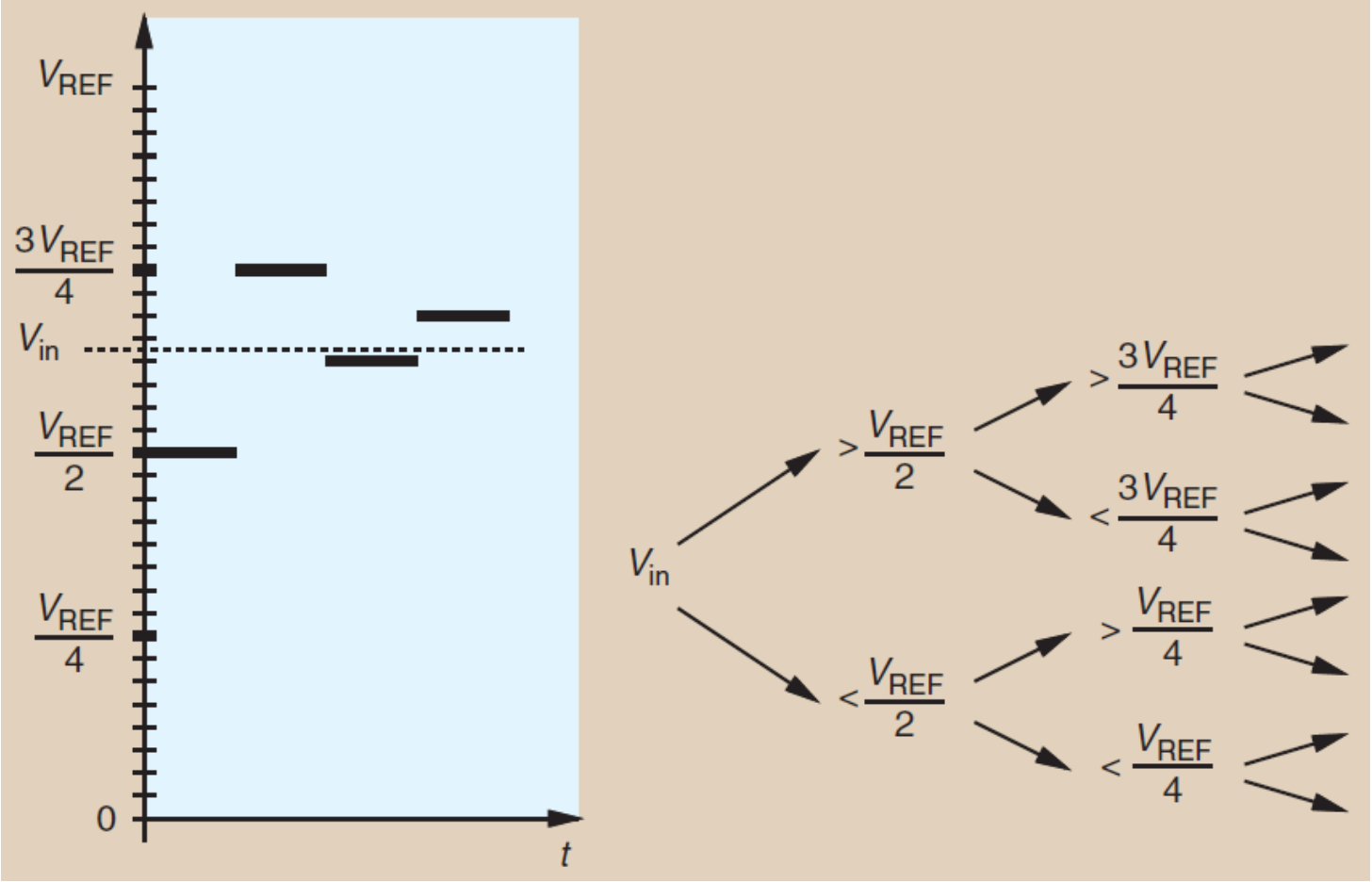
Ideal Comparator



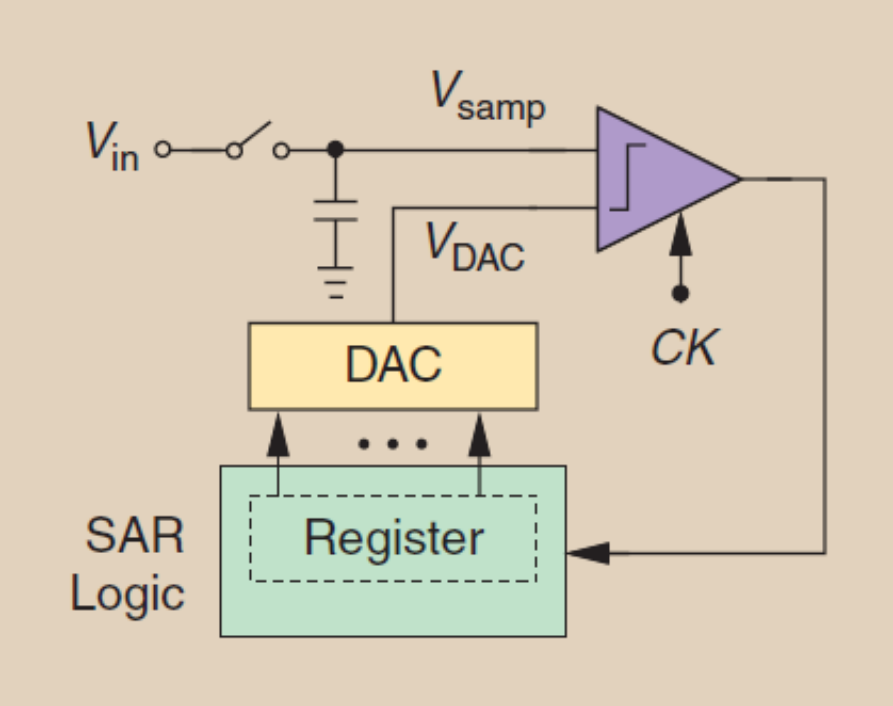


Need reverse polarity for open & close voltages

Binary search for Analog Estimates

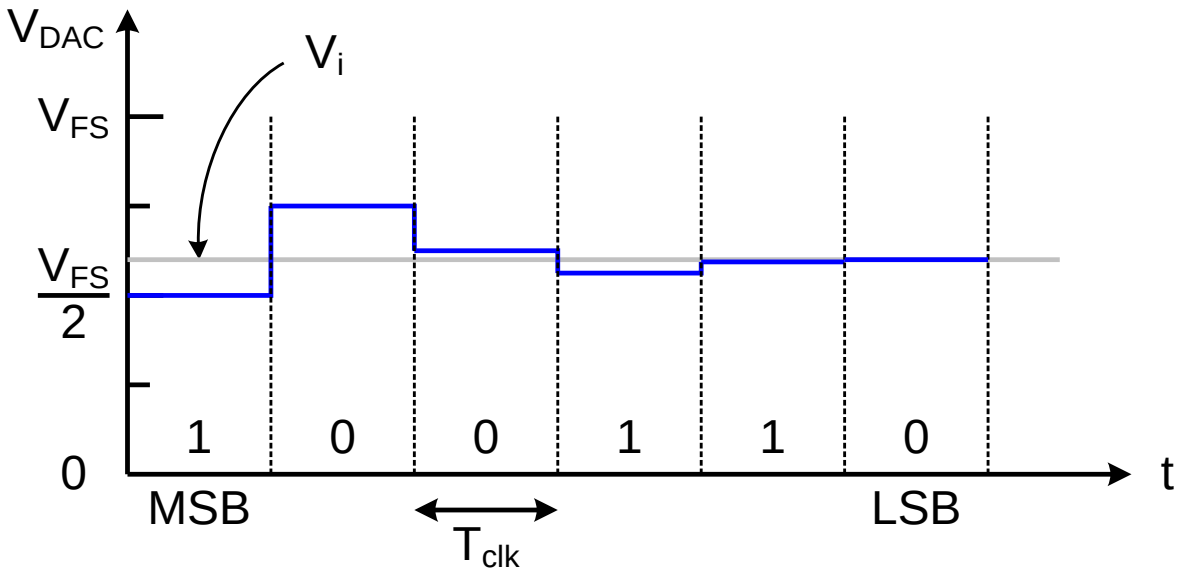


Successive Approximation Register (SAR) ADC



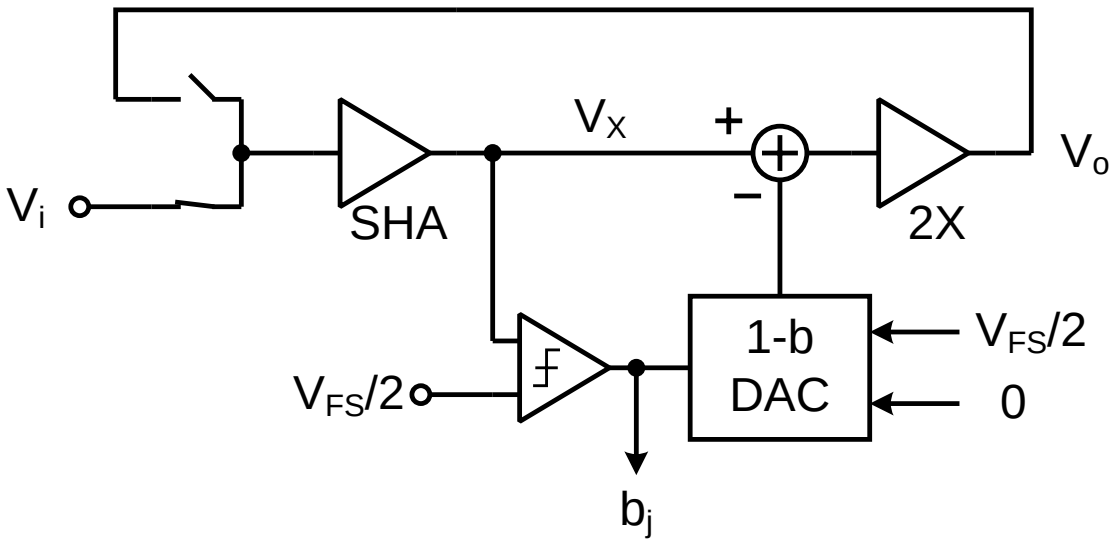
- Binary search algorithm → $N*T_{clk}$ to complete N bits
- Conversion speed is limited by comparator, DAC, and digital logic (successive approximation register or SAR)

Successive Approximation Register (SAR) ADC



- DAC output gradually approaches the input voltage
- Comparator differential input gradually approaches zero

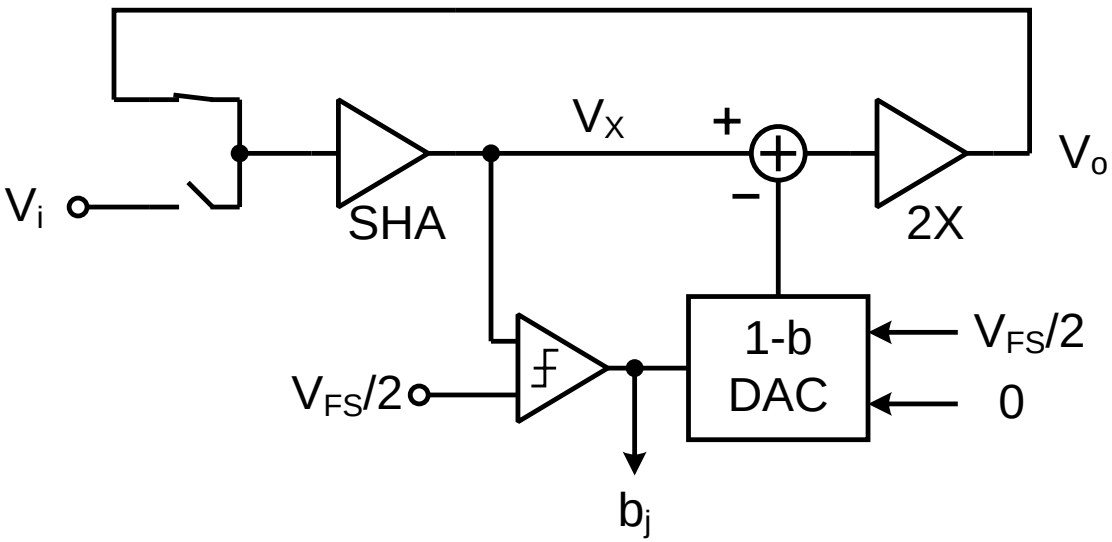
Algorithmic (or Cyclic) ADC



Sample mode

- Input is sampled first, then circulates in the loop for N clock cycles
- Conversion takes N cycles with one bit resolved in each T_{clk}

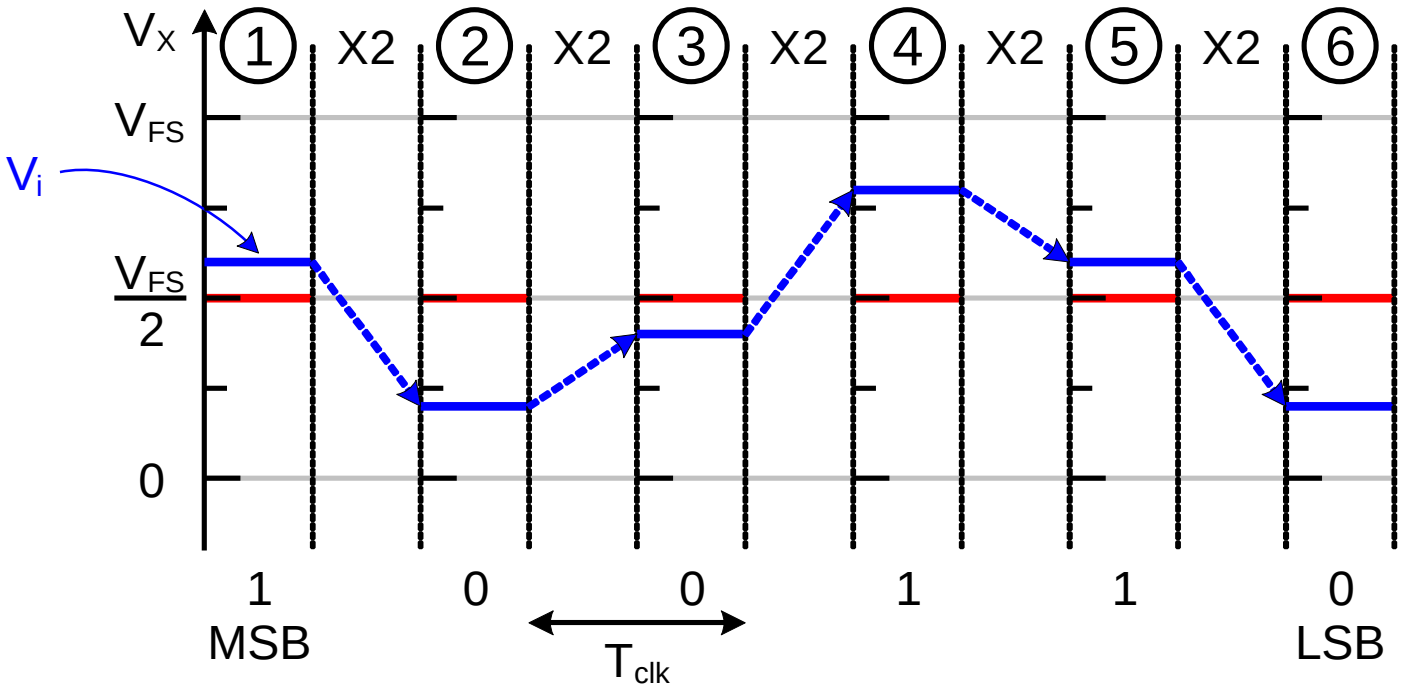
Algorithmic (or Cyclic) ADC



Conversion mode

- If $V_X < V_{FS}/2$, then $b_j = 0$, and $V_o = 2*V_X$
- If $V_X > V_{FS}/2$, then $b_j = 1$, and $V_o = 2*(V_X - V_{FS}/2)$
- V_o is called conversion "**residue**"

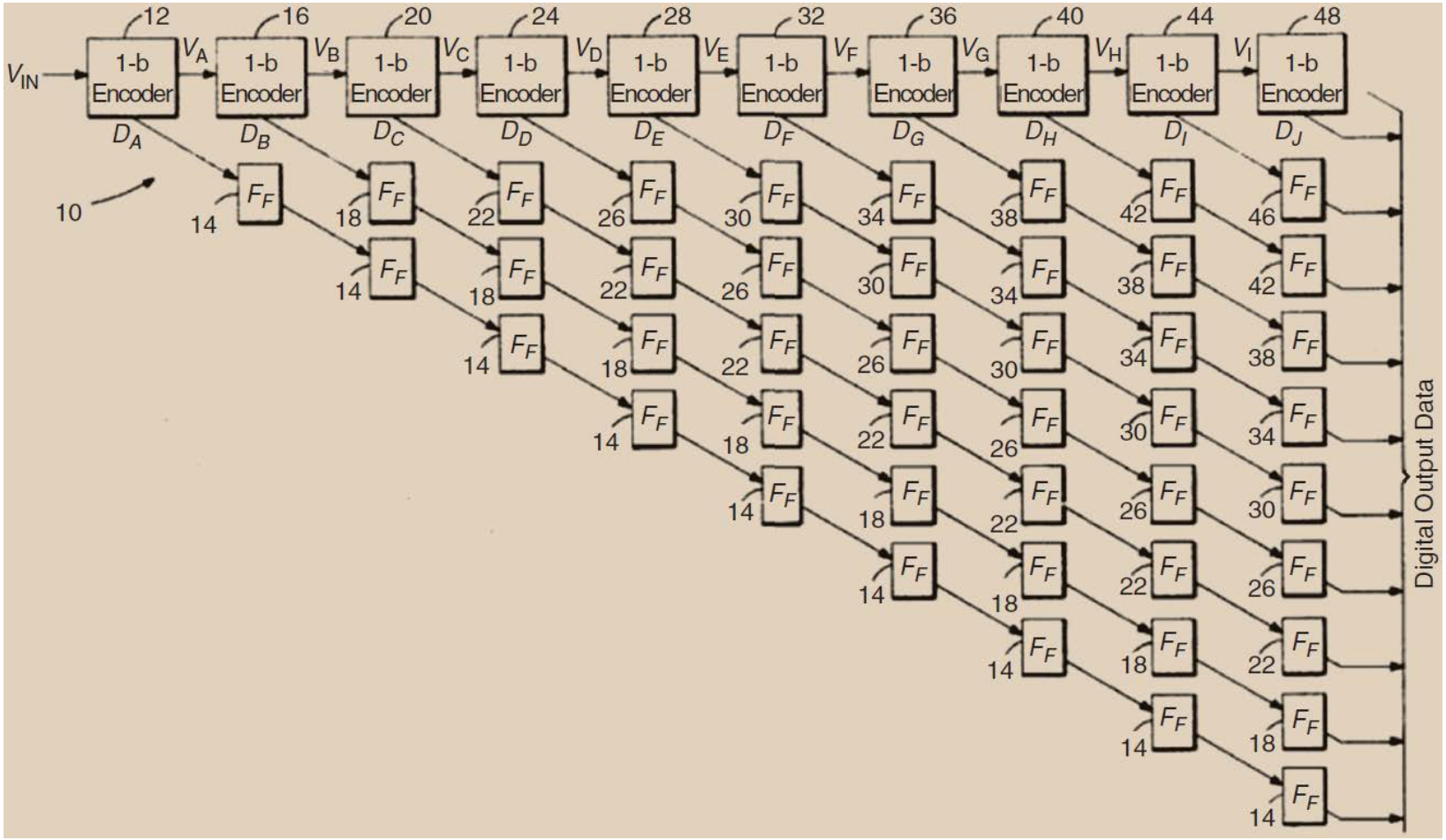
Algorithmic (or Cyclic) ADC



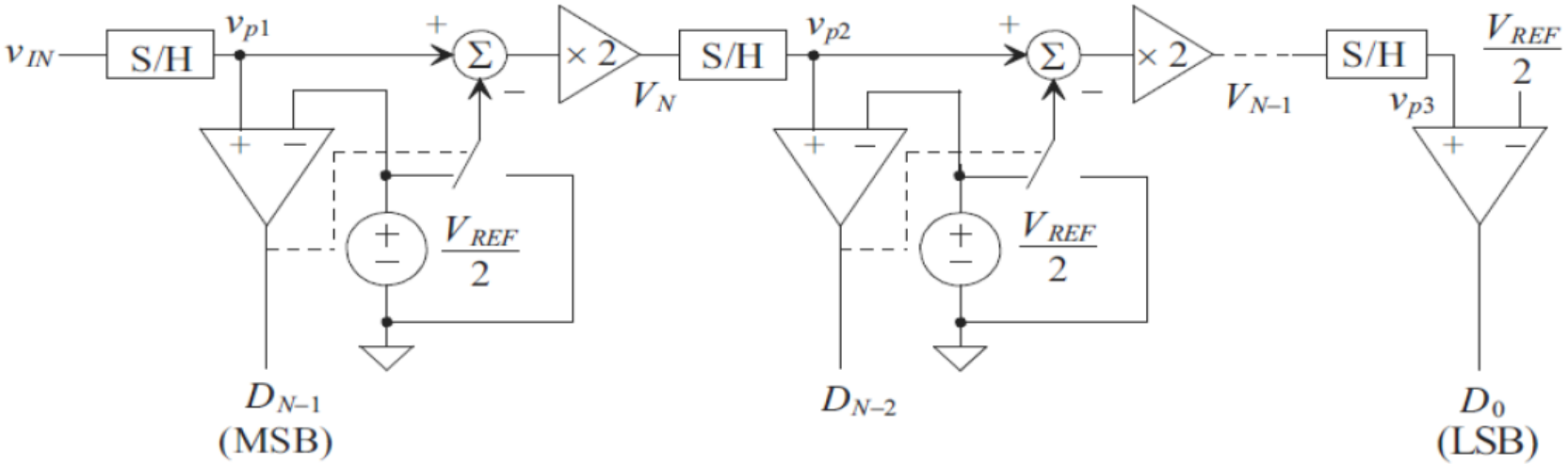
- Constant threshold ($V_{FS}/2$) is used for each comparison
- Residue experiences 2X gain each time it circulates the loop

1-bit/stage Pipelined ADC

J. A. Severin, “Technique for high speed analog-to-digital conversion,”
U.S. patent 3,599,204, Aug. 10, 1971



1-bit/stage Pipelined ADC



1-bit/stage Pipelined ADC