University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

B. Nikolić

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12:30-3:30pm

EECS 141: FALL 2002—FINAL EXAM

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):
NMOS:
$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$
PMOS:
$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last First

GRAD/UNDERGRAD	

Problem 1: _____/ 10

Problem 2: _____/ 8

Problem 3: _____/ 10

Problem 4: _____/ 10

Problem 5: _____/ 10

Problem 6: _____/ 18

Problem 7: _____/ 8

Total: _____/ 74

PROBLEM 1. Devices and delay models (10 points)

A company *A* makes a breakthrough invention of the PMOS transistor that has identical I-V characteristics as an NMOS with the same input capacitance. They also implement it in SOI, where the diffusion capacitance is negligible.

a) (6 pts) If the logical effort of the inverter in this technology is 1, find the logical efforts of 2-input NAND and NOR gates.

b) (4 pts) What is the optimal fanout of an inverter in this technology?

PROBLEM 2: Technology Scaling (8 points)

You work in a company that successfully designed a 4GHz microprocessor in 130nm technology with V_T of 0.3V. The part runs at 1.5V, and the measured skew is 20ps. The power of the 100mm^2 part turned out to be 100W, which is too high for the inexpensive heat removal that you planned. Your colleagues that work on thermal engineering request you to lower the power to 70W to have reasonably inexpensive cooling.

a) (4 pts) If you lower the power to 70W by scaling down the supply, at what frequency would the part run? Assume that your skew does not scale with the supply voltage and the devices are always velocity saturated.

b) (4 pts) You are considering scaling the part to a 90nm process with V_T = 0.25V. What would be the operating frequency of the microprocessor in this technology with 1.2V supply? Power dissipation? Assume that skew does not scale.

PROBLEM 3. Logical effort. (10pts)

Determine sizes of the transistors M_1-M_6 in the circuit of Figure 2 that provide the same pull-up and pull-down current at the output *Z* as a unit inverter (ratio of PMOS to NMOS in this inverter is 2:1). The input capacitance of all inputs (*A*, *B*, and *C*) should be the same. Then determine the logical effort of the circuit.

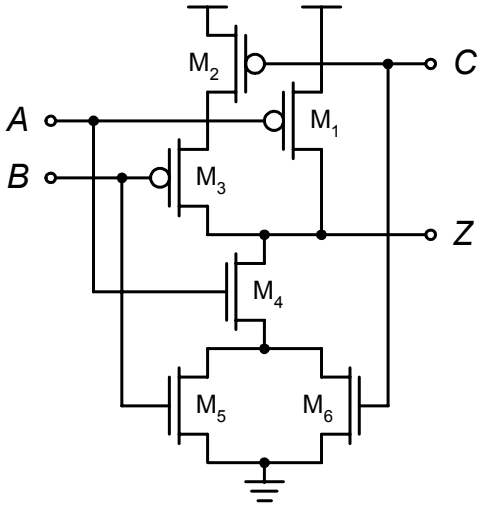
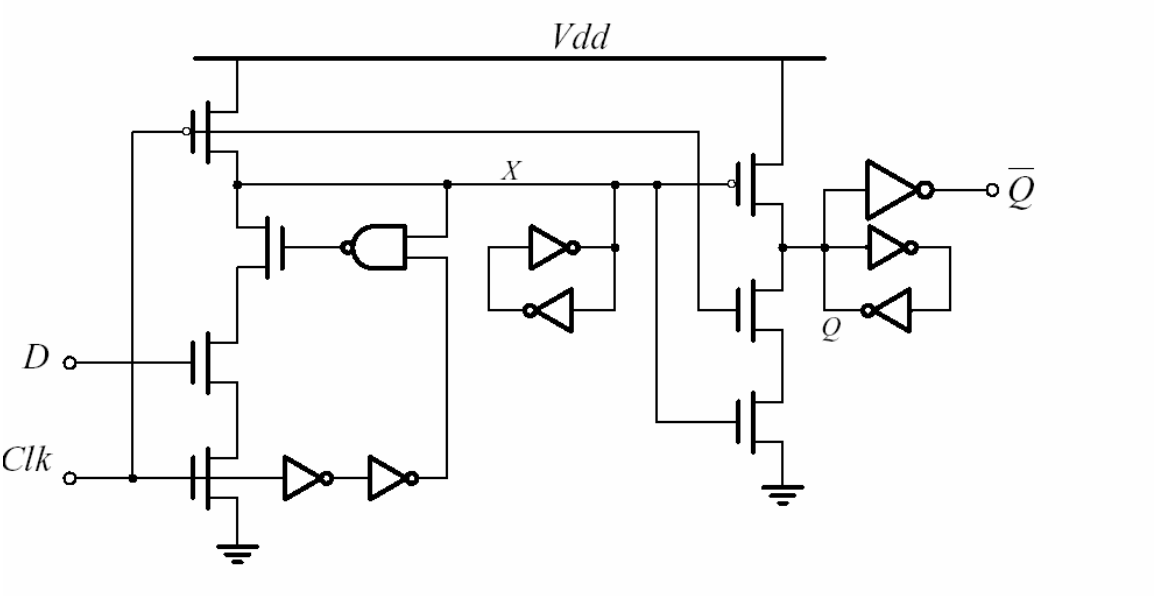


Figure 2.

PROBLEM 4. Sequential circuits. (10 pts)



a) (2 pts) Would the sequential circuit from the figure above be considered a latch, a master-slave latch pair or a pulse-triggered latch? Briefly explain your answer.

b) (4 pts) Draw the timing waveforms for this circuit.

D

X

$\overline{Q}$

c) (4pts) Redesign this circuit, such that it also implements an OR function of the inputs.

PROBLEM 5: Dynamic Circuits. (10 points)

Consider a 16-bit wide zero detector ($N = 16$) implemented in footless domino logic, as shown in Figure 5, implemented in 90nm, 1.0V, technology that has 70nA leakage current for both NMOS and PMOS transistors. I_{onN} (@ $V_{DD} = 1V$) is 600μA/μm, I_{onP} (@ $V_{DD} = 1V$) is 300μA/μm. The requirement in your company is that the keeper must provide 5% of the maximum pull down current in the NMOS network.

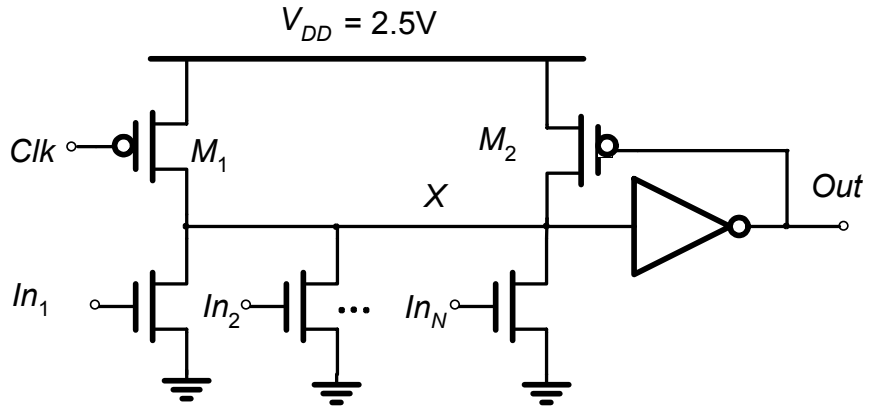


Figure 5.

a) (2pts) What is the largest leakage current at node X, if there is no keeper, and all NMOS transistors are 1μm wide?

b) (8 pts) Draw (on the same diagram) the voltage-transfer characteristics of the dynamic gate (V_X (V_{In})), with a 5% keeper, for two cases: when only one input switches, and when all the inputs switch. Please clearly label the breakpoints on the graph.

PROBLEM 6: Adders (18 points)

In this problem we will analyze and compare two carry lookahed trees: the Kogge – Stone tree (Figure 6a) that you studied in the class, and an alternate one (Fig.2). Both are 16-bit trees. As usual, the dots present the 'dot' operators.

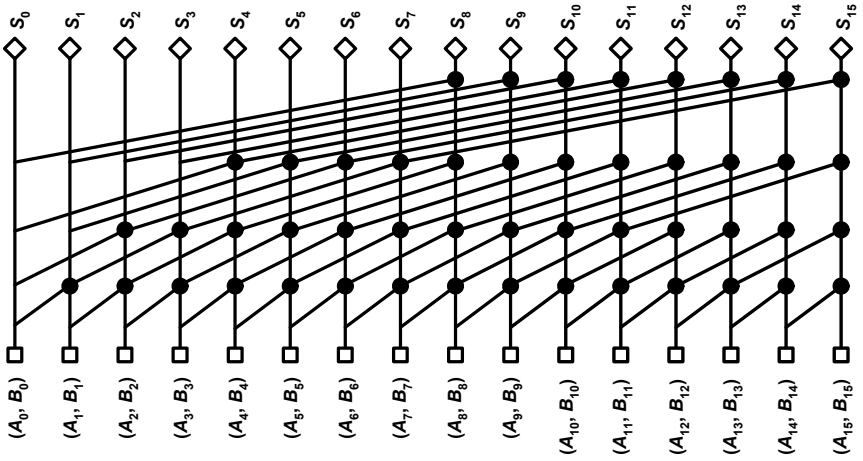


Figure 6.a

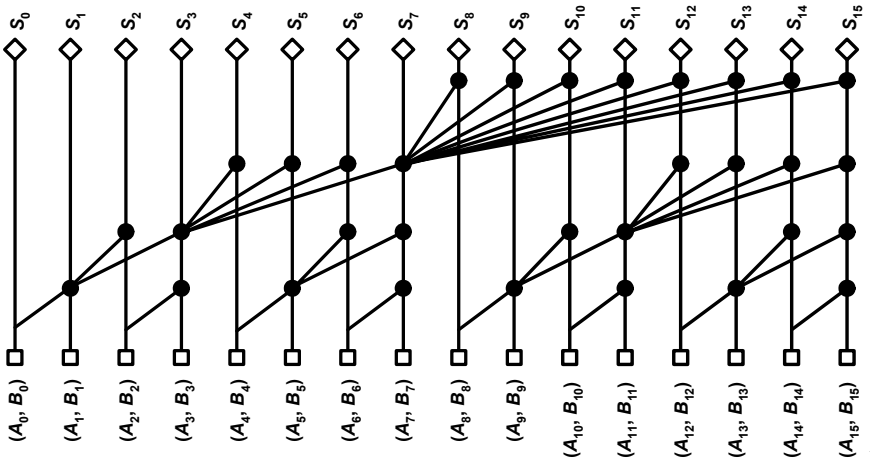


Figure 6.b.

a) (1 pt) What is the radix of each of the above trees?

b) (6 pts) Draw the critical path for each tree.

c) (4 pts) Compute the overall branching effort on the critical path for each tree.

d) (4pts) Generalize (express as a function of N) your result from c) for the case when the tree has 2^N bits.

e) (3pts) Briefly explain in which situations you would use each of the trees. Consider different bitwidths, performance targets and power budgets.

PROBLEM 7: Timing (8 points)
Let's analyze the digital system from Figure 7. Combinational logic (with indicated maximum and minimum propagation delays) is separated by two registers. The registers are edge triggered with $t_{Clk\text{-}Q}$ = 500ps, setup times of t_{su} = 200ps and hold times of t_h = 100ps.

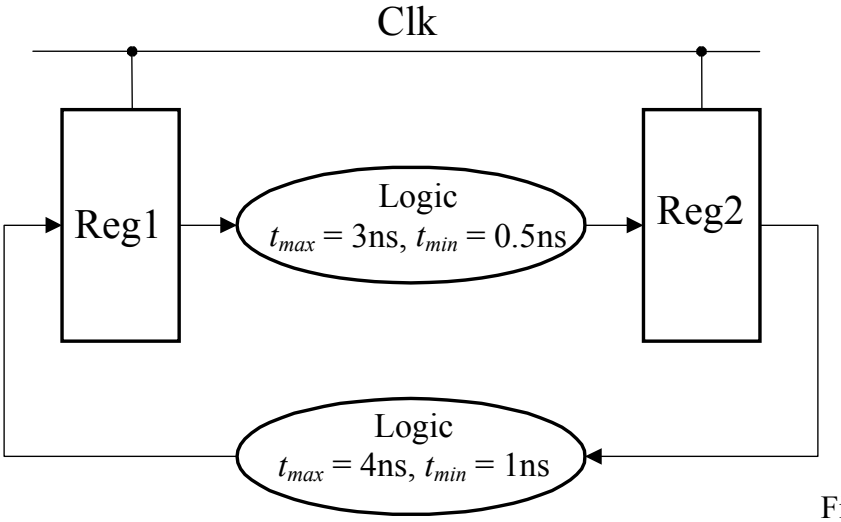


Figure 7.

a) (4 pts) What is the maximum operating frequency of this system if there is no skew?

b) (4 pts) What is the maximum allowable skew in this system?