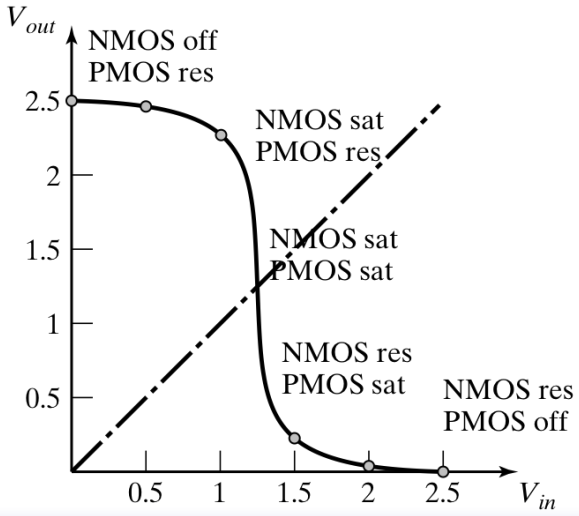
EE141-Spring 2010 Digital Integrated Circuits

Lecture 12
Inverter Delay + Energy

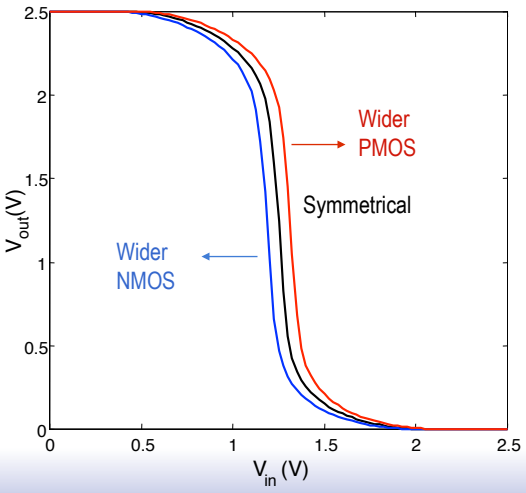
Administrativia

- HW 4 Due Today. New HW today as well.
- Final Lab next week
- Project to be launched on Wednesday! Probably is wise to be in class that day.

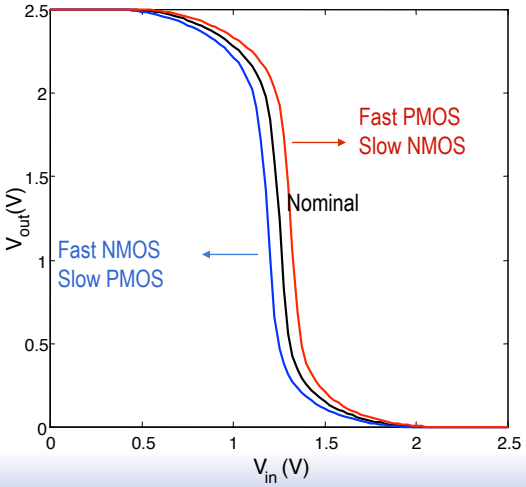
CMOS Inverter VTC



Impact of Sizing

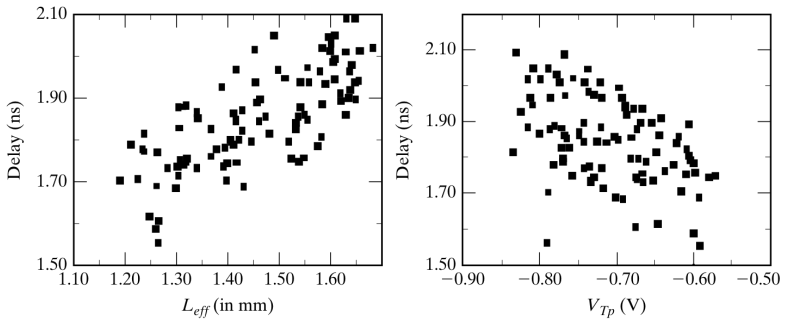


Impact of Process Variations



Process Variations

Not all transistors are alike
Impacts parameters such as reliability and performance

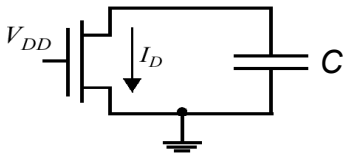


Define process corners: SS, FF, SF, FS

CMOS Switching Delay

MOS Transistor as a Switch

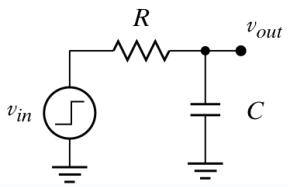
- Discharging a capacitor



$$i_D = i_D(v_{DS})$$

$$i_D = C\frac{dV_{DS}}{dt}$$

- We modeled this with:



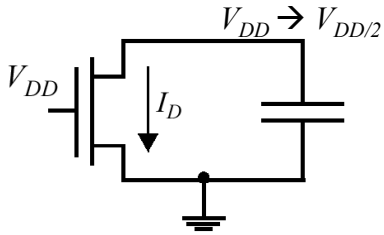
t_p = ln (2) RC

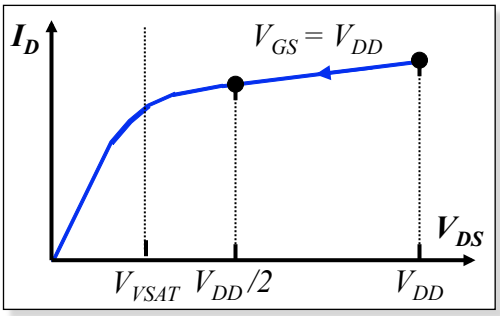
MOS Transistor as a Switch

- Real transistors aren't exactly resistors
  - Look more like current sources in saturation
- Two questions:
  - Which region of IV curve determines delay?
  - How can that match up with the RC model?

Transistor Discharging a Capacitor

• With a step input:

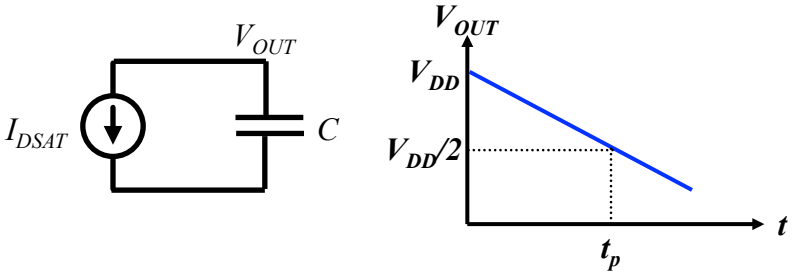




• Transistor is in (velocity) saturation during entire transition from V_{DD} to $V_{DD}/2$

Switching Delay

- In saturation, transistor basically acts like a current source:

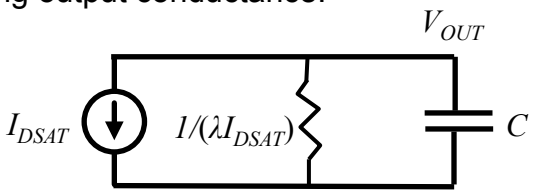


$$V_{OUT} = V_{DD} - (I_{DSAT}/C)t \longrightarrow \boxed{t_p = C(V_{DD}/2)/I_{DSAT}}$$

Defining IDSAT

Switching Delay (with Output Conductance)

- Including output conductance:

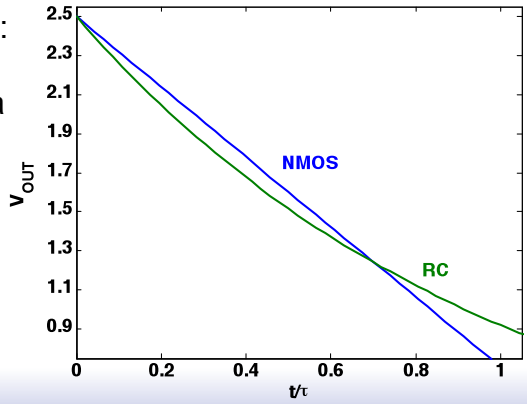


$$V_{OUT} = \left(V_{DD} + \lambda^{-1}\right) e^{-t/(C/\lambda I_{DSAT})} - \lambda^{-1}$$

- For "small" λ: $t_p \approx \dfrac{C\left(V_{DD}/2\right)}{\left(1+\lambda V_{DD}\right) I_{DSAT}}$

RC Model

- Transistor current not linear on V_{OUT} – how is the RC model going to work?
- Look at waveforms:
- Voltage looks like a ramp for RC too



Finding Req

- Match the delay of the RC model with the actual delay:

$$t_p = t_{p,RC}$$

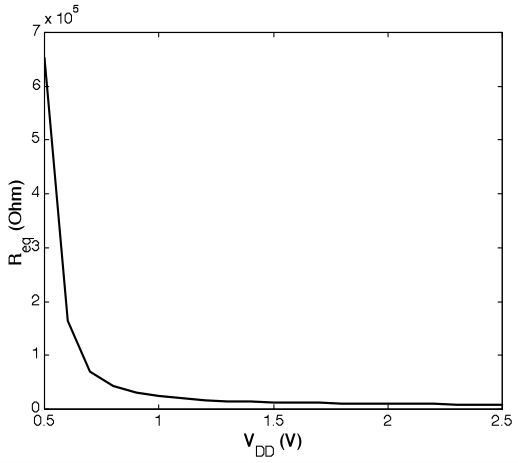
$$\frac{C(V_{DD}/2)}{(1+\lambda V_{DD})I_{DSAT}} = \ln(2) R_{eq} C \longrightarrow \boxed{R_{eq} = \frac{(V_{DD}/2)}{\ln(2)(1+\lambda V_{DD})I_{DSAT}}}$$

- Often just: $\boxed{R_{eq} \approx \frac{1}{2 \cdot \ln(2)} \frac{V_{DD}}{I_{DSAT}}}$

- Note that the book uses a different method and gets $0.75 \cdot V_{DD}/I_{DSAT}$ instead of ~$0.72 \cdot V_{DD}/I_{DSAT}$.

The Book's Method

The Transistor as a Switch

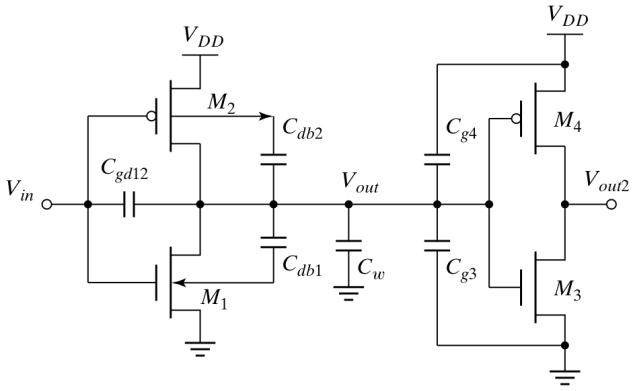


The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

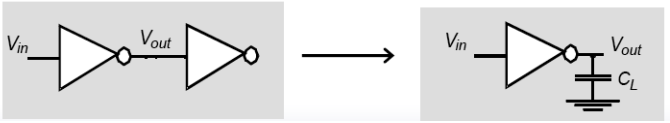
V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

Inverter Capacitances



Inverter Capacitance Model

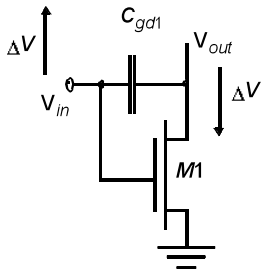
- Capacitance models important for analysis and intuition
  - But often need something simpler to work with
- Simpler model:
  - Lump together as effective linear capacitance to (ac) ground
  - In most processes: *Cg* = *Cd* = 1.5 – 2fF·W(μm)



Lumping the Caps

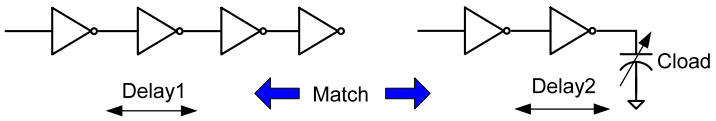
The Miller Effect

- As V_{in} increases, V_{out} drops
  - Once get into the transition region, gain from V_{in} to V_{out} > 1
- So, C_{gd} experiences voltage swing larger than V_{in}
  - Which means you need to provide more charge
  - Makes C_{gd} look larger than it really is
- Known as the "Miller Effect" in the analog world

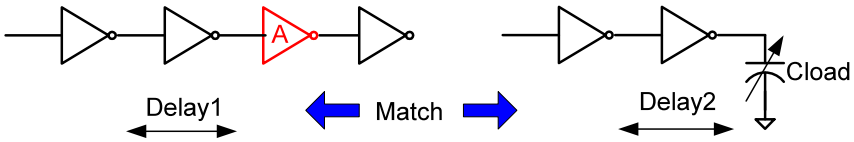


Model Calibration - Capacitance

- Can calculate C_g, C_d based on tech. parameters
  - But these models are simplified too
- Another approach:
  - Tune (e.g., in spice) the linear capacitance until it makes the simplified circuit match the real circuit
  - Matching could be for delay, power, etc.

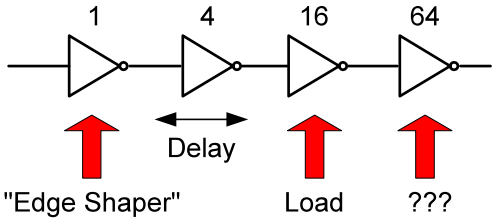


Model Calibration for Delay



- For gate capacitance:
  - Make inverter fanout 4
  - Adjust C_{load} until Delay1 = Delay2
- For diffusion capacitance
  - Replace inverter "A" with a diffusion capacitance load

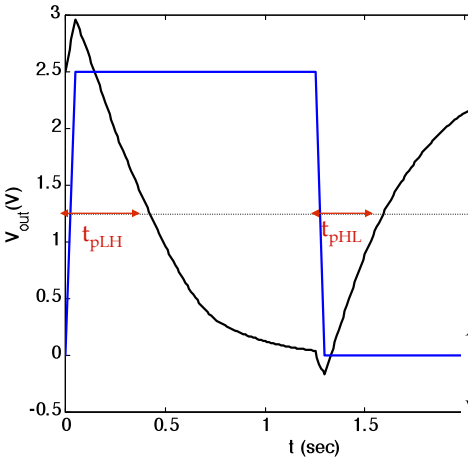
Delay Calibration



- Why did we need that last inverter stage?

Propagation Delay

Transient Response

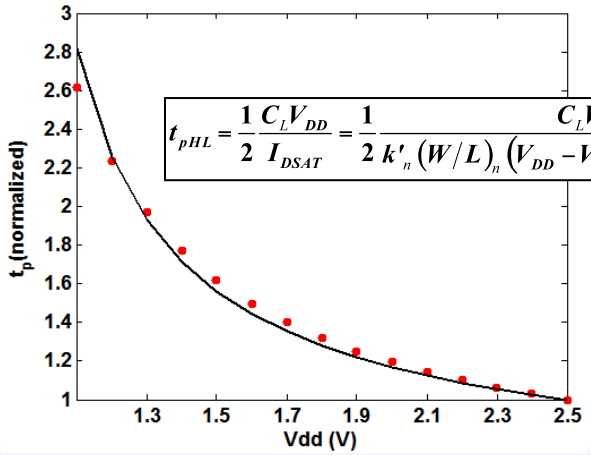


$t_{pHL} = 0.69\ C_L\ R_{eqn}$
$t_{pLH} = 0.69\ C_L\ R_{eqp}$

$$R_{eq} = \frac{1}{2\ln(2)}\frac{1}{(1+\lambda V_{DD})}\frac{V_{DD}}{I_{DSAT}}$$

$$\text{with } I_{DSAT} = k'\frac{W}{L}\left(V_{DD} - V_T - \frac{V_{DS,eff}}{2}\right)V_{DS,eff}$$

Delay as a function of V_{DD}

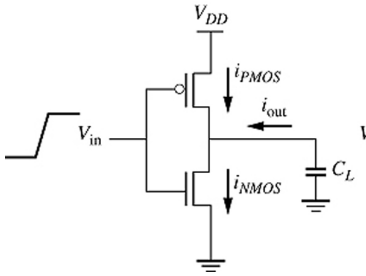


$$t_{pHL} = \frac{1}{2}\frac{C_L V_{DD}}{I_{DSAT}} = \frac{1}{2}\frac{C_L V_{DD}}{k'_n (W/L)_n \left(V_{DD} - V_{Tn} - V_{DS,eff}/2\right)V_{DS,eff}}$$

Step Inputs?

- Derived RC model assuming input was a step
  - But input is not a step
  - Transistor turns on gradually
- Let's look at gate switching more carefully
  - Use our models to understand the effect of input slope

Input Slope Dependence



$$I_{out} = C_L \frac{dV_{out}}{dt} = I_{NMOS} - I_{PMOS}$$

- One way to analyze slope effect
  - Plug non-linear IV into diff. equation and solve…
- Simpler, approximate solution:
  - Use V_T* model

Slope Analysis

- For falling edge at output:
  - For reasonable inputs, can ignore I_{PMOS}
  - Either V_{ds} is very small, or V_{gs} is very small
- So, output current ramp starts when $V_{in}=V_T^*$
  - Could evaluate the integral
  - Learn more by using an intuitive, graphical approach

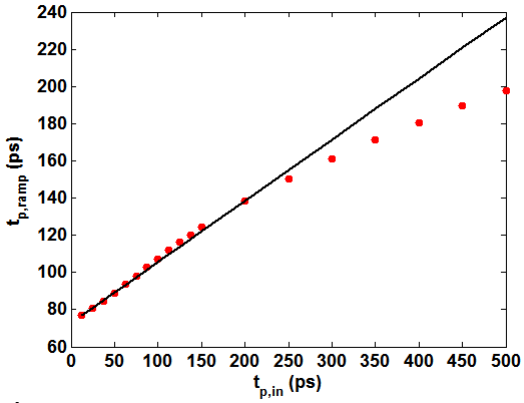
Result Summary

- For reasonable input slopes:

$$t_{p,ramp} = t_{p,step} + \frac{V_T^*}{V_{DD}} \cdot t_{p,in}$$

Model vs. Spice Data

- For reasonable input slope
  - Model matches Spice very well
- Model breaks with very large t_r
  - Input looks "DC" – traces out VTC
  - Have other problems here anyways
    - Short-circuit current

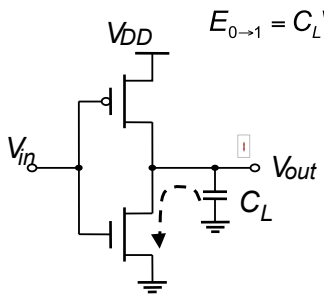


CMOS Power Dissipation

Where Does Power Go in CMOS?

- Switching power
  - Charging/discharging capacitors
- Leakage power
  - Transistors are imperfect switches
- Short-circuit power
  - Both pull-up and pull-down on during transition
- Static currents
  - Biasing currents, in e.g. analog, memory

Dynamic Power Consumption



$$E_{0\to1} = C_L V_{DD}^2$$

$$E_R = \frac{1}{2} C_L V_{DD}^2$$

$$E_C = \frac{1}{2} C_L V_{DD}^2$$

- One half of the energy from the supply is consumed in the pull-up network, one half is stored on C_L
- Energy from C_L is dumped during the 1→0 transition

Dynamic Power Consumption

Power = Energy/transition • Transition rate

$$= C_L V_{DD}^2 \bullet f_{0\to1}$$

$$= C_L V_{DD}^2 \bullet f \bullet \alpha_{0\to1}$$

$$= C_{switched} V_{DD}^2 \bullet f$$

- Power dissipation is data dependent – depends on the switching probability
- Switched capacitance $C_{switched} = C_L \bullet \alpha_{0\to1}$

Transition Activity and Power

- Energy consumed in N cycles, E_N:

$$E_N = C_L \bullet V_{DD}^2 \bullet n_{0\to1}$$

$n_{0\to1}$ – number of 0→1 transitions in N cycles

$$P_{avg} = \lim_{N\to\infty} \frac{E_N}{N} \cdot f = \left(\lim_{N\to\infty} \frac{n_{0\to1}}{N} \right) \cdot C_L \cdot V_{DD}^2 \cdot f$$

$$\alpha_{0\to1} = \lim_{N\to\infty} \frac{n_{0\to1}}{N}$$

$$\boxed{P_{avg} = \alpha_{0\to1} \cdot C_L \cdot V_{DD}^2 \cdot f}$$