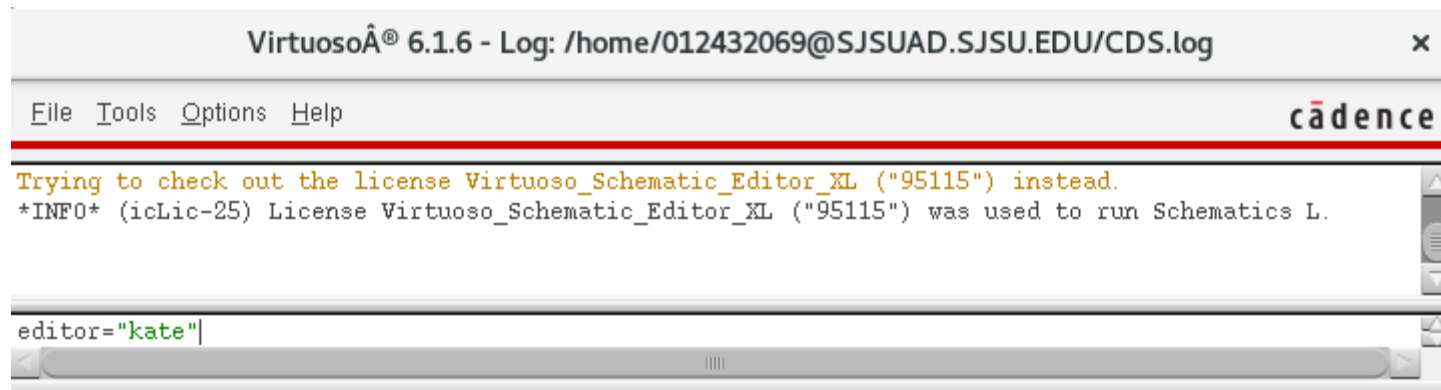


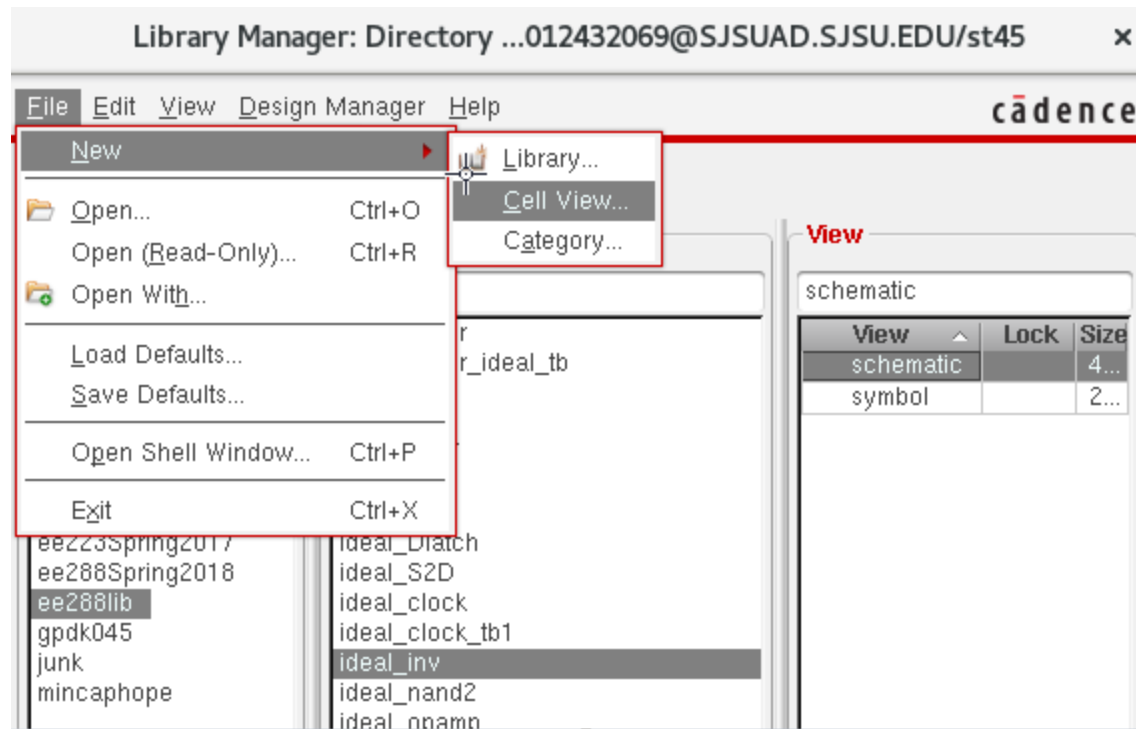
# Creating Veriloga View

- In CIW window, type  
editor="kate"



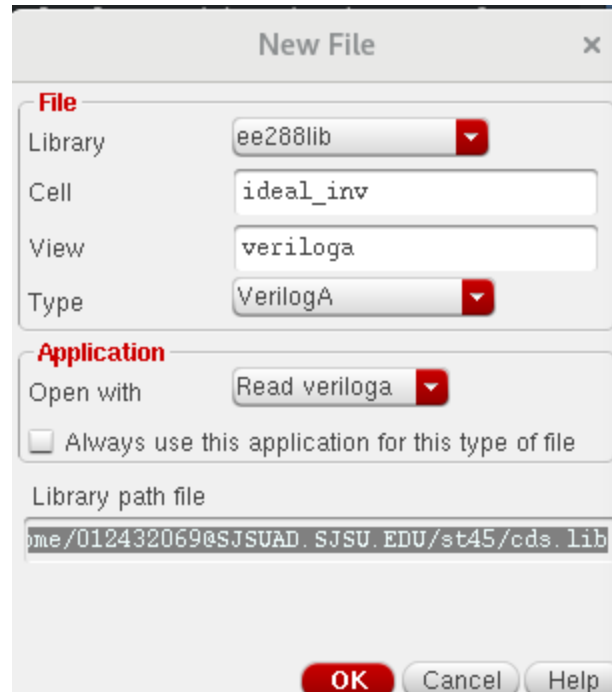
# Creating Veriloga View

- From Library Manager, File->New->Cell View



# Creating Veriloga View

- Fill out the form like this



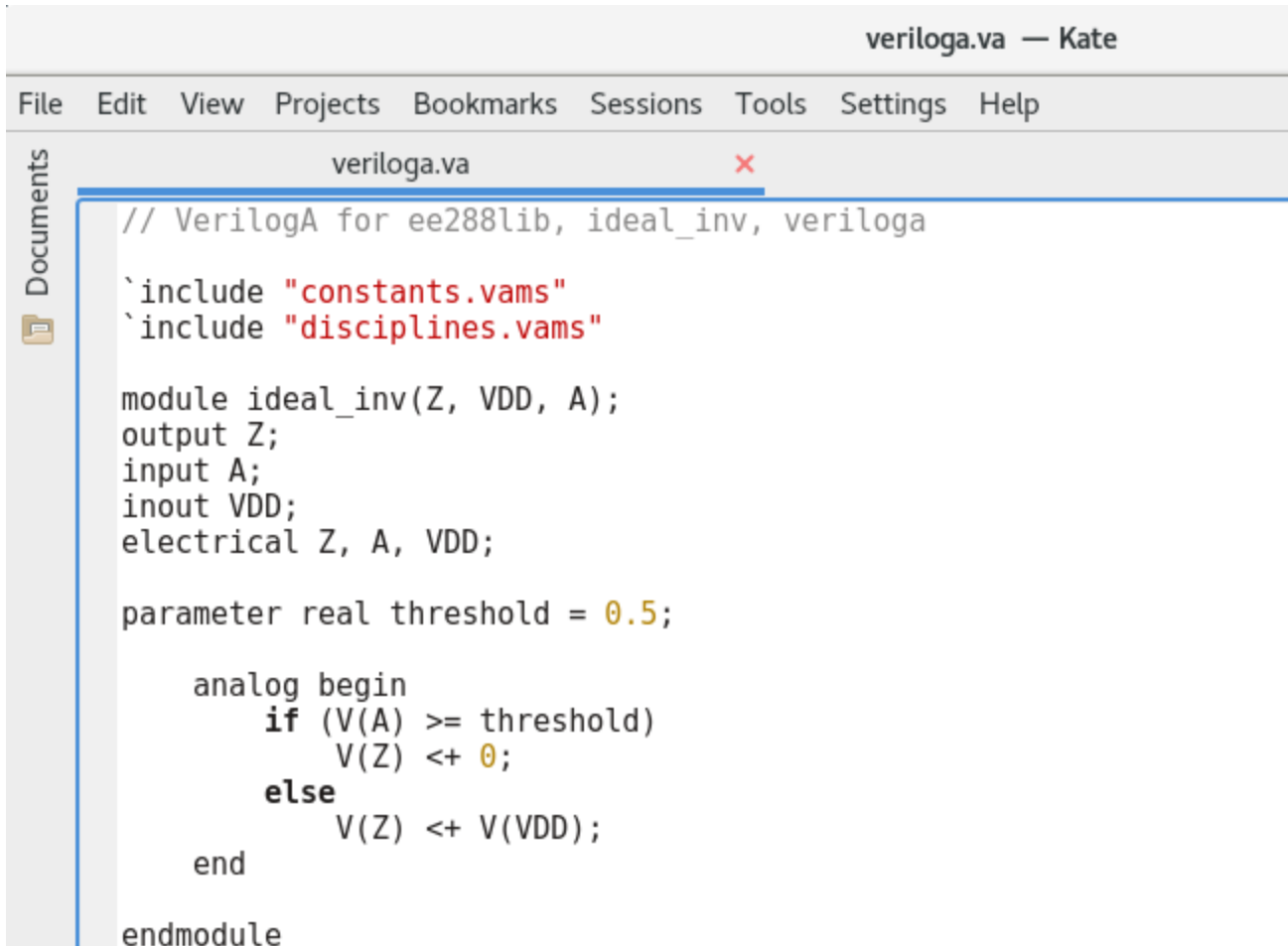
The screenshot shows a 'New File' dialog box with the following fields and values:

- File**
  - Library: ee288lib
  - Cell: ideal\_inv
  - View: veriloga
  - Type: VerilogA
- Application**
  - Open with: Read veriloga
  - ☐ Always use this application for this type of file
- Library path file: /me/012432069@SJSUAD.SJSU.EDU/st45/cds.lib

Buttons at the bottom: OK, Cancel, Help.

# Creating Veriloga View

- In the editor, write a code like below example



```
veriloga.va — Kate
File Edit View Projects Bookmarks Sessions Tools Settings Help
Documents
veriloga.va
// VerilogA for ee288lib, ideal_inv, veriloga
`include "constants.vams"
`include "disciplines.vams"

module ideal_inv(Z, VDD, A);
output Z;
input A;
inout VDD;
electrical Z, A, VDD;

parameter real threshold = 0.5;

    analog begin
        if (V(A) >= threshold)
            V(Z) <+ 0;
        else
            V(Z) <+ V(VDD);
    end
endmodule
```

# Running Simulation Using Verilog View

- Check the following test bench “ideal\_inv\_tb1” in ee288lib

The screenshot displays the Cadence ADE L Editing interface. The main window shows a schematic of an ideal inverter circuit. The circuit includes a VDD supply, a ground connection, and an ideal inverter component labeled 'ideal\_inv'. The input of the inverter is connected to a signal source 'v1' with a value of 'vdc=VDD'. The output of the inverter is connected to a signal source 'v0' with a value of 'v1:0' and a delay of 'tr=10p'. The output of the inverter is also connected to a signal source 'v2' with a value of 'VDD'. The output of the inverter is labeled 'out'.

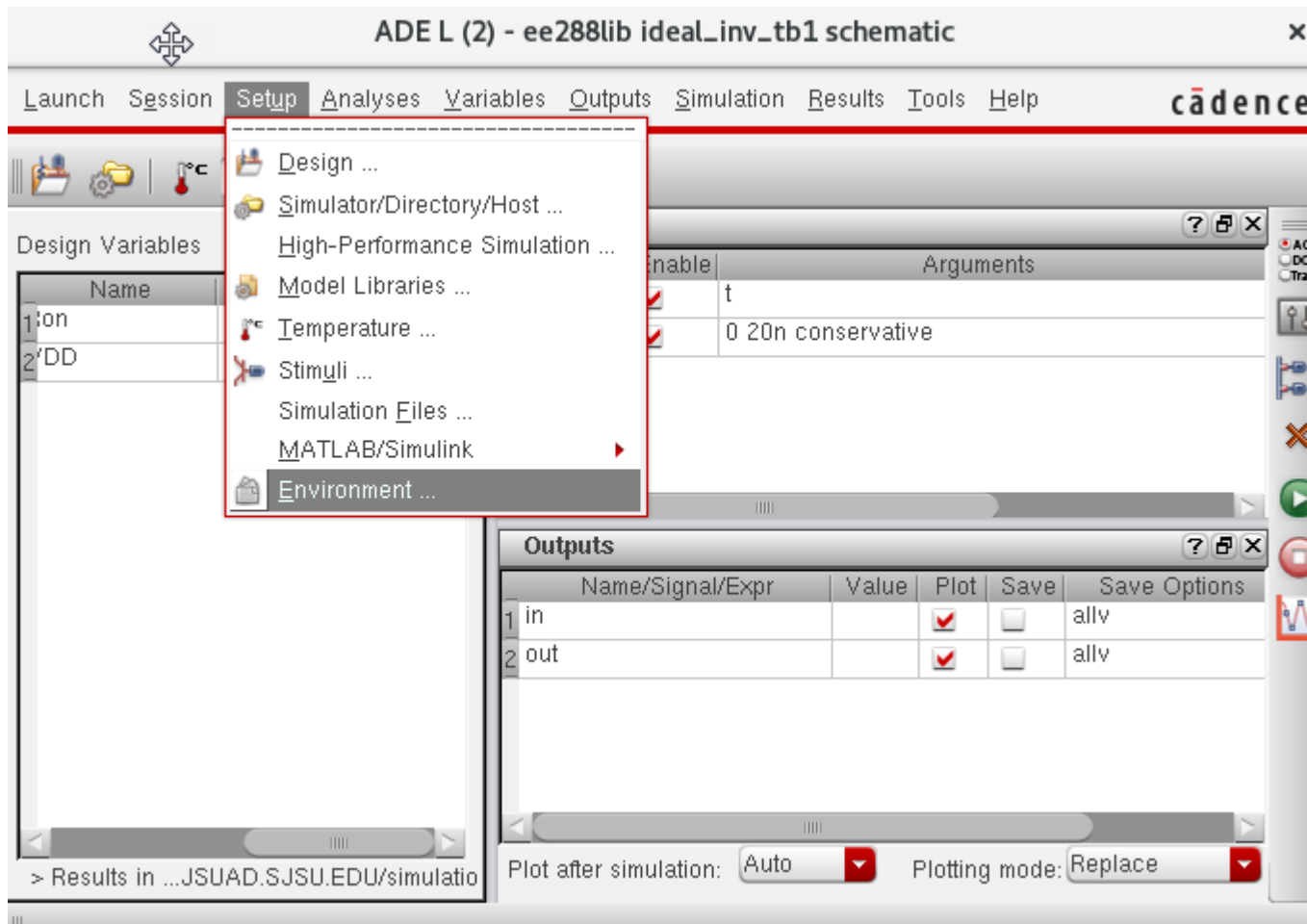
The Library Manager window on the right shows the 'ee288lib' library. The 'Cell' list includes 'ideal\_inv' and 'ideal\_inv\_tb1'. The 'View' list shows 'schematic' and 'symbol'.

The Messages window at the bottom shows the following text:

```
Processing files to be copied...
Renaming Cell "ideal_inv_tb1" to "ideal_inva_tb1" in library "ee288lib".
Deleting view "schematic" from cell "ideal_inva" in library "ee288lib".
Deleted cellview 'ee288lib/ideal_inva/schematic'. Deletion of 1 view done.
Beginning simple copy to library "ee288lib".
Processing files to be copied...
```

# Running Simulation Using Verilog View

- In ADL L window, choose Setup->Environment



# Running Simulation Using Verilog View

- Rearrange the Switch View List so that verilog comes before schematic -> verilog view will be used in simulation

