EE230-02 RFIC II
Fall 2018

Lecture 1: RFIC Introduction

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ENG-259

Why RFIC?
Where do we use RF circuits?
How big is the market?

Semiconductor Market

Largest IC Product Categories, 2018F

Rank	Market	$B
1	DRAM	$101,620
2	NAND Flash	$62,604
3	Std PC, Server MPU	$50,782
4	Computer and Periph—Spcl Purp Logic	$27,619
5	Wireless Comm—Spcl Purp Logic	$25,998
Rank	**Shipments**	**Units, M**
1	Power Management Analog	71,192
2	Wireless Comm—App Specific Analog	23,376
3	General Purpose Logic	21,675
4	Industrial—App Specific Analog	18,924
5	Automotive—App Specific Analog	15,969

Source: IC Insights

Semiconductor Sales Leaders

1H18 Top-15 Semiconductor Sales Leaders ($M, Including Foundries)

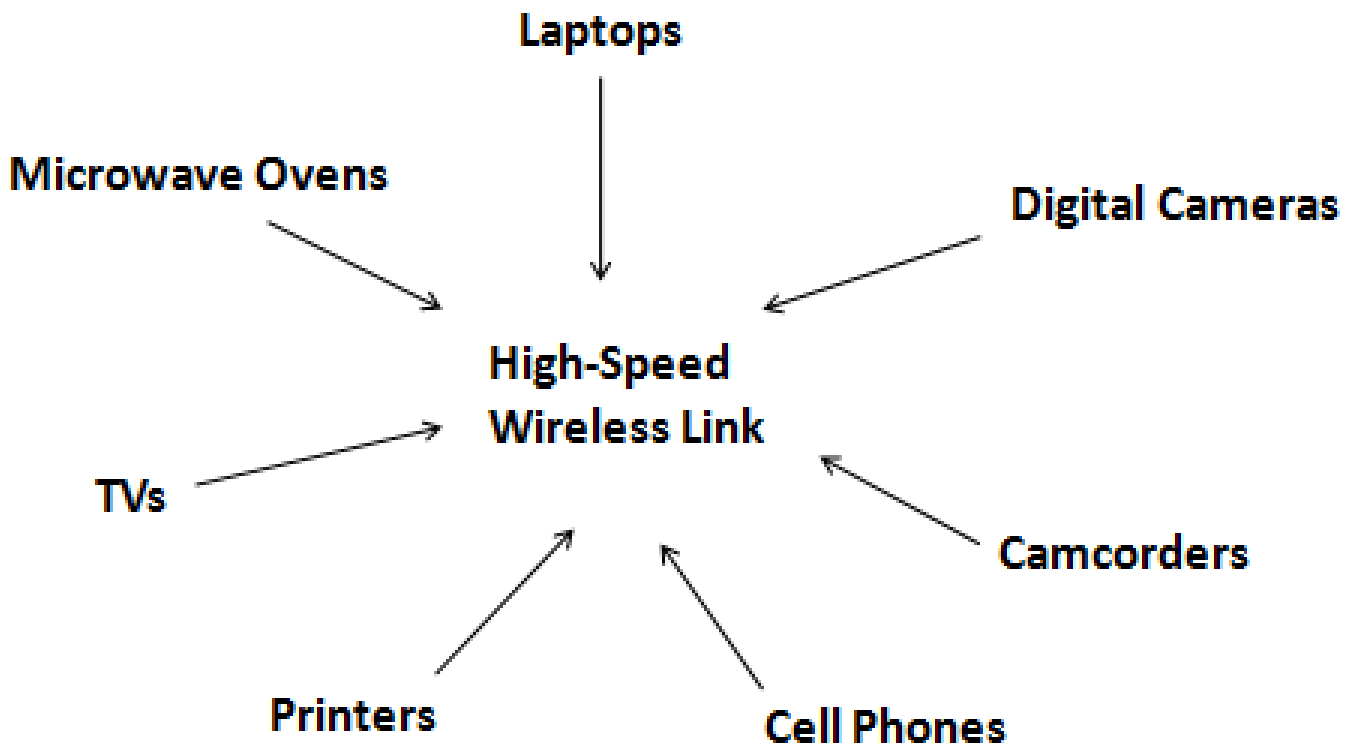
1H18 Rank	2017 Rank	Company	Headquarters	1Q18 Tot IC	1Q18 Tot O-S-D	1Q18 Tot Semi	2Q18 Tot IC	2Q18 Tot O-S-D	2Q18 Tot Semi	2Q18/1Q18 % Change	1H18 Tot Semi	1H17 Tot Semi	1H18/1H17 % Change
1	1	Samsung	South Korea	18,491	910	19,401	19,434	950	20,384	5%	39,785	29,181	36%
2	2	Intel	U.S.	15,832	0	15,832	16,753	0	16,753	6%	32,585	28,839	13%
3	4	SK Hynix	South Korea	8,016	125	8,141	9,421	192	9,613	18%	17,754	11,393	56%
4	3	TSMC (1)	Taiwan	8,473	0	8,473	7,839	0	7,839	-7%	16,312	14,601	12%
5	5	Micron	U.S.	7,486	0	7,486	7,920	0	7,920	6%	15,406	10,653	45%
6	6	Broadcom Ltd. (2)	U.S.	4,125	434	4,559	4,150	435	4,585	1%	9,144	8,404	9%
7	7	Qualcomm (2)	U.S.	3,897	0	3,897	4,087	0	4,087	5%	7,984	7,728	3%
8	9	Toshiba/Toshiba Memory	Japan	3,517	310	3,827	3,575	315	3,890	2%	7,717	6,159	25%
9	8	TI	U.S.	3,339	227	3,566	3,535	245	3,780	6%	7,346	6,595	11%
10	10	Nvidia (2)	U.S.	3,108	0	3,108	3,135	0	3,135	1%	6,243	4,083	53%
11	15	WD/SanDisk	U.S.	2,350	0	2,350	2,375	0	2,375	1%	4,725	3,715	27%
12	13	Infineon	Europe	1,360	907	2,267	1,388	926	2,314	2%	4,581	3,896	18%
13	11	NXP	Europe	2,017	252	2,269	2,035	255	2,290	1%	4,559	4,413	3%
14	12	ST	Europe	1,696	518	2,214	1,724	526	2,250	2%	4,464	3,732	20%
15	16	MediaTek (2)	Taiwan	1,696	0	1,696	2,032	0	2,032	20%	3,728	3,726	0%
—	—	Top-15 Total		85,403	3,683	89,086	89,403	3,844	93,247	4.7%	182,333	147,118	24%

(1) Foundry (2) Fabless

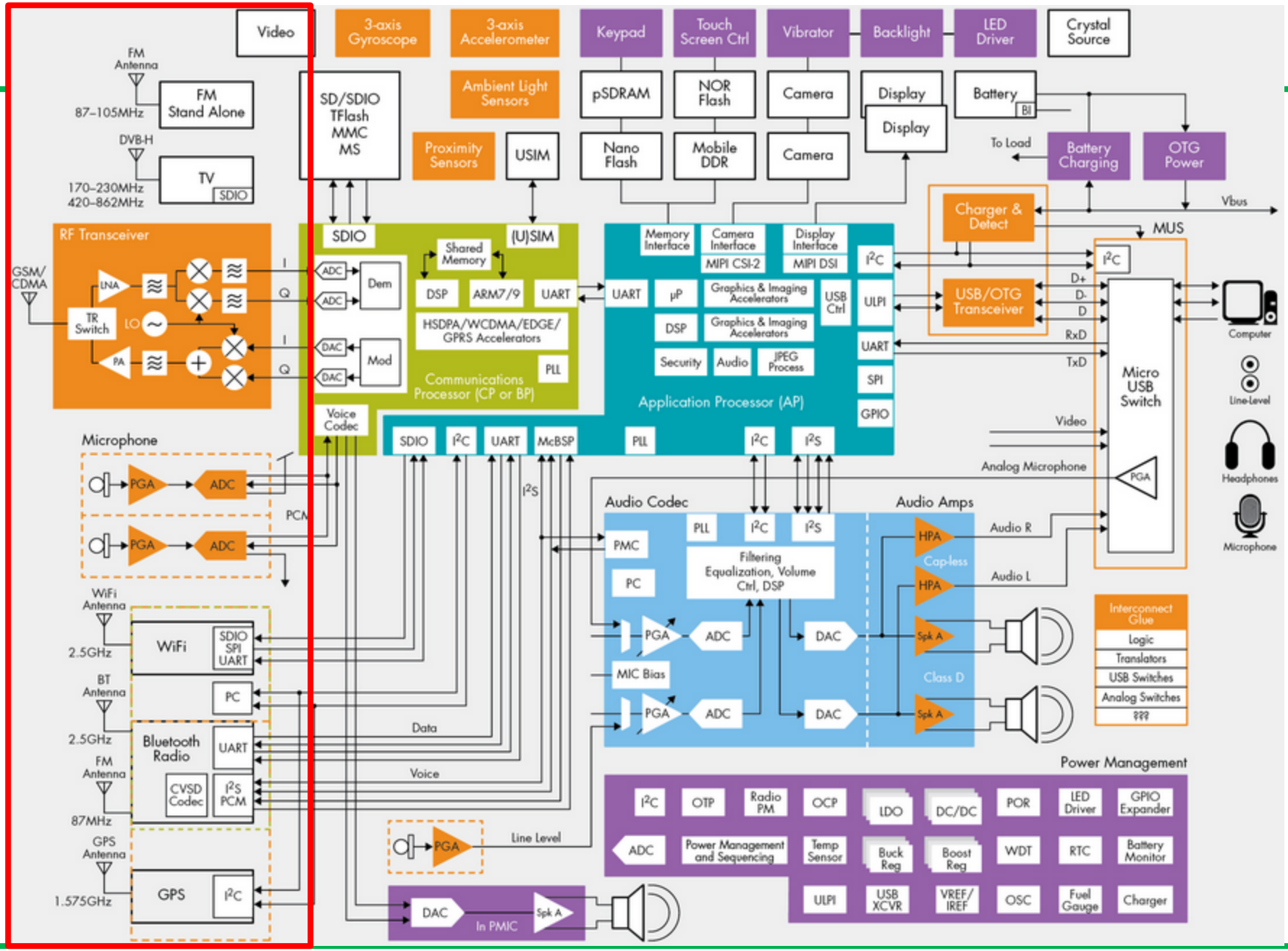
Source: Company reports, IC Insights' *Strategic Reviews* database

*Custom devices for internal use.

Wireless World Everywhere



Smartphones


Video
3-axis Gyroscope
3-axis Accelerometer
Keypad
Touch Screen Ctrl
Vibrator
Backlight
LED Driver
Crystal Source
FM Antenna
87–105MHz
FM Stand Alone
DVB-H
170–230MHz
420–862MHz
TV
SDIO
SD/SDIO TFlash MMC MS
Ambient Light Sensors
pSDRAM
NOR Flash
Camera
Display
Battery
BI
Proximity Sensors
USIM
Nano Flash
Mobile DDR
Camera
Display
To Load
Battery Charging
OTG Power
Vbus
Charger & Detect
MUS
RF Transceiver
GSM/CDMA
LNA
TR Switch
LO
PA
I
Q
SDIO
(U)SIM
Shared Memory
ADC
Dem
DSP
ARM7/9
UART
HSDPA/WCDMA/EDGE/ GPRS Accelerators
PLL
Communications Processor (CP or BP)
Memory Interface
Camera Interface
MIPI CSI-2
Display Interface
MIPI DSI
I²C
UART
µP
Graphics & Imaging Accelerators
USB Ctrl
ULPI
DSP
Graphics & Imaging Accelerators
Security
Audio
JPEG Process
UART
SPI
GPIO
Application Processor (AP)
USB/OTG Transceiver
D+
D-
D
RxD
TxD
Computer
Micro USB Switch
Line-Level
Headphones
Microphone
Video
Analog Microphone
PGA
DAC
Mod
Voice Codec
SDIO
I²C
UART
McBSP
PLL
I²C
I²S
Microphone
PGA
ADC
PCM
I²S
Audio Codec
Audio Amps
PLL
I²C
I²S
PMC
PC
Filtering Equalization, Volume Ctrl, DSP
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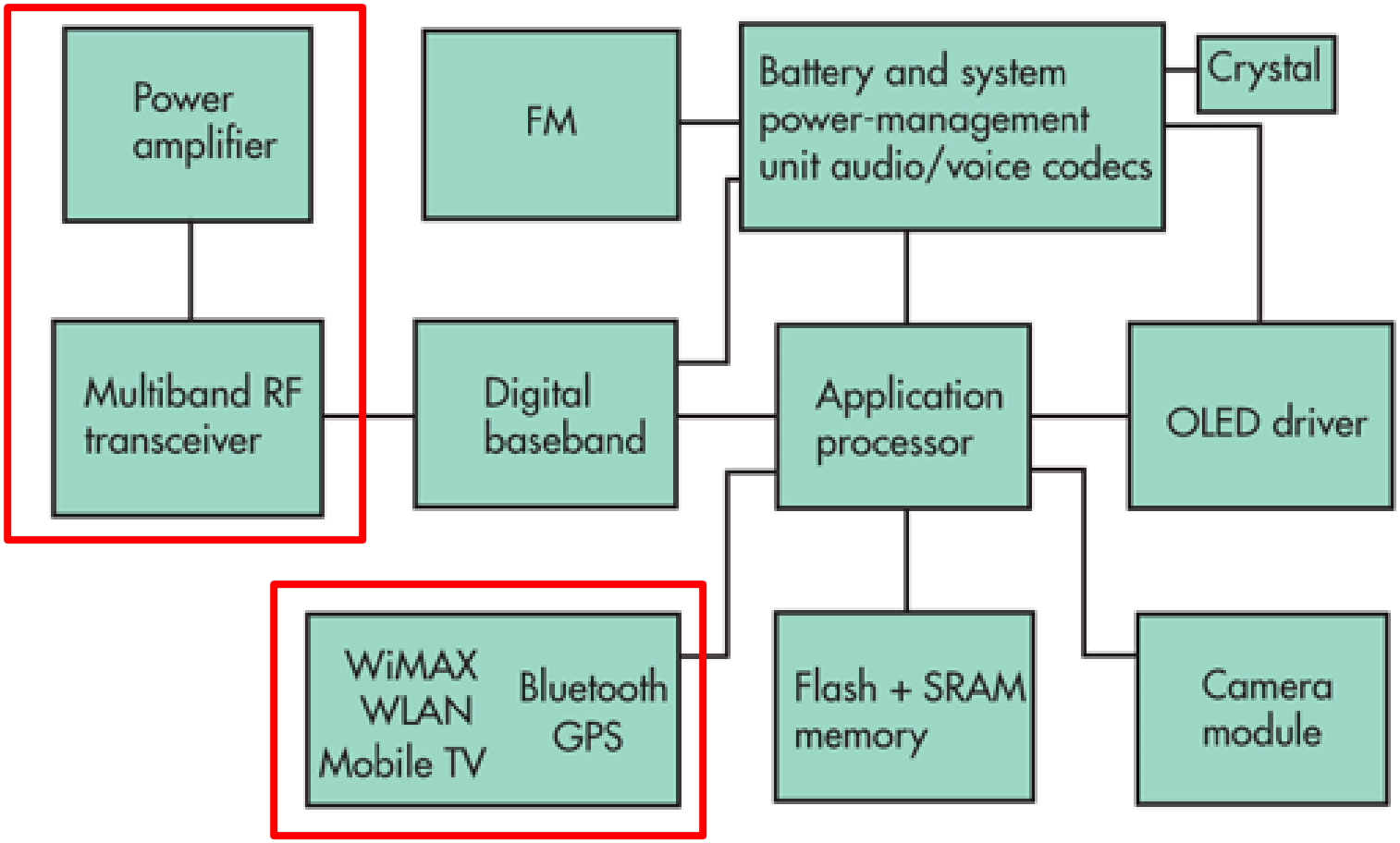
Cap-less
HPA
Audio R
Audio L
PGA
ADC
DAC
Spk A
MIC Bias
PGA
ADC
DAC
Spk A
Class D
Interconnect Glue
Logic
Translators
USB Switches
Analog Switches
???
WiFi Antenna
2.5GHz
WiFi
SDIO SPI UART
BT Antenna
2.5GHz
PC
Bluetooth Radio
UART
FM Antenna
87MHz
CVSD Codec
I²S PCM
Data
Voice
GPS Antenna
1.575GHz
GPS
I²C
PGA
Line Level
DAC
Spk A
In PMIC
Power Management
I²C
OTP
Radio PM
OCP
LDO
DC/DC
POR
LED Driver
GPIO Expander
ADC
Power Management and Sequencing
Temp Sensor
Buck Reg
Boost Reg
WDT
RTC
Battery Monitor
ULPI
USB XCVR
VREF/ IREF
OSC
Fuel Gauge
Charger

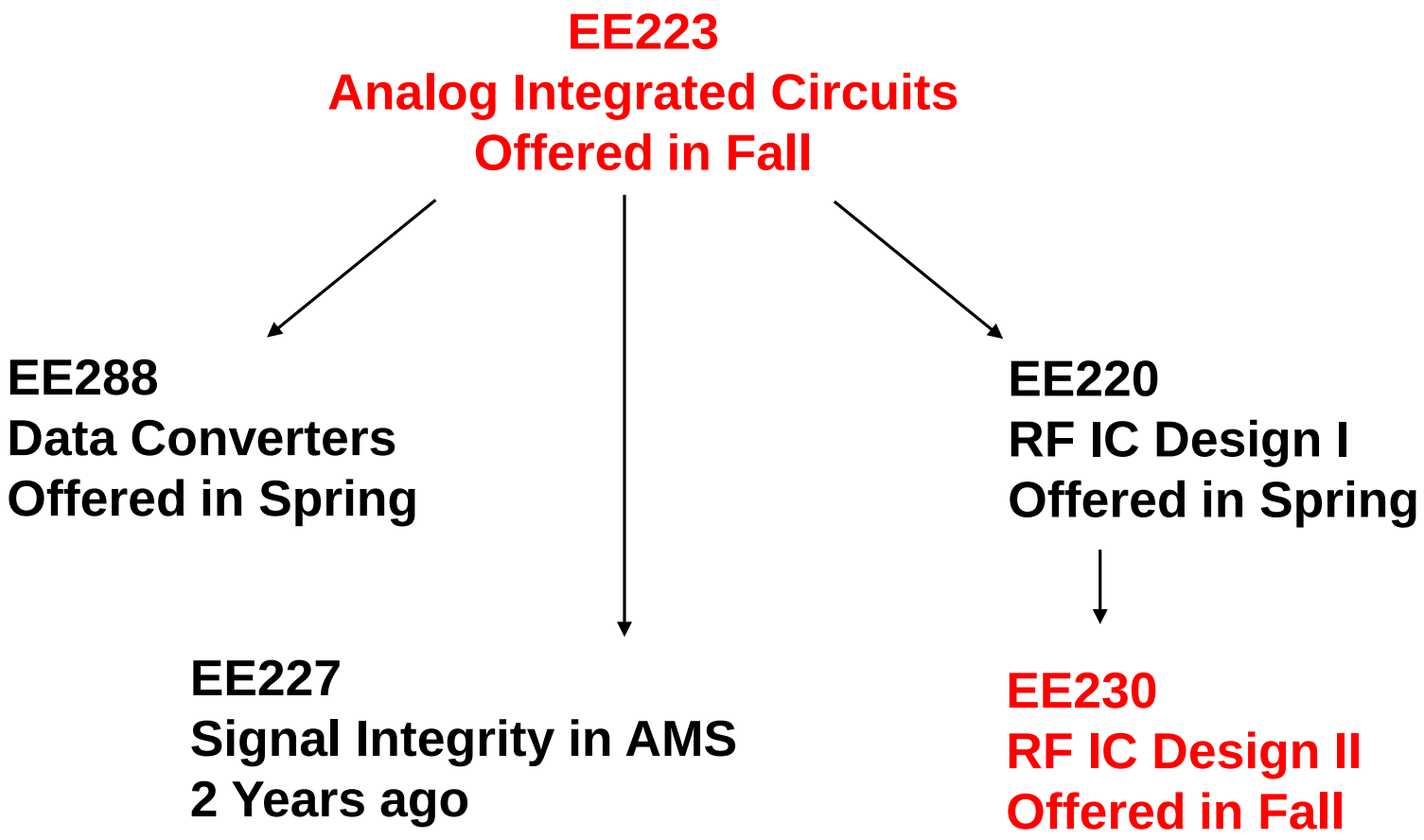
Smartphone Block Diagram



Course Information

Instructor:	Sang-Soo Lee, PhD Carnegie Mellon University	
Time:	Class : Tuesday, Thursday 4:30 – 5:45 pm	
	Office Hour : Tuesday, Thursday 5:50 – 6:50 pm	
	Other time by appointment	
Lab ISA:	TBD	user@sjsu.edu
Lab Time:	TBD	TBD

Analog Course Sequence at SJSU



Prerequisite

- Familiarity with basic electrical engineering concepts
  - Ohm’s Law : V = I x R, Power, KCL & KVL
  - Trigonometric functions, sine, cosine, etc.
  - Time-domain and Frequency-domain
  - Familiar with Filtering
  - A/D Converter and D/A Converter
  - Semiconductor Physics

- EE220 or equivalent

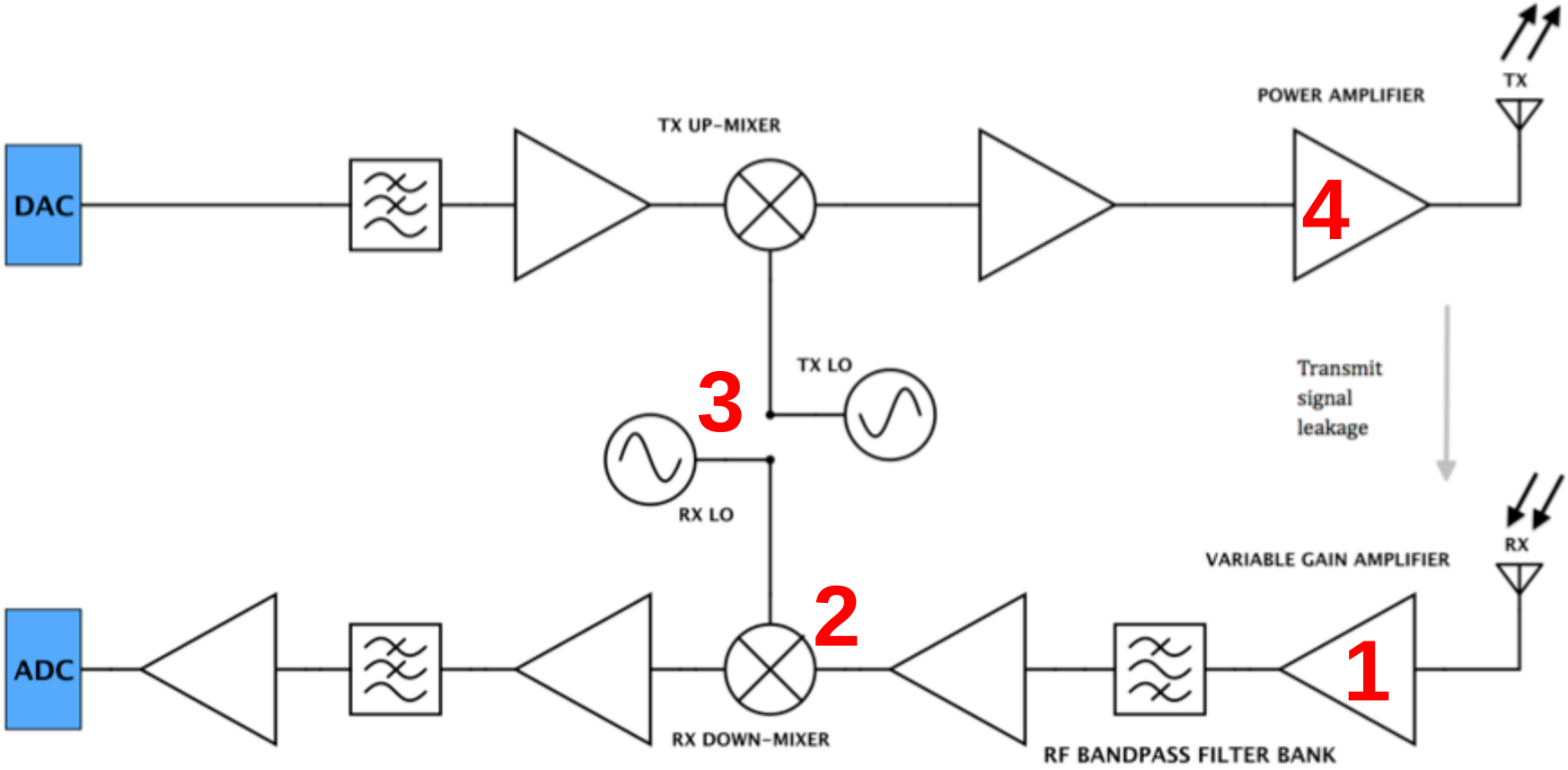
Course References

1. Lecture Notes
2. B. Razavi, RF Microelectronics, 2nd Edition, Upper Saddle River, New Jersey, Prentice Hall, 2012
3. T. H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge, U.K., Cambridge University Press, 2004.
4. Selected publications from
   - Journal of Solid-State Circuits (JSSC)
   - Transactions on Microwave Theory and Techniques (MTT)
   - International Solid-State Circuits Conference (ISSCC)
   - Custom Integrated Circuits Conference (CICC)

   Papers can be downloaded from IEEE Xplore website.

Topics to be covered

Focus on learning key building blocks used in every RF Transceiver.



Quiz on RF Basic

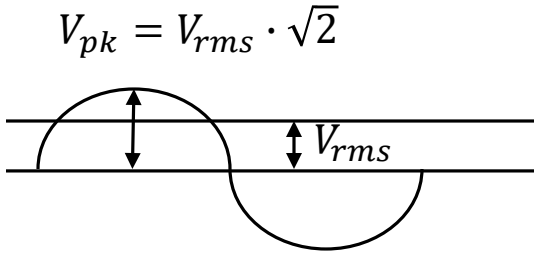
Calculate the peak-to-peak voltage swing for 0 dBm signal in 50-ohm system.

$0\ dBm \leftrightarrow 1mW$

$$Power = \frac{{V_{rms}}^2}{R} = \frac{{V_{rms}}^2}{50} = 0.001$$

$$V_{rms} = \sqrt{0.05} = 0.224$$

$$V_{pk-pk} = 2(0.224\ \cdot \sqrt{2}) = 0.632V$$

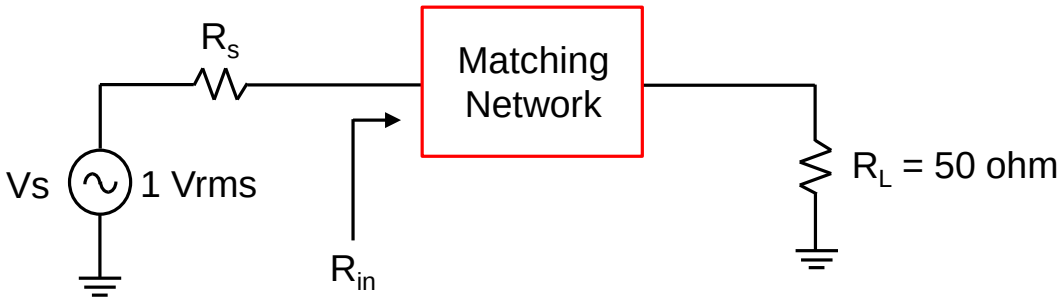


Quiz on RF Basic

The RF amplifier shown below produces Vs = 1 Vrms signal with a source resistance of Rs.
We want to deliver 1 Watt of average power to an antenna with 50-ohm load for GSM 1.8GHz application.

1. What should be the value of Rs when a matching network is inserted to ensure Rin = Rs for maximum power transfer at the frequency of interest?

2. Suggest a circuit you have to put in the matching network shown below.



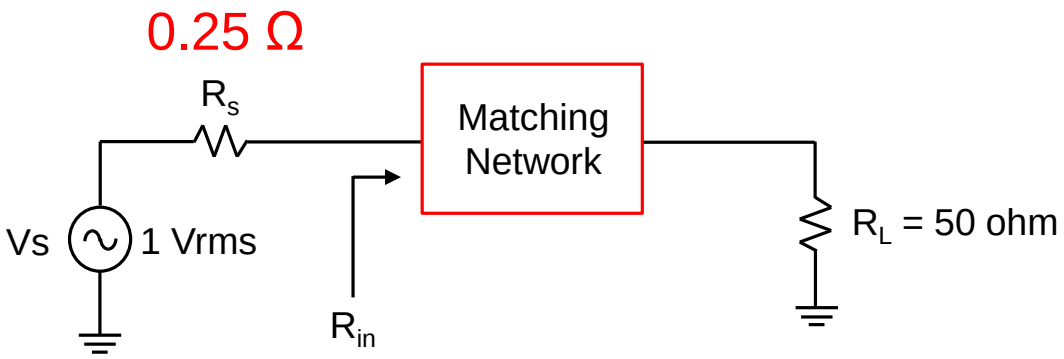
Quiz Solution

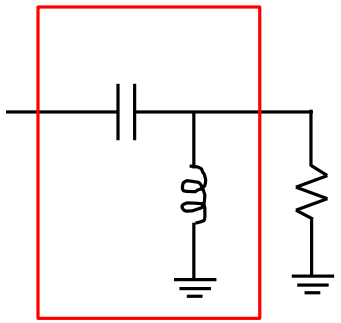
The RF amplifier shown below produces Vs = 1 Vrms signal with a source resistance of Rs.
We want to deliver 1 Watt of average power to an antenna with 50-ohm load for GSM 1.8GHz application.

1. What should be the value of Rs when a matching network is inserted to ensure Rin = Rs for maximum power transfer at the frequency of interest?

2. Suggest a circuit you have to put in the matching network shown below.

$$Power = \frac{{V_{rms}}^2}{R_s} = \frac{0.5^2}{R_s} = 1 \quad \Longrightarrow \quad R_s = 0.5^2 = 0.25$$



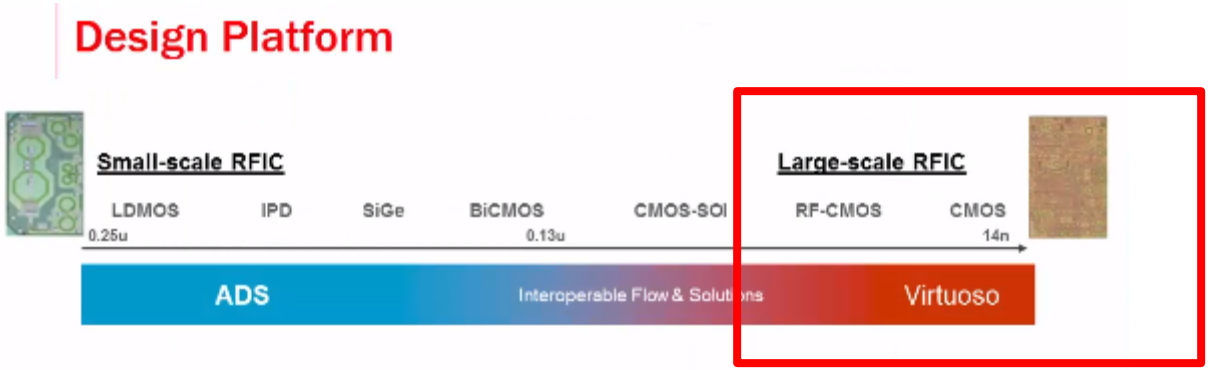


Technology to be used in the course

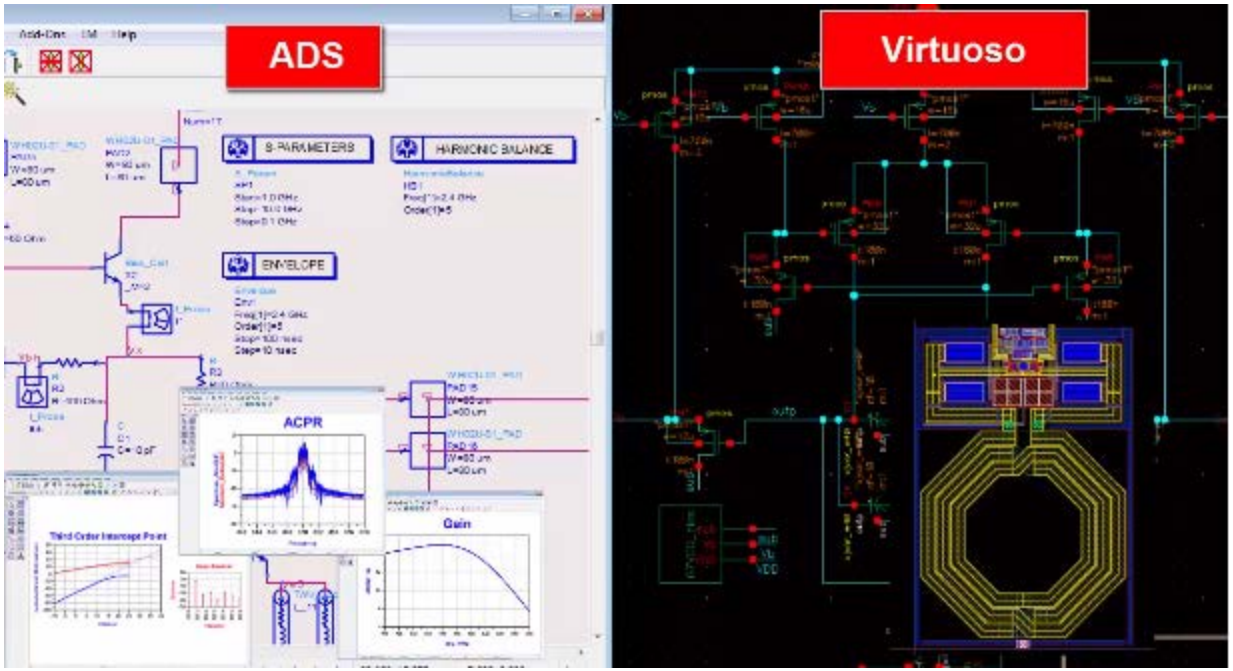
RF CMOS process

Design Tools to be used in the course

Cadence Virtuoso SpectreRF



ADS vs. Virtuoso



Cadence Spectre

- Homework and project will use Cadence Spectre simulation.
- Device models are from g045pdk.

- For Cadence related information,

  See the files in the following link

https://drive.google.com/open?id=1Jr0l9xn0Q2XQ9hzQKrLPH1I0xZhwuTg1

  You have to use sjsu email address to access the files.

- TA Lab hours : TBD

- Additional Cadence Spectre Tutorials
  - If you have no experience in Cadence, please check Youtube videos such as
  - https://www.youtube.com/watch?v=u0WgSMa1hrc&list=PLK2eyR1C9gjr7j-YoL_-JwJmjU6lNZGTO

Grading Policy

Grading Basis

- Homework 30%
- Project 20%
- Midterm 25%
- Final Exam 25%

- Exams will be closed book
- No make-up exam

Grading Percentage

- 90% and above A
- 89% - 85% A-
- 84% - 82% B+
- 81% - 79% B
- 78% - 75% B-
- 74% - 72% C+
- 71% - 69% C
- 68% - 65% C-
- 64% - 62% D+
- 61% - 59% D
- 58% - 55% D
- below 55% F

Homework Problems

All homework problems should be done individually
and submitted by 4 PM on the due date.

Submission: Email to sang-soo.lee@sjsu.edu
File name convention: EE230HW#1_your_name

You will design the following circuits using Cadence Spectre or write a report on the summary of the paper for each block.

- HW#1 (10%) – LNA
- HW#2 (10%) – Mixer
- HW#3 (10%) – Oscillator

Course Project

PLL (20%)

Group (maximum 2 students) project

Detailed project description will be posted after Midterm exam.

Schedule subject to change with advanced notice

Midterm Around 10/16

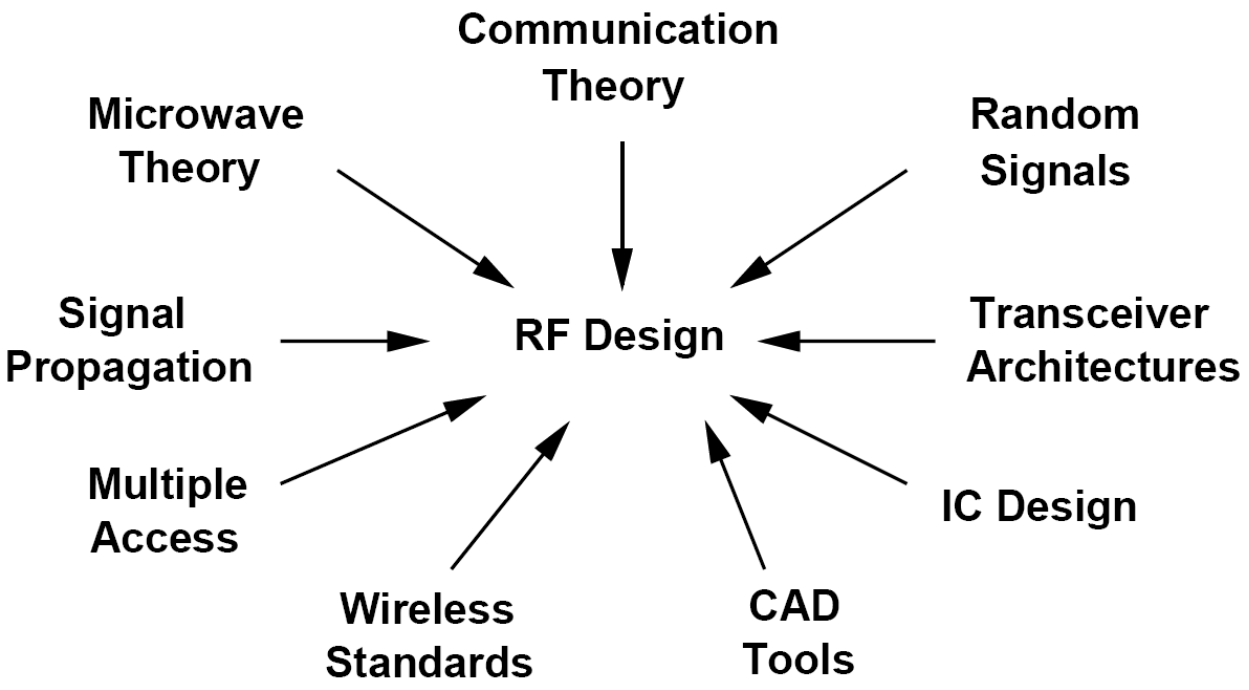
Final 12/14

Lecture #	Topics	Book reading
1	RFIC Introduction I	Chapter 1, 2.2
2	RFIC Introduction II	Chapter 2.3-2.5
3	Wireless Receiver Architecture - I	Chapter 4.2.1
4	Wireless Receiver Architecture - II	Chapter 4.2.3
5	LNA General Considerations and Input Matching	Chapter 5.1-5.2
6	Common-Source LNA	Chapter 5.3.1-2
7	Common-Gate LNA (**HW#1 handout, 10% grade**)	Chapter 5.3.3
8	Cascode Common-Source LNA with Inductive Degeneration	Chapter 5.3.4
9	Variants of Common-Gate LNA	Chapter 5.3.5
10	Wireless Transmitter Architecture - I	Chapter 4.3
11	Wireless Transmitter Architecture - II	Chapter 4.4
12	Mixer – General Considerations	Chapter 6.1
13	Passive Down Conversion Mixers	Chapter 6.2
14	Active Down Conversion Mixers (**HW#2 handout, 10% grade**)	Chapter 6.3
15	Active Mixers with High IP2	Chapter 6.4
16	Active Up Conversion Mixers	Chapter 6.5
17	***Midterm Exam, 75 minutes, 25% grade***	
18	Oscillators – Basic Principles	Chapter 8.1-8.2
19	Cross coupled Oscillators	Chapter 8.3
20	Voltage Controlled Oscillators	Chapter 8.5
21	Low-noise VCOs (**HW#3 handout, 10% grade**)	Chapter 8.6
22	Phase-locked loops (PLL) basic concepts	Chapter 9.1
23	Type-I PLLs	Chapter 9.2
24	Type-II PLLs	Chapter 9.3
25	PFD and Charge Pump Nonidealities	Chapter 9.4
26	PLL modeling and stability	Lecture Note
27	Project Presentation - Group 1-5	
28	Project Presentation - Group 6-10	
29	Project Presentation - Group 11-15	
30	Review for Final Exam	
Final Exam	***Dec. 14, Friday, from 2:45PM — 5:00PM, 25% grade***	

Lecture Style

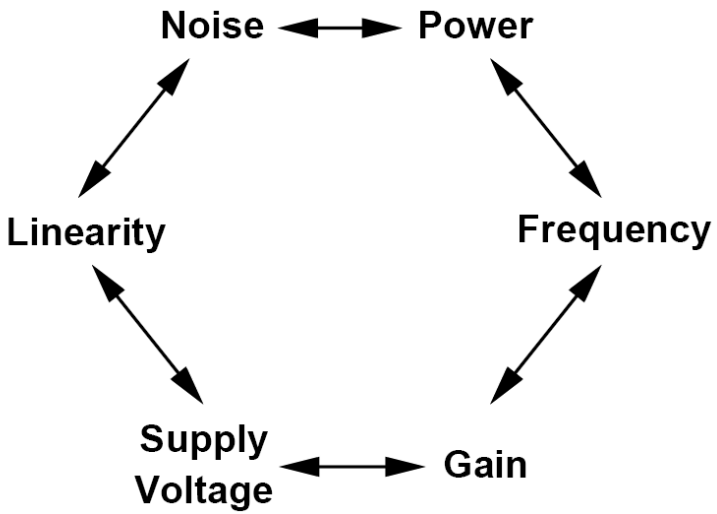
- Class room lecture – most of the time
- Online lecture – when I am traveling
  - Use Zoom Online Meeting
- Guest lecture
  - If I can make find one
- Reading materials
  - If I cannot make it any of the above

Challenges of RFIC Design 1



- **Require understanding multitude disciplines**

Challenges of RFIC Design 2

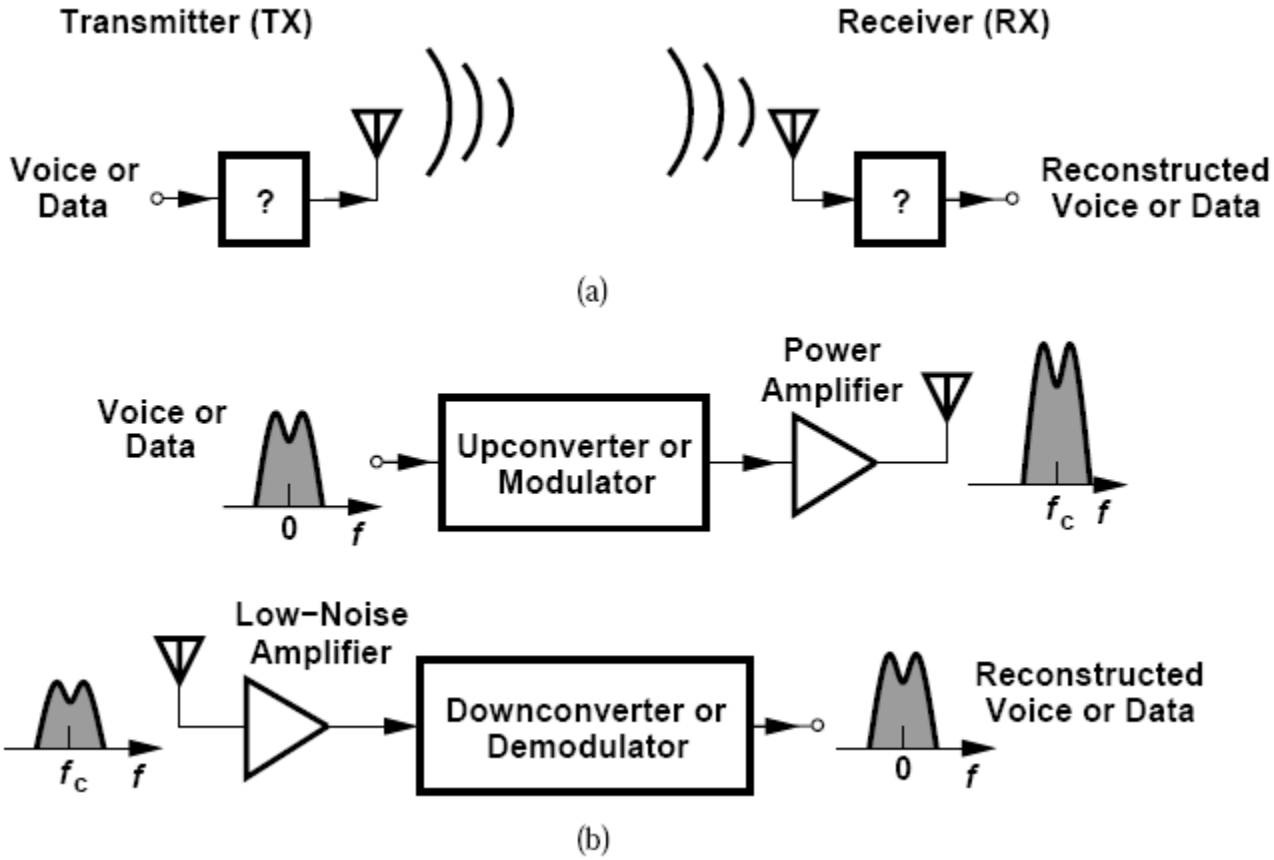


- **Require numerous Trade-offs**

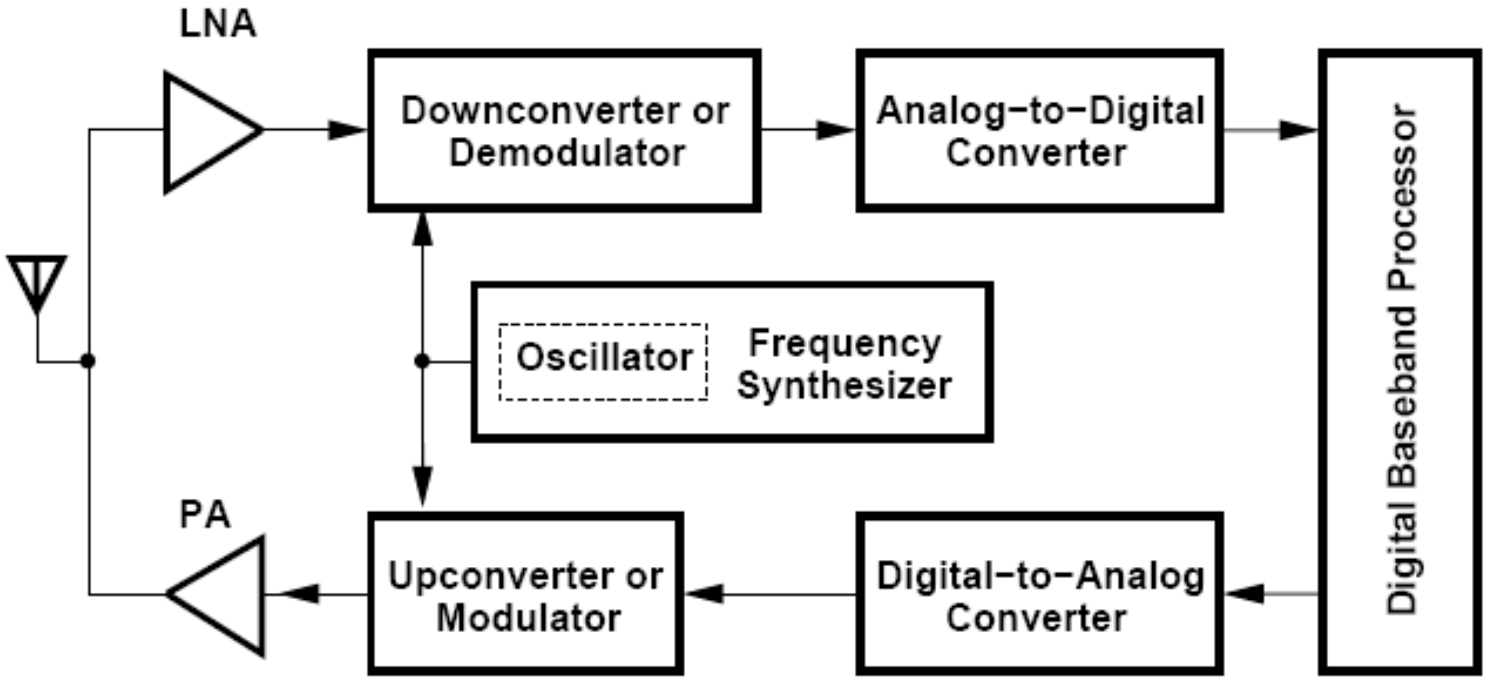
Big Picture of RF Communications

TX: Drive antenna with high power level

RX: Sense small signal (amplify with low noise)



Block Diagram Representation



- **Signals are upconverted/downconverted at TX/RX, by an oscillator controlled by a Frequency Synthesizer**

How to send data without wire?