UNIVERSITY OF CALIFORNIA, BERKELEY

College of Engineering

Department of Electrical Engineering and Computer Sciences

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Due Friday, April 30, 5pm, box in 240 Cory

[PROBLEM 1] GENERAL SCALING (30pts)

(a) **(5pts)** A company has implemented a single-core microprocessor in 90nm technology with 300mV threshold voltages, that operates at 3.8GHz with a 1.2V supply, a 100W power dissipation, and a die area of 200mm^2. They would like to build a dual core microprocessor in the same technology, by duplicating the single core design. What frequency and supply voltage should be for the dual core design to maintain the same size of the heat sink, i.e. $P_{DUAL} = P_{SINGLE}$? You can assume that the frequency of operation is roughly linearly proportional to the supply voltage in this technology, i.e. $f \propto V_{DD}$.

$P \propto C*V_{DD}^2*f \rightarrow P \propto C*V_{DD}^3$
$P_{DUAL} / P_{SINGLE} = C_{DUAL}*V_{DD,DUAL}^3 / C_{SINGLE}*V_{DD,SINGLE}^3 = 1$
$V_{DD,DUAL}^3 / V_{DD,SINGLE}^3 = ½$
$V_{DD,DUAL} = 0.95V$
$f_{DUAL} / f_{SINGLE} = V_{DD,DUAL} / V_{DD,SINGLE}$
$f_{DUAL} = 3GHz$

(b) **(5pts)** If the single-core design from part (a) is fabricated with a 65nm technology with 1.0V supply, what would be its size, frequency of operation, and power? You can assume that all of the power is switching power, i.e. no static current and leakage current.

S=90nm/65nm=18/13, U=1.2/1.0=1.2
$AREA \propto 1/S^2 \rightarrow AREA_{65nm}=1/S^2*AREA_{90nm} = 104.32mm2$
$f \propto 1/tp \propto S \rightarrow f_{65nm} = S*f_{90nm} = 5.26GHz$
$P \propto 1/U^2 \rightarrow P_{65nm} = 1/U^2*P_{90nm} = 69.44W$

(c) **(5pts)** According to the scaling rules, what should be the threshold voltage in the 1.0V 65nm technology, if the 90nm from part (a) is the starting technology?

$V_{TH,65nm} = 1/U * V_{TH,90nm} = 0.25V$

(d) **(15pts)** If the total power of 100W was actually composed of 80% switching and 20% leakage in a single-core design from part (a), what would be the total power ($P_{DYNAMIC} + P_{LEAKAGE}$) of a scaled processor in 65nm technology with 1.0V supply? Assume the sub-threshold slope S=80mV/dec. The leakage current can be expressed as $I_{LEAKAGE} \propto Is*\exp(0-V_{TH}/nV_T)$ @ V_{GS}=0V where V_T is thermal voltage

(kT/q), n=1.5, and Is=4uA (VT, n, and Is are independent of scaling). You can assume that the chip operates at room temperature (300K).

$P_{DYNAMIC} \propto 1/U^2$
$P_{DYNAMIC,90nm} = 0.8 * 100W = 80W$
$\therefore P_{DYNAMIC,65nm} = 1/U^2 * P_{DYNAMIC,90nm} = 55.56W$

$P_{LEAKAGE,90nm} = 0.2 * 100W = 20W$
$I_{LEAKAGE,90nm} = P_{LEAKAGE,90nm} / V_{DD,90nm} = 20/1.2 = 16.67A$
$I_{LEAKAGE} \propto Is*\exp(-V_{TH}/nV_T)$
$I_{LEAKAGE,65nm} / I_{LEAKAGE,90nm} = \exp[(V_{TH,90nm} - V_{TH,65nm})/(n*V_T)]$

From pard(c), $V_{TH,65nm} = 1/U * V_{TH,90nm} = 0.25V$
$I_{LEAKAGE,65nm} = I_{LEAKAGE,90nm} * \exp[(0.3 – 0.25)/(1.5*26mV)] = 60.08A$
$\therefore P_{LEAKAGE,65nm} = I_{LEAKAGE,65nm} * 1.0 = 60.08W$

90nm: $P_{DYNAMIC,90nm} + P_{LEAKAGE,90nm} = 96.67W$
65nm: $P_{DYNAMIC,65nm} + P_{LEAKAGE,65nm} = 115.64W$

[PROBLEM 2] Activity Factors and Sensitivity Analysis (30pts)

This problem will deal with the circuit in Fig.2; throughout this problem you can assume that $C_D = 0$, i.e. $\gamma=0$.

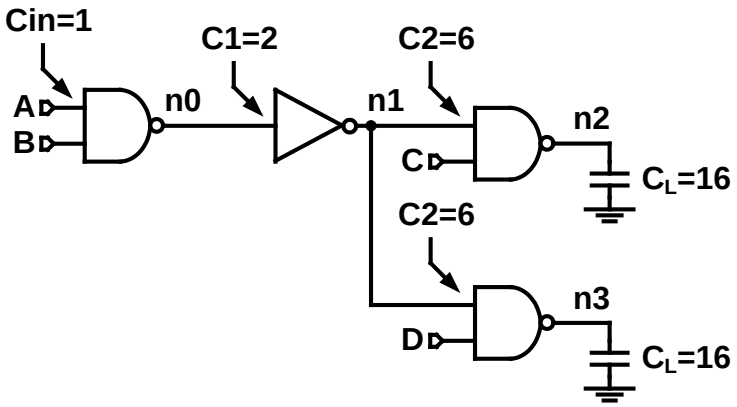

Fig.2

(a) **(5pts)** Assuming that all of the inputs A, B, C, and D have equal probability of being a 1 or a 0, what are the activity factors (i.e., $\alpha_{0\to1}$) at each of the nodes of the circuit (i.e., n0 – n3)?

i) n0: $P(n0=0)=P(A=1)*P(B=1)=1/4$
$\alpha_{0\to1}(n0) = 1/4*(1- 1/4) = 3/16$
ii) Inverter does not change activity factor
$\alpha_{0\to1}(n1) = ¼*(1- ¼) = 3/16$, NOTE: $P(n1=1)=P(n0=0)=1/4$
iii) n2: $P(n2=0)=P(n1=1)*P(C=1)=1/4*1/2 = 1/8$
$\alpha_{0\to1}(n2) = 1/8*(1- 1/8) = 7/64$
iv) n3: The same as n2 = 7/64

(b) **(5pts)** Assuming the circuit operates with a supply voltage VDD and a clock frequency f, what is the total dynamic power consumed by this circuit as a function of Cin, C1, C2, and C_L (as labeled above)? Note that you should include the power dissipated by driving the A, B, C, and D inputs.

$P_A = \alpha_{0\to1}(A)*Cin*VDD^2*f = 1/4*Cin*VDD^2*f$
$P_B = \alpha_{0\to1}(B)*Cin*VDD^2*f = 1/4*Cin*VDD^2*f$
$P_C = \alpha_{0\to1}(C)*C2*VDD^2*f = 1/4*C2*VDD^2*f$
$P_D = \alpha_{0\to1}(D)*C2*VDD^2*f = 1/4*C2*VDD^2*f$

$P_{n0} = \alpha_{0\to1}(n0)*C1*VDD^2*f = 3/16*C1*VDD^2*f$
$P_{n1} = \alpha_{0\to1}(n1)*2*C2*VDD^2*f = 3/8*C2*VDD^2*f$
$P_{n2} = \alpha_{0\to1}(n2)*CL*VDD^2*f = 7/64*CL*VDD^2*f$
$P_{n3} = \alpha_{0\to1}(n3)*CL*VDD^2*f = 7/64*CL*VDD^2*f$

$\therefore P_{TOTAL} = [1/2*Cin + 3/16*C1 + 7/8*C2 + 7/32*CL]*VDD^2*f$

(c) **(5pts)** Assuming that A is the critical input (i.e., the last one to transition) and that the transistors are quadratic long-channel, what is the delay of the decoder (in units of tinv) as a function of Cin, C1, C2, and C_L? Use LE method. Assume that tinv = 50pS.

$LE_{NAND2}=4/3$
$Tp = tinv*[4/3*C1/Cin + 2*C2/C1 + 4/3*CL/C2]$ because $\gamma=0$.
$= 50pS*[4/3*C1/Cin + 2*C2/C1 + 4/3*CL/C2]$

(d) **(10pts)** With the specific sizes shown above, what are the sensitivities S_{C1} and S_{C2}, where Sx = (∂ Power/∂ x)/(∂ Delay/∂ x)?

From part(b), $P_{TOTAL} = [1/2*Cin + 3/16*C1 + 7/8*C2 + 7/32*CL]*VDD^2*f$.
From part(c), $Tp = tinv*[4/3*C1/Cin + 2*C2/C1 + 4/3*CL/C2]$.

i) For C1,

S_{C1} = (∂ Power/∂ C1)/(∂ Tp/∂ C1)
$= (3/16* VDD^2*f) / (4/3*1/Cin – 2*C2/C1^2)*tinv$
$= -0.1125* VDD^2*f / tinv$

ii) For C2,

S_{C2} = (∂ Power/∂ C2)/(∂ Tp/∂ C2)
$= (7/8* VDD^2*f) / (2/C1 – 4/3*CL/C2^2)*tinv$
$= 2.148* VDD^2*f / tinv$

(e) **(5pts)** If you could change only one of the gate sizes (i.e., either C1 or C2), which one would you change, and in what direction? Be sure to explain your answer.

The magnitude of SC2 is larger than SC1. Moreover the sign of SC3 is positive. This means that if we decrease C2, we can get both lower power AND smaller delay. So, C2 should be decreased.

[PROBLEM 3] Minimum Energy Design (40pts)

Consider the logic block in Fig.3, consisting of sub-blocks A and B.

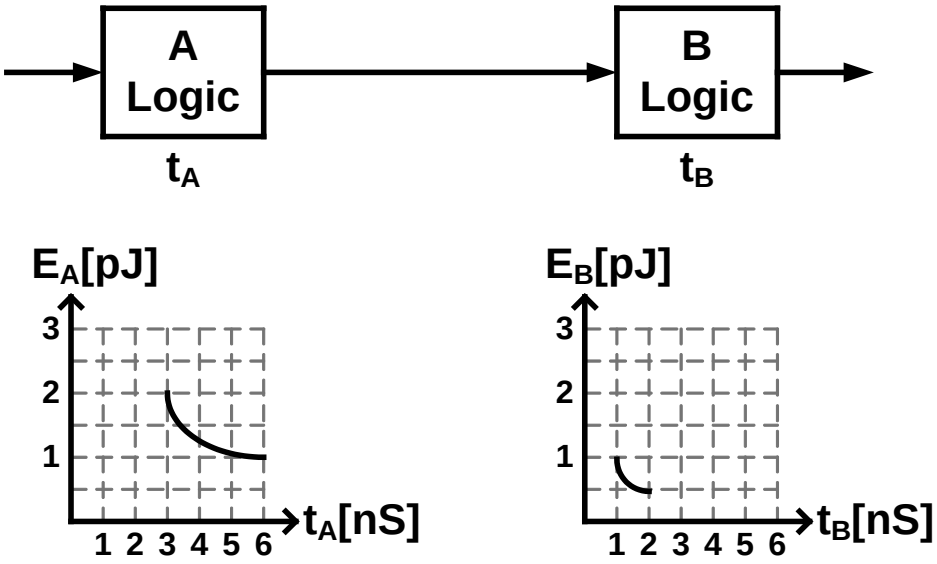

Fig.3

Sub-block A can be sized for the minimum delay of 3nS with the nominal supply voltage (1.2V) and the sub-block B can be sized for the minimum delay of 1nS with the nominal supply voltage, and their delays are additive (t_A+t_B=4nS). **Your task is to minimize the energy of operation of this block (t_A+t_B) when running at 5nS (which is more than the minimum delay by 1nS).**

Assumption:
i) The capacitance of logics is proportional to their size,
ii) The supply voltage is much higher than V_{TH},
iii) All of the energy is switching energy, i.e. no static current and leakage current.
iv) Long channel device and no channel length modulation. $\lambda = 0$.

Energy-delay tradeoffs with respect to sizing can be approximated analytically as:
$E_A = 6\times10^{-21}$J·S/t_A and $E_B = 10^{-21}$J·S/t_B

(a) **(20pts)** You can change sizing of either one or both of the blocks with the same supply voltage to get minimum energy when running at 5nS. (Circuit optimization)

$E_{TOT} = E_A + E_B = 6X10^{-21}/t_A + 10^{-21}/t_B$
$t_{TOT} = t_A + t_B = 5nS$
$\rightarrow E_{TOT} = E_A + E_B = 6X10^{-21}/(t_{TOT} - t_B) + 10^{-21}/t_B$

$\partial E_{TOT} / \partial t_B = 0$

$\therefore t_{A,NEW} = 3.55nS, t_{B,NEW} = 1.45nS$

$E_{A,NEW} = 6X10^{-21} / 3.55nS = 3nS / 3.55nS * 6X10^{-21} / 3nS = 0.845* E_{A,OLD}$
$\rightarrow AREA_{A,NEW} = 0.854*AREA_{A,OLD}$
$E_{B,NEW} = 10^{-21} / 1.45nS = 1nS / 1.45nS * 10^{-21} / 1nS = 0.69* E_{B,OLD}$
$\rightarrow AREA_{B,NEW} = 0.69*AREA_{B,OLD}$

$\therefore E_{TOT,NEW} = E_{A,NEW} + E_{B,NEW} = 0.845* E_{A,OLD} + 0.69* E_{B,OLD}$
$= 0.845*2pJ + 0.69* 1pJ = 2.38pJ$

(b) **(20pts)** You change their supply voltage to get minimum energy when running at 5nS, but there is only one supply voltage for the entire design. Assume that all transistors operate in saturation region. (VDD optimization)

Delay = $\ln(2)*R*C$ where $R = ¾*VDD/I_{D,SAT}$
$I_{D,SAT} = K*W/L*1/2*(VDD-V_{TH})2 \approx K*W/L*1/2*VDD^2$
$R = 2L/(K*W*VDD)$
Delay = $\ln(2) * ¾ * 2L/(K*W*VDD)*C = \alpha*C/VDD$

$t_{TOT,OLD} = 4nS = \alpha*(C_A+C_B)/V_{DD,OLD}$
$t_{TOT,NEW} = 5nS = \alpha*(C_A+C_B)/V_{DD,NEW}$
$V_{DD,NEW} /V_{DD,OLD} = t_{TOT,OLD} / t_{TOT,NEW} = 4/5$
$V_{DD,NEW} = 1.2 * 4/5 = 0.96V$

$t_{A,NEW} / t_{A,OLD} = [\alpha*C_A/V_{DD,NEW}] / [\alpha*C_A/V_{DD,OLD}] = V_{DD,OLD} / V_{DD,NEW}$
$t_{B,NEW} / t_{B,OLD} = [\alpha*C_B/V_{DD,NEW}] / [\alpha*C_B/V_{DD,OLD}] = V_{DD,OLD} / V_{DD,NEW}$

$\therefore t_{A,NEW} = 3.75nS$ and $t_{B,NEW} = 1.25nS$

$\therefore E_{TOT,NEW} = E_{A,NEW} + E_{B,NEW} = 6X10^{-21} / t_{A,NEW} + 10^{-21} / / t_{B,NEW} = 2.4pJ$