EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 7: EE223 Review

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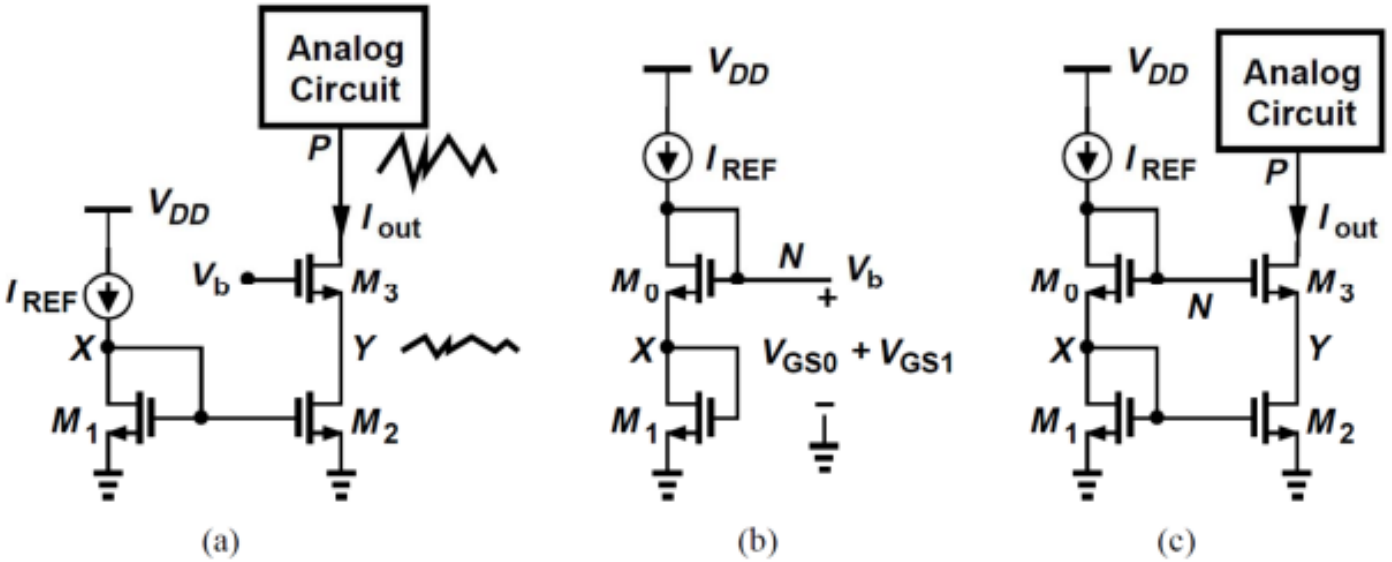
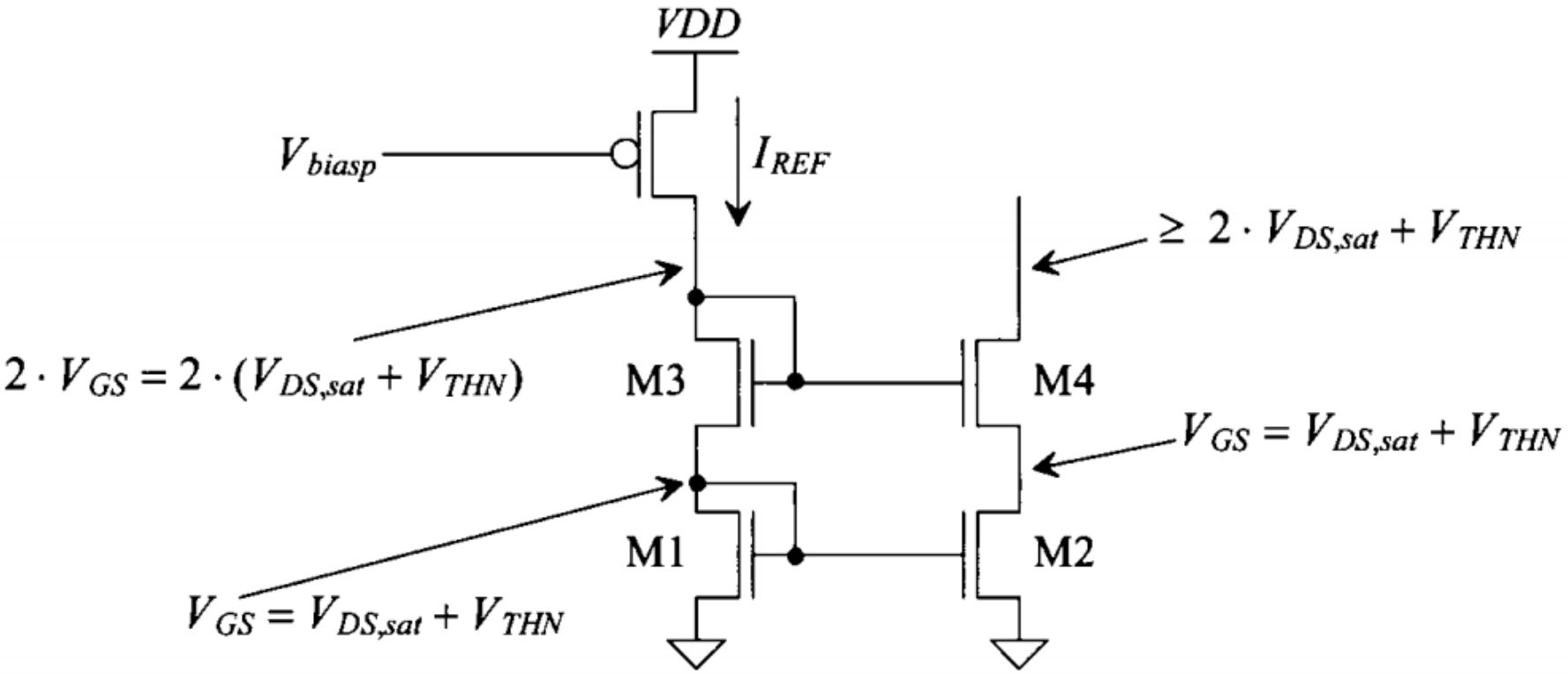
Cascode Biasing

Cascode Current Mirror



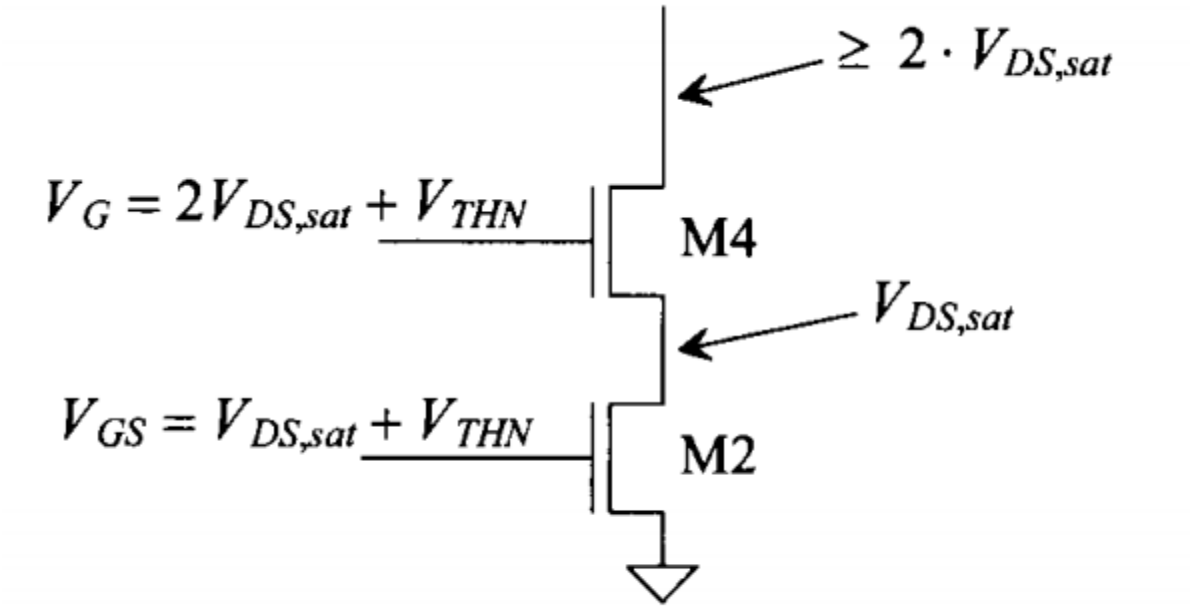
- A cascode device can shield a current source, thereby reducing the voltage variations across it.
- But, how do we ensure that $V_{DS2} = V_{DS1}$?
- We can generate V_b such that $V_b - V_{GS3} = V_{DS1}(=V_{GS1})$ with a stacked diode connected transistor

Cascode Current Mirror Compliance Voltage



(a) Regular cascode structure

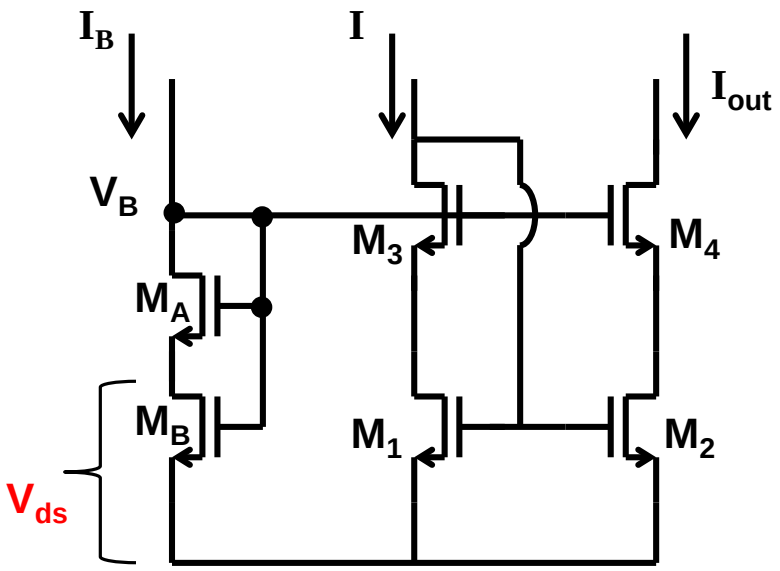
Wide-Swing (High-Swing or Low-Voltage) Cascode



(b) Low-voltage (aka wide-swing) structure

Biasing High Swing Cascode Current Mirror

Another approach for cascode biasing
→ Will use this biasing scheme extensively

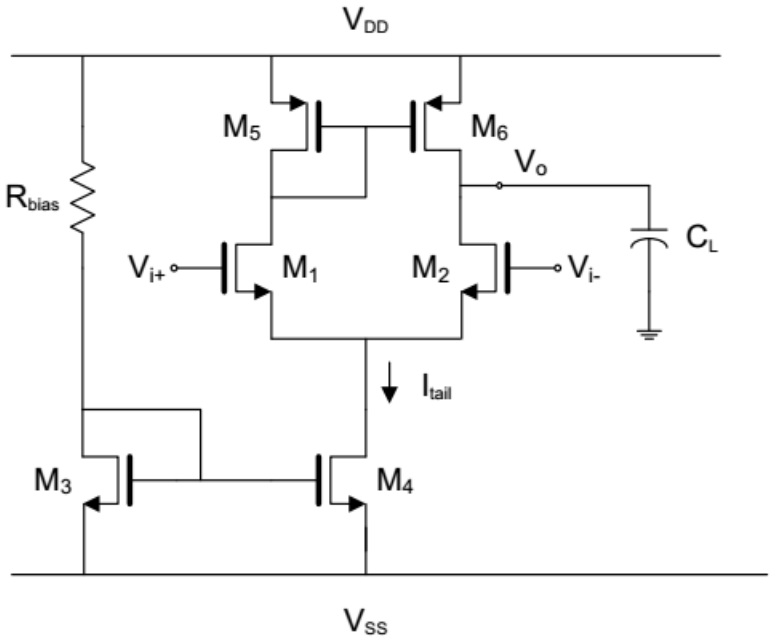


- M_A in Saturation
- M_B in Triode
- $(W/L)_A = (W/L)_3 = (W/L)_4$
- $(W/L)_B$ with large L
- Example:
  - $(W/L)_{A,3,4} = 5/0.18$
  - $(W/L)_B = 5/5$
  - Adjust L of M_B in Simulation to get the Vds you want

If you make the current densities of M_A, M_3 and M_4 are equal, V_{ds} of M_B will be copied over to V_{ds} of M_1 and M_2

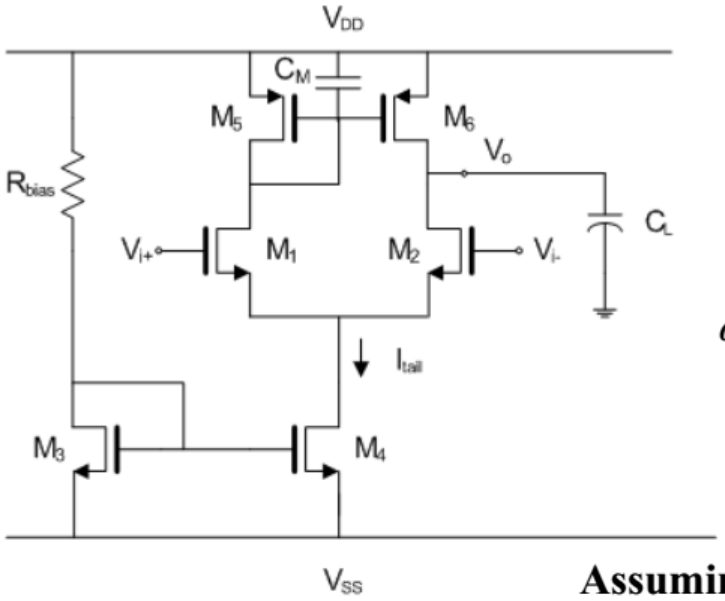
OTA

Operational Transconductance Amplifiers (OTA)



- Important Parameters
  - Differential Gain
  - Gain-Bandwidth Product
  - Common-Mode Input Range
  - Common-Mode Gain
  - Common-Mode Rejection Ratio (CMRR)
  - Power-Supply Rejection Ratio (PSRR)
  - Slew Rate

OTA Gain and Bandwidth



$$A_{DM} = \frac{g_{m1}}{g_{o6} + g_{o2}}$$

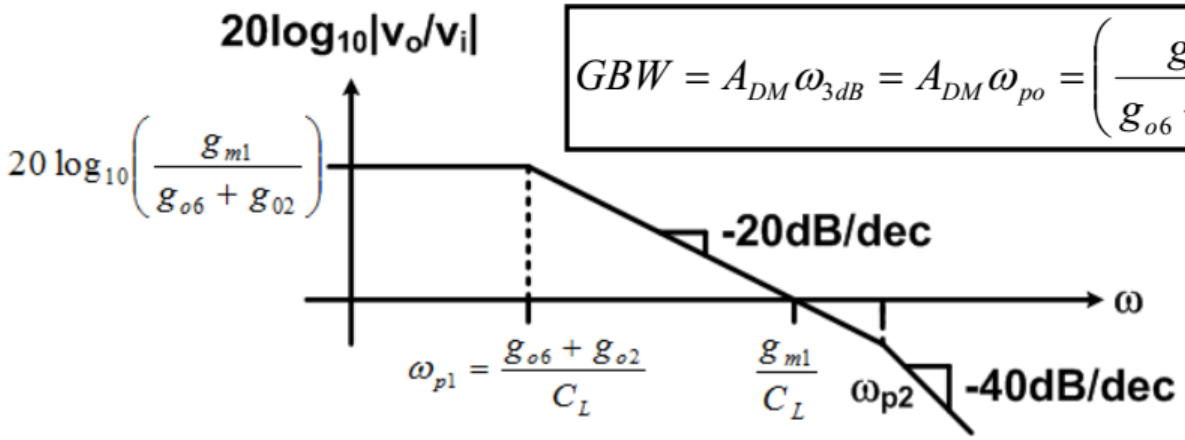
The circuit will have 2 poles

ω_{po} at the output node and ω_{pm} at the "mirror" node

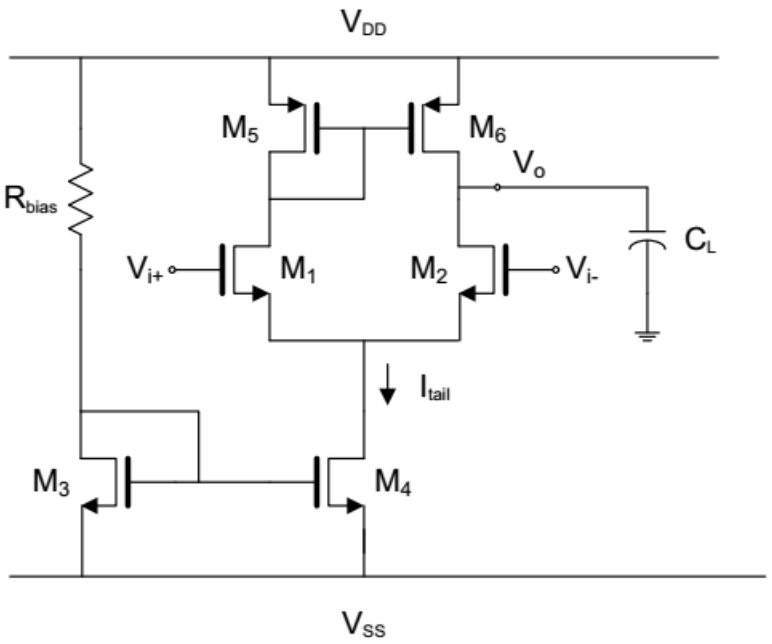
$$\omega_{po} \approx \frac{g_{o6} + g_{o2}}{C_L}, \quad \omega_{pm} \approx \frac{g_{m5}}{C_M}$$

Assuming the poles are widely spaced and ω_{po} dominates

$$GBW = A_{DM}\omega_{3dB} = A_{DM}\omega_{po} = \left(\frac{g_{m1}}{g_{o6} + g_{o2}}\right)\left(\frac{g_{o6} + g_{o2}}{C_L}\right) = \frac{g_{m1}}{C_L}$$



Simple OTA Summary



Transconductance $G_m = g_{m1} = \sqrt{KP_n \frac{W}{L_1} I_{TAIL}}$

Output Conductance $g_{out} = g_{o2} + g_{o6} = \frac{I_{TAIL}}{2}\left(\lambda_n + \lambda_p\right)$

DC Gain $A_v = G_m R_{out} = \frac{g_{m1}}{g_{o2} + g_{o6}} = \frac{2\sqrt{\frac{KP_n}{I_{TAIL}} \frac{W}{L_1}}}{\lambda_n + \lambda_p}$

Dominant Pole $\omega_{p1} = \frac{g_{o2} + g_{o6}}{C_L}$

Non-Dominant Pole $\omega_{p2} = \frac{g_{m6}}{C_M} \approx \frac{g_{mg}}{2C_{gs6}}$

Output Noise Current $i_{on}^2 = 2\left(\frac{8}{3}kT\right)\left(g_{m1} + g_{m6}\right)$

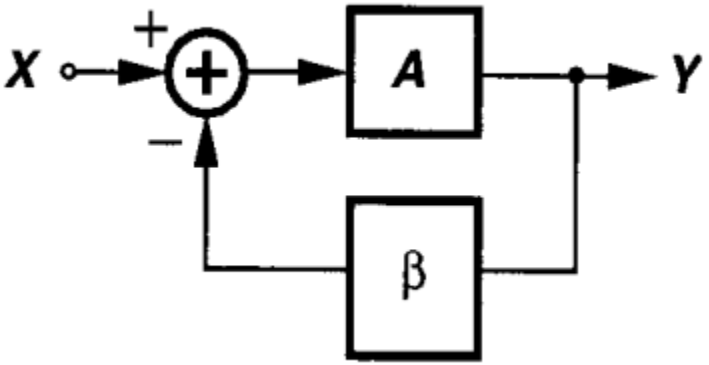
Input Noise Voltage $v_{in}^2 = 2\left(\frac{8}{3}kT\right)\left(\frac{1}{g_{m1}}\right)\left(1 + \frac{g_{m6}}{g_{m1}}\right)$

$GBW = \frac{G_m}{C_L} = \frac{\sqrt{KP_n \frac{W}{L_1} I_{TAIL}}}{C_L}$

Slew Rate $SR = \frac{I_{tail}}{C_L}$

Feedback

Simple Feedback System



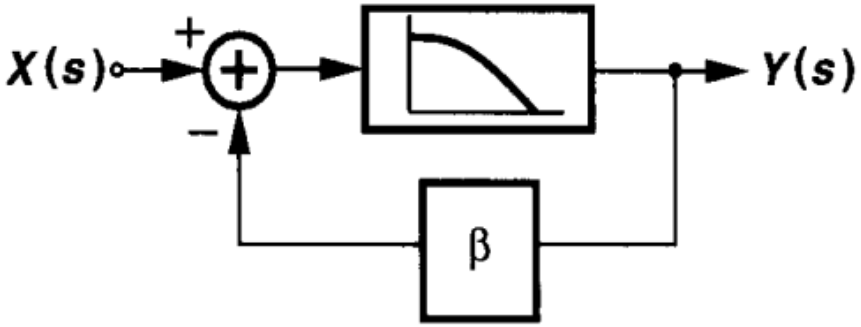
$$\frac{Y}{X} = \frac{A}{1+\beta A}$$

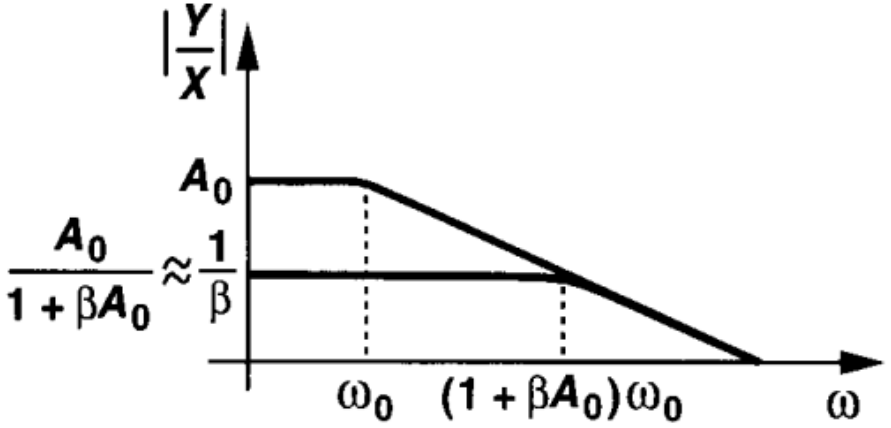
$$\approx \frac{1}{\beta}\left(1 - \frac{1}{\beta A}\right)$$

where we have assumed $\beta A \gg 1$

Bandwidth Modification of Feedback System

$$A(s) = \frac{A_0}{1 + \dfrac{s}{\omega_0}}$$



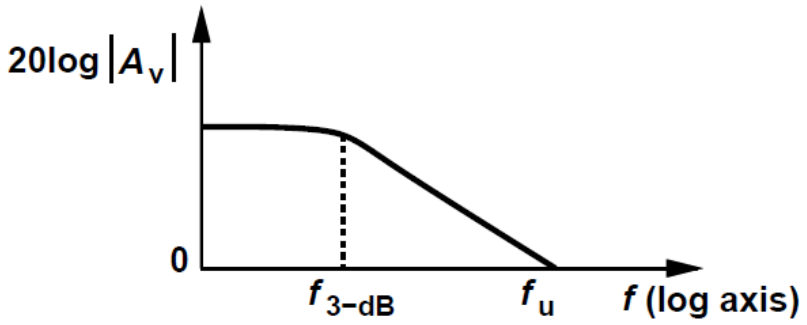


$$\frac{Y}{X}(s) = \frac{\dfrac{A_0}{1 + \dfrac{s}{\omega_0}}}{1 + \beta\dfrac{A_0}{1 + \dfrac{s}{\omega_0}}} = \frac{A_0}{1 + \beta A_0 + \dfrac{s}{\omega_0}} = \frac{\dfrac{A_0}{1 + \beta A_0}}{1 + \dfrac{s}{(1 + \beta A_0)\omega_0}}$$

OPAMP

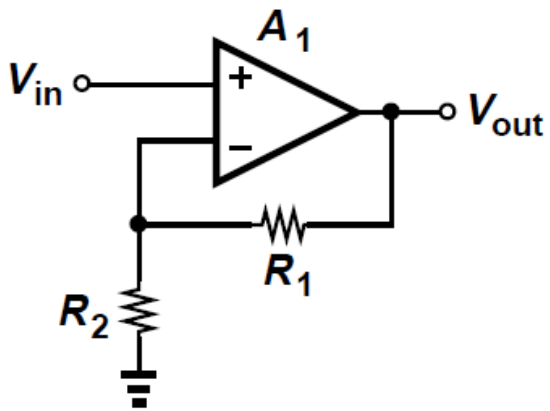
Performance Parameters

- **Gain(Precision), Bandwidth(Speed): 3-dB, f_u Output Swing, Power dissipation**
- **Noise, Linearity, Supply Rejection, Offset**
- **Input CM Range, Input/Output Impedance**
- **Large-Signal behavior (e.g. Slew rate)**



OPAMP Gain Requirement

The circuit has a nominal gain of 10. i.e.,$1+R_1/R_2=10$. Determine the minimal value of A1 for a gain error 1%:



Solution:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{A_1}{1+\frac{R_2}{R_1+R_2}A_1}}{} = \frac{R_1+R_2}{R_2}\frac{A_1}{\frac{R_1+R_2}{R_2}+A_1}$$

$$\frac{V_{out}}{V_{in}} \approx \left(1+\frac{R_1}{R_2}\right)\left(1-\frac{R_1+R_2}{R_2}\frac{1}{A_1}\right)$$

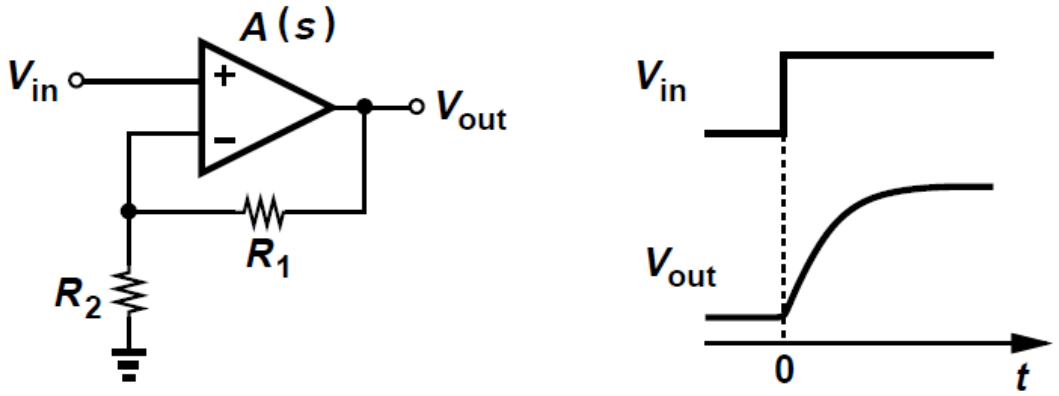
$$\textbf{Gain error} = \frac{\mathbf{1}}{\boldsymbol{\beta A}}$$

OPAMP Speed Requirement

OPAMP open-loop transfer function

$$A(s) = A_0/(1 + s/\omega_0)$$

For a small step input, calculate the time required it to reach within 1% of its final value if $1+R_1/R_2=10$. What is the required unity-gain bandwidth of the amplifier for it to achieve 5ns settling time? Assume A_0 is very large.

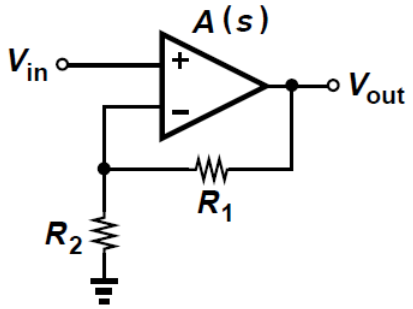


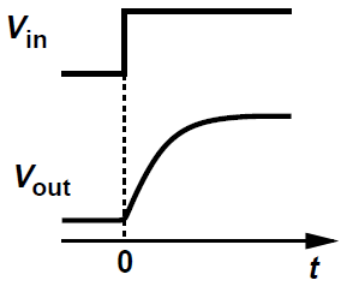
OPAMP Speed Requirement

$$[V_{in} - \beta V_{out}]A(s) = V_{out}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1+\beta A(s)}$$

$$A(s) = \frac{A_0}{1+\frac{S}{\omega_0}}$$





$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1+\beta A(s)} = \frac{\frac{A_0}{1+\frac{S}{\omega_0}}}{1+\beta\left[\frac{A_0}{1+\frac{S}{\omega_0}}\right]} = \frac{A_0}{1+\frac{S}{\omega_0}+\beta A_0} = \frac{\frac{A_0}{[1+\beta A_0]}}{1+\frac{S}{[1+\beta A_0]\omega_0}} \approx \frac{1}{\beta}\,\frac{1}{1+\frac{S}{\beta A_0 \omega_0}} = \frac{A_{dc}}{1+\tau S}$$

where $A_{dc} = \frac{1}{\beta}$, $\tau = \frac{1}{\omega_{-3dB,CL}} = \frac{1}{\beta A_0 \omega_0} = \frac{1}{\beta \omega_u}$

$$V_{out}(s) = \frac{A_{dc}}{1+\tau S}V_{in}(s) = \frac{A_{dc}}{1+\tau S}\cdot\frac{a}{S} = aA_{dc}\left[\frac{1}{S} - \frac{\tau}{1+\tau S}\right] = aA_{dc}\left[\frac{1}{S} - \frac{1}{1+\frac{S}{\tau}}\right]$$

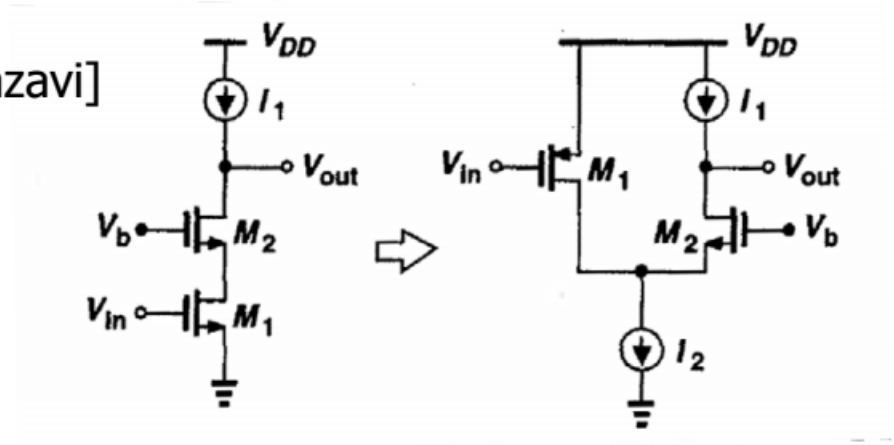
$$\rightarrow V_{out}(t) = aA_{dc}\left[1 - e^{\frac{-t}{\tau}}\right]u(t)$$

For 1% settling, $1 - e^{\frac{-t}{\tau}} = 0.99 \rightarrow t_{1\%} = \tau \ln 100 \approx 4.6\tau = 5$ ns $\rightarrow \tau = 1.09$ ns

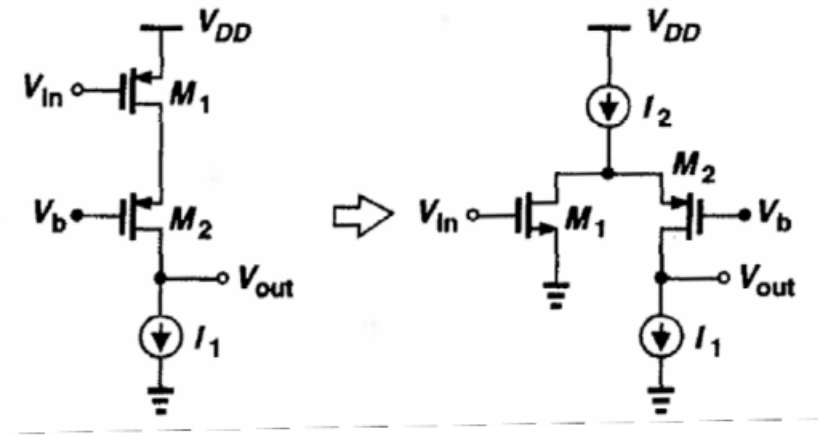
$$\rightarrow \tau = \frac{1}{\beta\omega_u} = \frac{10}{\omega_u} \rightarrow \omega_u = \frac{10}{1.09\,ns} = 9.21G\ rad/s \rightarrow f_u = 1.47GHz$$

Folded Cascode Circuits

[Razavi]



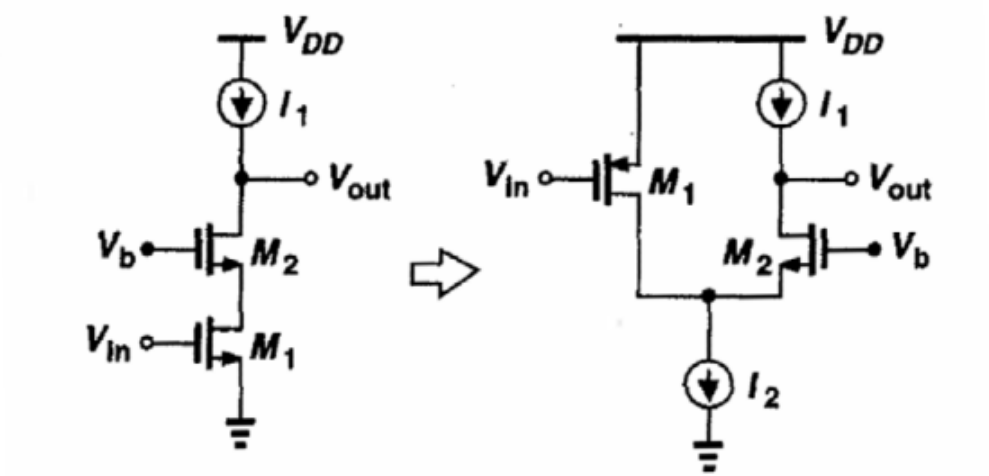
PMOS Input & NMOS Cascode



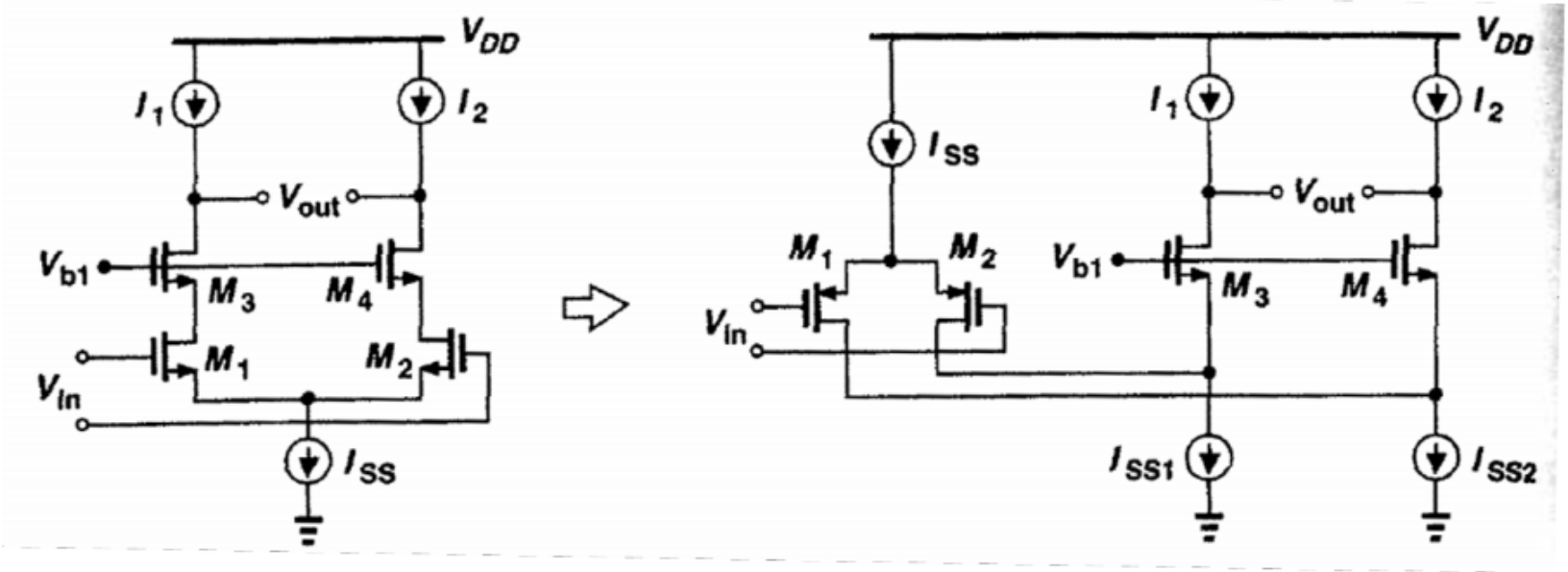
NMOS Input & PMOS Cascode

- "Folding" about the cascode node will increase input and output swing range

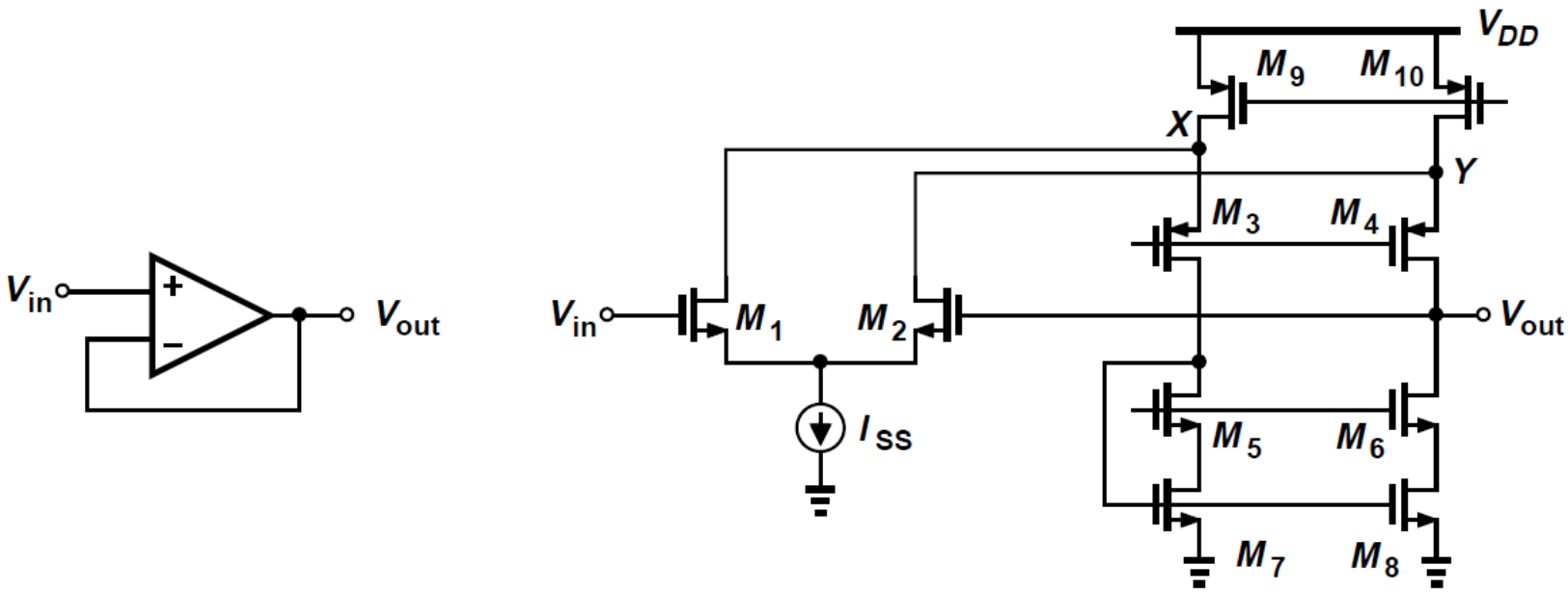
Folded Cascode OTA



[Razavi]

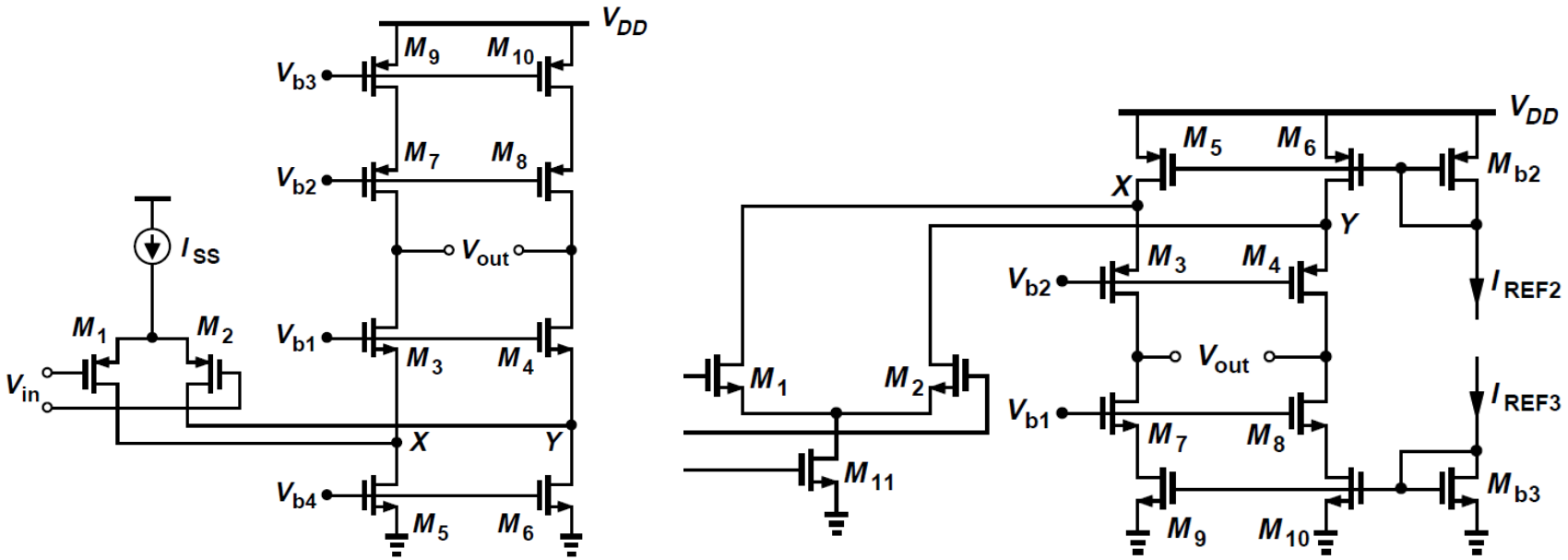


Folded Cascode OPAMP

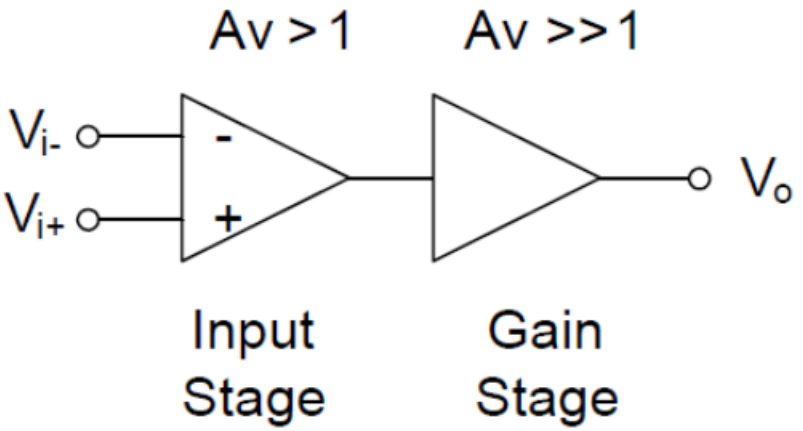


NMOS vs PMOS Input

- Greater mobility from NMOS input leads to higher gain
- PMOS input is less sensitive to flicker noise (wider WL)
- Usually input common-mode level dictates which input to use



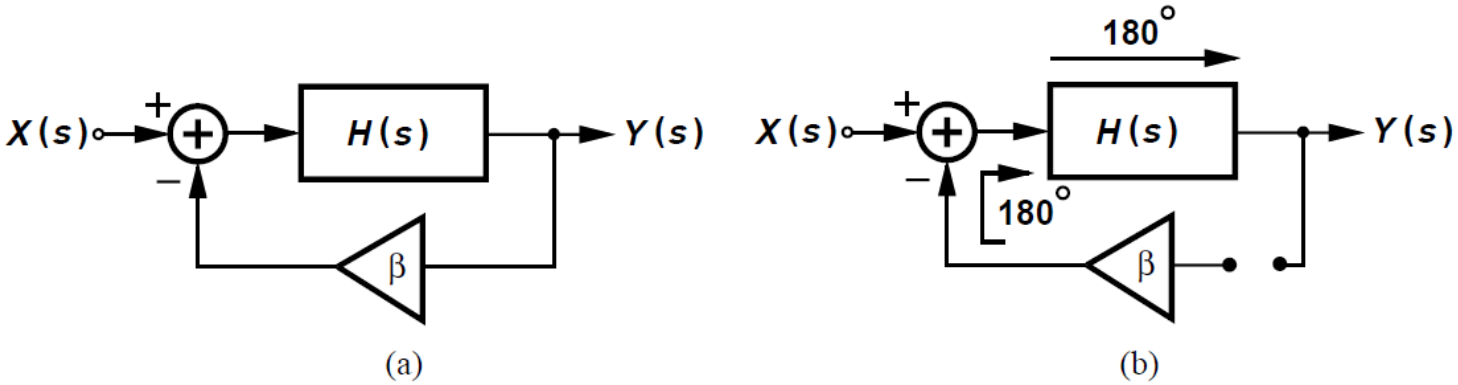
Multi-Stage Amplifiers



- Single-stage amplifiers typically have to trade-off gain and swing range
- Multi-stage amplifiers allow for higher gain without sacrificing swing range
- The major challenge with multi-stage amplifiers is achieving adequate phase margin to insure stability in a feedback configuration

Stability

Negative Feedback and Phase Shift



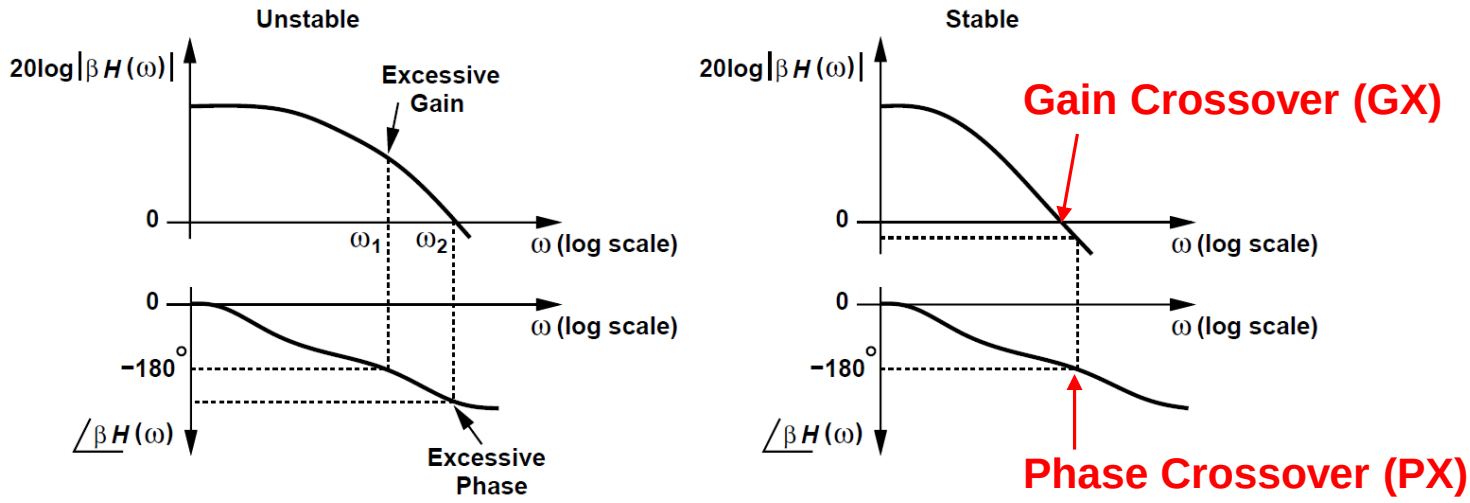
- **Feedback systems suffer from potential instability and they may oscillate.**
- **Closed-loop transfer function:** $\frac{Y}{X}(s) = \frac{H(s)}{1 + \beta H(s)}$
- **What happens if the denominator goes to infinity**

$$|\beta H(j\omega_1)| = 1$$
$$\angle \beta H(j\omega_1) = -180^\circ$$

"Barkhausen's criteria"

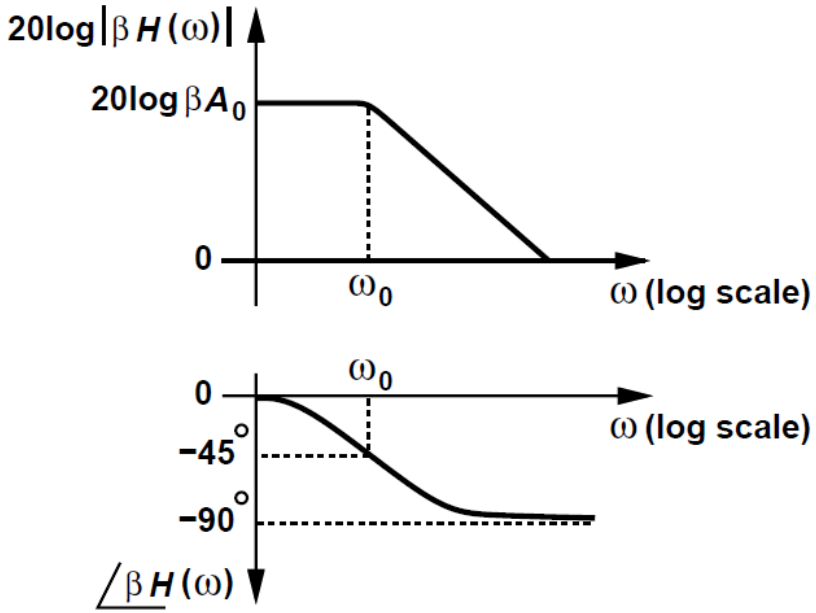
- **Negative feedback itself provide 180 phase shift**
- **Loop transmission determines the stability issue**

Bode Plots of Loop Gain



- Phase shift changes the negative feedback to positive
- Gain crossover when gain is unity
- Phase crossover when phase is –180 degrees
- PX must be behind GX, and GX is equal to unity-gain bandwidth in the open-loop system

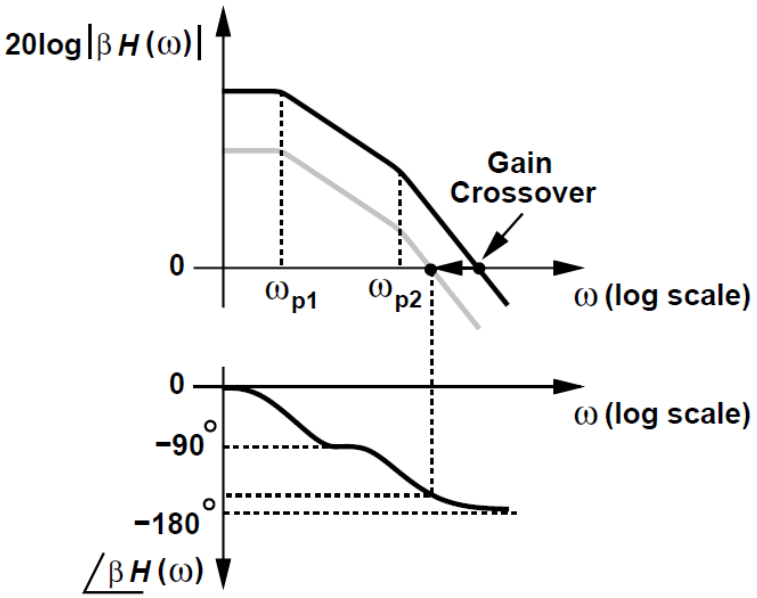
One-Pole System – Unconditionally Stable



$$H(s) = A_0/(1 + s/\omega_0)$$

$$\frac{Y}{X}(s) = \frac{\dfrac{A_0}{1+\beta A_0}}{1 + \dfrac{s}{\omega_0(1+\beta A_0)}}$$

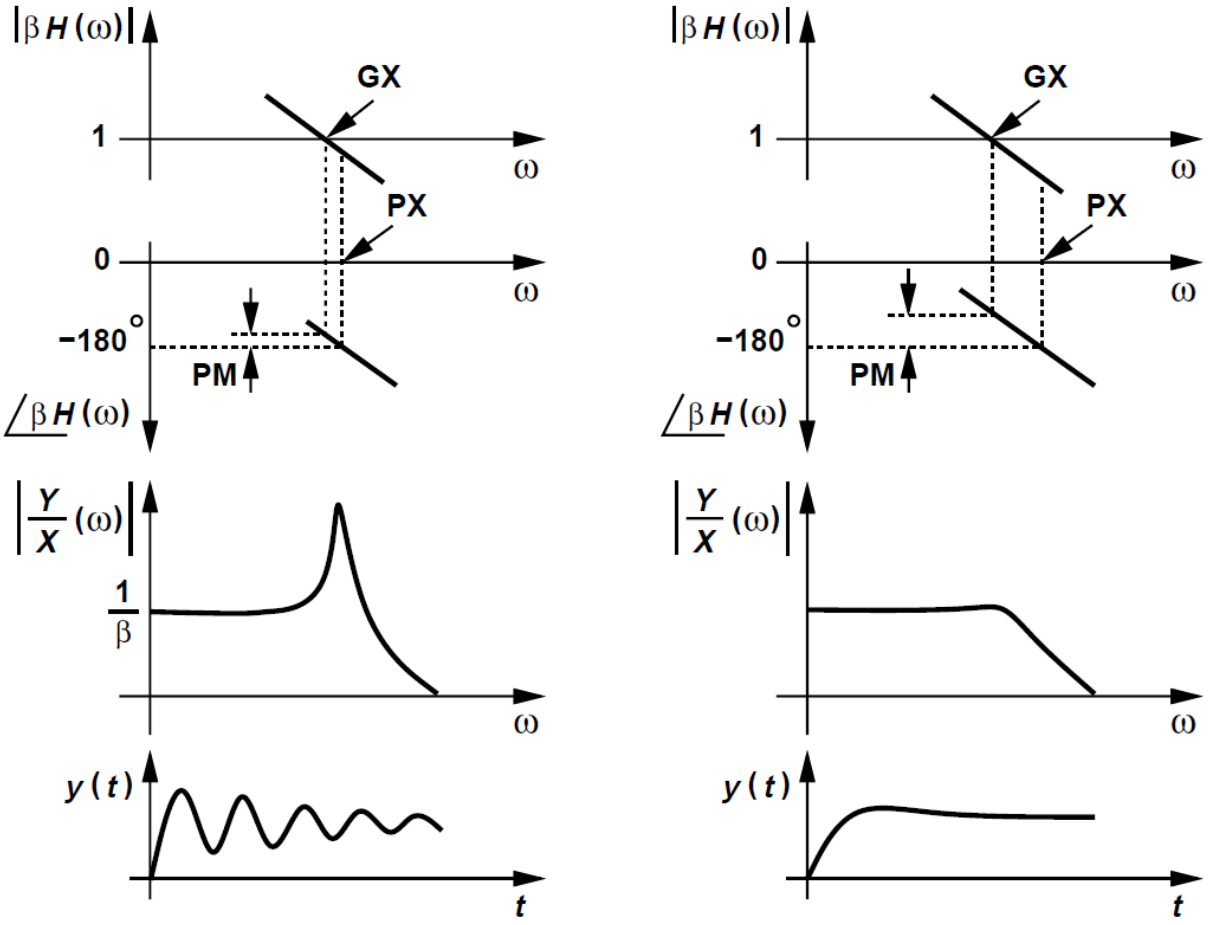
Multi-Pole System



- **The system is stable if phase is less than -180 degrees at gain crossover**
- **If the feedback becomes weaker, the system is more stable**

Phase Margin

How far should PX be from GX?



Phase Margin

- **Phase Margin(PM), defined as**

$$\text{PM} = 180^\circ + \angle \beta H(\omega = \omega_1)$$

- **A “well-behaved” closed-loop response will have a greater spacing between GX and PX**
- **The unity-gain bandwidth cannot exceed the second pole frequency**

- **For large-signal application, time-domain simulation of closed-loop system more relevant and useful than small-signal as computations**

Phase Margin Comparison

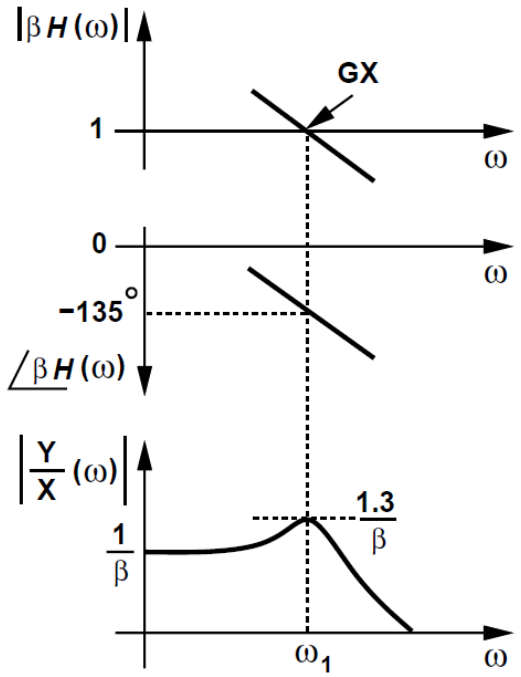
- **How much phase margin is adequate?**

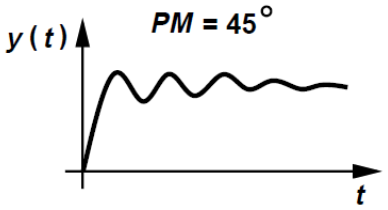
PM = 45 degrees

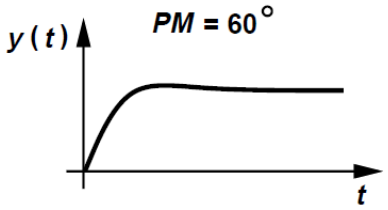
$$\frac{Y}{X} = \frac{H(j\omega_1)}{1 + 1 \times \exp(-j135^\circ)} = \frac{H(j\omega_1)}{0.29 - 0.71j} \approx \frac{1.3}{\beta}$$

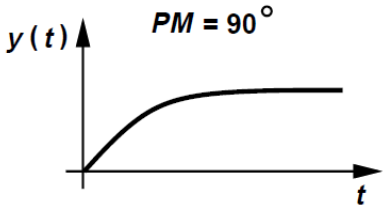
PM = 60 degrees

$$Y(j\omega_1)/X(j\omega_1) = 1/\beta$$









Step Response and Phase Margin

Consider the step response of second-order system which closely models the closed-loop gain of the op amp connected in unity gain.

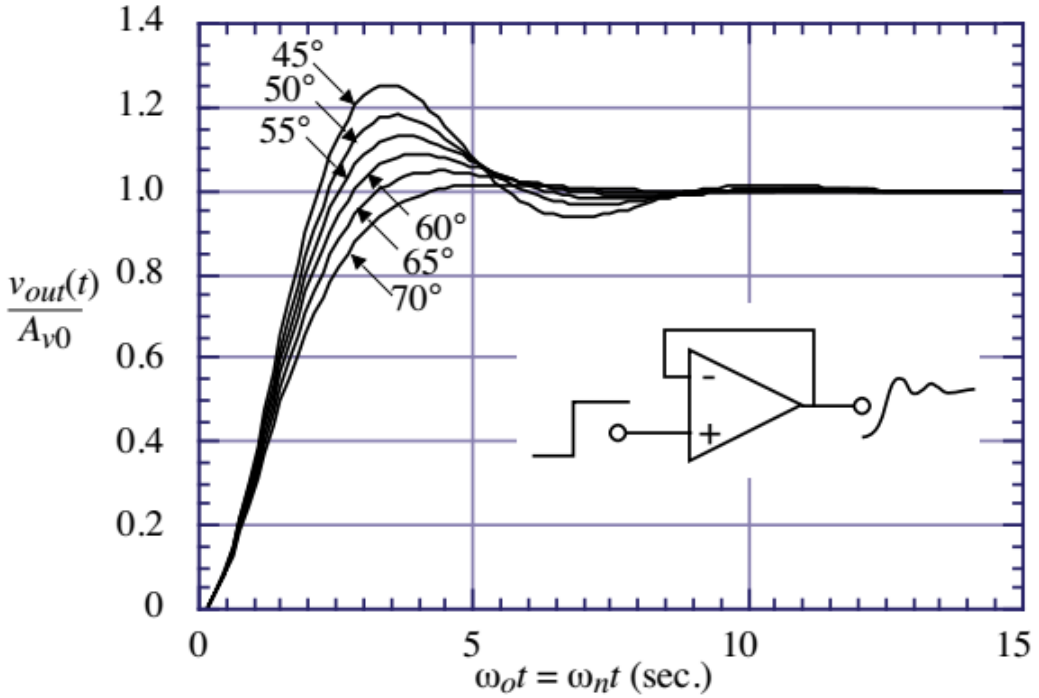


Fig. 120-03

A "good" step response is one that quickly reaches its final value.

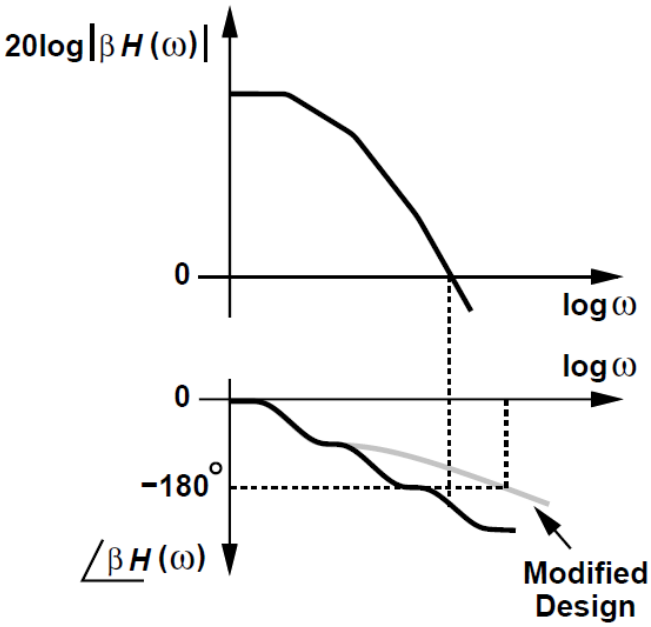
Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

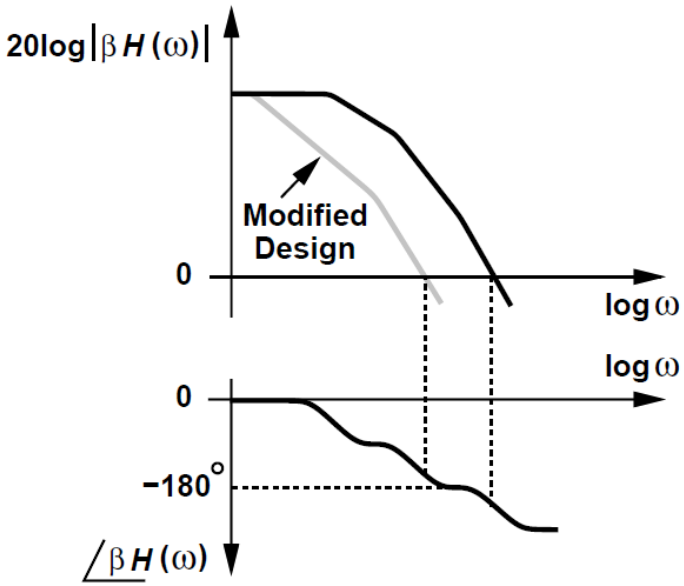
(A rule of thumb for satisfactory stability is that there should be less than three rings.)

Note that good stability is not necessarily the quickest rise time.

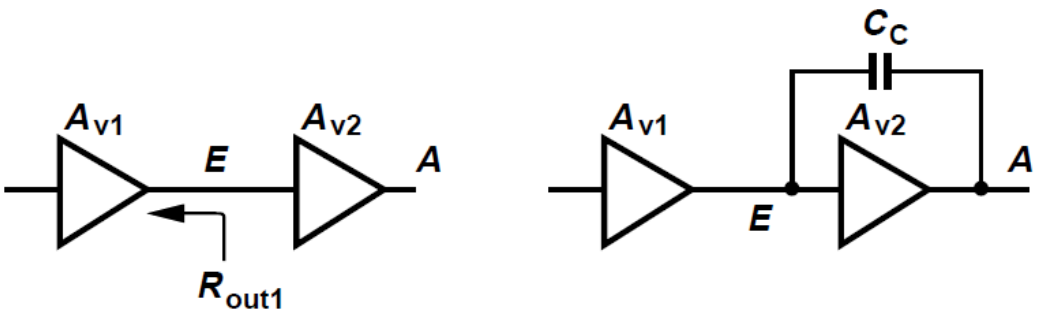
Basic Frequency Compensation

- Be “compensated”, the circuit open-loop transfer function must be modified such that closed-loop circuit is stable
  - minimizing the overall phase shift
  - dropping the gain with frequency

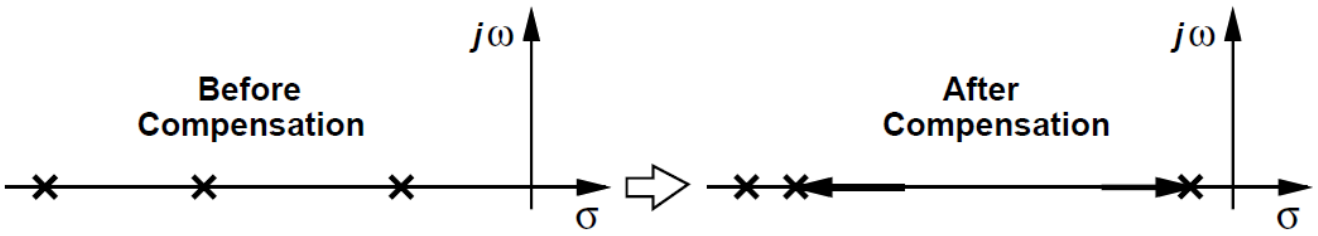




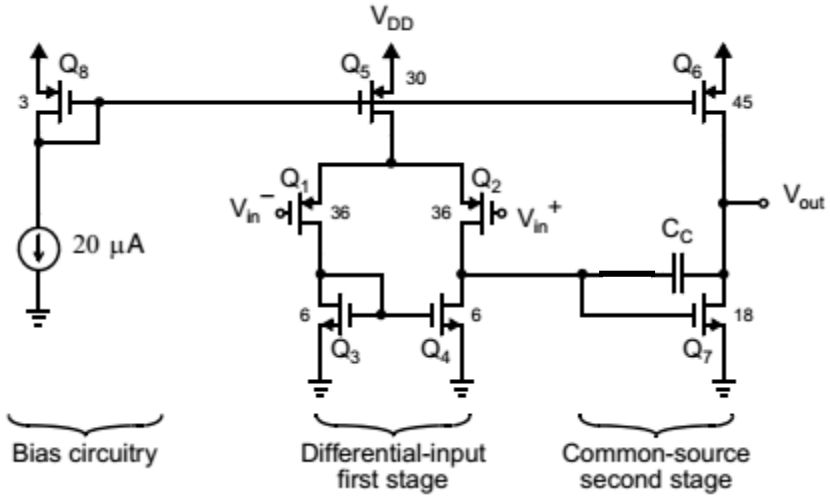
Miller Compensation



- **A larger C creating a dominating pole** $R_{out1}^{-1}[C_E + (1 + A_{v2})C_C]^{-1}$
- **Pole splitting**



Two-Stage OPAMP with Miller Compensation



$$A_{v1} = -g_{m1}(r_{ds2} \parallel dr_{ds4})$$

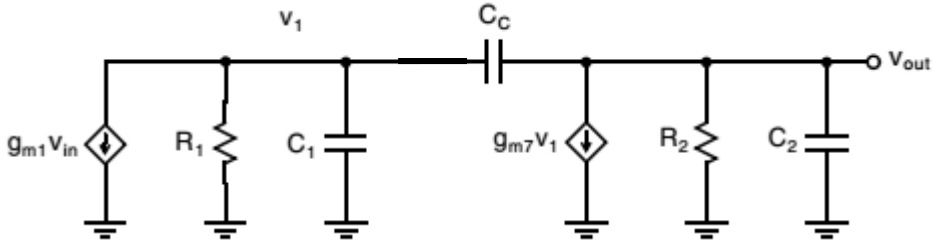
$$A_{v2} = -g_{m7}(r_{ds6} \parallel r_{ds7})$$

$$R_1 = r_{ds4} \parallel r_{ds2}$$

$$C_1 = C_{db2} + C_{db4} + C_{gs7}$$

$$R_2 = r_{ds6} \parallel r_{ds7}$$

$$C_2 = C_{db7} + C_{db6} + C_{L2}$$



$$A_v(s) = \frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m7}R_1R_2\left(1 - \frac{sC_C}{g_{m7}}\right)}{1 + sa + s^2b}$$

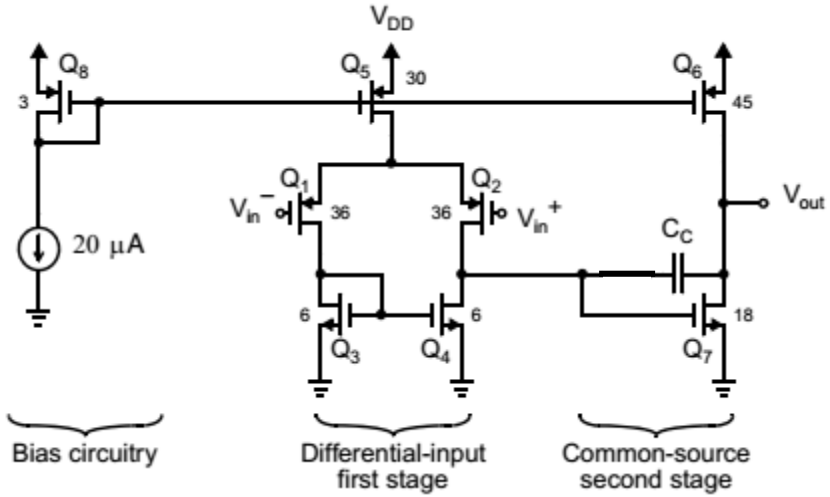
$$a = (C_2 + C_C)R_2 + (C_1 + C_C)R_1 + g_{m7}R_1R_2C_C$$

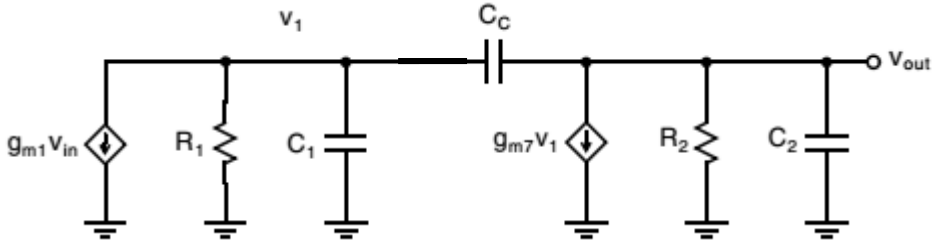
$$b = R_1R_2(C_1C_2 + C_1C_C + C_2C_C)$$

$$A(s) = \frac{A_0\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) \cong 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}}$$

Two-Stage OPAMP with Miller Compensation





$$A_{v1} = -g_{m1}(r_{ds2} \parallel dr_{ds4})$$

$$A_{v2} = -g_{m7}(r_{ds6} \parallel r_{ds7})$$

$$\omega_{p1} \cong \frac{1}{R_1[C_1 + C_C(1 + g_{m7}R_2)] + R_2(C_2 + C_C)} \cong \frac{1}{R_1 C_C(1 + g_{m7}R_2)} \cong \frac{1}{g_{m7}R_1R_2C_C}$$

$$\omega_{p2} \cong \frac{g_{m7}C_C}{C_1C_2 + C_2C_C + C_1C_C} \cong \frac{g_{m7}}{C_1 + C_2}$$

$$\omega_z = \frac{-g_{m7}}{C_C}$$

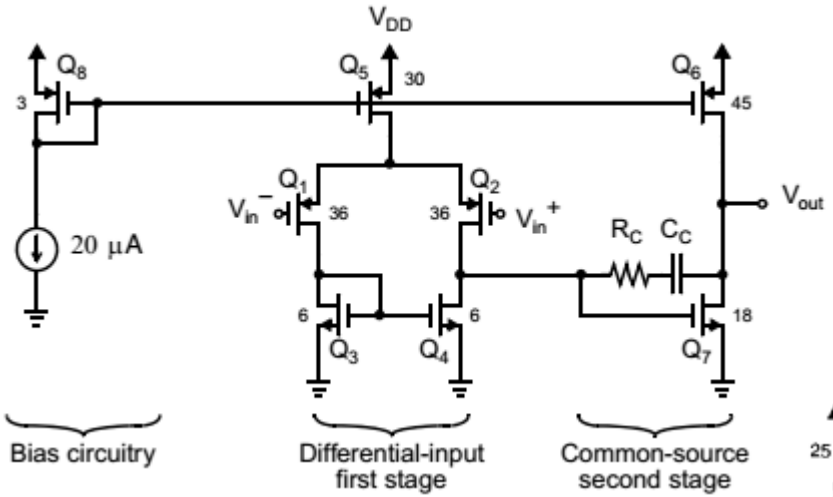
← RHP Zero due to C_c

$$A(s) = \frac{A_0(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

$$\text{GBW} = \omega_u = (A_{v1}A_{v2})\left(\frac{1}{R_1A_{v2}C_c}\right) = \frac{A_{v1}}{R_1C_c} = \frac{g_{m1}R_1}{R_1C_c} = \boxed{\frac{g_{m1}}{C_c}}$$

Two-Stage OPAMP with RC Compensation

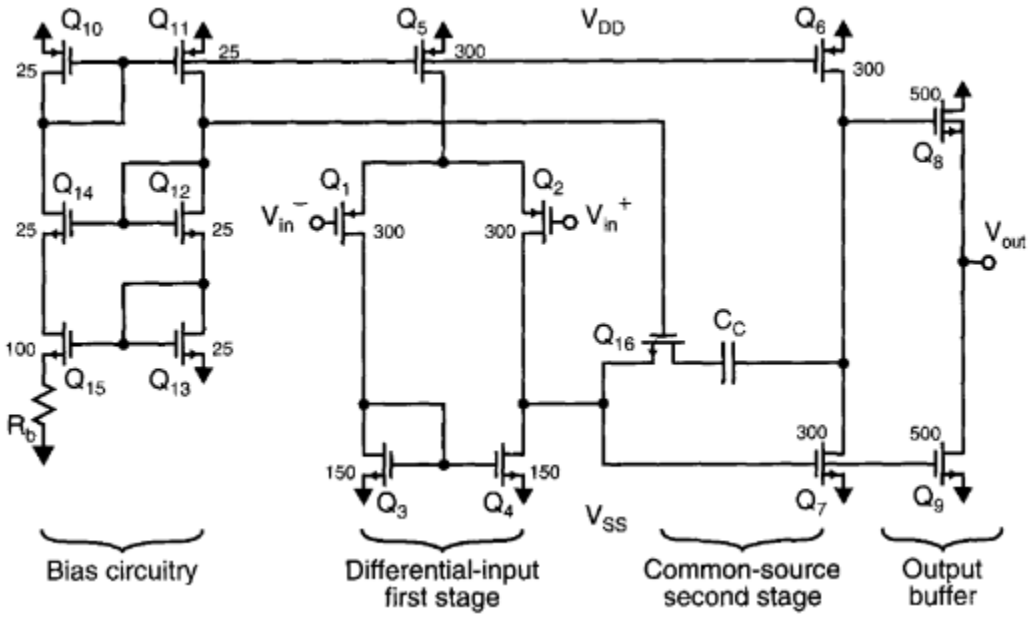
2-stage opamp



$$A(s) = \frac{A_0(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}$$

$$\omega_z = \frac{-1}{C_c(\frac{1}{g_{m7}} - R_c)}$$

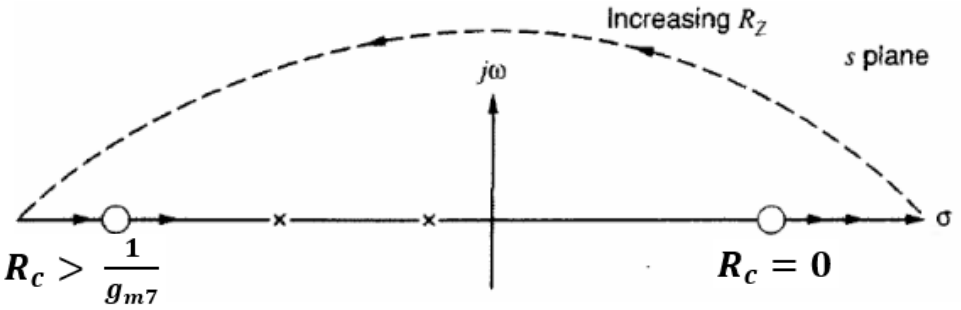
2-stage opamp with output stage



Choice of Rc

$$A(s) = \frac{A_0(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \qquad \omega_z = \frac{-1}{C_c(\frac{1}{g_{m7}} - R_c)}$$

- $R_c = 0 \rightarrow \omega_z = \frac{-1}{C_c(\frac{1}{g_{m7}})} = \frac{-g_{m7}}{C_c} \rightarrow$ RHP Zero ! Stability Issue
- $R_c = \frac{1}{g_{m7}} \rightarrow \omega_z = \infty$
- $R_c > \frac{1}{g_{m7}}$



$\rightarrow \omega_z = \omega_{p2}$

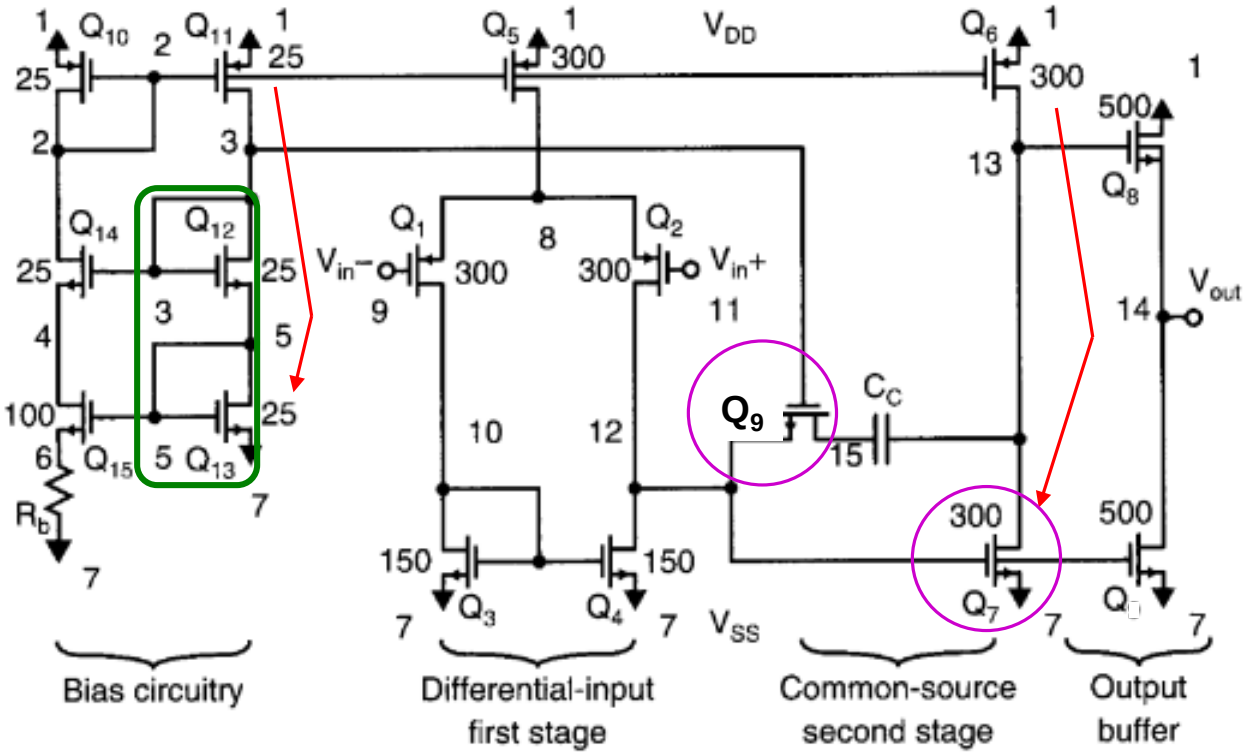
$$\frac{-1}{C_c(\frac{1}{g_{m7}} - R_c)} = \frac{g_{m7}}{C_1+C_2} \rightarrow R_c = \frac{1}{g_{m7}}\left(1+\frac{C_1+C_2}{C_c}\right)$$

- $R_c \gg \frac{1}{g_{m7}}$

$$\omega_z \approx \frac{1}{R_c C_c} = \alpha\omega_u = \alpha\frac{g_{m1}}{C_c}$$

Choosing $\alpha = 2$ is a good starting point.

Conclusion for Replacing Rz with Transistor



1. $\frac{(\frac{W}{L})_6}{(\frac{W}{L})_7} = \frac{(\frac{W}{L})_{11}}{(\frac{W}{L})_{13}}$

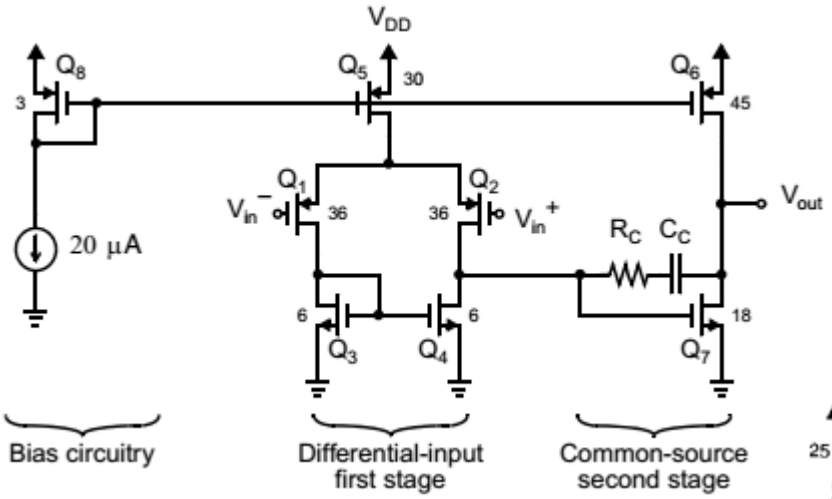
2. $(\frac{W}{L})_{12} = (\frac{W}{L})_{13}$

3. $(\frac{W}{L})_9 = 0.2\,(\frac{W}{L})_7$

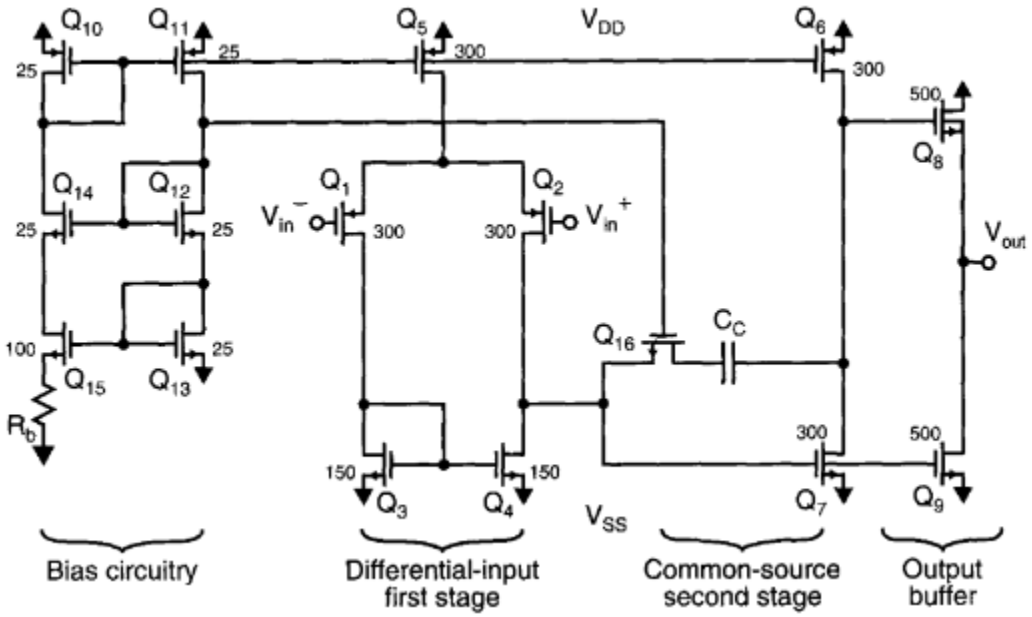
Output Stages

Two-Stage OPAMP with SF Output Stage

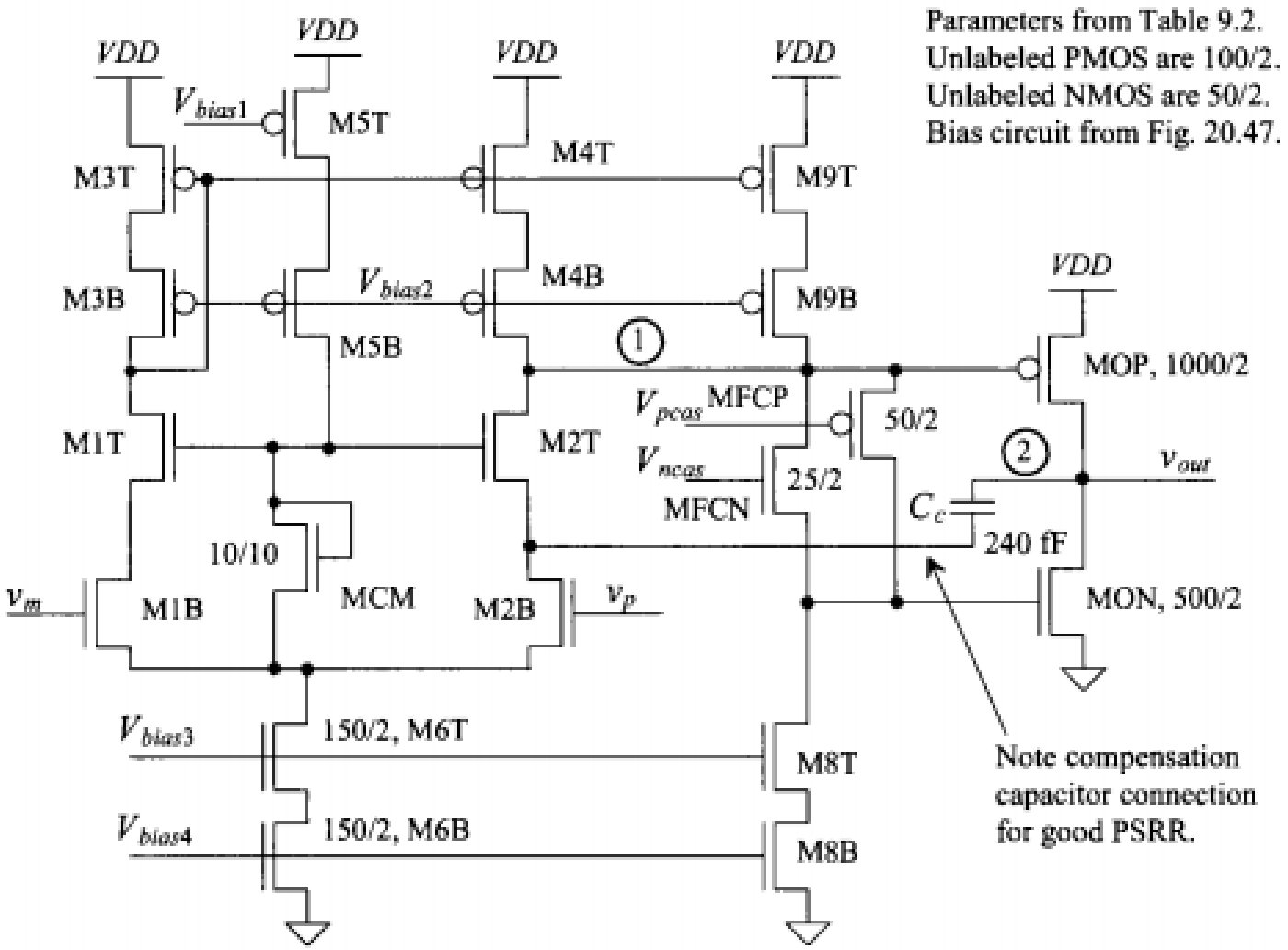
2-stage opamp



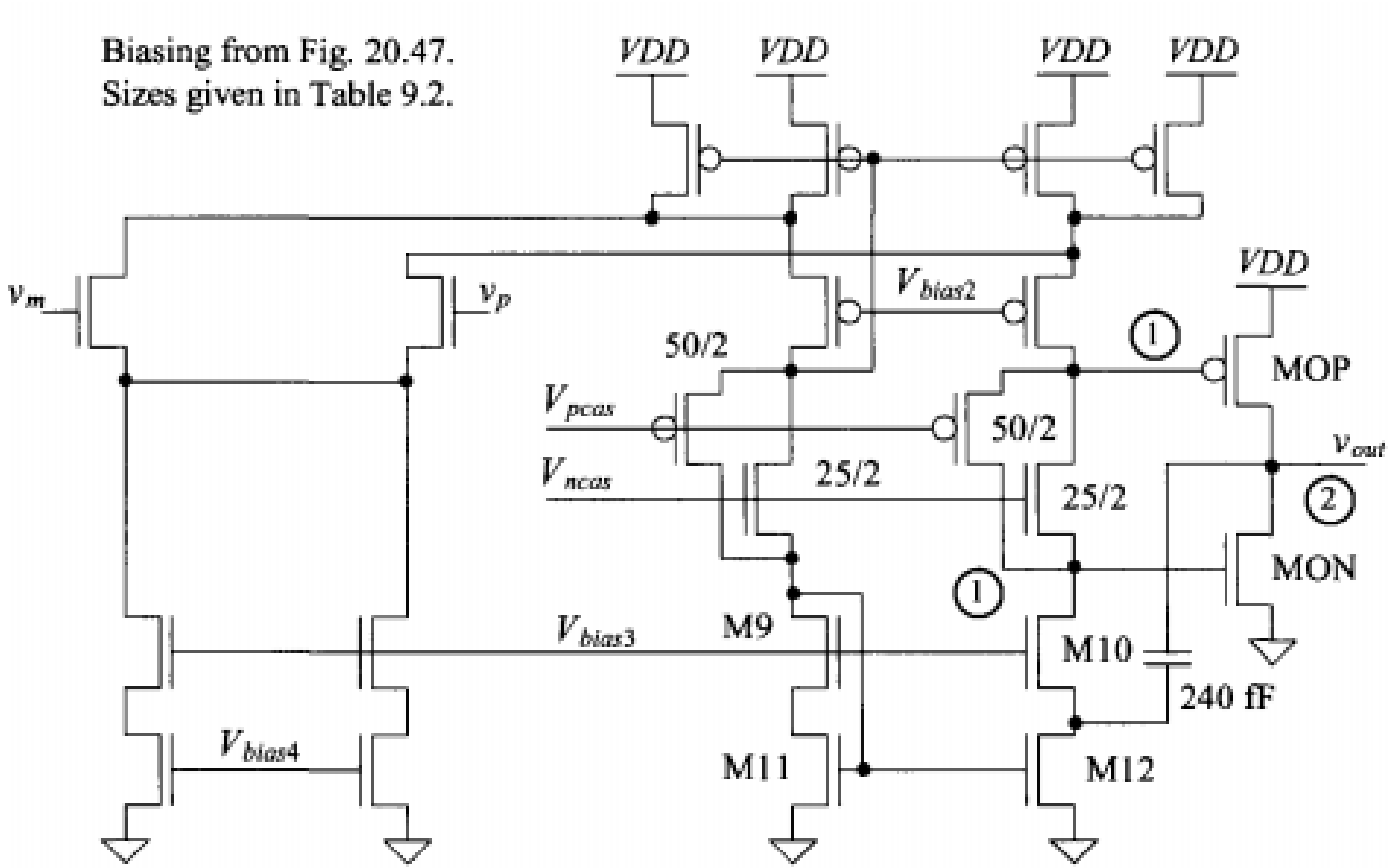
2-stage opamp with output stage



Two-Stage OPAMP with Class AB Output Stage



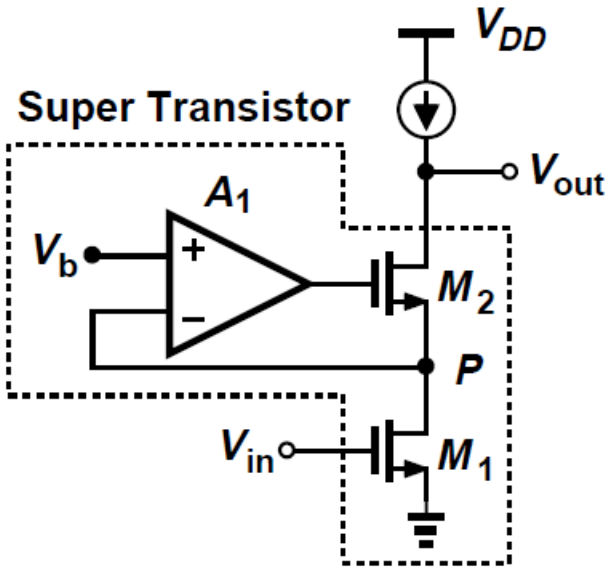
Folded-Cascode OPAMP with Class AB Output Stage



Gain Boosting

Gain Boosting

- Increase the output impedance without adding more cascode devices.
- A transistor preceded by an ideal voltage amplifier exhibits an effective transconductance of $g_m \cdot A_1$

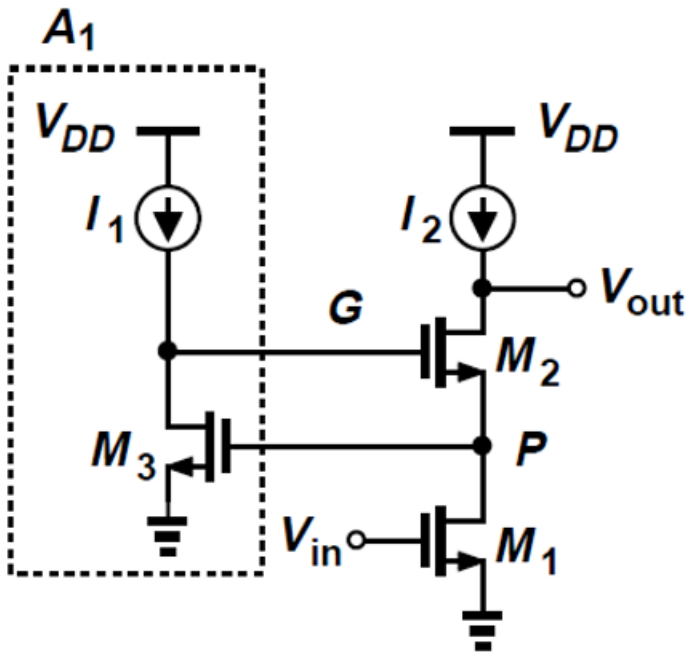


$$|A_v| \approx g_{m1}[r_{O2} + (A_1 + 1)g_{m2}r_{O2}r_{O1} + r_{O1}]$$
$$\approx g_{m1}g_{m2}r_{O1}r_{O2}(A_1 + 1).$$

Gain Boosting Circuit Implementation

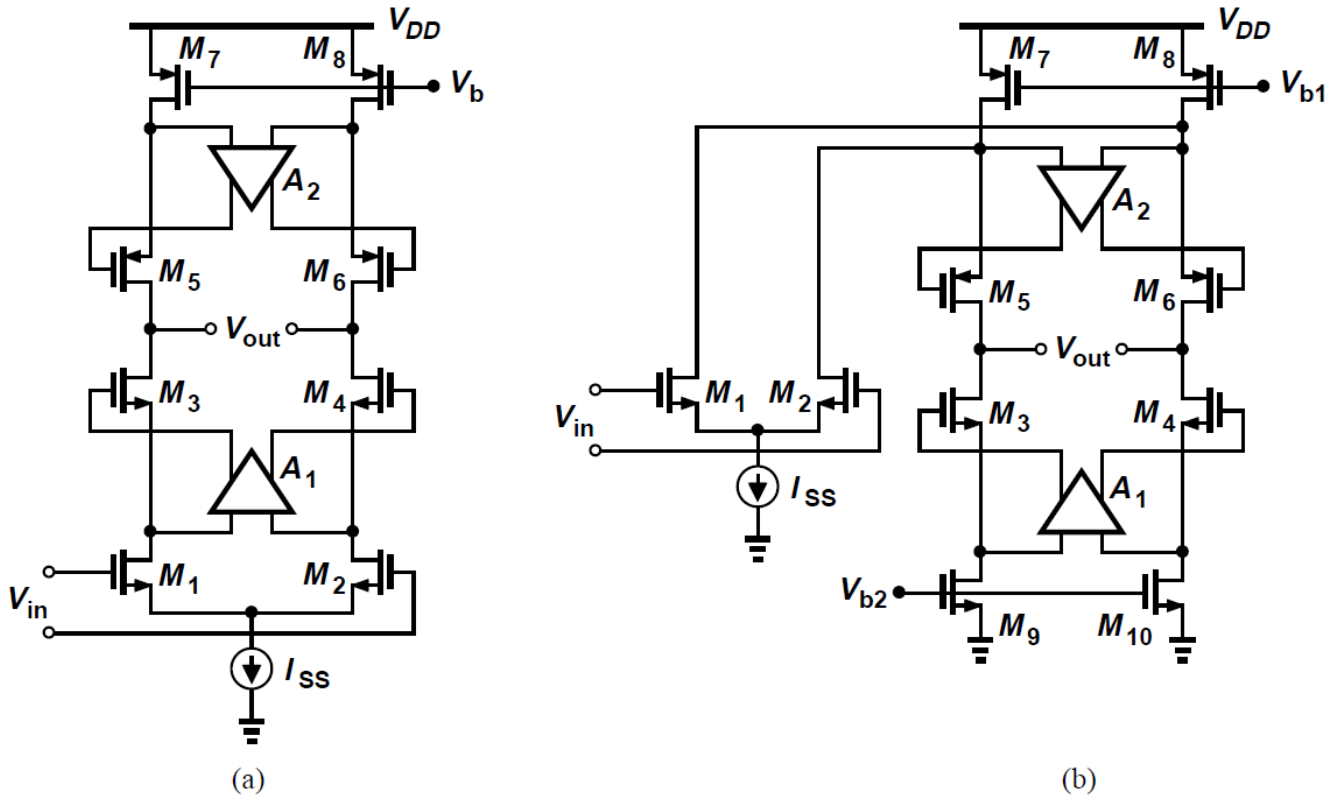
- Simplest is a common-source stage

$$|V_{out}/V_{in}| \approx g_{m1}r_{O1}g_{m2}r_{O2}(g_{m3}r_{O3}+1)$$

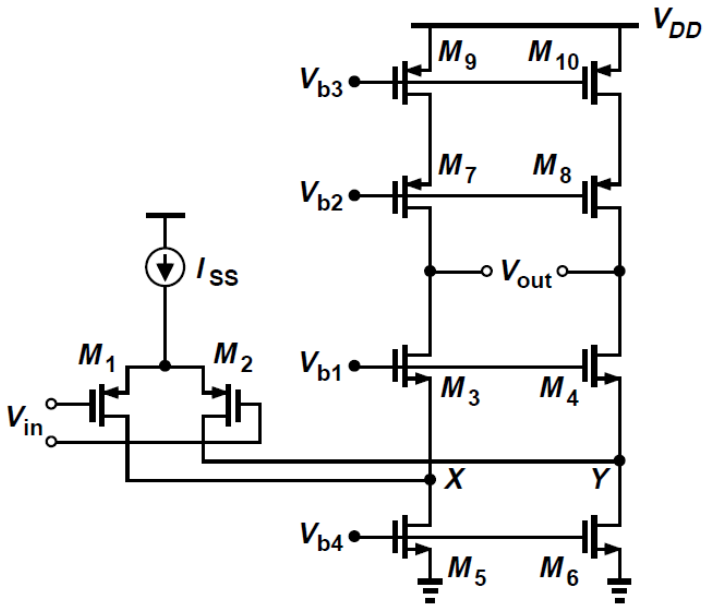


Gain Boosting in Signal Path and Load

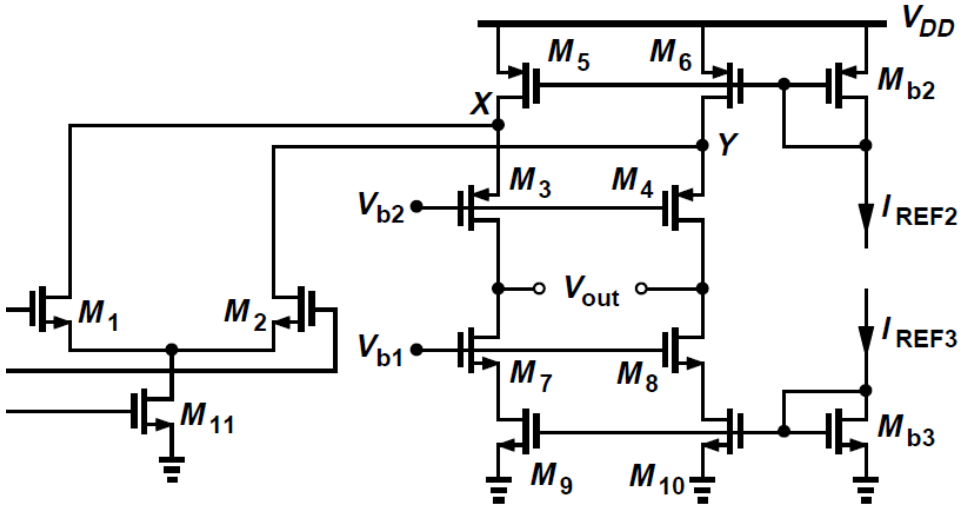
- Gain boosting can be utilized in the load current source
- To allow maximum swings, A2 employs NMOS-input



Gain Boosting Amp Choice



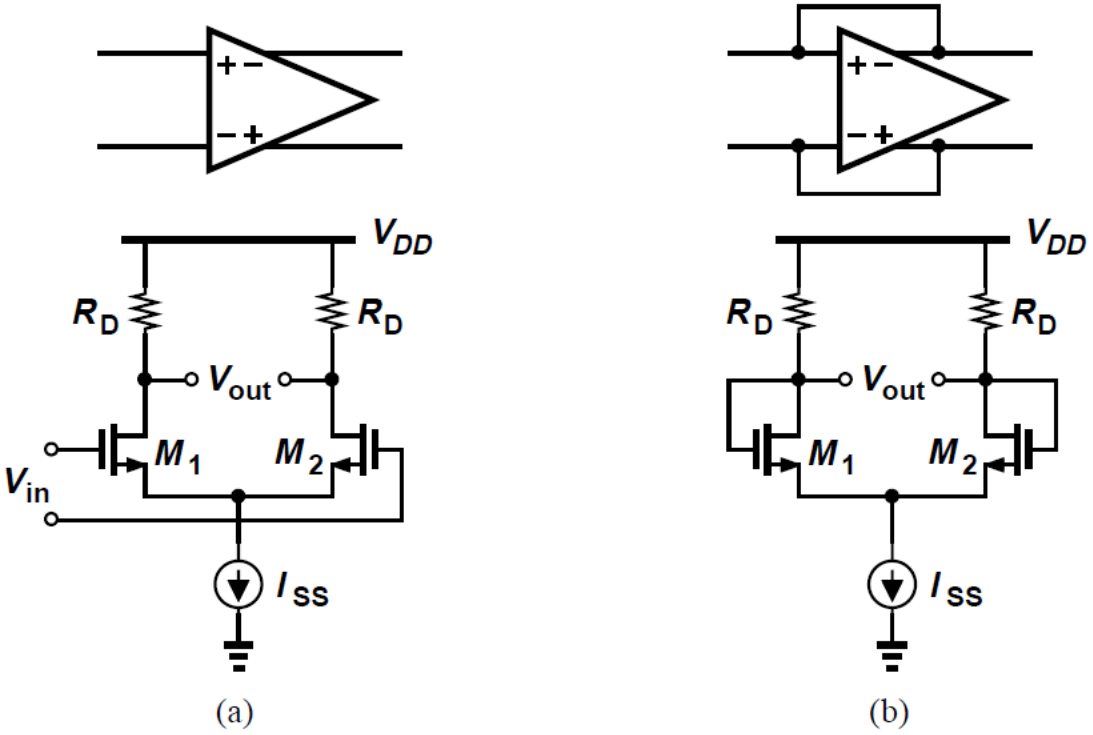
Good for Lower Common-Mode Input



Good for Higher Common-Mode Input

Fully Differential Amplifiers

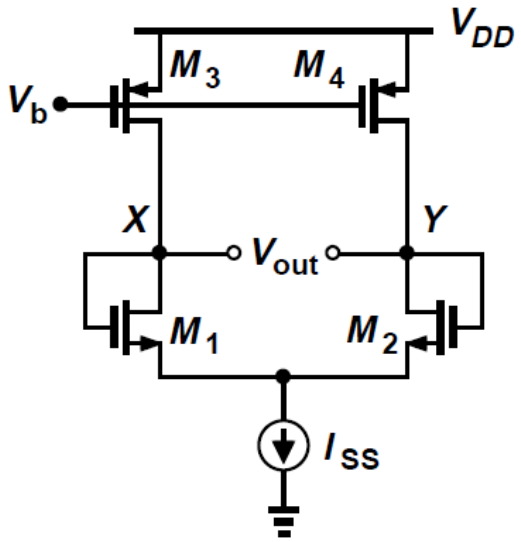
Fully Differential Amplifier



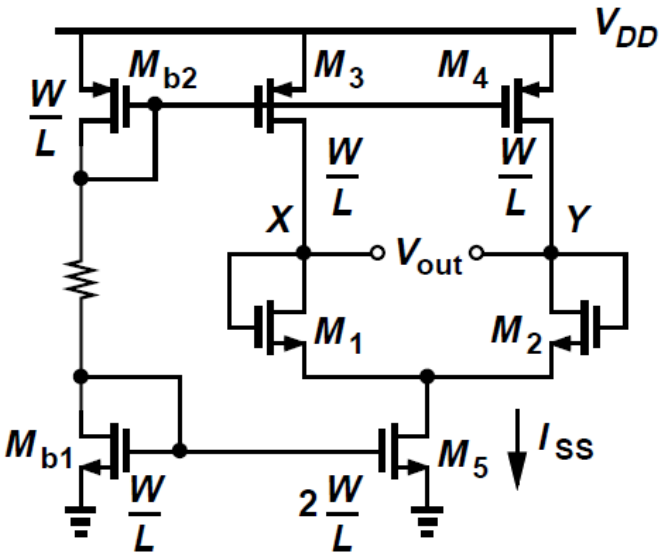
- $V_{cm(in)}$ and $V_{cm(out)}$: $V_{DD} - I_{SS}R_D/2$

Common-Mode Basic Concepts

- In fully-differential op amps, the output CM level is usually not well defined.
  - Case 1: $I_{D3,4} < I_{SS}/2$, Vx,Vy decreases, I_{ss} triode;
  - Case 2: In reverse, Vx,Vy increases, M3,M4 triode.



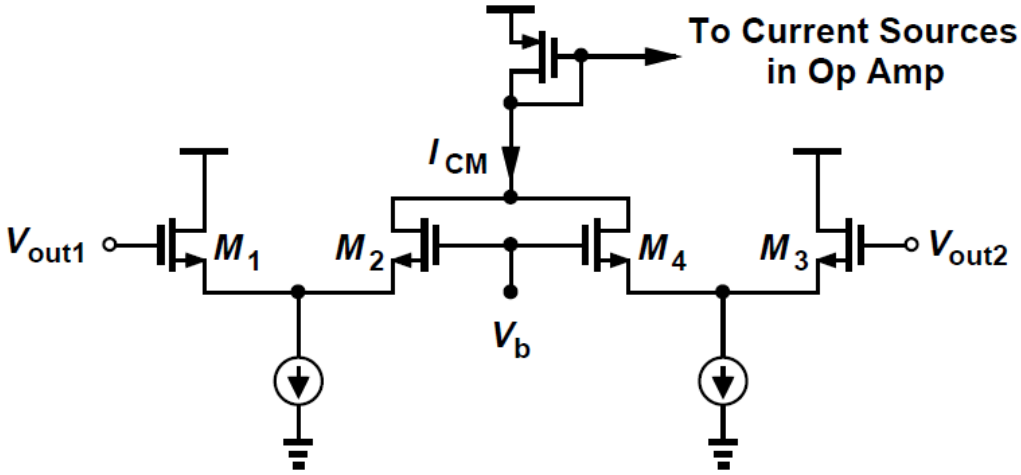
(a)



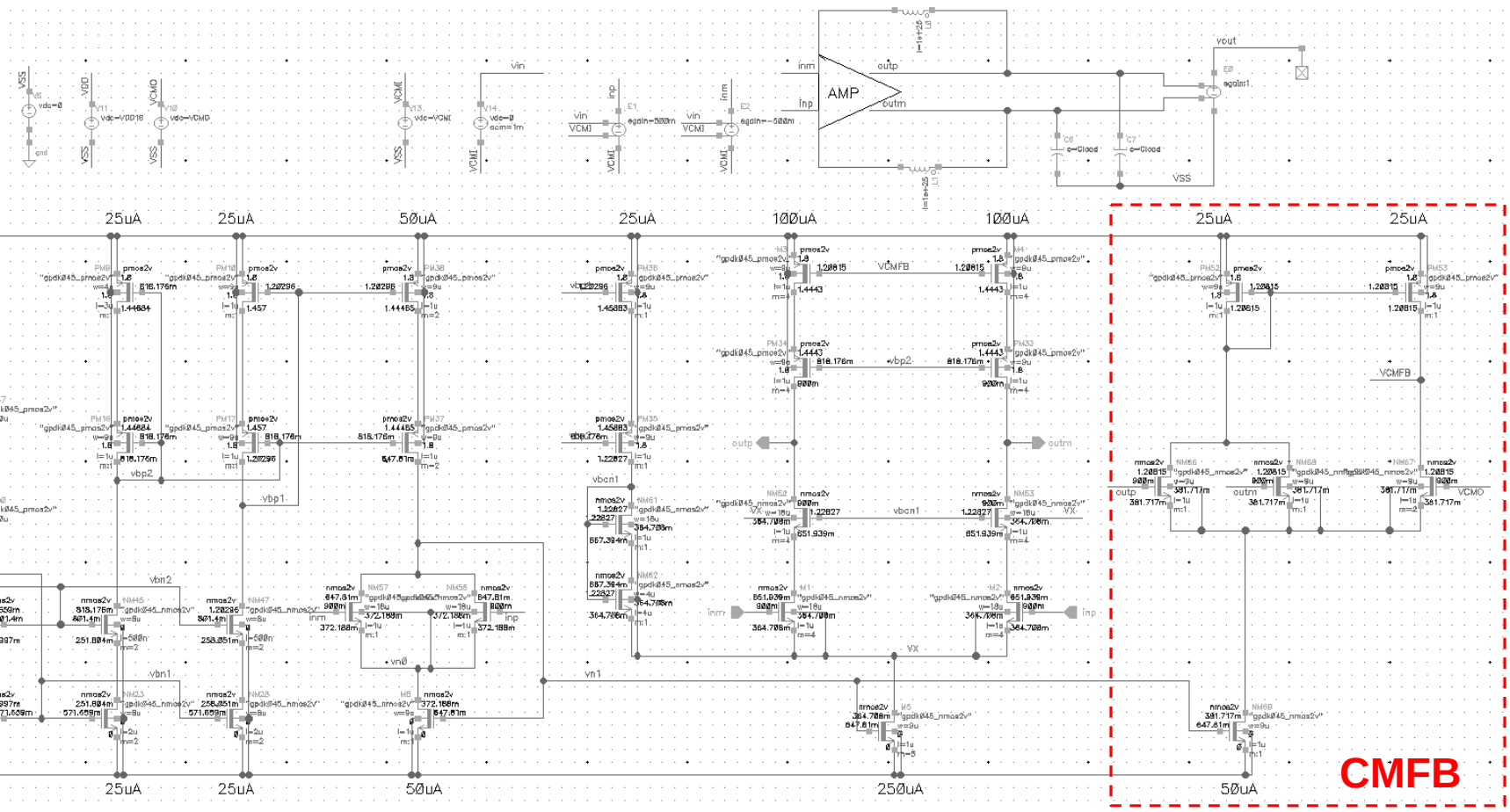
(b)

Differential Pair Common-Mode Sensing

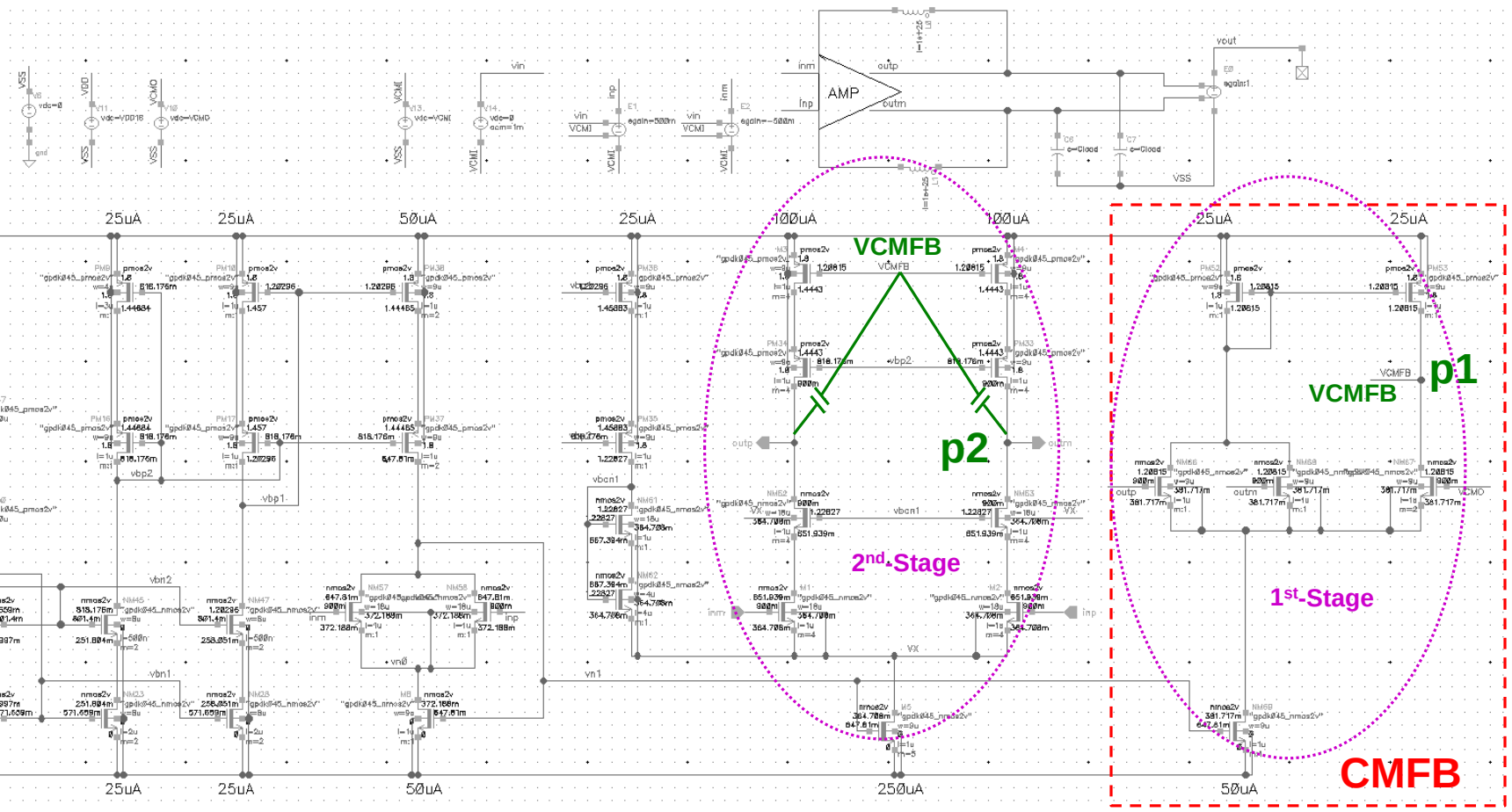
- $I_{CM} \propto V_{out1} + V_{out2}$ by small signal analysis
- Under Large swings situation, sensing is not valid due to large non-linearity.



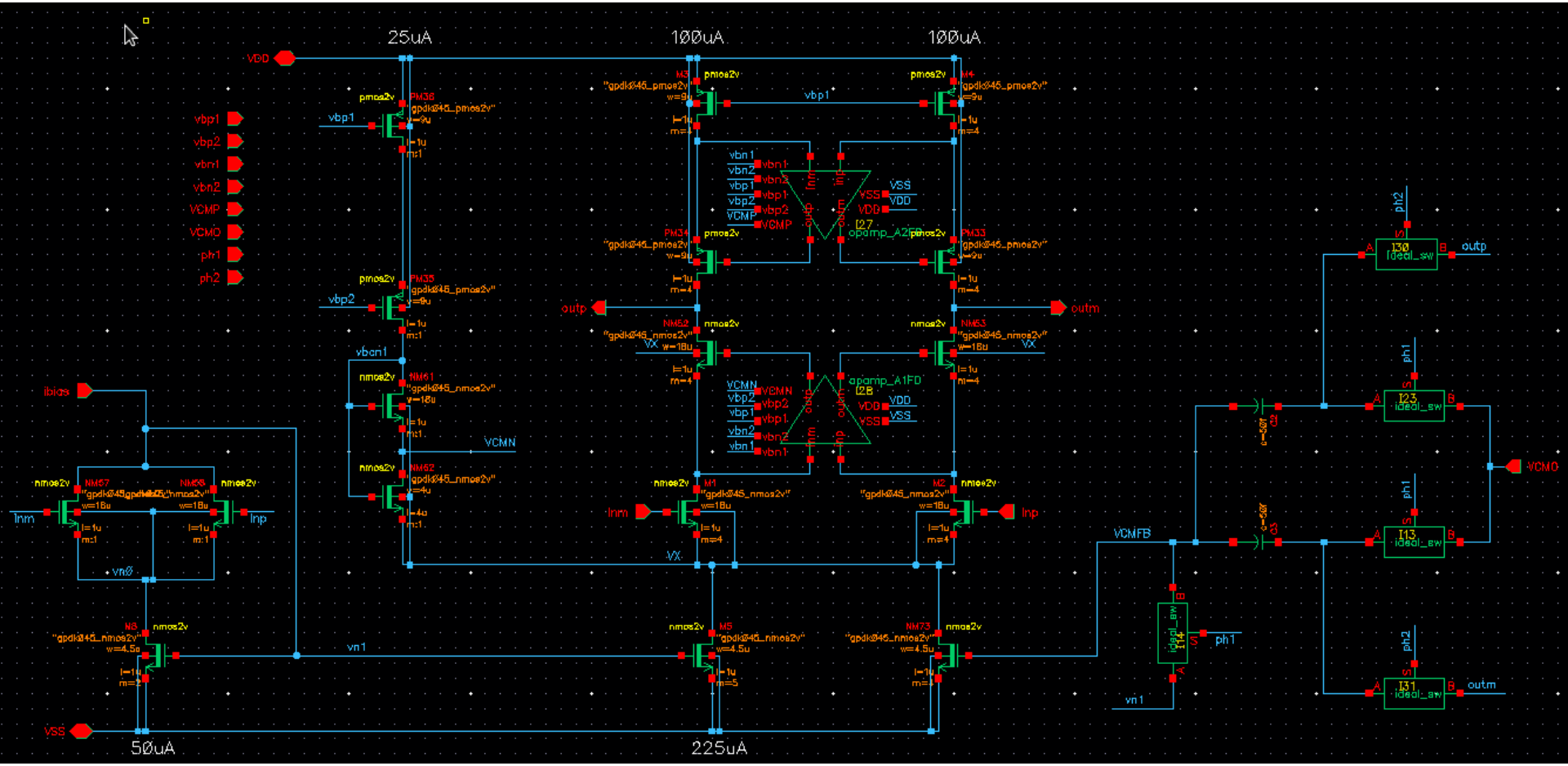
Fully Differential Telescopic OTA with CMFB



Common-Mode Loop → Two-Stage



Switched-Capacitor CMFB



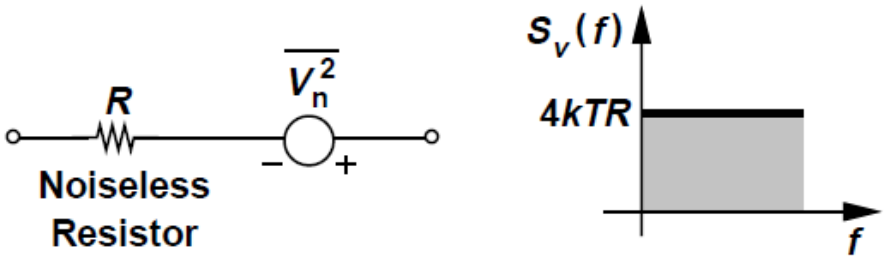
Noise

Resistor Thermal Noise

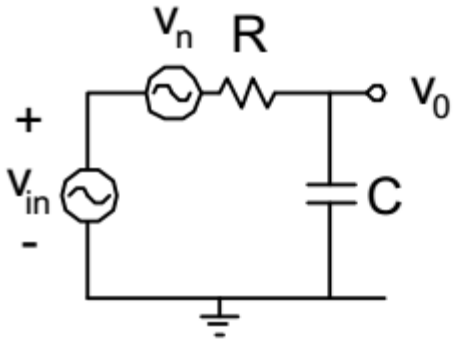
- Random motion of electrons in a conductor induces fluctuations in the voltage measured across it even though the average current is zero
- Thermal noise of a resistor *R* can be modeled by a series voltage source, with one-sided spectral density

$$S_v(f) = 4kTR, \quad f \geq 0$$

- Here, k = 1.38 X 10^{-23} J/K is the Boltzmann constant
- $S_V(f)$ is expressed in V^2/Hz, we also write $\overline{V_n^2} = 4kTR$
- For a 50-Ω resistor at T = 300 K, thermal noise is 8.28 X 10^{-19} V^2/Hz, or 0.91 nV/√Hz **1kohm-> 4 nV/√Hz**
- $S_V(f)$ is flat up to 100 THz, and is "white" for our purposes

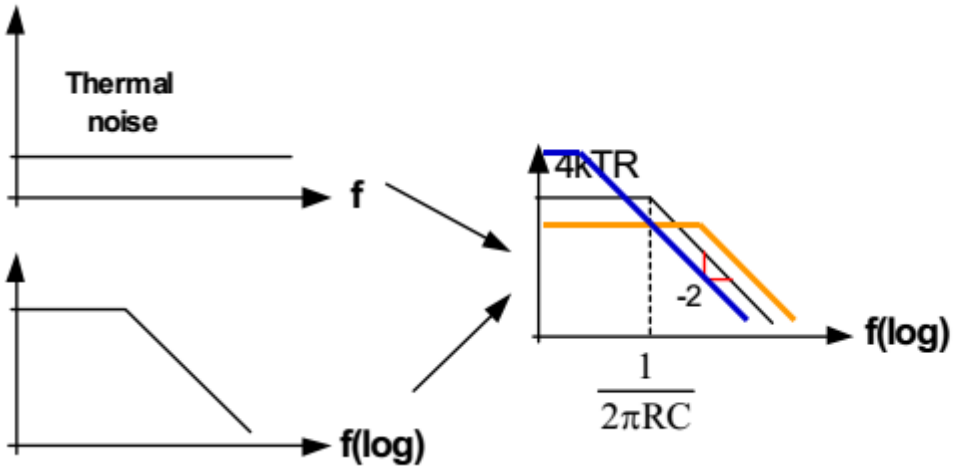


Noise generated by R, but depends on C



$$v_{total}^{\ 2} = \int_0^{\infty} \left(\left(\frac{1}{1+(\omega RC)^2} \right) (4kTR) \right) df = \frac{kT}{C}$$

To get more insight, lets have a closer look on the operations!



Notice that:
When R increases thermal noise increases too but the corner frequency decreases, leading to a constant area under the curves!

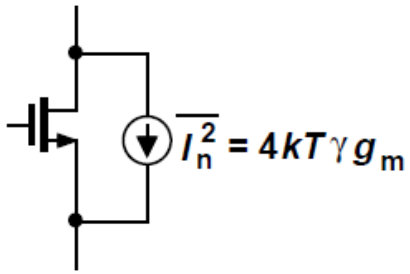
- *kT/C* noise can only be decreased by increasing C (if T is fixed)

MOSFET Thermal Noise

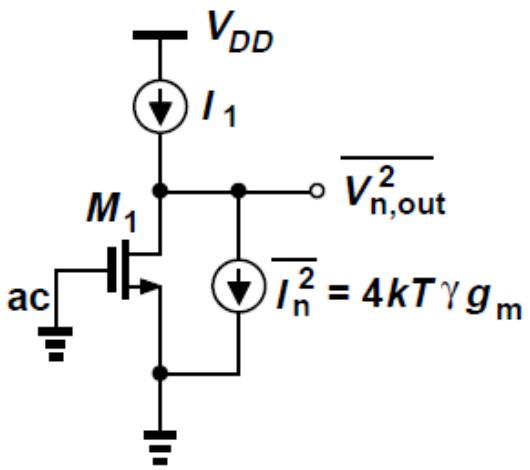
- MOS transistors exhibit thermal noise with the most significant source being the noise generated in the channel
- For long-channel MOS devices operating in saturation, the channel noise can be modeled by a current source connected between the drain and source terminals with a spectral density

$$\overline{I_n^2} = 4kT\gamma g_m$$

- The coefficient 'γ' (not the body effect coefficient) is derived to be 2/3 for long-channel transistors and is higher for submicron MOSFETs

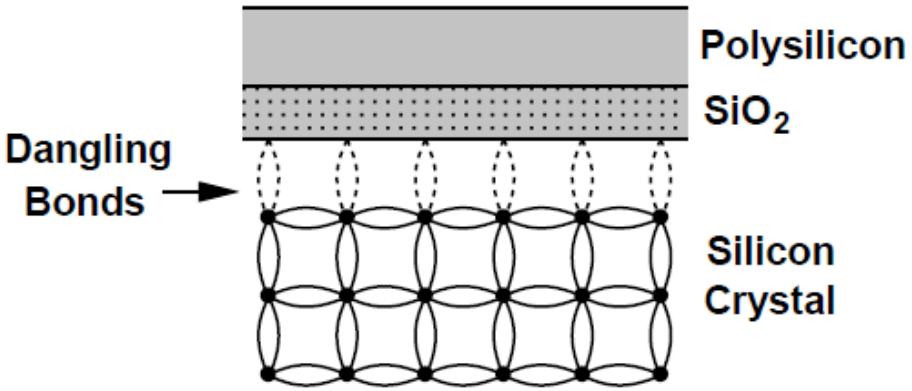


MOSFET Thermal Noise



- Noise current of a MOS transistor decreases if the transconductance drops
- Noise measured at the output of the circuit does not depend on where the input terminal is because input is set to zero for noise calculation
- The output resistance r_O does not produce noise because it is not a physical resistor

MOSFET Flicker Noise



- At the interface between the gate oxide and silicon substrate, many “dangling” bonds appear, giving rise to extra energy states
- Charge carriers moving at the interface are randomly trapped and later released by such energy states, introducing “flicker” noise in the drain current
- Other mechanisms in addition to trapping are believed to generate flicker noise

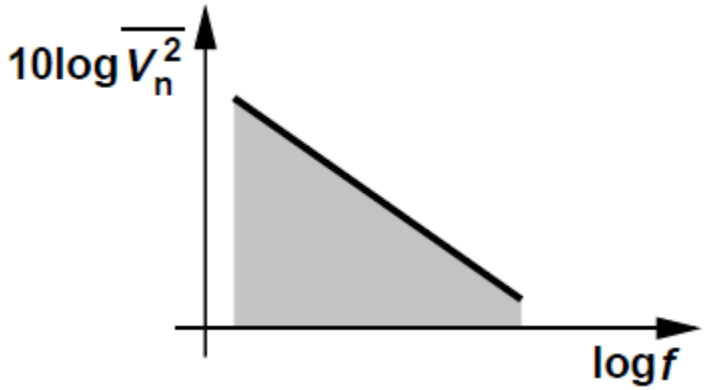
MOSFET Flicker Noise

- Average power of flicker noise cannot be predicted easily
- It varies depending on cleanness of oxide-silicon interface and from one CMOS technology to another
- Flicker noise is more easily modeled as a voltage source in series with the gate and in the saturation region, is roughly given by

$$\overline{V_n^2} = \frac{K}{C_{ox} W L} \cdot \frac{1}{f}$$

- *K* is a process-dependent constant on the order of $10^{-25}\ V^2F$

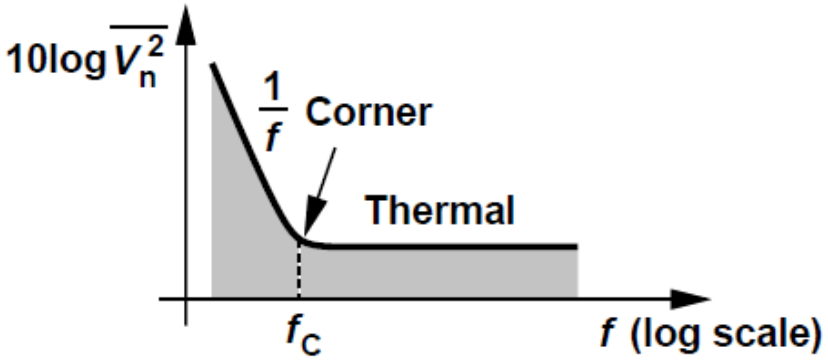
MOSFET Flicker Noise



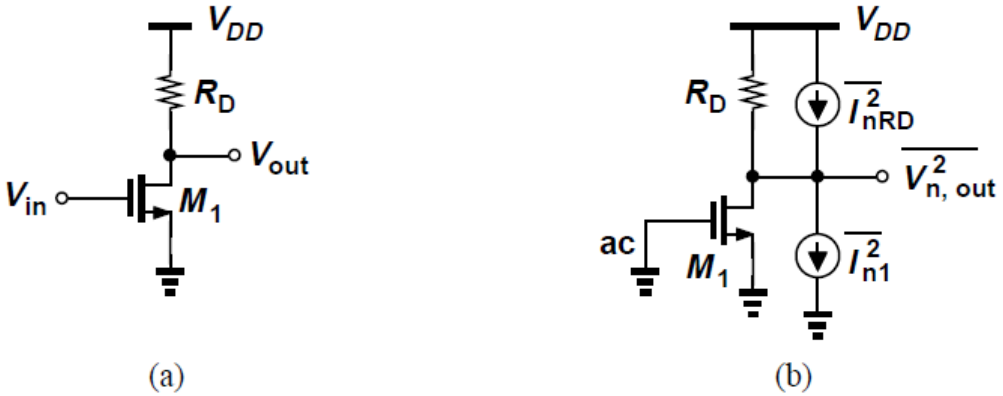
- The noise spectral density is inversely proportional to frequency
  - Trap and release phenomenon occurs at low frequencies more often
- Flicker noise is also called "*1/f*" noise
- To reduce *1/f* noise, device *area* must be increased
- Generally, PMOS devices exhibit less *1/f* noise than NMOS transistors
  - Holes are carried in a "buried" channel, at some distance from the oxide-silicon interface

Flicker Noise Corner Frequency

- At low frequencies, the flicker noise power approaches infinity
- Intersection point of thermal noise and flicker noise spectral densities is called “corner frequency” f_C



Representation of Noise in Circuits Example



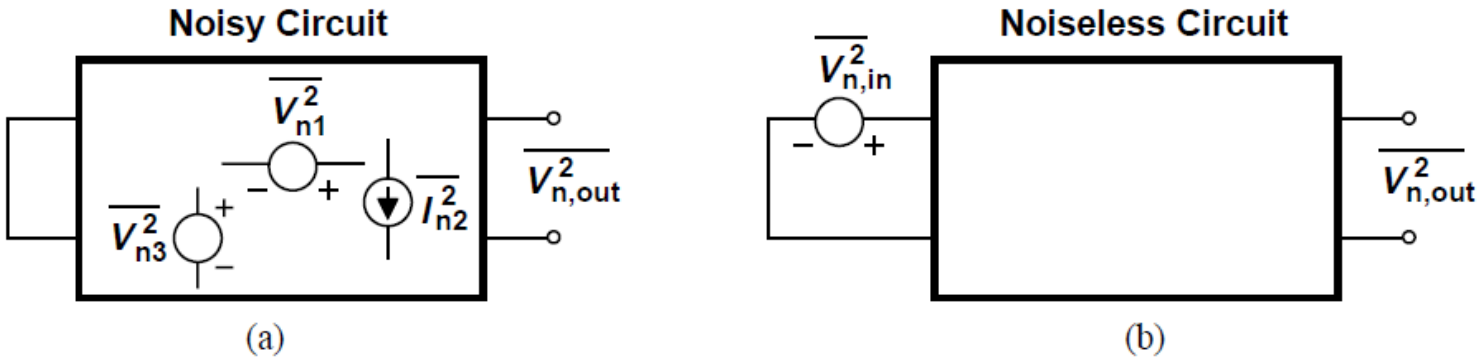
- To find: Total output noise voltage of common-source stage [Fig. (a)]
- Follow noise analysis procedure described earlier
- Thermal and flicker noise of M1 and thermal noise of RD are modeled as current sources [Fig. (b)]

$$\overline{I^2_{n,th}} = 4kT\gamma g_m \qquad \overline{I^2_{n,1/f}} = Kg_m^2/(C_{ox}WLf) \qquad \overline{I^2_{n,RD}} = 4kT/R_D$$

- Output noise voltage per unit bandwidth, added as power quantities is

$$\overline{V^2_{n,out}} = \left(4kT\gamma g_m + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 + \frac{4kT}{R_D}\right)R_D^2$$

Input-Referred Noise

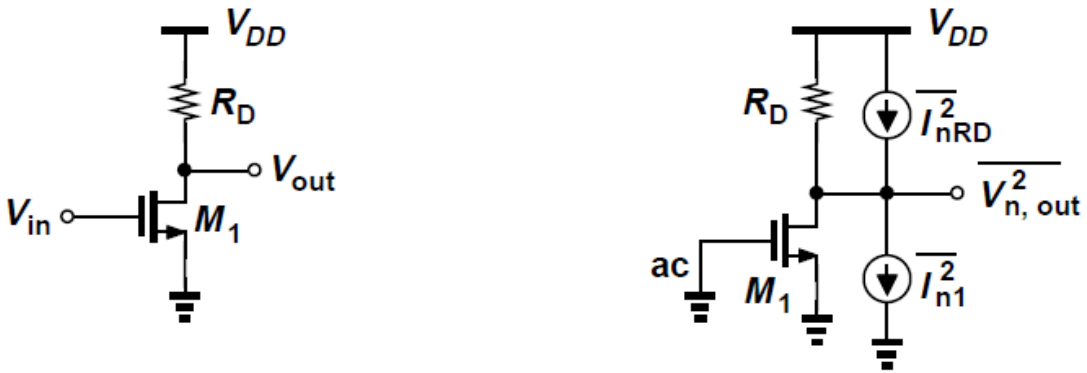


- Input-referred noise represents the effect of all noise sources in the circuit by a single source $\overline{V_{n,in}^2}$, at the input such that the output noise in Fig. (b) is equal to that in Fig. (a)
- If the voltage gain is A_v, then we must have

$$\overline{V_{n,out}^2} = A_v^2 \overline{V_{n,in}^2}$$

- The input-referred noise voltage in this simple case is simply the output noise divided by the gain squared.

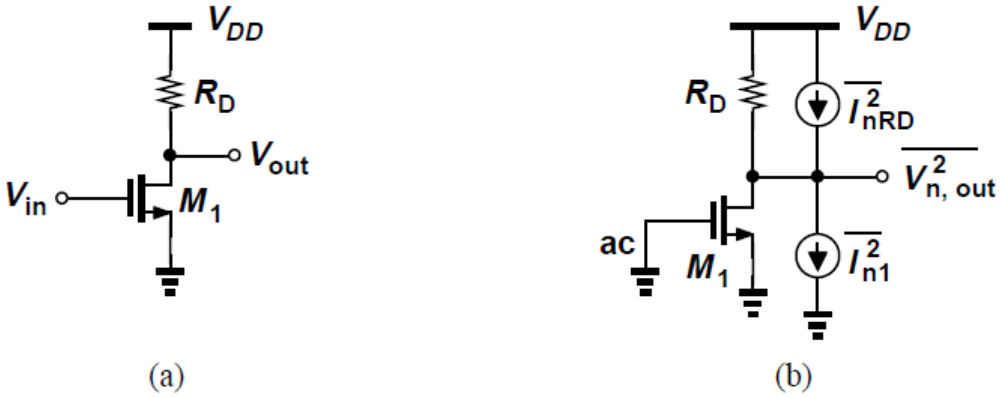
Input-Referred Noise Example



- For the simple CS stage, the input-referred noise voltage is given by

$$\begin{aligned}\overline{V_{n,in}^2} &= \frac{\overline{V_{n,out}^2}}{A_v^2} \\ &= \left(4kT\gamma g_m + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 + \frac{4kT}{R_D}\right) R_D^2 \frac{1}{g_m^2 R_D^2} \\ &= 4kT\frac{\gamma}{g_m} + \frac{K}{C_{ox}WL}\cdot\frac{1}{f} + \frac{4kT}{g_m^2 R_D}.\end{aligned}$$

Common-Source Noise at the Output



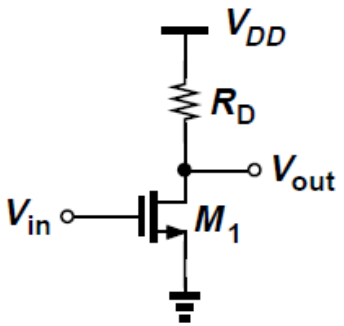
$$\overline{I^2_{n,th}} = 4kT\gamma g_m$$

$$\overline{I^2_{n,1/f}} = K g_m^2/(C_{ox}WLf)$$

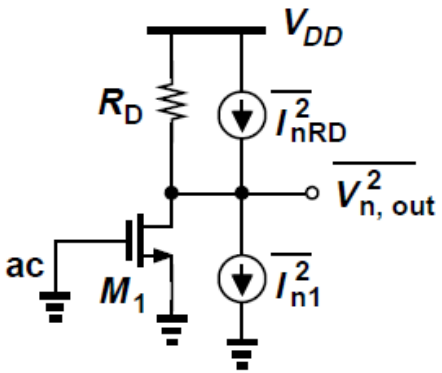
$$\overline{I^2_{n,RD}} = 4kT/R_D$$

$$\overline{V^2_{n,out}} = \left(4kT\gamma g_m + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 + \frac{4kT}{R_D}\right)R_D^2$$

Common-Source Input-Referred Noise



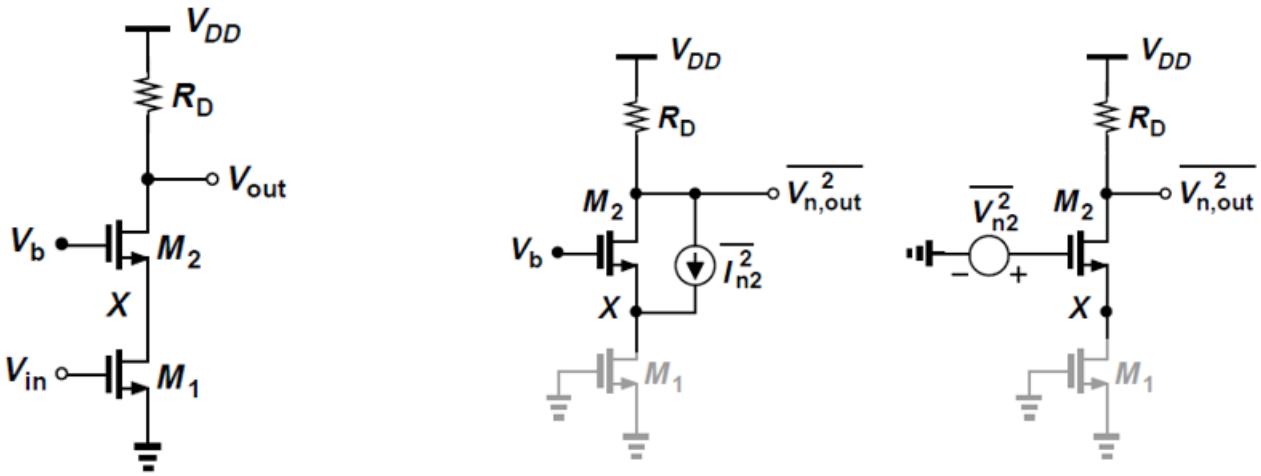
(a)



(b)

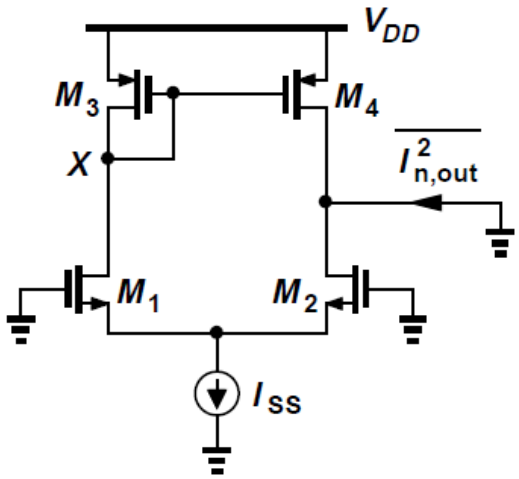
$$\begin{aligned}
\overline{V_{n,in}^2} &= \frac{\overline{V_{n,out}^2}}{A_v^2} \\
&= \left(4kT\gamma g_m + \frac{K}{C_{ox}WL}\cdot\frac{1}{f}\cdot g_m^2 + \frac{4kT}{R_D}\right) R_D^2 \frac{1}{g_m^2 R_D^2} \\
&= 4kT\frac{\gamma}{g_m} + \frac{K}{C_{ox}WL}\cdot\frac{1}{f} + \frac{4kT}{g_m^2 R_D}.
\end{aligned}$$

Cascode Stage



- M_2 contributes negligibly to noise at the output,
- Voltage gain from V_{n2} to the output is small if impedance at node X is large

Noise in Five-Transistor OTA



- The noise current of M_3 primarily circulates through the diode-connected impedance $1/g_{m3}$, producing a voltage at the gate of M_4 with spectral density $4kT\gamma/g_{m3}$

- This noise is multiplied by g_{m4}^2 as it emerges from the drain of M_4; the noise current of M_4 also flows directly through the output short-circuit, thus

$$\overline{I^2_{n,out}} = 4kT\gamma(2g_{m1,2} + 2g_{m3,4})$$

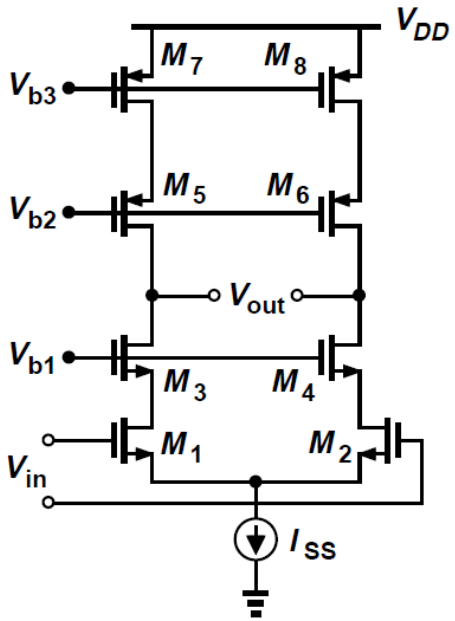
- Multiplying this noise by $R^2_{out} \approx (r_{O1,2}||r_{O3,4})^2$ and dividing the result by $A_v^2 = G_m^2 R^2_{out}$, the total input-referred noise is

$$\overline{V^2_{n,in}} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g^2_{m1,2}}\right)$$

Noise in Telescopic OPAMP

- At low frequency the cascode devices contribute negligible noise

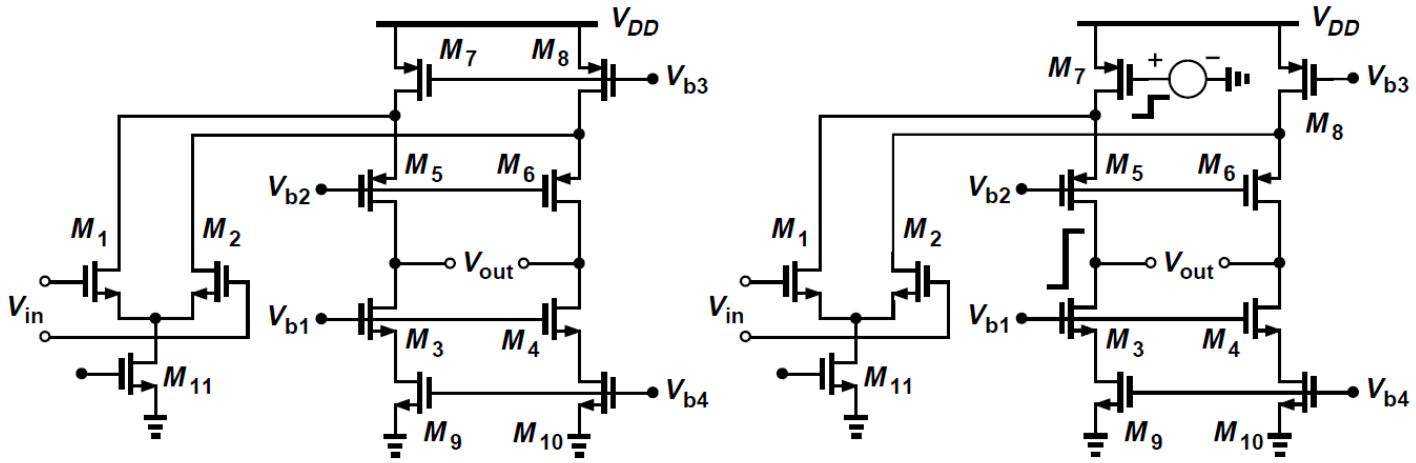
$$\overline{V_n^2} = 4kT\left(2\frac{\gamma}{g_{m1,2}} + 2\frac{\gamma g_{m7,8}}{g_{m1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{7,8}C_{ox}f}\frac{g_{m7,8}^2}{g_{m1,2}^2}$$



Noise in Folded-Cascode OPAMP

- At low frequency the cascode devices contribute negligible noise

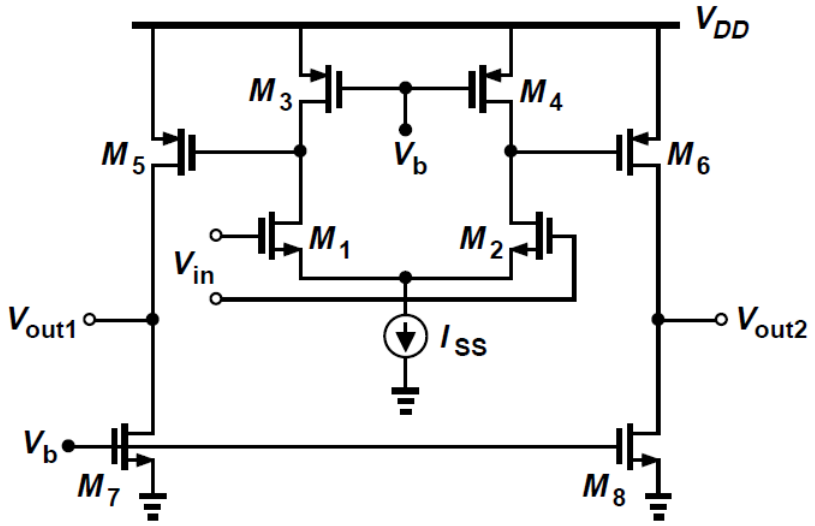
$$\overline{V_{n,int}^2} = 8kT\left(\frac{\gamma}{g_{m1,2}} + \gamma\frac{g_{m7,8}}{g_{m1,2}^2} + \gamma\frac{g_{m9,10}}{g_{m1,2}^2}\right)$$



Noise in Two-Stage OPAMP

- The noise in the second stage contributes negligible noise

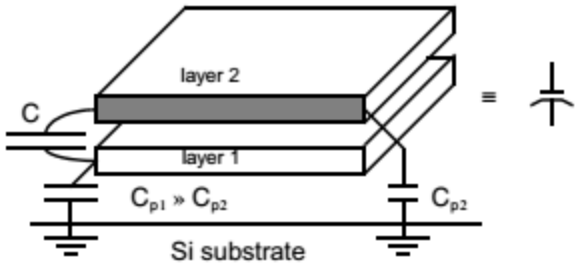
$$\overline{V_{n,tot}^2} = 8kT\gamma \frac{1}{g_{m1}^2}\left[g_{m1} + g_{m3} + \frac{g_{m5}+g_{m7}}{g_{m5}^2(r_{O1}\|r_{O3})^2}\right]$$



Switched-Capacitor Circuits

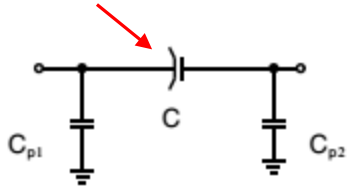
Basic Building Blocks of Switched-Capacitor Circuits

- OPAMP (OTA)
- Capacitor
- Switch
- Clock

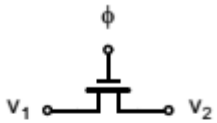


(a)

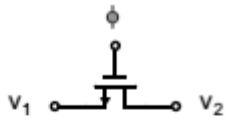
Bottom Plate



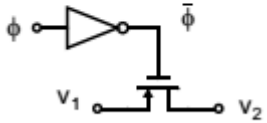
(b)



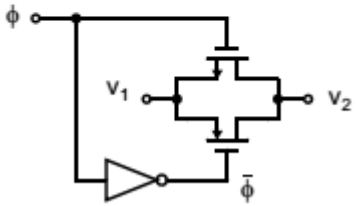
(a)



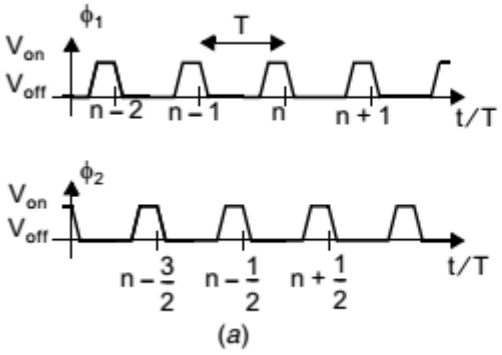
(b)



(c)

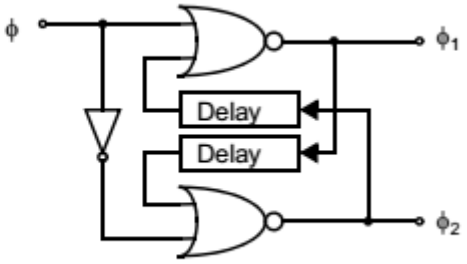


(d)



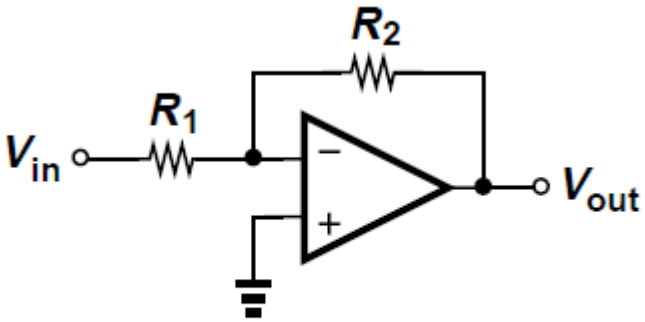
(a)

$f_s \equiv \frac{1}{T}$



(b)

General Considerations

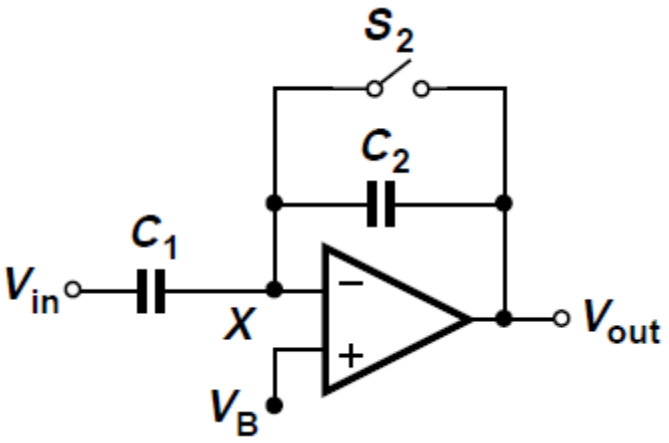


(a)

- For continuous-time amplifier, $V_{out}/V_{in} = -R_2/R_1$
- Difficult to implement in CMOS technology
- Typically, open-loop output resistance of CMOS op-amps is maximized to maximize A_v
- R_2 heavily drops open-loop gain, affecting precision

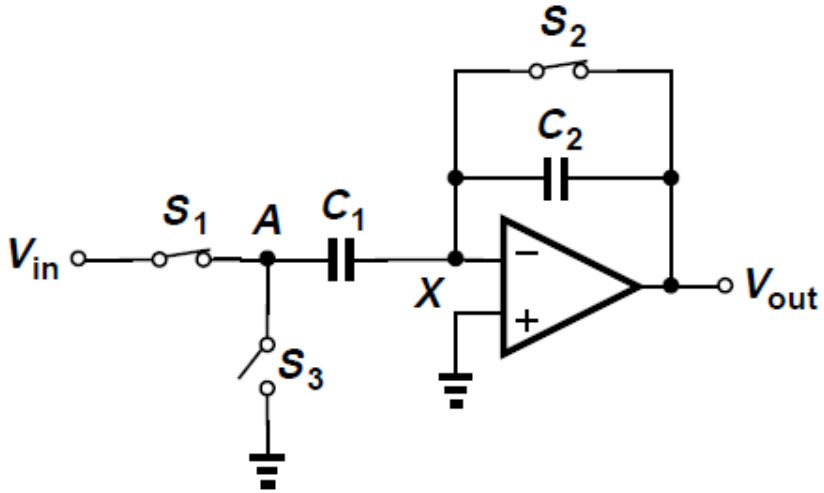
General Considerations

- R_F can be replaced by a switch
- S_2 is turned on to place op amp in unity gain feedback to force V_X equal to V_B, a suitable common-mode value
- When S_2 turns off, node X retains the voltage allowing amplification
- When S_2 is on, circuit does not amplify V_{in}

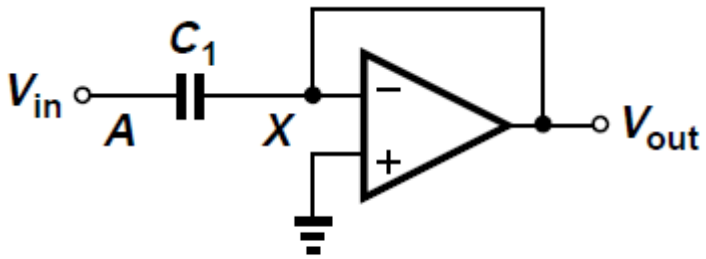


S2 status	Phase
On	Reset OTA or Sample input
Off	Amplify

General Considerations



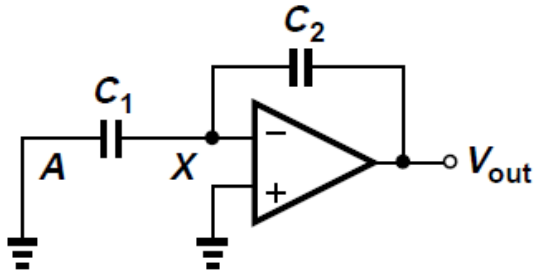
S_1, S_2 on, S_3 off



(a)

Sampling Phase

S_1, S_2 off, S_3 on

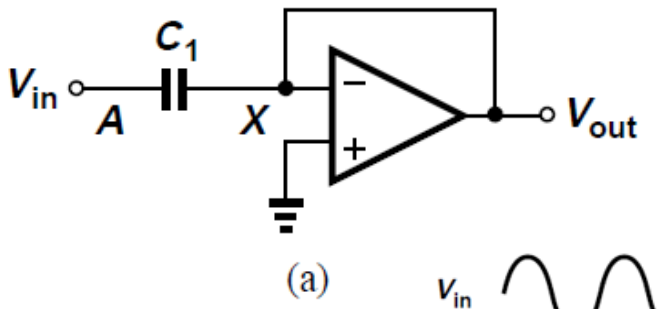


(b)

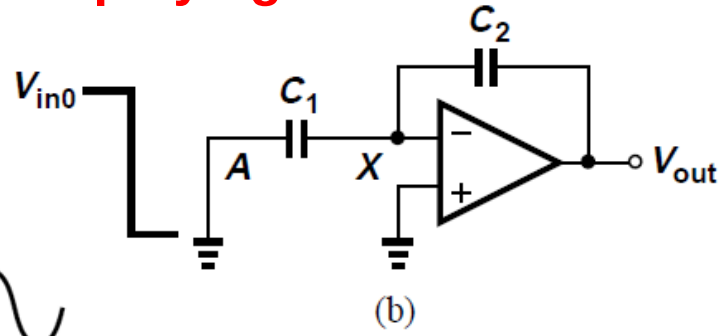
Amplifying Phase

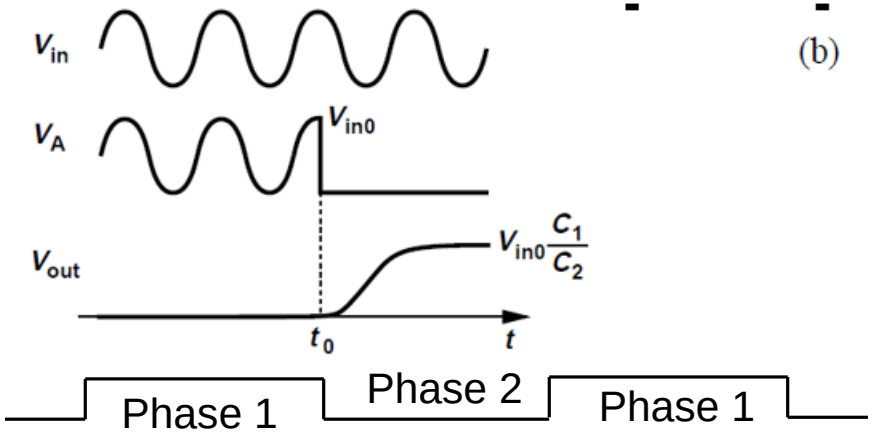
General Considerations

Sampling Phase



Amplifying Phase

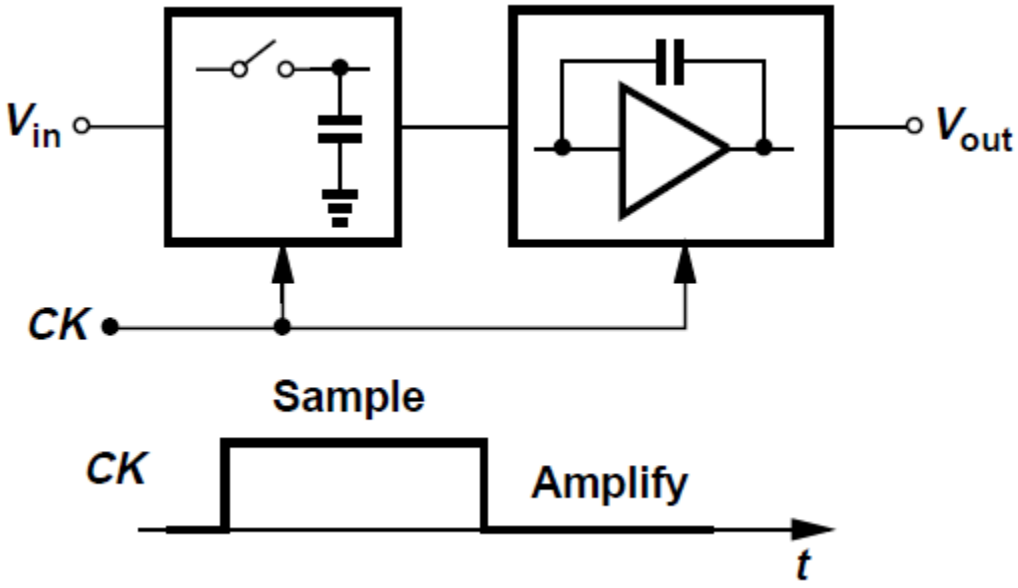




- Phase 1: Samples the input
- Phase 2: Amplify the signal
- *During Phase 2, V_A* changes from V_{in} to *0*, therefore V_{out} must change from zero to $V_{in0}C_1/C_2$

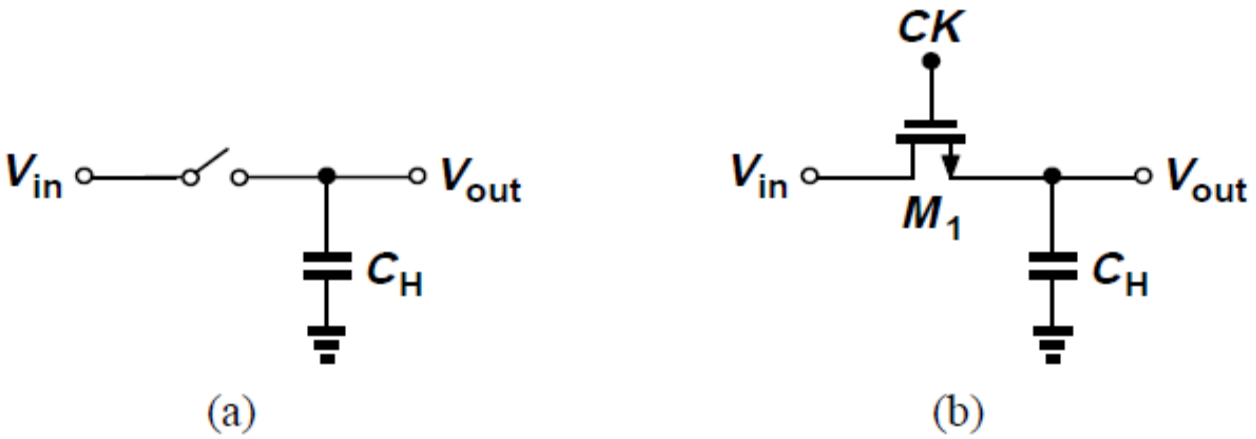
General Considerations

- Switched-capacitor amplifiers operate in two phases: Sampling and Amplification
- Clock needed in addition to analog input V_{in}

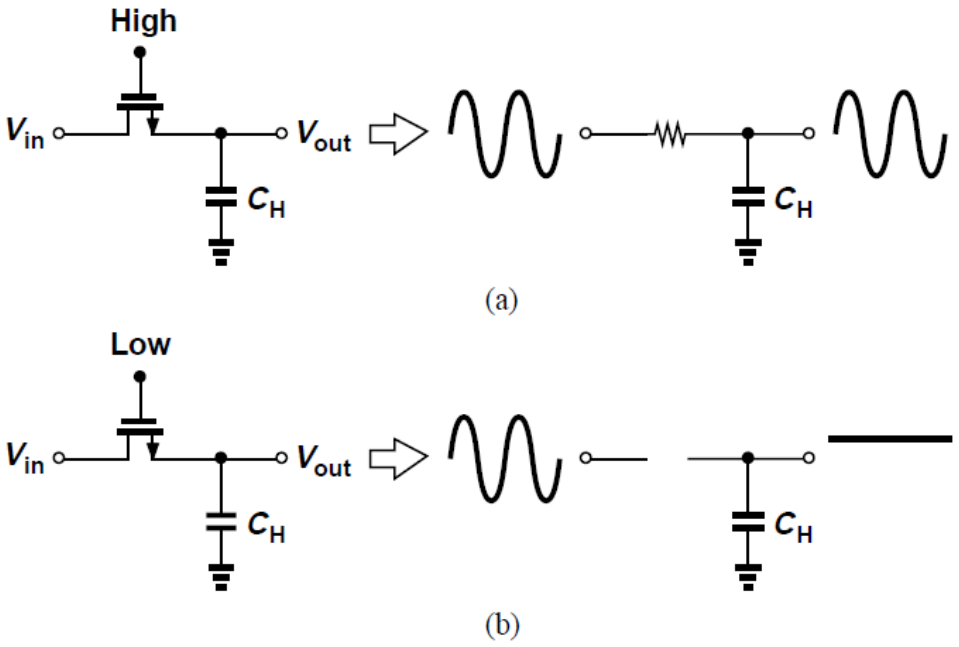


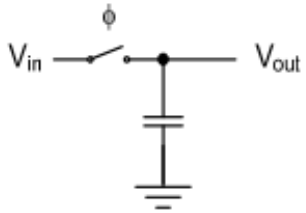
MOSFET as Switches

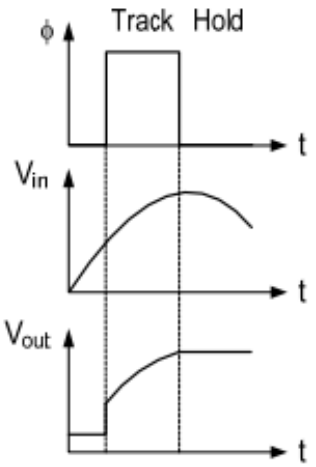
- Sampling circuit consists of a switch and a capacitor [Fig. (a)]
- MOS transistor can function as switch [Fig. (b)] since it can be on while carrying zero current



MOSFET as Switches

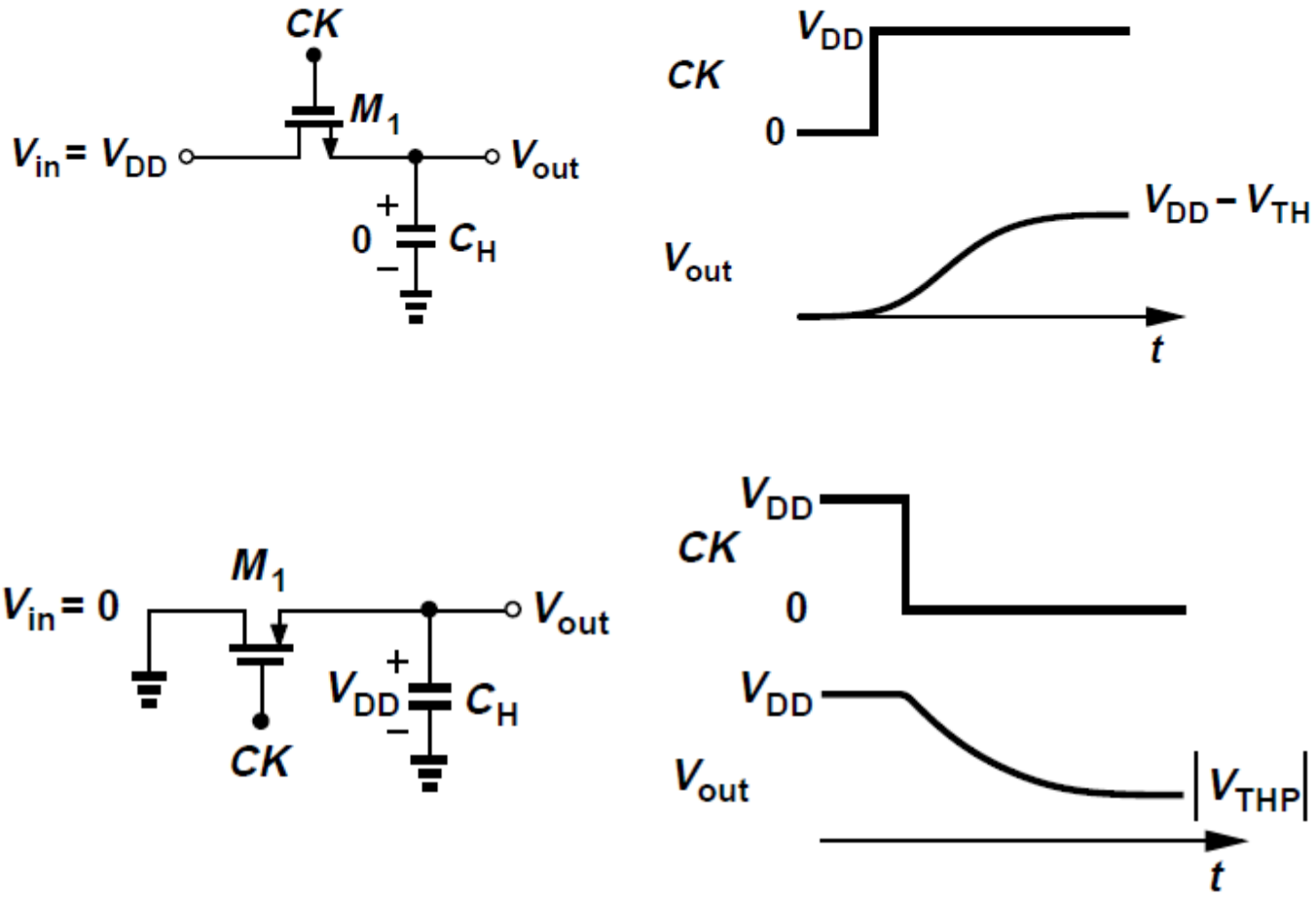






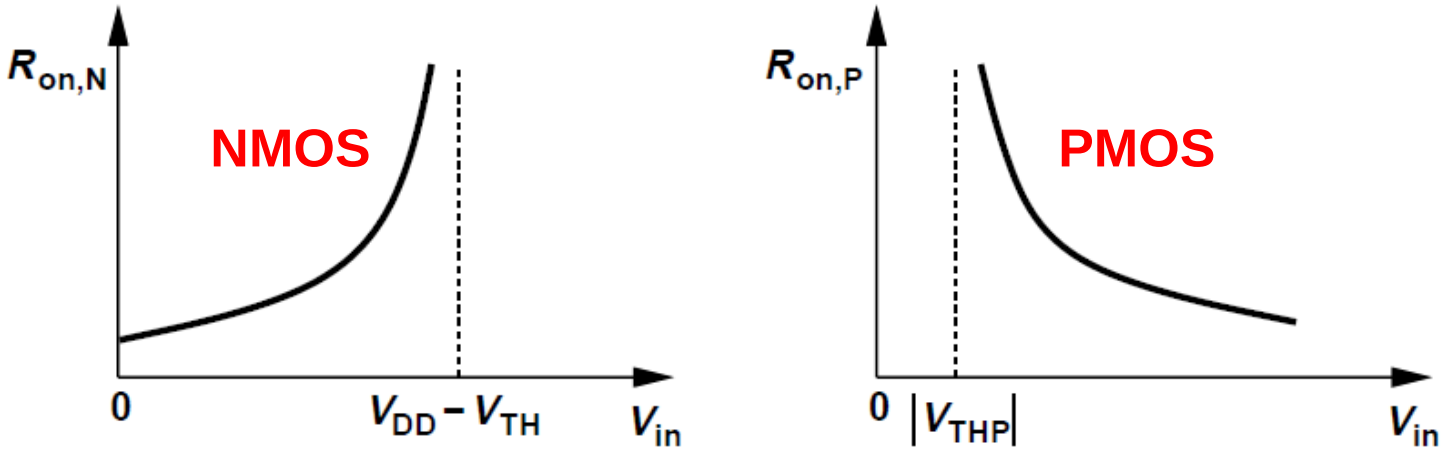
- When switch is on [Fig. (a)], V_{out} follows V_{in}
- When switch is off [Fig. (b)], V_{out} remains constant
- Circuit “tracks” signal when *CK* is high and “freezes” instantaneous value of V_{in} across C_H when *CK* goes low

MOSFET as Switches



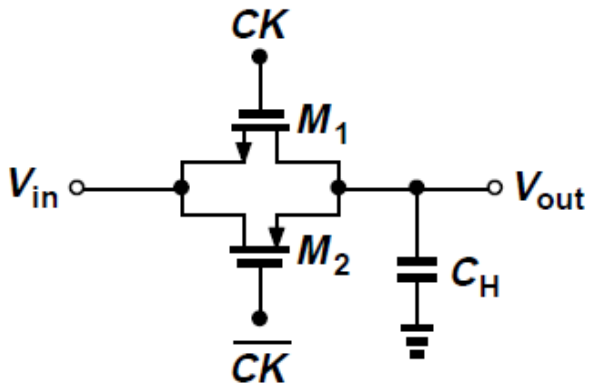
MOSFET as Switches: Speed Considerations

- Sampling speed is given by two factors: switch on-resistance and sampling capacitance
- For higher speed, large aspect ratio and small capacitance are needed
- On-resistance also depends on input level for both NMOS and PMOS

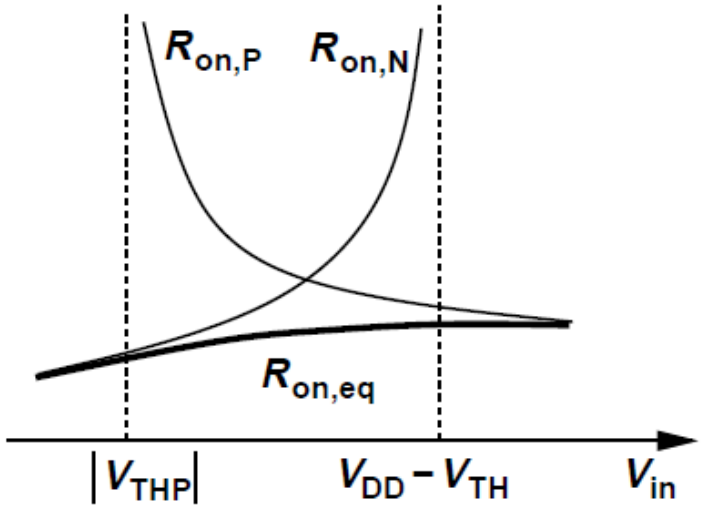


MOSFET as Switches: Speed Considerations

- To allow greater input swings, we can use “complementary” switches, requiring complementary clocks [Fig. (a)]
- Equivalent on-resistance shows following behavior [Fig. (b)], revealing much less variation



(a)

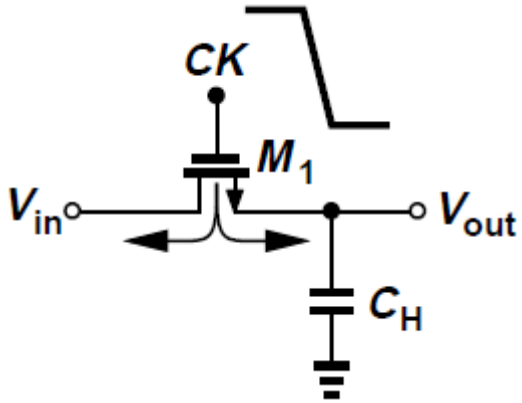


(b)

MOSFET as Switches: Precision Considerations

- Speed trades with precision
- Channel Charge Injection:
- For MOSFET to be on, a channel must exist at the oxide-silicon interface
- Assuming $V_{in} \approx V_{out}$, total charge in the inversion layer is

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$



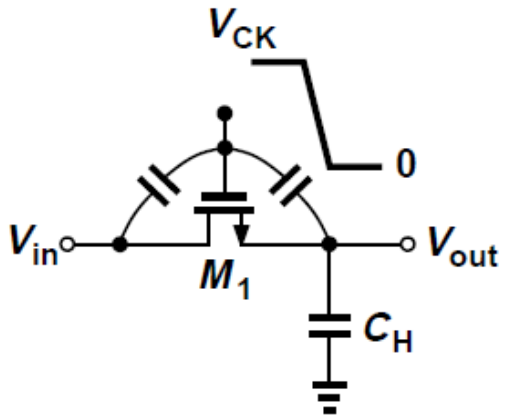
- When switch turns off, Q_{ch} exits through the source and drain terminals ("channel charge injection")

MOSFET as Switches: Precision Considerations

- Clock Feedthrough:
- MOS switch couples clock transitions through C_{GD} or C_{GS}
- Sampled output voltage has error due to this given by

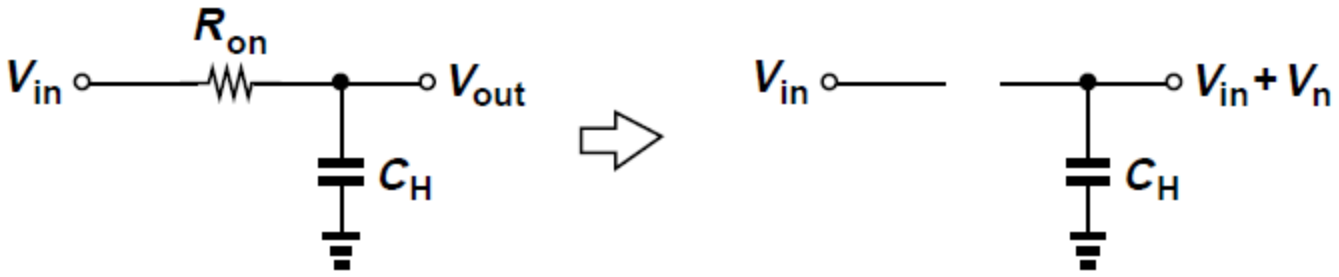
$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov}+C_H}$$

- C_{ov} is the overlap capacitance per unit width
- Error ΔV is independent of input level, manifests as constant offset in the input/output characteristic

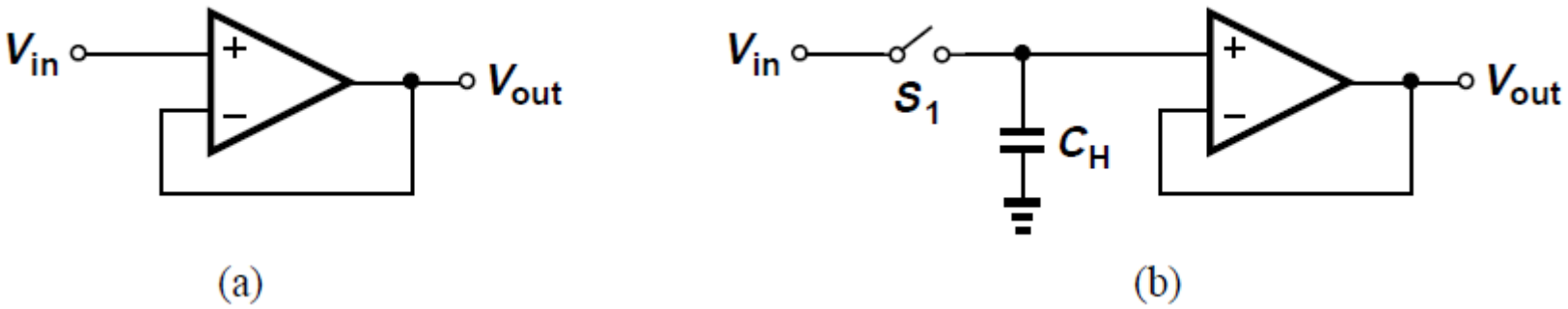


MOSFET as Switches: Precision Considerations

- kT/C Noise:
- Resistor charging a capacitor gives a total RMS noise voltage of $\sqrt{kT/C}$.
- On resistance of switch introduces thermal noise at output which is stored on the capacitor when switch turns off
- RMS voltage of sampled noise is still approximately equal to $\sqrt{kT/C}$.

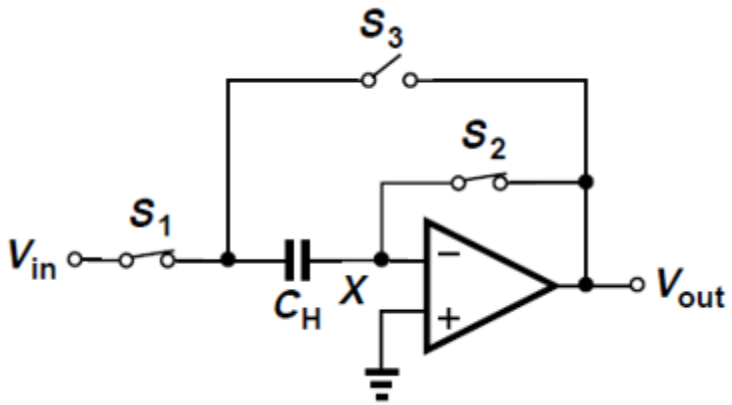


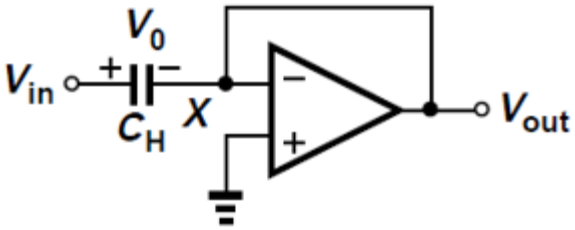
Unity-Gain Sampler / Buffer



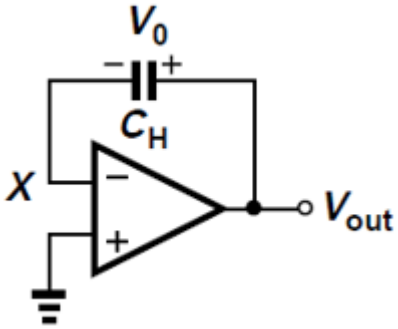
- For discrete-time applications, unity-gain amplifier [Fig. (a)] requires a sampling circuit [Fig. (b)]
- Accuracy limited by input-dependent charge injected by S_1 onto C_H

Unity-Gain Sampler / Buffer





Sample



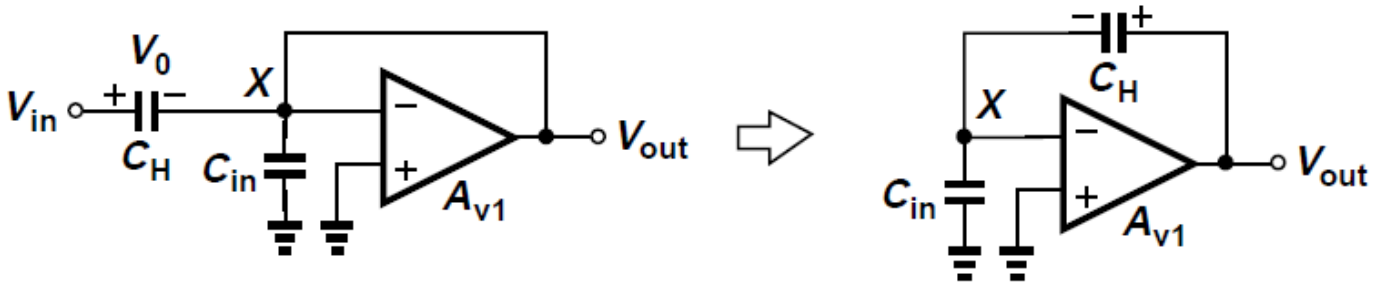
Amplify

Unity-Gain Sampler / Buffer

Precision Considerations:

- Output in amplification mode

Flip Around Sample & Hold

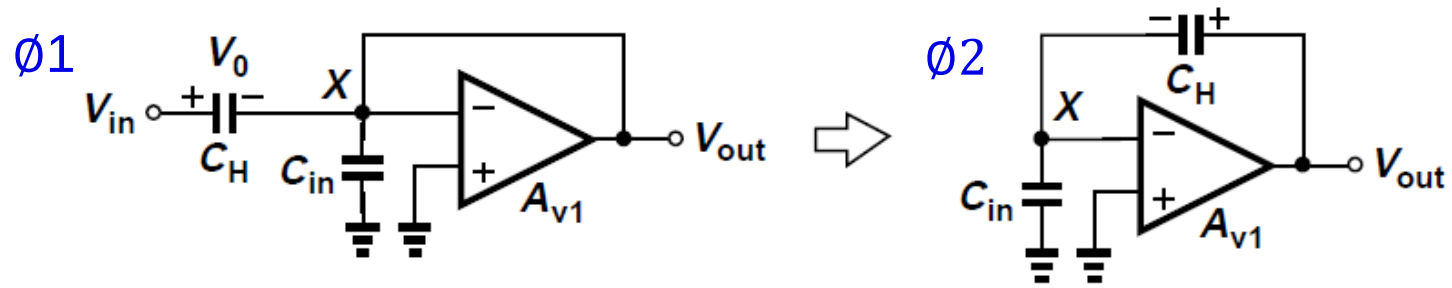


$$V_{out} = \frac{V_0}{1 + \frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H} + 1\right)}$$

$$\approx V_0\left[1 - \frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H} + 1\right)\right]$$

Derive this using charge conservation

Unity-Gain Sampler / Buffer



Charge conservation during Ø1 and Ø2

During Ø1, total charge at node X is $Q1 = C_H(0-V_{in})$

During Ø2, total charge at node X is $Q2 = C_{in}V_x + C_H(V_x-V_{out})$

Let Q1 = Q2

$-V_{in}C_H = C_{in}V_x + C_H(V_x-V_{out}) = (C_{in} + C_H)V_x - C_HV_{out}$

$V_x(-A_{v1}) = V_{out}$

$-V_{in}C_H = (C_{in} + C_H)(-V_{out}/A_{v1}) - C_HV_{out}$

$V_{in}C_H = (C_{in} + C_H)(V_{out}/A_{v1}) + C_HV_{out}$

$V_{in}C_H = [(C_{in} + C_H)/A_{v1} + C_H]V_{out}$

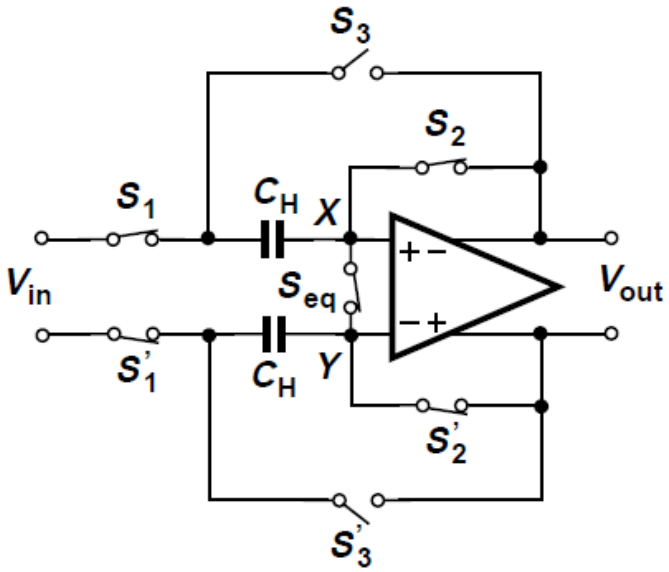
$V_{in} = [(C_{in} + C_H)/(C_HA_{v1}) + 1]V_{out}$

$V_{out}/V_{in} = 1/[(C_{in} + C_H)/(C_HA_{v1}) + 1] = 1/[1 + 1/(\beta A_{v1})]$

$$\beta = \frac{C_H}{C_H + C_{in}}$$

$$V_{out} \approx V_0\left[1 - \frac{1}{\beta A_{v1}}\right]$$ ← *To reduce gain error, Increase βA_V*

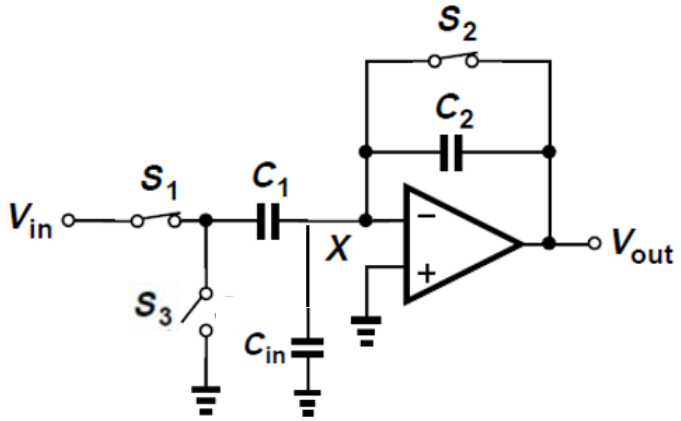
Differential Unity-Gain Sampler / Buffer



- Input-independent charge injected by S_2 can be cancelled by differential operation as shown
- Charge injected by S_2 and S_2' appears as common-mode disturbance at nodes *X* and *Y*
- Charge injection mismatch between S_2 and S_2' resolved by adding another switch S_{eq} that turns off slightly after S_2 and S_2', equalizing the charge at nodes *X* and *Y*

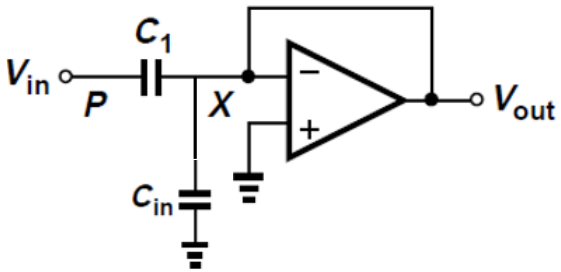
Non-Inverting Amplifier

- Precision Considerations:

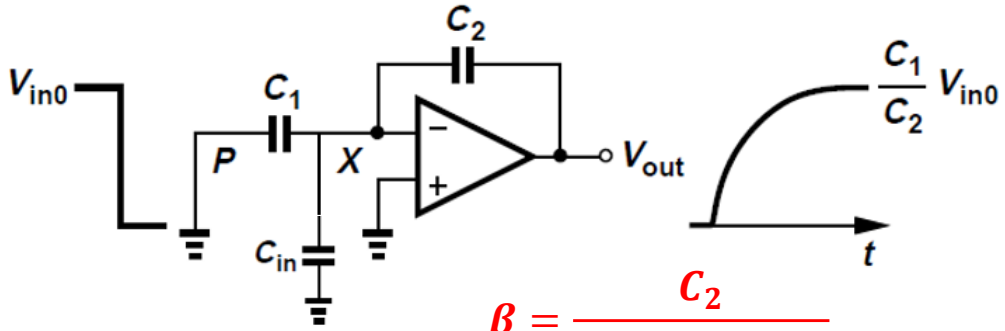


$$Q_1 = C_1(0 - V_{in})$$
$$Q_2 = (C_1 + C_{in})V_x + C_2(V_x - V_{out}) \qquad V_x = \frac{V_{out}}{-A}$$
$$Q_1 = Q_2$$
$$C_1(0 - V_{in}) = (C_1 + C_{in})V_x + C_2(V_x - V_{out}) = (C_1 + C_{in})(\frac{V_{out}}{-A}) + C_2(\frac{V_{out}}{-A} - V_{out})$$
$$-C_1V_{in} = -C_1\frac{V_{out}}{A} - C_{in}\frac{V_{out}}{A} - C_2\frac{V_{out}}{A} - C_2V_{out}$$
$$C_1V_{in} = (\frac{C_1 + C_{in} + C_2}{A} + C_2)\,V_{out} = C_2\left(\frac{C_1 + C_{in} + C_2}{C_2A} + 1\right)V_{out} = C_2\left(\frac{1}{\beta A} + 1\right)V_{out}$$
$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2\left(\frac{1}{\beta A} + 1\right)} \approx \frac{C_1}{C_2}\left(1 - \frac{1}{\beta A}\right)$$

Sample



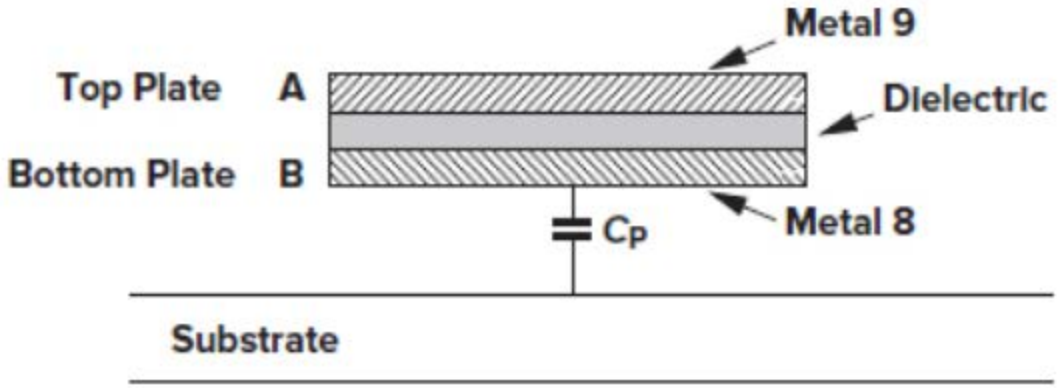
Amplify

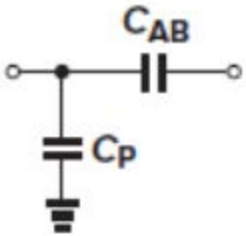


$$\beta = \frac{C_2}{C_2 + C_1 + C_{in}}$$

Connection of Capacitor

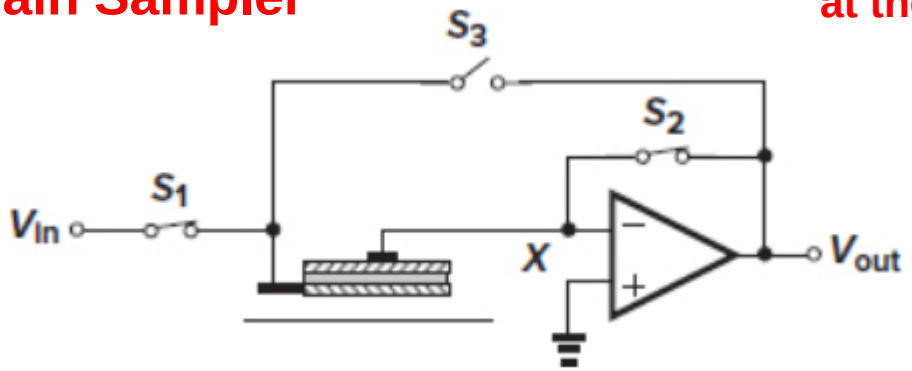
Capacitor





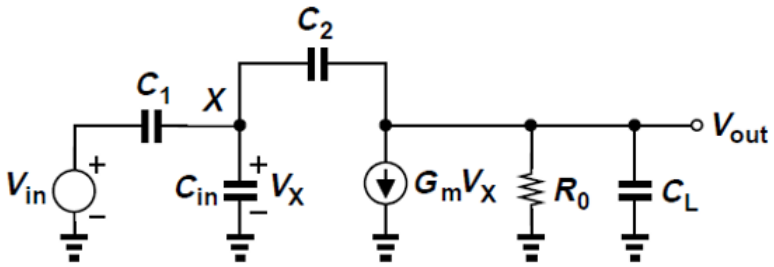
Unity-Gain Sampler

Need to minimize the capacitance at the summing node

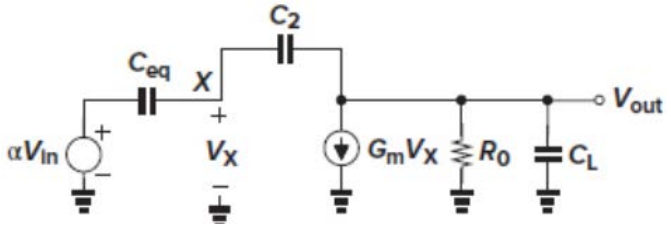


Non-Inverting Amplifier

- Speed Considerations:



$$C_{eq} = C_1 + C_{in}$$



$$\frac{V_{out}}{V_{in}}(s) \approx \frac{-C_{eq}\dfrac{C_1}{C_1 + C_{in}}(G_m - C_2 s)R_0}{R_0(C_L C_{eq} + C_L C_2 + C_{eq} C_2)s + G_m R_0 C_2}$$

$$\tau_{amp} = \frac{C_L C_{eq} + C_L C_2 + C_{eq} C_2}{G_m C_2}$$

$$= \frac{C_1 + C_2 + C_{in}}{C_2} \cdot \frac{C_L + \dfrac{C_2(C_{in} + C_1)}{C_2 + C_{in} + C_1}}{G_m}$$

$$= \frac{C_{L,eq}}{\beta G_m} = \frac{1}{\beta\, \omega_u}$$

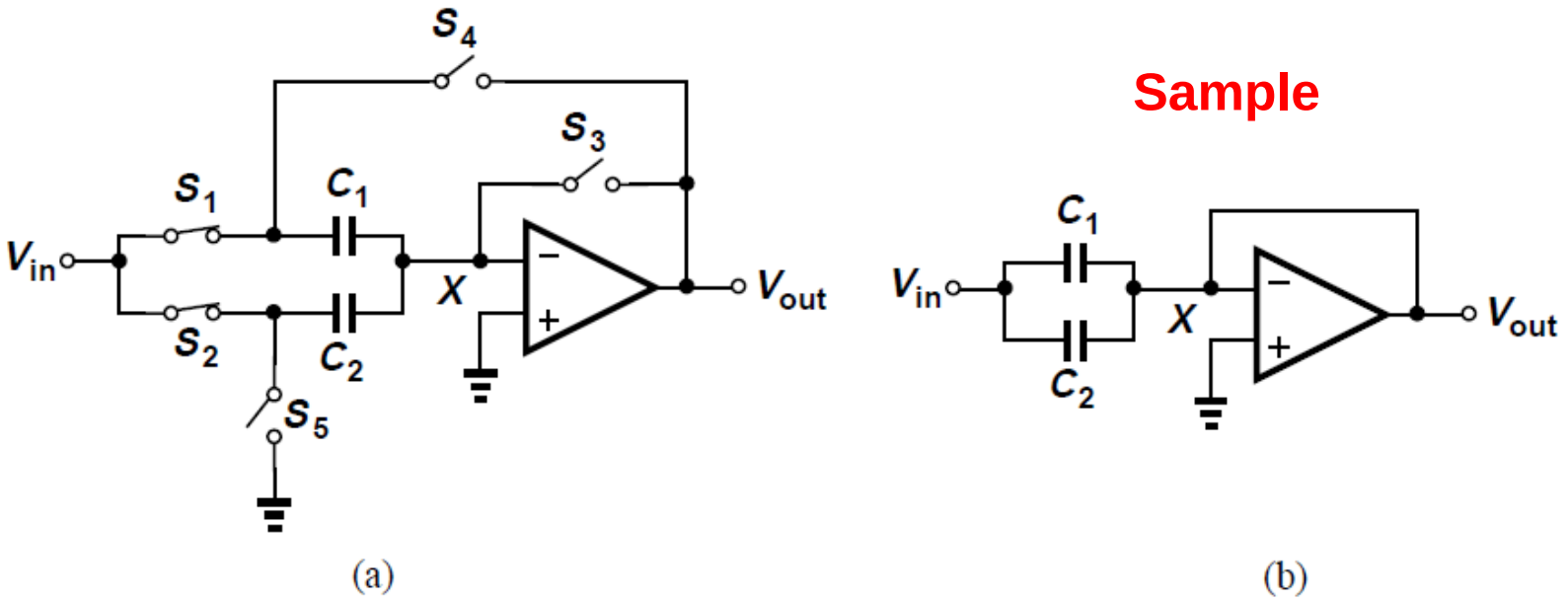
C_{in} needs to be minimized to increase β

$$\beta = \frac{C_2}{C_2 + C_1 + C_{in}}$$

$$\omega_u = \frac{G_m}{C_{L,eq}}$$

Multiply-by-Two Circuit

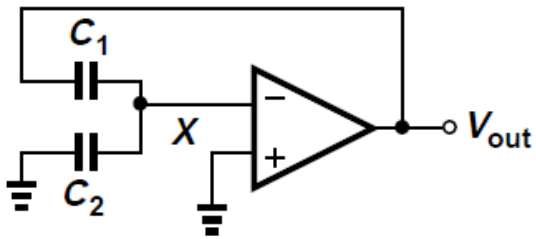
- Topology shown in Fig. (a) provides a nominal gain of two while achieving higher speed and lower gain error



- Incorporates two equal capacitors $C_1 = C_2 = C$
- In sampling mode [Fig. (b)], node X is a virtual ground, allowing voltage across C_1 and C_2 to track V_{in}

Multiply-by-Two Circuit

- During transition to amplification mode [Fig. (c)], S_3 turns off first, placing C_1 around op-amp and left plate of C_2 is grounded
- At the moment S_3 turns off, total charge on C_1 and C_2 equals $2V_{in0}C$ and since voltage across C_2 approaches zero in amplification mode, final voltage across C_1 and hence output are approximately $2V_{in0}$



(c)