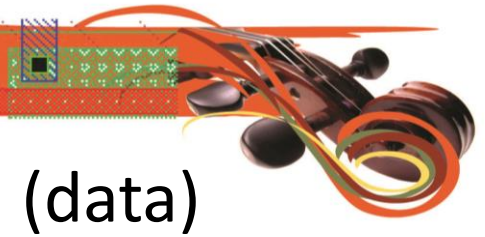
Semiconductor Memories

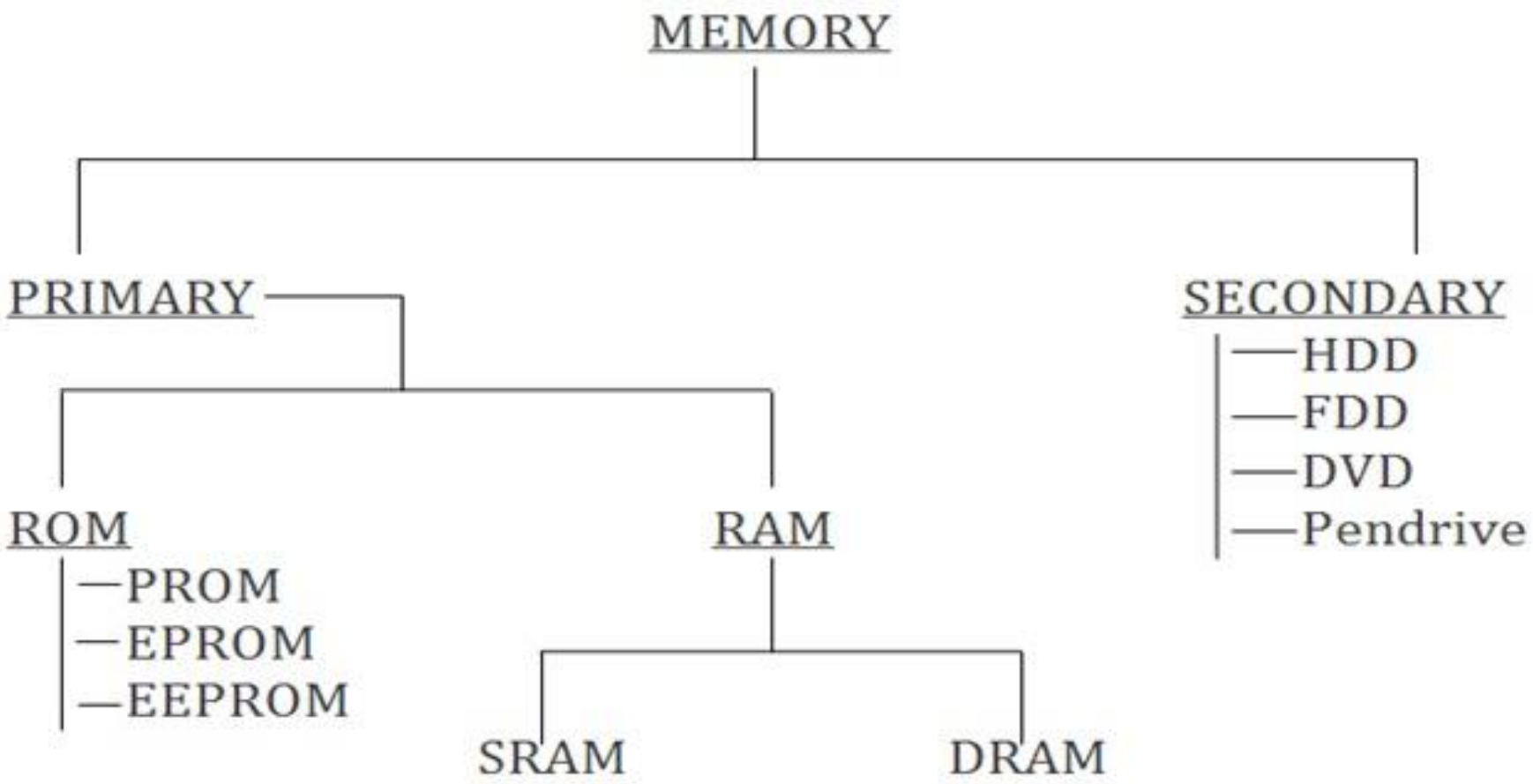
Lecture 25



- Memory array stores digital information (data)
- Number of transistor used for data storage are much larger than transistors used in logic operations and other purpose.
- The maximum data storage capacity of single chip doubles every two years.
- On chip memory is popular
- Commercially available single chip read/write memory capacity has increased to more than I gigabits (1 GB)
- This trend is leading edge of digital system design

- Design objectives
- Higher number of stored data bit per unit area
- Lower memory cost per bit
- Faster memory access time. Higher memory speed.
- Access time is time required to store or retrieve a particular data bit in memory array.
- Low static and dynamic power consumption.

- Memories:



- Semiconductor memory classifications criteria:
- Yes or No
- ❶ The type of the data
- Read and write on demand, Random Access Memory
- ❷ Data access
- Data access-time nearly equal for any cell.
- ❸ Power supply
- Power supply voltage off memory lost.

- Semiconductor memories:
  - 1 Random Access Memory (RAM) or Read/Write (R/W) Memory
    - Dynamic RAM (DRAM)
    - Static RAM (SRAM)
  - 2 Read-Only Memory (ROM)
    - Flash Memory
    - Ferroelectric Memory
    - Mask (Fuse) Memory
    - Programmable ROM (PROM)
      - Erasable PROM (EPROM)
      - Electrically Erasable PROM (EEPROM)

- DRAM consist of:
- ❶ A capacitor to store binary information High voltage: 1 , Low voltage:0
- ❷ A transistor to access the capacitor.
- Cell information (voltage) degraded due to junction leakage current at storage node.
- Cell data must be read and rewritten periodically (Refresh)
- DRAMs have low cost to be manufactured.
- Used for main memory in PC, main frame computer, and Engineering workstations.

- SRAM consist of:
- 1 SRAM consist of latch.
- Low power consumption
- High speed.
- Cell data is kept as long as the power is on. Refresh operation is not needed.
- SRAM is used for cache memory in microprocessor, main frame computer, Engineering workstations, and memory in hand-held devices due to high speed and lower power consumption.

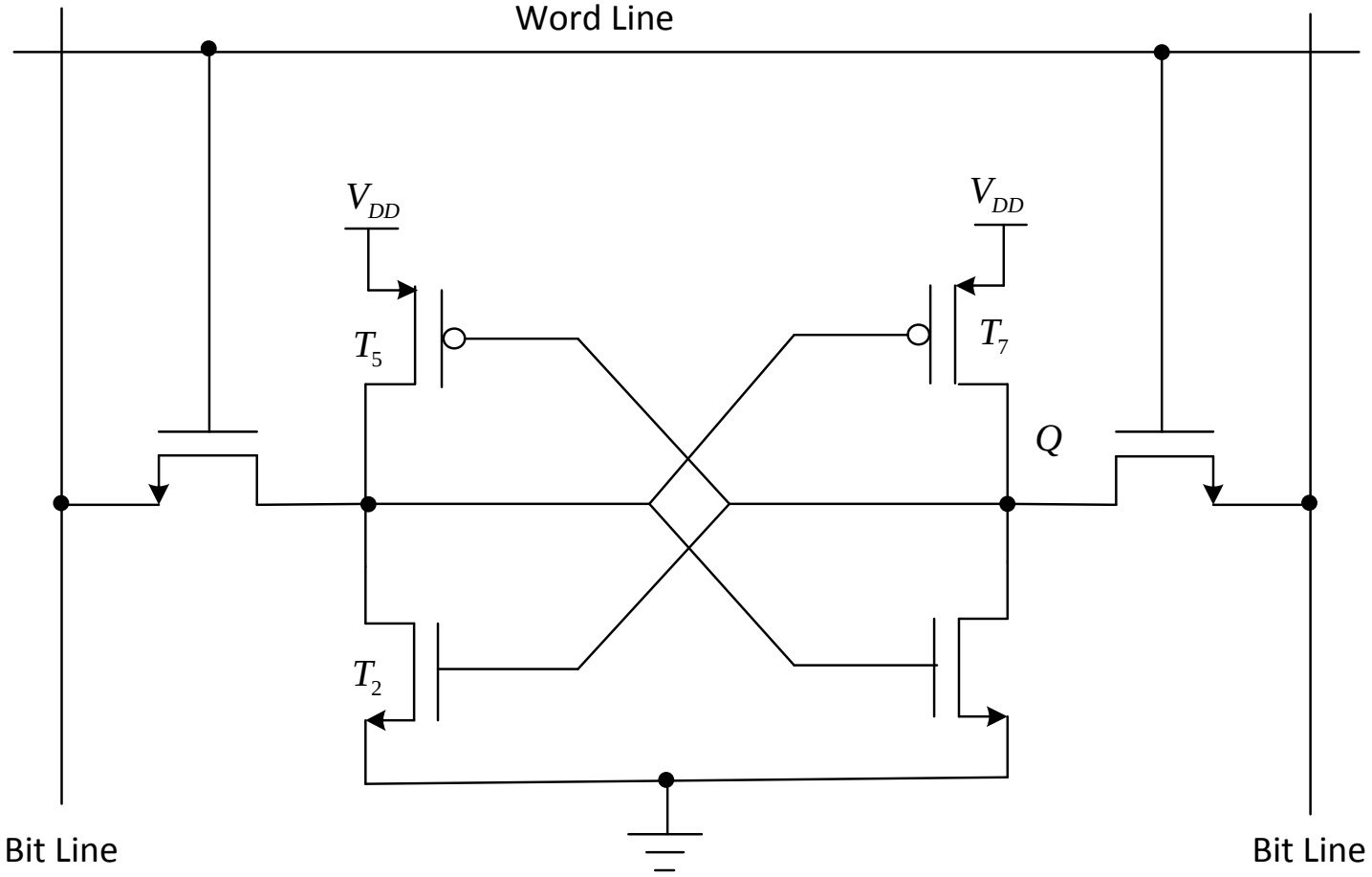
- Read-only-memory (ROM)
- Allows only retrieval of previously stored data and does not permit any modification of stored data during normal operation
- ROMs are nonvolatile memories:
- The stored information is not lost even when the power is off.
- Refresh operation is not required.
- ROM is categorized according to the type of storage (data write) method.
- Mask ROM: data are written during chip manufacturing by using photo mask.
- Programmable ROM (PROM) data are written electrically

- After the chip fabrication
- PROM is categorized according to the type of data erasing characteristic
- Fuse ROM
- Erasable PROM (EPROM): data can be rewritten
- Ultra violet rays (can penetrate through the crystal glass on the packaging) used to erase whole data in the chip simultaneously.
- Electrically erasable PROM (EEPROM)
- High electrical voltage is used to erase
- 8 bit unit in the chip simultaneously
- Slower write speed of order of microsecond

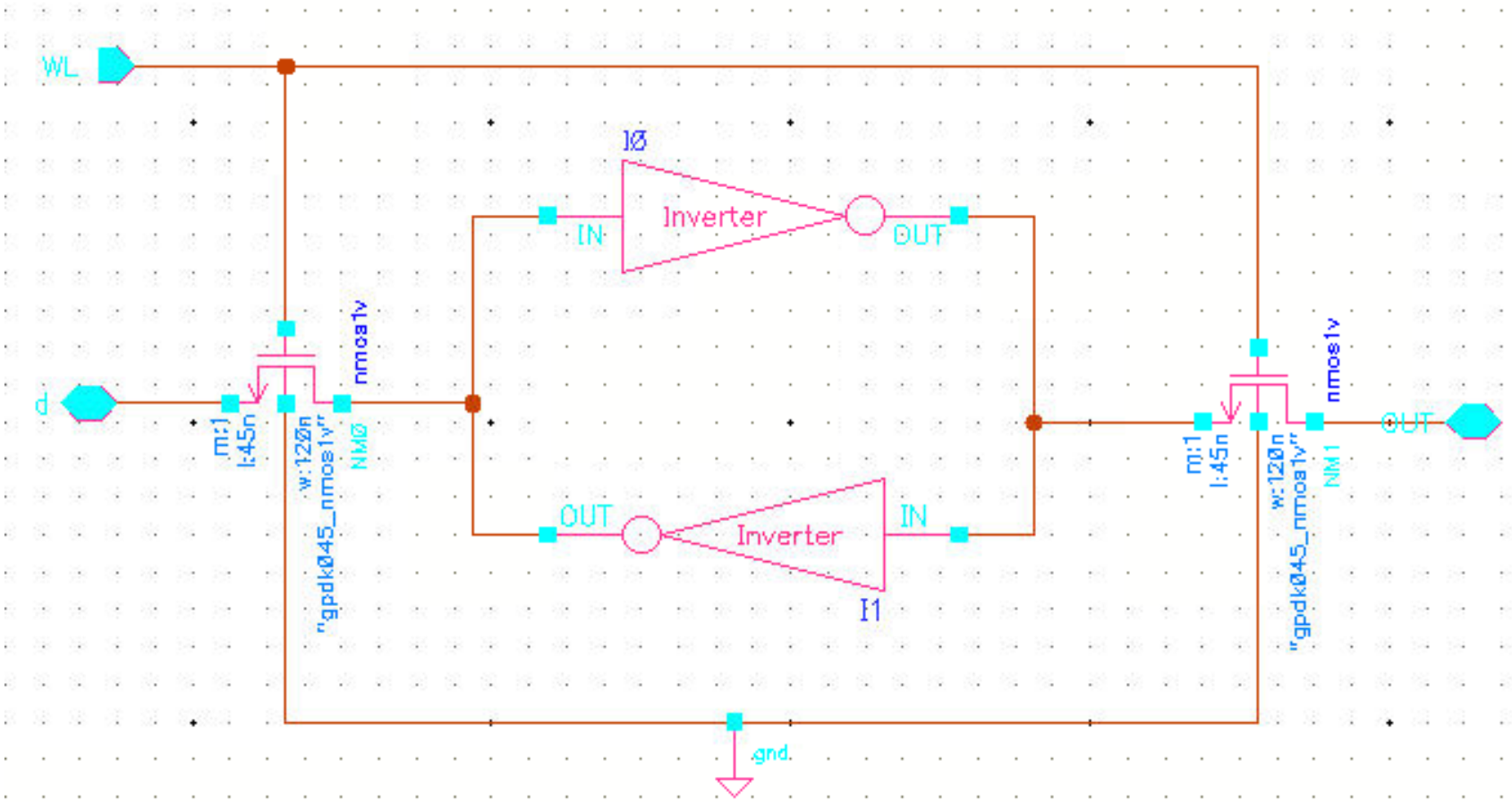
- Static and Dynamic memories)

Static memory	Dynamic memory
• Preserve state as long as power is on • Build by positive feedback or regeneration • Most useful when register will not be updated for extend of time • When the clock is turned off for unused modules no guarantee on how frequently the register will be clocked and static memories are needed to state info. • Bistable is the most popular	• Store data for short (ms) period of time • Based on the principle of temporary charge on MOS parasitic capacitor. • Capacitor need to be refreshed periodically to compensate for charge leakage. • Significantly simpler, provide higher performance and lower power dissipation • Most useful in data-path circuits that require higher performance levels and are periodically clocked.

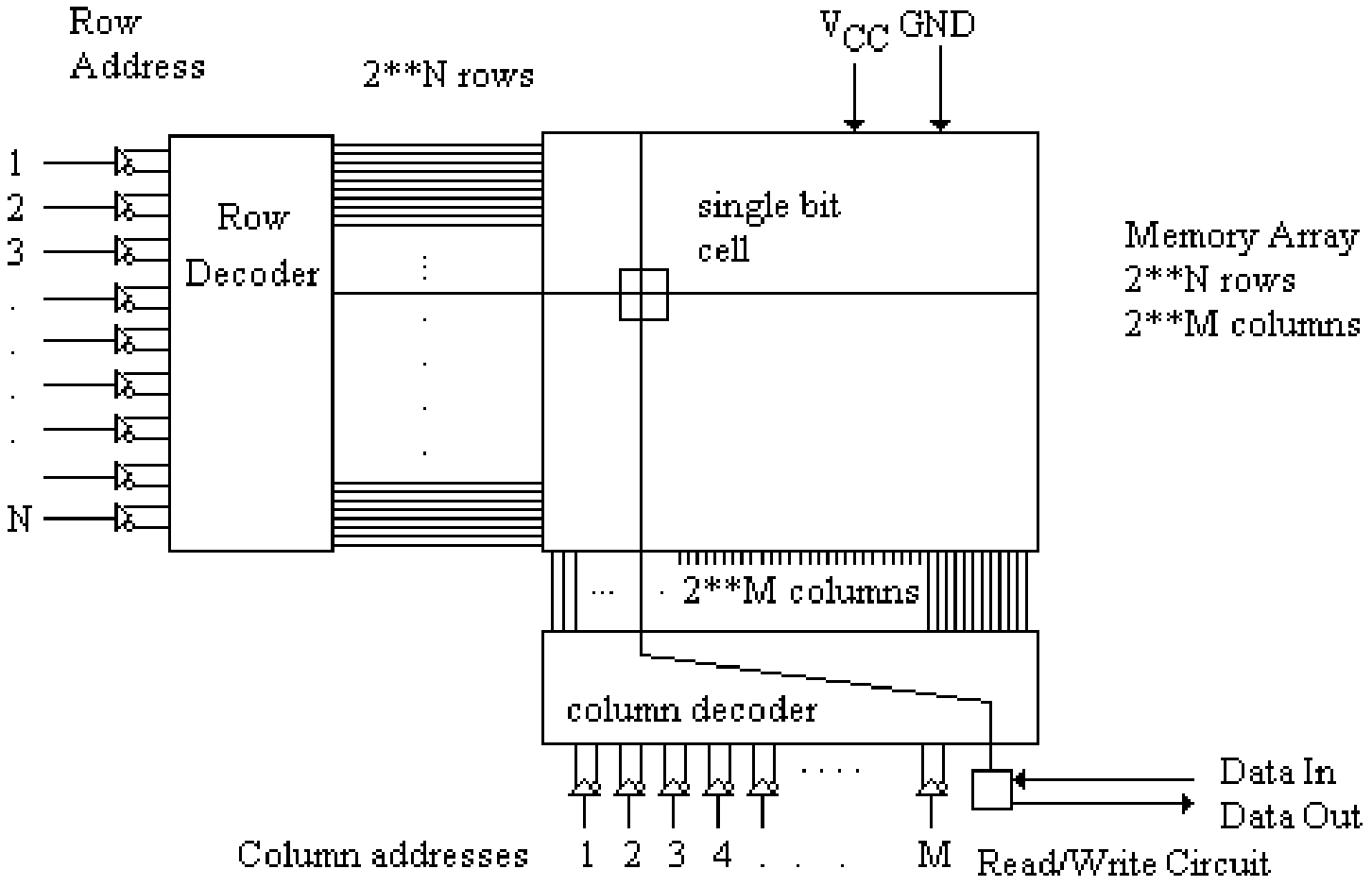
- SRAM



- SRAM (conventional 6-transistor SRAM)



- Converts binary data from inputs to unique outputs
- Activate row, activate column → Select cell

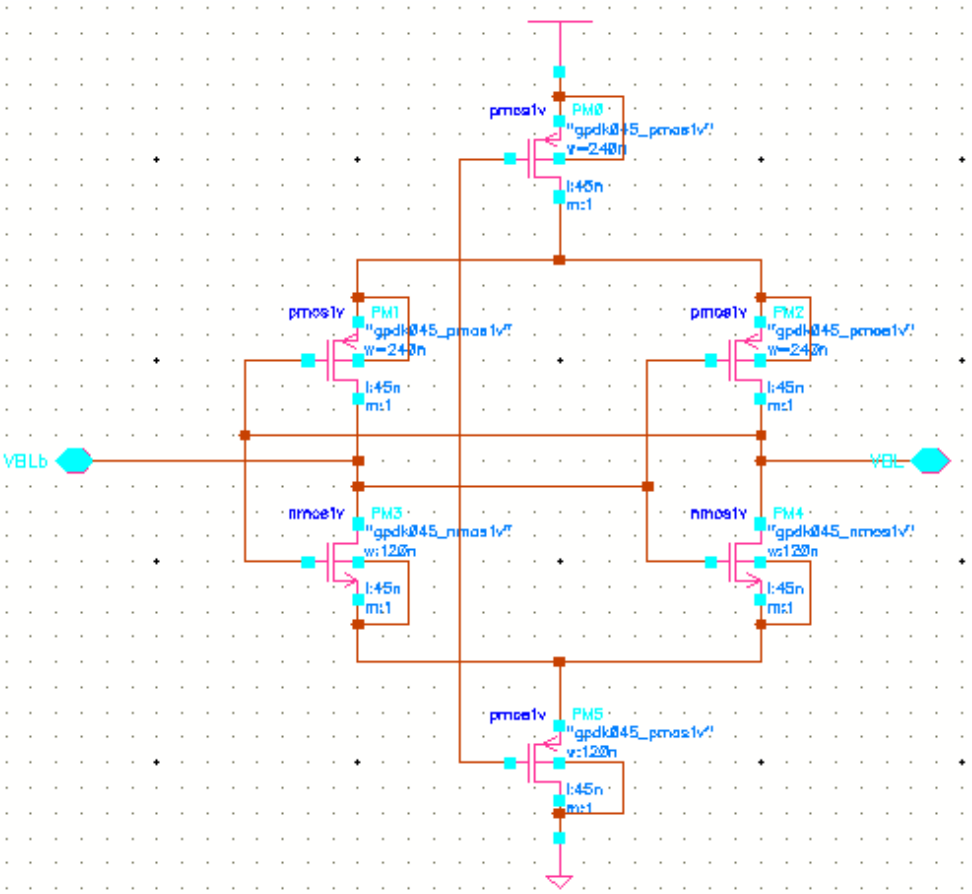


What does it do?

- Detect stored value
- Display value

How does it do it?

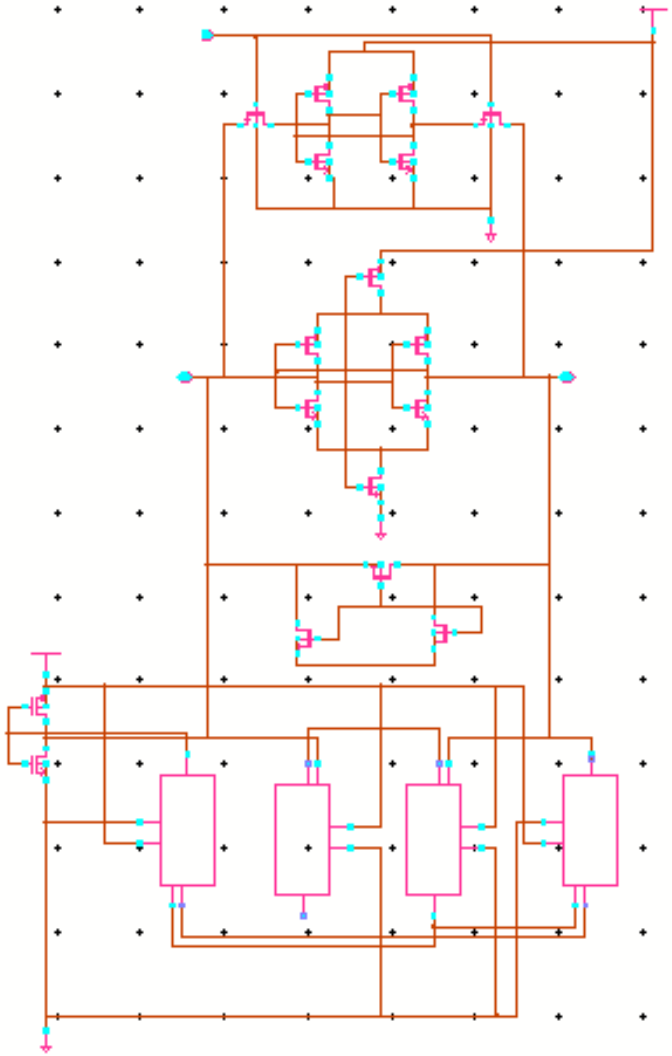
- **Sense ΔV (at bitline)**
- **Amplify (at output)**



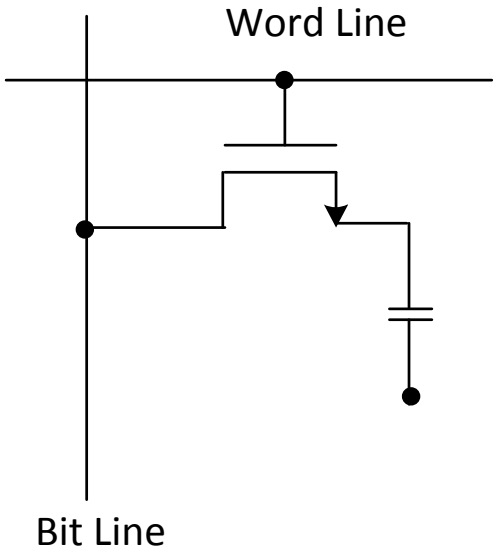
Control Circuit
with tristate buffers

Control Circuit
Activate read and write

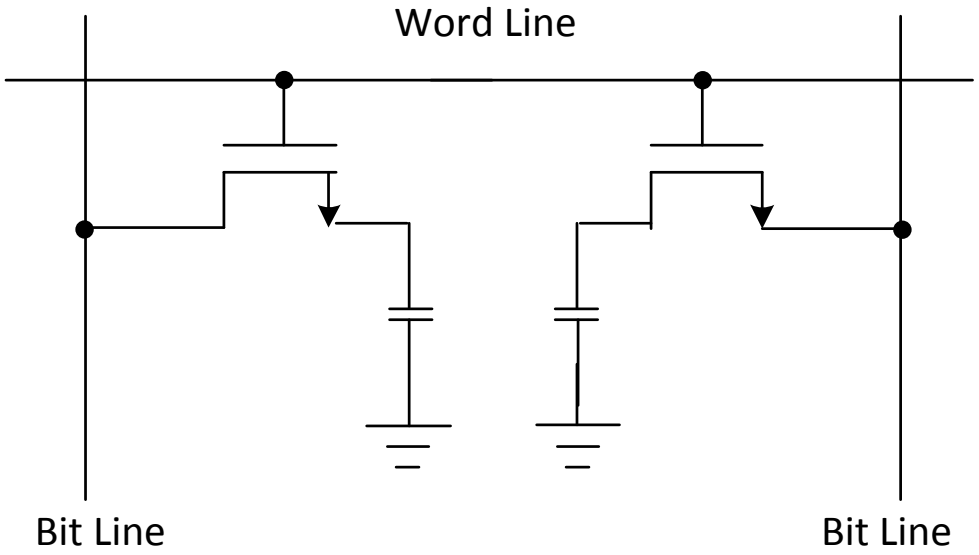
Tristate Buffer
Control read and write



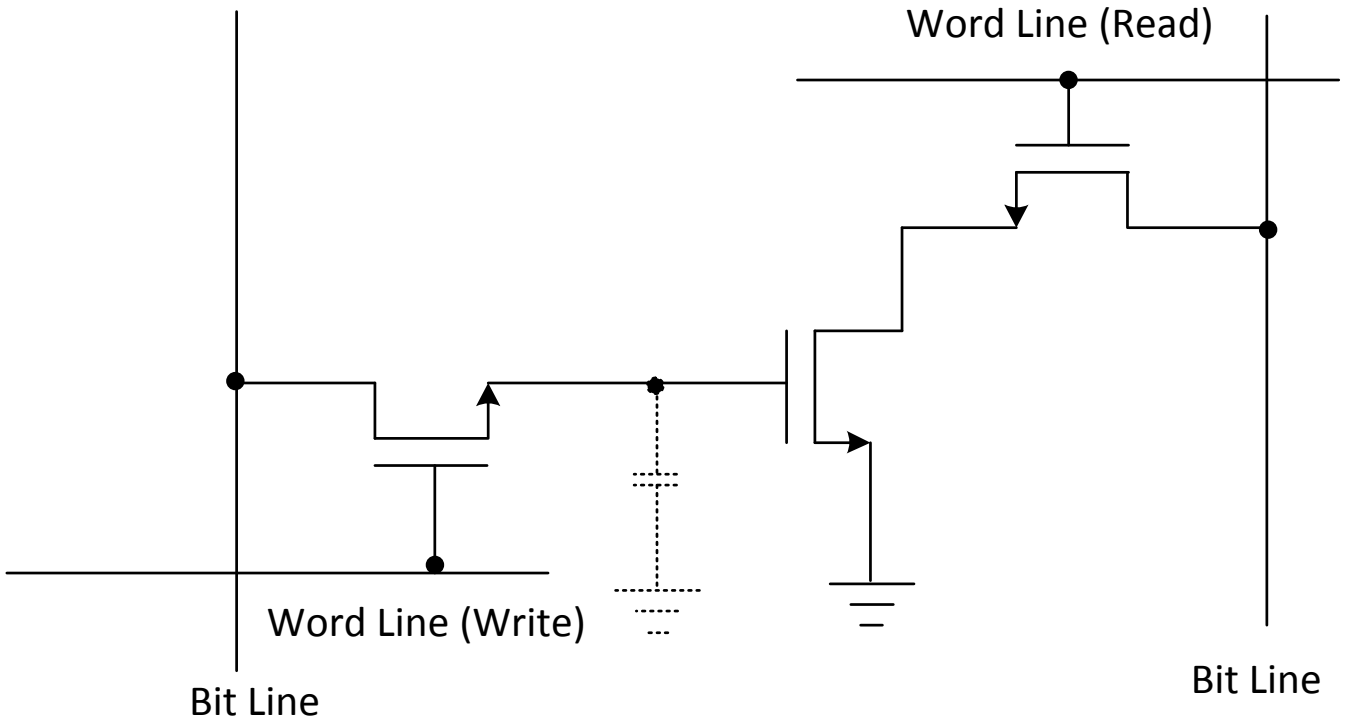
- DRAM
- Single transistor with single bit line and single word line



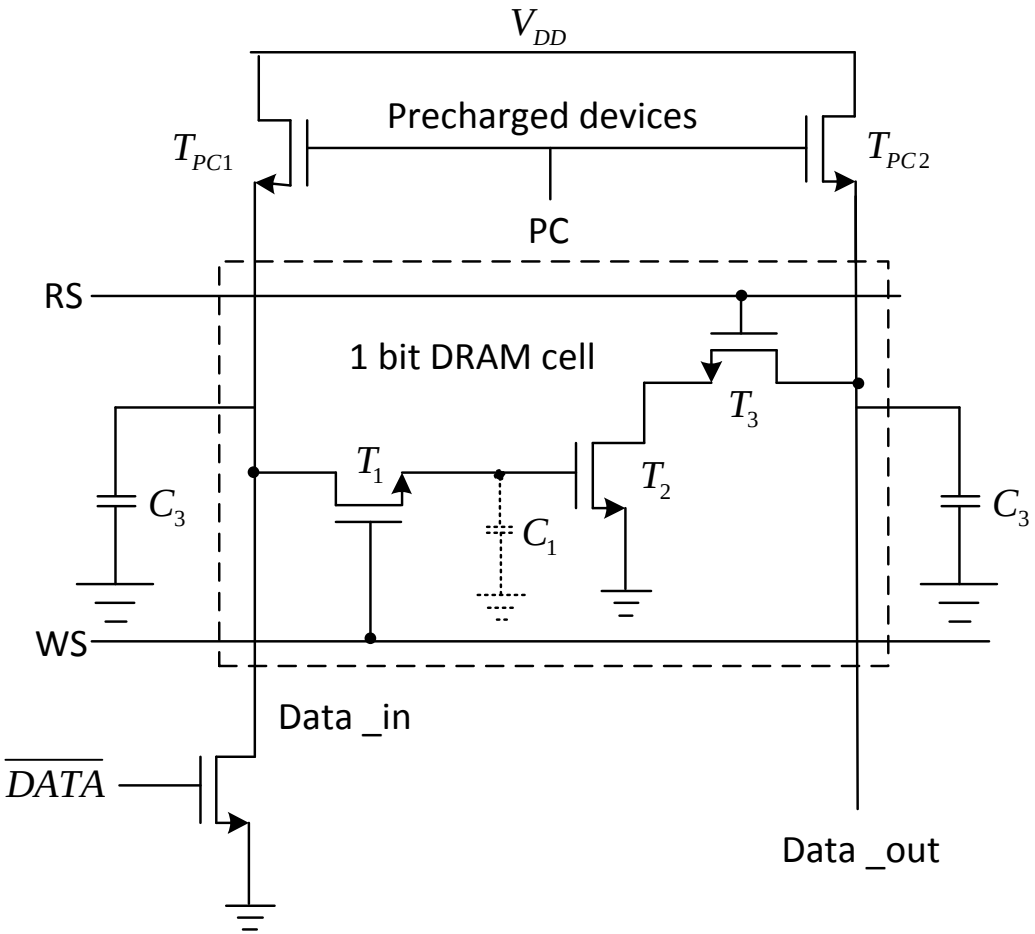
- DRAM
- Two transistors DRAM with two bit lines and single word line



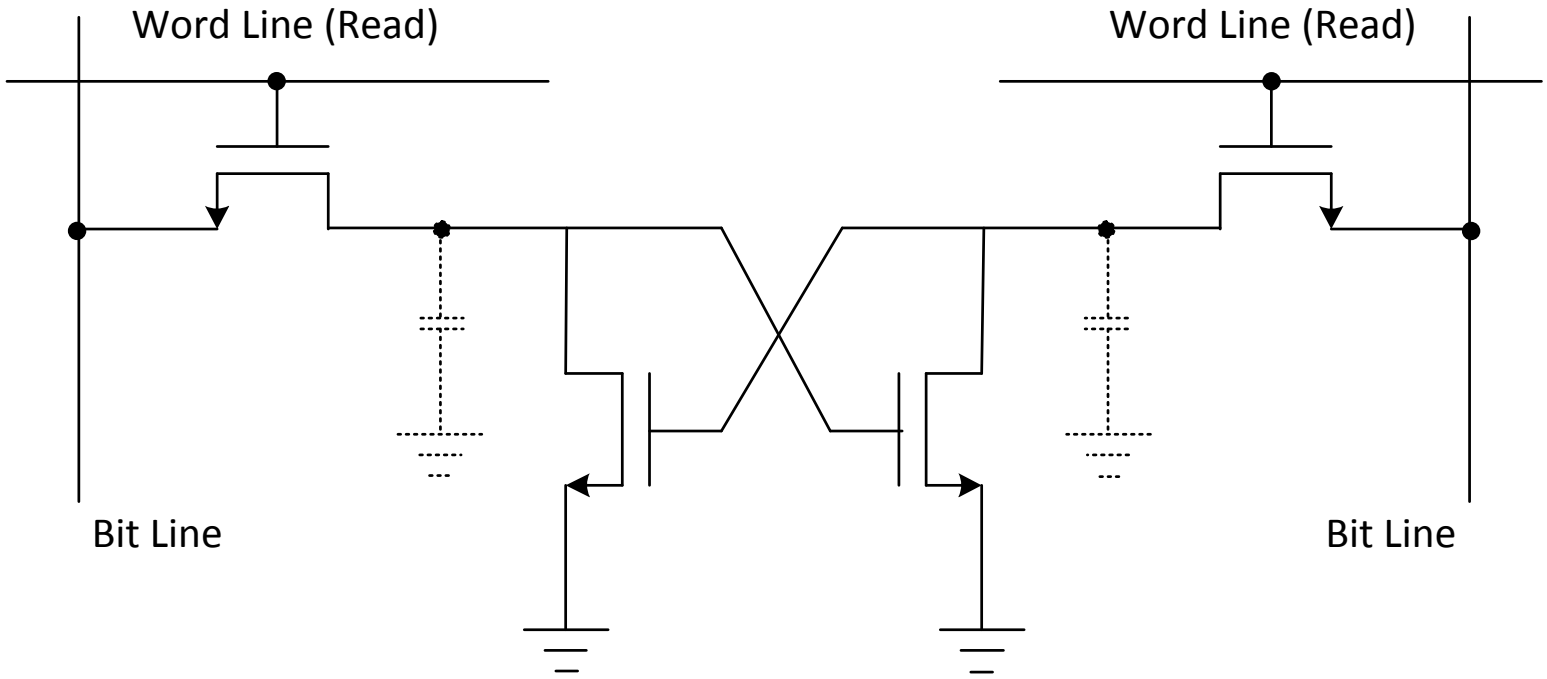
- DRAM
- Three transistors DRAM with two bit lines and two word lines.



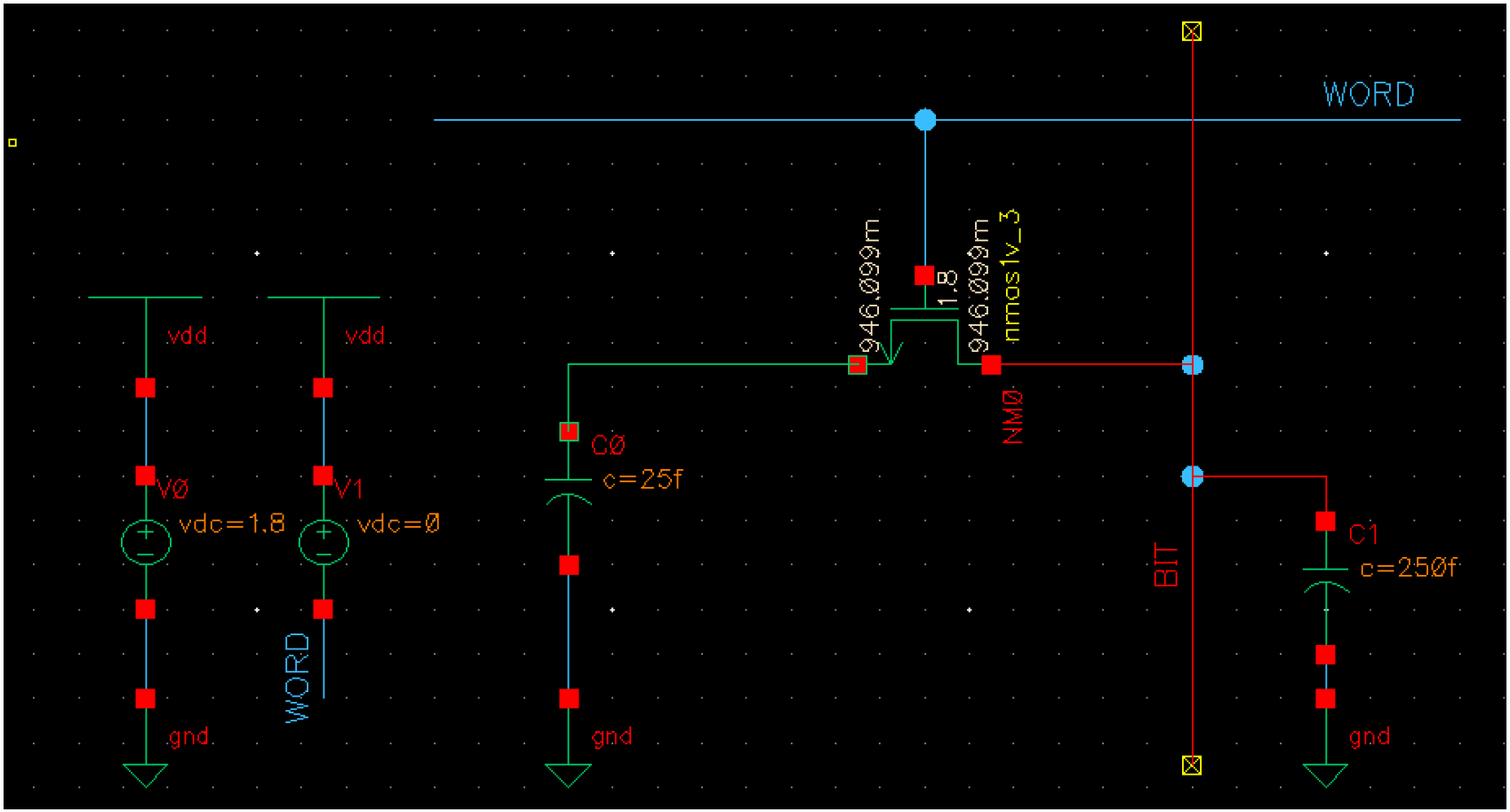
- Operation of three-transistors DRAM cell



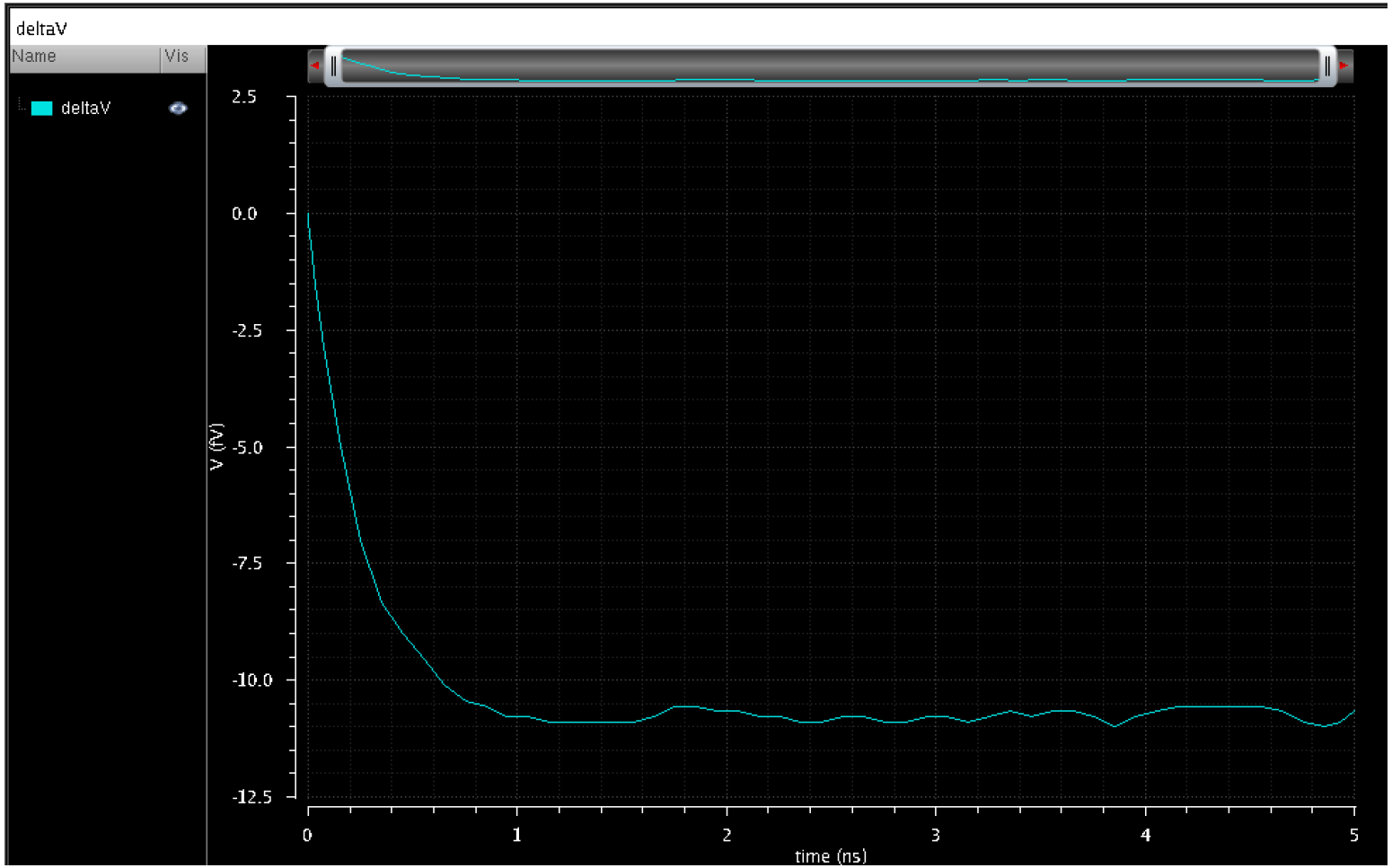
- DRAM
- Three transistors DRAM with two storage nodes



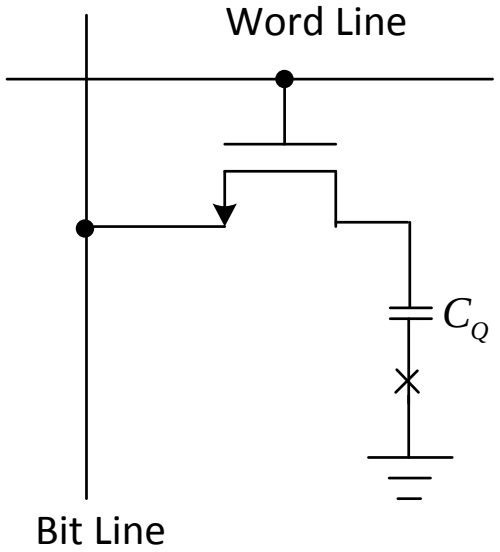
- **Write:** 0 or 1 (0 or VDD on word/bit) discharges or charges capacitor C0
- **Read:** Destructive



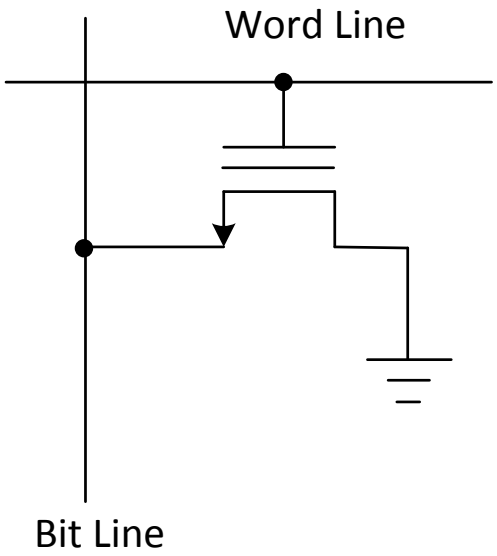
- DRAM delay



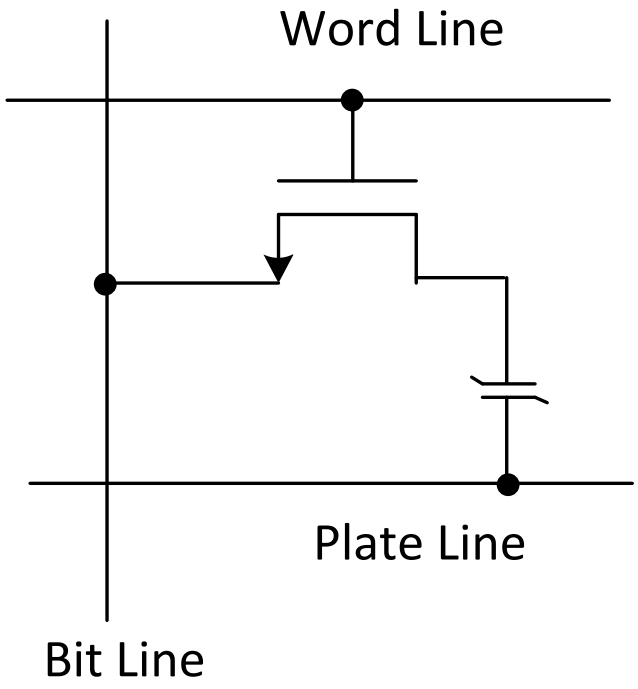
- Mask (Fuse) ROM



- EPROM-EEPROM



- FRAM (Ferroelectric RAM)
- FRAM consist of a ferroelectric capacitor to overcome the slow write operation by the hystereis.



- Flash Memory
- FRAM consist of a ferroelectric capacitor to overcome the slow write operation by the hystereis.