



J. Rabaey

University of California  
College of Engineering  
Department of Electrical Engineering  
and Computer Sciences

WeFr 2-3:30pm

Friday, February , 6:00-7:30pm

## EECS 141: SPRING 08—MIDTERM 1

|             |      |       |
|-------------|------|-------|
| <b>NAME</b> | Last | First |
|-------------|------|-------|

|            |  |
|------------|--|
| <b>SID</b> |  |
|------------|--|

**Problem 1 (19):**

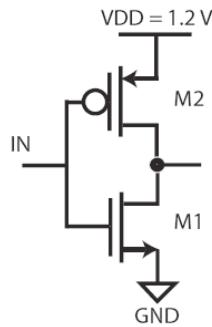
**Problem 2 (16):**

**Problem 3 (17):**

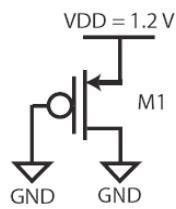
|                   |  |
|-------------------|--|
| <b>Total (52)</b> |  |
|-------------------|--|

## PROBLEM 1: MOS Transistor (19 pts)

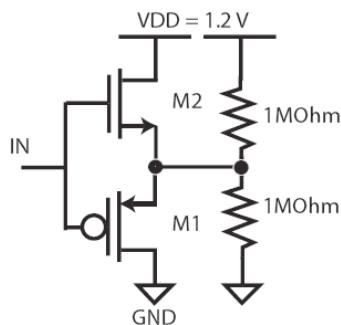
- a) Indicate the regions of operation of the transistors shown in the circuits in the tables next to the circuits. Assume short channel devices unless otherwise stated  $V_{Tn}=V_{Tp}=0.3$  V,  $V_{vsatn}=0.3$  V,  $V_{vsatp}=0.6$  V and neglect the body effect. (11 pts)



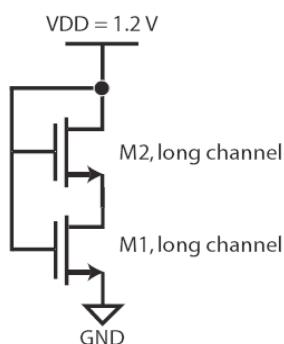
| Voltage     | Region of Operation                                       |                                                           |                                                           |
|-------------|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
|             | IN                                                        | M1                                                        | M2                                                        |
| GND (0 V)   | X cutoff<br>O linear<br>O saturation<br>O vel. saturation | O cutoff<br>X linear<br>O saturation<br>O vel. saturation | O cutoff<br>X linear<br>O saturation<br>O vel. saturation |
| VDD (1.2 V) | O cutoff<br>X linear<br>O saturation<br>O vel. saturation | X cutoff<br>O linear<br>O saturation<br>O vel. saturation | O cutoff<br>O linear<br>O saturation<br>O vel. saturation |



| Region of Operation |
|---------------------|
| M1                  |
| O cutoff            |
| O linear            |
| O saturation        |
| X vel. saturation   |



| Voltage     | Region of Operation                                       |                                                           |                                                           |
|-------------|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
|             | IN                                                        | M1                                                        | M2                                                        |
| GND (0 V)   | O cutoff<br>O linear<br>X saturation<br>O vel. saturation | X cutoff<br>O linear<br>O saturation<br>O vel. saturation | O cutoff<br>O linear<br>O saturation<br>O vel. saturation |
| VDD (1.2 V) | X cutoff<br>O linear<br>O saturation<br>O vel. saturation | O cutoff<br>O linear<br>X saturation<br>O vel. saturation | O cutoff<br>O linear<br>X saturation<br>O vel. saturation |



| Region of Operation |              |
|---------------------|--------------|
| M1                  | M2           |
| O cutoff            | O cutoff     |
| X linear            | O linear     |
| O saturation        | X saturation |

b) Table I provides some measured operating points of an unknown MOS-like device. The only thing we know is that the measurements were taken at room temperature (300K)

- 1) Can you guess what kind of device was measured? What lead you to your conclusion? (1 pts)

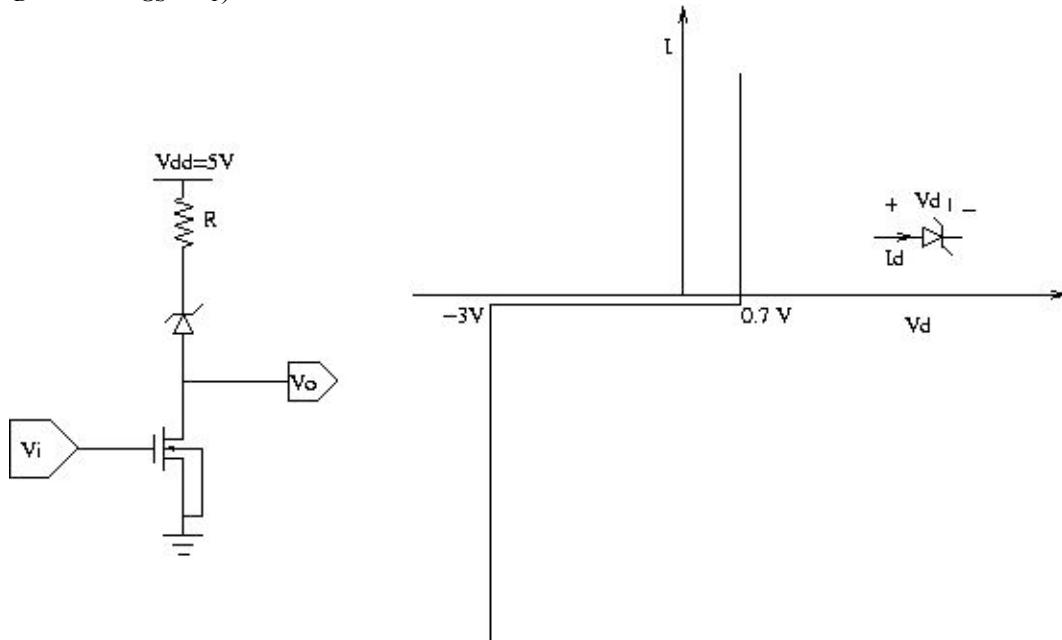
The negative voltages indicate a PMOS transistor

- 2) Complete Table I with the regions of operation of the device for each operating point (cutoff, linear, saturation, velocity saturation). Assume a short channel device (7 pts)

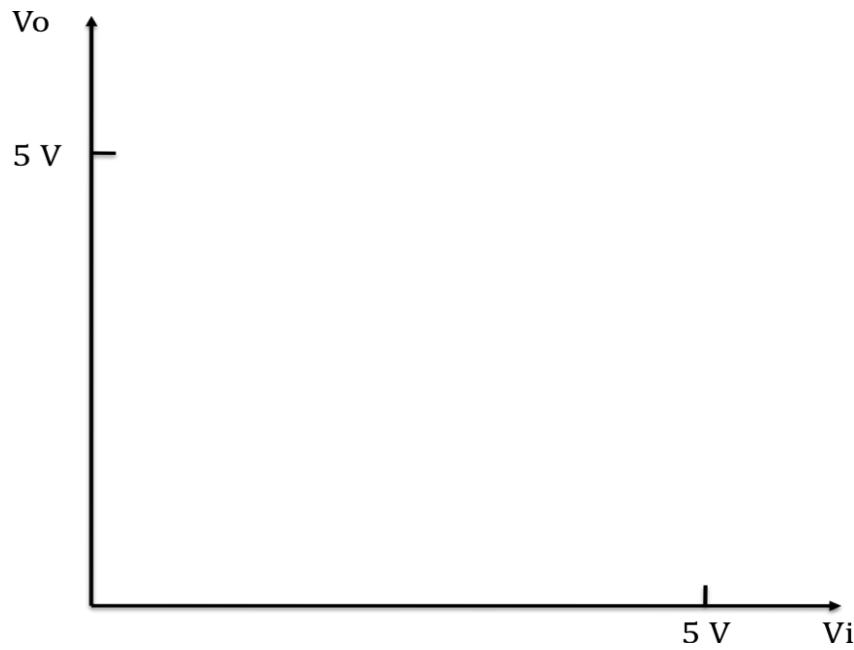
| Operating Point # | V <sub>GS</sub> [V] | V <sub>DS</sub> [V] | V <sub>SB</sub> [V] | I <sub>D</sub> [A] | Region of Operation                                      |
|-------------------|---------------------|---------------------|---------------------|--------------------|----------------------------------------------------------|
| 1                 | -0.1                | -0.3                | 0                   | -2.1n              | X cutoff O linear<br>O saturation O vel.<br>Saturation   |
| 2                 | -0.189              | -0.3                | 0                   | -21n               | X cutoff O linear<br>O saturation O vel.<br>Saturation   |
| 3                 | -0.4                | -0.5                | 0                   | -8.43μ             | O cutoff O linear<br>X saturation O vel.<br>Saturation   |
| 4                 | -0.5                | -0.5                | 0                   | -21.45μ            | O cutoff O linear<br>X saturation O vel.<br>Saturation   |
| 5                 | -1.2                | -0.2                | 0                   | -91.64μ            | O cutoff X linear<br>O saturation O vel.<br>Saturation   |
| 6                 | -1.2                | -1.2                | 0                   | -209.9μ            | O cutoff O linear<br>O saturation X vel.<br>Saturation   |
| 7                 | -1.2                | -1.2                | -0.5                | -209.9μ            | O cutoff 1 O linear<br>O saturation X vel.<br>Saturation |

## PROBLEM 2: VTC (16 pts)

The following gate has been built in a special  $0.5\mu\text{m}$  NMOS process that features our old favorites Zener diodes. The I-V characteristic of the Zener diode is shown on the right. In the flat region (between -3V and 0.7V), the current of the diode equals  $-20\mu\text{A}$ . The NMOS transistor (obviously a long channel device) has the following characteristics:  $k_n=200\mu\text{A/V}^2$ ,  $V_T=1\text{V}$ ,  $\lambda=0$ ,  $W=10\mu\text{m}$ ;  $L=0.5\mu\text{m}$ . It has **no** leakage current (i.e.  $I_D=0$  for  $V_{GS}<V_T$ ).



- a. Draw the VTC of the circuit **assuming (for the time being) that  $R=0$**  (make sure to mark the important values on your graph). (3 pts)



- b. Calculate the noise margins and the gain in the transition region gain. (3pts).

$NMH =$   
 $NML =$   
 $G =$

- c. Now, determine the value of  $R$  such that  $V_{OL}=250\text{mV}$ . (4 pts)

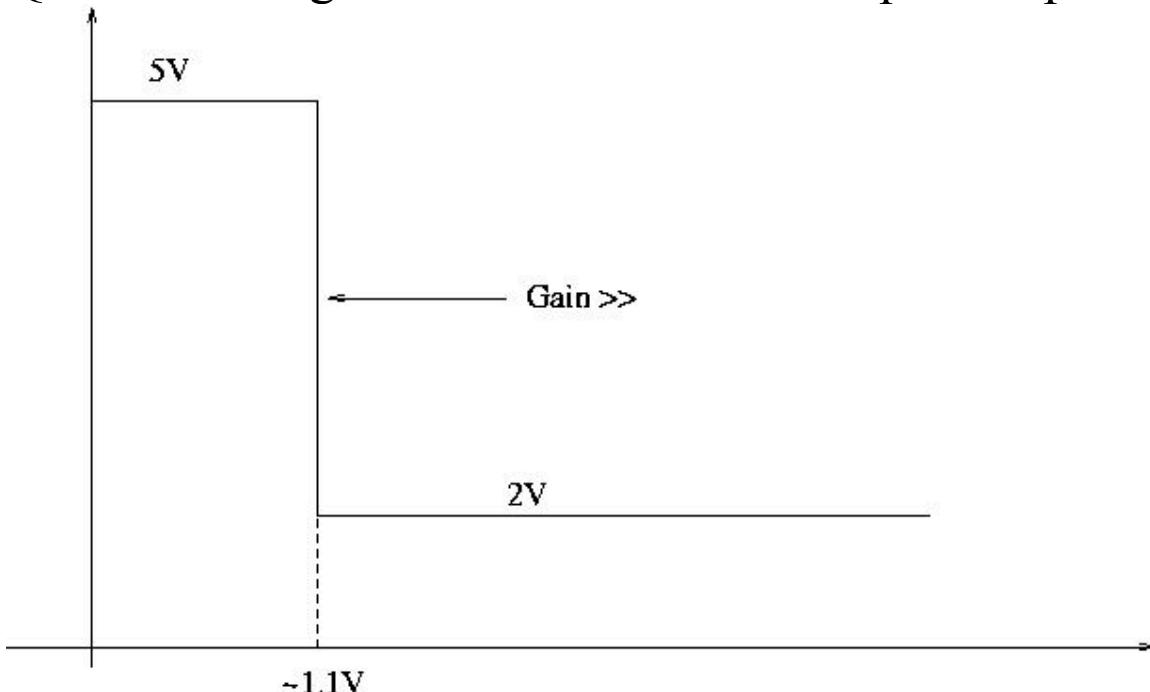
$R =$

- d. Determine the relationship between  $V_{OL}$  and supply voltage  $VDD$  for this gate. At what supply voltage does the  $V_{OL}$  drop to zero? (4pts)

- e. What is the average static power dissipation of the circuit assuming inputs 1 and 0 are equally likely? (2pts)

$$P_{\text{avg}} =$$

Q1: Draw the gate VTC and mark the important points



Q2: Calculate the gate noise margins and the transition region gain

$$NMH = VOH - VIH = 5V - 1.1V = 3.9V$$

$$NML = VIL - VOL = 1V - 2V = -1V$$

The midband gain is infinite as both the MOS device and the Zener Diode have 0 output conductance.

Since The minimum voltage output of this gate is 2V, the cascade of 2 gates has output stuck at 0. This gate is therefore not a useful digital gate (as could be seen from the negative low noise margin)

Q3: Calculate the values of the resistor R such that

$V_{ol}=250\text{mV}$ .

If  $V_{ol}=250\text{mV}$ , then  $V_i=5\text{V}$ , and the MOS device is in triode. Therefore its on resistance can be calculated as  $R_{on}=K_n(W/L)(V_{gs}-V_t-V_{ds})=200\mu\text{A}*20*(3.75)\sim60\ \Omega$ .

To get  $V_{ol}=250\text{mV}$ , an extra 1.75 have to dropped on R (3V drop is already provided by the Zener Diode).

Therefore  $2\text{V } R/(R+R_{on})=1.75\text{V}$  that results in  $R=450\ \Omega$ .

Q4: Express  $V_{ol}$  as a function of  $V_{dd}$ . Calculate the value of  $V_{dd}$  such that  $V_{ol}=0\text{V}$ .

$V_{ol}=V_{dd}-V_z-R*I_{MOS}$  regardless of the choice of  $R$ ,

$V_{ol}=0$  if  $V_{dd}=3\text{V}$

Q5: Calculate the static power consumption of the gate assuming inputs are equally likely

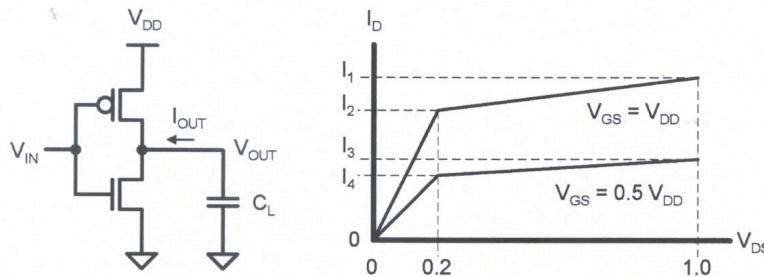
In general  $P=V_{dd}*(p_0I_0+p_pI_1)$  In this case  $p_0=p_1=1/2$  and  $I_0=20\mu\text{A}\sim0$

Assuming the question is solved for  $V_{ol}=250\text{mV}$  case, we have  $I_1=1.75\text{V}/R=3.8\text{mA}$  and  $P_d=9.8\text{mW}$

Similar derivation for  $R=0$  case give  $P_d=60\text{mW}$

**PROBLEM 3: Propagation Delay (17 pts)**

Given the inverter below with  $V_{DD} = 1V$ , and the I-V characteristics of the NMOS and PMOS transistors:



The NMOS and PMOS transistors are fully symmetric, that is  $I_D = I_{DN} = |I_{DP}|$  for the same absolute gate-to-source and drain-to-source voltage conditions.

The values of the drain current are  $I_1 = 100 \mu A$ ,  $I_2 = 80 \mu A$ ,  $I_3 = 50 \mu A$  and  $I_4 = 40 \mu A$  and  $C_L = 10 fF$ . The input is an ideal step input with  $V_{LOW} = 0V$  and  $V_{HIGH} = V_{DD}$ . Note that the propagation delay is referenced to  $0.5 V_{DD}$  and all other capacitances are ignored.

- a. Determine the high-to-low propagation delay. (3 points)

$$R_1 = R(V_{GS} = 1V) = 1V / 100 \mu A = 10 k\Omega \quad (0.5 \text{ pts})$$

$$I_D(V_{GS} = 1V, V_{DS} = 0.5V) = 80 \mu A + \frac{20 \mu A}{0.8V} (0.5V - 0.2V) = 87.5 \mu A \quad (0.5 \text{ pts})$$

$$R_2 = \frac{0.5V}{87.5 \mu A} = 5.71 k\Omega \quad (0.5 \text{ pts}) \quad t_{PHL} = \ln 2 \cdot R_{eq} C_L \quad (0.5 \text{ pts})$$

$$t_{PHL} = 54.46 \text{ ps} \quad (0.5 \text{ pts}) \quad R_{eq} = \frac{R_1 + R_2}{2} = 7.86 k\Omega \quad (0.5 \text{ pts})$$

- b. Determine the low-to-high propagation delay. (2 points)

$$R_1 = 10 k\Omega \quad R_{eq} = 7.86 k\Omega \quad (0.5 \text{ pts})$$

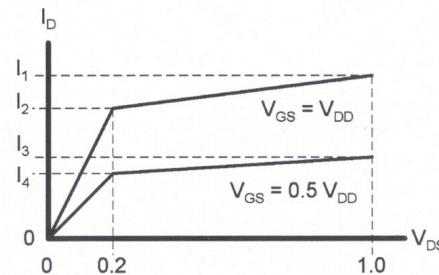
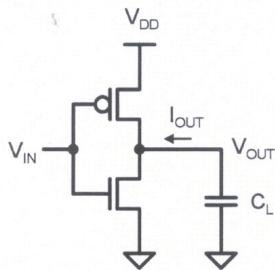
$$R_2 = 5.71 k\Omega \quad (0.5 \text{ pts})$$

$$t_{PLH} = \ln 2 \cdot R_{eq} C_L \quad (0.5 \text{ pts})$$

$$t_{PLH} = 54.46 \text{ ps} \quad (0.5 \text{ pts})$$

**PROBLEM 3: Propagation Delay (17 pts)**

Given the inverter below with  $V_{DD} = 1V$ , and the I-V characteristics of the NMOS and PMOS transistors:



The NMOS and PMOS transistors are fully symmetric, that is  $I_D = I_{DN} = |I_{DP}|$  for the same absolute gate-to-source and drain-to-source voltage conditions.

The values of the drain current are  $I_1 = 100 \mu A$ ,  $I_2 = 80 \mu A$ ,  $I_3 = 50 \mu A$  and  $I_4 = 40 \mu A$  and  $C_L = 10 fF$ . The input is an ideal step input with  $V_{LOW} = 0V$  and  $V_{HIGH} = V_{DD}$ . Note that the propagation delay is referenced to  $0.5 V_{DD}$  and all other capacitances are ignored.

- a. Determine the high-to-low propagation delay. (3 points) *Alternate Solution*

$$I_1 = 100 \mu A = I(V_{DS} = 1V, V_{GS} = 1V) \quad (0.5 \text{ pts})$$

$$I_2 = I(V_{DS} = 0.5V, V_{GS} = 1V) = 80 \mu A + \frac{20 \mu A}{0.8V} (0.5V - 0.2V) = 87.5 \mu A \quad (0.5 \text{ pts})$$

$$I_{eq} = \frac{I_1 + I_2}{2} = 93.75 \mu A \quad (0.5 \text{ pts})$$

$$t_{PLH} = \frac{C_L \Delta V}{I_{eq}} = \frac{C_L (0.5V)}{I_{eq}} \quad (1 \text{ pt.})$$

$$t_{PLH} = 53.33 \text{ ps} \quad (0.5 \text{ pts})$$

- b. Determine the low-to-high propagation delay. (2 points) *Alternate Solution*

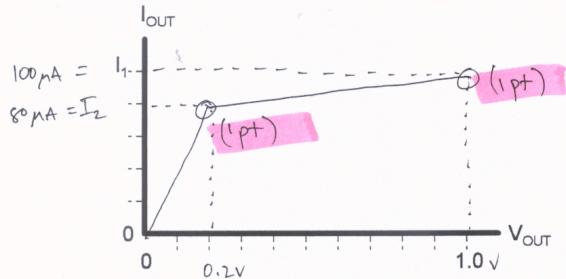
$$I_1 = 100 \mu A \quad t_{PLH} = \frac{C_L \Delta V}{I_{eq}} \quad (0.5 \text{ pts})$$

$$I_2 = 87.5 \mu A \quad (0.5 \text{ pts})$$

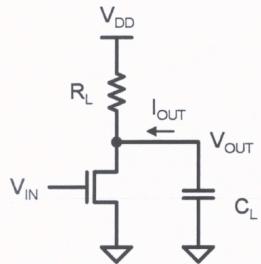
$$I_{eq} = 93.75 \mu A \quad (0.5 \text{ pts}) \quad t_{PLH} = 53.33 \text{ ps} \quad (0.5 \text{ pts})$$

$$t_{PLH} = 53.33 \text{ ps}$$

c. Plot the  $I_{OUT}$  vs.  $V_{OUT}$  during a high-to-low transition. (2 points)



The PMOS is replaced by a linear resistor as shown in the figure below.



Note that  $R_L = 10 \text{ k}\Omega$ .

d. What is  $V_{OL}$ ? (3 points)

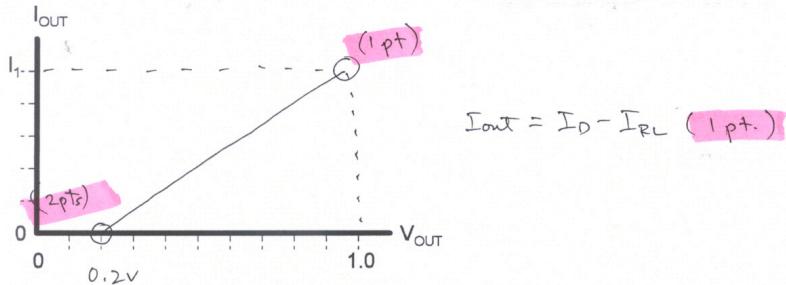
$$I_{R_L} = I_D \text{ or } I_{out} = 0 \quad (\text{1 pt.})$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{80 \text{ mA}}{0.2 \text{ V}} V_{OL} \quad \text{if } V_{OL} \leq 0.2 \text{ V} \quad (\text{1 pt.})$$

$$V_{OL} = \frac{\frac{1}{10 \text{ k}\Omega}}{\frac{80 \text{ mA}}{0.2 \text{ V}} + \frac{1}{10 \text{ k}\Omega}} = 0.2 \text{ V} \quad (\text{1 pt.})$$

$V_{OL} = 0.2 \text{ V}$

e. Plot the  $I_{OUT}$  vs.  $V_{OUT}$  during a high-to-low transition. (4 points)



f. Determine the high-to-low propagation delay. (3 points)

$$R_1 = R(V_{DS} = 1V) = 10k\Omega \quad (0.5 \text{ pts})$$

$$I_D (V_{DS} = 0.5V) = \frac{100\mu A}{0.8V} (0.5V - 0.2V) = 37.5\mu A \quad (0.5 \text{ pts})$$

$$R_2 = R(V_{DS} = 0.5V) = \frac{0.5V}{37.5\mu A} = 13.33k\Omega \quad (0.5 \text{ pts})$$

$$R_{eq} = \frac{R_1 + R_2}{2} = 11.67k\Omega \quad (0.5 \text{ pts})$$

$$t_{PHL} = \ln 2 \cdot R_{eq} C_L \quad (0.5 \text{ pts}) \quad t_{PHL} = 80.86 \text{ ps} \quad (0.5 \text{ pts})$$

$$t_{PHL} = 80.86 \text{ ps}$$

Alternate Solution:

$$I_1 = 100\mu A \quad (0.5 \text{ pts})$$

$$I_2 = I (V_{DS} = 0.5V) = \frac{100\mu A}{0.8V} (0.5V - 0.2V) = 37.5\mu A \quad (0.5 \text{ pts})$$

$$I_{eq} = \frac{I_1 + I_2}{2} = 68.75\mu A \quad (0.5 \text{ pts})$$

$$t_{PHL} = \frac{C_L \Delta V}{I_{eq}} = \frac{C_L (0.5V)}{I_{eq}} \quad (1 \text{ pt.})$$

$$t_{PHL} = 72.72 \text{ ps} \quad (0.5 \text{ pts})$$