**San Jose State University**
**Department of Electrical Engineering**
**College of Engineering**

# Exam 1

**EE 224** **Sample**

**Closed Book, Closed Notes, No electronic devices**

**Instructions:**

❶ **There are four problems. They are weighted as shown. Interpretation of questions will not be given during the exam. If you are unsure about the meaning of a question, make an assumption, state what it is and continue.**

❷ **Work all four problems. Show all your work. Justify your answer. Partial credit will be granted for an answer but only if the intermediate work is shown.**

❸ **All writing must be on the paper provided (No additional, scratch paper allowed).**

❹ **Candidates guilty of any of following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:**

- **Making use of any books, papers or memoranda, calculators, cellphone, or any memory aid devices.**
- **Speaking or communicating with other candidates.**
- **Purposely exposing written papers with other candidates.**

| Problem | Possible | Score |
|---|---|---|
| 1 | 25 | |
| 2 | 25 | |
| 3 | 25 | |
| 4 | 25 | |
| Total | 100 | |

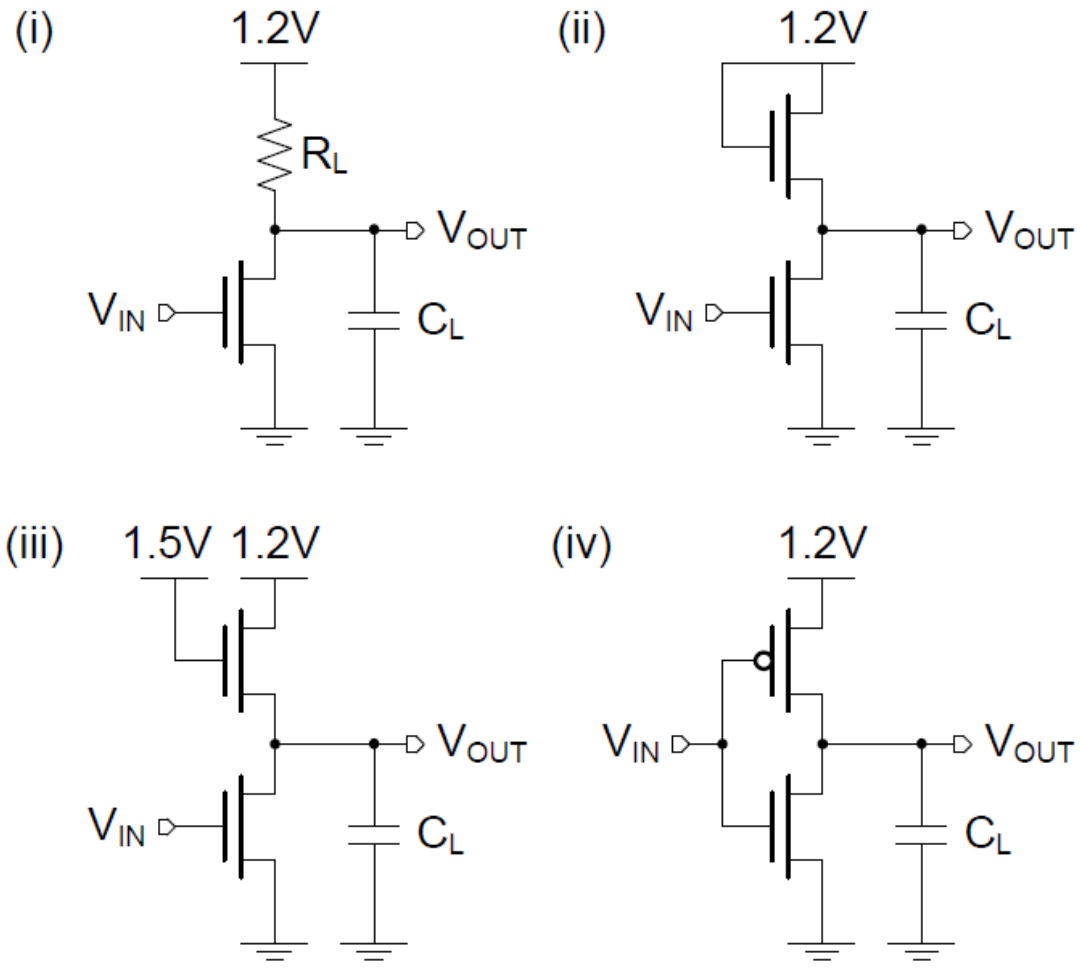
❺ **Candidate should be prepared to produce, upon request, her/his SJSU identification card.**

❻ **Verify your name and enter your student identification number at the bottom of this page and sign.**

**Name** **Signature:**

**PROBLEM 1: (25 points)**

Consider the circuits below showing different implementation of an inverter, whose output is connected to a capacitor. Assume $V_{tn} = |V_{tp}| = 0.3V$, and output capacitor $C_L$ is initially discharged. Ignore sub-threshold conduction and body effect




a) Which one(s) of the circuits consume(s) static power when the input is high $V_{IN} = 1.2V$ ? (8 points)

All inverters but the CMOS inverter, (iv), consume static power when the input is high. Notice that in the first three inverters, (i)~(iii) when the input is high, there is always a direct connection from VDD to GND.

b) Which one(s) of the circuits consume(s) static power when the input is low $V_{IN} = 0V$ ? (8 points)

None of the static inverters consumes power when the input is low because there is no path from VDD to GND.

c) $V_{OH}$ of which circuit(s) is 1.2V (If possible)? (8 points)

All inverters but the saturated enhancement inverter,(ii), has a $V_{OH}$ of 1.2 V.

d) $V_{OL}$ of which circuit(s) is 0V (If possible)? (8 points)

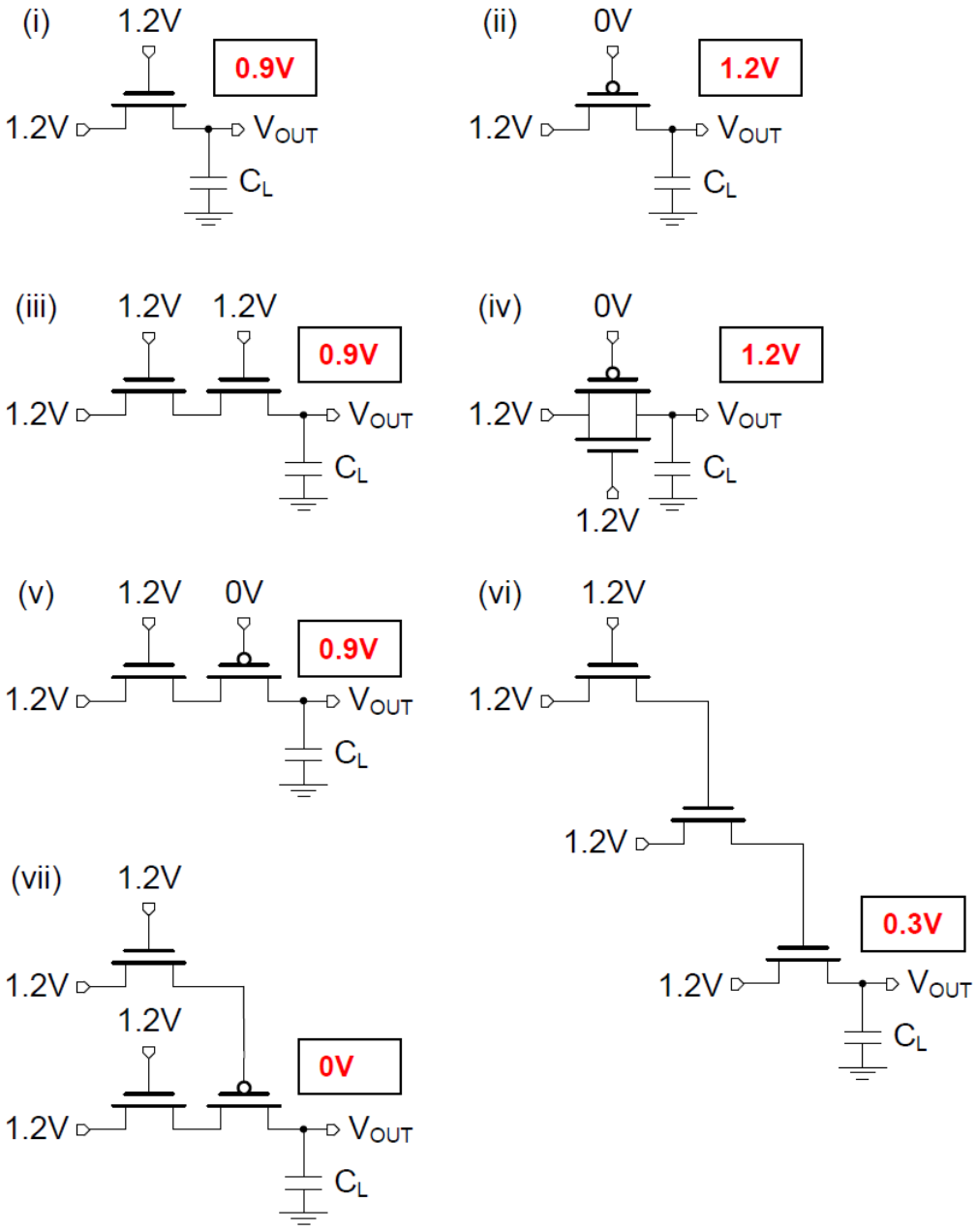
Only the CMOS inverter, (iv), has a VOL of 0 V.

e) The proper functionality of which circuit(s) depends on the size of devices? (8 points)

Except for the CMOS inverter, (iv), all the other inverters' functionality depend on the relative sizes of the transistors.

**PROBLEM 2: (45 points)**

Find the final value of the voltage VOUT for the various switch logics as shown in below figure. Assume that $V_{tn} = |V_{tp}| = 0.3V$, that and the output capacitor, $C_L$, is initially discharged. Ignore sub-threshold conduction and body effect. All middle nodes are discharged initially.



**PROBLEM 3: (30 points)**

A CMOS inverter has the following device parameters:

NMOS: $V_{TN}=0.5V$ $\quad k_n=115\mu A/V^2$ $\quad (W/L)_n=2$

PMOS: $V_{TP}=-0.6V$ $\quad k_p=-30\mu A/V^2$ $\quad (W/L)_p=4$

The power supply voltage is $V_{DD}=2.5V$ , and the output load capacitance of 0.5Pf. Assume that CMOS inverter is implemented with long-channel devices, and that channel modulation is neglected.

a) Calculate the low-to-high and high-to-low delay times of the output signal.

$$\Delta V = V_{DD} - \frac{V_{DD}}{2} = 1.25V \quad \& \quad C = 0.5pF$$

Long channel => no vel. Sat.

$$t_{PHL}: \quad V_{GS}=V_{DD}, \quad V_{DS}=V_{DD} \quad \Rightarrow sat.$$

$$I_{2.5} = \frac{1}{2}k_n\left(\frac{W}{L}\right)_n\left(V_{GS}-V_t\right)^2 = 460\mu A$$

$$V_{GS}=V_{DD}, \quad V_{DS}=\frac{V_{DD}}{2} \quad \Rightarrow linear$$

$$I_{1.25} = k_n\left(\frac{W}{L}\right)_n\left[\left(V_{GS}-V_t\right)V_{DS} - \frac{{V_{DS}}^2}{2}\right] = 395\mu A$$

$$I_{avg} = \frac{1}{2}\left(460+395\right)\mu A = 427.5\mu A$$

$$t_{PHL} = \frac{C\Delta V}{I_{avg}} = 1.46n\sec$$

$$t_{PLH}: \quad V_{GS}=-V_{DD}, \quad V_{DS}=-V_{DD} \quad \Rightarrow sat.$$

$$I_{2.5} = \frac{1}{2}k_p\left(\frac{W}{L}\right)_p\left(V_{GS}-V_t\right)^2 = 216.6\mu A$$

$$V_{GS}=-V_{DD}, \quad V_{DS}=-\frac{V_{DD}}{2} \quad \Rightarrow linear$$

$$I_{1.25} = k_p \left(\frac{W}{L}\right)_p \left[ (V_{GS} - V_t) V_{DS} - \frac{V_{DS}^2}{2} \right] = 191.25 \mu A$$

$$I_{avg} = \frac{1}{2}(191.25 + 216.6)\,\mu A = 203.925 \mu A$$

$$t_{PLH} = \frac{C \Delta V}{I_{avg}} = 3.06 n \sec$$

b) Determine the maximum frequency of the output signal.

Solution:

$$t_P = \frac{1}{2}(t_{PLH} + t_{PHL}) = \frac{1}{2}(3.06 + 1.46) = 2.26 n \sec$$

$$f_{\max} = \frac{1}{t_p} = 442 MHz$$

c) Calculate the dynamic power dissipation at this maximum frequency. Neglect any diffusion capacitance.

Solution:

$$P_{dyn} = \alpha_{0 \to T} C V_{DD}^2 \, f_{clk}$$

$$= (0.5 pF)(2.5V)^2 (442 \times 10^6 Hz) = 1.38 mW$$

d) Assume that the output load capacitance is mainly dominated by fixed fanout components (which are independent of $W_n$ and $W_p$). We want to re-design the inverter so that the propagation delay times are reduced by 25%. Determine the required channel dimensions of the NMOS and PMOS transistors. How does this re-design influence the dynamic power dissipation? Which of the two designs produces lower Power-Delay-Product?

Solution:

$$t_{pnew} = 0.75 \quad t_{pold} = 1.695 n \sec$$

**Reduce each,**

$t_{PLH}$ & $t_{PHL}$ by 25% $\rightarrow$ increase $\left(\frac{W}{L}\right)$ by $\frac{1}{0.75} = \frac{4}{3}$

So new channel dimensions are

$$\left(\frac{W}{L}\right)_n = \frac{8}{3}, \left(\frac{W}{L}\right)_p = \frac{16}{3}$$

$$t_{PLH} = 2.295\, n\text{sec}, \quad t_{PHL} = 1.095\, n\text{sec} \quad \rightarrow t_P = 1.695\, n\text{sec} \rightarrow f_{\max} = 590 MHz$$

The PDPs are exactly the same since the increase in frequency and power is compensated by same decrease in $t_P$.
Also there is no considerable change in C due to assumption of large fanout.

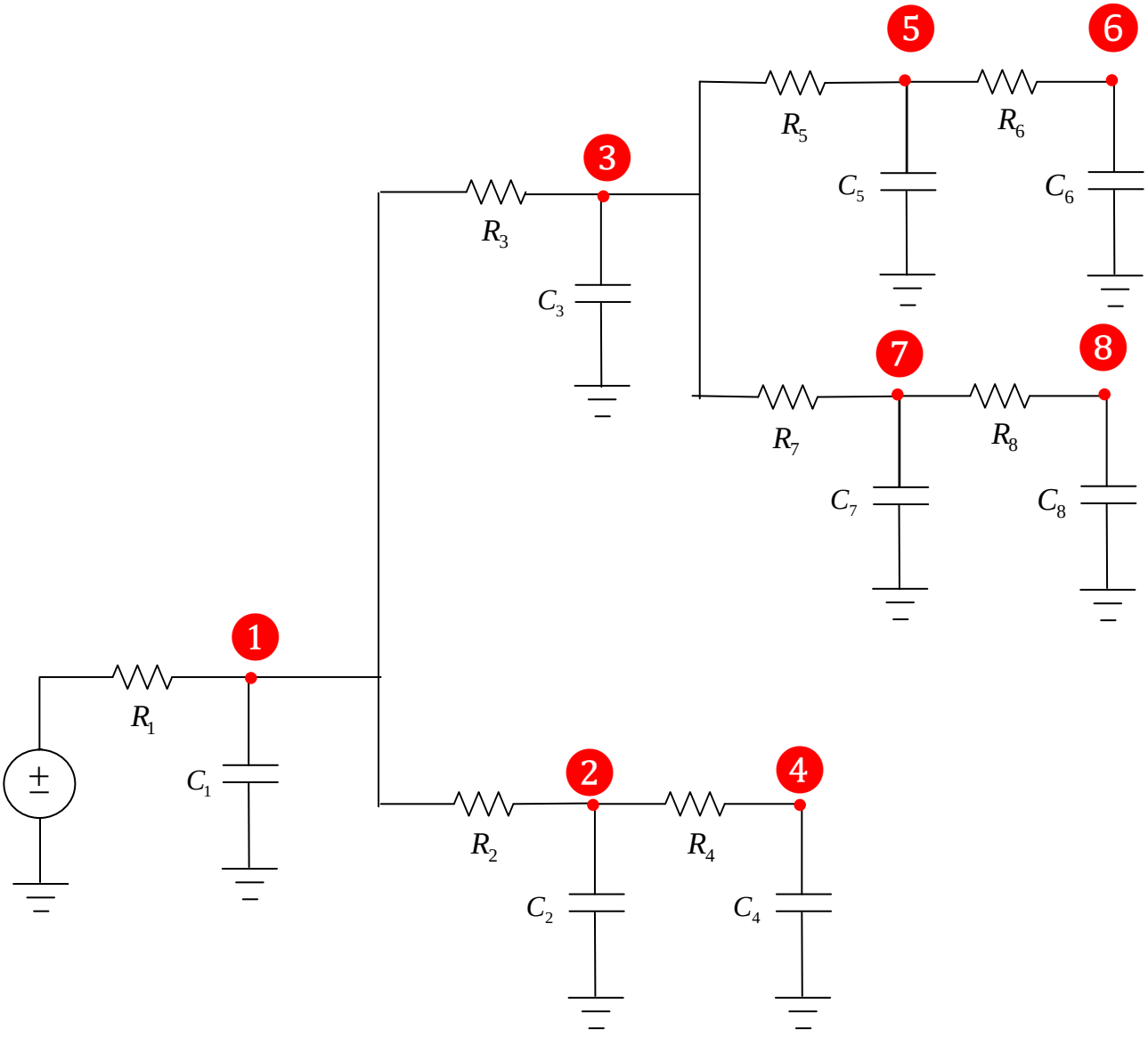
e) How does this re-design influence the switching threshold of the CMOS inverter?

Solution:

Both the nMOS and the pMOS were scaled by the same factor 4/3, the pMOS is still twice as big as the nMOS, therefore, that device should be the same (proportionally) as before. Thus V will be the same too.

PROBLEM 3: (30 points) **PROBLEM 3: (40 points)**

Use Elmore delay approximation to find the delay at nodes1,2,3,4,5,6,7,and 8 in the below RC circuit.



$$\tau_{V_1} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8)$$
$$\tau_{V_2} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_2(C_2 + C_4)$$
$$\tau_{V_3} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_3(C_3 + C_5 + C_6 + C_7 + C_8)$$
$$\tau_{V_4} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_2(C_2 + C_4) + R_4C_4$$
$$\tau_{V_5} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_3(C_3 + C_5 + C_6 + C_7 + C_8) + R_5(C_5 + C_6)$$
$$\tau_{V_6} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_3(C_3 + C_5 + C_6 + C_7 + C_8) + R_5(R_5 + R_6) + R_6C_6$$
$$\tau_{V_7} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_3(C_3 + C_5 + C_6 + C_7 + C_8) + R_7(C_7 + C_8)$$
$$\tau_{V_8} - v_{in} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8) + R_3(C_3 + C_5 + C_6 + C_7 + C_8) + R_7(C_7 + C_8) + R_8C_8$$
$$t_{delay} = 0.69\tau_{V_{in} - V_{node}}$$