University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

J. Rabaey

WeFr 2-3:30pm

Wednesday, April 9 , 7:00-8:30pm

EECS 141: SPRING 08—MIDTERM 2

NAME	Last First

SID	

Problem 1 (13):

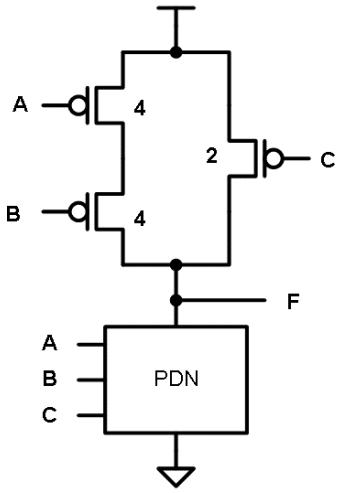
Problem 2 (17):

Problem 3 (12):

Total (42)	

Problem 1: Combinational Logic Gates (13 pts)

Given the PMOS pull-up network below:



a. Draw the NMOS pull-down network to complete the static CMOS gate. (2pt)

b. Size the pull-down transistors such that its worst-case drive strength is the same as a unit inverter (PMOS to NMOS ratio of 2/1) and that **all the input capacitances are the same**. (4 pt).

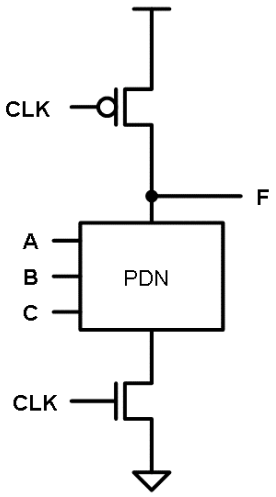
Pull-down network:

M_A =
M_B =
M_C =

c. What is the logical effort of this gate for each input? (1.5 pt)

LE_A =
LE_B =
LE_C =

Assume now that we want to implement the same function in a dynamic CMOS gate as shown below.



d. Draw the NMOS pull-down network such that it has the same logic function as the static CMOS gate in Part 1. (2 pt)

e. Size the transistors such that the worst-case drive strength for all inputs is the same as a unit 2/1 inverter. (2pt)

Pull-down network:

M_A =
M_B =
M_C =

f. What is the logical effort of this gate? (1.5pt)

LE_A =
LE_B =
LE_C =

Problem 2: Optimizing Complex Logic Networks for Speed (17 pts)

Throughout this problem you can assume the following: $\gamma = 1$ and the gate capacitance of a minimum sized NMOS = 1fF. *X, Y, Z* stands for the input capacitance of that particular gate and *min* means that this gate is sized such that is has equal driving strength to a minimum sized inverter with a NMOS to PMOS ratio of 1/2 (as assumed in class all the time)

One day your boss shows up on your office and shows you the logic network shown in Fig. 1. It turns out that it is the most critical part in the new super-processor your company is working on and he asks you to analyze the network and optimize it for speed.
The two critical paths are the ones from In1 to Out and from In2 to Out.

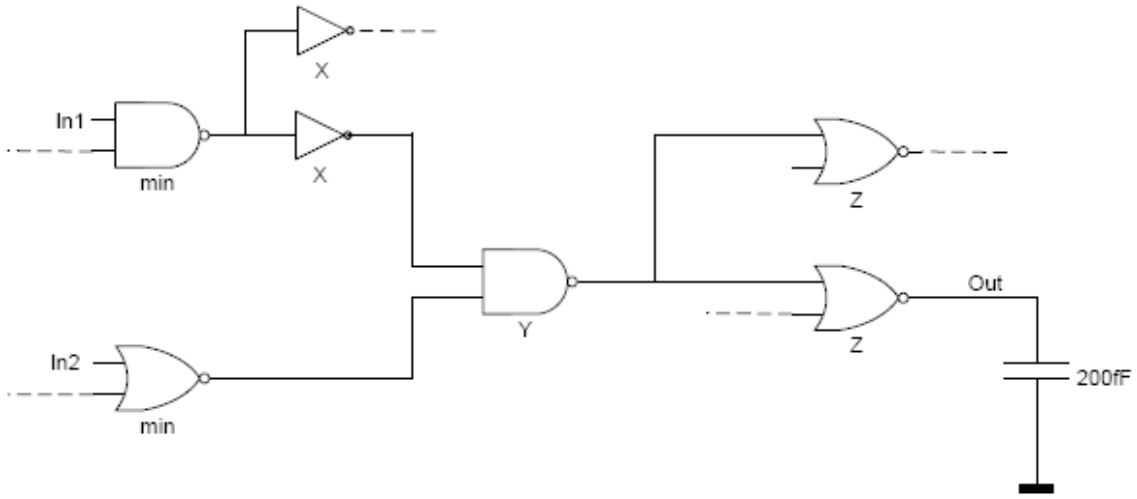


Figure 1: Logic network in need for speed

a) First you start analyzing the path from In1 to Out. In order to do so you calculate the path electrical fan-out F, the path logical effort LE, the path branching effort B, the total path effort PE as well as the optimal stage effort SE (You are assuming that you can optimize this path independently from the path In2 to Out). Finally, you estimate the total intrinsic delays along the path (Σp_i) and the minimum delay $t_{pin1\text{-}out,min}$ from In1 to Out in terms of $t_{inv.}$ (5 pt)

F =

LE =

B =

PE =

SE =

Σp_i =

$t_{pin1\text{-}out,min}$ =

b) You repeat the same for the path from In2 to Out. Again, you assume you can independently optimize that path for speed. (5 pt)

F =

LE =

B =

PE =

SE =

Σp_i =

$t_{pin2\text{-}out,min}$ =

c) Based on this information, you decide to optimize the delay of the critical (that is, the slowest) path by carefully sizing the transistors. (If the path between In2 and Out is the slower one, optimize Y and Z first and then optimize X to minimize the delay from In1 to Out without changing Z and Y). After you are done you also write down the actual delay of the path you just optimized. (4 pt)

X =

Y =

Z =

$t_{pinx\text{-}out}$ =

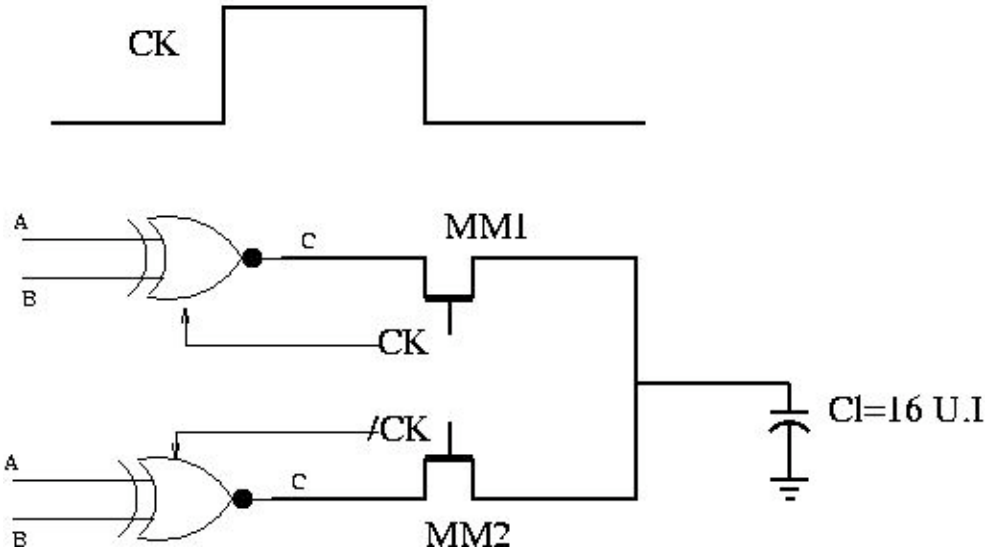
d) Based on the obtained transistor sizes, recalculate the delay of the second (faster) path. Is it still lower than the other one? In not, explain how this is possible. (3 pt)

$t_{piny\text{-}out}$ =

PROBLEM 3: Dynamic Logic (12 pts)

a. We would like to implement the functionality y= ~(A XOR B) (that is, XNOR) using **np-CMOS dynamic logic** so that the maximum performance is obtained. The A and B inputs are available from unity-strength (minimum size) buffers. The output C is loaded with a capacitance equal to 16 minimum-size inverters. For all gates in your design, you may assume that the parasitic delay p = 0. You may also assume that $\gamma = 1$, and a PMOS/NMOS driving strength ratio of 2.
Draw the circuit topology that would minimize delay, and annotate the relevant transistors sizes. (8 points). Explain your choices.

b. A clever engineer has figured out a way to further enhance the performance of this circuit. He proposes a ping-pong approach, as shown below. The logic is replicated in two paths, activated on opposite clock phases. Transistors MM1 and MM2 are used to connect the load Cl to the top gate during its evaluation period (CLK =1) and to the bottom gate during its evaluation period (CLK=0).



- Explain why this may be an interesting idea and why it may help to increase performance (2 pts)

- Also identify a potential (major) problem with the proposed circuit. Can you propose a solution for it? (2 pts)
Hint: think about the potential pitfalls of dynamic circuits.