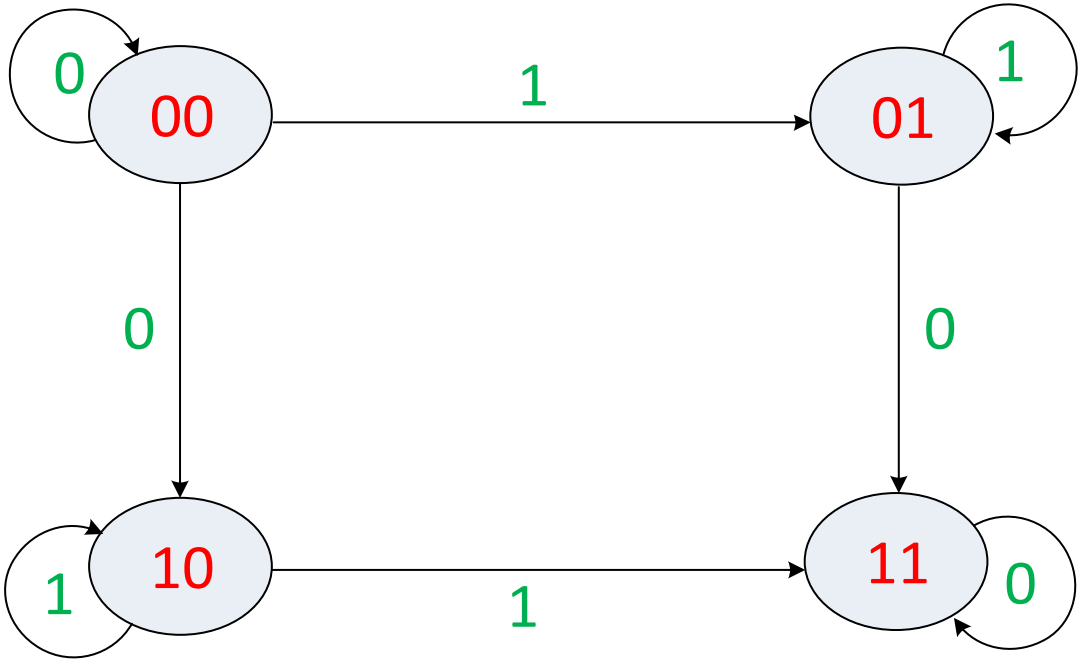
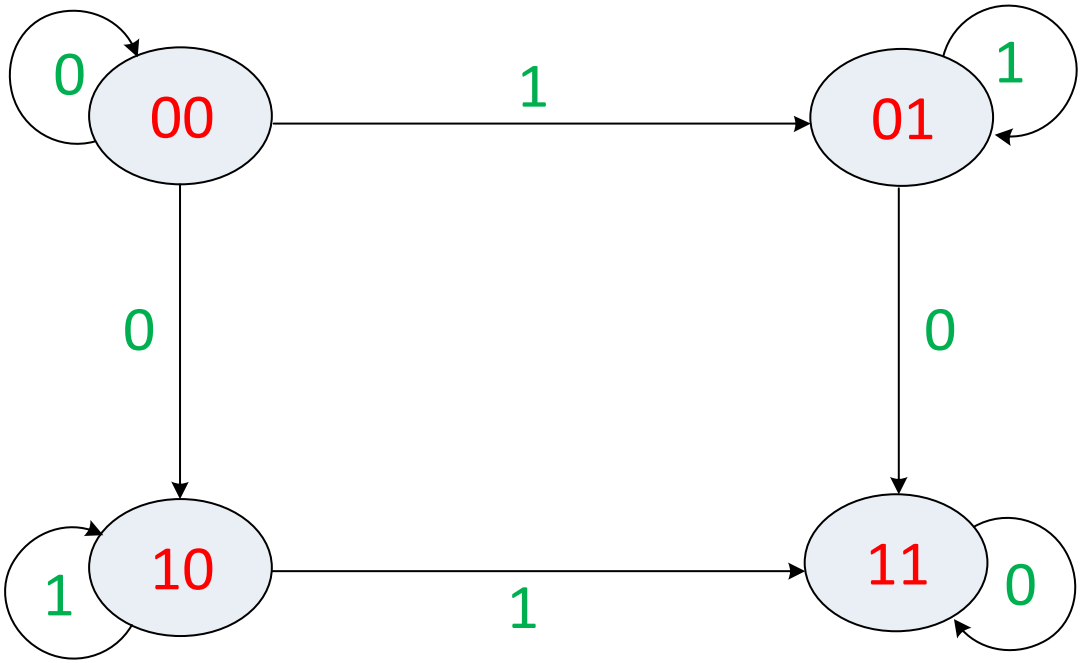
Sequential Circuit

Lecture 16

- Finite State Machine:
- Four states: 00, 01,10,and 11 represented by two bits: $S_0 S_1$
- One input i with values 0, and 1.
- Transition structure:

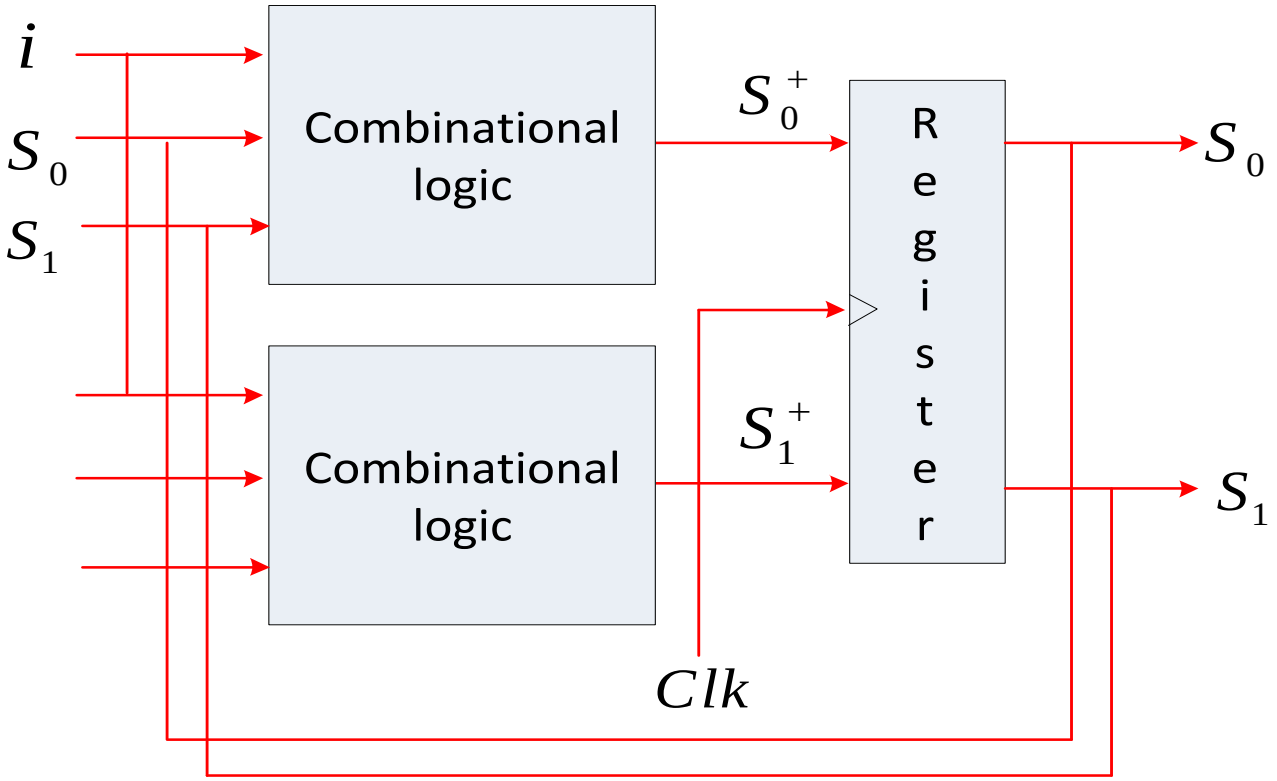


- Finite State Machine:
- Truth table:

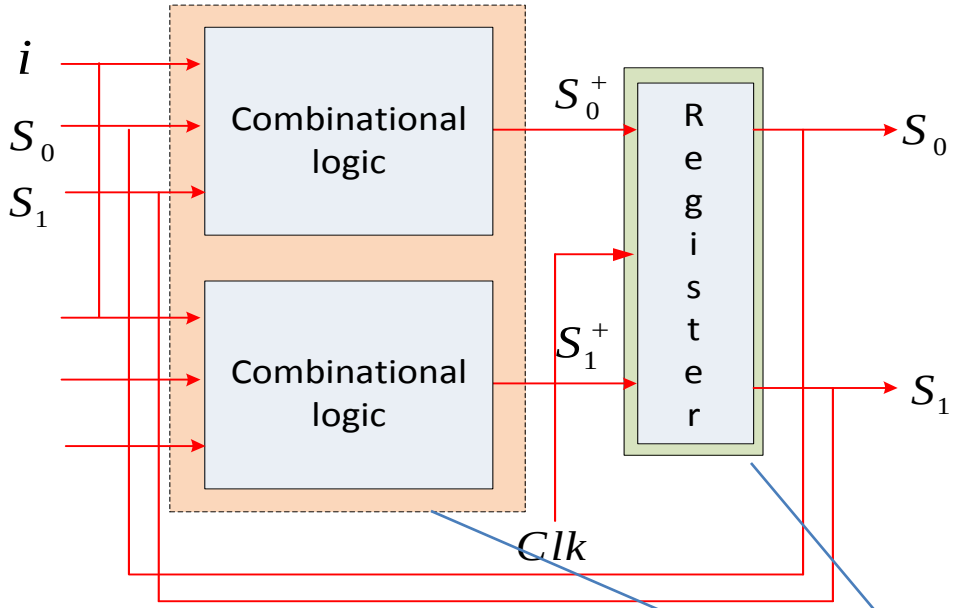


i	S_0	S_1	S_0^+	S_1^+
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

- Finite State Machine:
- Implementing the two Boolean variable $S_0 S_1$.
- Stored in the register

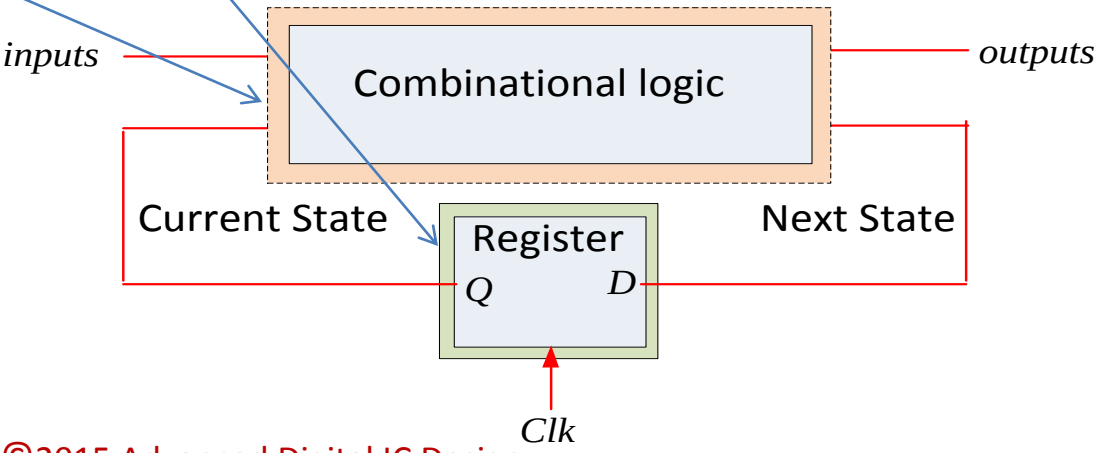


- Finite State Machine:

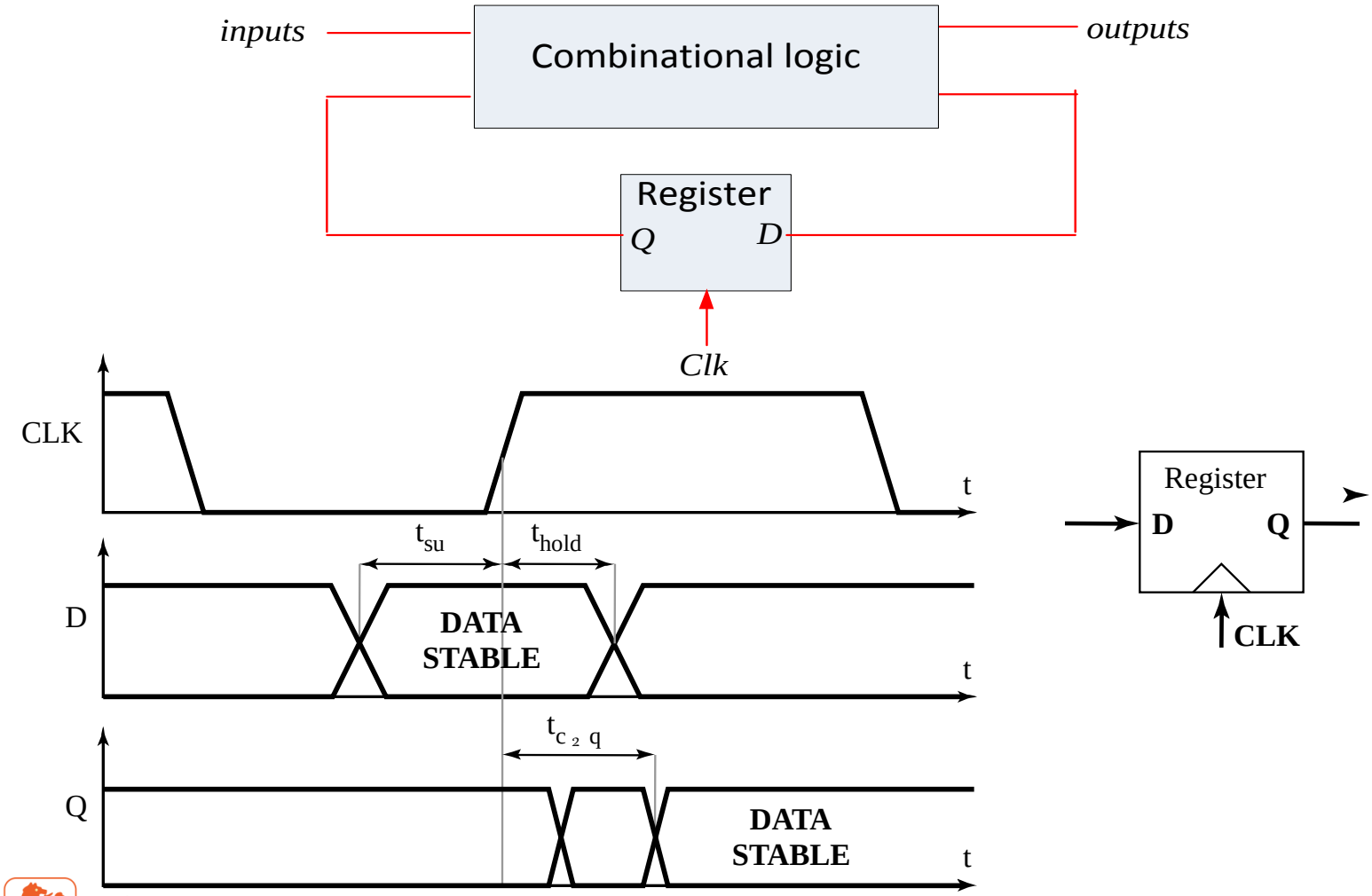


i	S_0	S_1	S_0^+	S_1^+	Q_1	Q_2
0	0	0	0	0		
0	0	1	1	1		
0	1	0	0	0		
0	1	1	1	1		
1	0	0	0	1		
1	0	1	0	1		
1	1	0	1	0		
1	1	1	1	0		

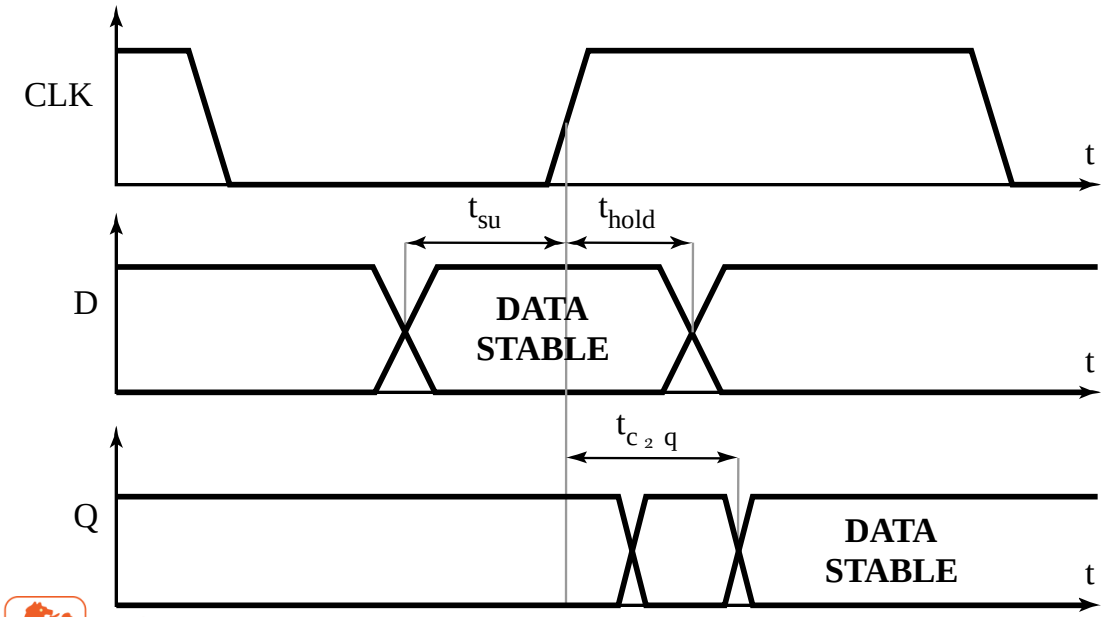
- Mealy Machine

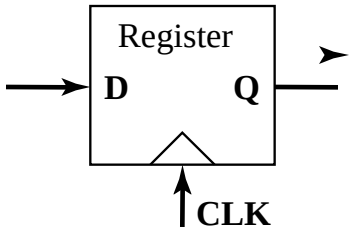


- Timing definition:

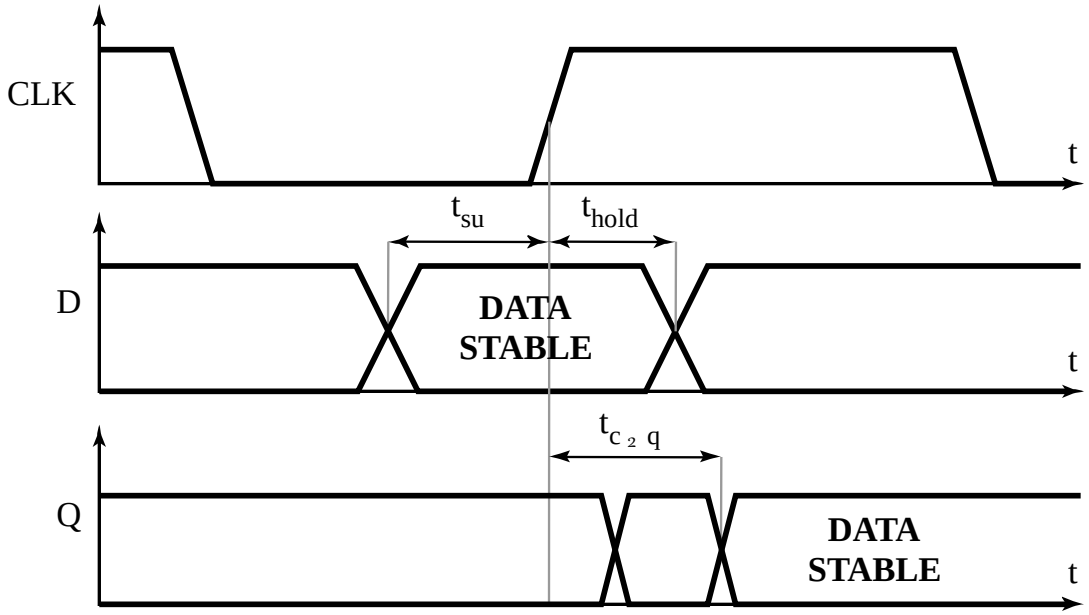


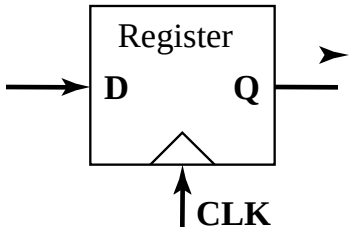
- Timing definition:
- ❶ Set–up time t_{su} : the duration that data inputs (D) must be valid before the clk transition edge.
- ❷ Hold time t_{hold} : the duration that data inputs (D) must be valid after the clk transition edge.
- ❸ The propagation delay t_{c2q} : the worst-case propagation delay the data at D is copied to Q reference to clk



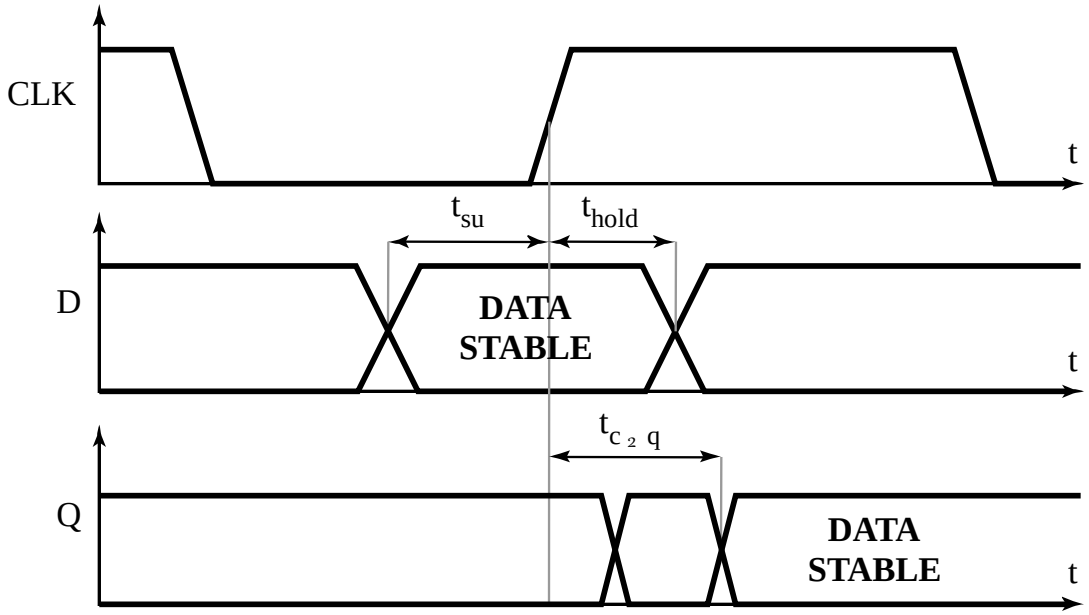


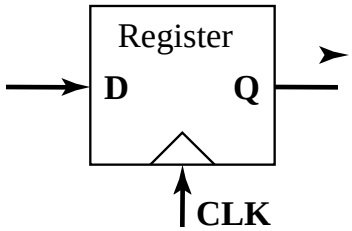
- Timing definition:
- The switching take place concurrently in response to a clock stimulus in the synchronous sequential circuit.
- Result of operations await the next till next clock transition before progressing to the next stage.





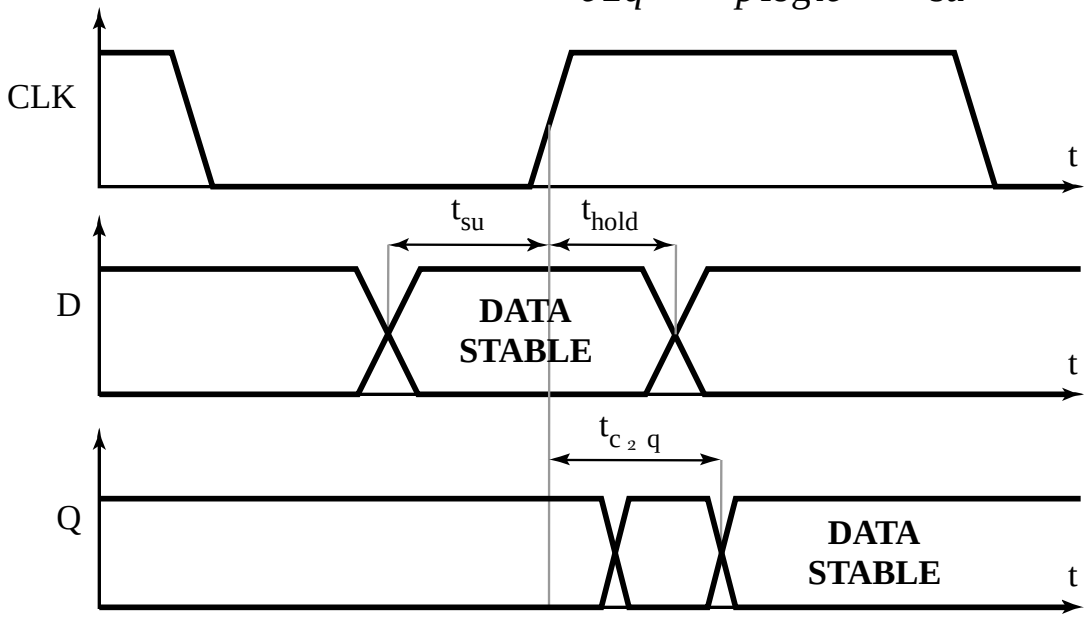
- Timing definition:
- All current computation must complete and the system has to come to rest before next cycle can begin.
- The clock period T at which the sequential circuit operates, must accommodate the longest delay of any stage in the network.

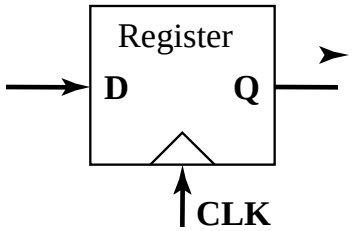




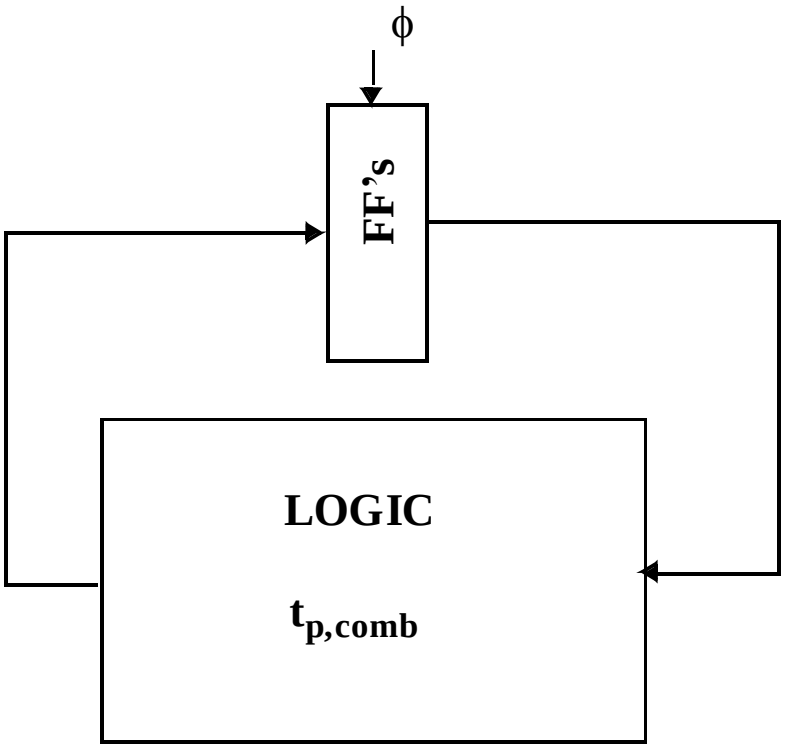
- Timing definition:
- The worst delay propagation delay of the logic: t_{plogic}
- The minimum delay of the logic (contamination delay): t_{cd}
- Constraint 1 : The minimum clock period T

$$T \geq t_{c2q} + t_{plogic} + t_{su}$$





- Maximum clock Frequency:



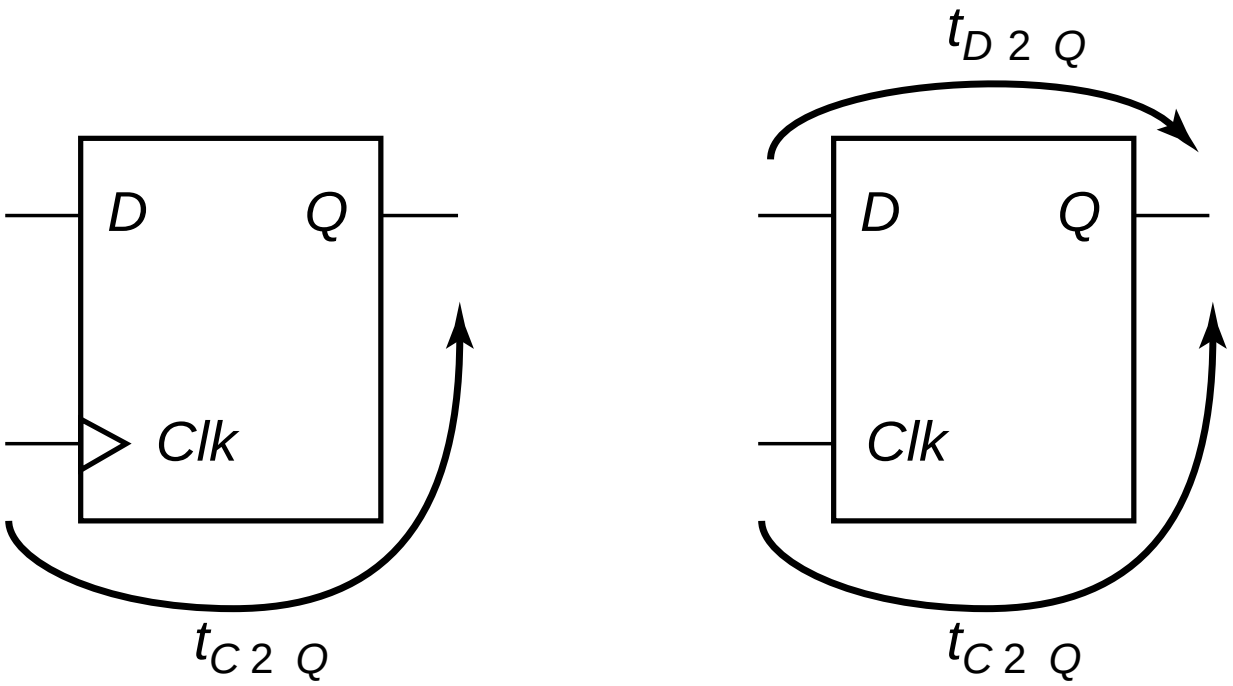
$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$

Also:

$t_{cdreg} + t_{cdlogic} > t_{hold}$

t_{cd}: contamination delay = minimum delay

- Characteristic Timing:

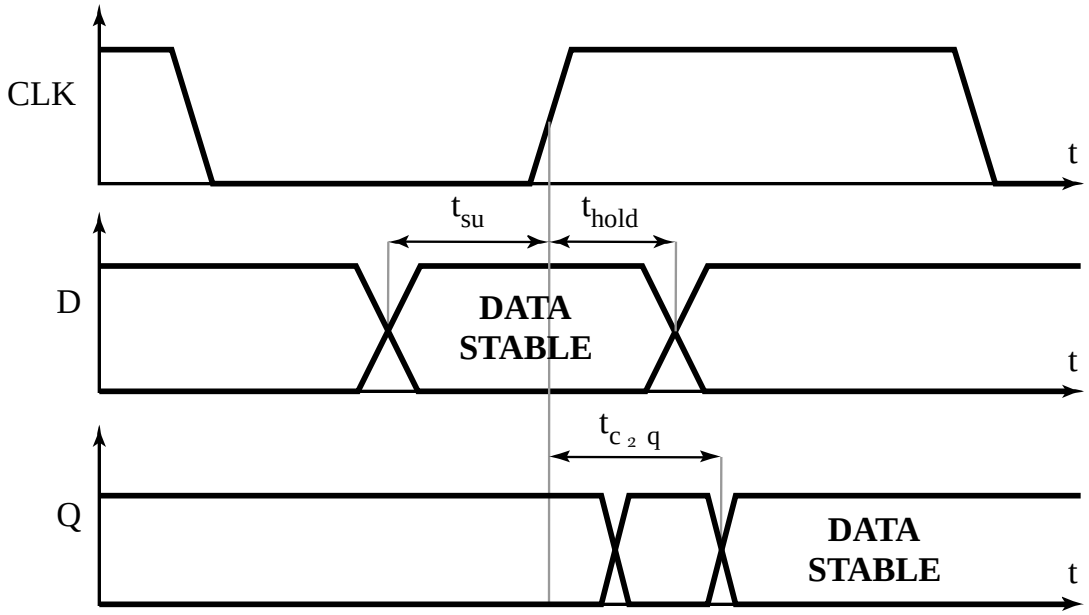


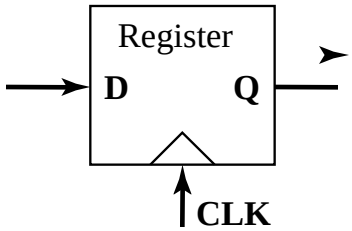
Register

Latch

- Timing definition:
- The the minimum propagation delay of the register $t_{cd\text{register}}$
- Constraint 2 : The hold time of the register.

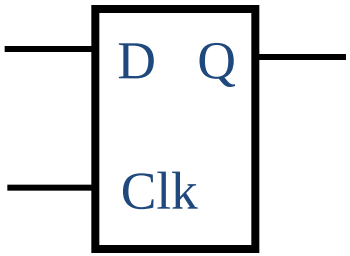
$$t_{cd\text{register}} + t_{cd\text{logic}} \geq t_{hold}$$

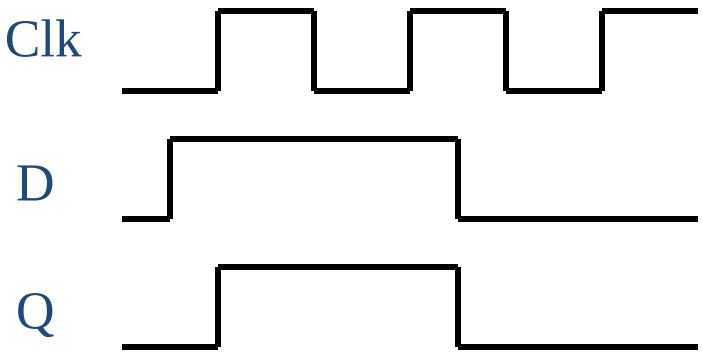




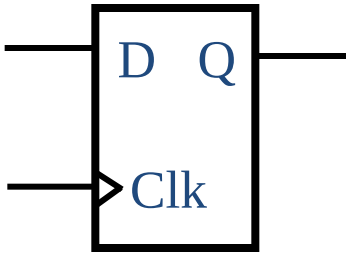
- Memory classification:
- ❶ Foreground: embedded into the logic.
- ❷ Background: large centralized memories
- Memory classification:
- ❶ Static: preserve the state as long as power is on. They are regenerative, positive feedback.
- ❷ Dynamic: large centralized memories. Store data for short period time. Temporary charge storage in MOS parasitic capacitors.

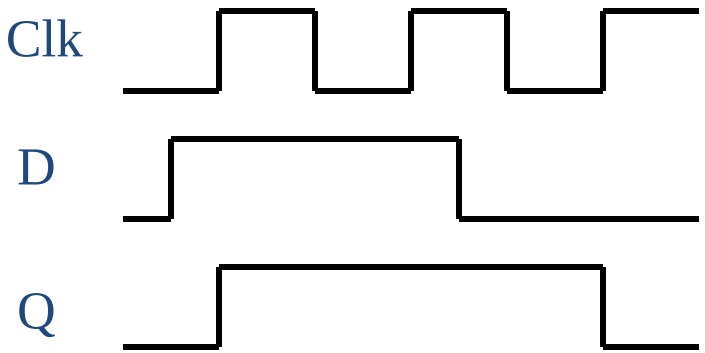
- Register (Flip-flop}: An edge-triggered storage elements. Any bistable component formed by the cross coupling of gates.
- Latch: a level sensitive device.
- Latch stores data when Clk is low.



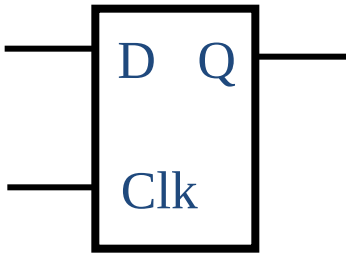


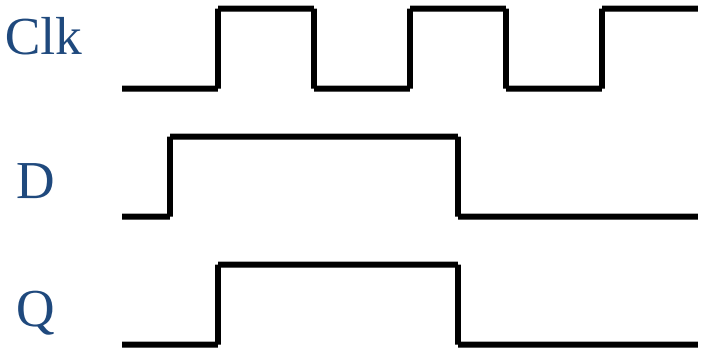
Register stores data when Clk rises.



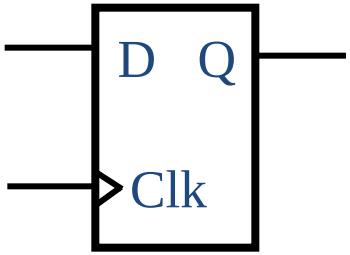


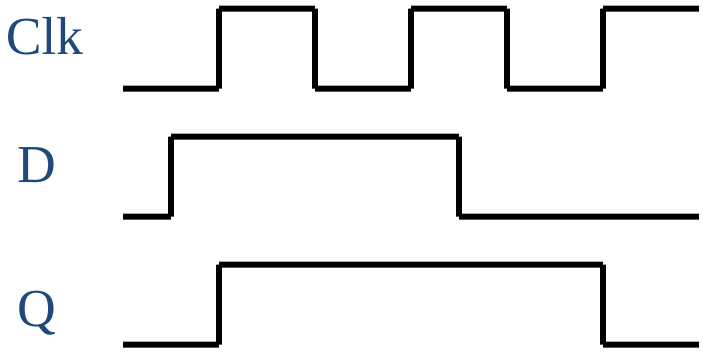
- Latch stores data when Clk is low.



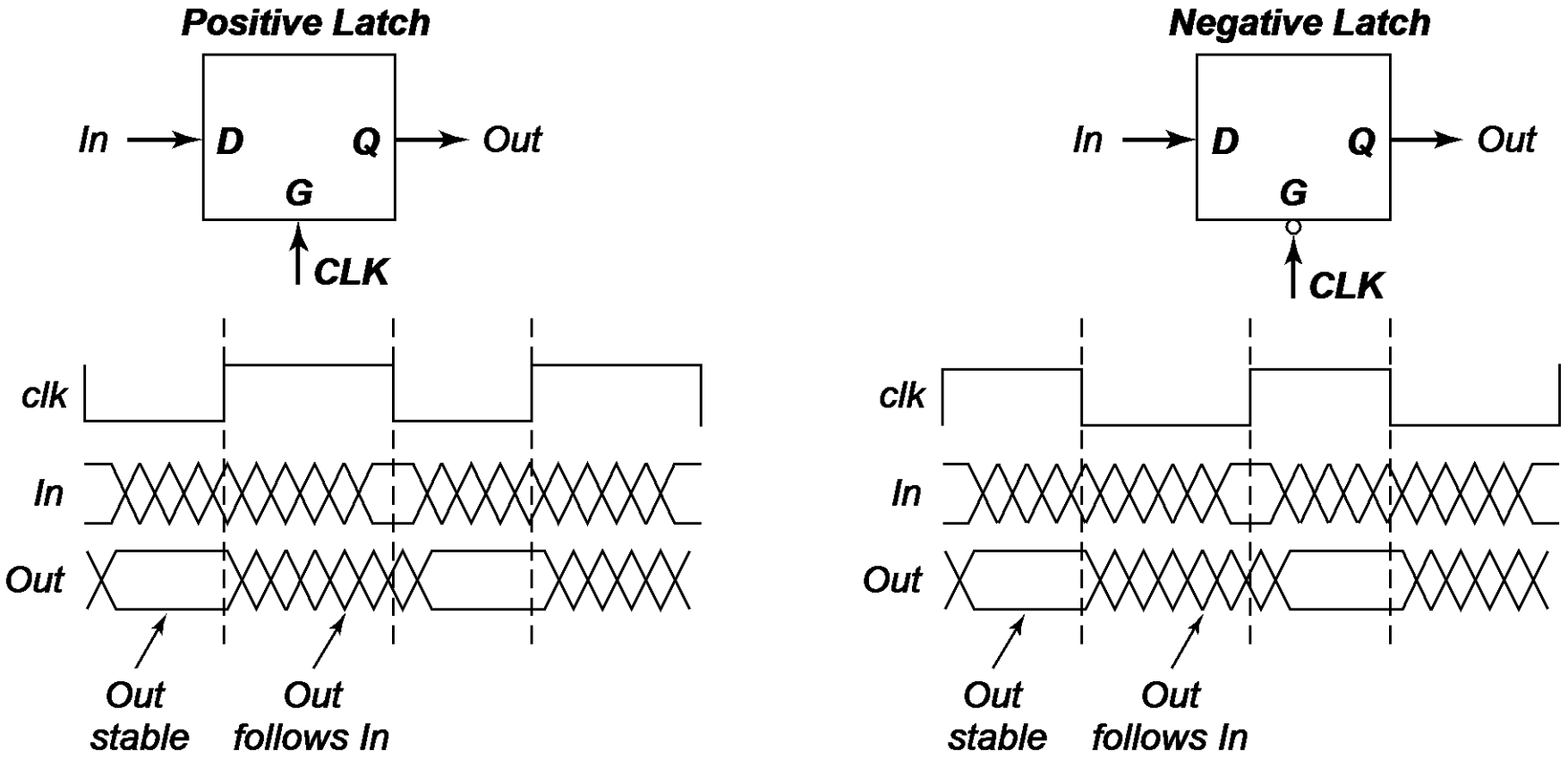


Register stores data when Clk rises.



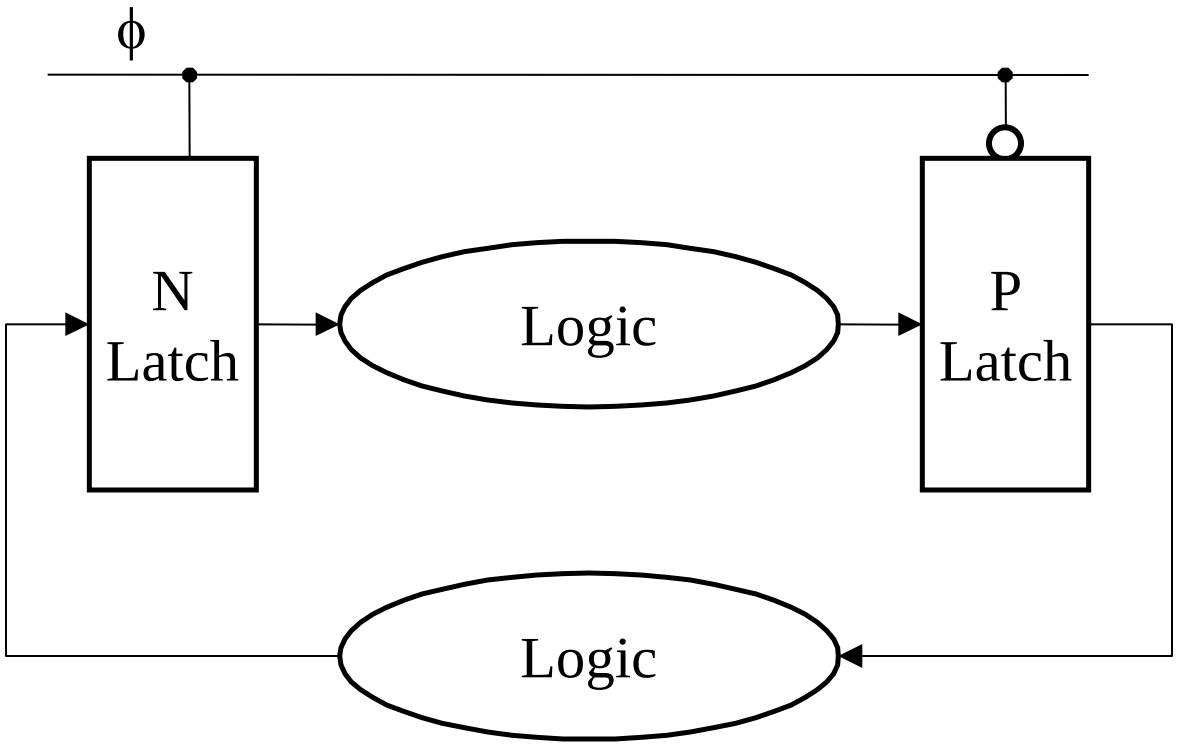


- Latches

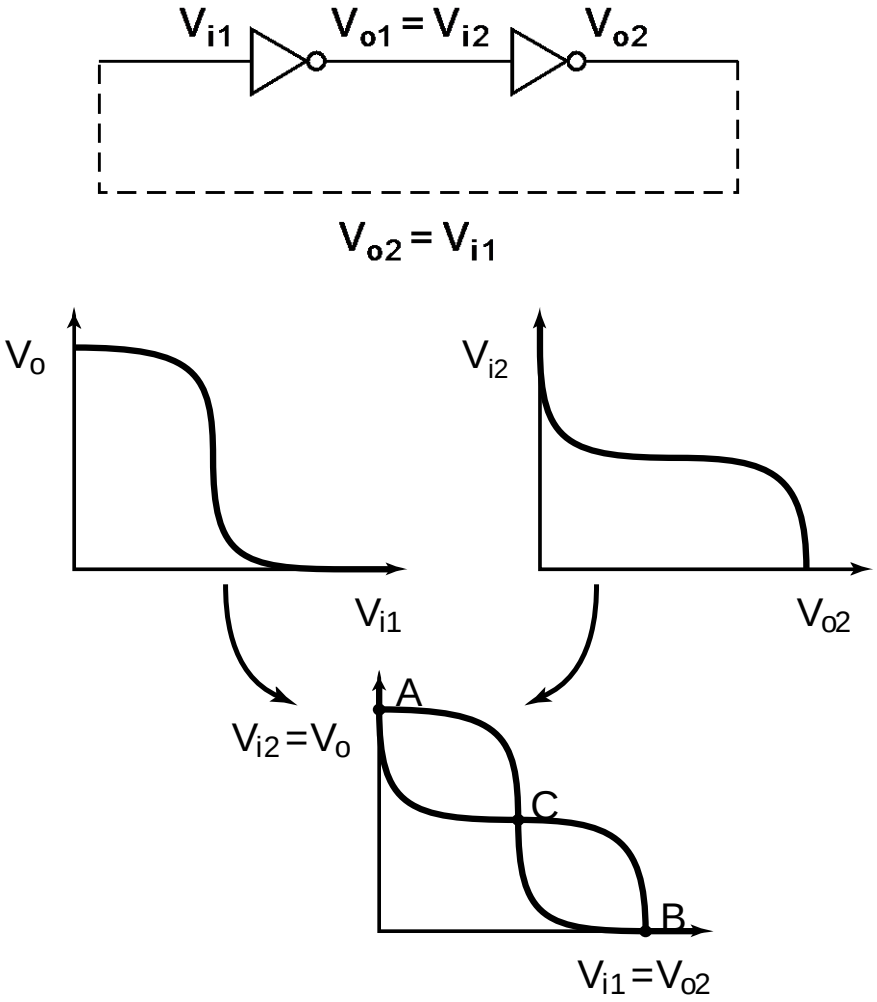


- A Positive Latches (Transparent High)
- Clk: High
- Pass the D-input to Q-output (transparent mode)
- Clk: Low
- The input data sampled on the falling edge of Clk is held stable at the output for the entire phase. (latch in hold mode)
- A Positive Latches (Transparent low)
- Clk: low
- Pass the D-input to Q-output (transparent mode)
- Clk: Low
- The input data sampled on the falling edge of Clk is held stable at the output for the entire phase. (latch in hold mode)

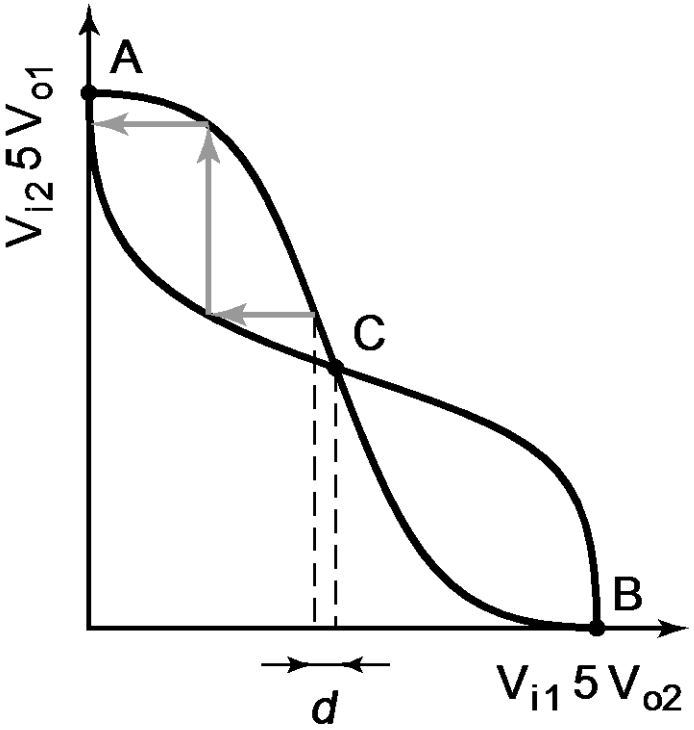
- Latch-based design:
- N latch is transparent when $\phi = 0$
- P latch is transparent when $\phi = 1$

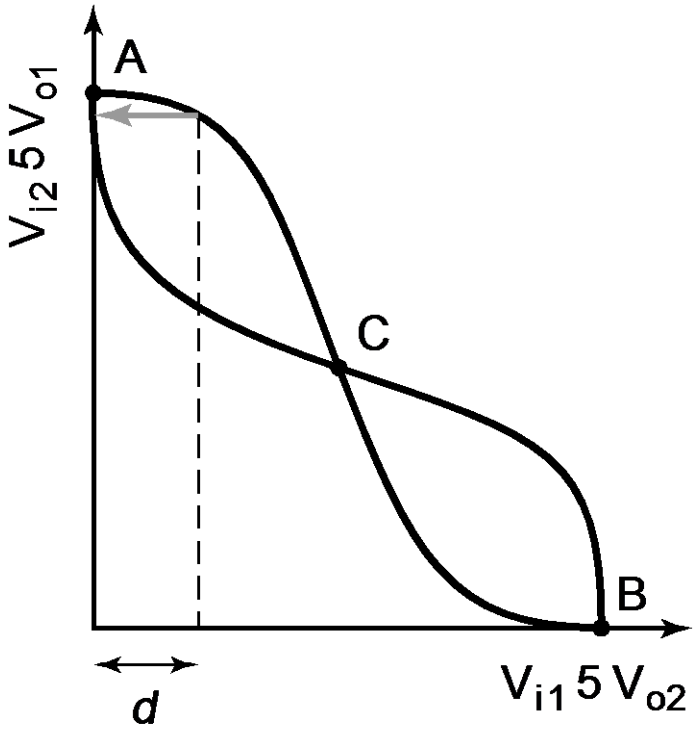


- Positive Feedback: Bistability



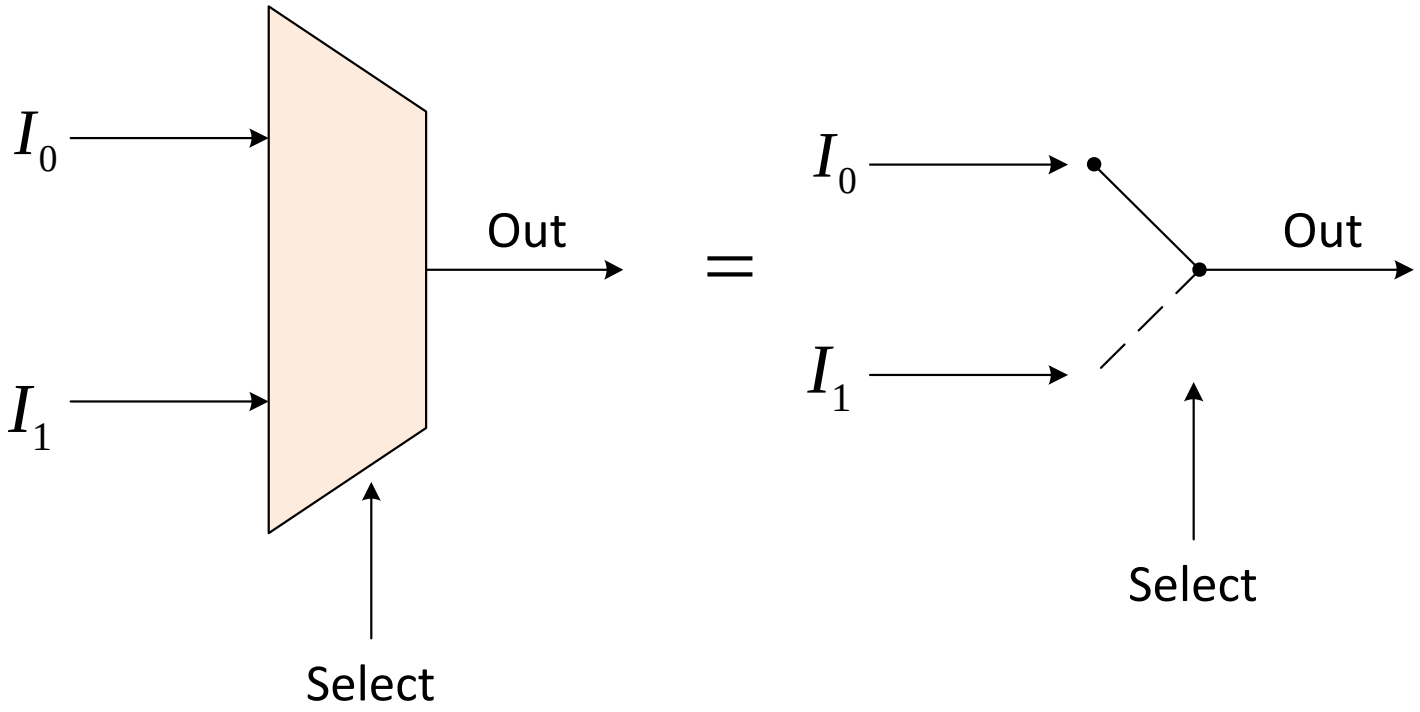
- Cross-coupled inverter is biased at point metastable C.





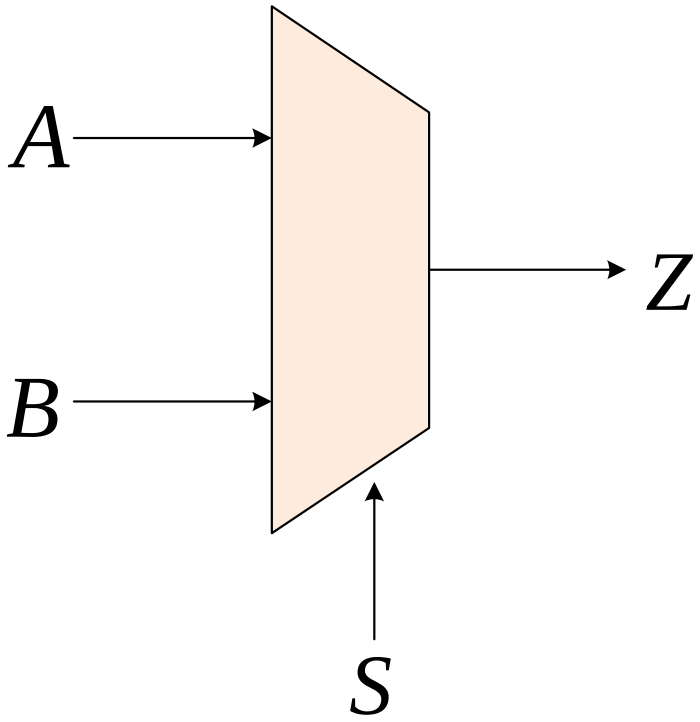
- Gain should be larger than 1 in the transition region A and B are the only stable state
- d is applied to V_{i1}

- Multiplexer (Data Selector)



- Multiplexer (Data Selector)
- Boolean equation

$$Z = A.\overline{S} + B.S$$



S	A	B	Z
0	1	1	1
		0	1
	0	1	0
		0	0
1	1	1	1
		0	0
	0	1	1
		0	0

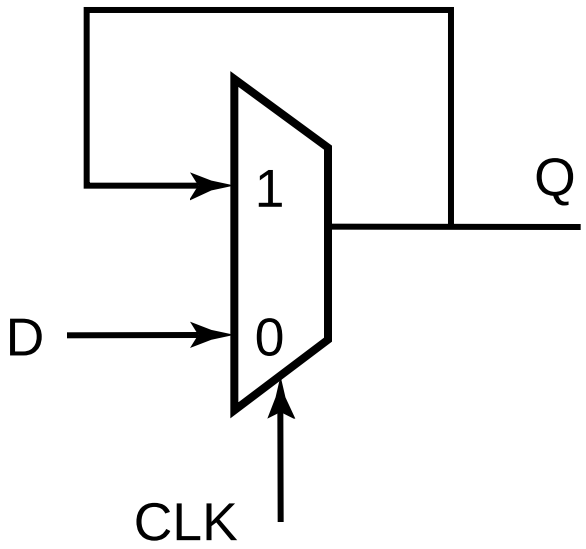
S	Z
0	A
1	B

- Multiplexer (Data Selector)

s	a	b	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

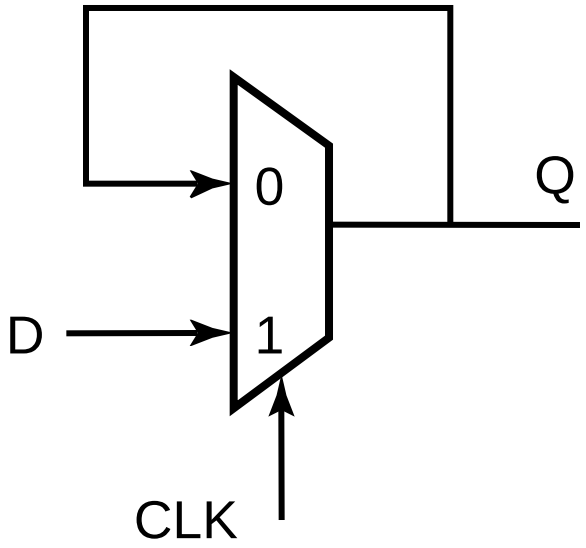
- Mux-based Latches

Negative latch (transparent when CLK= 0)



$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

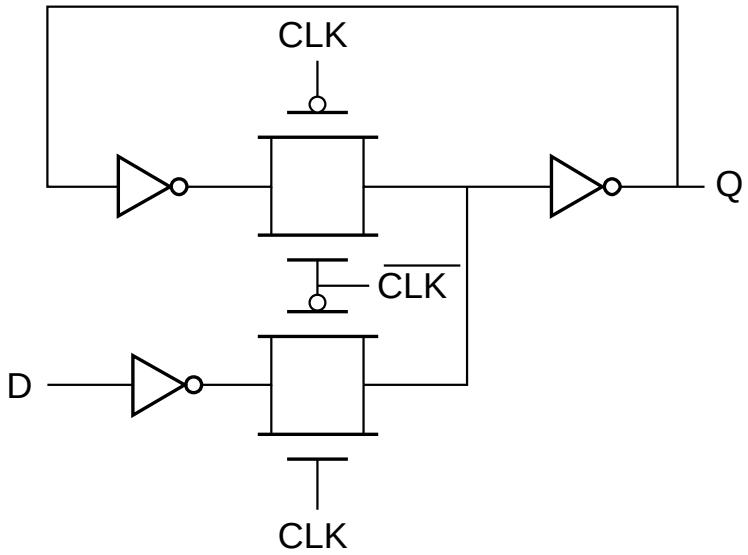
Positive latch (transparent when CLK= 1)



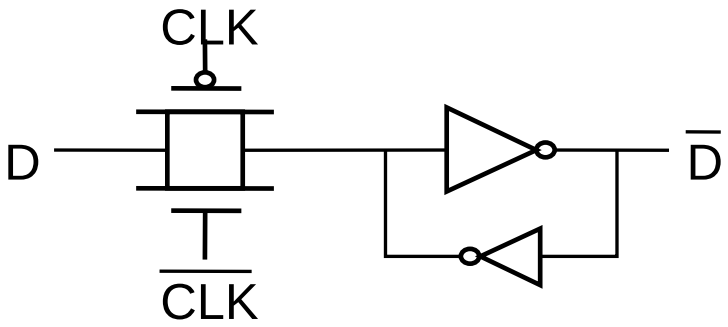
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

- Writing into a static latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

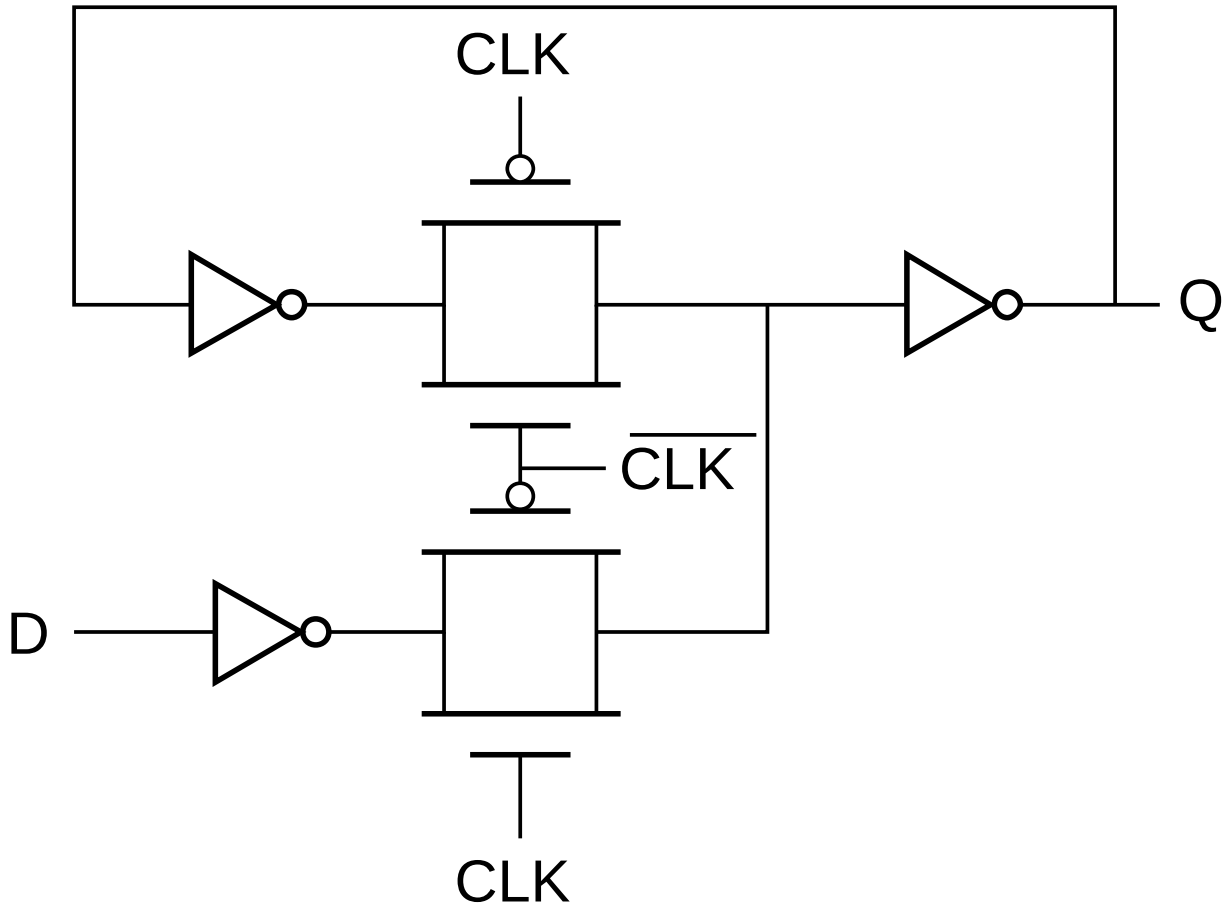


Converting into a MUX

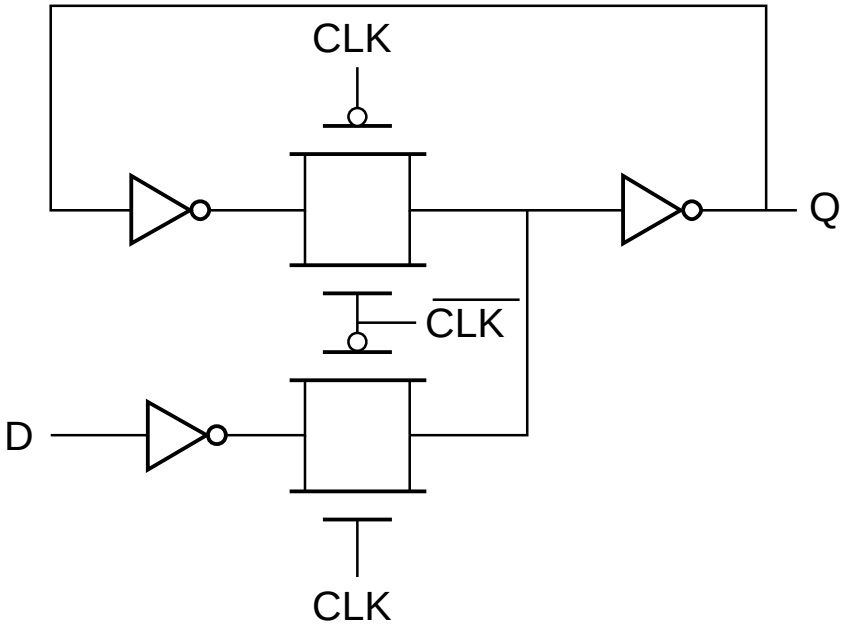


Forcing the state
(can implement as NMOS-only)

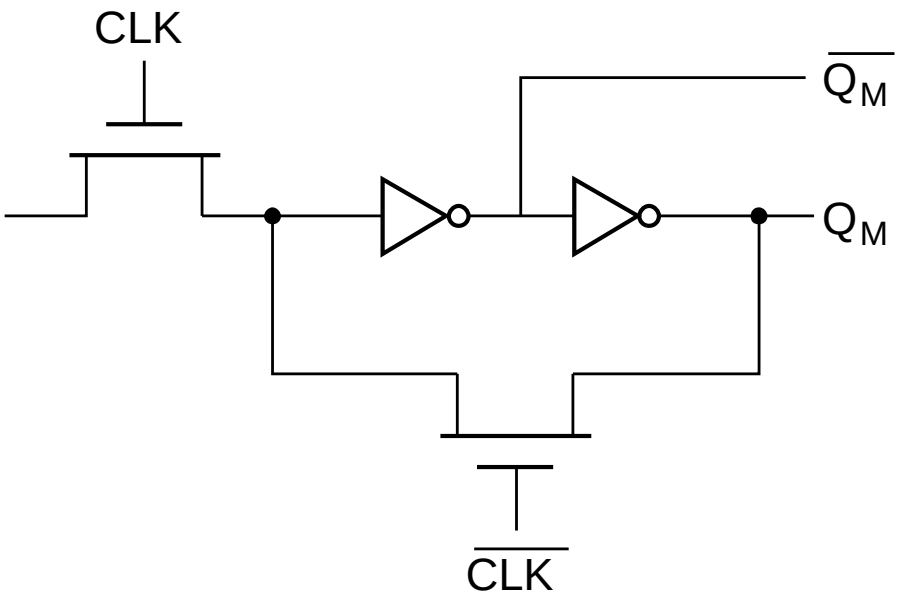
- Mux-based positive Latch



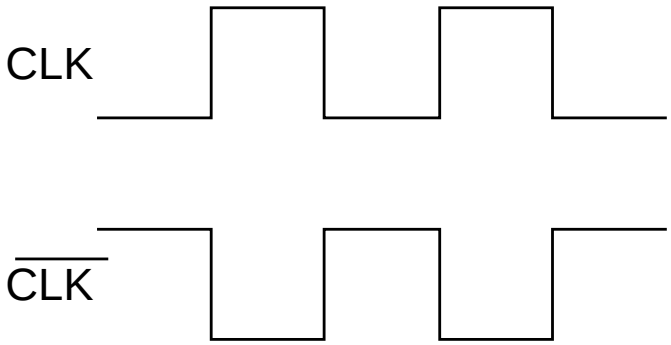
- Mux-based positive Latch operation:
- Clk high, bottom transmission gate is ON and the latch is transparent. –D input is copied to Q output-
- Top transmission gate is OFF Feedback loop is open
- It is not very efficient - It present
- the load of 4 transistors to the clock-.



- Mux-based nMOS-only Latches

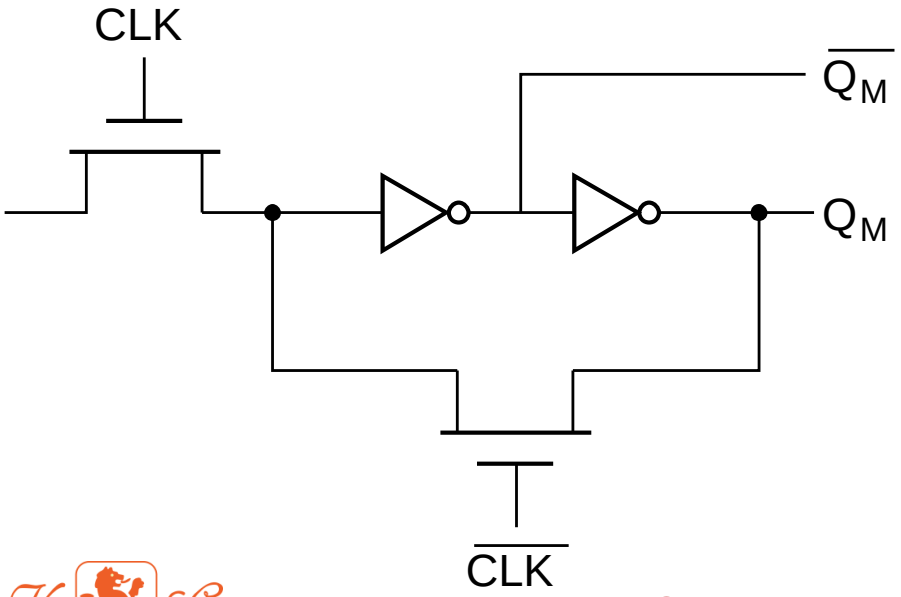


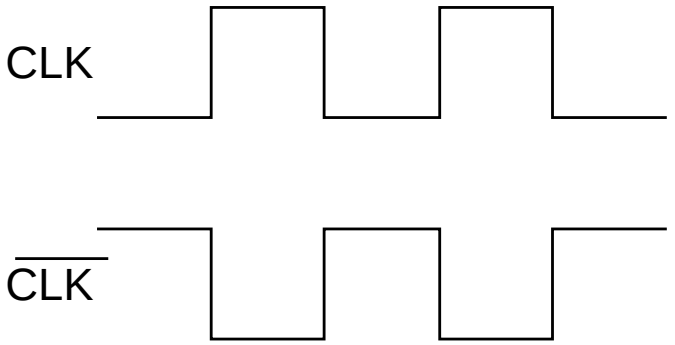
NMOS only



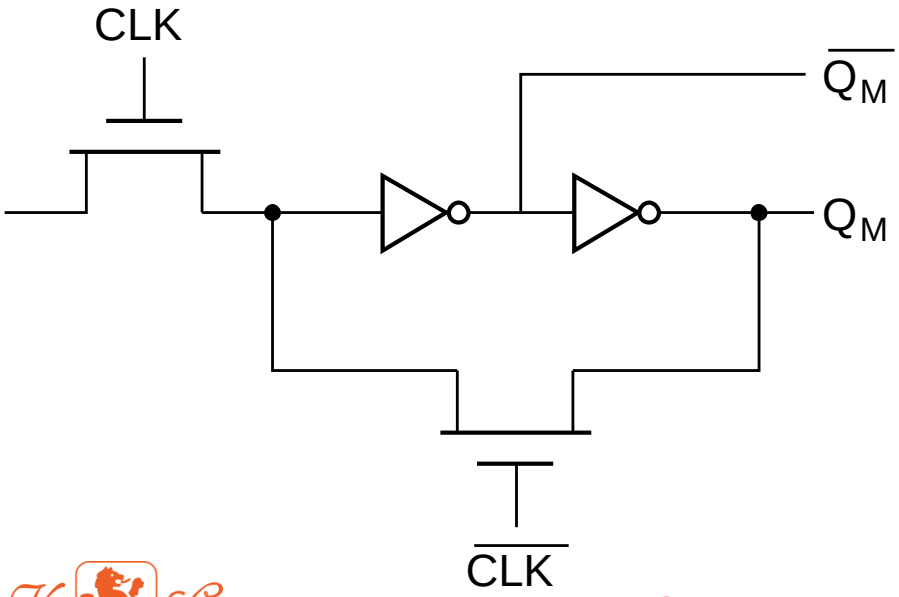
Non-overlapping clocks

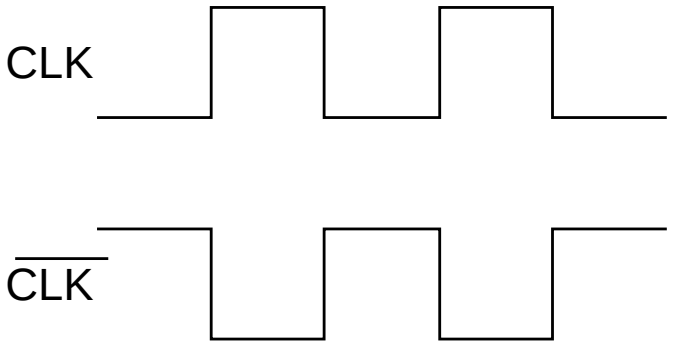
- Mux-based nMOS-only Latches
- Clk: high, the latch samples the D input.
- Clk: low enables the feedback loop, and puts the latch in the hold mode.
- Disadvantages: It pass the degraded high voltages of $V_{DD} - V_{Tn}$
- To the input of the first inverter. .



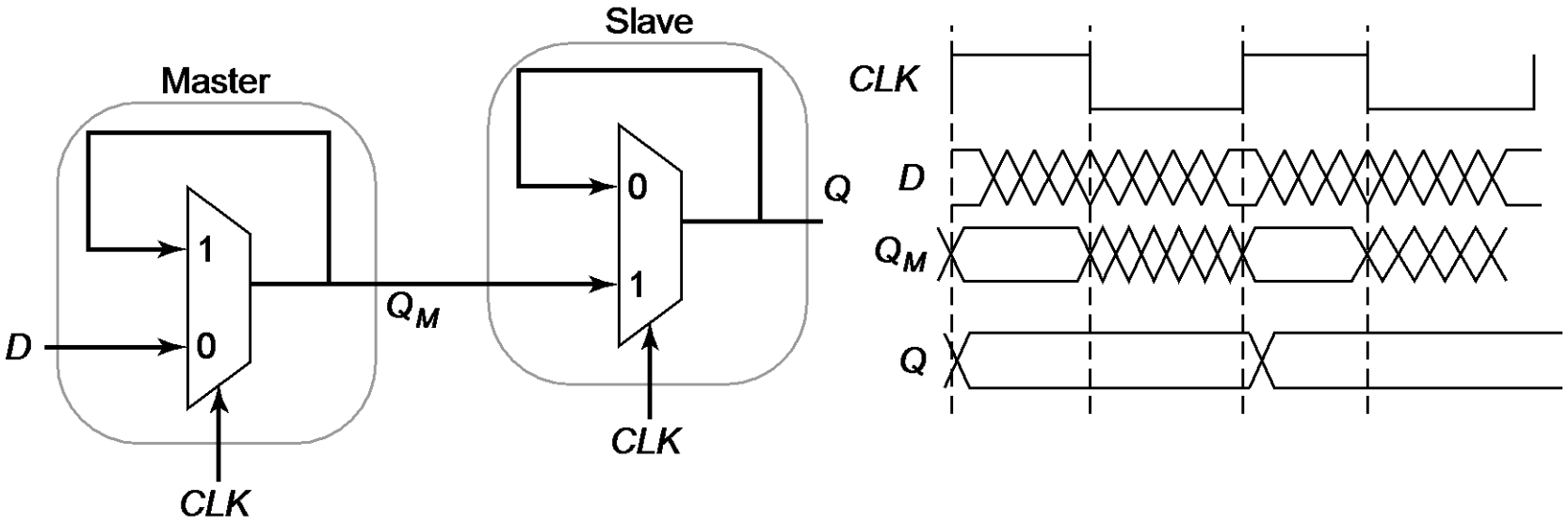


- Mux-based nMOS-only Latches
- Disadvantages: It pass the degraded high voltages of
- to the input of the first inverter.
- Impact noise margin and switching performance.
- Static power dissipation because the maximum voltage equals $V_{DD} - V_{Tn}$ and the pMOS of inverter never fully OFF





- Master-slave (edge-triggered} Register:

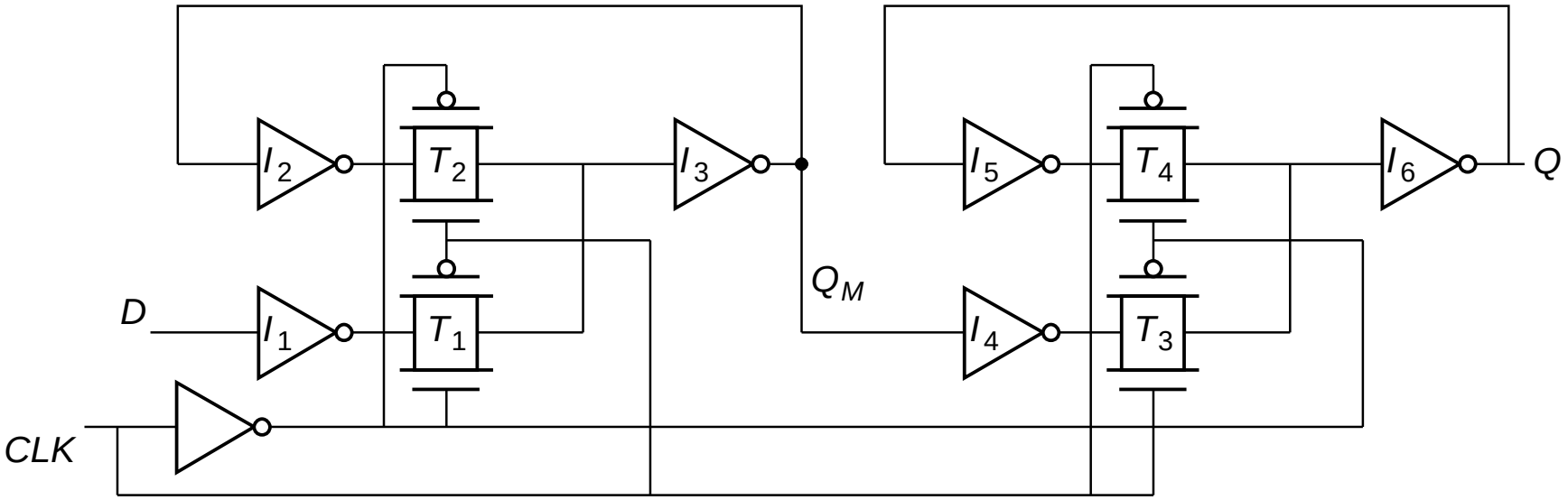


- Cascading a negative and positive latches.

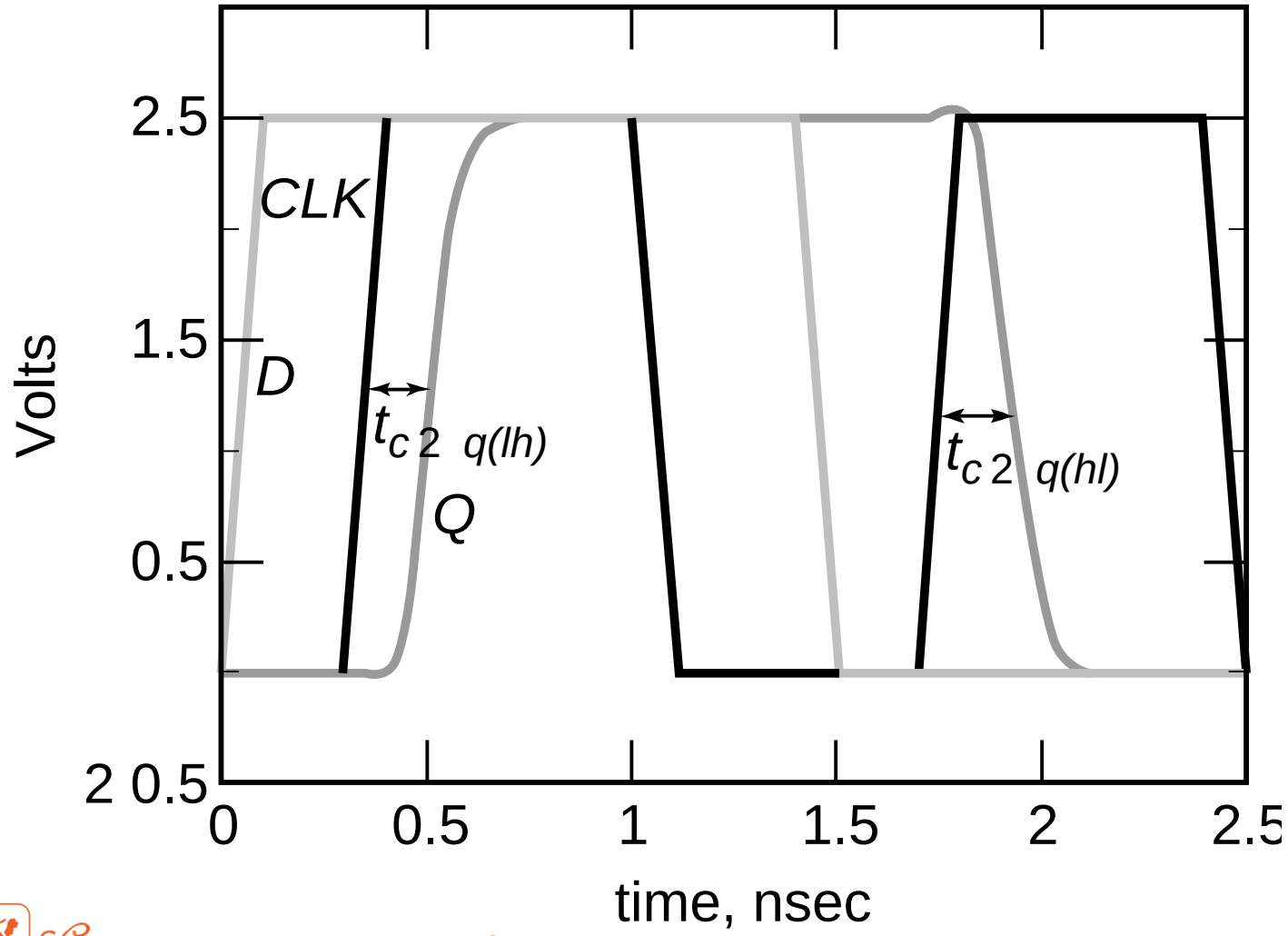
Two opposite latches trigger on edge
Also called master-slave latch pair

- Master-slave (edge-triggered) Register:

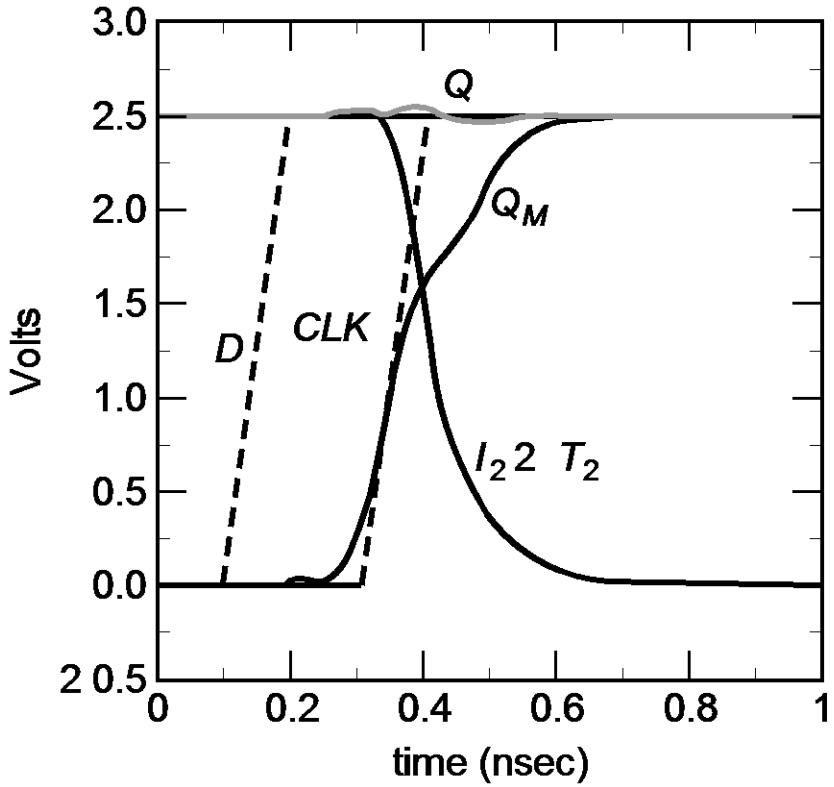
Multiplexer-based latch pair



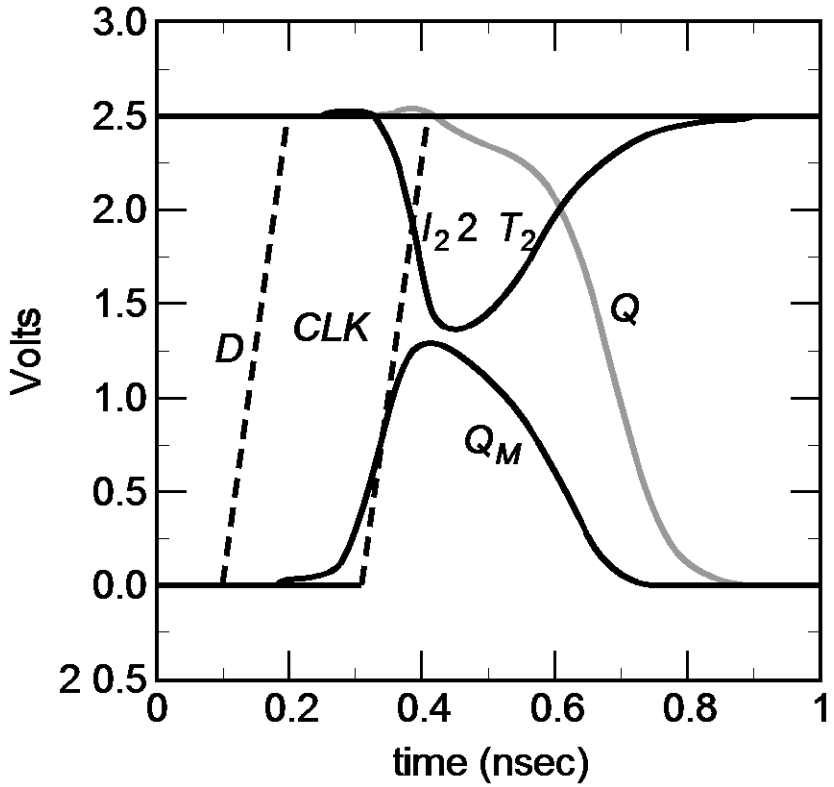
- Clk-Q delay:



- Set-up time:

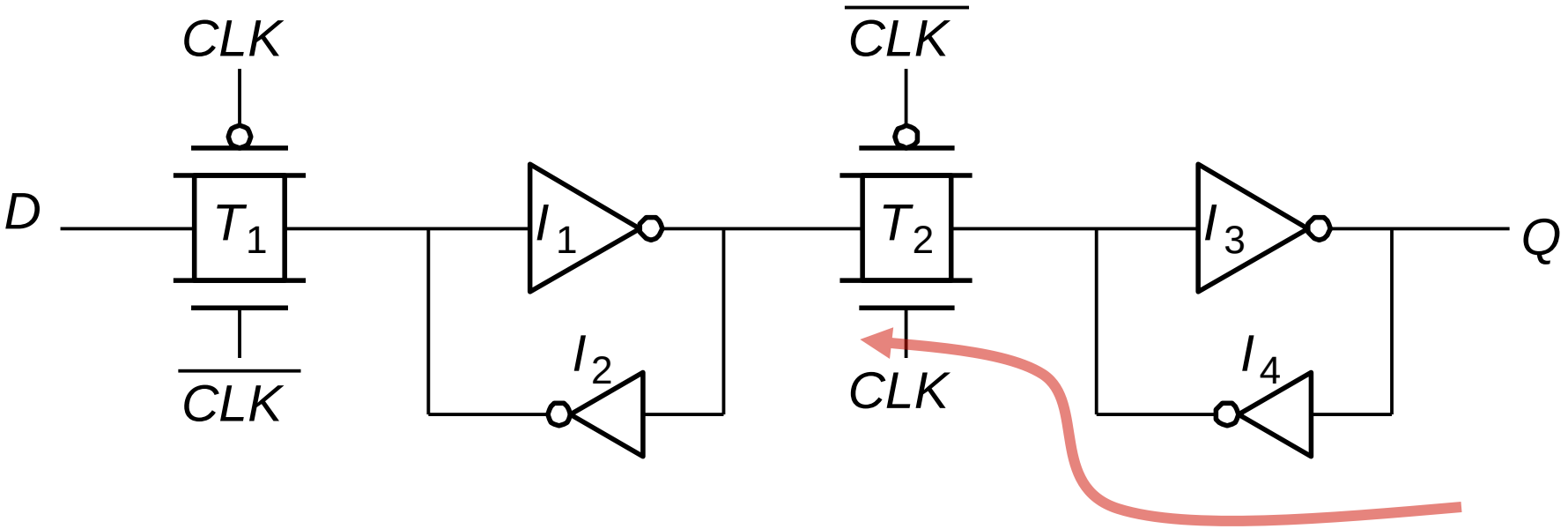


(a) T_{setup} 5 0.21 nsec

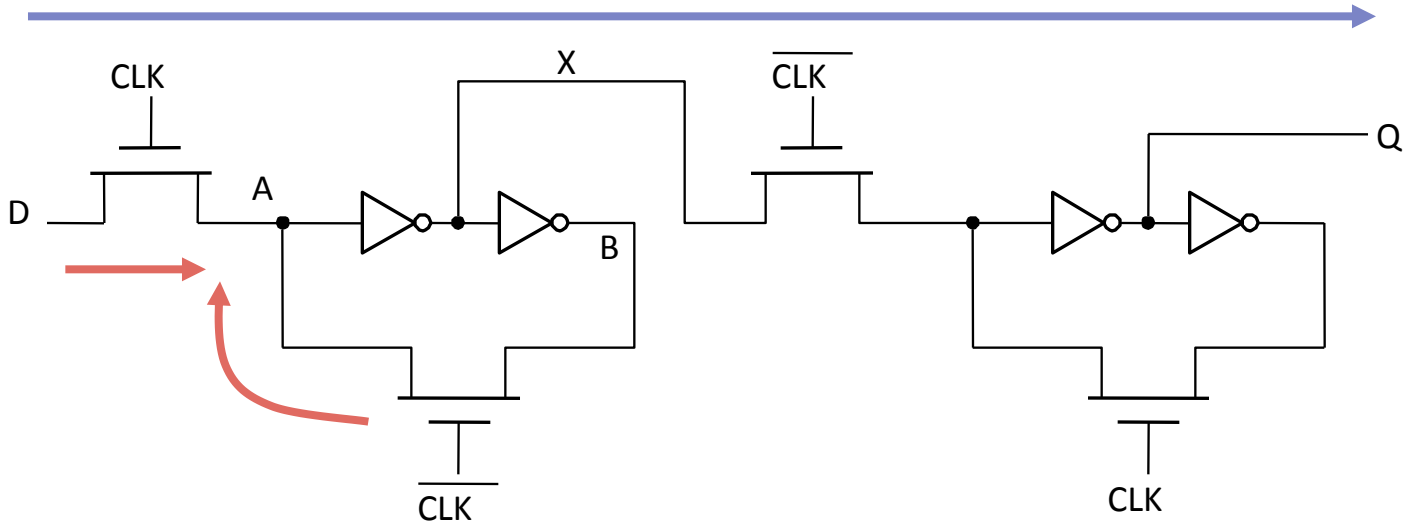


(b) T_{setup} 5 0.20 nsec

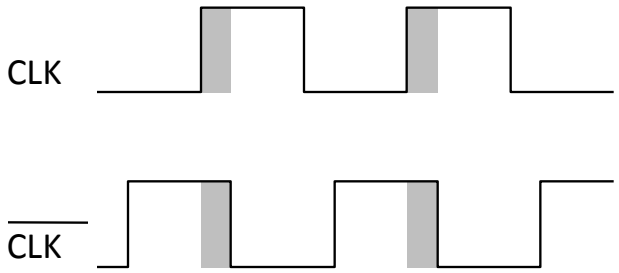
- Reduced clock load master=slave register:



- Avoiding clock overlap:



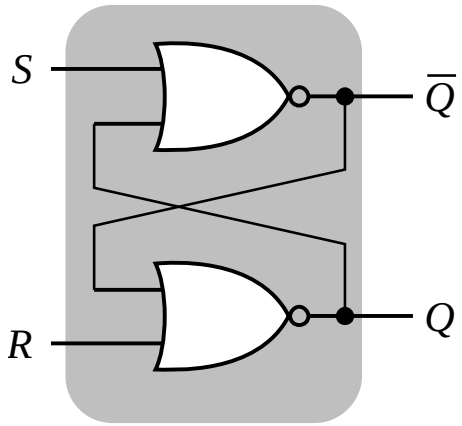
(a) Schematic diagram

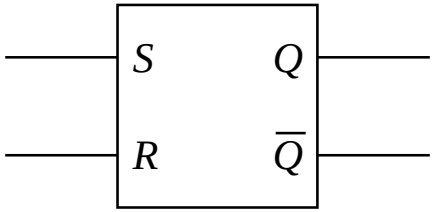


(b) Overlapping clock pairs

- Overpowering the feedback loop
- Cross-coupled pairs:

NOR-based set-reset



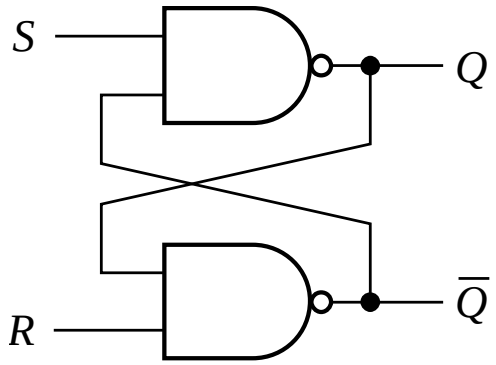


S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

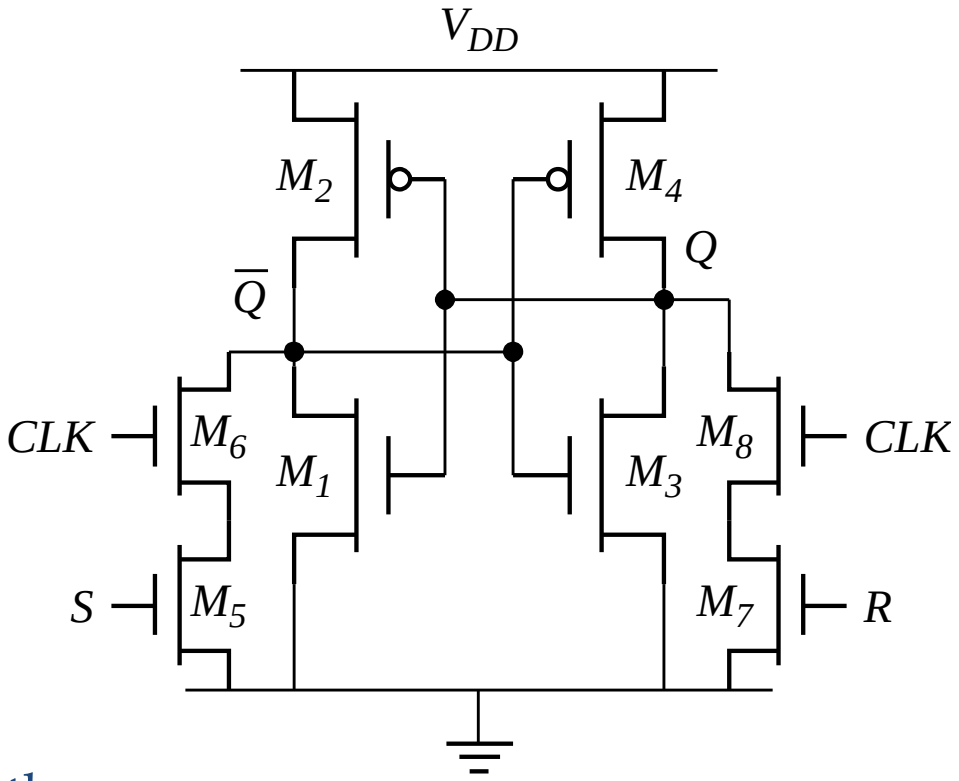
Forbidden State

- Cross-coupled NAND

Cross-coupled NANDs

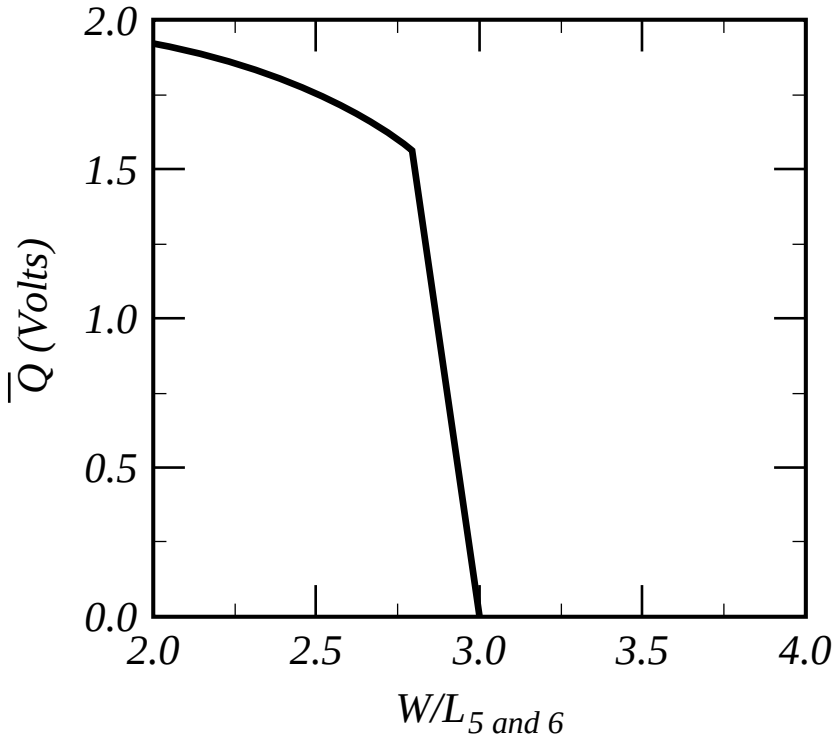


Added clock



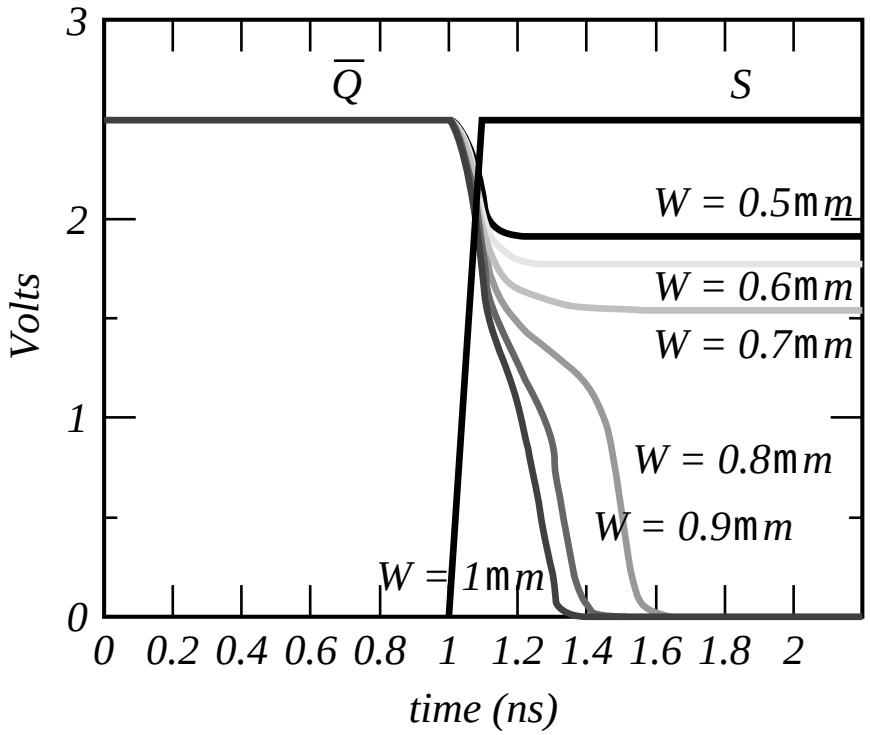
This is not used in datapaths any more, but is a basic building memory cell

- Sizing issues



(a)

Output voltage dependence on transistor width

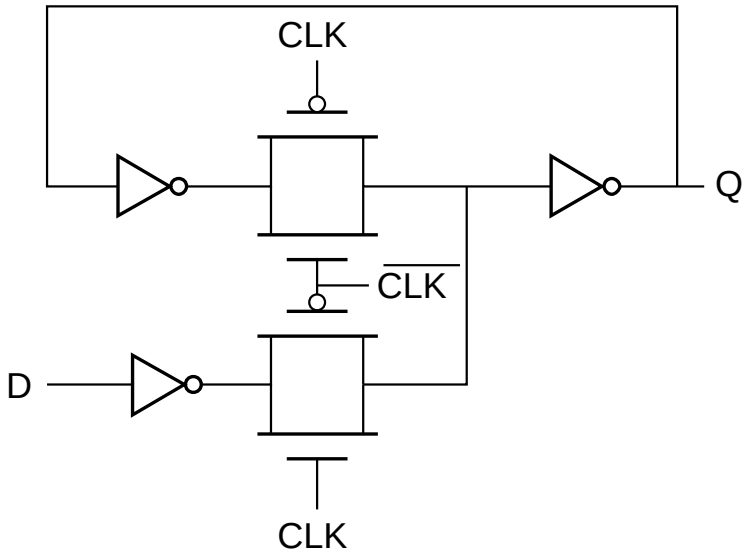


(b)

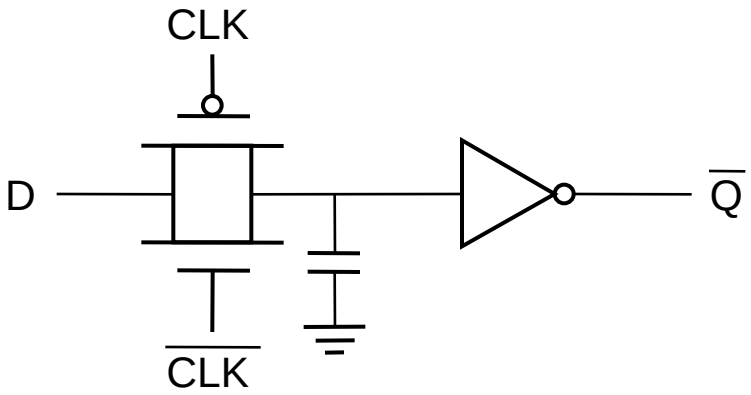
Transient response

- Storage mechanism

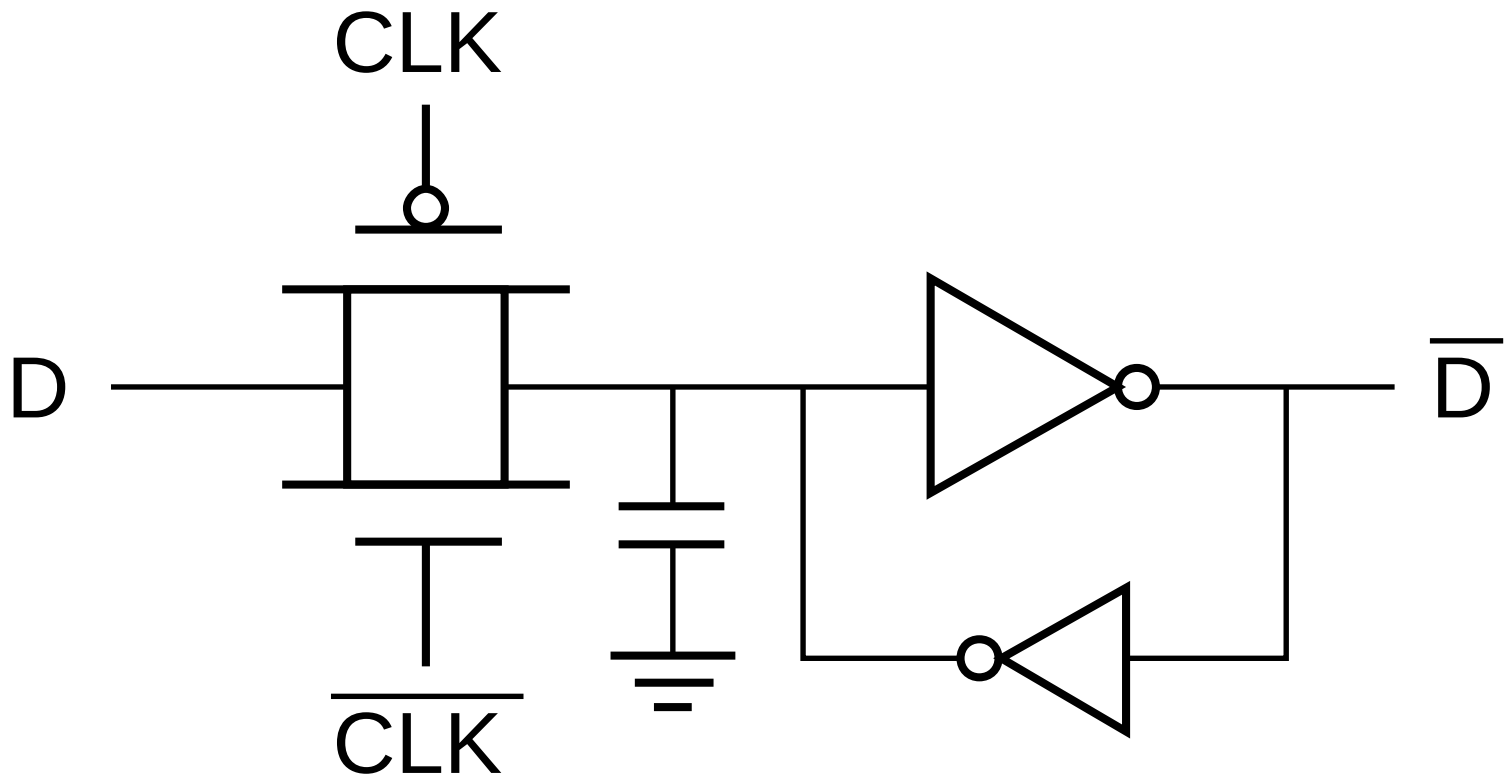
Static



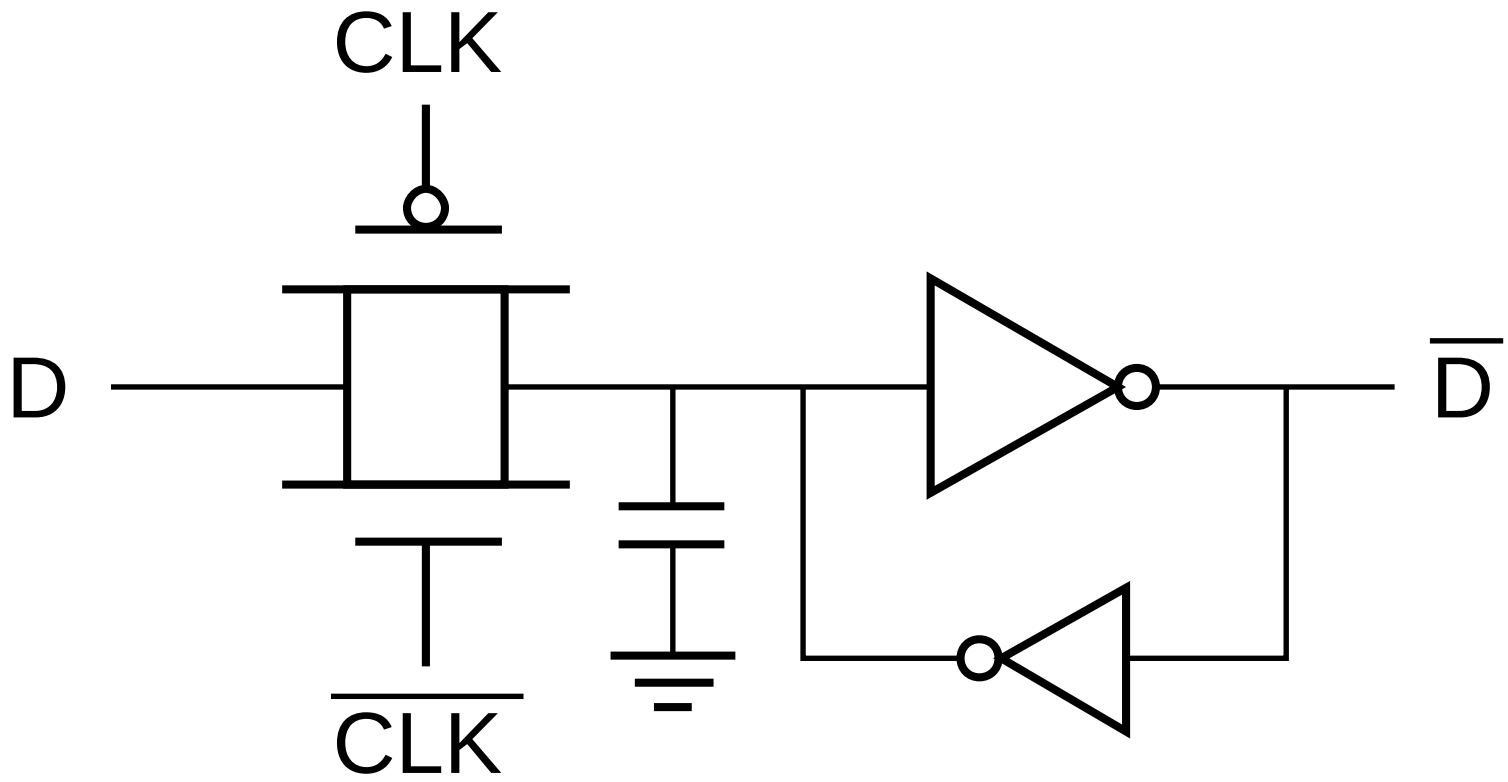
Dynamic (charge-based)



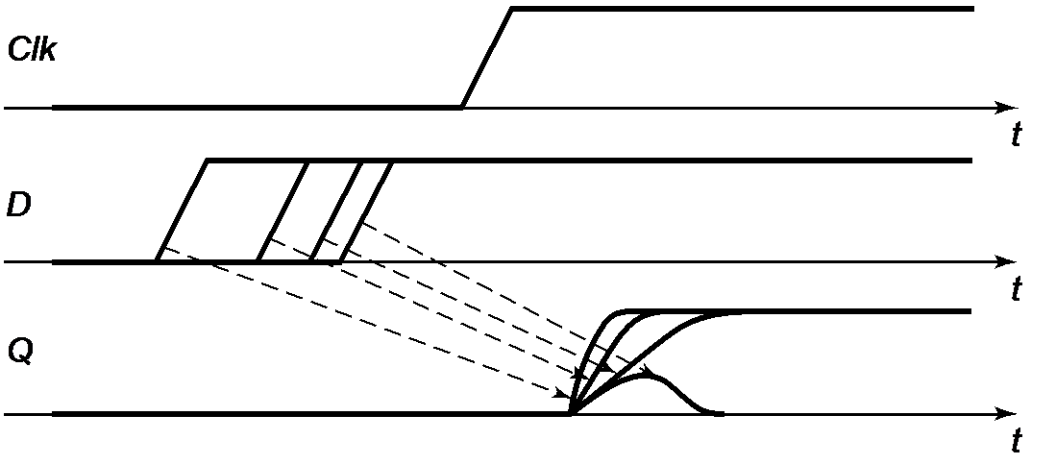
- A dynamic latch pseudo-static:



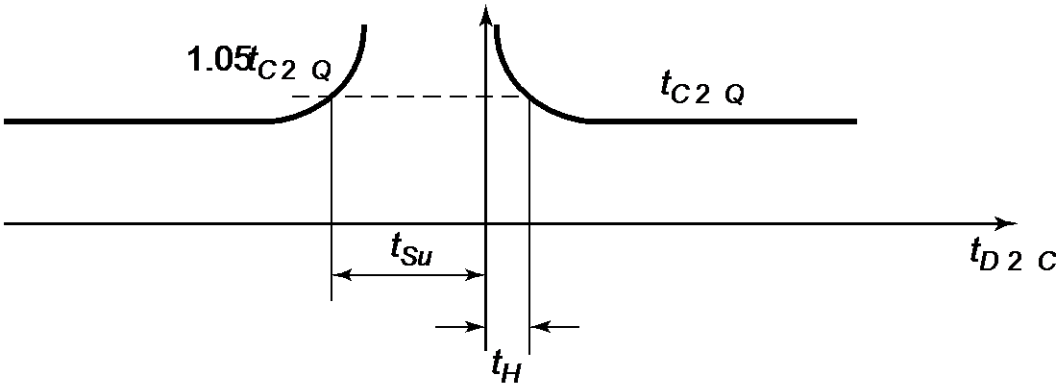
- A dynamic latch pseudo-static:



- More precise setup time:

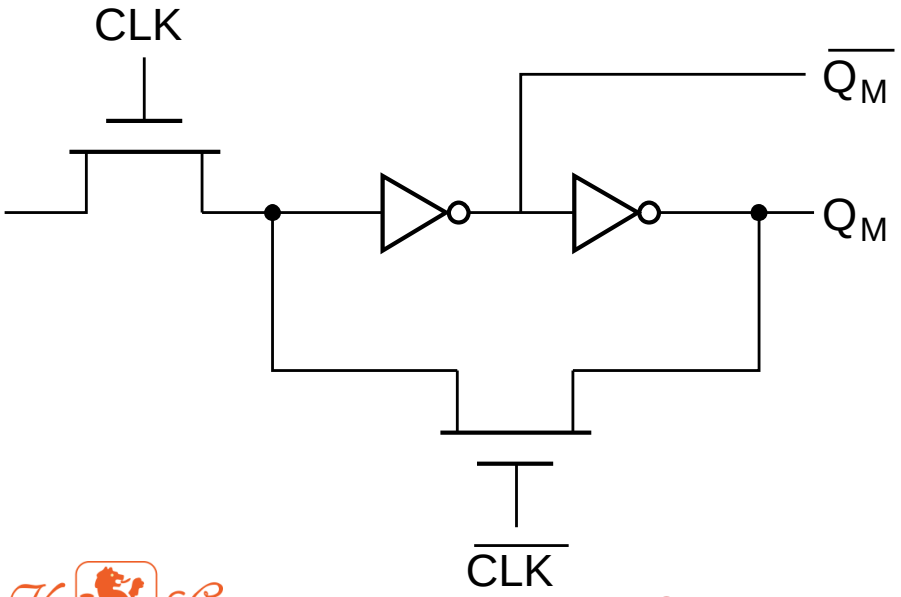


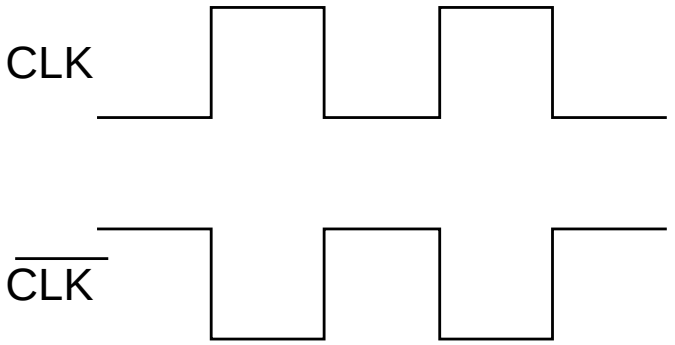
(a)



(b)

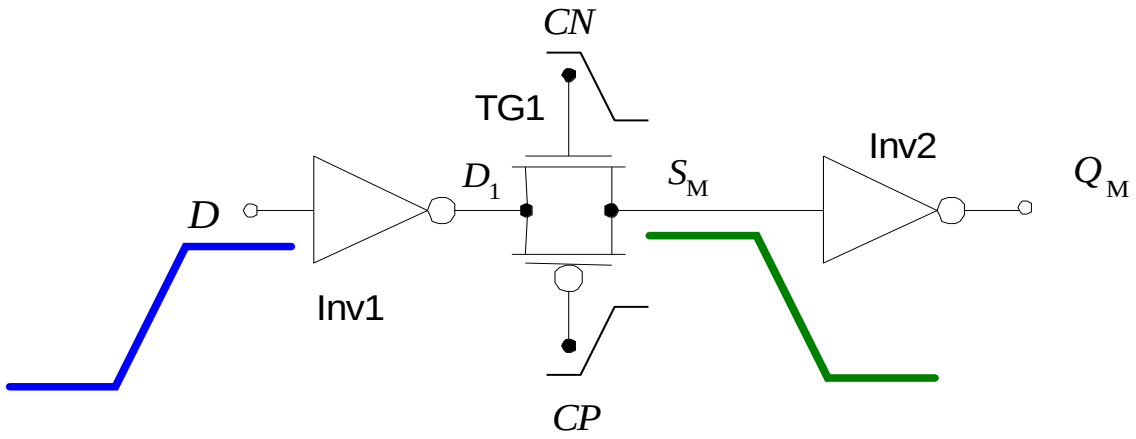
- Mux-based nMOS-only Latches
- Clk: high, the latch samples the D input.
- Clk: low enables the feedback loop, and puts the latch in the hold mode.
- Disadvantages: It pass the degraded high voltages of $V_{DD} - V_{Tn}$
- To the input of the first inverter. .

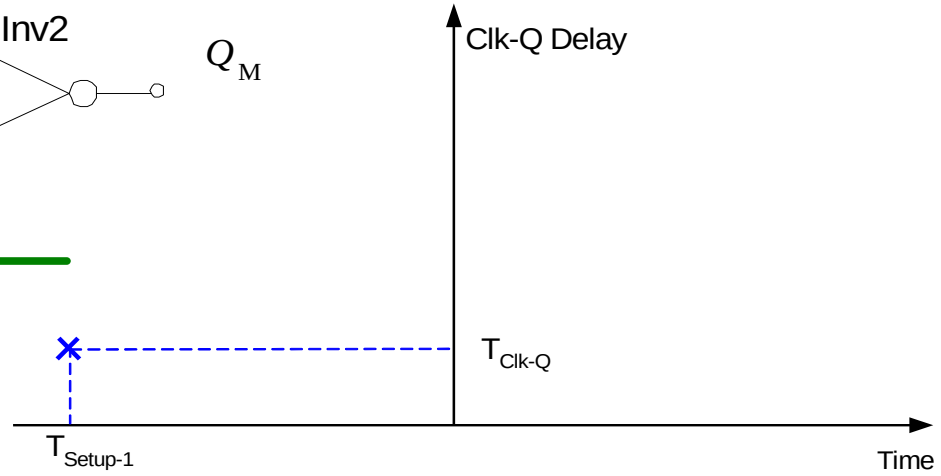


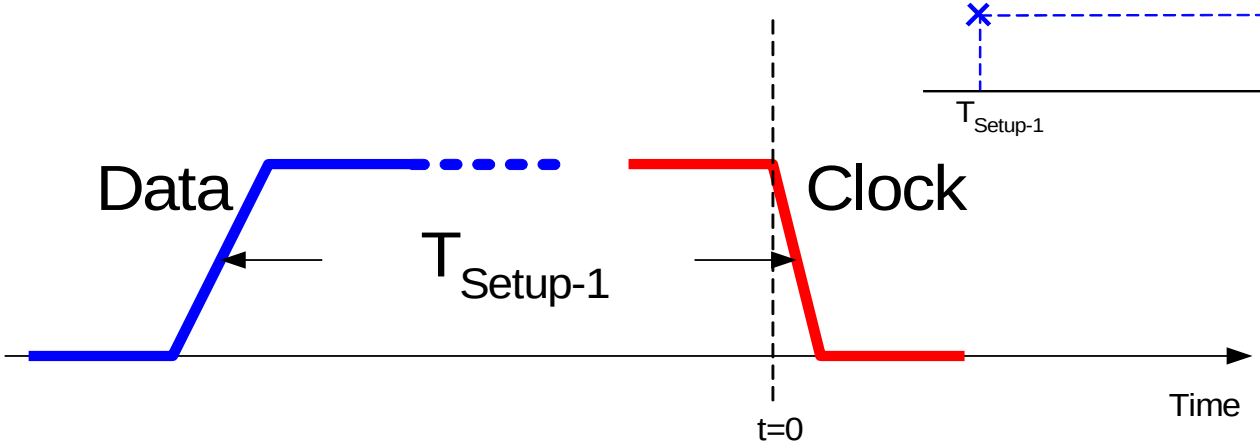


- Setup and Hold time illustrate:

Circuit before clock arrival (Setup-1 case)

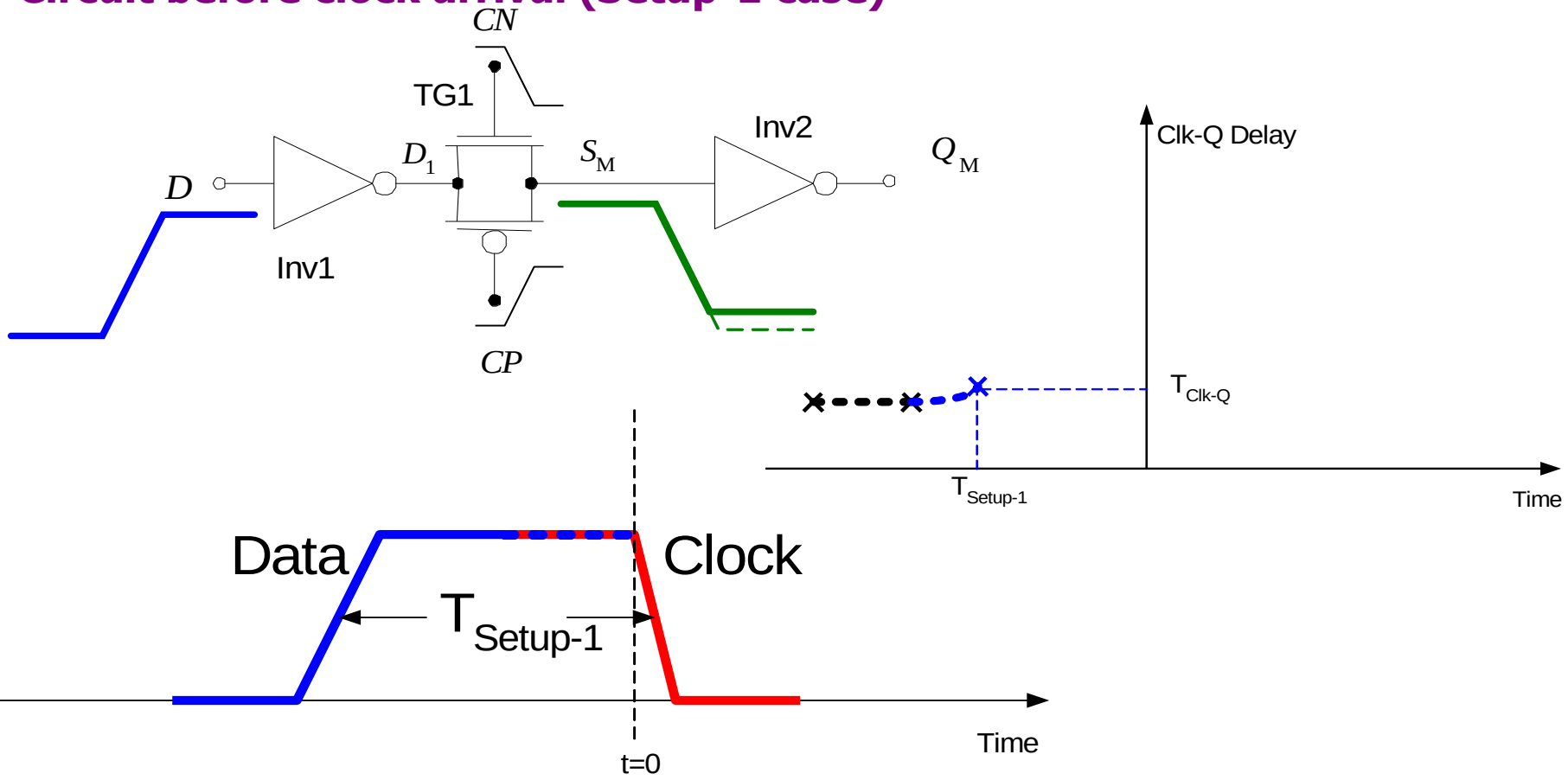






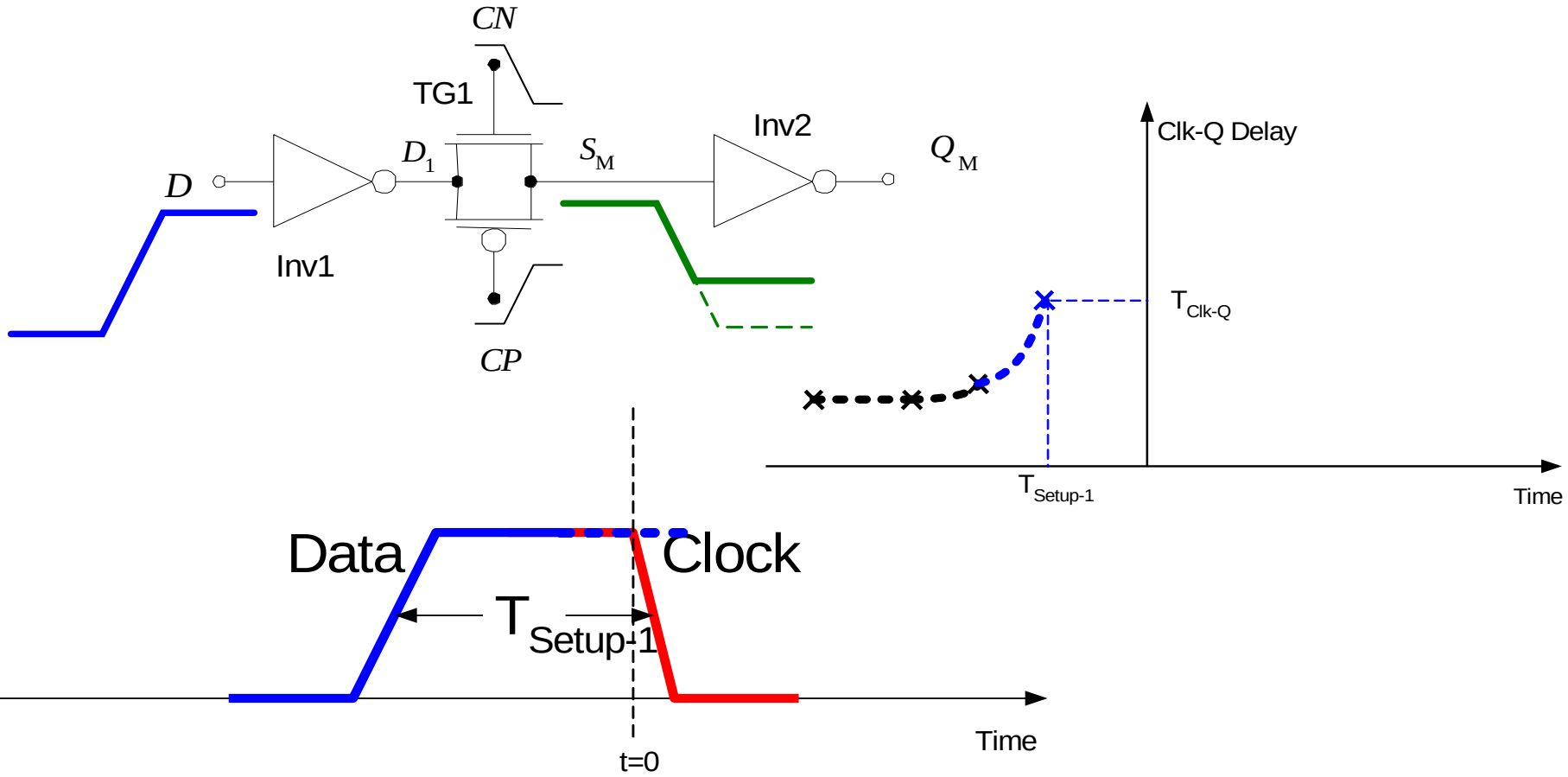
- Setup and Hold time illustrate:

Circuit before clock arrival (Setup-1 case)



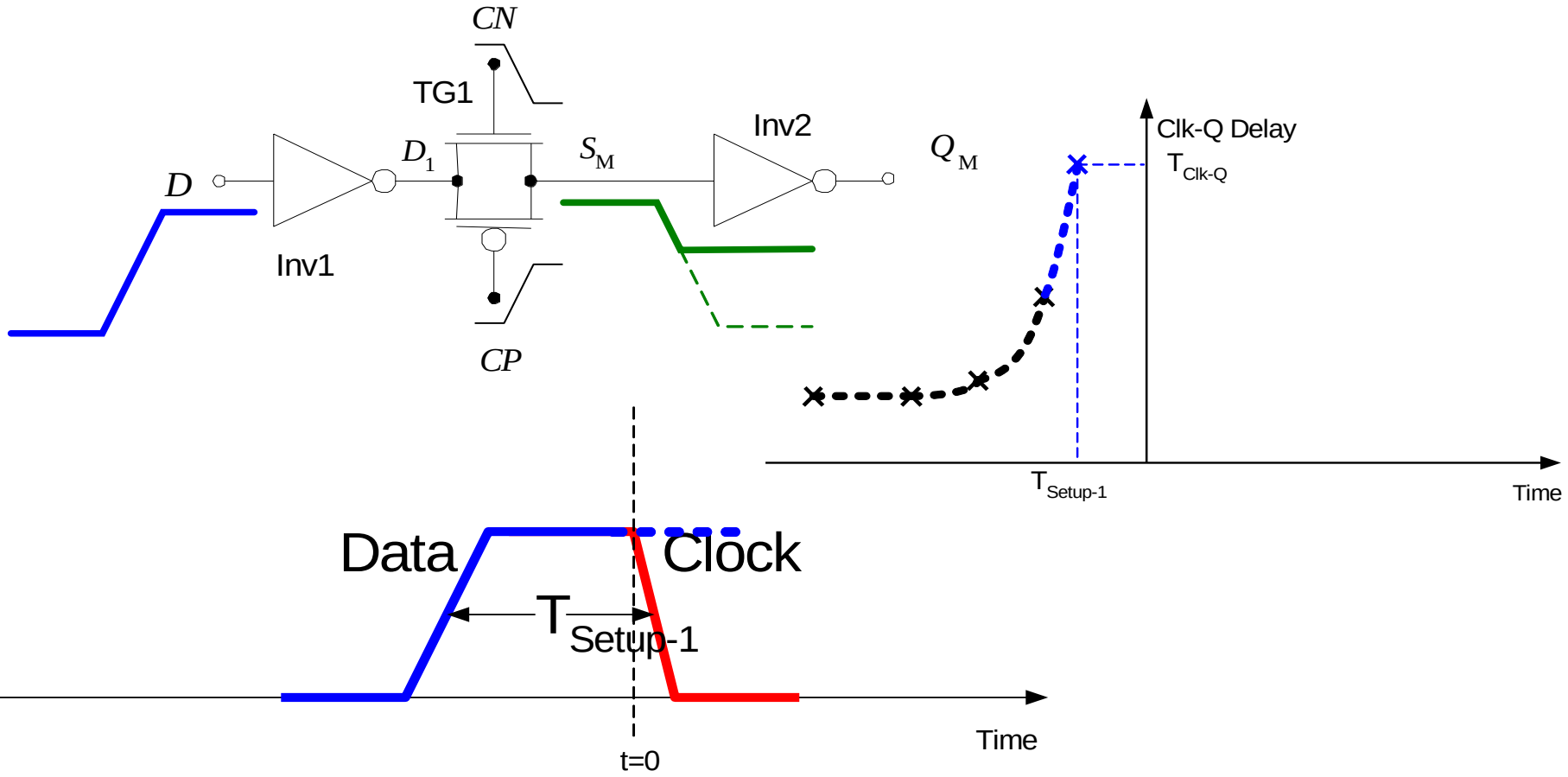
- Setup and Hold time illustrate:

Circuit before clock arrival (Setup-1 case)



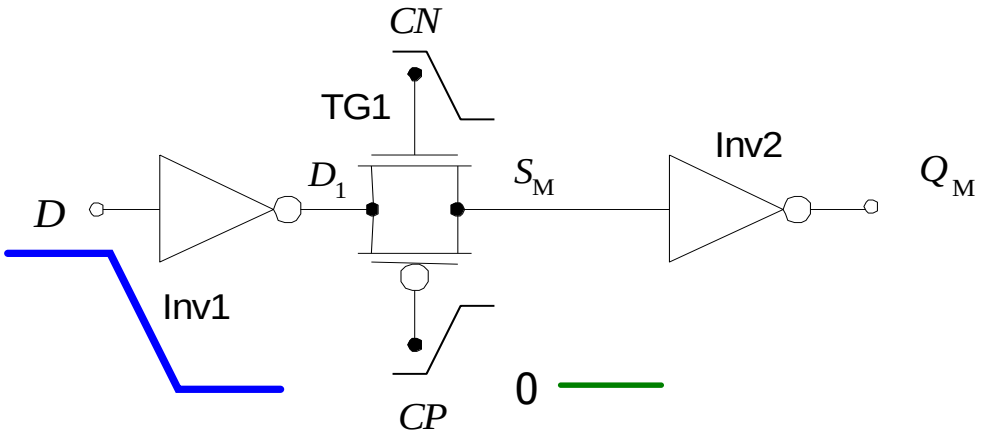
- Setup and Hold time illustrate:

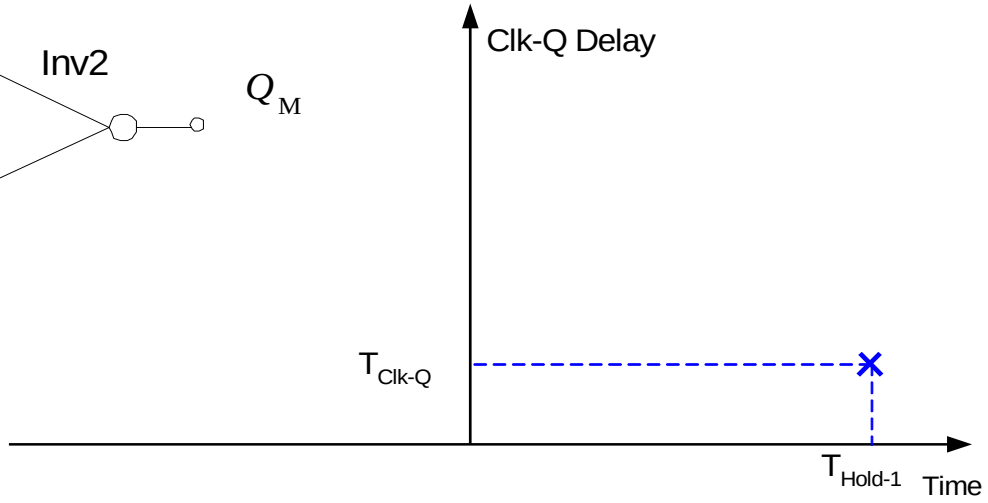
Circuit before clock arrival (Setup-1 case)

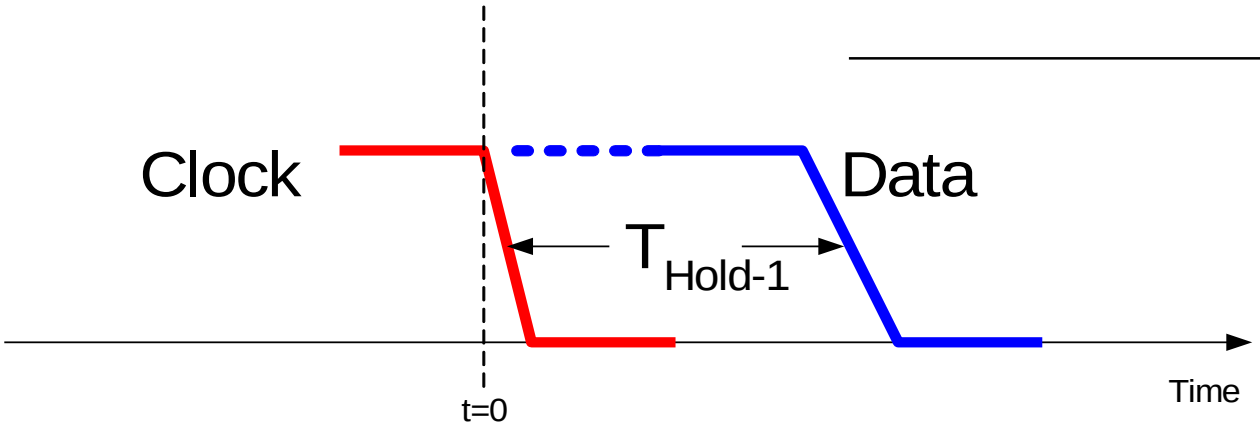


- Setup and Hold time illustrate:

Hold-1 case

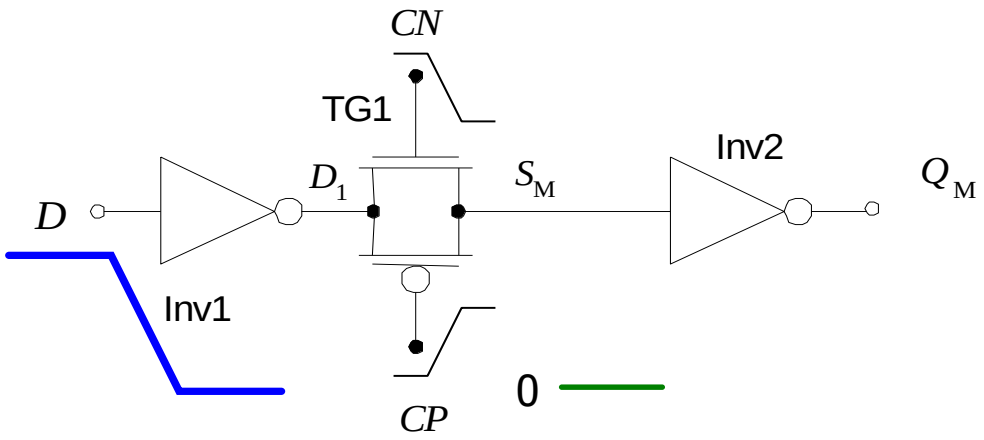


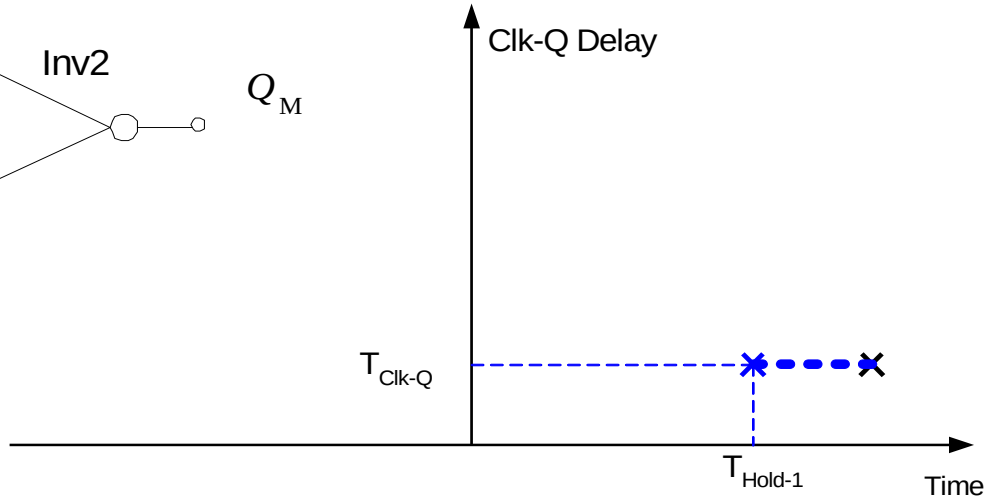


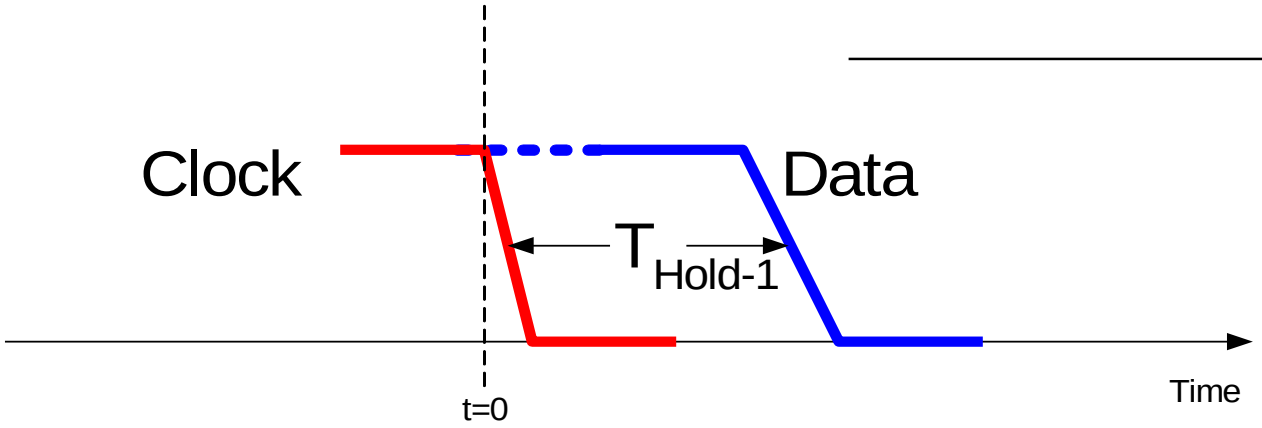


- Setup and Hold time illustrate:

Hold-1 case

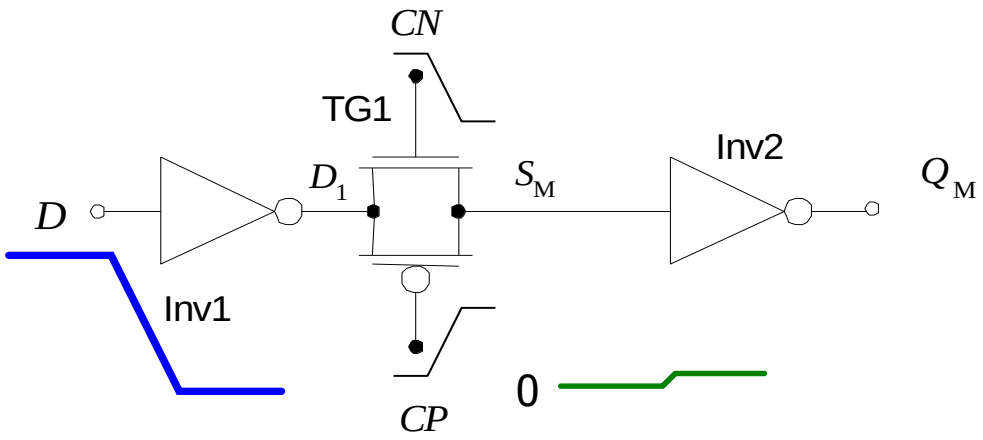


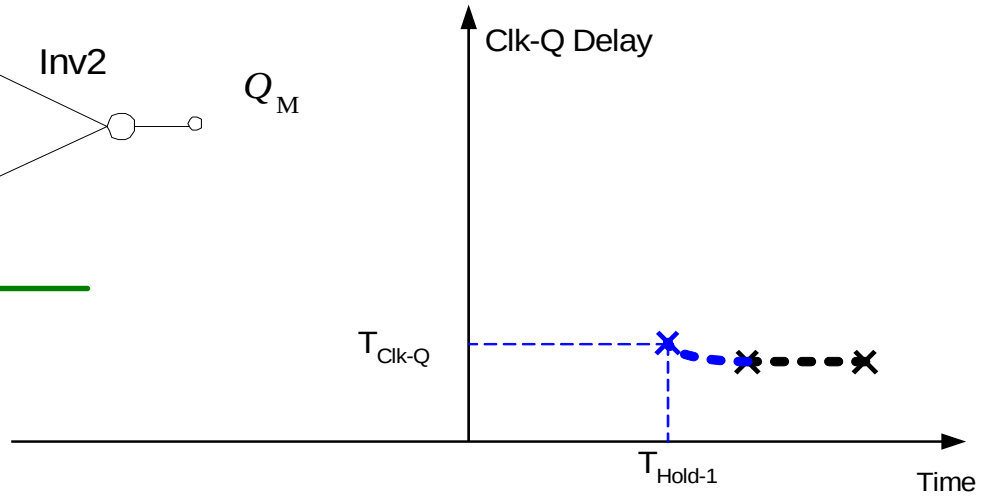


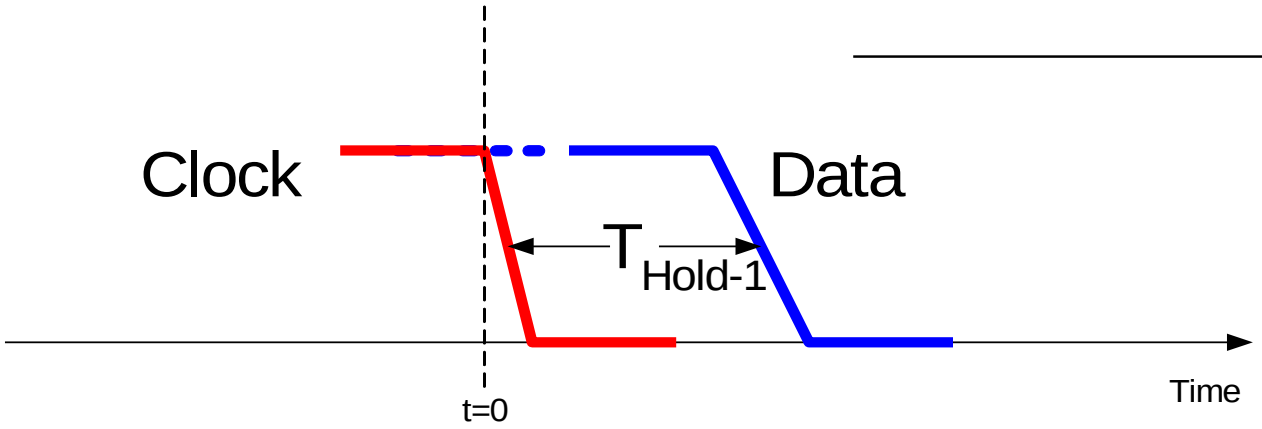


- Setup and Hold time illustrate:

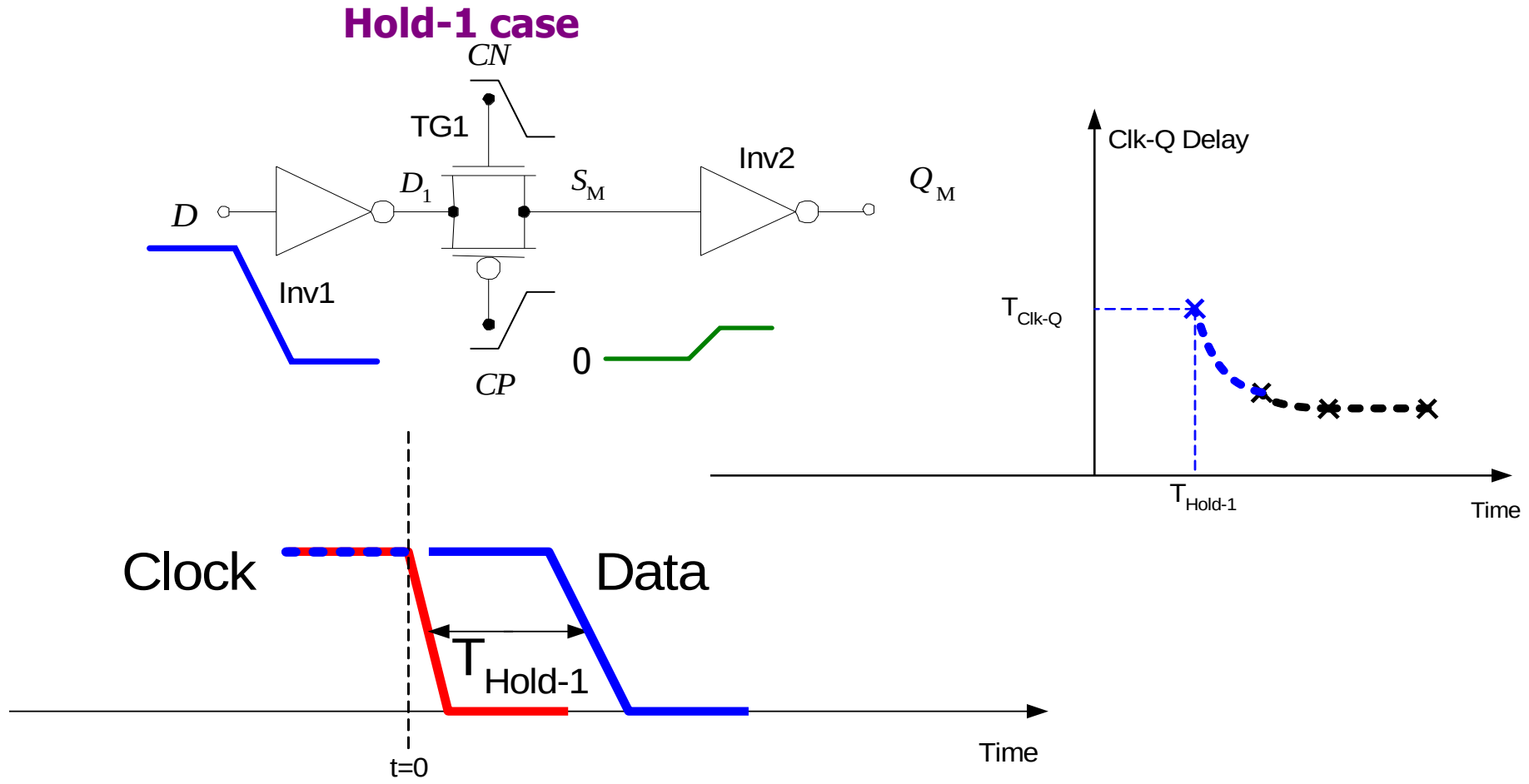
Hold-1 case





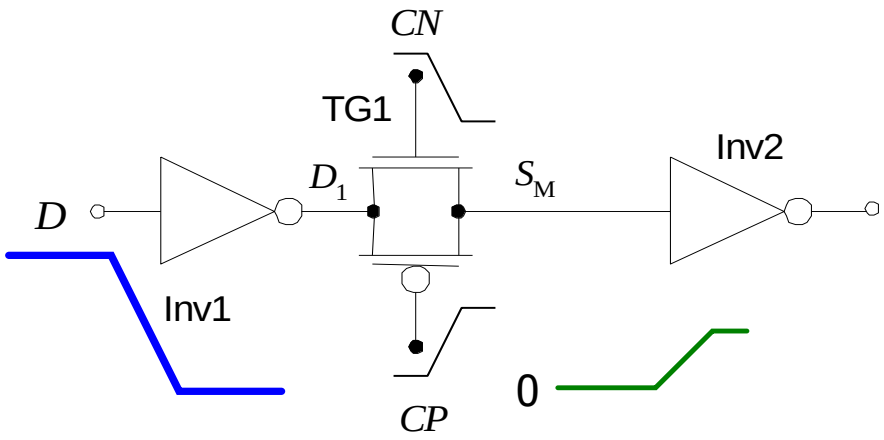


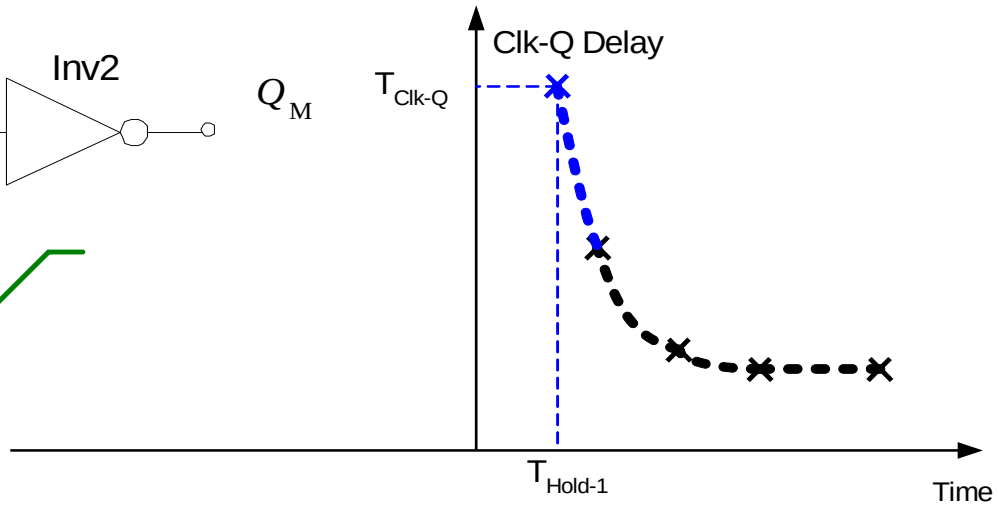
- Setup and Hold time illustrate:

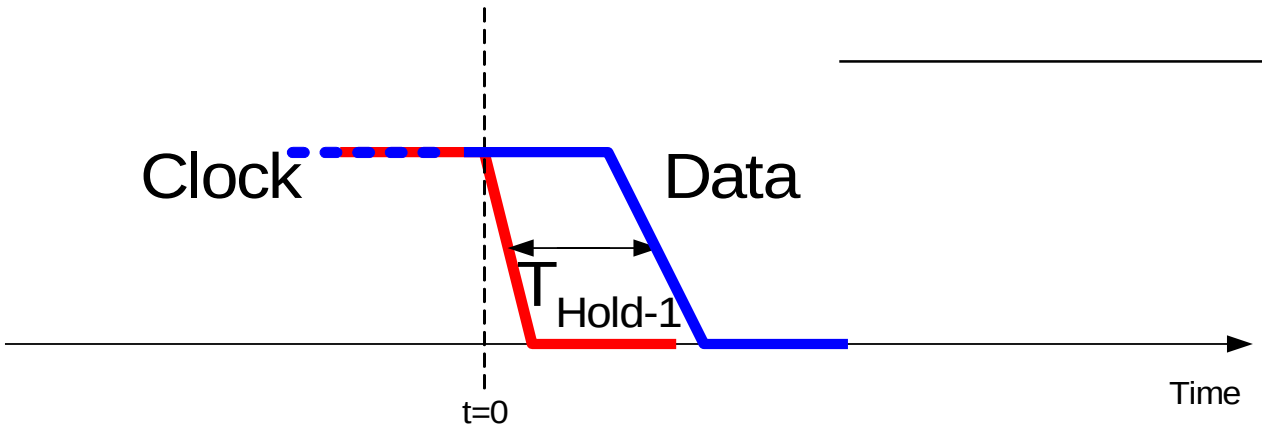


- Setup and Hold time illustrate:

Hold-1 case

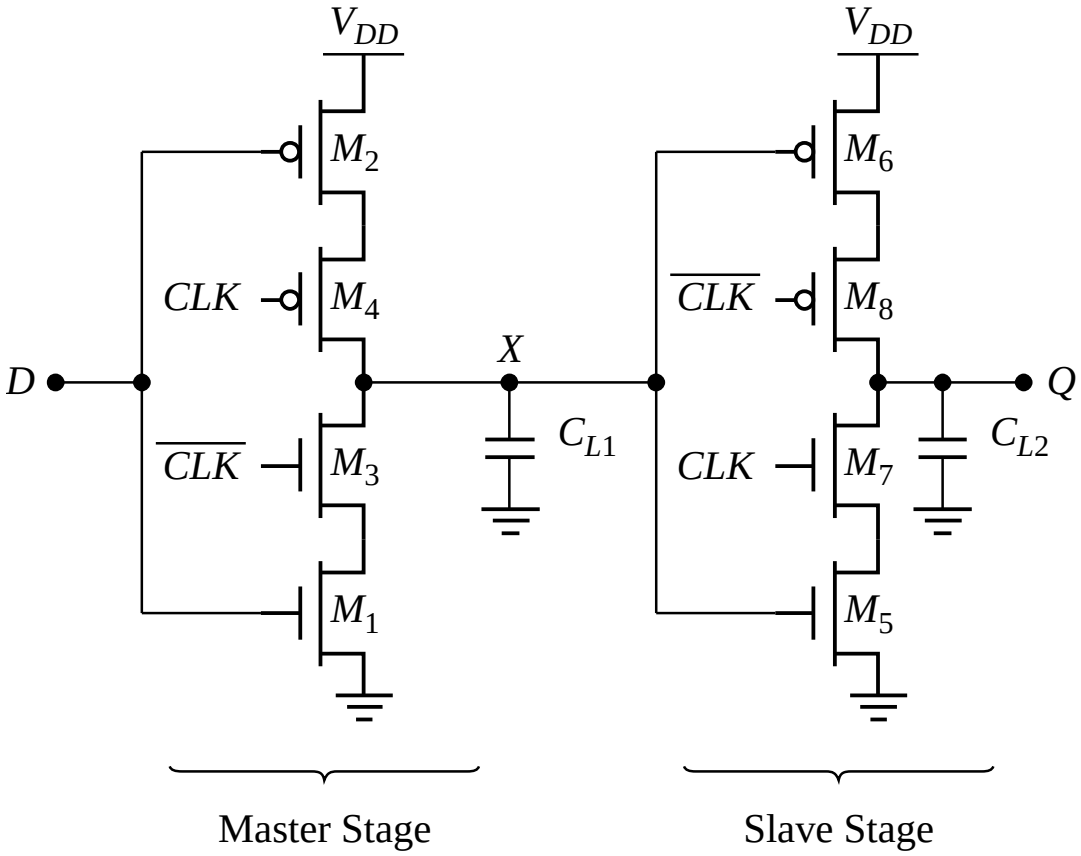






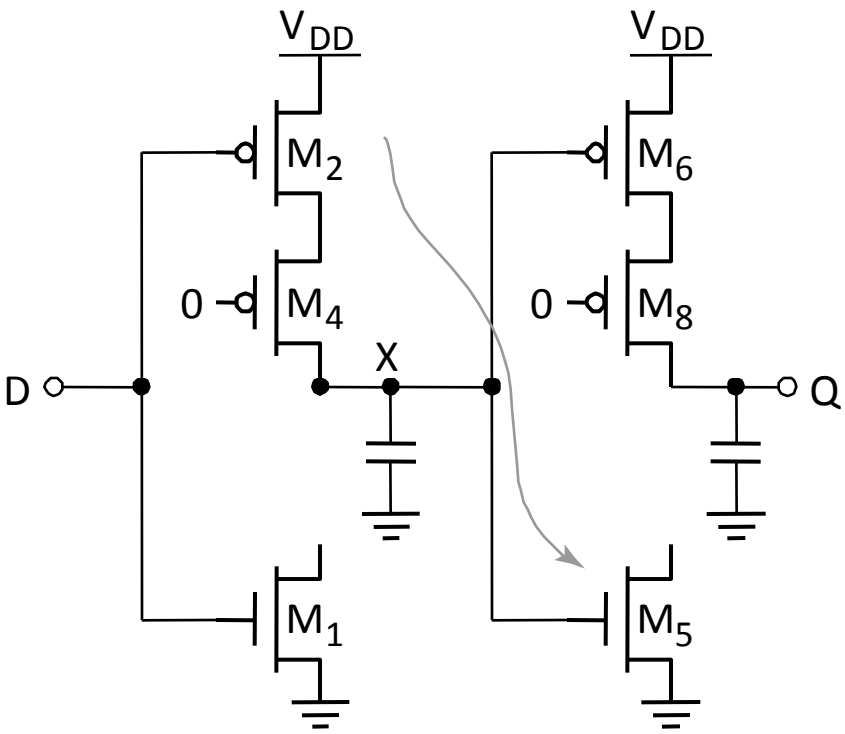
⇒

- Other latches/Registers:C2MOS

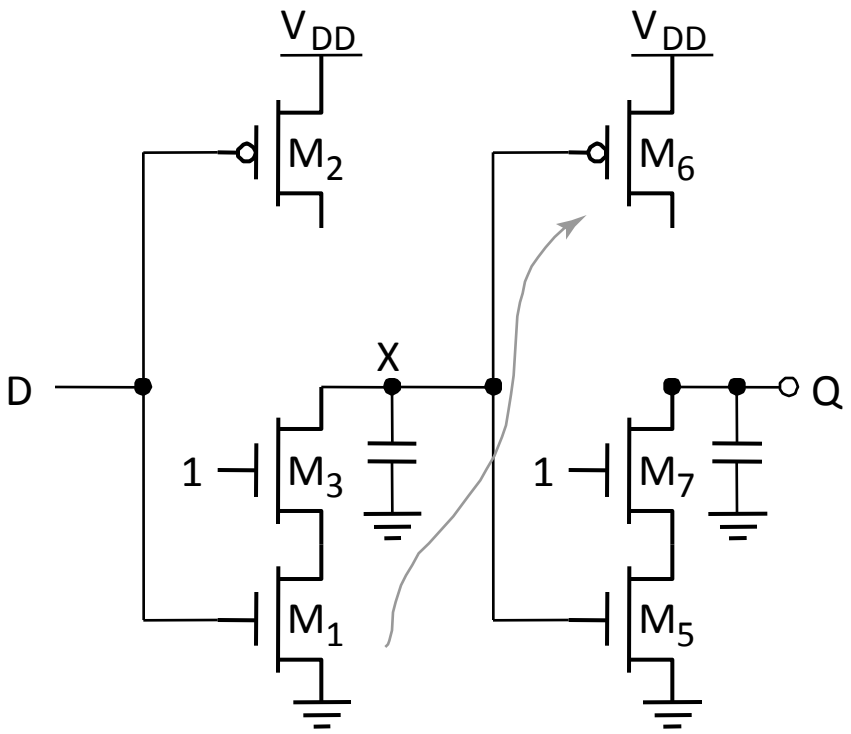


"Keepers" can be added to make circuit pseudo-static

- Insensitive to Clk-overlap:

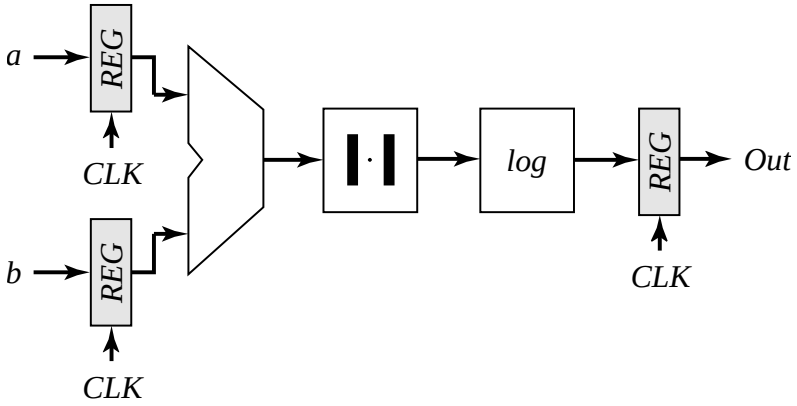


(a) (0-0) overlap

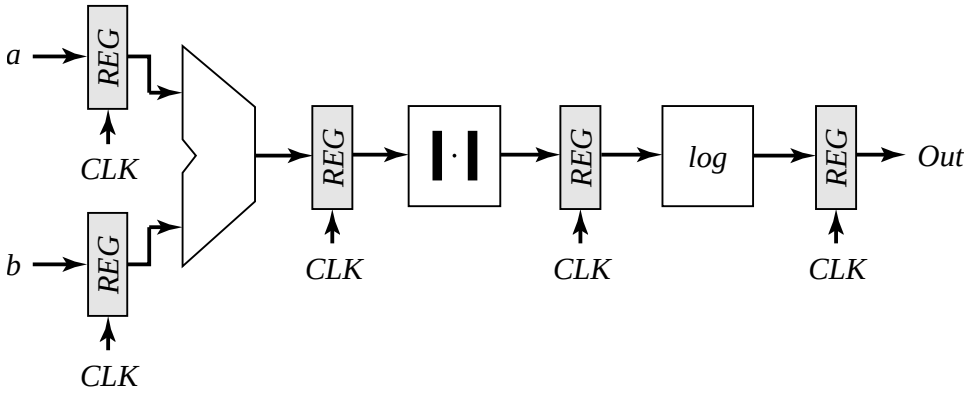


(b) (1-1) overlap

- Pipelining:



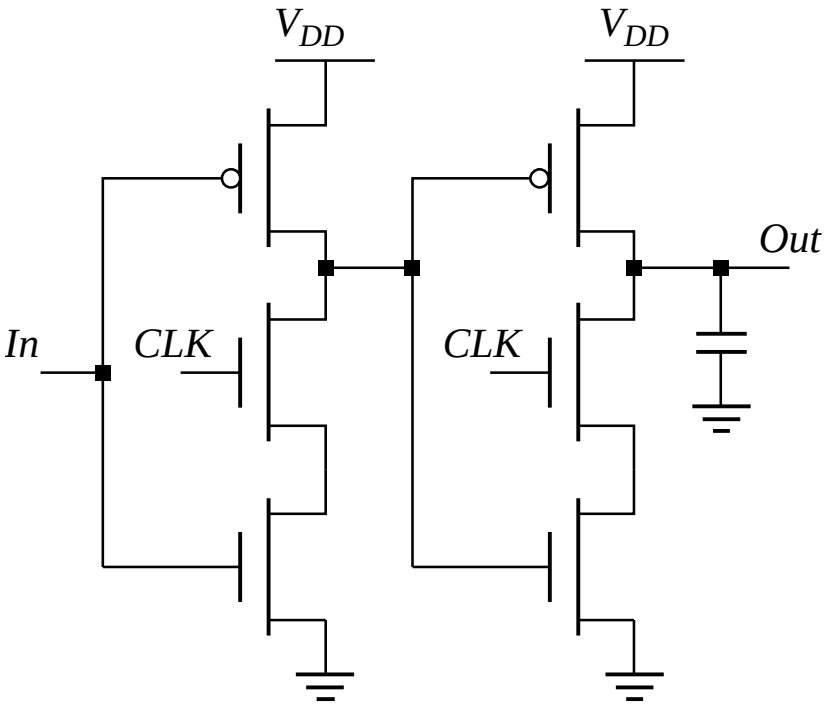
Reference



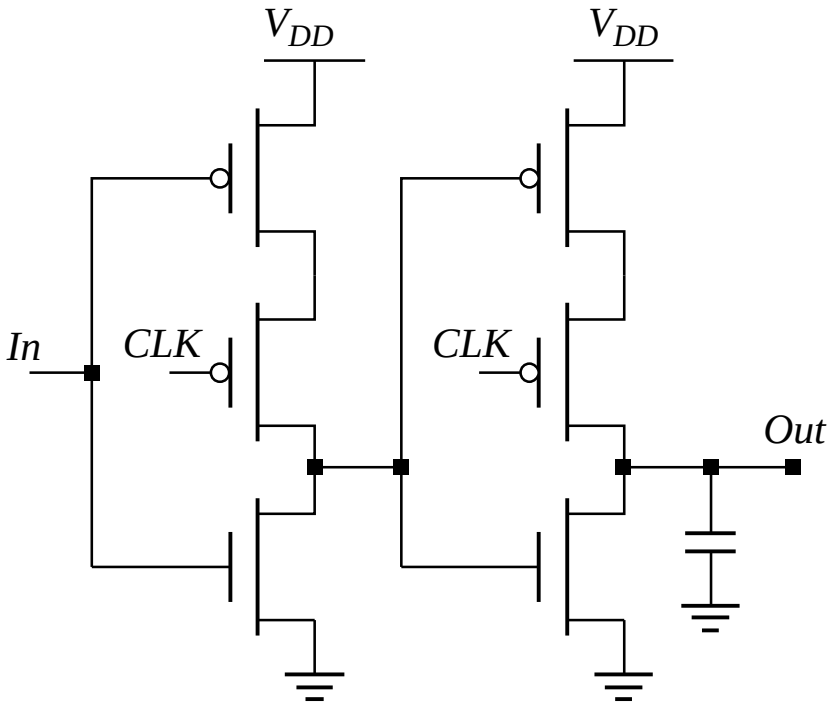
Pipelined

Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

- Other latches/registers: TSPC

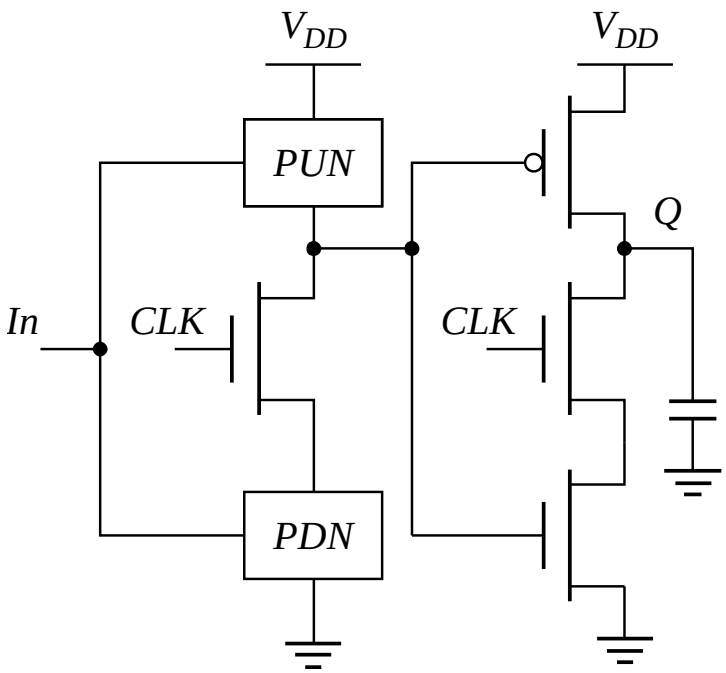


Positive latch
(transparent when CLK= 1)

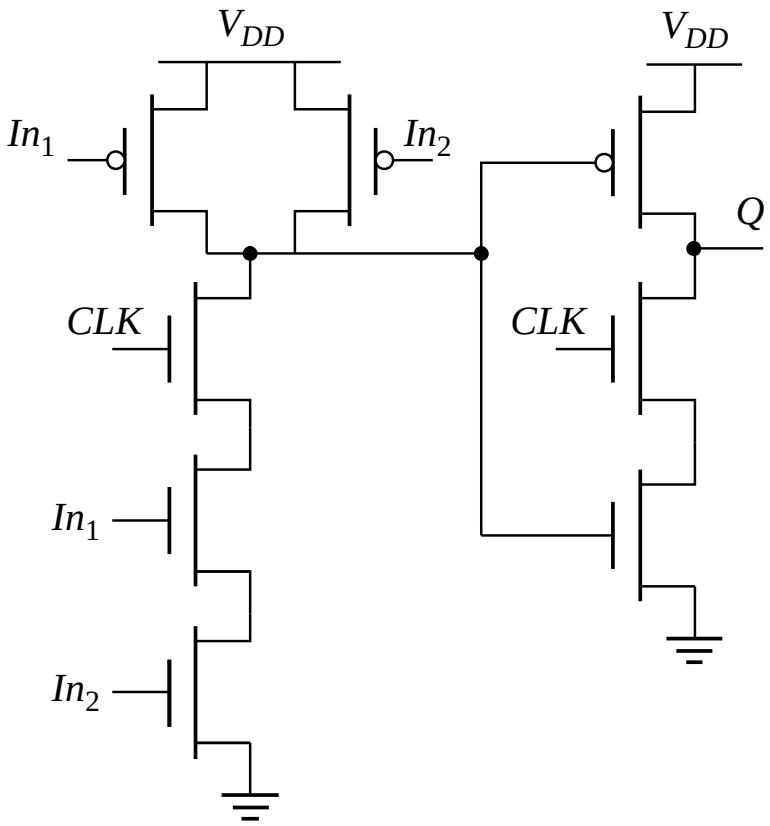


Negative latch
(transparent when CLK= 0)

- Including logic in TSPC

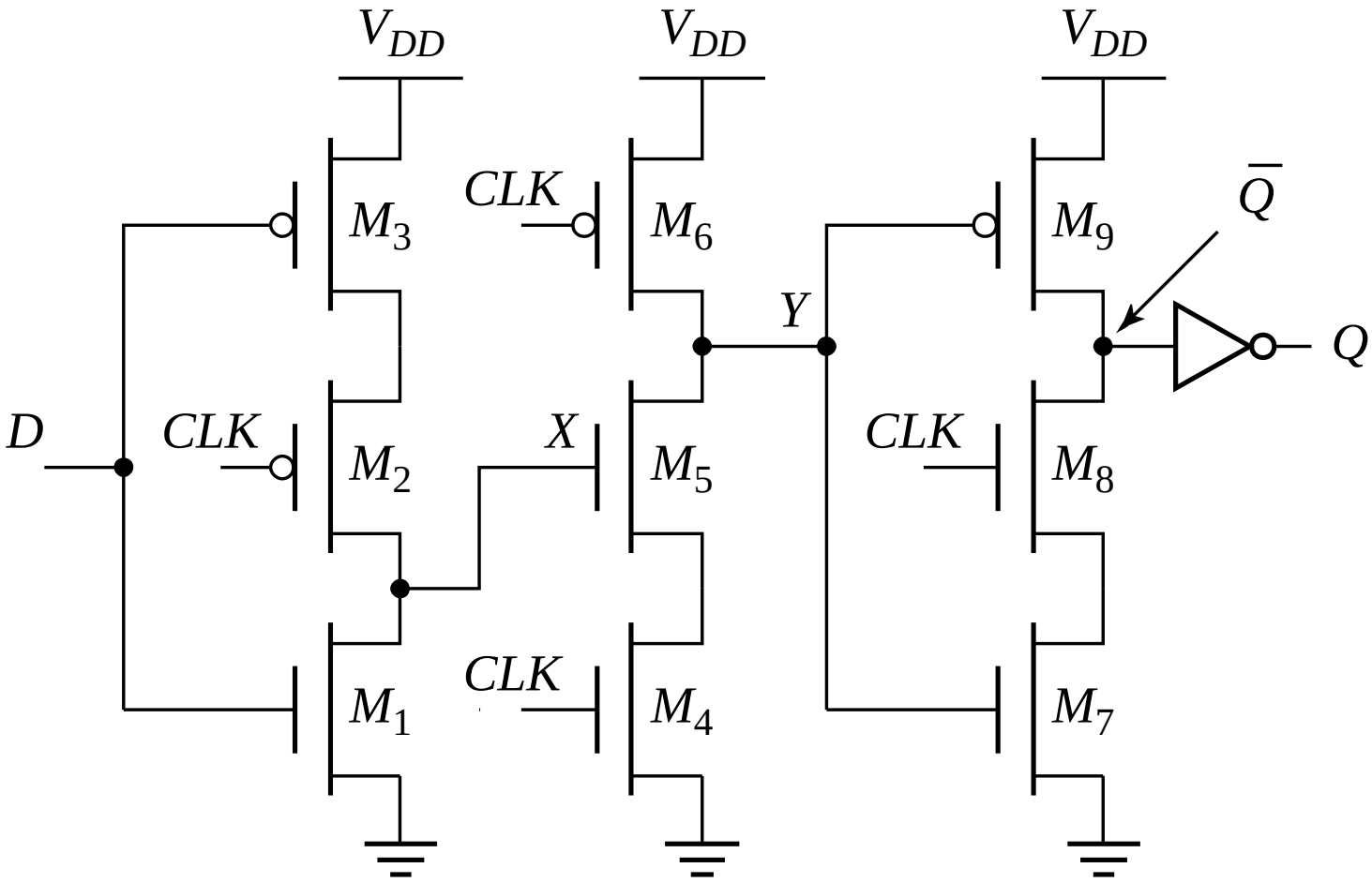


Example: logic inside the latch



AND latch

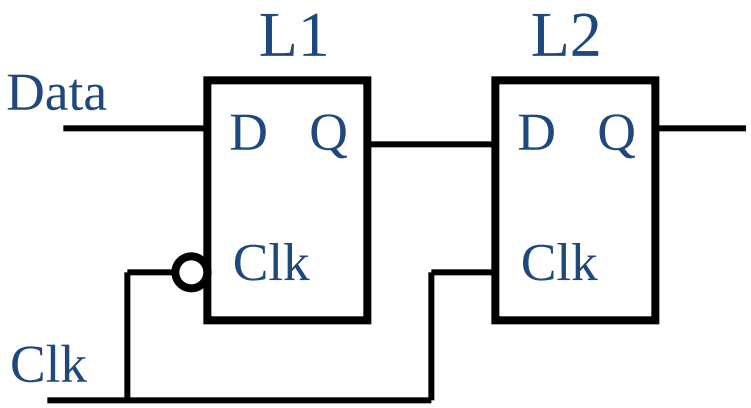
- TSPC register



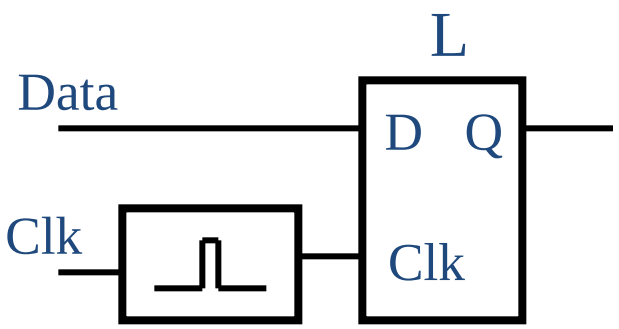
- Pulse-triggered latches, An alternative approach

Ways to design an edge-triggered sequential cell:

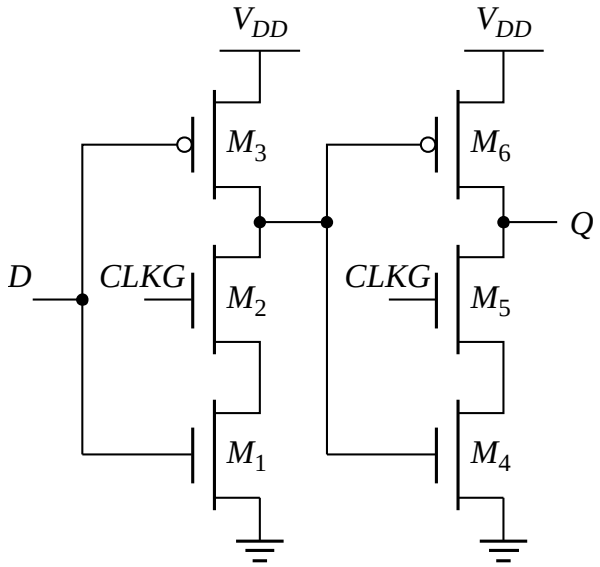
Master-Slave Latches



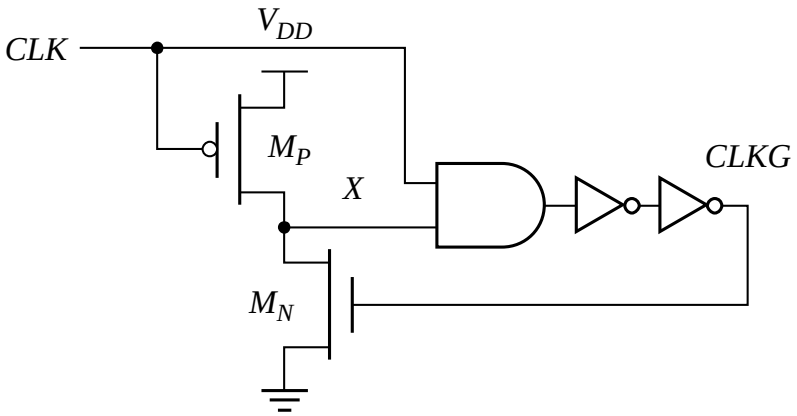
Pulse-Triggered Latch



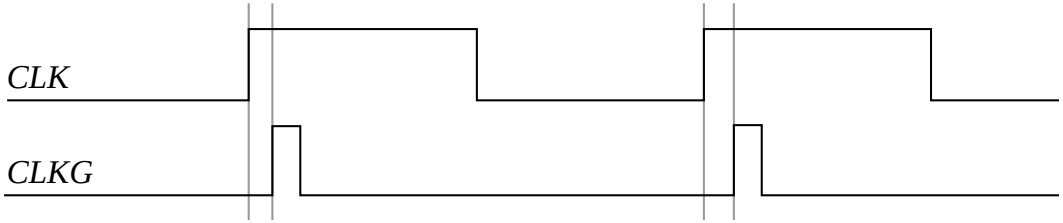
- Pulse latches



(a) register



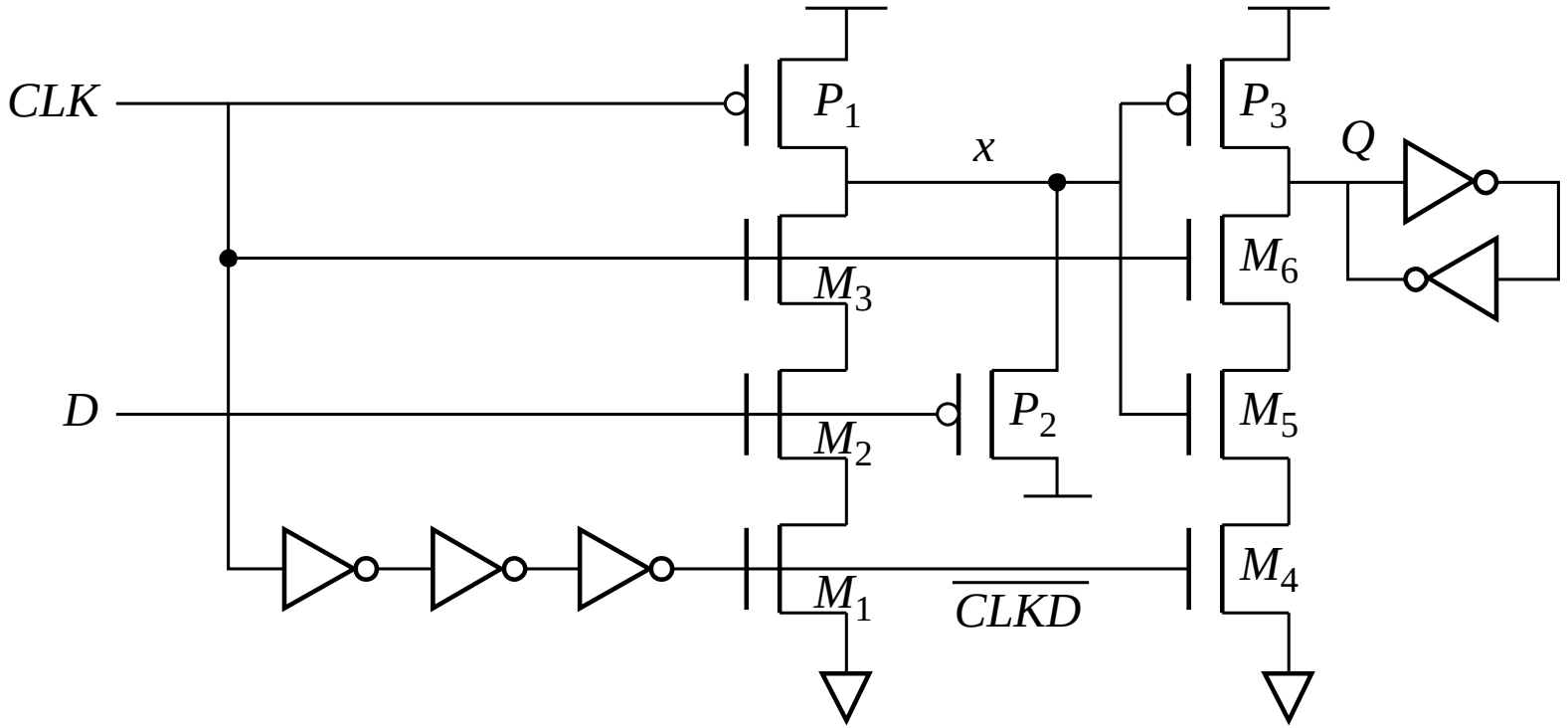
(b) glitch generation



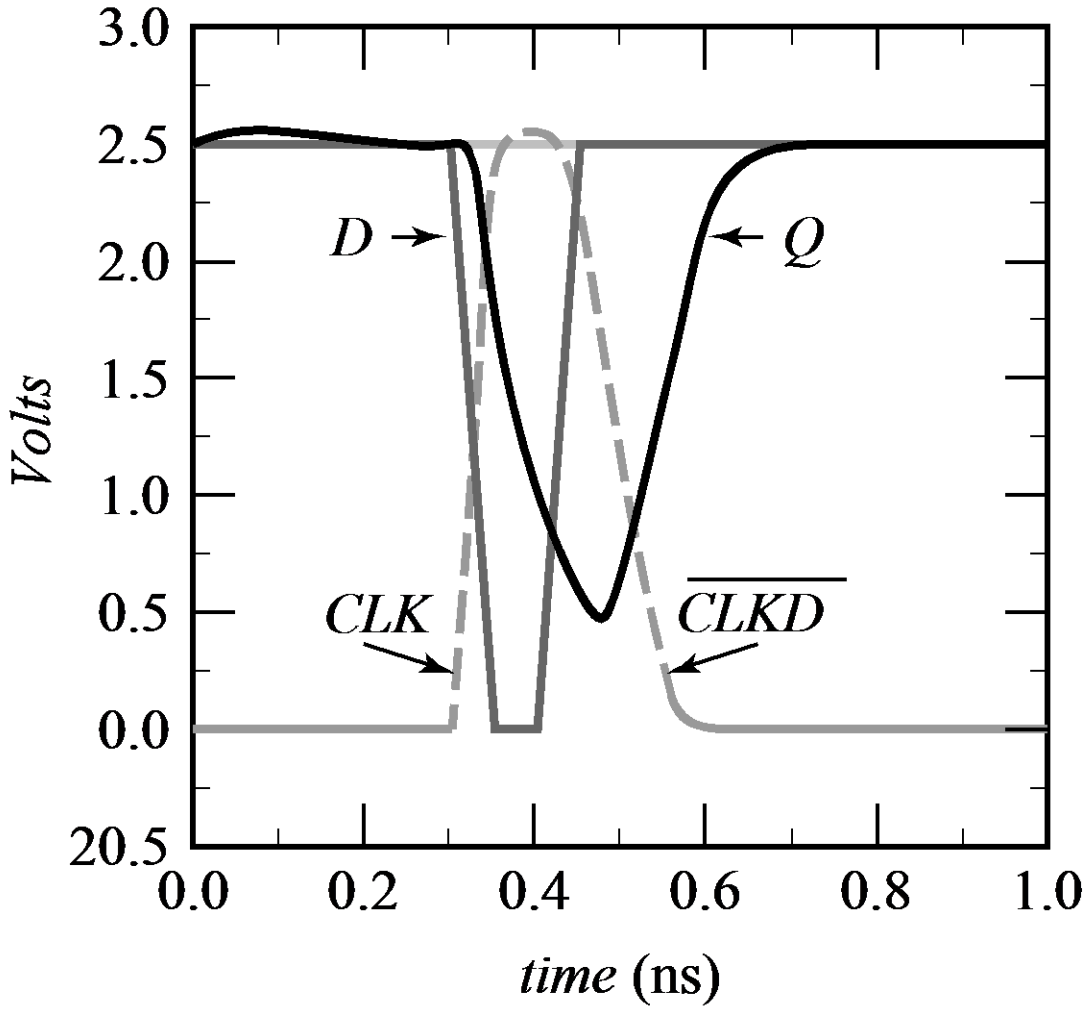
(c) glitch clock

- Pulse latches

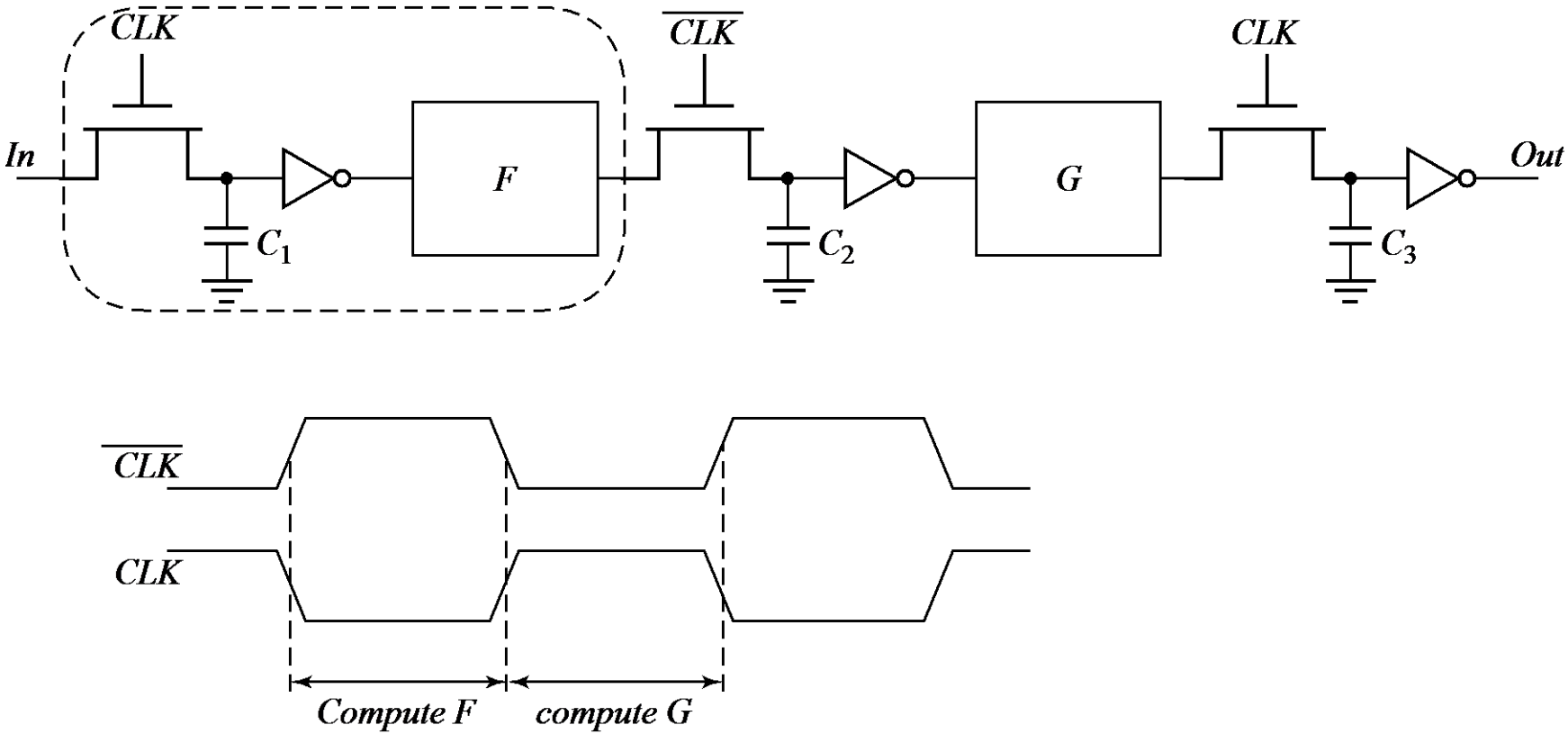
Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7 :



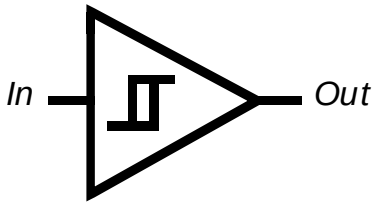
- Hybrid Latch-FF timing

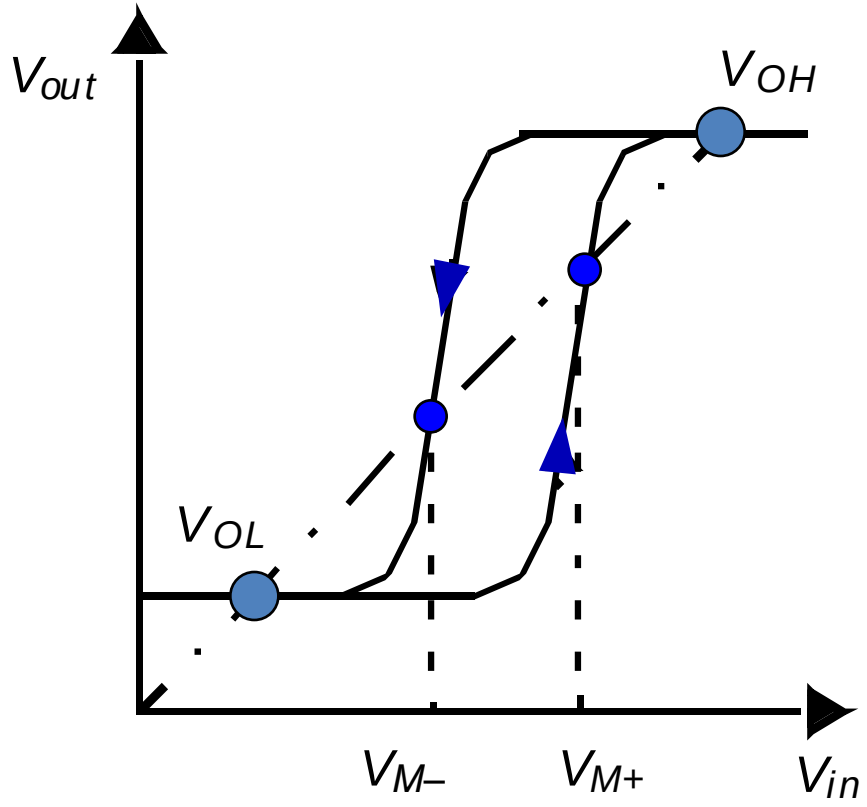


- Latch-based pipeline



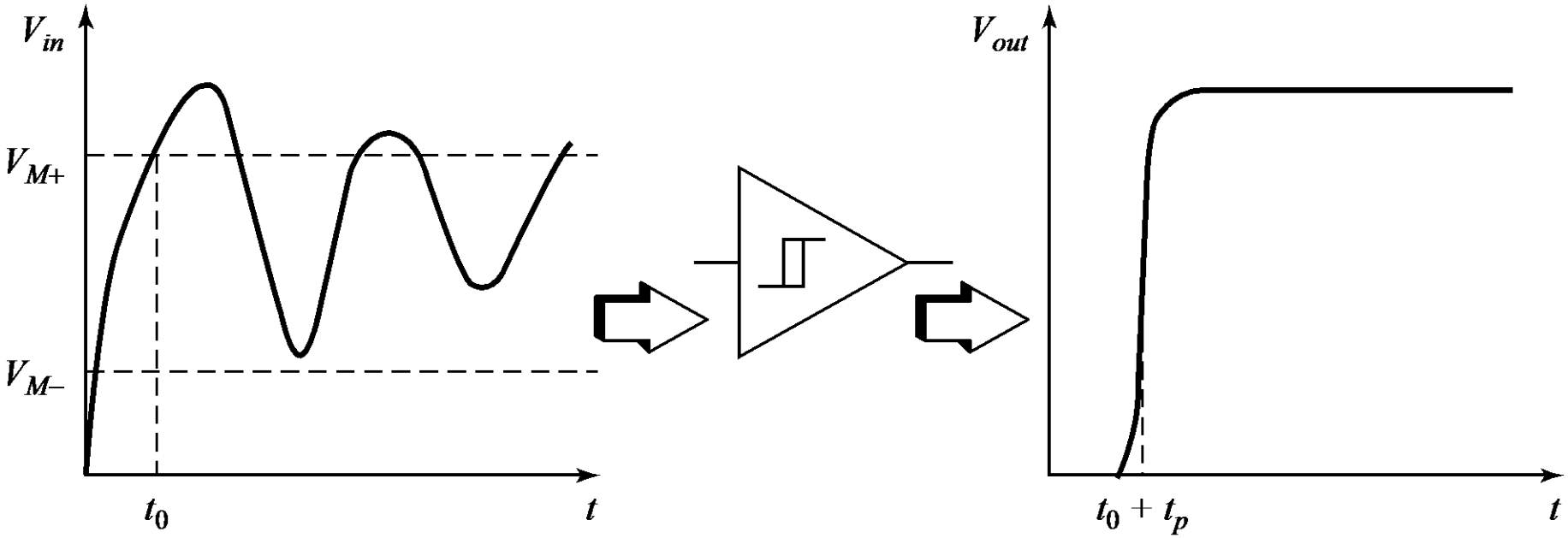
- Non-bistable sequential circuits Scmitt trigger



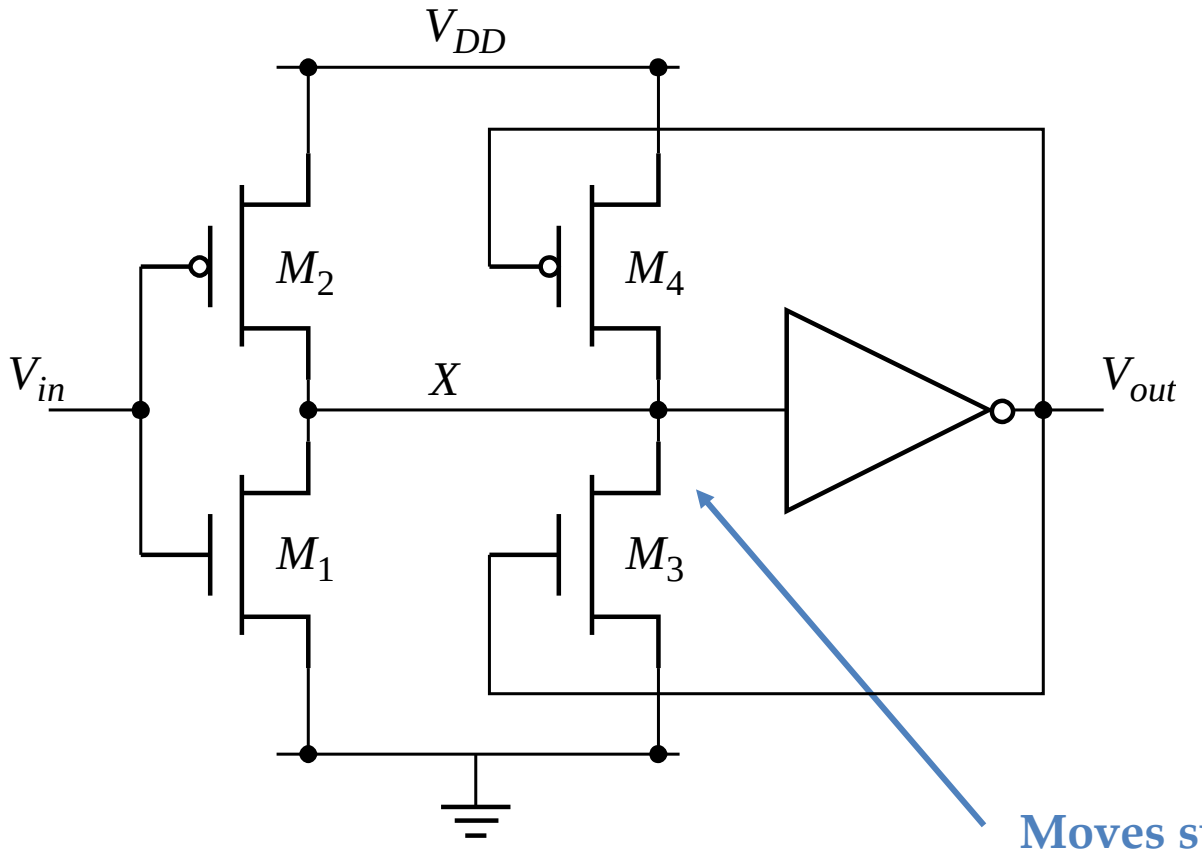


- **VTC with hysteresis**
- **Restores signal slopes**

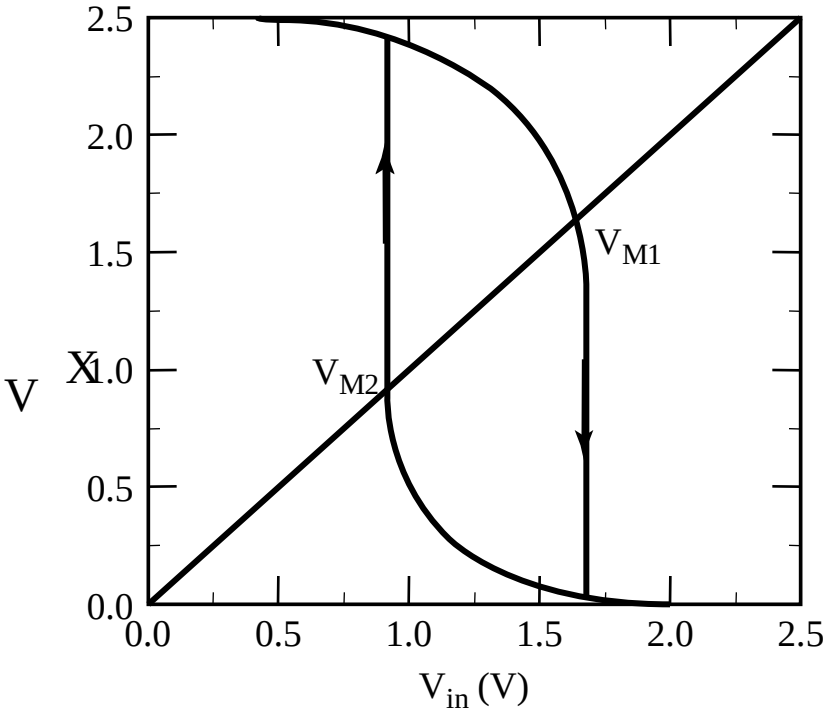
- Noise suppression using Schmittt trigger



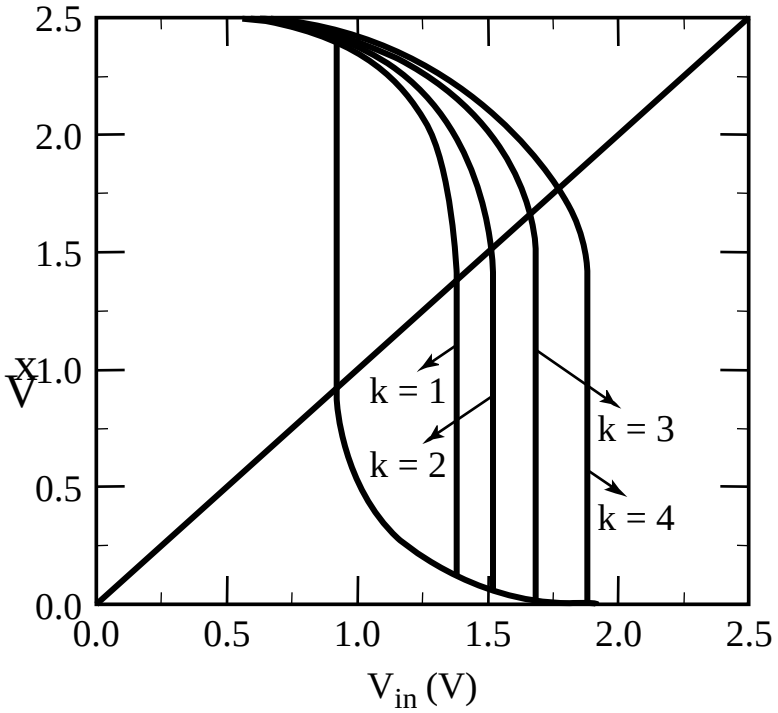
- CMOS Schmitt trigger



- Schmitt trigger simulated VTC



Voltage-transfer characteristics with hysteresis.



The effect of varying the ratio of the PMOS device M_4. The width is k* 0.5$_m$ m.