EE 223 Homework 5

Two-Stage OPAMP with RC Compensation

Enrique Hernandez

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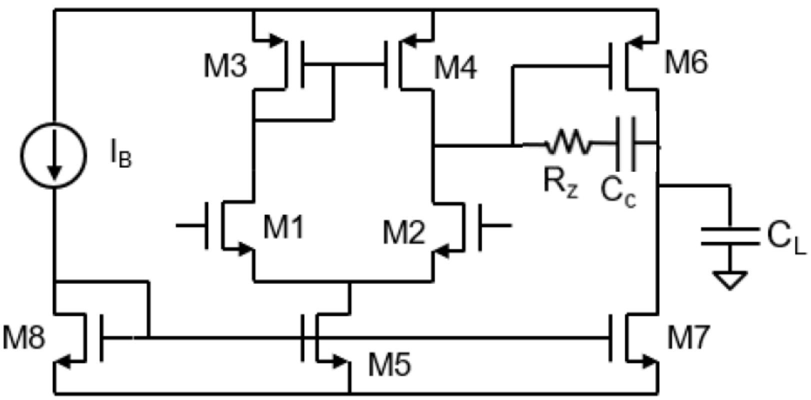
1. Design the circuit to meet the key spec parameters.
    a. Hand Calculations

Parameters given:



- AV = 60 dB
- GBW = 100 MHz
- PM > 60˚
- GM > 12 dB
- SR > 60 V/us
- Power < 2.5mV
- C_L = 5 pF
- KP_n = 300 uA/V^2
- KP_p = 160 uA/V^2
- Vdsat = 0.2 V
- I_B = 100 uA

$$I_1 = \frac{g_{m_1} V_{dsat}}{2} \qquad f_u = \frac{1}{2\pi} \cdot \frac{g_{m_1}}{C}$$

$$100\mu = \frac{g_{m_1}(0.2)}{2} \qquad C_c = \frac{g_{m_1}}{2\pi f_u}$$

$$C_c = \frac{1.0 \times 10^{-3}}{2 \cdot \pi \cdot 100 \times 10^6} = 1.6pf$$

$$\frac{2(100\mu)}{0.2} = g_{m_1}$$

$$g_{m_1} = 1mS \qquad g_{m_1} = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{gs} - V_{th})$$

$$I_1 = I_2 = I_3 = I_4 \qquad \left(\frac{W}{L}\right)_1 = \frac{g_{m1}}{K_{pn}(V_{gs} - V_{th})} = \frac{\frac{2I_D}{(V_{gs}-V_{th})}}{K_{pn}(V_{gs}-V_{th})} = \frac{2I_D}{K_{pn}(V_{gs}-V_{th})^2} = \frac{2I_D}{K_{pn} V_{dsat}^2}$$

$$\left(\frac{W}{L}\right)_3 = \frac{2I_1}{K_p V_{ds}^2} = \frac{2 \cdot 100\mu}{160\mu \cdot (0.2)^2} = 31.25 \qquad = \frac{2(100\mu)}{300\mu \cdot (0.2)^2} = 16.67$$

$$\left(\frac{W}{L}\right)_5 = \frac{2(I_1 + I_2)}{K_p V_{ds}^2} = \frac{2(200\mu)}{300\mu \cdot (0.2)^2} = 33.5$$

Base on HW#5 hint File

$g_{m_6} = 10 g_{m_1}$ For 60° PM $\rightarrow I_6 = 10 I_1$

$g_{m_6} = 10mS$

$I_6 = 10\ (100\mu A)$
$= 1mA$

$$R_c = \frac{1}{g_{m_6}}\left(1 + \frac{C_L}{C_c}\right) = \frac{1}{10m} \cdot \left(1 + \frac{5pf}{1.6pf}\right) = 412.5$$

$I_6 \approx I_7 = 1mA$

$$\left(\frac{W}{L}\right)_6 = 10\left(\frac{W}{L}\right)_4 \approx 10\left[4\left(\frac{9}{1}\right)\right] \Rightarrow 40\left(\frac{9}{1}\right)$$

$$\left(\frac{W}{L}\right)_7 = 5\left(\frac{W}{L}\right)_5 = 5\left[4\left(\frac{9}{1}\right)\right] \Rightarrow 20\left(\frac{9}{1}\right)$$

$$\left(\frac{W}{L}\right)_1 = 16.67 \approx> 18 = 2\left(\frac{9}{1}\right)$$

$$\left(\frac{W}{L}\right)_3 = 31.25 \approx> 36 = 4\left(\frac{9}{1}\right)$$

$$\left(\frac{W}{L}\right)_5 = 33 \approx> 36 = 4\left(\frac{9}{1}\right)$$

b. Schematic

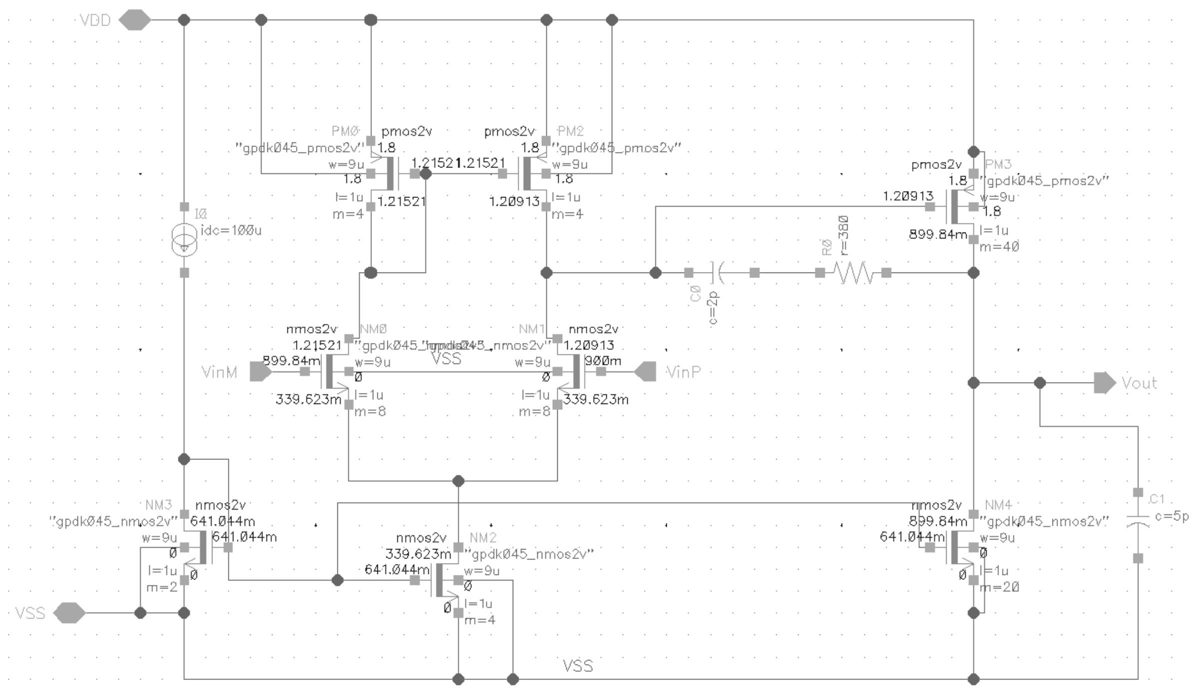


Figure 1: Two stage OPAMP schematic

2. Unity Gain Configuration DC simulation
   a. Figure 2 shows the operating region of the transistors as well as the node voltages. The sizes used in figure 1 and 2 are the same. The size of the signal transistor(NM0) is different than the designed size. This is because the gain and phase margin specs were not meet with designed values. One way to increase the gain and phase margin of the OPAMP is by increasing the signal transistor's size. As well as the compensation RC circuit.

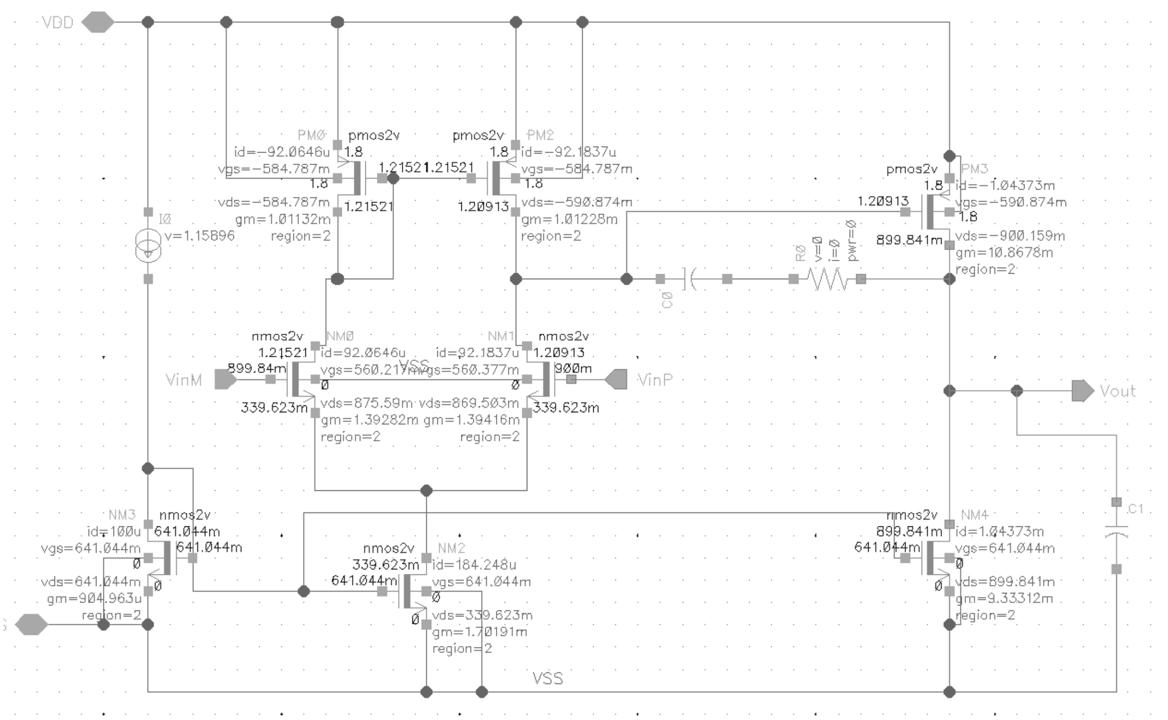


Figure 2: Two Stage OPAMP DC Operating values.

B. Figure 3 shows the current sick by the OPAMP, using it the power consumption can be calculated. PW = 1.8V*1.32797mA = 2.39mW

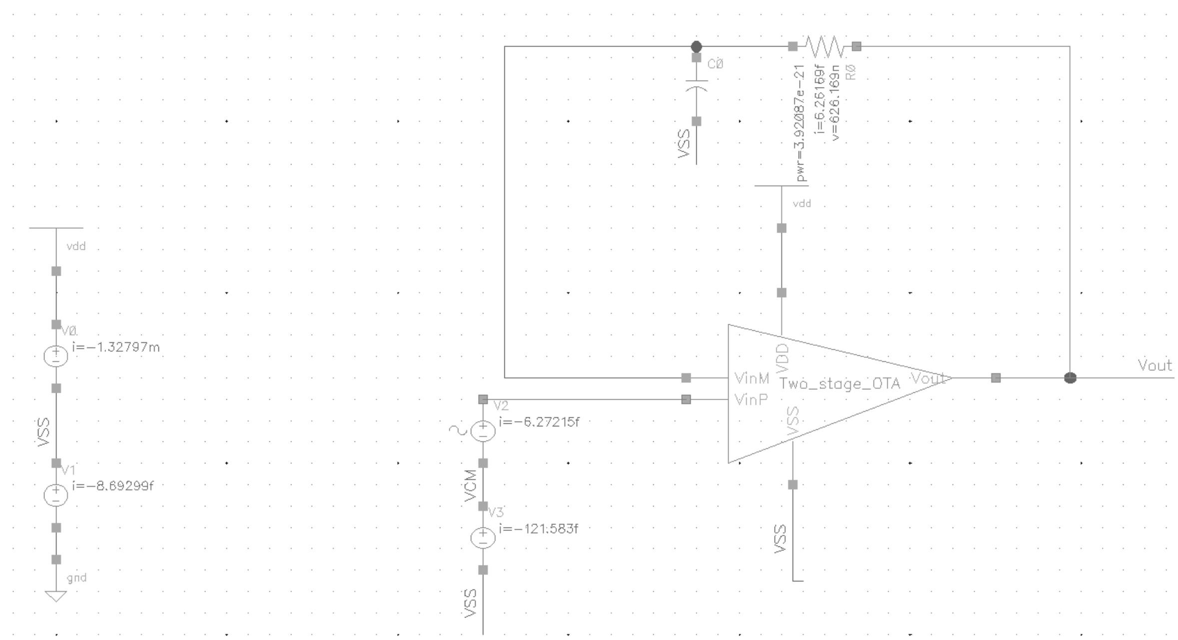


Figure 3: Two Stage OPAMP power consumption.

3. AC Response of the OPAMP
    a. Figure 4 shows the fallowing information, DC gain(A_0), -3dB bandwidth (W_{-3db}) and unity gain bandwidth(w_u).
    b. Calculating W_u base on the plot.

$W_u = A_0 * W_{-3db} = 10^{(61.868/20)} * 82.671 * 10^3 = 102.5\text{MHz}$

    c. Unity gain bandwidth from the plot, $W_u \approx$ 99.9579
    d. There is a difference between the expected and the actual unity gain bandwidth. I think it is due to several reasons. One of the reasons is because the curser on the plot is not exactly on the Zero dB point. Another reason can be because the parasitics of the transistors can be affecting the performance of the OPAMP.

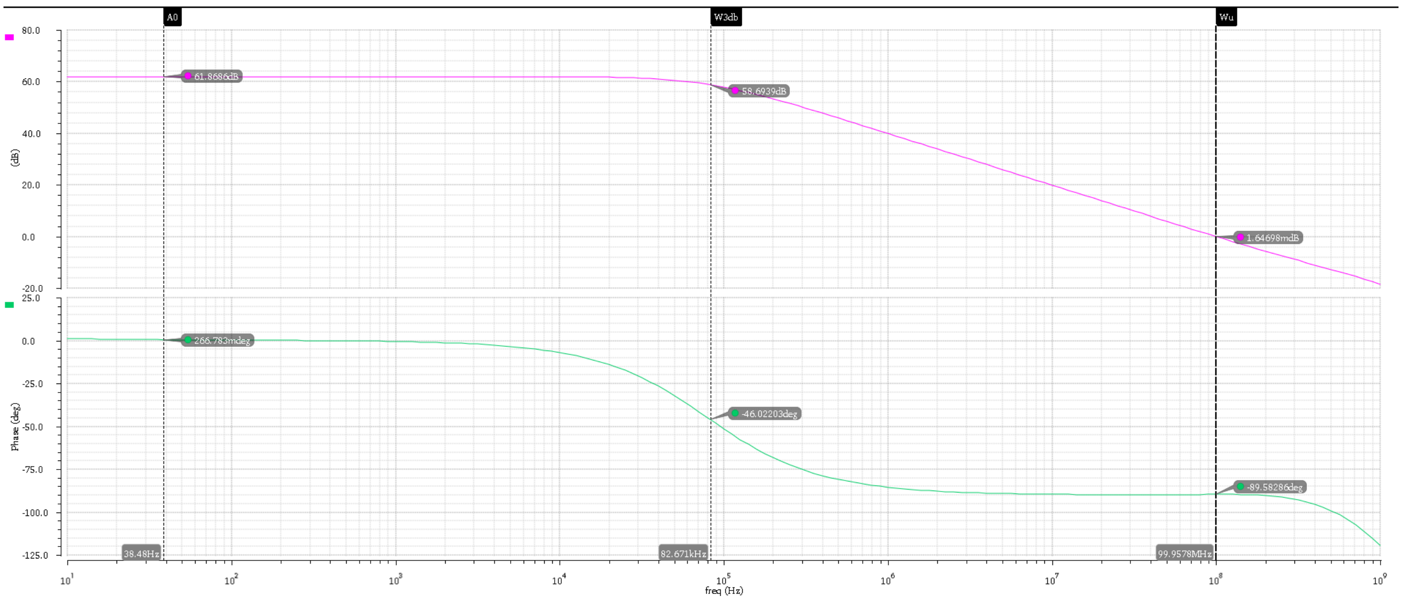


Figure 4: AC response of the OPAMP.

4. Transient Response.
    a. Figure 5 shows the Slew rate of the OPAMP. SR = 74.29 MV/S

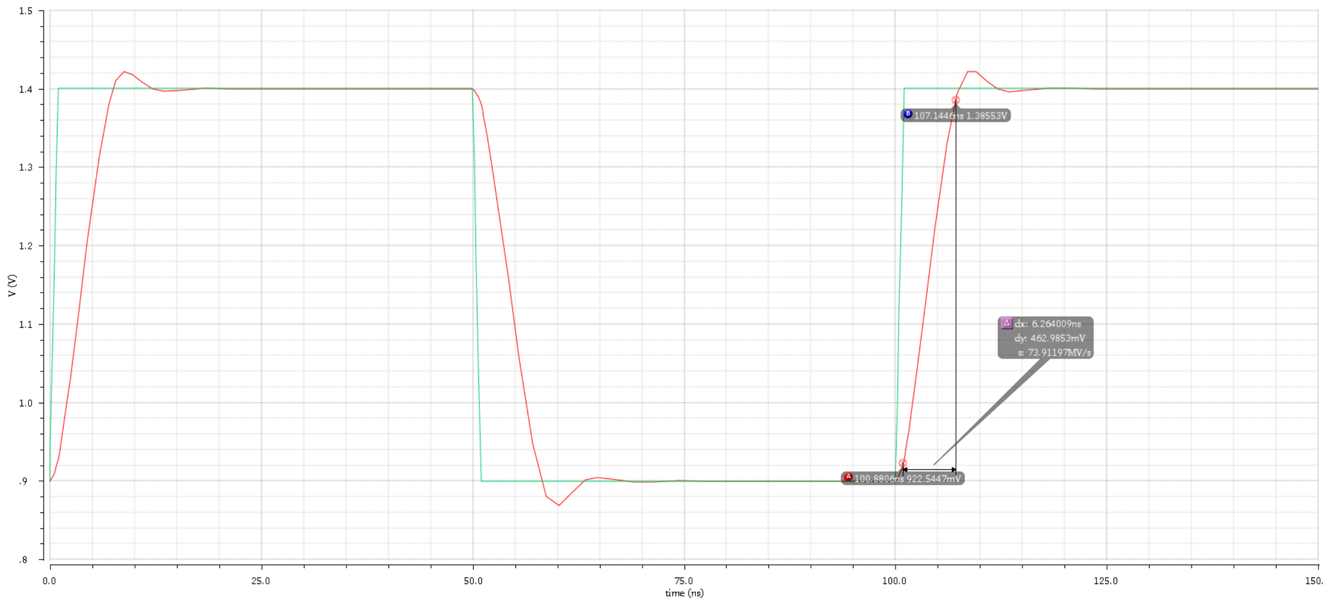


Figure 5: Transient response of the OPAMP.

5. Replacing Rz with a PMOS transistor.
    a. Figure 6 shows the transistors sizes and figure 7 shows the transistors DC operating values. The transistors have been size to meet the require specs.

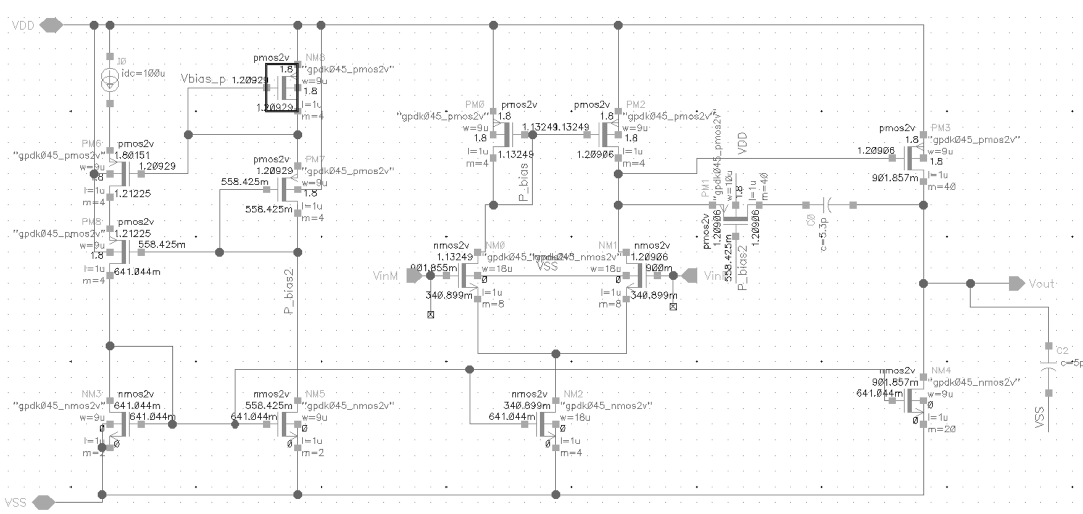


Figure 6: Two stage OPAMP with PMOS as a compensation Rz transistor sizes.

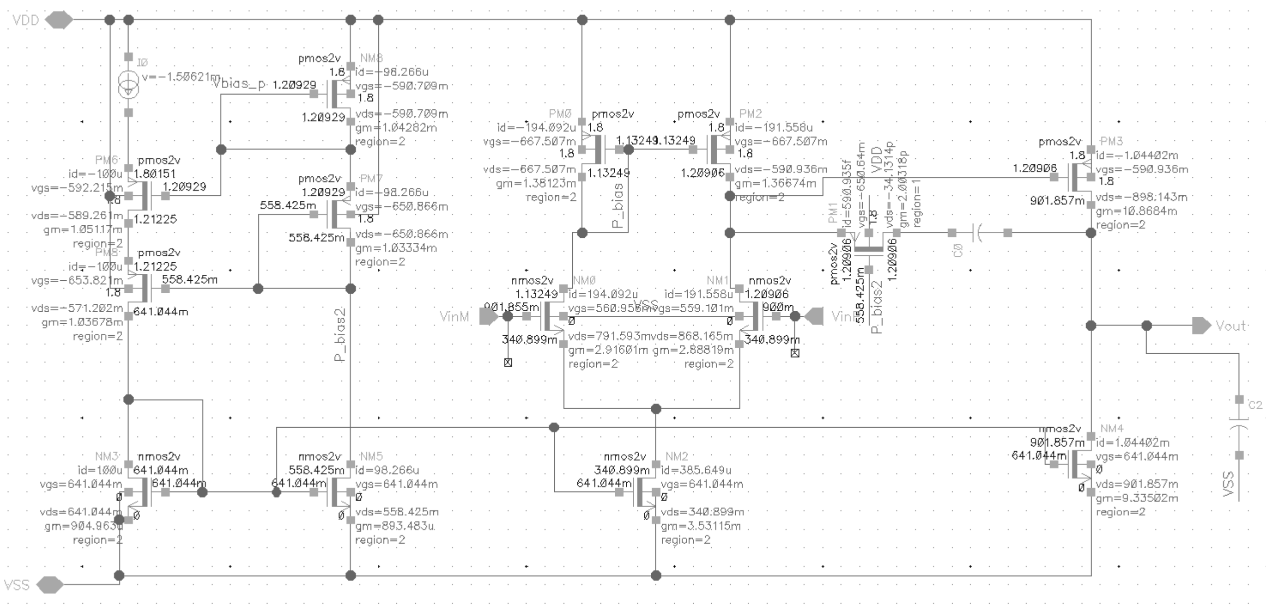


Figure 7: Two stage OPAMP with PMOS as a compensation Rz DC operating values and node voltages.

b. Figure 8 shows the current sink by the OPAMP with a PMOS as Rz compensation, using it the power consumption can be calculated.
   PW = 1.8V*1.34207mA = 2.416mW

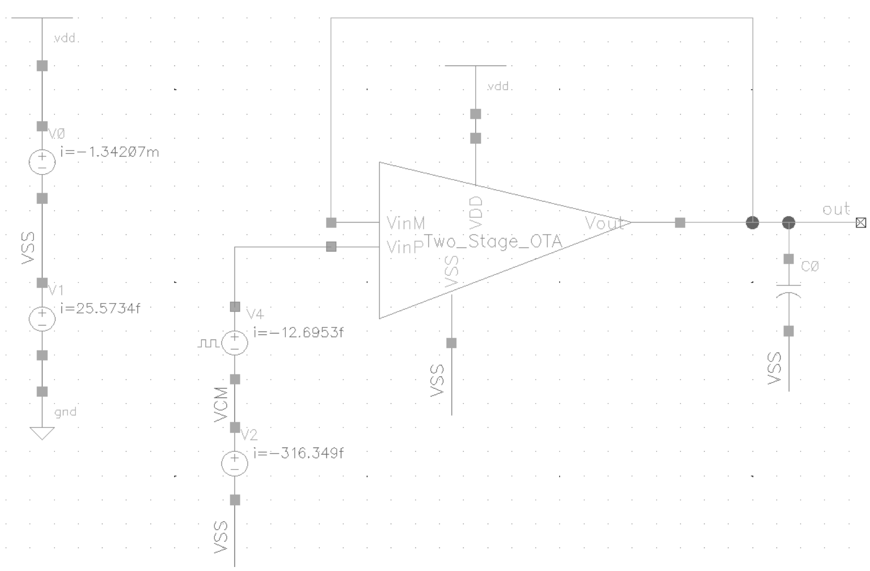


Figure 8: OPAMP with PMOS as a compensation Rz power consumption.

c. AC response of the Two stage OPAMP with PMOS as a compensation Rz.
d. Figure 9 shows the fallowing information, DC gain(A_0), -3dB bandwidth (W_{-3db}) and unity gain bandwidth(w_u).
e. Calculating W_u base on the plot.

$W_u = A_0 * W_{-3db} = 10^{(62.68/20)} * 85.271 * 10^3 = 115.958\text{MHz}$

f. Unity gain bandwidth from the plot, $W_u \approx 100.3\text{MHZ}$

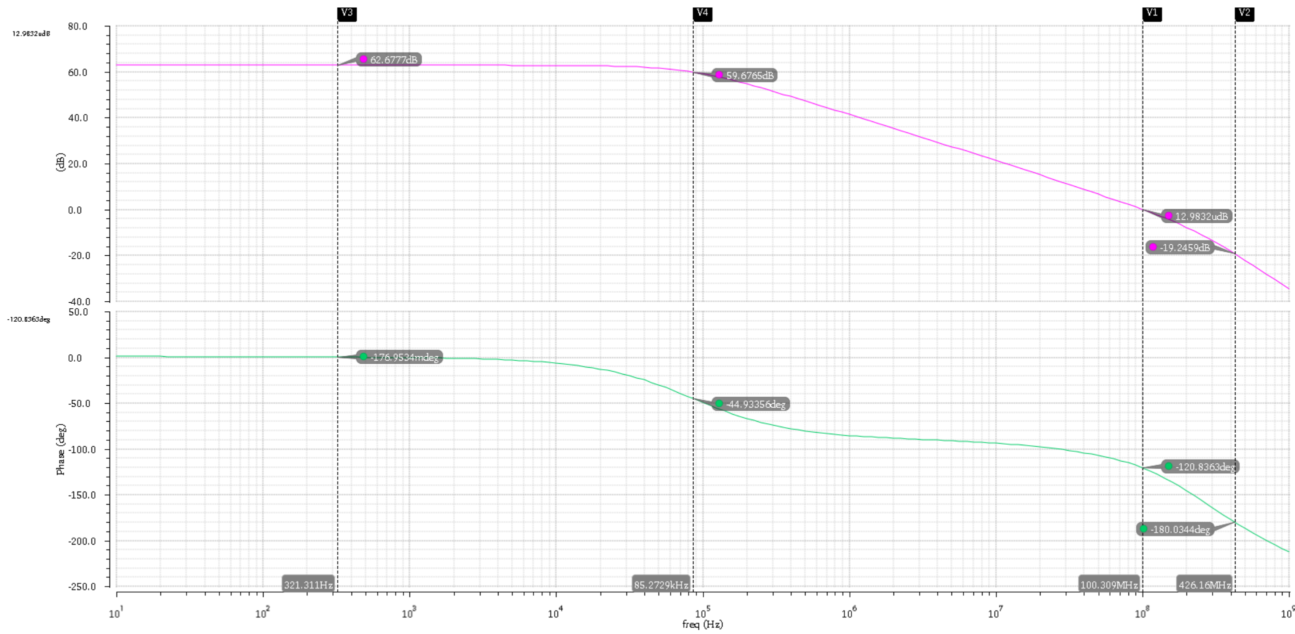


Figure 9: AC responses of the OPAMP with PMOS as a compensation Rz where A_0=1359.88 W_{-3dB}= 85.3KHZ, W_u=100MHZ, PM = 60˚ and GM = 19 dB.

g. Transient response. Figure 10 shows the slew rate of the OPAMP with PMOS as a compensation Rz.

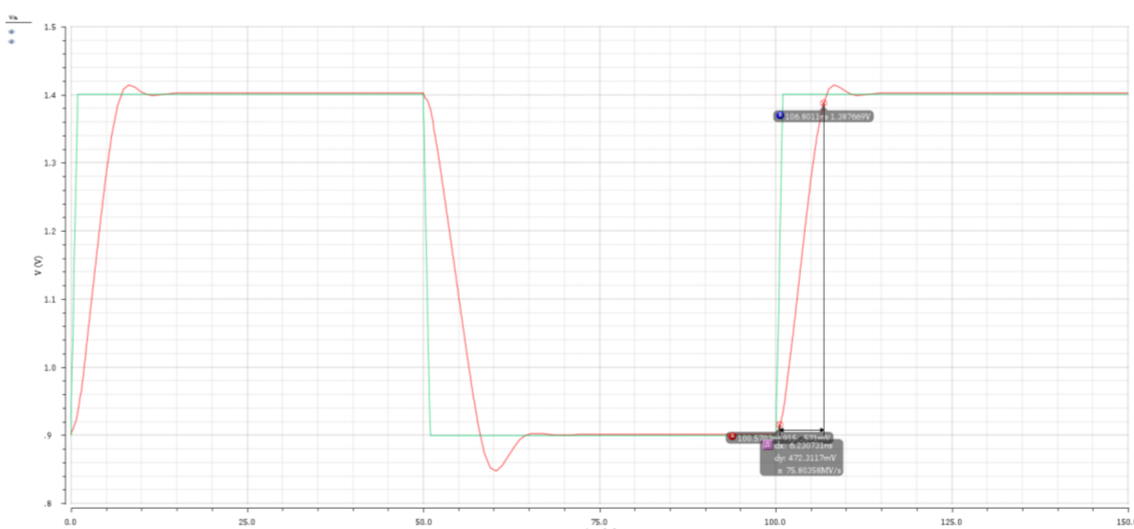


Figure 10: Transient response of OPAMP with PMOS as a compensation Rz.