Texas A&M University
Electrical Engineering Department

ECEN 665

Laboratory #8: Analysis and Simulation of a CMOS Power Amplifier

Objectives: To understand the fundamental operation of a single-stage CMOS power amplifier (PA) and analyze its performance trade-offs for different bias conditions (class A, AB, B and C amplifier modes). To learn how to characterize the main figures of merit of a PA using Spectre.

1. Schematic setup

Using a library for CMOS 0.5um technology in cadence, create the schematic shown in figure 1. This is a single-stage CMOS PA designed to operate around 1.9GHz. The component values are given in Table 1. RFC is a biasing inductor (RF "Choke"), which should present large impedance at the frequency of operation. CB is a bypass capacitor employed to provide DC isolation between the active device (N0) and the load (50ohm, Port 1). Inductor L1 forms a band-pass filter with the parasitics of N0 to filter out undesired harmonics. When VDC is set to 900mV this PA operates in class A mode and is able to deliver a power of 10dBm with a drain efficiency of around 50%.

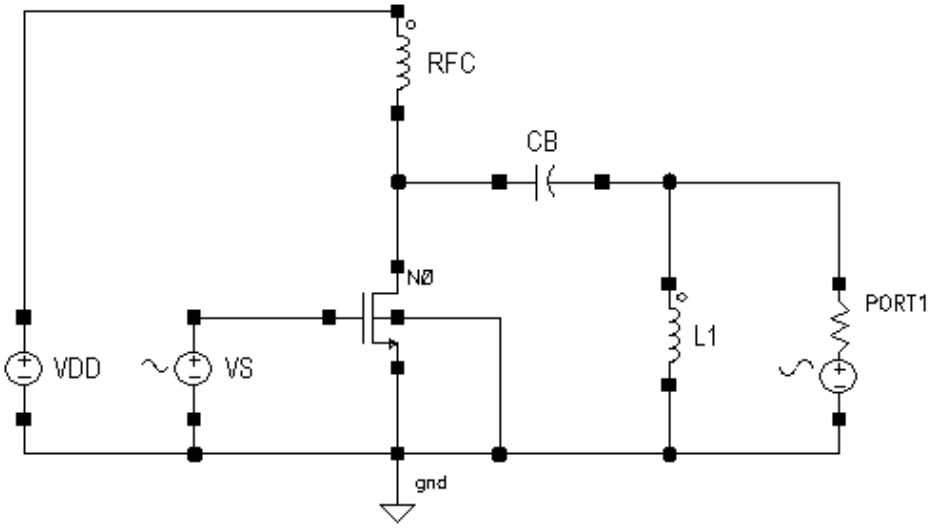

Figure 1. PA circuit schematic

Table 1. Component values

Component	Value
L1	3n
CB	50pF
RFC	100n
N0	W = 48um, L = 0.6um, m = 40
PORT1	Resistance = 50ohm, Source type = dc
VDD	VDC = 1V
VS	DC Voltage = VDC, Amplitude = VIN, Frequency = 1.9GHz

1.1 List and briefly explain the main figures of merit for a PA in a wireless transceiver. Under which conditions the linearity of a power amplifier becomes a relevant issue? Why is it often a pre-amplifier (or two-stage PA) required?

1.2 The PA in Figure 1 does not have an input matching network. Under which circumstances would an input match be required? What would be a reasonable way to couple an on-chip preamplifier?

1.3 Explain the concept of conduction angle in a PA and provide a brief definition of the class A, AB, B and C operating modes for a PA along with their respective maximum theoretical efficiencies.

2. Transient simulation

The class of operation of a PA is determined by its current and voltage waveforms. A transient simulation is useful to analyze and verify the design of a power amplifier. Figure 2 shows the current signals at the load, the drain of the nmos transistor and the power supply. For this simulation VDC=900mV and VIN=500mV.

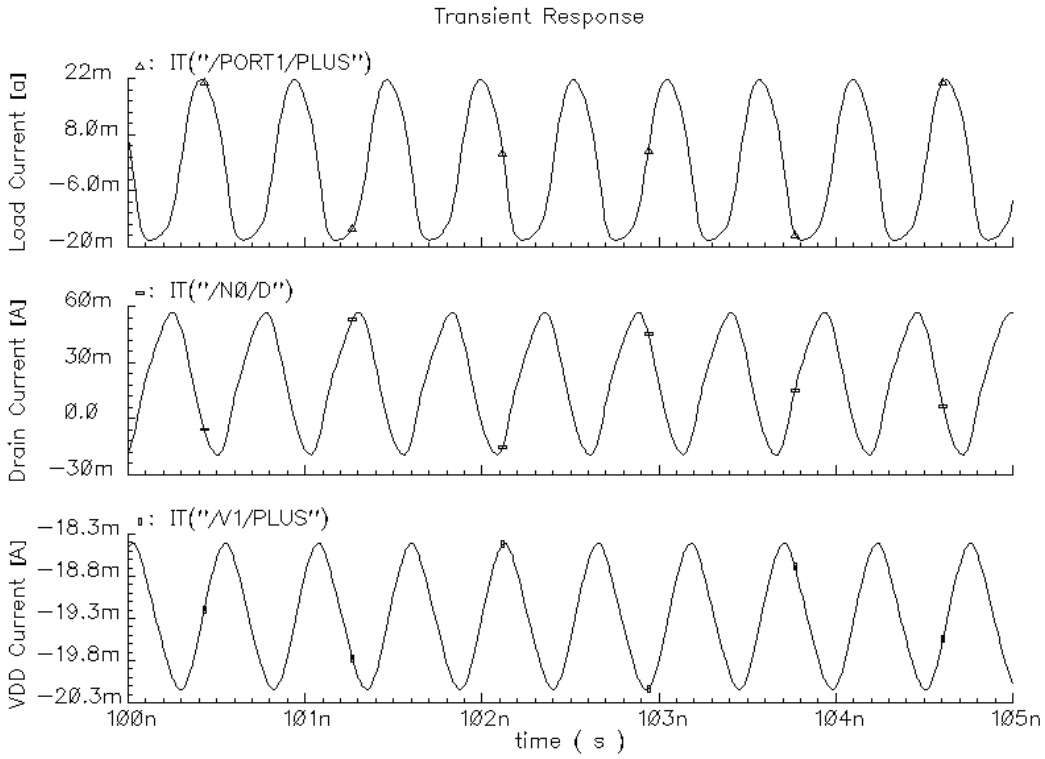

Figure 2. Current waveforms for the CMOS PA

2.1 Run a transient simulation. Plot the current waveforms shown in figure 2 and also the current flowing across CB. What is the operating mode of this PA? What is the power delivered to the load? Why there is a negative swing in the drain current? From these simulation results, what is the drain efficiency of the amplifier?

NOTE: For this and the next simulations make sure that you save the current waveforms at the terminals of interest.

3. PSS and SPSS simulation

3.1 Run a PSS simulation (same parameters as the transient simulation) and plot the output spectrum (choose at least 5 harmonics). What is the power delivered to the load at the fundamental frequency? What is the THD? From this simulation it is also possible to measure the DC power dissipated in the power supply. Obtain the drain efficiency. How does the output power, THD and efficiency change if you remove the inductor L1?

The efficiency and operating class of the PA are strongly dependent on the DC bias and the input amplitude. SPSS Analysis can be employed to analyze the parametric behavior of the PA. Figure 3 and 4 show the simulation results. Notice that, as the input amplitude increases, the supply power keeps constant while the output power grows. This is a characteristic of class A amplifiers (why?).

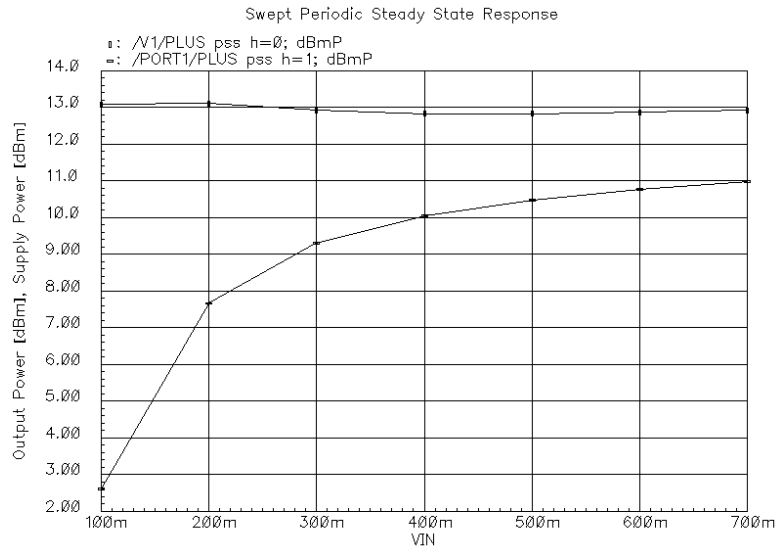

Figure 3. SPSS Results: Output power and Supply power Vs. VIN

The drain efficiency is shown in figure 4. Note that, to obtain this plot, the power at the load and the supply have to be compared in magnitude NOT in dBm. Why does the drain efficiency go beyond 50%?

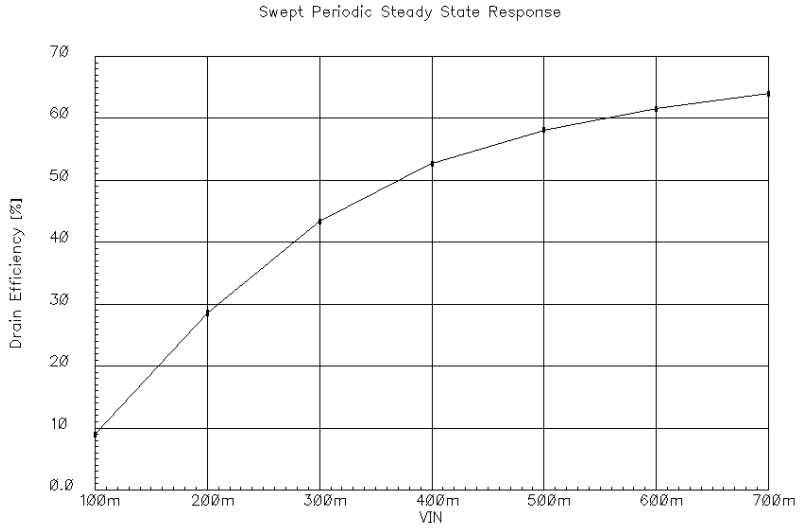

Figure 4. SPSS Results: Drain Efficiency Vs. VIN

3.2 Obtain transient plots (like the ones in section 2.1) and parametric plots (like figure 3 and 4) for VDC=0.5V, 0.6V, 0.7V, 0.8V. What is the maximum achievable output power and drain efficiency in each case? What is the power and efficiency obtain at VIN=300mV in each case? From your observations, what is the operating class of the PA for the different bias conditions?

3.3 What is the role of the DC supply voltage in the maximum power and efficiency of the amplifier? Is VDD 1V a convenient choice for an output power of 10dBm? If the output power specification is only 4dBm which VDD and VDC would you use? Justify your answer with simulation results.

3.4. Provide your own conclusions about the trade-off between maximum power and efficiency for the different operating classes of a PA.