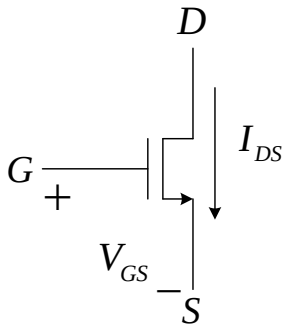
Elmore 2

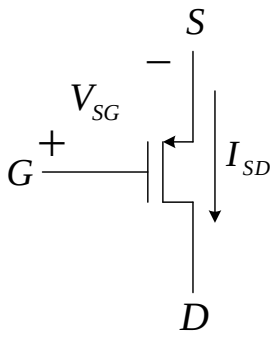
Lecture 17

- nMOSFET



Operation Regions	Voltages	Current
Cut Off	$V_{GS} \le V_{Tn}$	$I_{DS} = 0$
Saturation	$V_{GS} > V_{Tn}$ $V_{DS} > V_{GS} - V_{Tn}$	$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2\left(1+\lambda V_{DS}\right)$
Resistive	$V_{GS} > V_{Tn}$ $V_{DS} < V_{GS} - V_{Tn}$	$I_{DS} = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{GS} - V_{Tn}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$

- pMOSFET

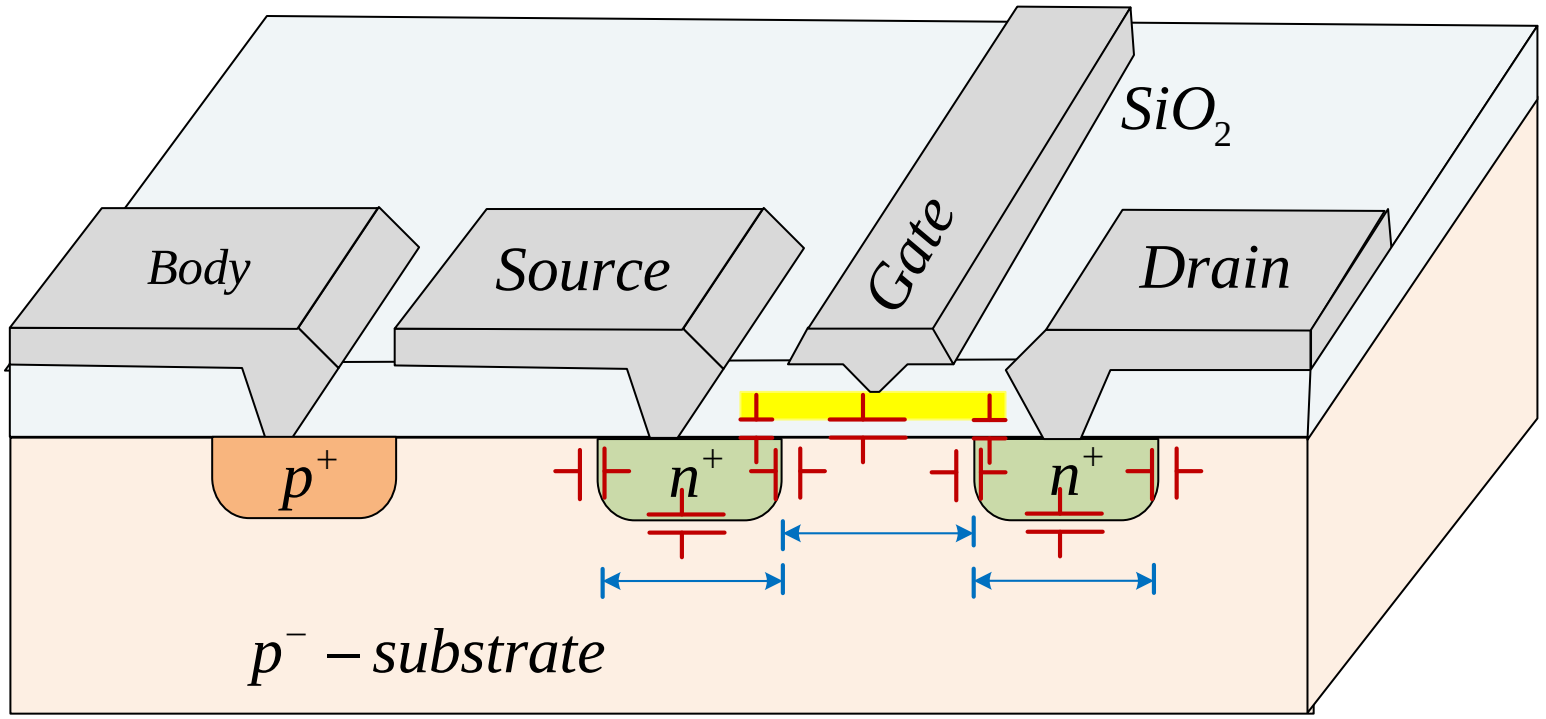


Operation Regions	Voltages	Current
Cut Off	$V_{SG} \le \lvert V_{Tp} \rvert$	$I_{SD} = 0$
Saturation	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} > V_{SG} - \lvert V_{Tp} \rvert$	$I_{SD} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG} - \lvert V_{Tp} \rvert\right)^2\left(1+\lambda V_{SD}\right)$
Resistive	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} < V_{SG} - \lvert V_{Tp} \rvert$	$I_{SD} = \mu_p C_{ox}\frac{W}{L}\left[\left(V_{SG} - \lvert V_{Tp} \rvert\right)V_{SD} - \frac{V_{SD}^2}{2}\right]$

- Enhancement mode MOSFET transistor region of operation

	Cut-off	Resistive	Saturation
nMOS	$V_{GSn} < V_{Tn}$ $V_{IN} < V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} < V_{GSn} - V_{Tn}$ $V_{OUT} < V_{IN} - V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} > V_{GSn} - V_{Tn}$ $V_{OUT} > V_{IN} - V_{Tn}$
pMOS	$V_{GSp} > V_{Tp}$ $V_{IN} > V_{Tp} + V_{DD}$	$V_{GSp} < V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{Tp}$ $V_{OUT} > V_{IN} - V_{Tp}$	$V_{GSp} = V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{Tp}$ $V_{OUT} < V_{IN} - V_{Tp}$

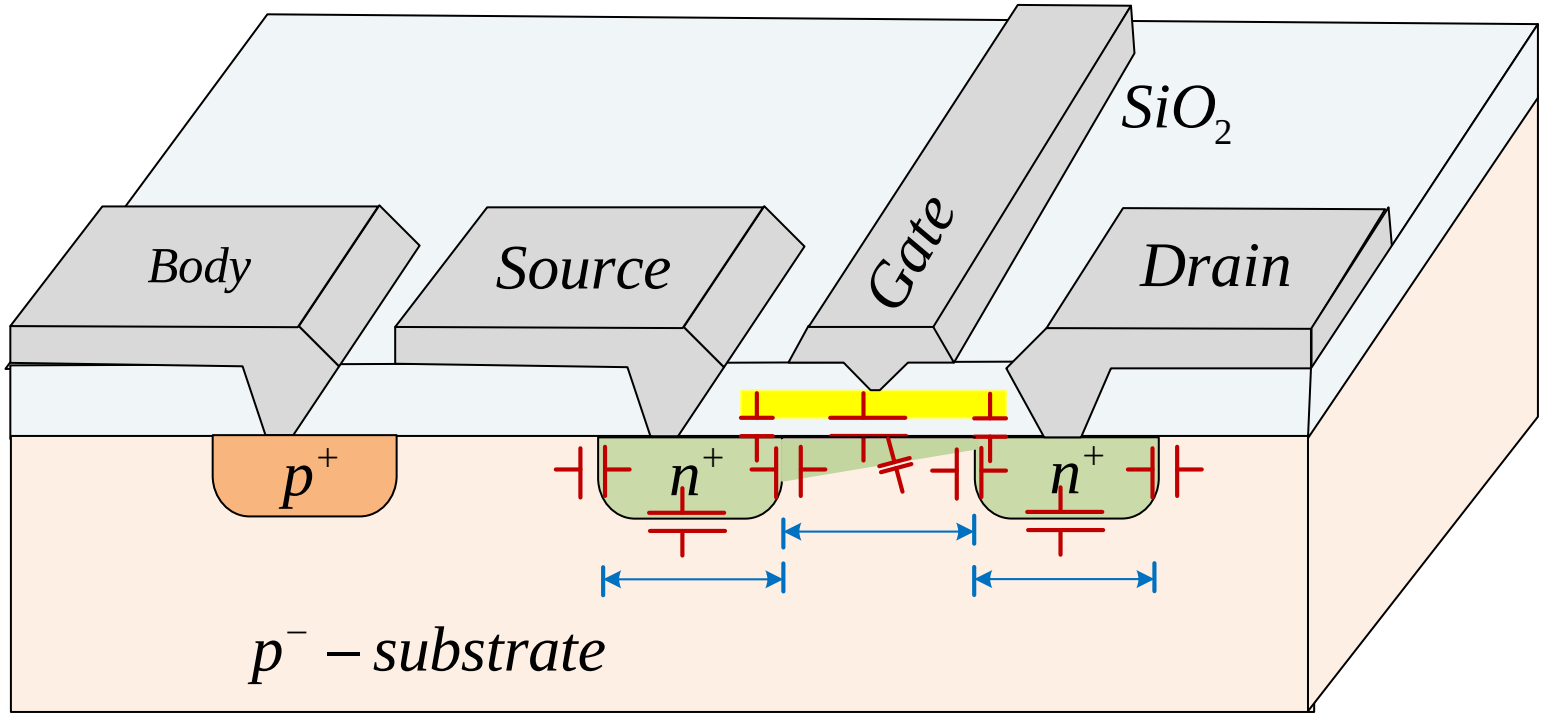
- Intrinsic capacitors in the cut-off $V_{GS} < V_{TN}$



- Channel is not inverted

$$C_{gate} = C_{gate-body} = C_0 = C_{ox}WL = \frac{\varepsilon_{ox}}{t_{ox}}WL$$

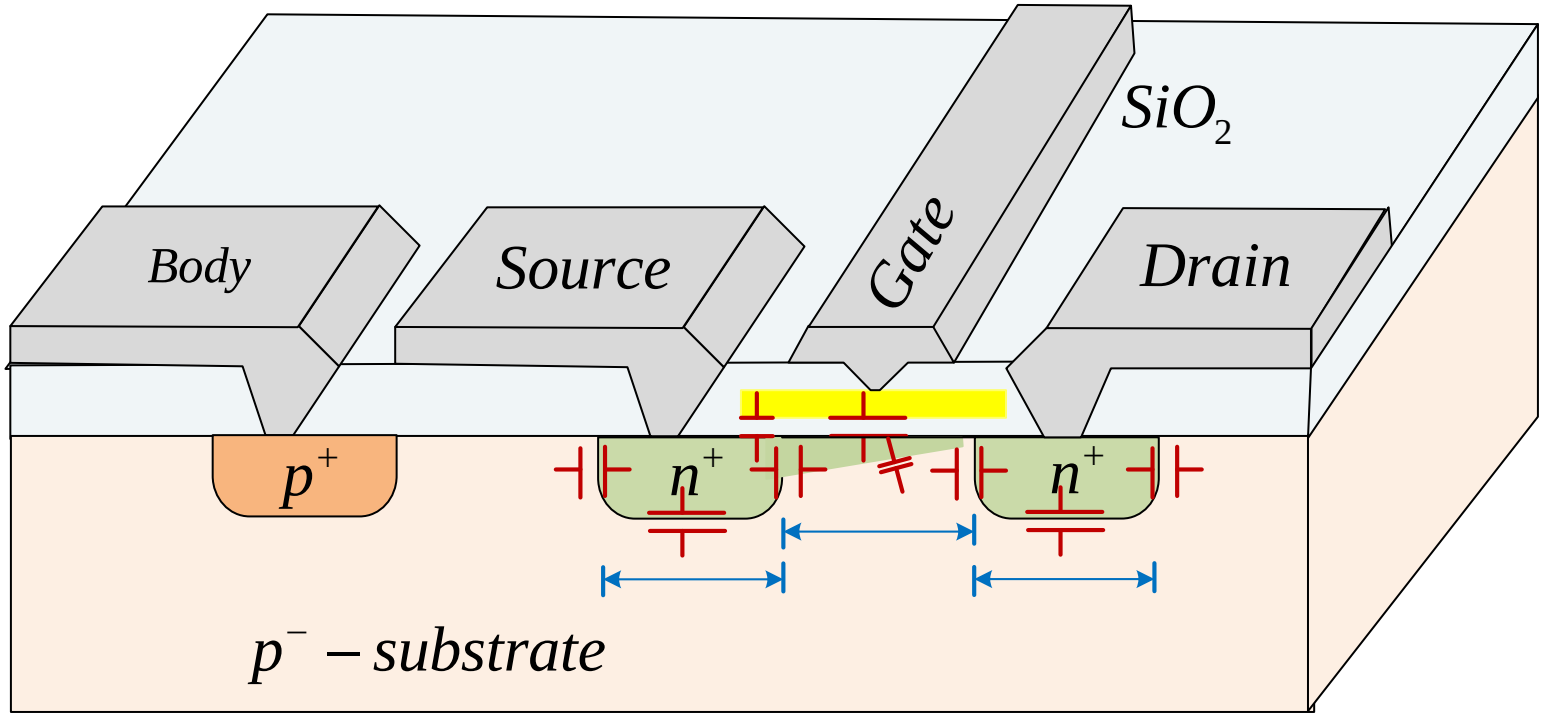
- Intrinsiccapacitors in the non-saturation $V_{GS} > V_{TN}$ & $V_{DS} < V_{GS} - V_{TN}$



$$C_{gate} = C_{gate-body} + C_{gate-source} + C_{gate-drain}$$

$$C_{gate} = 0 + \frac{C_0}{2} + \frac{C_0}{2} = C_0$$

- Intrisic capacitors in the saturation $V_{GS} > V_{TN}$ & $V_{DS} > V_{GS} - V_{TN}$



$$C_{gate} = C_{gate-body} + C_{gate-source} + C_{gate-drain}$$

$$C_{gate} = 0 + \frac{2C_0}{3} + 0 = \frac{2C_0}{3}$$

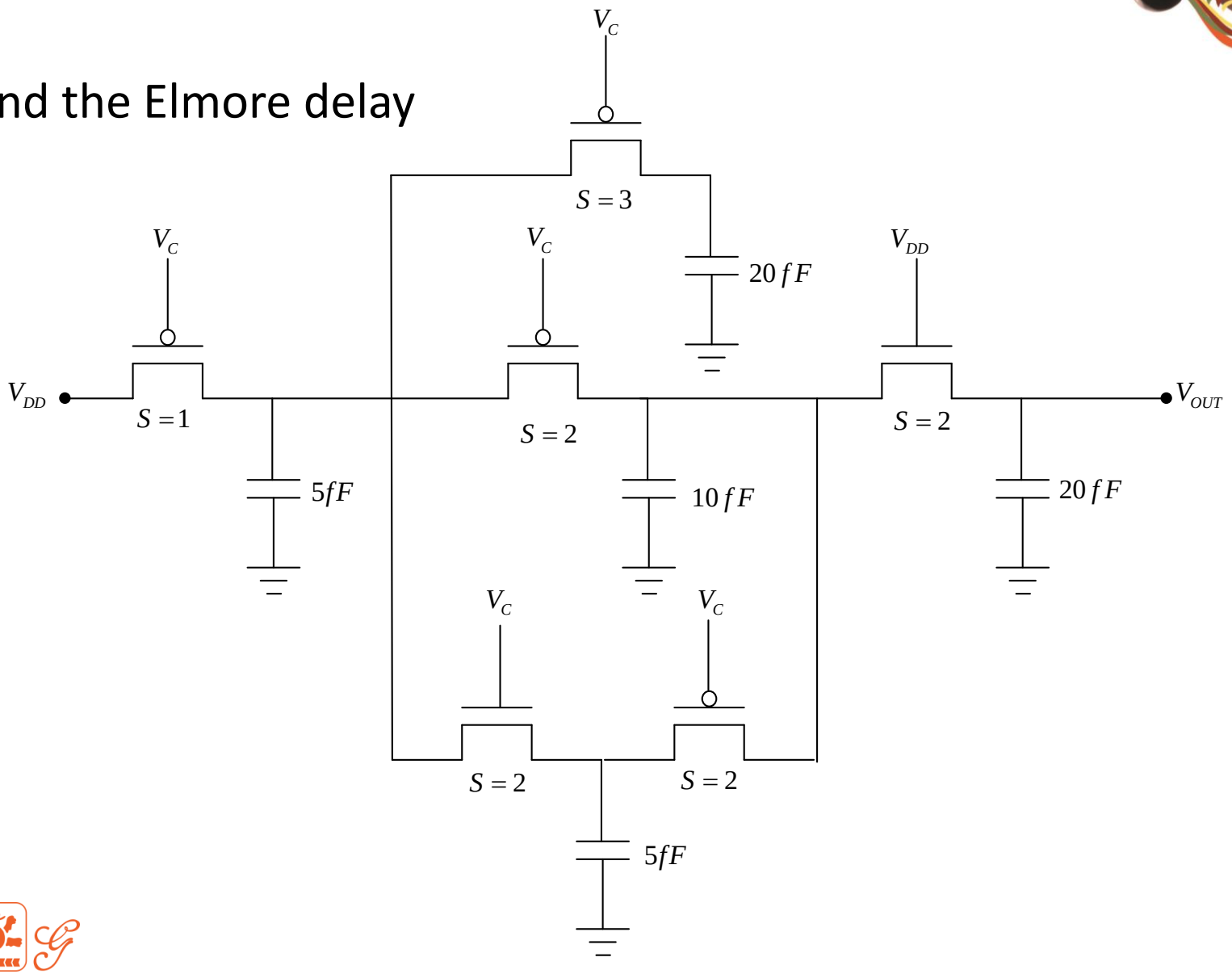
- Intrinsic MOS gate capacitor

Operation	Cut-off	Saturation	Resistive
C_{gs}	0	$\frac{2}{3}C_{OX}WL_{eff}$	$\frac{1}{2}C_{OX}WL_{eff}$
C_{gd}	0	0	$\frac{1}{2}C_{OX}WL_{eff}$
C_{gb}	$C_{OX}WL_{eff}$	0	0
C_g	$C_{OX}WL_{eff}$	$\frac{2}{3}C_{OX}WL_{eff}$	$C_{OX}WL_{eff}$

- Detailed gate capacitors

Operation	Cut-off	Saturation	Resistive
C_{gs}	$C_{OX}WL_D$	$\frac{2}{3}C_{OX}WL_{eff}+C_{OX}WL_D$	$\frac{1}{2}C_{OX}WL_{eff}+C_{OX}WL_D$
C_{gd}	$C_{OX}WL_D$	$C_{OX}WL_D$	$\frac{1}{2}C_{OX}WL_{eff}+C_{OX}WL_D$
C_{gb}	$C_{OX}WL_{eff}$	0	0

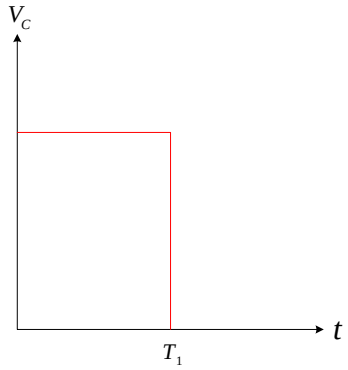
- Find the Elmore delay



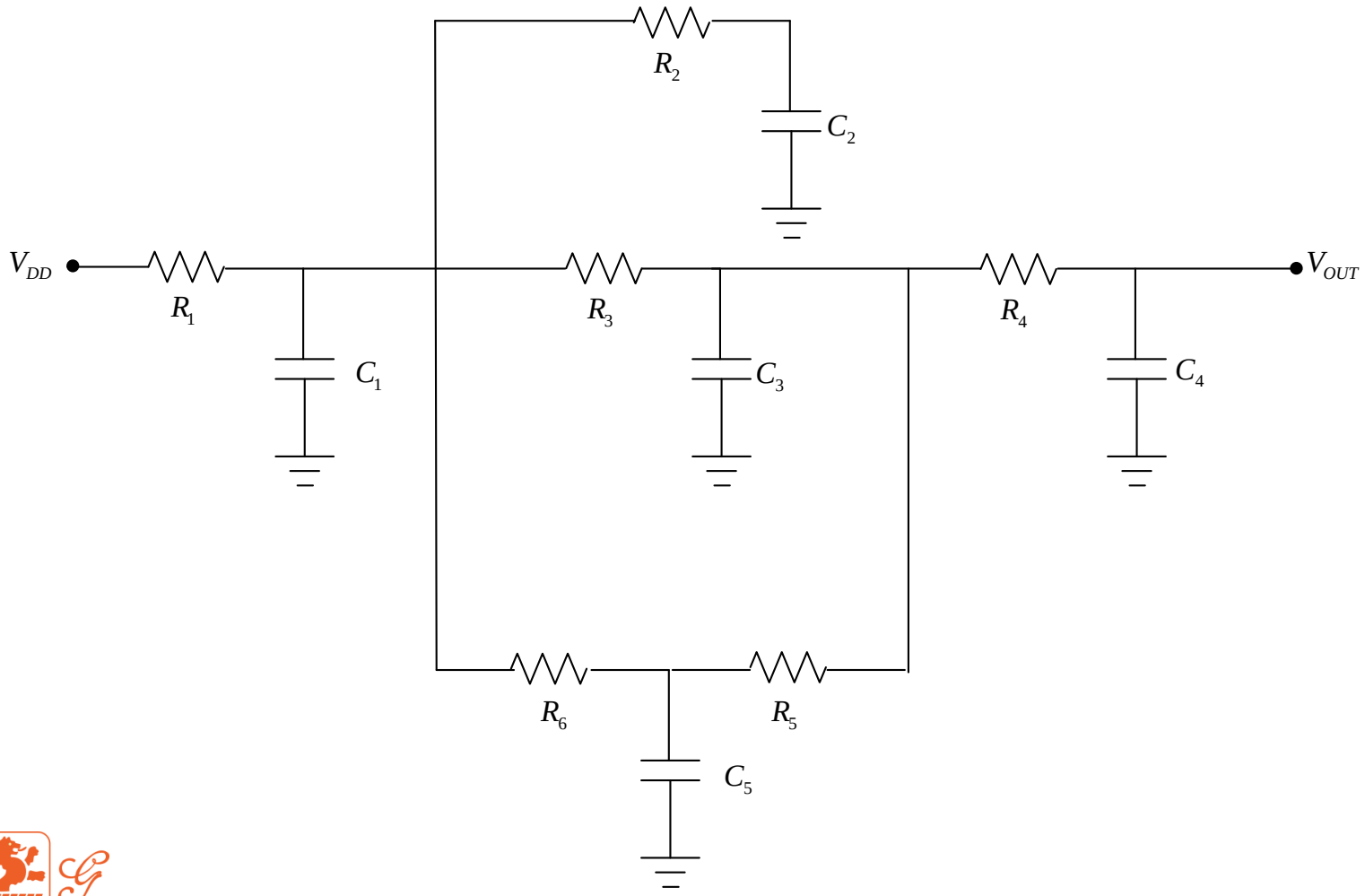
- Find the Elmore delay after T_1, given:
- Minimum size: $s = 1,\ W = W_{\min}$
- Size: $s = 2,\ W = 2W_{\min}$
- Resistances: $R_{eqnMOS} = 10k\Omega$, $R_{eqpMOS} = 20k\Omega$
- Capacitances: $C_{gs} = C_{gd} = 0.5fF$

$$C_{db} = C_{sb} = 1fF$$

- Ignore overlap capacitance and feedthrough.
- Except $V_{in} = V_{DD}$, initially all nodes are at zero.



- Equivalent RC circuit.



- R and C equivalent

$$R_1 = R_{eqpMOS} = 20k\Omega$$

$$C_1 = 5fF + 6C_{gs} + 8C_{db} = 5fF + 6(0.5) + 8(1) = 16fF$$

$$R_2 = \frac{R_{eqpMOS}}{3} = 6.7k\Omega$$

$$C_2 = 20fF + 3C_{gs} + 3C_{db} = 20fF + 3(0.5) + 3(1) = 24.5fF$$

$$R_3 = \frac{R_{eqpMOS}}{2} = 10k\Omega$$

$$C_3 = 10fF + 4C_{gs} + 4C_{db} = 10fF + 4(0.5) + 4(1) = 16fF$$

- R and C equivalent

$$R_4 = \frac{R_{eqnMOS}}{2} = 5k\Omega$$

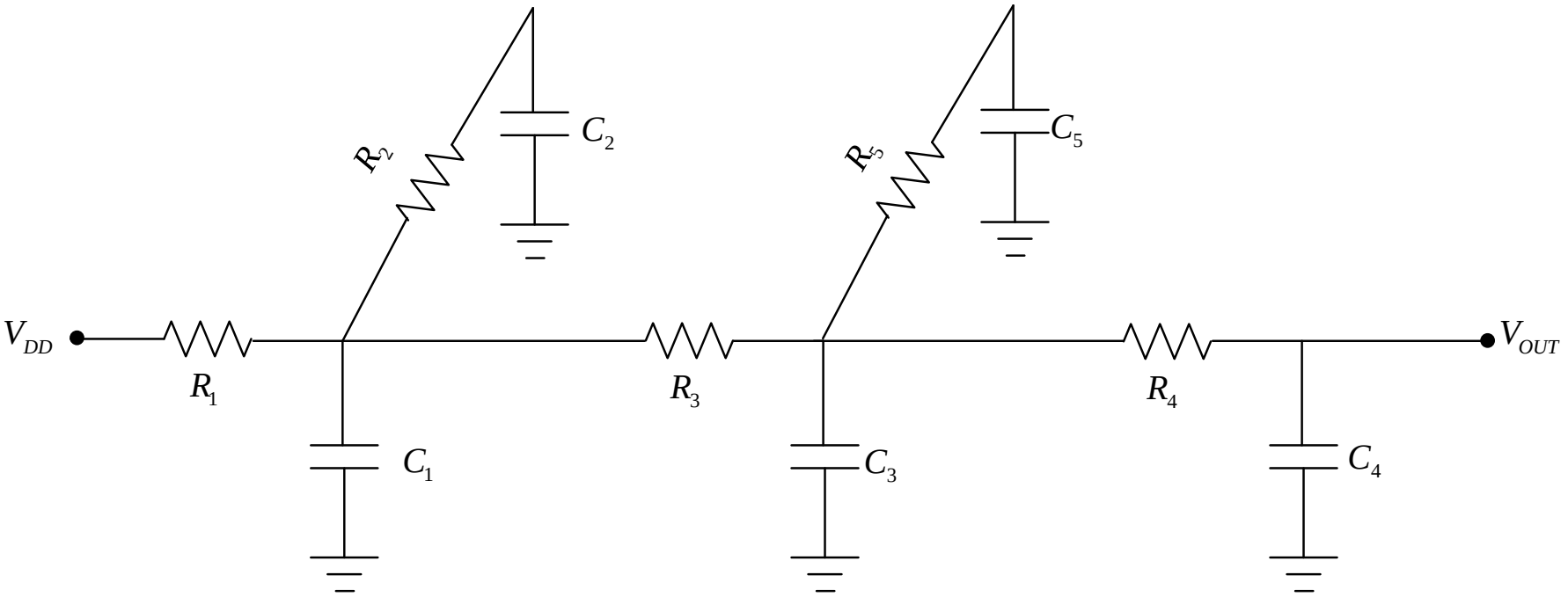
$$C_4 = 10fF + 4C_{gs} + 4C_{db} = 20fF + 4(0.5) + 4(1) = 26fF$$

$$R_5 = \frac{R_{eqpMOS}}{2} = 10k\Omega$$

$$C_5 = 5fF + 2C_{gs} + 4C_{db} = 5fF + 4(0.5) + 4(1) = 10fF$$

$$R_6 = \infty$$

- Tree-structured RC network



- The Elmore delay

$$\tau_{out} = R_1C_1 + R_1C_2 + (R_1 + R_3)C_3 + (R_1 + R_3)C_5 + (R_1 + R_3 + R_4)C_5$$

$$t_{PHL} = 0.69\tau_{V_{OUT}}$$