UNIVERSITY OF CALIFORNIA, BERKELEY

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Due Friday, February 5, 5pm, box in 240 Cory

[PROBLEM 1] VTC

The circuits of Fig.1 show different implementations of an digital inverter, whose output is connected to a capacitor. Assume $V_{TN}=|V_{TP}|=0.3V$, and the output capacitor, C_L, is initially discharged. Ignore sub-threshold conduction and body effect. (25 pts)

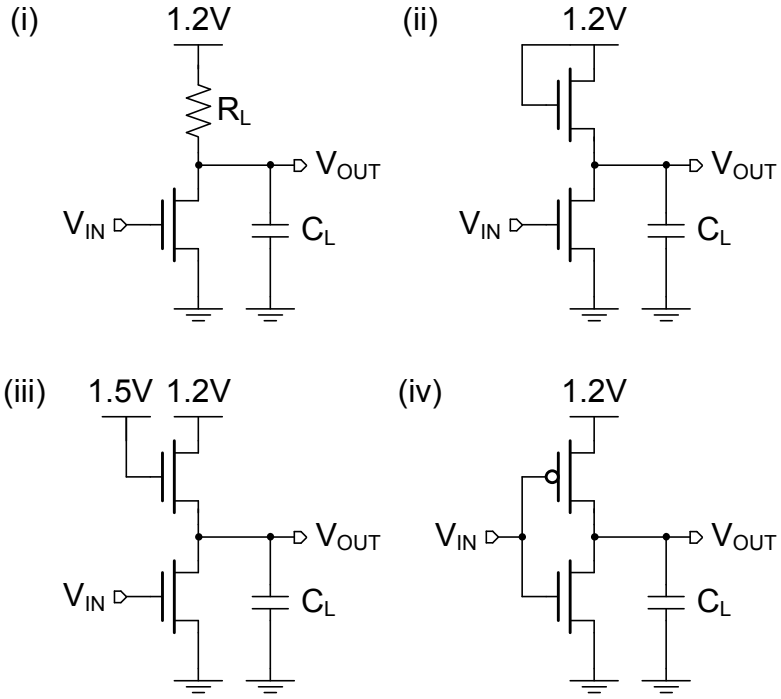

Fig.1. Different implementation of an inverter

(a) **Which one(s)** of the circuits consume(s) static power when the input is high (V_{IN}=1.2V)? (5 pts)

All inverters but the CMOS inverter, (iv), consume static power when the input is high. Notice that in the first three inverters, (i)~(iii) when the input is high, there is always a direct connection from VDD to GND.

(b) **Which one(s)** of the circuits consume(s) static power when the input is low (V_{IN}=0V)? (5 pts)

None of the static inverters consumes power when the input is low because there is no path from VDD to GND.

(c) V_{OH} of which circuit(s) is 1.2V (if possible)? (5 pts)

All inverters but the saturated enhancement inverter,(ii), has a VOH of 1.2 V.

(d) V_{OL} of which circuits(s) is 0V (if possible)? (5 pts)

Only the CMOS inverter, (iv), has a VOL of 0 V.

(e) The proper functionality of which circuit(s) depends on the size of the devices? (Note that they are designed for an 'DIGITAL INVERTER') (5 pts)

Except for the CMOS inverter, (iv), all the other inverters' functionality depend on the relative sizes of the transistors.

[PROBLEM 2] SWITCH MODEL

(a) Find the final value of the voltage V_{OUT} for the various switch logics as shown in Fig.2. Assume that $V_{TN}=|V_{TP}|=0.3V$, that and the output capacitor, C_L, is initially discharged. Ignore sub-threshold conduction and body effect. (21 pts)
All middle nodes are discharged initially.

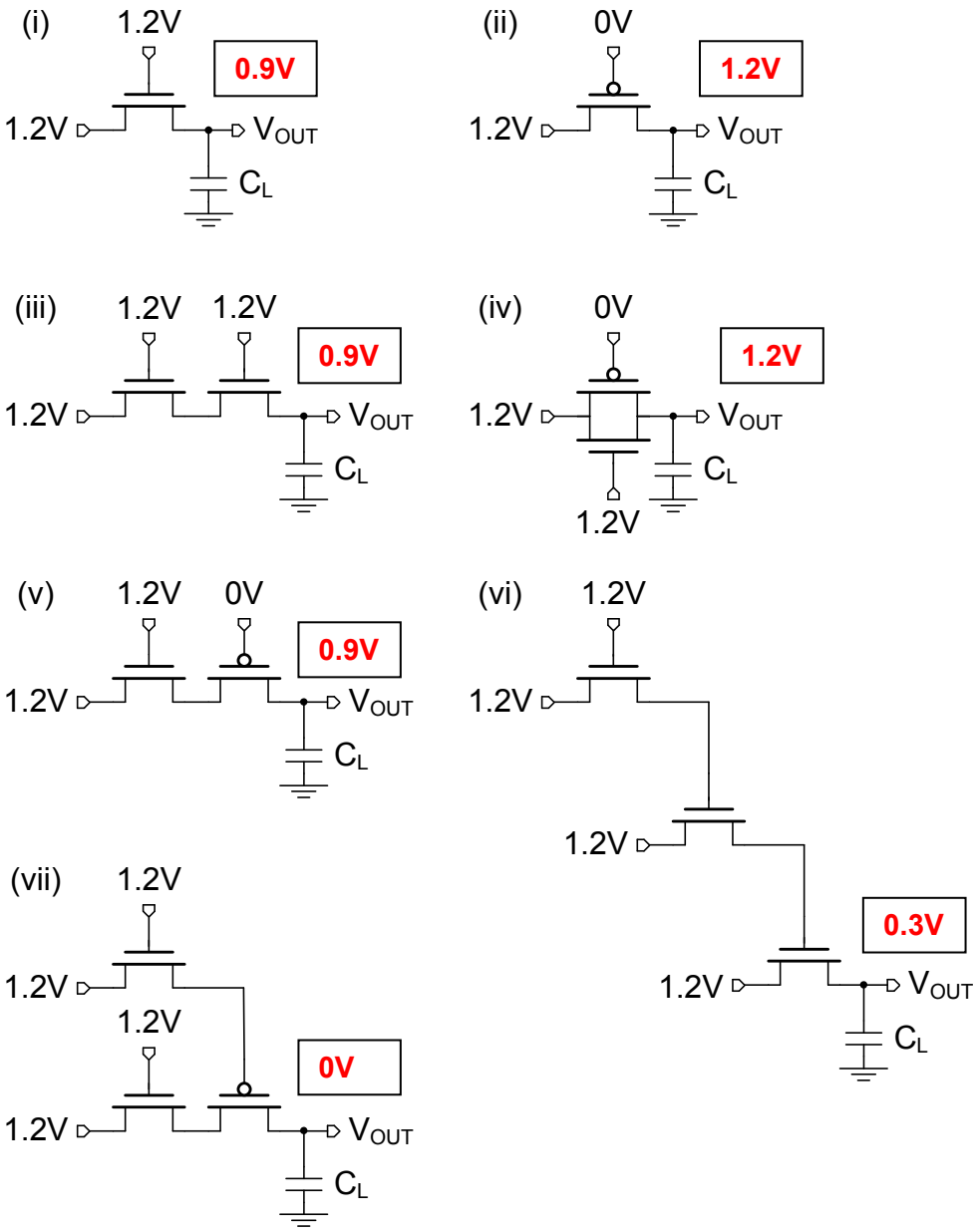

Fig.2 (a).

(b) Find the final value when the input is high, V_{IN}=1.2V.

VDD-2*VTN=0.6V (3pt)

After the output reaches its final value, a 1.2V to 0 step is applied to the input, V_{IN}. Determine the energy consumed in the transistors, $\mathbf{E_{1->0}}$, from Fig.2.(b) during the transition. The load capacitor C_L is 10fF. Ignore any other parasitic capacitors except C_L. (8 pts)

Because stored Energy is totally dissipated in the transistor,
E(diss) = E(stored)
E1->0 = ½* CL * $(VDD-2*VTN)^2$=0.5*(10f)*$(1.2-0.6)^2$=1.8fJ (5pt)

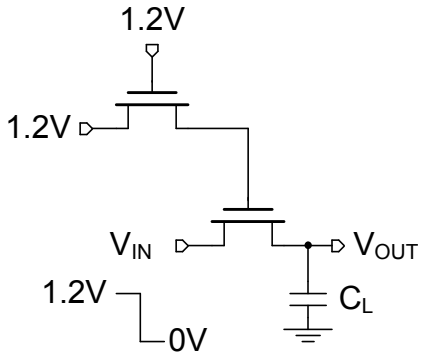

Fig.2 (b).

(c) For Fig.2.(c), Initially output voltage, V_{OUT}, is discharged, V_{OUT}=0. Find the energy dissipated in the transistor during the first 0→ 1 transition, **First $E_{0->1}$**.

E(diss) = E(supply)-E(stored) = $CL*VDD^2$ - ½*$CL*VDD^2$
First E0->1 = ½* CL * $(VDD)^2$ = $0.5*(10f)*(1.2)^2$ = 7.2fJ (6pt)

Then, after the output reaches its final value, a 1.2V to 0 step is applied to the input, followed by the second 0 to 1.2V step. Find the energy dissipated in the transistor in the first 1 → 0 transition, **First $E_{1->0}$**,and the second 0→ 1 transition, **Second $E_{0->1}$**. The load capacitor C_L is 10fF. (16 pts)

There is still remained Energy in the C_L because final V_{OUT} is 0.3V.
First E1->0 = E(supply)-E(remained)
= ½* CL * (VDD^2-VTP^2) =$0.5*(10f)*(1.2^2-0.3^2)$ =6.75fJ (5pt)

Second E0->1 = E(supply)-E(stored)
= CL*VDD*(VDD-VTP) - ½* CL * (VDD^2-VTP^2)
= ½* CL * (VDD^2-2*VDD*VTP+VTP^2)
= ½* CL * $(VDD-VTP)^2$ =$0.5*(10f)*(1.2-0.3)^2$ =4.05fJ (5pt)

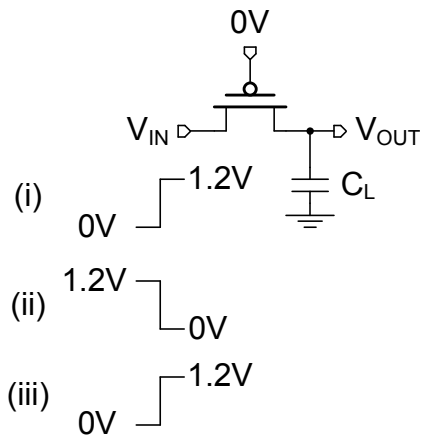

Fig.2 (c).

[PROBLEM 3] SIZING A CHAIN OF INVERTERS

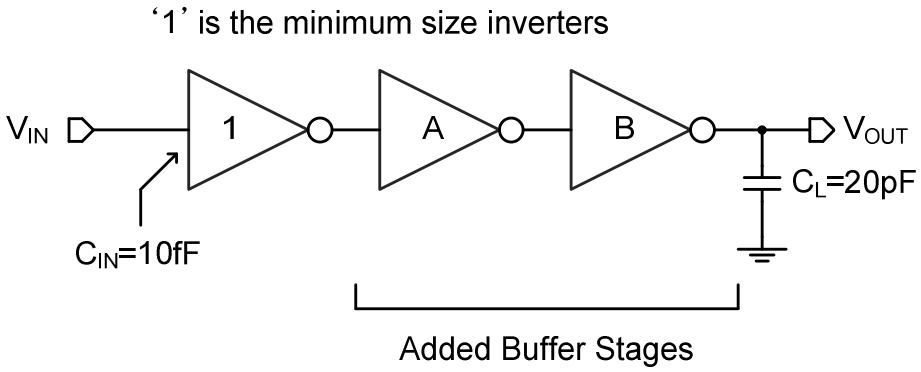

Fig.3. Buffer insertion for driving large loads.

(a) In order to drive a large capacitance (C_L=20pF) from a minimum size gate (with input capacitance C_{IN}=10fF), you decide to introduce a two-stage buffer as shown in Fig.3. Assume that the intrinsic propagation delay of a minimum size inverter, t_{inv}, is 70pS. Also assume that the input capacitance of a gate is proportional to its size, and there is no diffusion capacitance of inverter, γ=0. Determine the sizing of the two additional stages that will minimize the propagation delay. (5 pts)

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as f, f2, respectively.

$f = \sqrt[N]{F} = \sqrt[3]{2000} = 12.6$
$tp = N*tinv*(\gamma+f) = 3*70pS*(12.6) = 2646pS$

(b) If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case? Ignore polarity of output, V_{OUT}. (10 pts)

From the text, we know that the minimum delay occurs when f = e. Therefore,

N = ln(2000) / ln(e) = 7.6 -> N=7 or 8, both case are right for this question. However, N=7 is better choice since the delay difference is very small amount but power consumption difference is large. If polarity should be concerned, N=8 cannot be right choice.

(i) In case of N=7
f = exp(ln(2000)/7) = 2.96, so new tp = 7*70pS*2.96 = 1450pS

(ii) In case of N=8
f = exp(ln(2000)/8) = 2.58, so new tp = 8*70pS*2.58 = 1445pS

(c) Determine a closed form expression for the energy consumption in the circuit of Fig.3 with 3-stage inverter chain. Consider gate capacitances and C_L only in your analysis. What is the energy consumption for a supply voltage of 1.2V? Assume that the activity factor, α, is 1, i.e. there are 0->1 transition and 1->0 transition at every cycle. (10 pts)

The energy consumption is determined as follows

If α=1 then there are 0->1 transition and 1->0 transition at every cycle.

i) Including CIN

$Ec = CtotVDD^2 = (CIN+CA+CB+CL)*VDD^2 = (\ CIN * (1+f+f2) + CL)*VDD^2$

$= (10fF*(1+12.6+12.6^2) + 20pF) * 1.2^2 = 31.28pJ$

ii) excluding CIN

$Ec = CtotVDD^2 = (CA+CB+CL)*VDD^2 = (\ CIN * (f+f2) + CL)*VDD^2$

$= (10fF*(12.6+12.6^2) + 20pF) * 1.2^2 = 31.27pJ$

Both i) & ii) are right. Actually there is no big difference.

(d) Describe the advantages and disadvantages of the methods shown in (a) and (b). (5 pts)

Solution (b) is faster but it consumes much more area and power than (a).