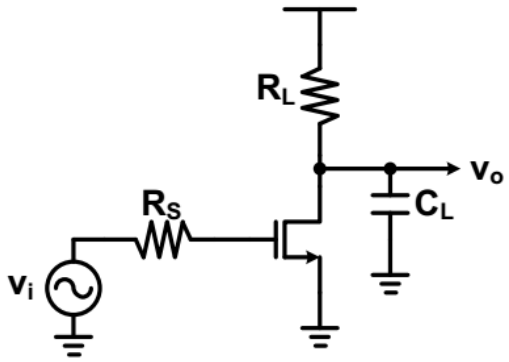
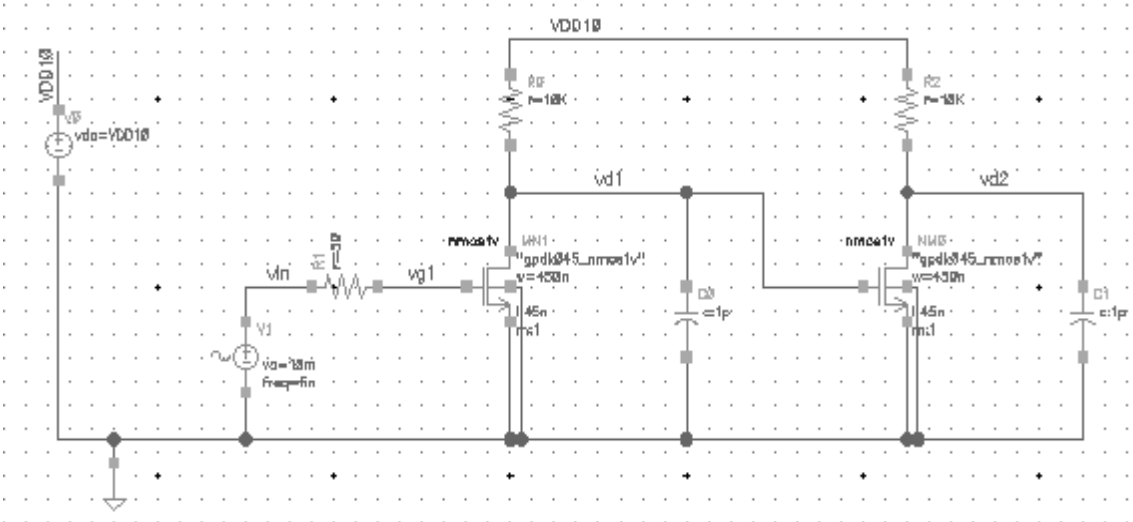
EE223 Homework #2 Sep. 17, 2018
Due: Oct. 1, 2018 6PM
Homework will not be received after due.

1. (**20 points**) MOS Small-Signal Analysis on Common Source Amplifier
   a) Draw the small-signal model for the Common Source amplifier circuit below, including the necessary capacitors. For the MOSFET, assume it is in the saturation region, infinite output impedance, and consider only capacitor C_{gs} (i.e. neglect C_{gd}, etc). **(5 points)**
   b) Derive the small-signal transfer function, $v_o(s)/v_i(s)$. This should be given as a function of g_m, C_{gs}, R_s, R_L, and C_L. Use s-domain expression for the impedance of capacitance, i.e., $1/sC_{gs}$. **(5 points)**
   c) Give expressions for the DC gain and the amplifier's poles and zeros (if any) **(5 points)**
   d) Sketch the Bode plot (magnitude only) of the amplifier's transfer function vs frequency. Label key slopes and give the location of any poles and/or zeros. Assume $R_LC_L >> R_SC_{gs}$. **(5 points)**



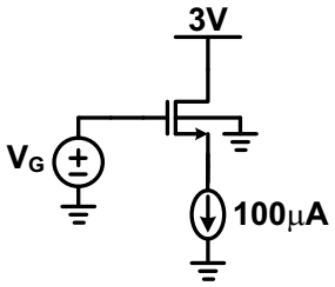
2. (**30 points**) Cadence Spectre Simulation of Common-Source Amplifiers
   Draw a schematic shown below using nmos1v with W/L=450n/45n, 10 Kohm ideal resistors ("res" from analogLib), 1 pF capacitors ("cap" from analogLib), vsin for input sinewave voltage source, and VDD10=1.0V.
   a) Run a DC simulation in ADE-L by sweeping Vin from 0.2V to 1V in 10mV step. Make plots for Id vs. Vg1, Vd1 vs Vg1, and gm vs. Vg1 for MN1. For gm, use deriv function in Calculator.



   b) Calculate small-signal voltage gain of MN1 at Vin=0.7V. Use DC operating point results for gm, gds, etc.

c) Run an AC simulation of the circuit and make Gain vs. Frequency plot from 1KHz to 1GHz.
d) Compare the DC gain from c) with the calculated gain from b) to check if the simulation agrees with the calculation. Explain the reason for the discrepancy if there is any.
e) Run a transient simulation by applying an input voltage of 1MHz sinwave with 10mV amplitude for 5usec. Plot the waveforms for Vin, Vd1, and Vd2 and calculate the gain of each stage by measuring the amplitude of the transient signals at each stage. Compare the result with the result from the AC simulation in c)
f) Run a Pole/Zero simulation of the circuit to find out the pole frequency of the stage and compare the value obtained from the simulation with the calculated pole frequency of MN1 using the expression derived in Problem#1c). Explain if there is any discrepancy.

3. **(20 points)** Body Effect on Threshold Voltage
For the circuit below, what is the value of V_G that causes the V_T of the transistor to increase to 0.6V? Assume the transistor is in saturation and that V_{T0}=0.5V, γ=0.4$V_{1/2}$, $2\Phi_F$=0.9V, μC_{ox}=130µA/V^2, (W/L)=(2µ/200n).



4. **(30 points)** Layout & Transistor Capacitors
For the following layout, assume C_{ox} = 7fF/um2, C_{ov} = 1fF/um, C_j = 1fF/um2, C_{jsw} = 0.01fF/um, C_{cb} = 1fF/um2). The dimensions are given in λ units, where λ=0.5µm. Assume all poly gates have L=1µm and L_D=0.05µm.
a) Draw the equivalent circuit. **Combine all parallel transistors. (15 points)**
b) Assume that V_O=0.5V, V_X=0.4V, V_Y=0V, V_{G1}=1V, V_{G2}=1.5V. Also, assume that the p-substrate is grounded, V_{T0}=0.7V, and γ=0. What region are the transistors operating in? **(5 points)**
c) Calculate the total gate capacitance of the transistors. **(5 points)**
d) Calculate the total junction capacitance at nodes O, X, and Y. Note for the perimeter terms **(5 points)**