EE230-02 RFIC II
Fall 2018

Lecture 22: Power Amplifier

Prof. Sang-Soo Lee
sang-soo.lee@sjsu.edu
ENG-259

Schedule

- **No class on Thursday, Dec. 6 - IEDM conference**
- **Project Report Due: Dec. 10**
- **Final Exam: Dec. 14, Friday 2:45 PM**

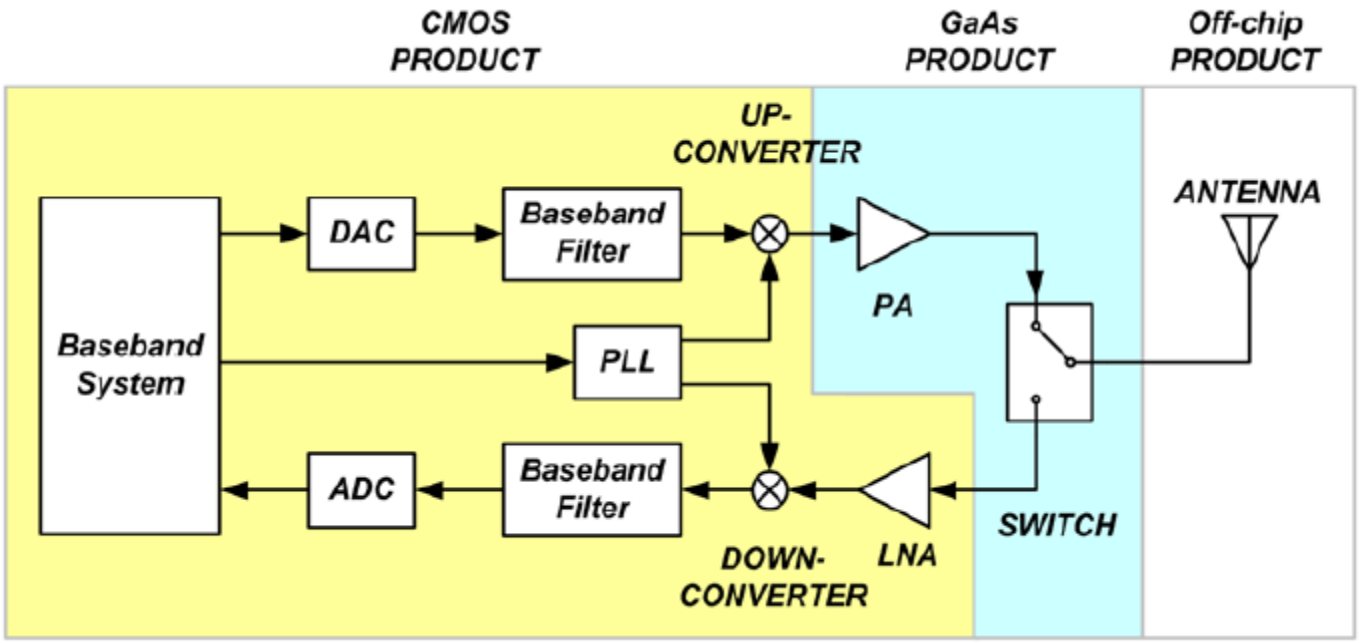
  One-page Aid sheet on Front side only

  Bring a Calculator

Final Exam Topic

- **Matching Network**
- **LNA and Noise**
- **VCO**
- **PLL**
- **PA**
- **Misc. questions**

Block Diagram of Direct Conversion System



Power Amplifier Performance Metrics

- Metrics defined in standards
  - Output Power
  - Spectral Mask
  - ACPR (Adjacent Channel Power Ratio)
  - Signal Modulation

- Metrics not defined in standards
  - PAE (Power Added Efficiency)
  - Drain Efficiency
  - Power Gain
  - IP3
  - P1dB

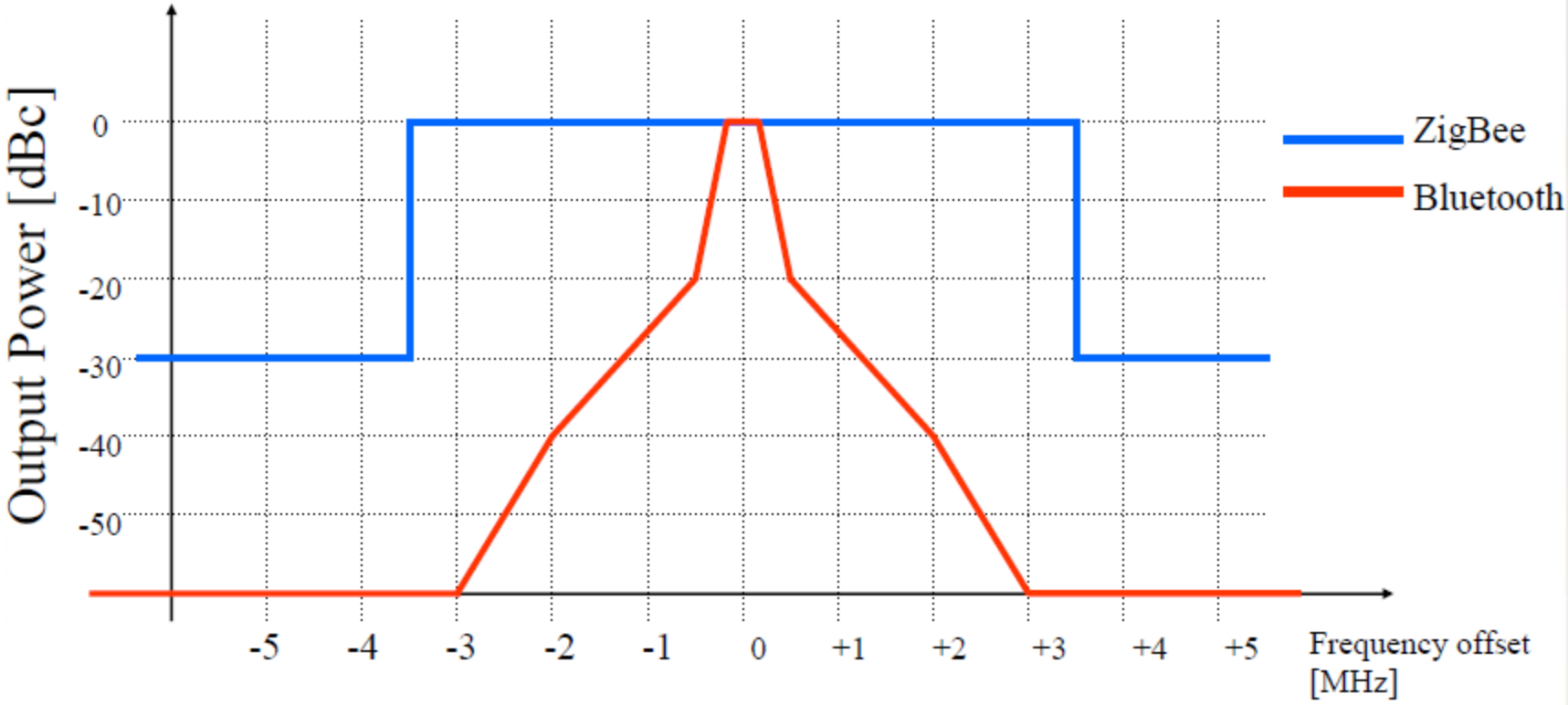
Output Power

- Maximum output power varies drastically among different standards

Standard	Modulation	Max. P_{out}
AMPS	FM	31 dBm
GSM	GMSK	36 dBm
CDMA	O-QPSK	28 dBm
DECT	GFSK	27 dBm
PDC	π/4 DQPSK	30 dBm
Bluetooth	FSK	16 dBm
802.11a	OFDM	14-19 dBm
802.11b	PSK-CCK	16-20 dBm

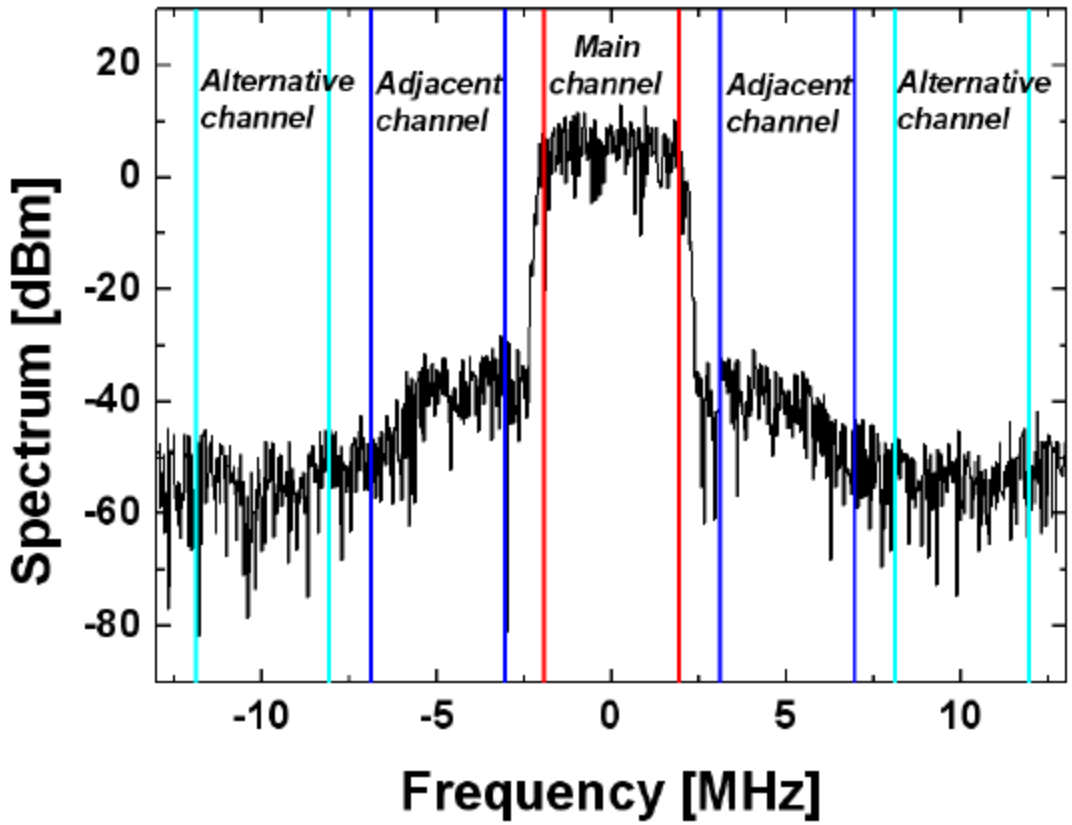
Spectral Mask

- Power mask is an indication of how much spectrum regrowth is allowed

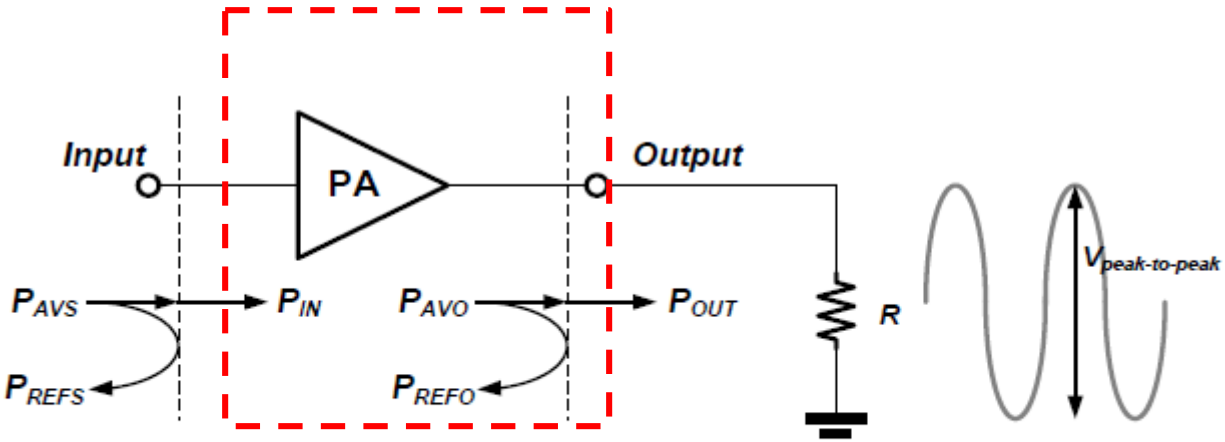


ACPR

$$ACLR\ (\text{dBc}) \equiv 10 \log \left(\frac{\text{Power in Adjacent or Alternative Channel in Watt}}{\text{Power in Main Channel in Watt}} \right)$$



Definition of Power and Gain



Transducer Gain (G_T) = P_{OUT} / P_{AVS}
Power Gain (G_P) = P_{OUT} / P_{IN}
Available Gain (G_A) = P_{AVO} / P_{AVS}

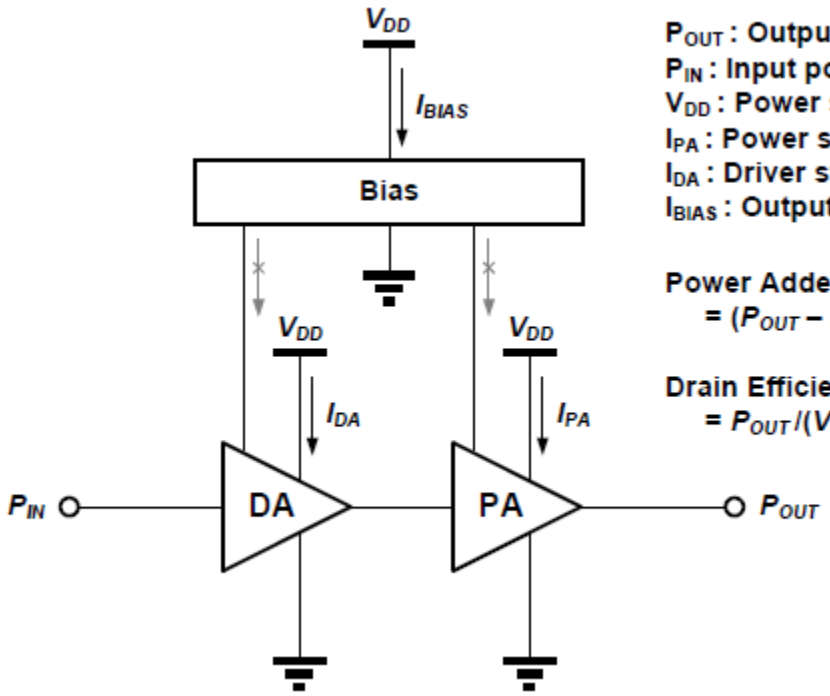
$$P_{OUT} = \frac{\left(\frac{V_{\text{peak-to-peak}}}{2}\right)^2}{2 \cdot R}$$

$$\text{Transducer Gain } (G_T) = \frac{P_{OUT}}{P_{AVS}},$$

$$\text{Power Gain } (G_P) = \frac{P_{OUT}}{P_{IN}} = G_T\left(1 + \frac{P_{REFS}}{P_{IN}}\right),$$

$$\text{Available Gain } (G_A) = \frac{P_{AVO}}{P_{AVS}} = G_T\left(1 + \frac{P_{REFO}}{P_{OUT}}\right)$$

Efficiency of PA



P_{OUT} : Output power
P_{IN} : Input power
V_{DD} : Power supply voltage
I_{PA} : Power stage current
I_{DA} : Driver stage current
I_{BIAS} : Output power

Power Added Efficiency (*PAE*)
$= (P_{OUT} - P_{IN})/(V_{DD} \times (I_{PA} + I_{DA} + I_{BIAS})) \times 100[\%]$

Drain Efficiency (η)
$= P_{OUT}/(V_{DD} \times I_{PA}) \times 100[\%]$

Drain Efficiency

$$\eta(DE) = \frac{P_{OUT}}{P_{DC}} = \frac{P_{OUT}}{P_{DC} \cdot I_{PA}}$$

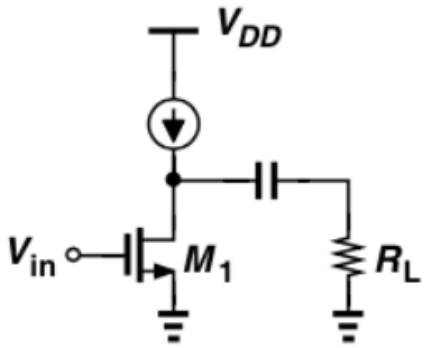
Power Added Efficiency

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}$$

Output Power and Voltage Swing

- Ex: 1 W (30 dBm) into a resistive 50 Ω load (e.g. antenna).

$$P = \frac{V_p^2}{2R_L}$$



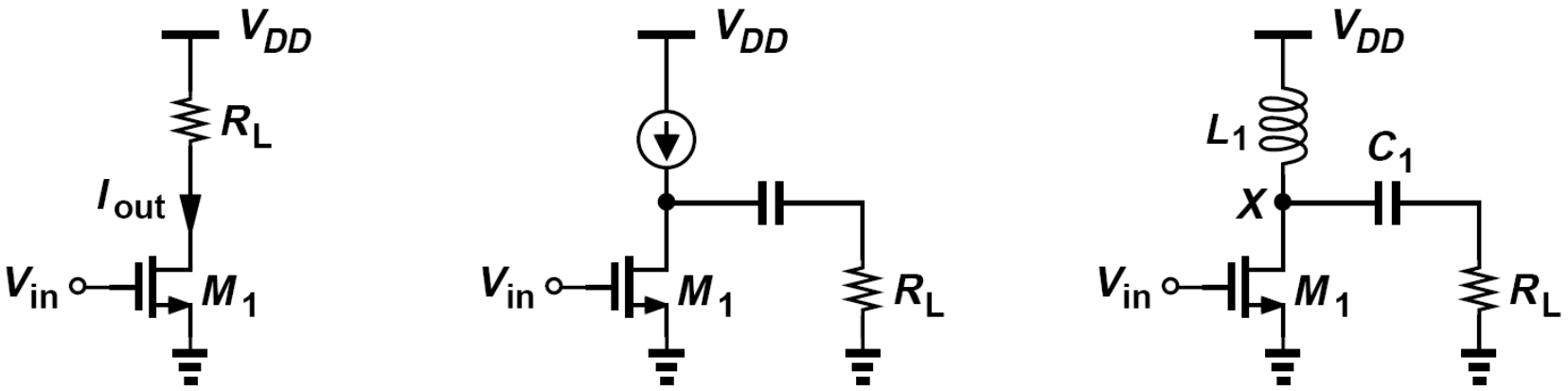
=> 10 V_p, I_p = 200 mA.

- How can we achieve this with nm-CMOS?

=> Impedance transformation: lower voltage, more current

- For high-power PAs: as high supply voltage as possible, and impedance transformation.

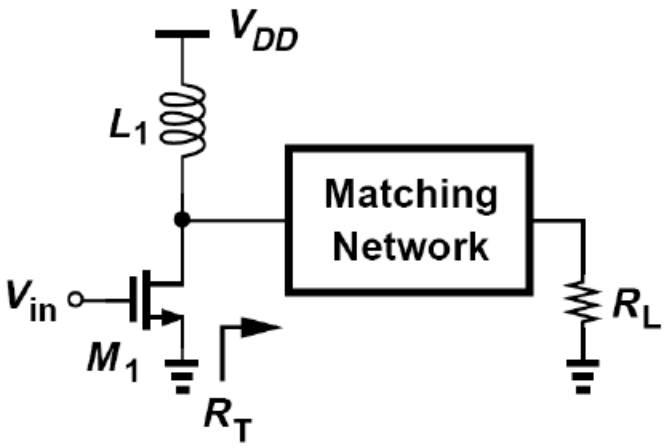
Output Power and Voltage Swing

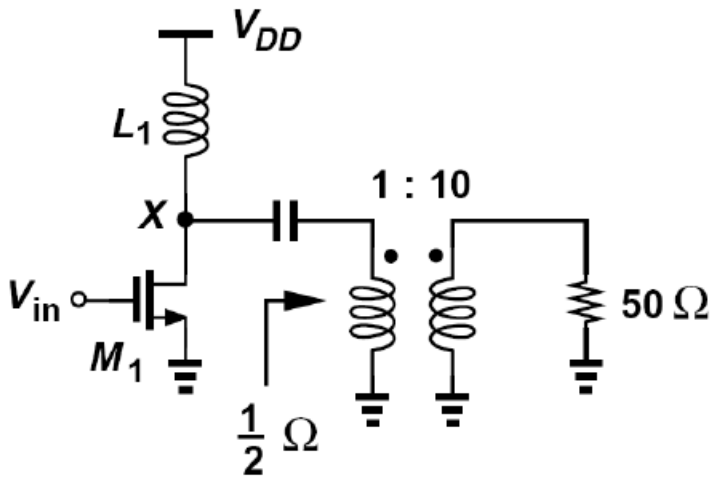


- For a common-source (or common-emitter) stage to drive the load directly, a supply voltage greater than V_{pp} is required.
- If the load is realized as an inductor, the drain ac voltage exceeds V_{DD}, even reaching $2V_{DD}$ (or higher). But the maximum drain-source voltage experienced by M_1 is still at least 20 V if the stage must deliver 1 W to a 50-Ω load.

Matching Network

- In order to reduce the peak voltage experienced by the output transistor, a matching network is interposed between the PA and the load. This network transforms the load resistance to a lower value, R_T, so that smaller voltage swings still deliver the required power.





Linear PA Classes

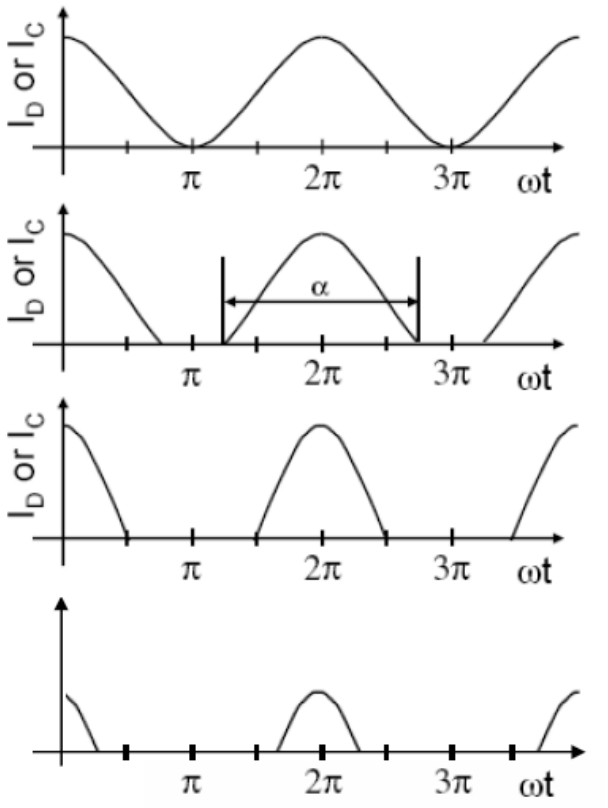
Conduction Angle:

Class A: $\alpha = 2\pi$

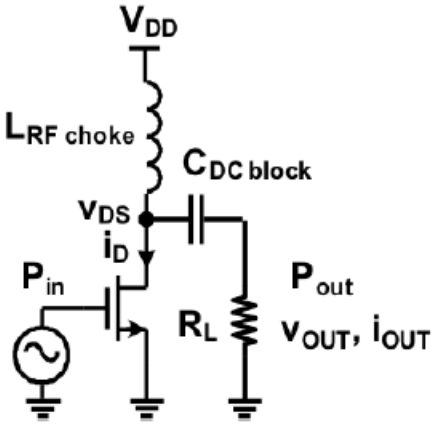
Class AB: $\pi < \alpha < 2\pi$

Class B: $\alpha = \pi$

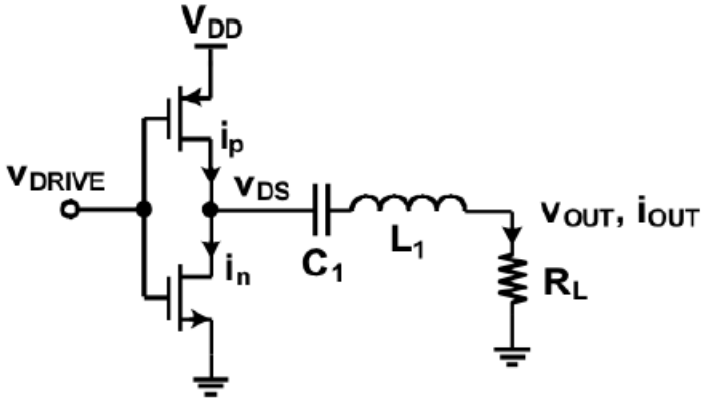
Class C: $\alpha < \pi$



PA Classes

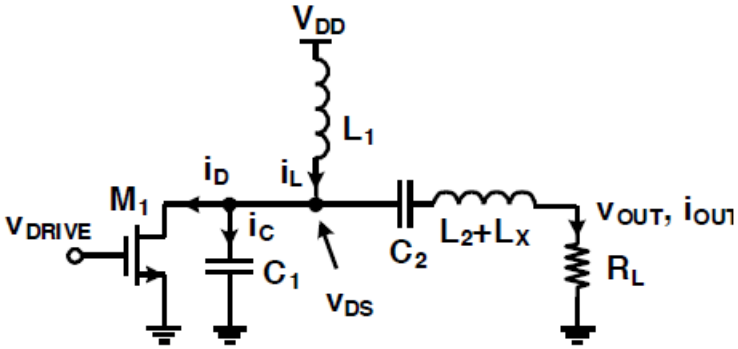


class-A/AB/B/C (linear)

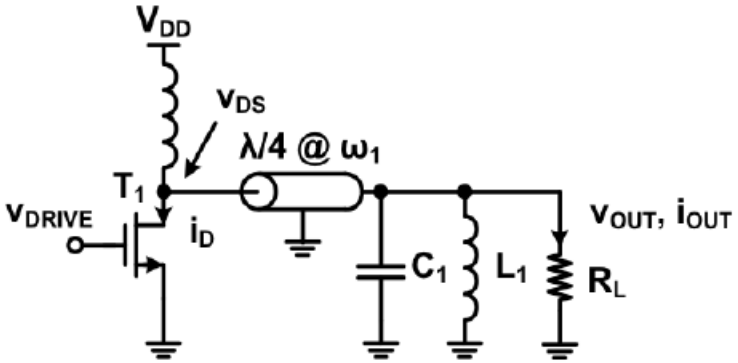


inverter-based class-D (switched)

class-E (switched)

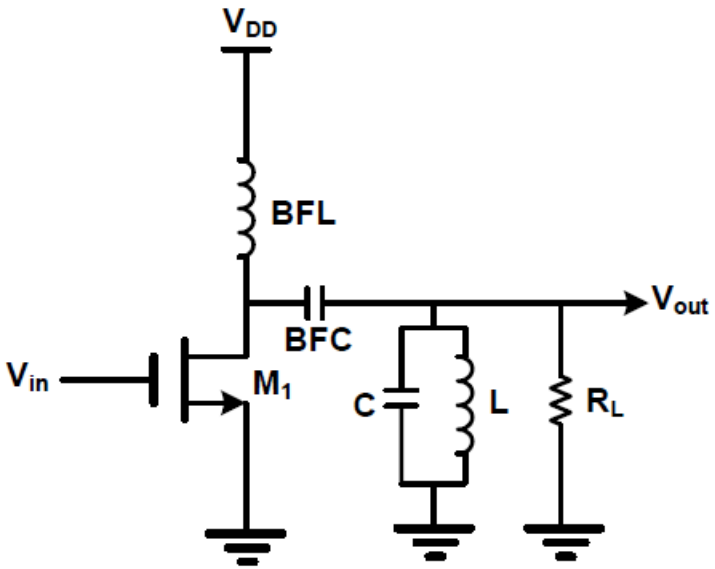


class-F (switched)



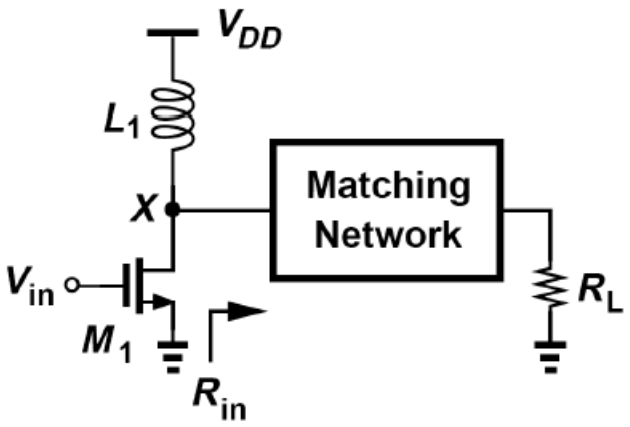
Linear PA Classes – A,B,C

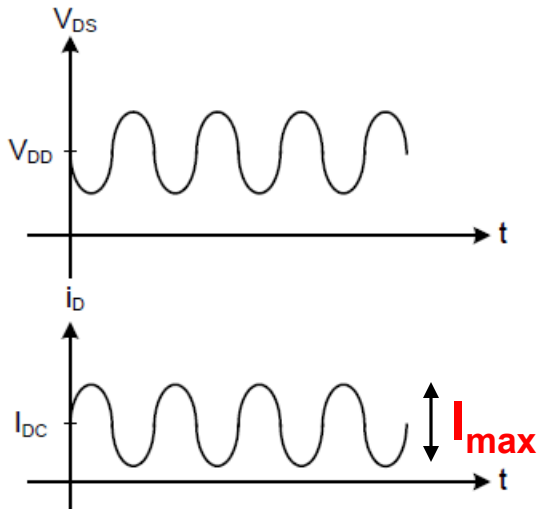
- Output power delivered to R_L.
- A “big fat” inductor (BFL) feeds DC power to the drain. It is big enough to create a constant current.
- BFC prevents DC dissipation in the load.
- The tank absorbs the parasitics of the transistor.
- LC tank filters out of band emissions created by non-linearities in the transistor.
- Different gate-biases => linear class A, AB, B, C.



Class A

- Since BFL presents a DC short, the drain voltage (which is the sum of DC and the signal voltage) has a symmetrical swing around V_{DD}.
- The drain voltage and current has a 180° phase difference.
- The product of drain current and voltage is positive; the transistor always dissipates power.



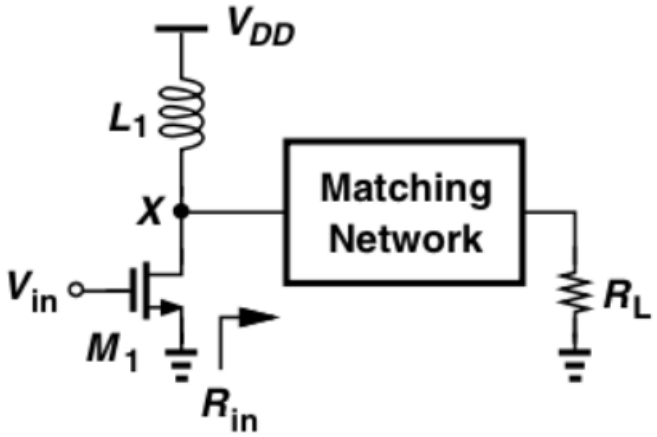


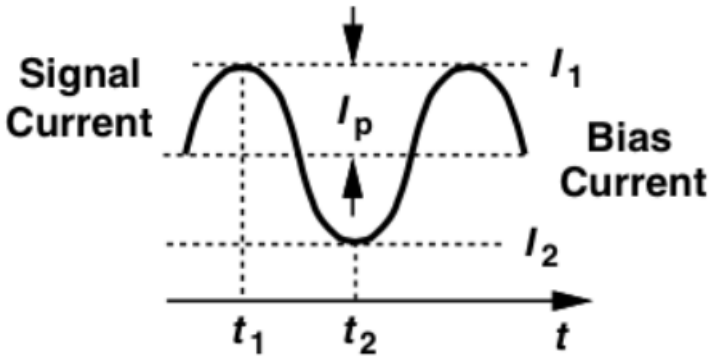
Class A

- Device biased to ~ $I_{max}/2$ to never switch off.
- Good linearity.
- Efficiency <= 50 %.
- V_x swings up to 2 x V_{DD} and the peak drain current is $2V_{DD}/R_L$. The device must be able to manage this stress!

$$\frac{I_{max}}{2} = \frac{V_{DD}}{R_L}$$

$$\eta = \frac{V_{DD}^2/(2R_{in})}{V_{DD}^2/R_{in}} = 50\%.$$





Efficiency of Class-A

$$\eta = \frac{P_1}{P_{dc}} = \frac{I_{1,rms} \cdot V_{1,rms}}{I_{dc} \cdot V_{dc}}$$

Class A:

$$\begin{cases} I_1 = \dfrac{I_{MAX}}{2}, \quad I_{dc} = \dfrac{I_{MAX}}{2} \\ \eta = \dfrac{\left(\dfrac{I_{MAX}/2}{\sqrt{2}}\right)\left(\dfrac{V_{DD}}{\sqrt{2}}\right)}{\left(\dfrac{I_{MAX}}{2}\right) \cdot V_{DD}} = 50\% \text{ max.} \end{cases}$$

Efficiency of Class-B

Class B:

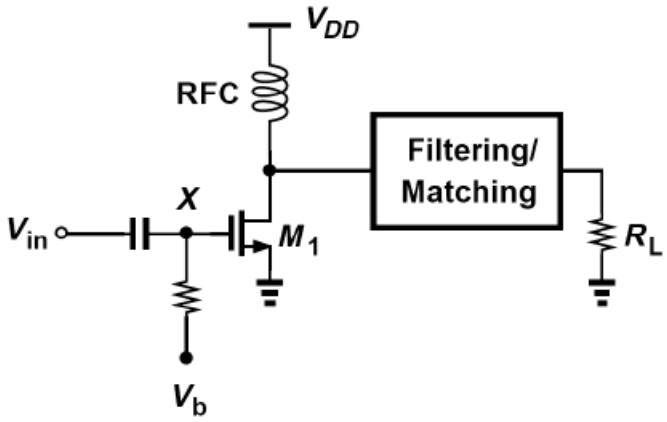
$$\begin{cases} I_1 = \dfrac{I_{MAX}}{2}, \quad I_{dc} = \dfrac{I_{MAX}}{\pi} \\ \eta = \dfrac{\left(\dfrac{I_{MAX}/2}{\sqrt{2}}\right)\left(\dfrac{V_{DD}}{\sqrt{2}}\right)}{\left(\dfrac{I_{MAX}}{\pi}\right).V_{DD}} = 78\% \text{ max.} \end{cases}$$

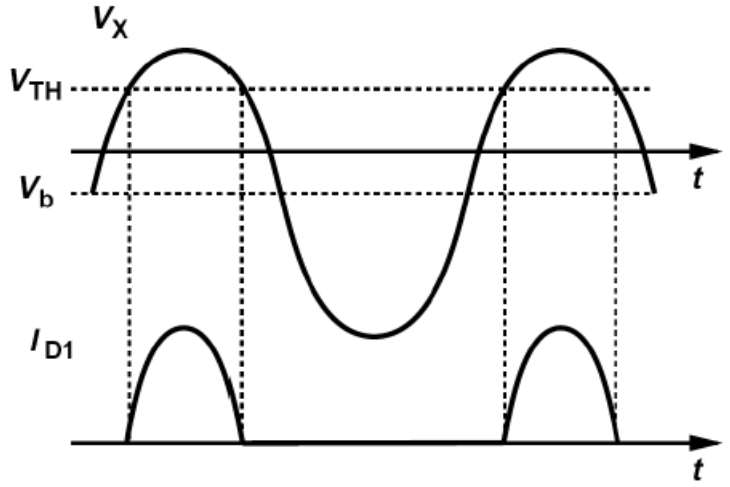
Class AB

- In a class A amplifier, the device conducts 100 % of the time, and in a class B, it conducts 50 % of the time.
- A class AB amplifier is something in-between; the device conducts between 50 % and 100% of the time.
- The efficiency and the linearity are intermediate between a class A and class B amplifier.
- Due to these trade-offs, class AB power amplifiers are popular in many applications.

Class C

- In a class C power amplifier, the time in which the transistor conducts is decreased to less than half period.
- The drain current consists of a periodic train of pulses, which can be approximated by the top pieces of a sine wave





Output Voltage Shape

- If load tank filters out all harmonics, output voltage is pure sinusoidal even when there is current discontinuity