EE141-Spring 2010 Digital Integrated Circuits

Lecture 18
Registers

Administrativia

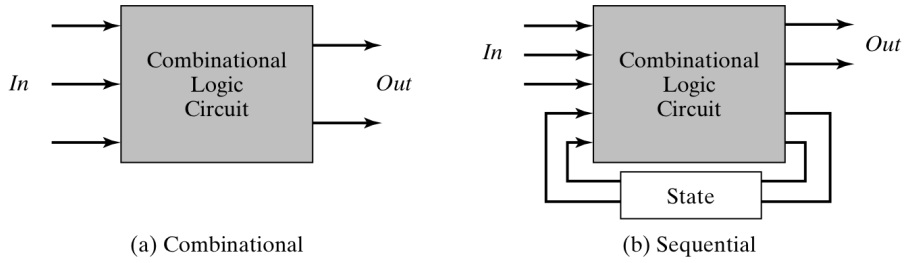
- Project Phase 2 now on the web-site.
- Hw 6 due today.
- New homework to be posted in a week.
- Cory Hall closed on Monday (Power Outage)
  - Instructional computers in 353 Cory should come back on line on Tu.
- Enjoy Spring Break!

Class Material

- Last lecture
  - Domino Logic
  - Introduction to registers
- Today's lecture
  - Registers
  - Timing
- Reading (Ch 7)

Sequential Logic

Combinational vs. Sequential Logic

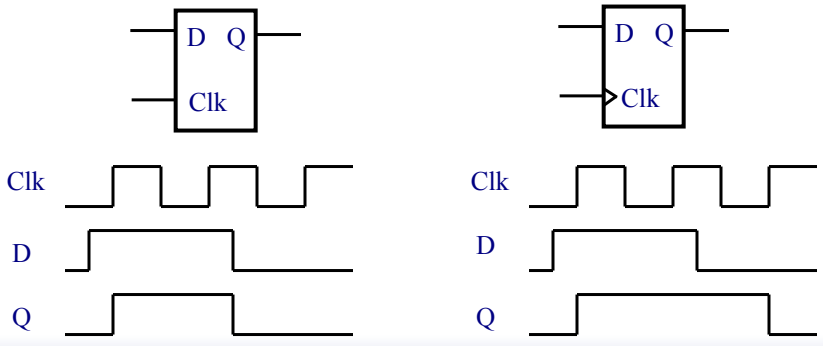


(a) Combinational (b) Sequential

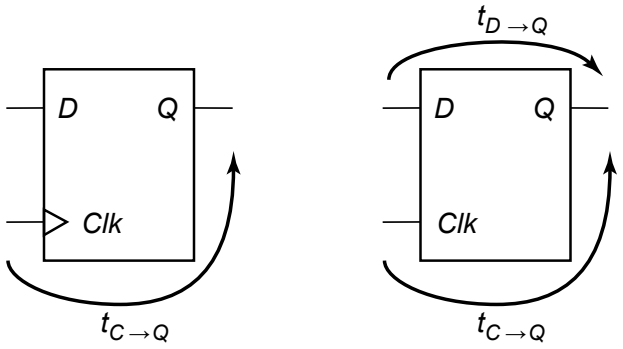
Output = *f*(*In*) **Output = *f*(*In, Previous In*)**

Latch versus Register (Flip-flop)

- Latch: level-sensitive
  clock is low - hold mode
  clock is high - transparent
- Register: edge-triggered
  stores data when
  clock rises

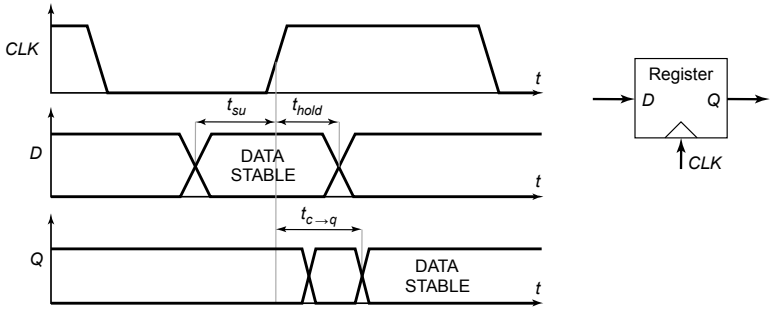


Characterizing Timing



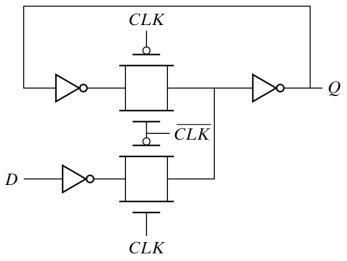
Register Latch

Timing Definitions – Set-up and Hold

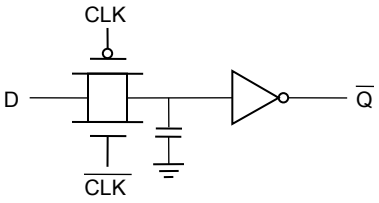


Storage Mechanisms

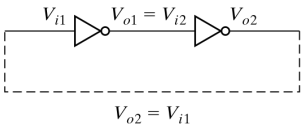
Static



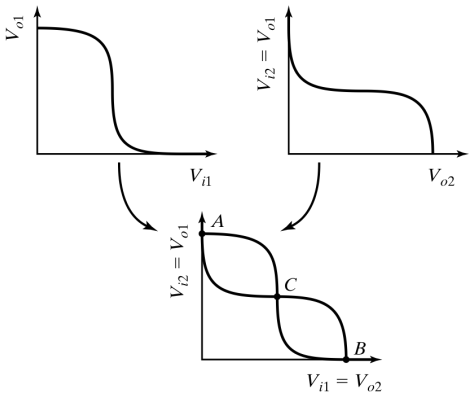
Dynamic



Positive Feedback: Bi-Stability

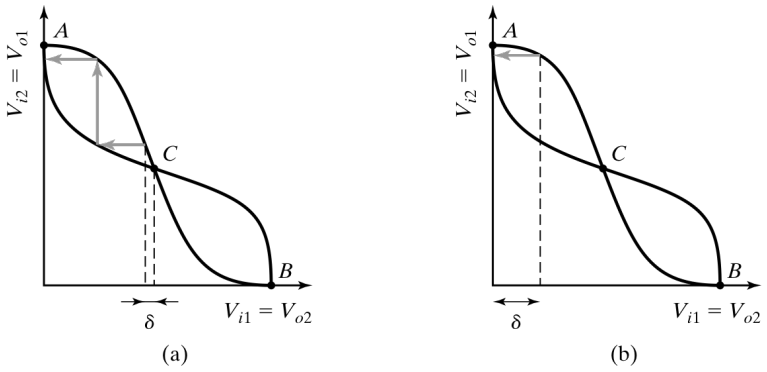


(a)



(b)

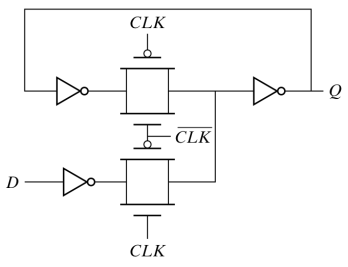
Meta-Stability



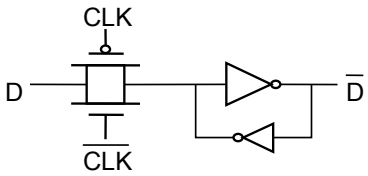
Gain should be larger than 1 in the transition region

Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

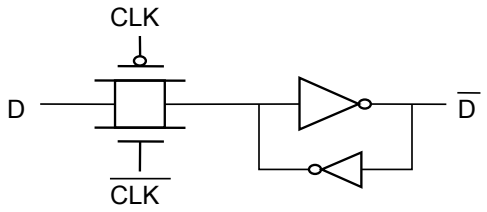


Converting into a MUX



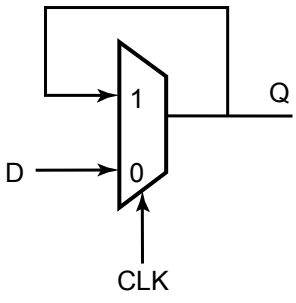
Forcing the state
(can implement as NMOS-only)

Pseudo-Static Latch



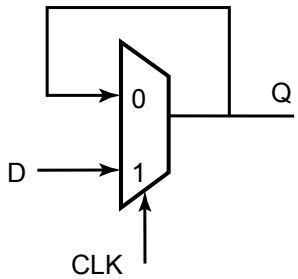
Mux-Based Latches

Negative latch
(transparent when CLK= 0)



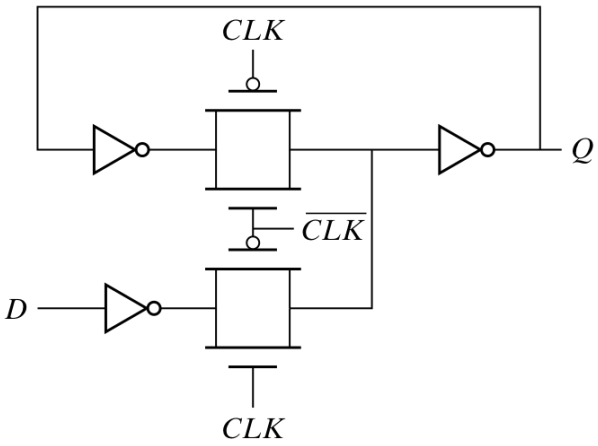
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

Positive latch
(transparent when CLK= 1)

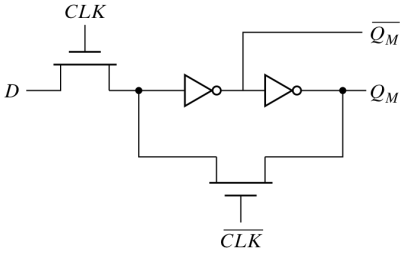


$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

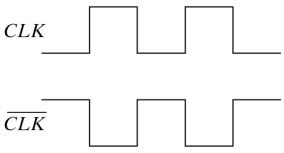
Mux-Based Latch



Mux-Based Latch



(a) Schematic diagram



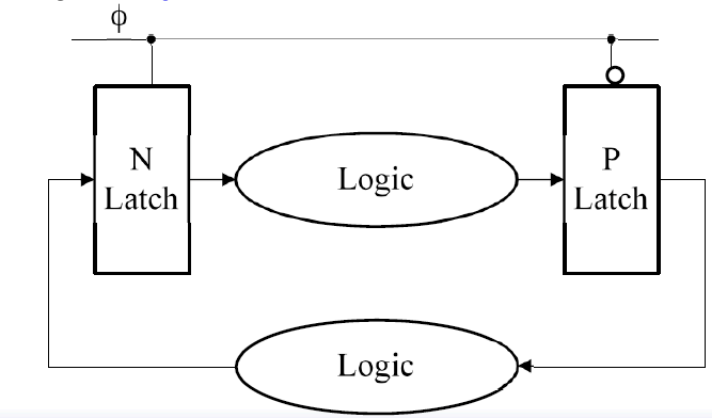
(b) Non overlapping clocks

NMOS only

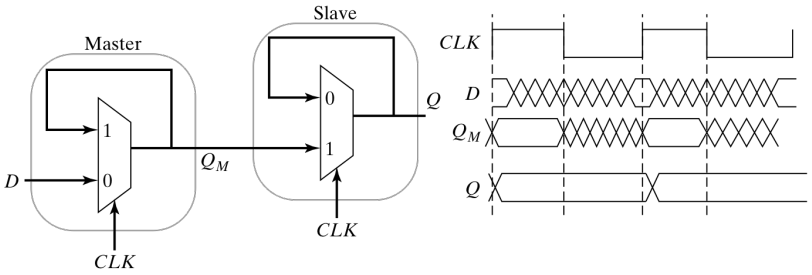
Non-overlapping clocks

Latch-Based Design

- N latch is transparent when $\Phi = 0$
- P latch is transparent when $\Phi = 1$



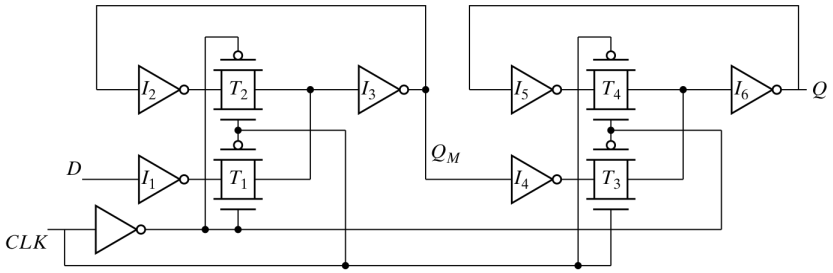
Master-Slave (Edge-Triggered) Register



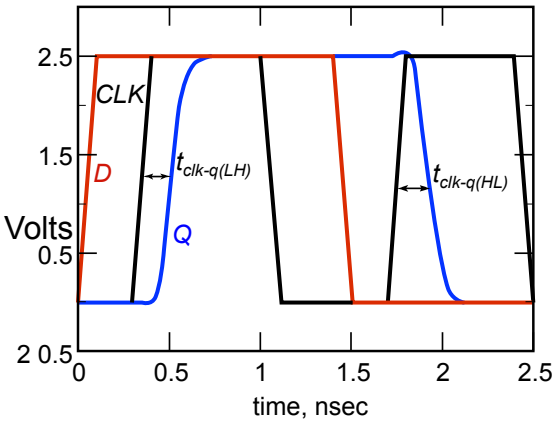
Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

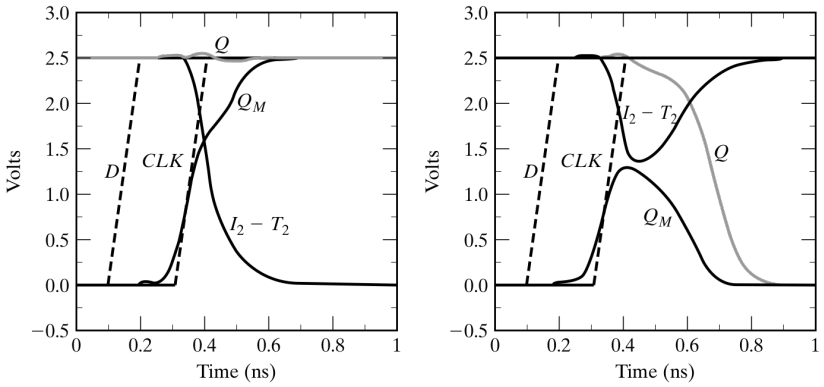
Multiplexer-based latch pair



Clk-Q Delay

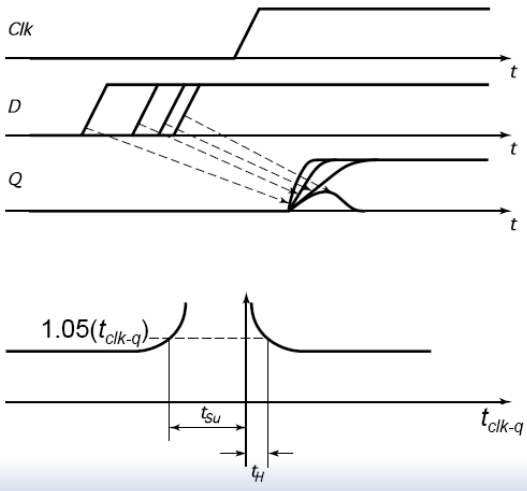


Setup Time



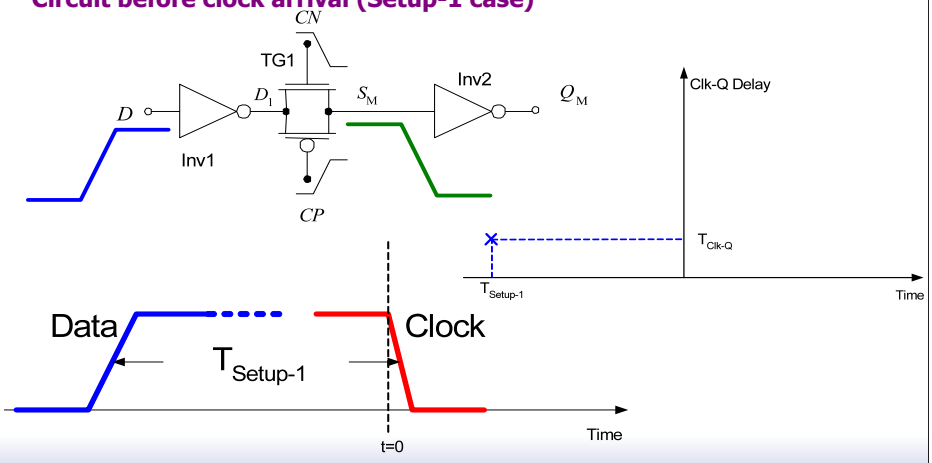
(a) T_{setup} = 0.21 ns (b) T_{setup} = 0.20 ns

More Precise Setup Time



Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



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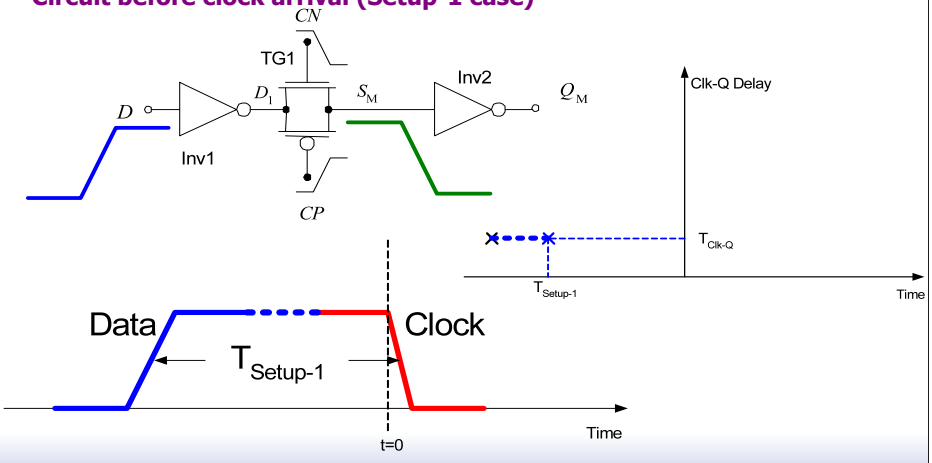

Setup-Hold Time Illustrations

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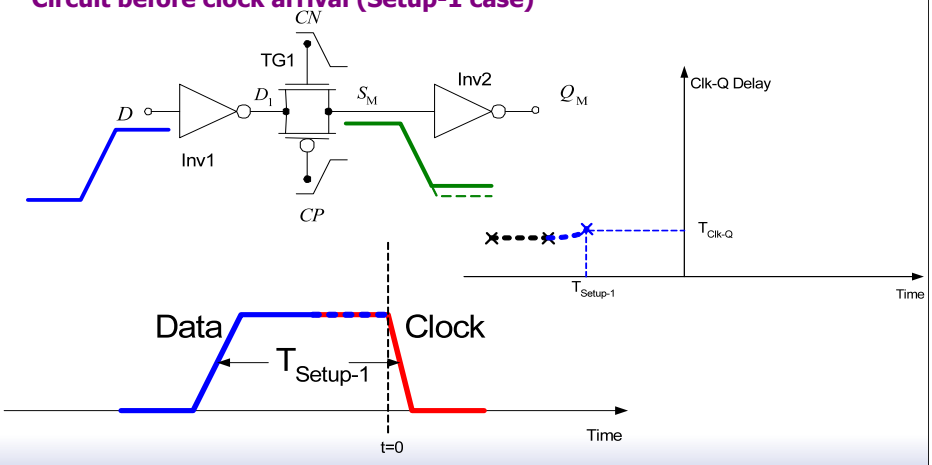
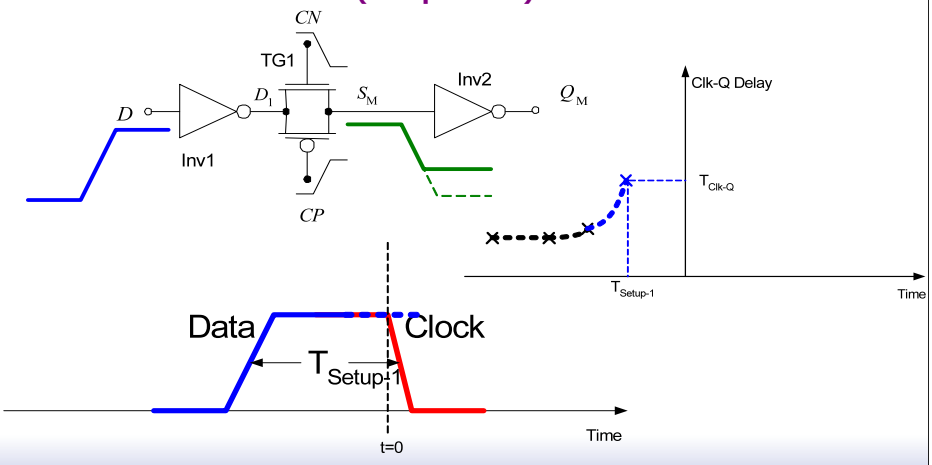


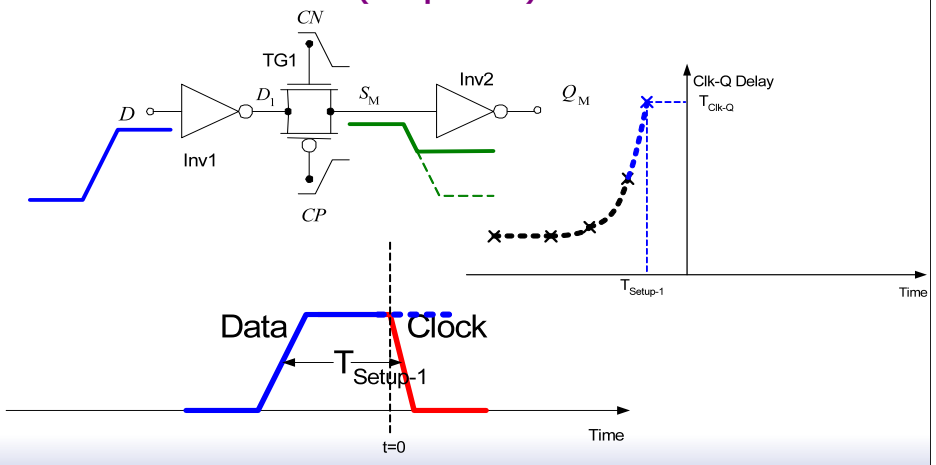
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



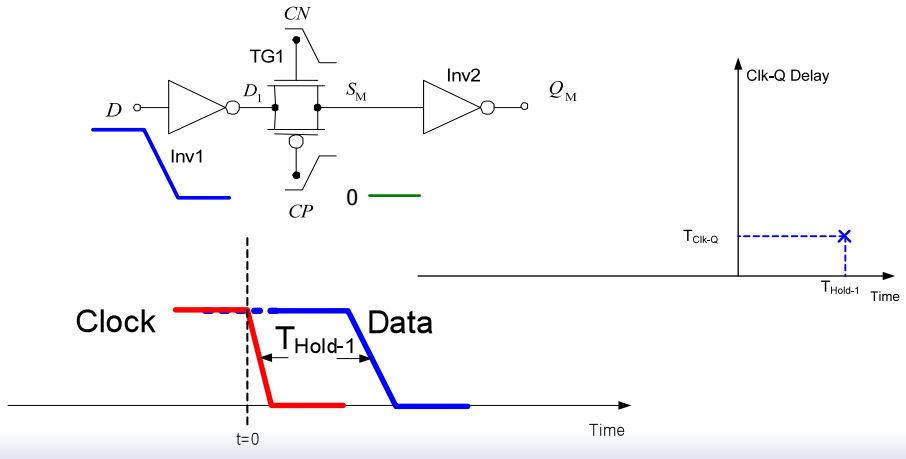
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



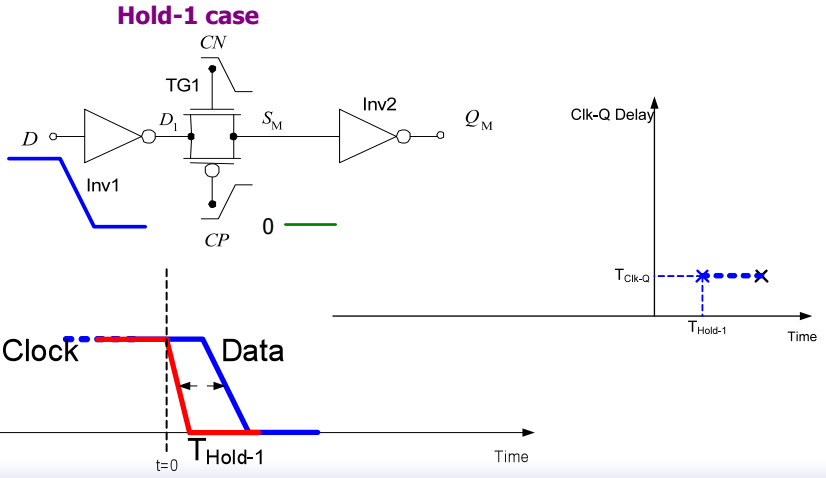
Setup-Hold Time Illustrations

Hold-1 case



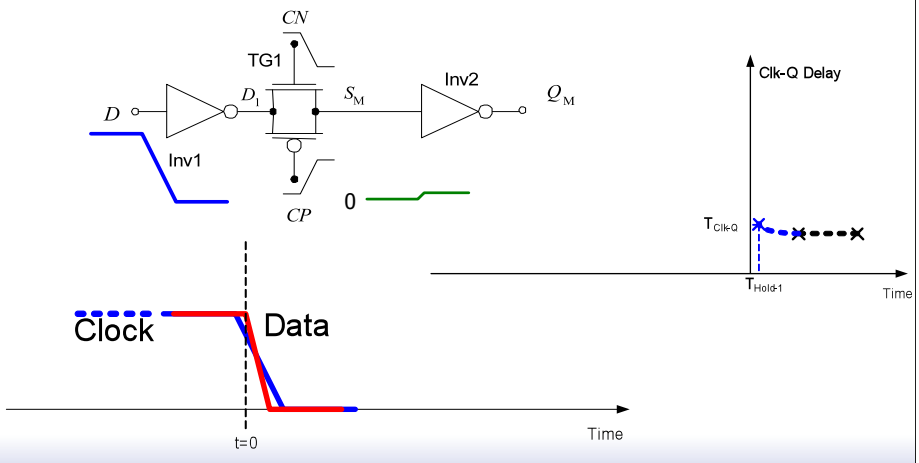
Setup-Hold Time Illustrations

Hold-1 case

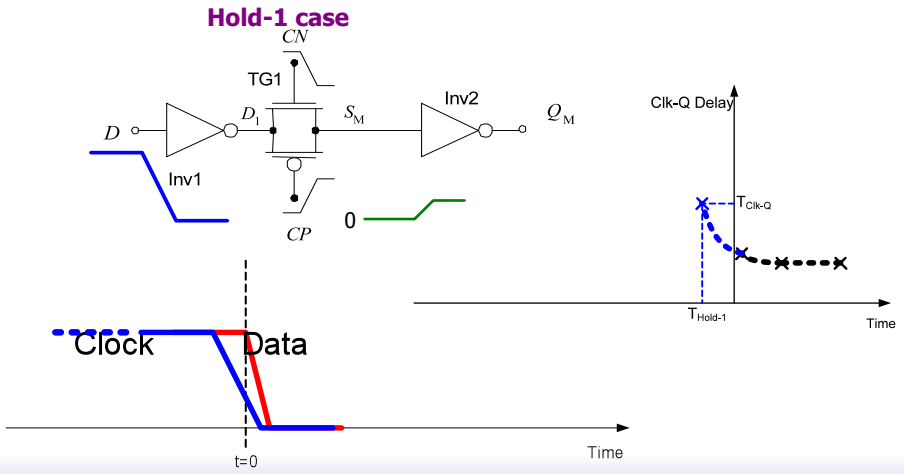


Setup-Hold Time Illustrations

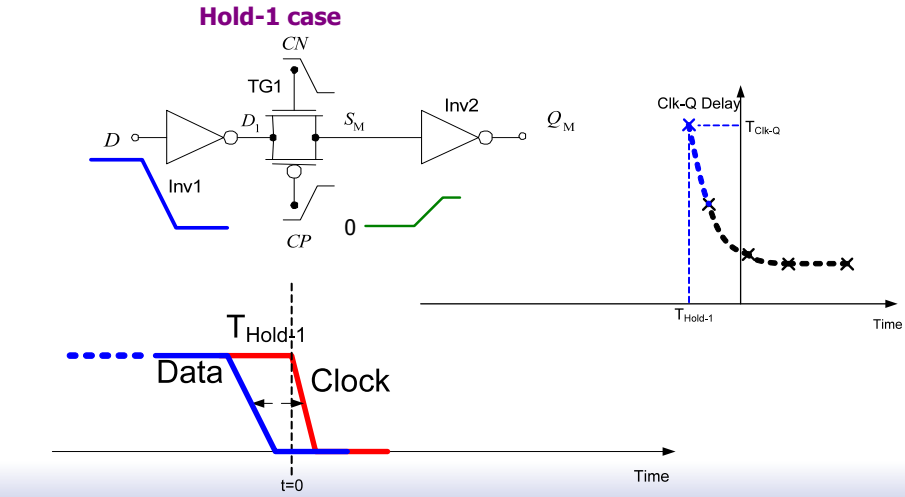
Hold-1 case



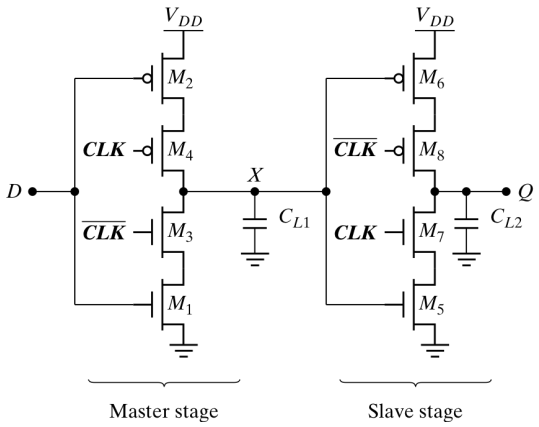
Setup-Hold Time Illustrations



Setup-Hold Time Illustrations

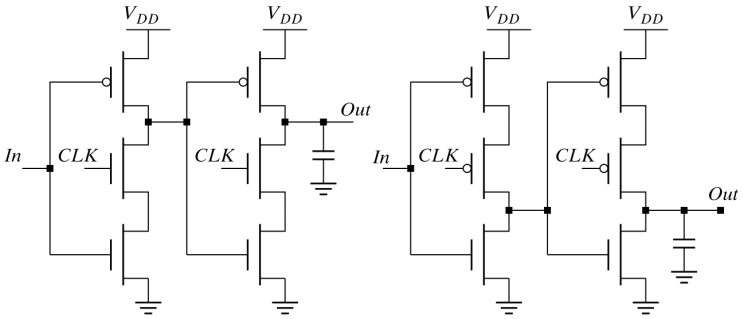


Other Latches/Registers: C²MOS



Keepers can be added to "staticize (?!)"

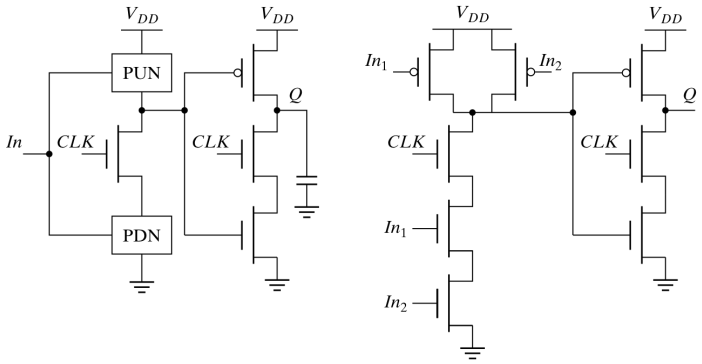
Other Latches/Registers: TSPC



Positive latch
(transparent when CLK= 1)

Negative latch
(transparent when CLK= 0)

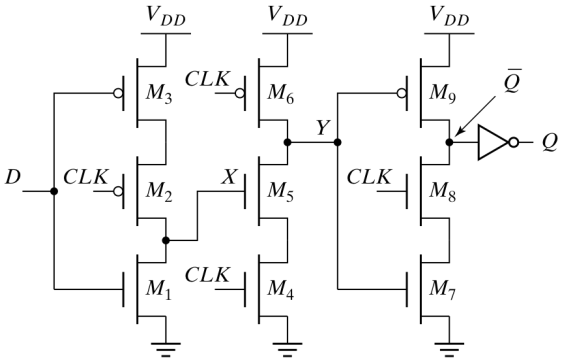
Including Logic in TSPC



Example: logic inside the latch

AND latch

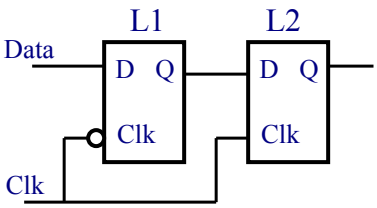
TSPC Register



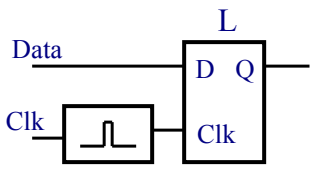
Pulse-Triggered Latches

Ways to design an edge-triggered sequential cell:

Master-Slave Latches



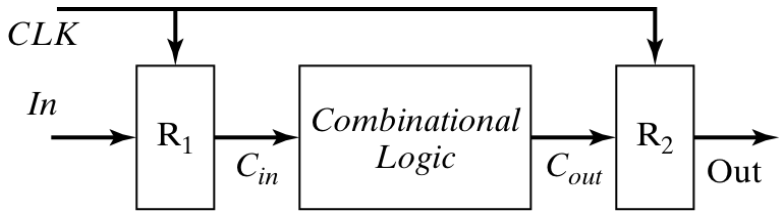
Pulse-Triggered Latch



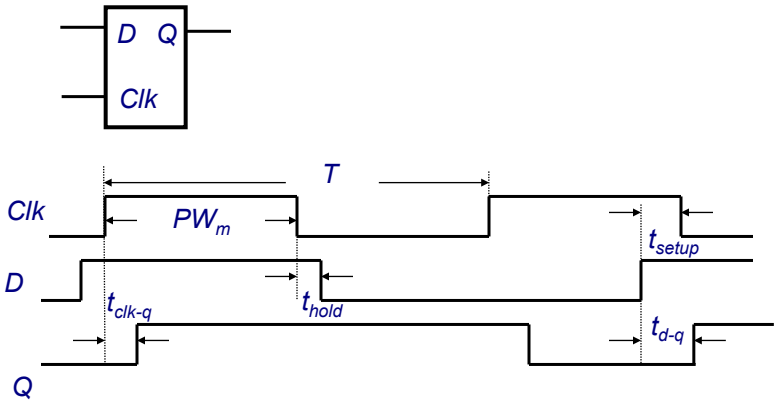
Why not route the pulse?

Timing

Synchronous Timing

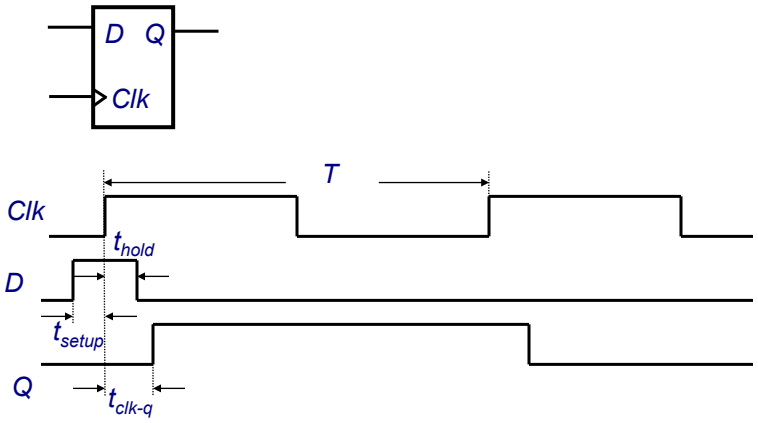


Latch Parameters



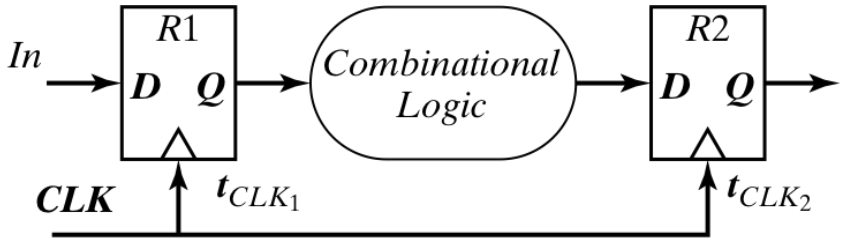
Delays can be different for rising and falling data transitions

Register Parameters



Delays can be different for rising and falling data transitions

Timing Constraints



$t_{clk\text{-}q}$
$t_{clk\text{-}q,min}$
t_{setup}, t_{hold}

t_{logic}
$t_{logic,min}$

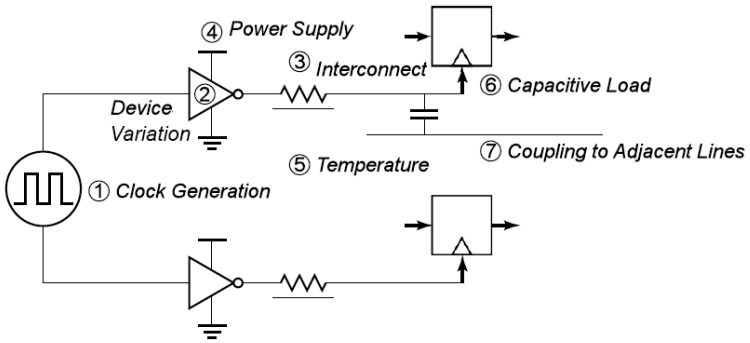
Cycle time (max): $T_{Clk} > t_{clk\text{-}q} + t_{logic} + t_{setup}$

Race margin (min): $t_{hold} < t_{clk\text{-}q,min} + t_{logic,min}$

Clock Nonidealities

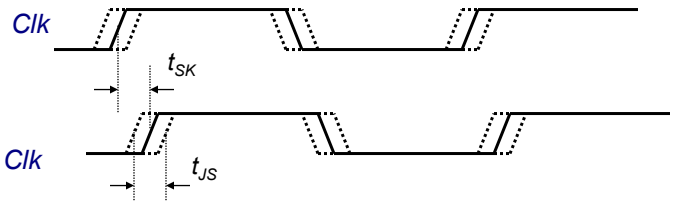
- **Clock skew**
  - Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}
- **Clock jitter**
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) t_{JS}
  - Long term t_{JL}
- **Variation of the pulse width**
  - Important for level sensitive clocking

Clock Uncertainties



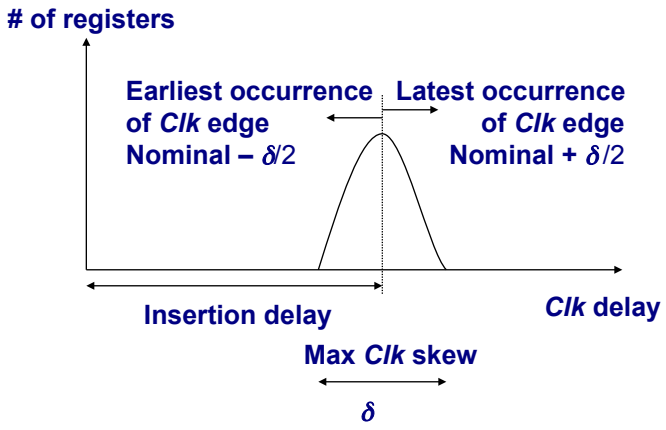
Sources of clock uncertainty

Clock Skew and Jitter



- Both skew and jitter affect the effective cycle time
- Only skew affects the race margin (usually)

Clock Skew


# of registers
Earliest occurrence of Clk edge Nominal – δ/2
Latest occurrence of Clk edge Nominal + δ/2
Insertion delay
Clk delay
Max Clk skew
δ