EE141-Spring 2009 Digital Integrated Circuits

Lecture 3
Metrics (Cntd)
IC Manufacturing

Administrativia

- Discussions start this week (Tomorrow)
- TA office hours will be held in 514 Cory
- Labs start next week
  - Everyone should have an EECS instructional account
  - You should have card key access to 353 Cory be now
- Concerns about discussion session
- Homework #1 is due this Friday
- Homework #2 to be posted on Friday

Class Material

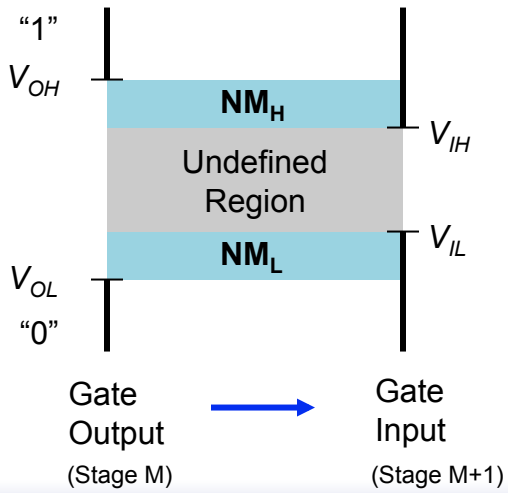
- Last lecture
  - Basic metrics for IC design (Started)
- Today's lecture
  - Metrics Continued
  - Design Rules
- Reading (1, 2.2, A)

Review: Cost

Review: Reliability

5

Definition of Noise Margins



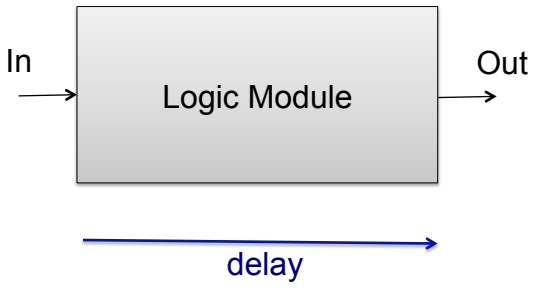
Noise margin high:
$NM_H = V_{OH} - V_{IH}$

Noise margin low:
$NM_L = V_{IL} - V_{OL}$

Key Reliability Properties

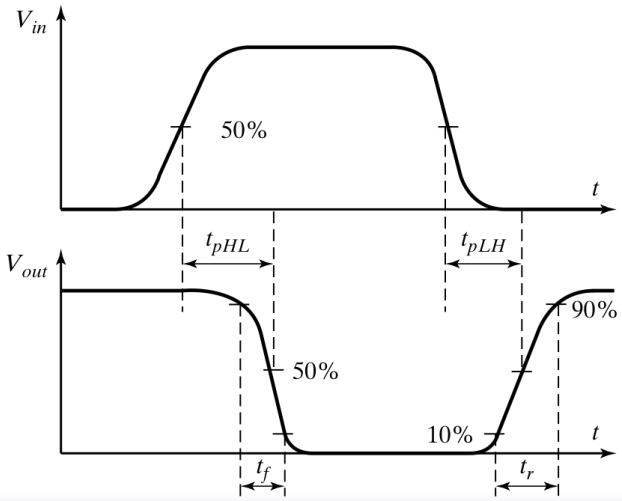
- Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too
- Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain = ∞, margin = $V_{dd}/2$)
  - Output impedance (ideal: $R_o = 0$)
  - Input impedance (ideal: $R_i = \infty$)

Primary Performance Metric: Delay



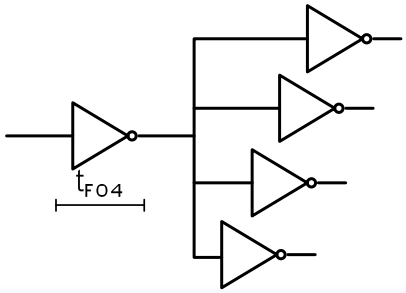
How to define delay in a universal way?

Delay Definitions

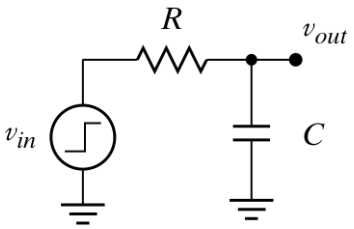


Fanout of Four (FO4) Delay

- Want a way to characterize the delay of a circuit (roughly) independent of environment
- Most common metric:
  - Delay of an inverter driving four copies of itself (t_{FO4})



A First-Order RC Network



$$v_{out}(t) = (1 - e^{-t/\tau})\ V$$

$$t_p = \ln(2)\,\tau = 0.69\ RC$$

Important model – matches delay of an inverter

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

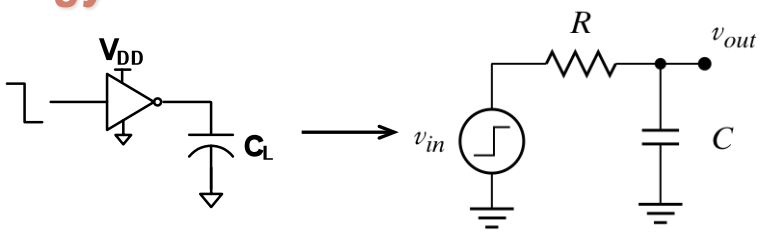
Average power:

$$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

"Power-Delay" and Energy-Delay

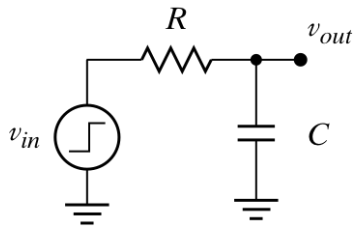
- Want low power and low delay, so how about optimizing the product of the two?
  - So-called "Power-Delay Product"
- Power·Delay is by definition Energy
  - Optimizing this pushes you to go as slow as possible
- Alternative gate metric: Energy-Delay Product
  - EDP = $(P_{av} \cdot t_p) \cdot t_p = E \cdot t_p$

Energy in CMOS



- The voltage on C_L eventually settles to V_{DD}
- Thus, charge stored on the capacitor is $C_L V_{DD}$
  - This charge has to flow out of the power supply
- So, energy is just $Q \cdot V_{DD} = (C_L V_{DD}) \cdot V_{DD}$

Energy (the harder way)



$$E_{0\to 1} = \int_0^T P_{DD}(t)dt = V_{DD}\int_0^T i_{DD}(t)dt = V_{DD}\int_0^{V_{DD}} C_L dv_{out} = C_L V_{DD}^2$$

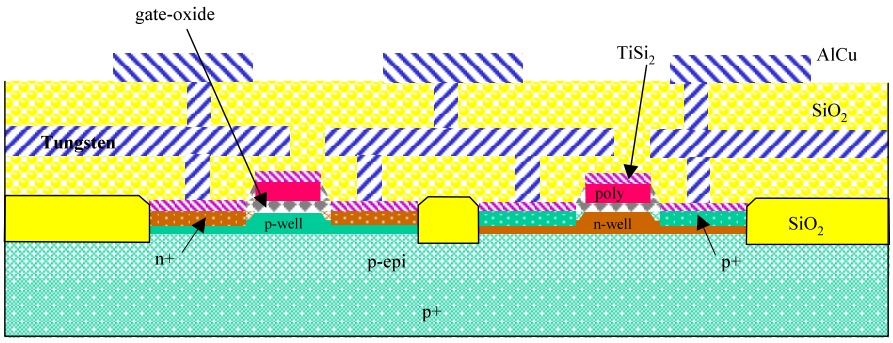
$$E_C = \int_0^T P_C(t)dt = \int_0^T v_{out} i_L(t)dt = \int_0^{V_{DD}} C_L v_{out} dv_{out} = \frac{1}{2} C_L V_{DD}^2$$

Summary

- Understanding the design metrics that govern digital design is crucial
  - Cost
  - Robustness
  - Performance/speed
  - Power and energy dissipation

Intermezzo: Design Rules

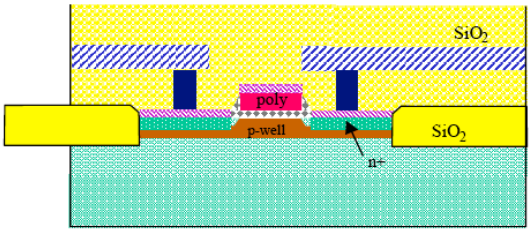
A Modern CMOS Process



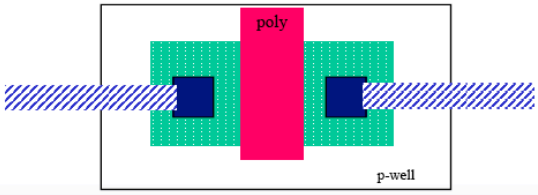
Dual-Well Shallow-Trench-Isolated CMOS Process

Transistor Layout

Cross-Sectional View



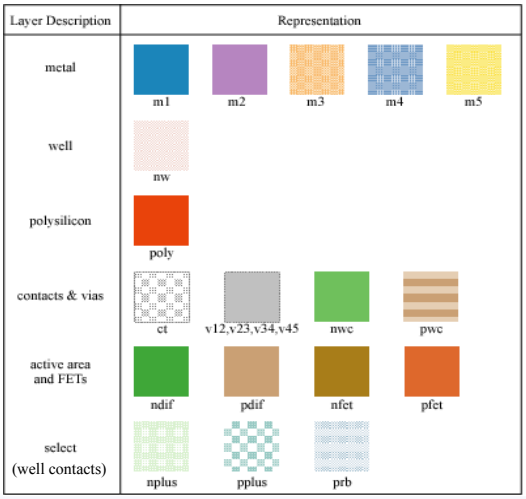
Layout View



CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Well contact (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layers in 0.25 μm CMOS process



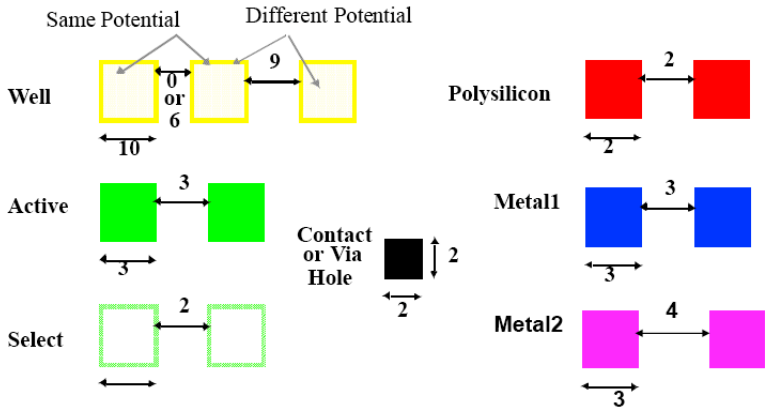
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

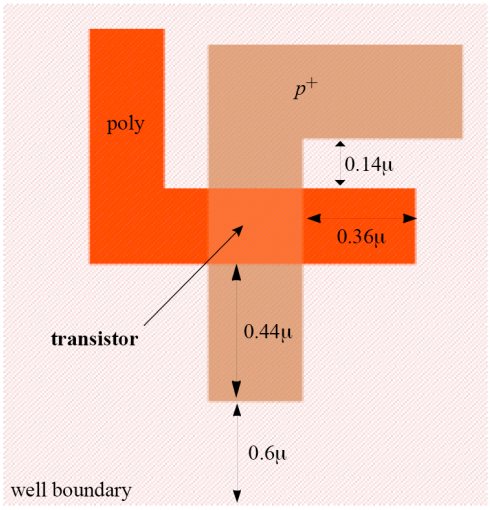
Design Rules

- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

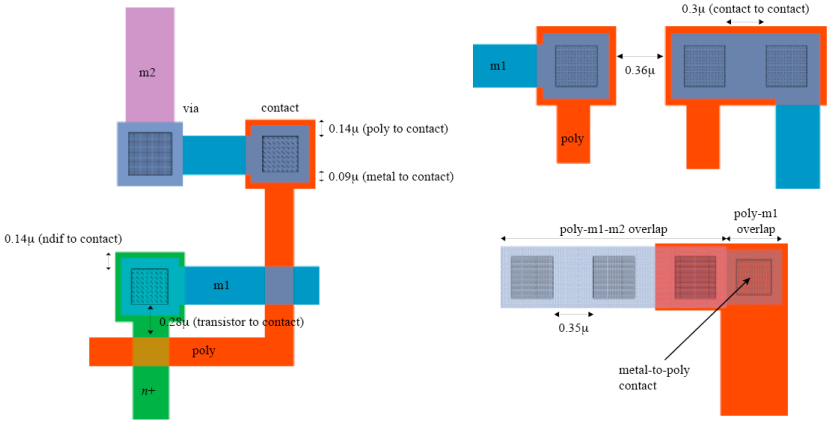
Intra-Layer Design Rules



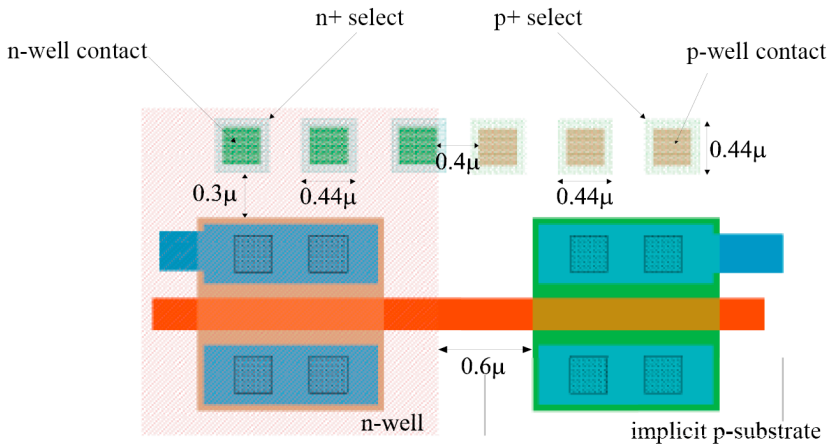
Inter-Layer: Transistor Layout



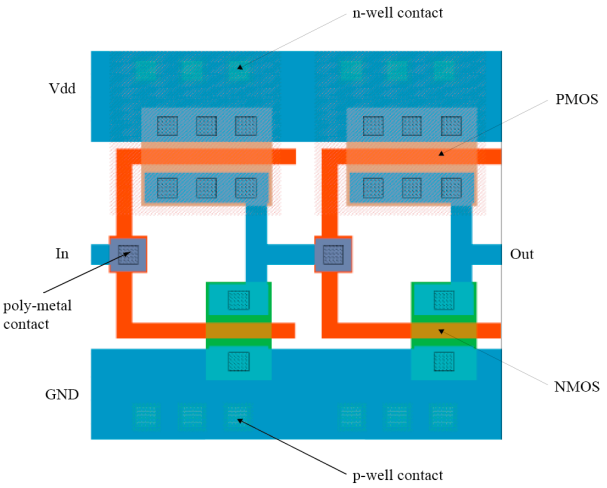
Inter-Layer: Vias and Contacts



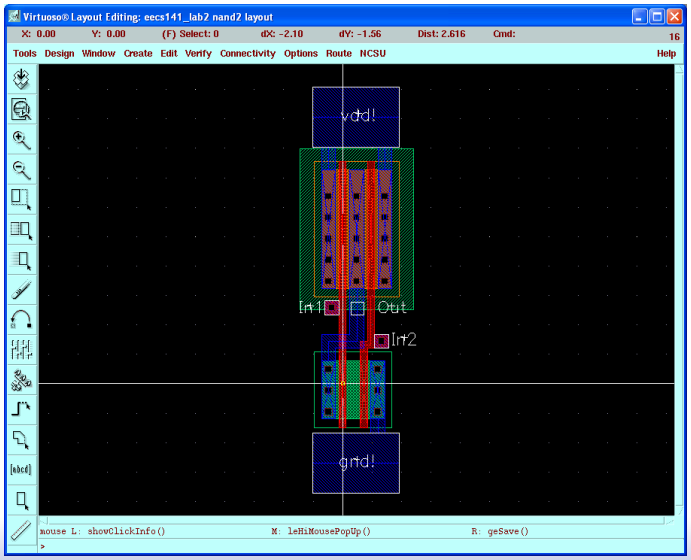
Inter-Layer: Well and Substrate



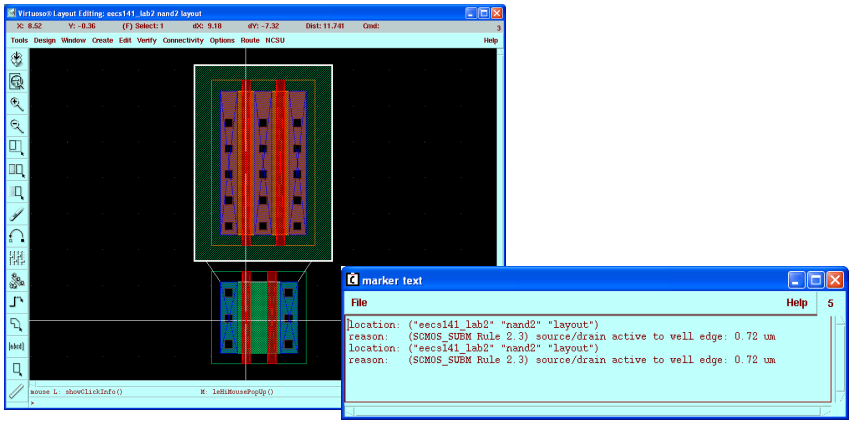
CMOS Inverter Layout



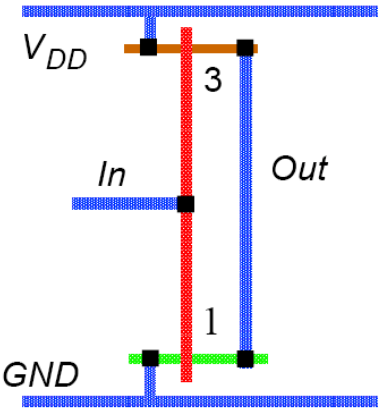
Layout Editor



Design Rule Checker



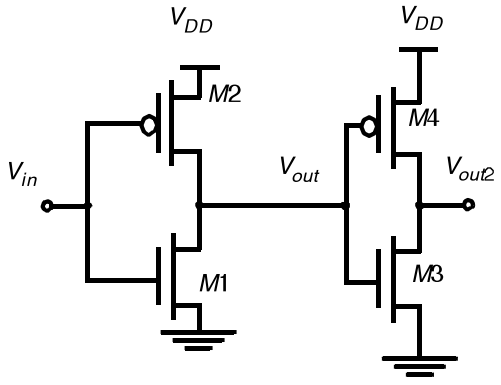
Sticks Diagram



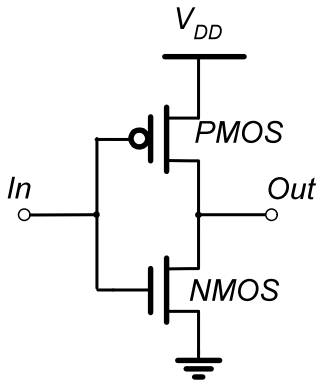
Stick diagram of inverter

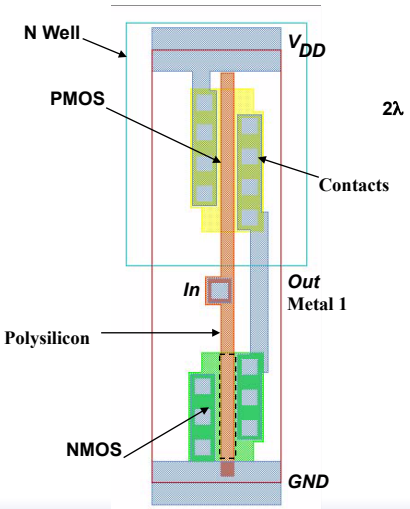
- Dimensionless layout entities
- Only topology is important

Circuit Under Design



CMOS Inverter

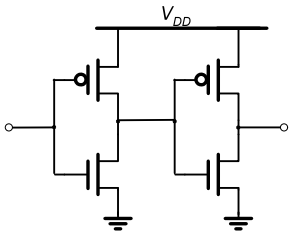


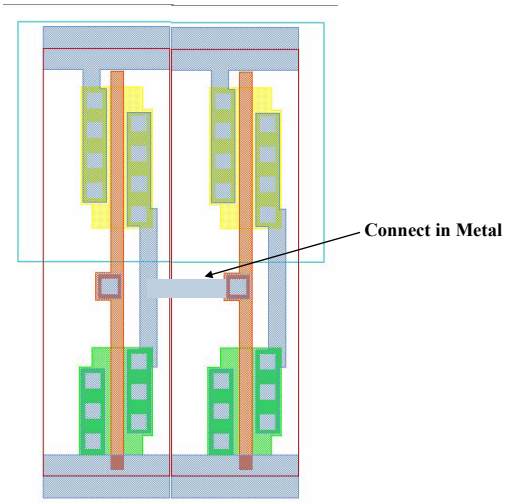


Two Inverters

Share power and ground

Abut cells





Next Lecture

- From simple to more complex gates …