EE223 Analog Integrated Circuits
Fall 2018

Lecture 6: MOS Capacitances

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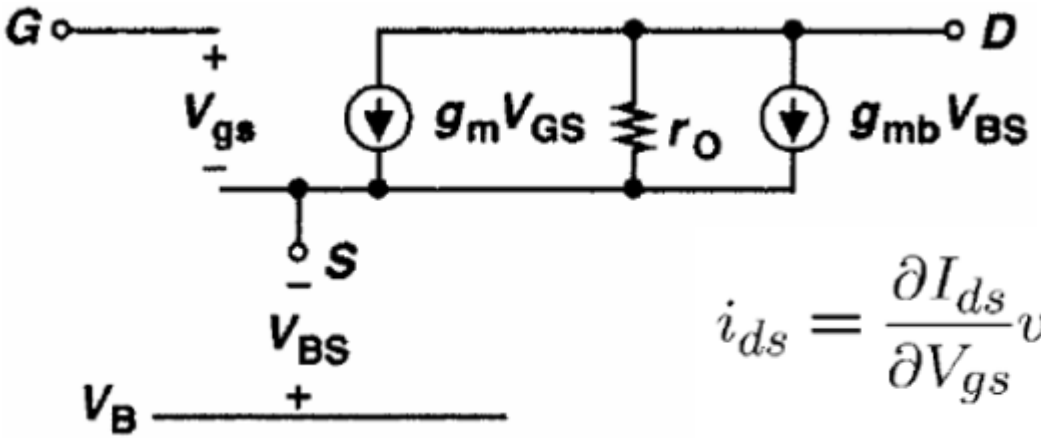
ENG-259

MOS Low-Frequency Small-Signal Model



$$i_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}} v_{gs} + \frac{\partial I_{ds}}{\partial V_{bs}} v_{bs} + \frac{\partial I_{ds}}{\partial V_{ds}} v_{ds}$$

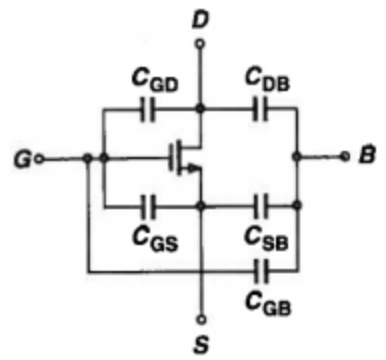
$$i_{ds} = g_m V_{gs} + g_{mb} V_{bs} + g_{ds} V_{ds}$$

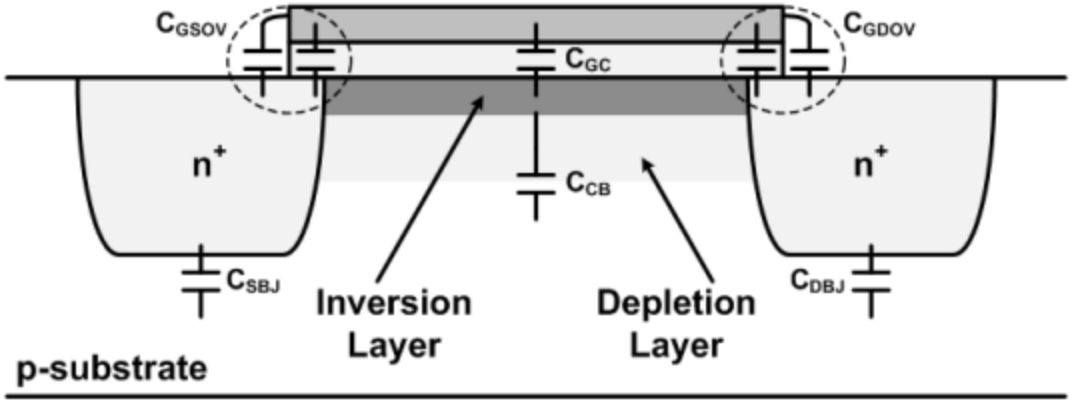
$$g_m = \left.\frac{\partial i_D}{\partial v_{gs}}\right|_Q \approx \mu C_{OX} \frac{W}{L_{eff}} \left.(V_{GS} - V_T)\right|_Q$$

$$g_0 = \left.\frac{\partial i_D}{\partial v_{ds}}\right|_Q \approx \left(\frac{\mu C_{OX}}{2}\right)\left(\frac{W}{L_{eff}}(V_{GS} - V_T)^2\right)\lambda \approx \lambda I$$

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{bs}}\right|_Q \approx \mu C_{OX} \left.\frac{W}{L_{eff}}[V_{GS} - V_T]\right|_Q * \left(-\left.\frac{\partial V_T}{\partial v_{bs}}\right|_Q\right) \cong \frac{\gamma g_m}{2\sqrt{2\phi_F + V_{SB}}} = \eta g_m$$

MOS Transistor Capacitances





Gate - Channel Cap $= C_{GC} = WL_{eff}C_{ox}$

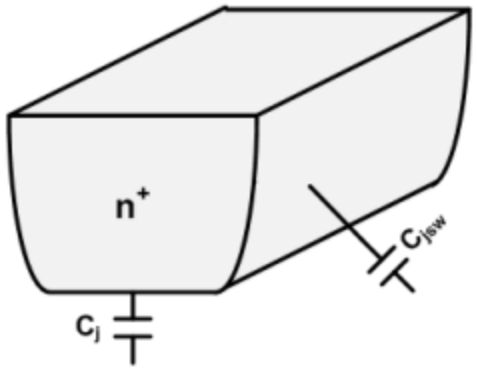
Channel - Bulk Cap $= C_{CB} = WL_{eff}\sqrt{\dfrac{q\varepsilon_{Si}N_{sub}}{4\Phi_F}}$

Gate - Source Overlap (Fringing) Cap $= C_{GSov} = WC_{ov}$ Note, $C_{ov} \neq C_{ox}L_D$

Gate - Drain Overlap (Fringing) Cap $= C_{GDov} = WC_{ov}$

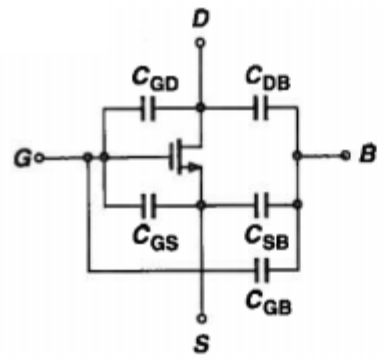
Source - Bulk Junction Cap $= C_{SBJ} = A_S C_j + P_S C_{jsw}$

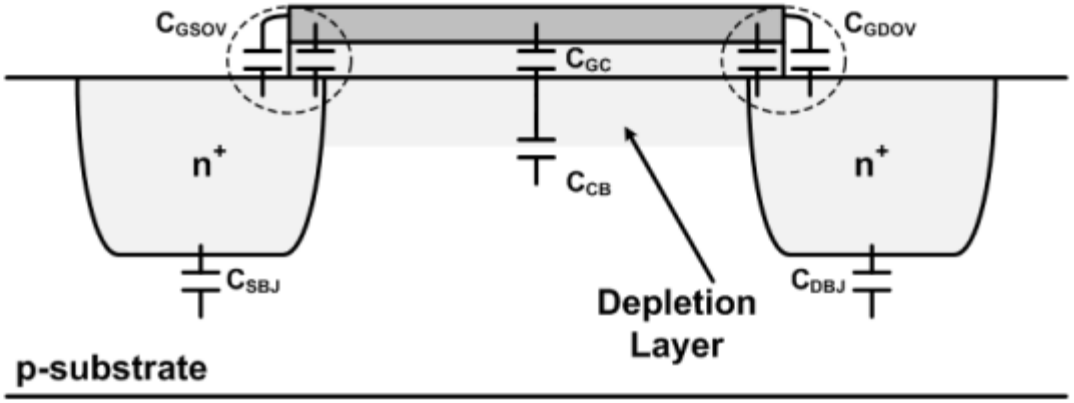
Drain - Bulk Junction Cap $= C_{DBJ} = A_D C_j + P_D C_{jsw}$



$$C_j = \frac{C_{j0}}{\left(1+\dfrac{V_{BX}}{\Phi_B}\right)^m} \qquad C_{jsw} = \frac{C_{jsw0}}{\left(1+\dfrac{V_{BX}}{\Phi_B}\right)^{msw}}$$

MOS Transistor Capacitances (Off)





$$\text{Gate - Drain Cap} = C_{GD} = C_{GDov} = WC_{ov}$$

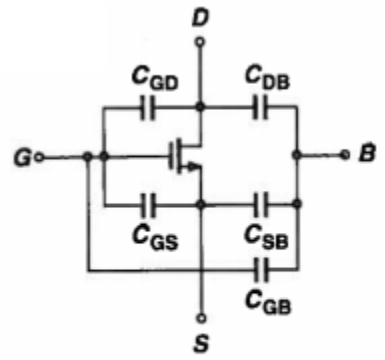
$$\text{Gate - Source Cap} = C_{GS} = C_{GDov} = WC_{ov}$$

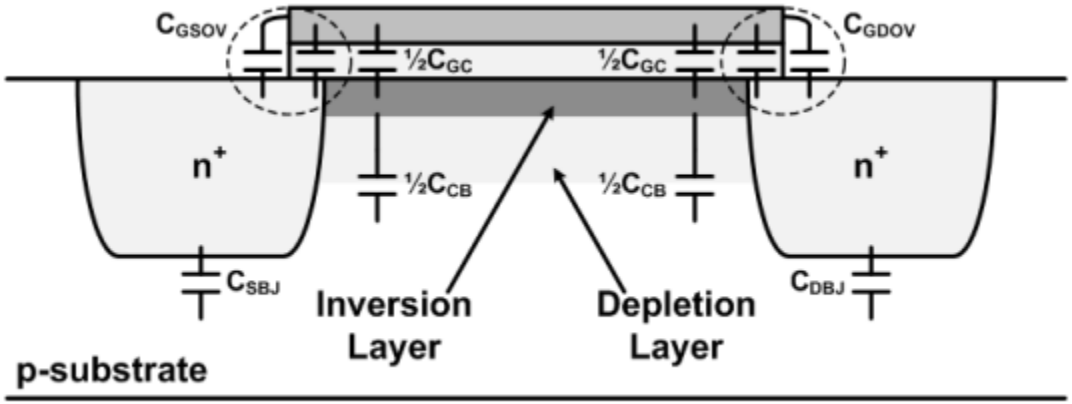
$$\text{Gate - Bulk Cap} = C_{GB} = \frac{C_{GC}C_{CB}}{C_{GC} + C_{CB}}$$

$$\text{Drain - Bulk Cap} = C_{DB} = C_{DBJ}$$

$$\text{Source - Bulk Cap} = C_{SB} = C_{SBJ}$$

MOS Transistor Capacitances (Triode)





$$\text{Gate - Drain Cap} = C_{GD} = C_{GDov} + \frac{1}{2}C_{GC}$$

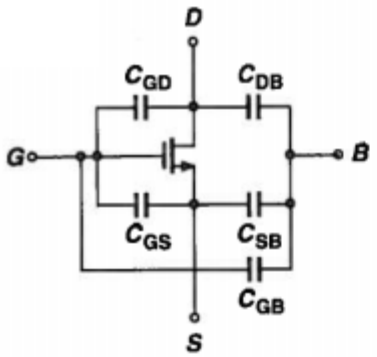
$$\text{Gate - Source Cap} = C_{GS} = C_{GSov} + \frac{1}{2}C_{GC}$$

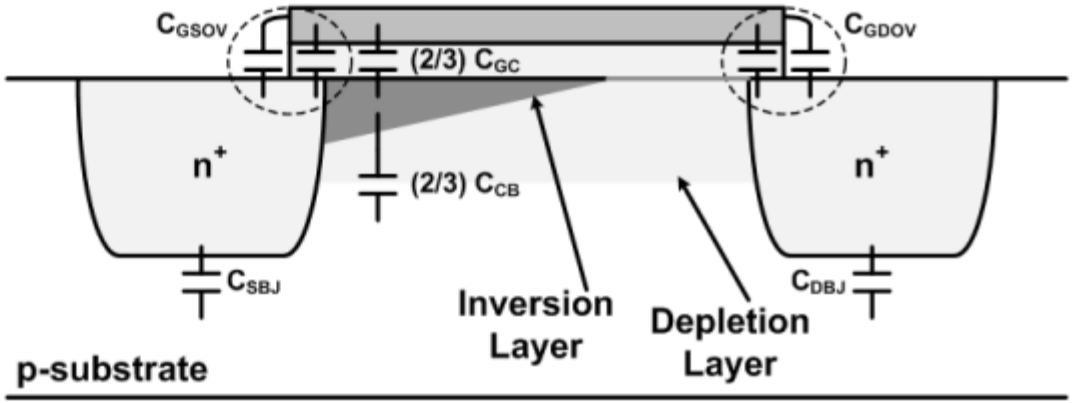
$$\text{Gate - Bulk Cap} = C_{GB} \approx 0$$

$$\text{Drain - Bulk Cap} = C_{DB} = C_{DBJ} + \frac{1}{2}C_{CB}$$

$$\text{Source - Bulk Cap} = C_{SB} = C_{SBJ} + \frac{1}{2}C_{CB}$$

MOS Transistor Capacitances (Saturation)





$$\text{Gate - Drain Cap} = C_{GD} = C_{GDov}$$

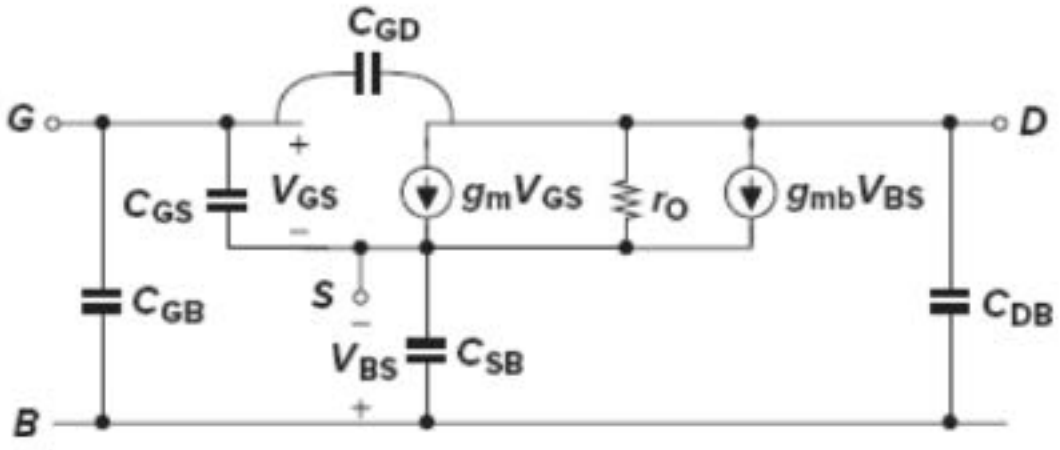
$$\text{Gate - Source Cap} = C_{GS} = C_{GSov} + \frac{2}{3}C_{GC}$$

$$\text{Gate - Bulk Cap} = C_{GB} \approx 0$$

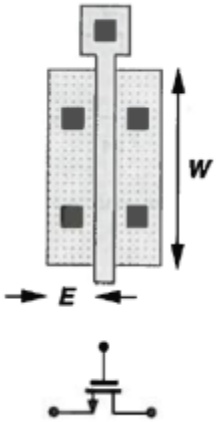
$$\text{Drain - Bulk Cap} = C_{DB} = C_{DBJ}$$

$$\text{Source - Bulk Cap} = C_{SB} = C_{SBJ} + \frac{2}{3}C_{CB}$$

MOS Small-Signal Model including Capacitances



MOS Source & Drain Junction Capacitors

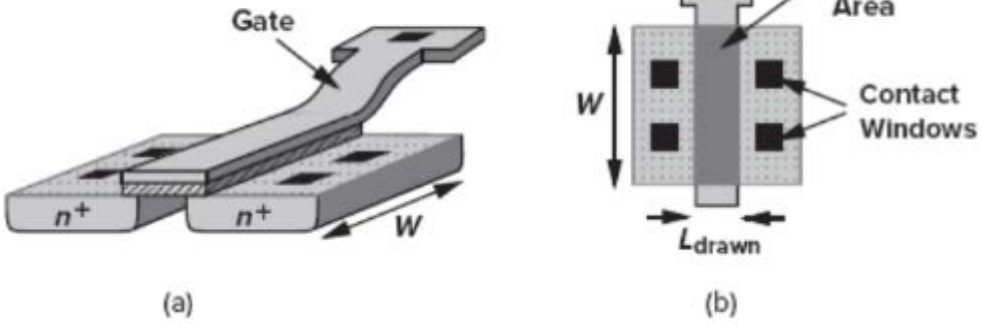


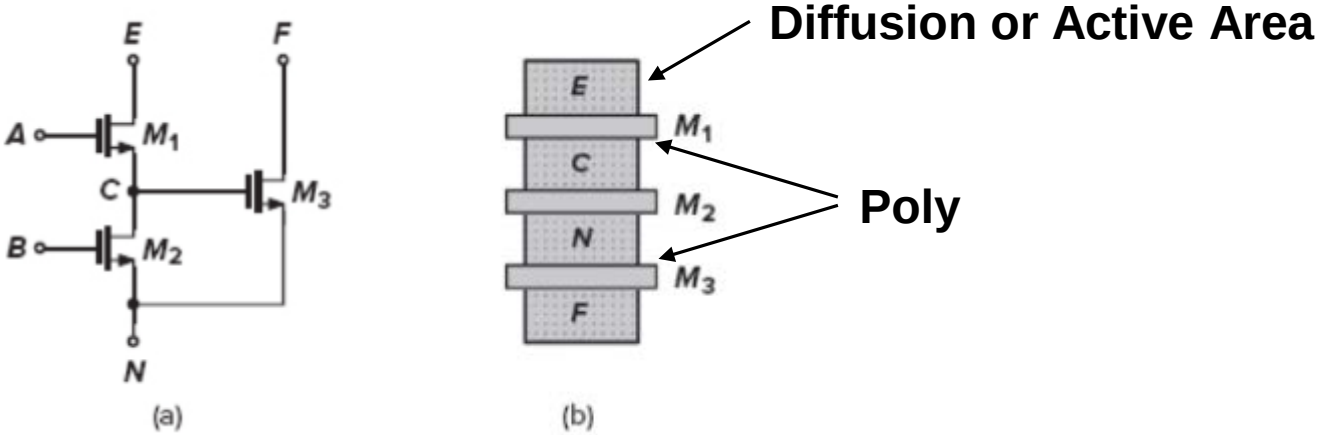
$$A_S = A_D = WE$$

$$P_S = P_D = 2(W + E)$$

$$\text{Junction } C_{SB} = C_{DB} = AC_j + PC_{jsw} = WEC_j + 2(W + E)C_{jsw}$$

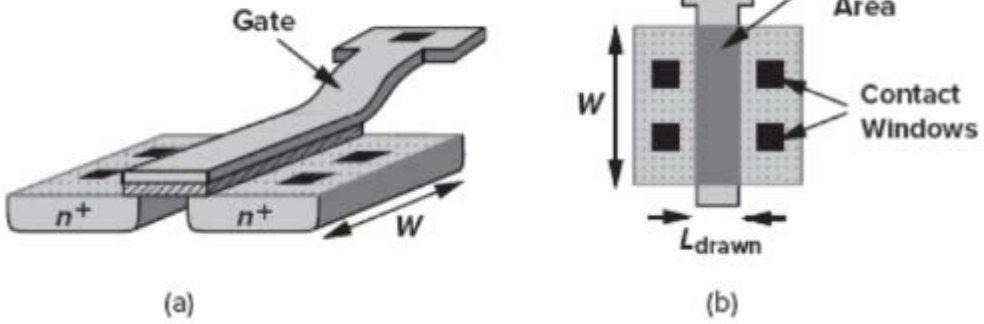
MOS Layout

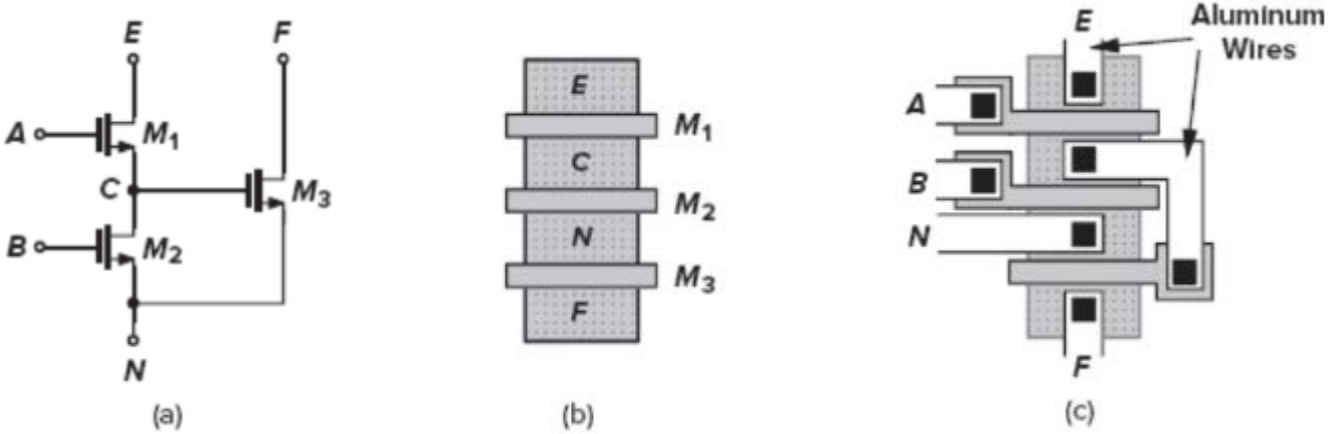




When Diffusion and Poly Intersects in the layout, Transistor is formed.

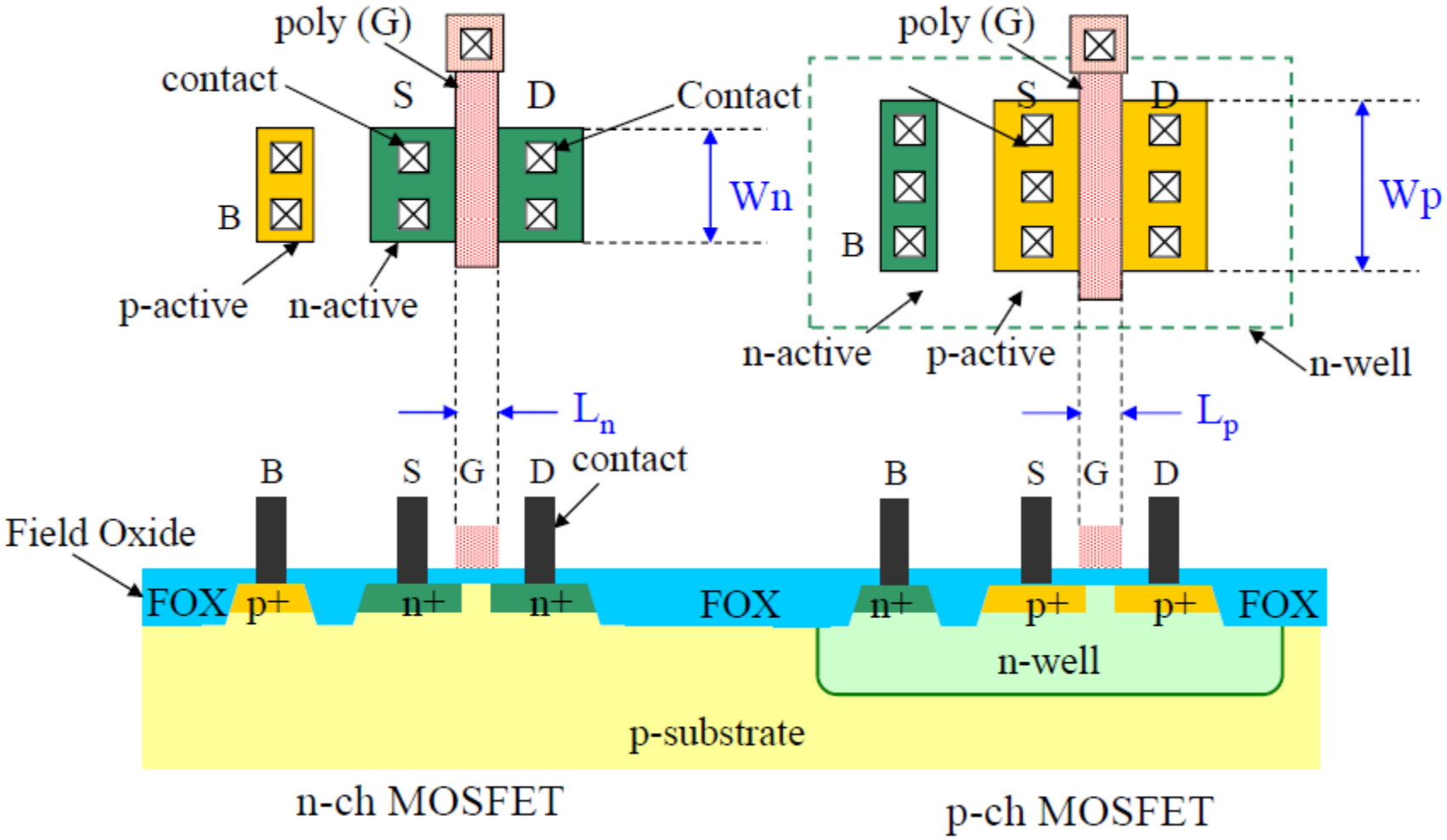
MOS Layout





Metal is used to make the circuit connection between transistors.

MOS Layout Example



Mask Layers

- Layer numbers are assigned to Well, Active, Poly, Contact, Metal, Via, Silicide Protect, and Dummy, respectively.
- Some layer is automatically generated from the pattern on the drawn layer.
  - ex. FOX and GOX is generated from the pattern on the active layer.