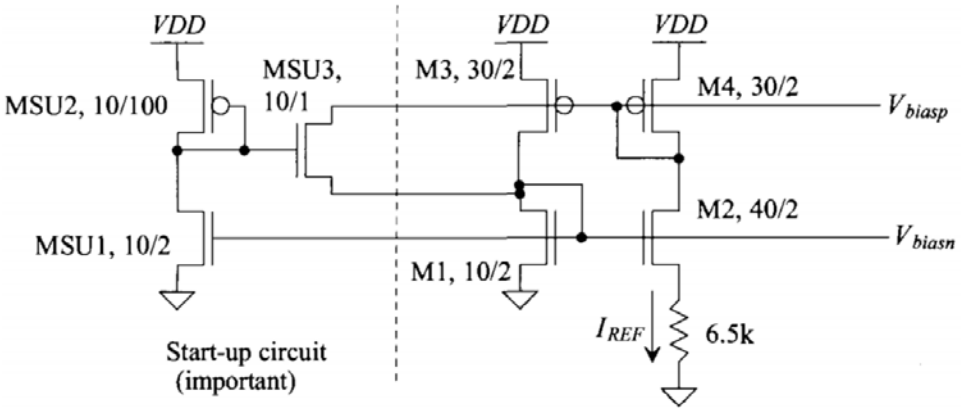
EE223 Homework #3 Oct. 1, 2018

Due: Oct. 15, 2018 6PM. 20% / day will be deducted if you miss the 6 PM Oct. 15 deadline.

Design of Beta Multiplier Circuit

In this homework, you will design a beta multiplier circuit presented in Lecture 11 which is shown here again. Run a dc simulation for problem 1. For problem 2 and 4, run transient simulations.



The device size above is reference only. You must come up with your own size based on VDD=1V at TT, 27C. Your simulation results on dc operating point should show M1-M4 are in saturation region.

1. Run a dc simulation with VDD=1V, Temperature=27C in Typical corner. Using ADE-L window, select Results->Annotate feature to get the dc operating point information as well as the node voltage information in the schematic you have designed. Create a screenshot of this! (**20 points**)

2. Using ADE-XL, run transient simulations for 1 us. Ramp up the power supply from 0V at t=0 to the final voltage (VDD=1V for example) in 10 ns. Plot the transient waveforms for VDD, Vbiasn, Vbiasp, drain currents of M1, M2, MSU1, MSU3. Repeat the simulation without the Start-up circuit by connecting the drain of MSU3 to VDD and the source of MSU3 to GND. Plot the same parameters to compare if there is any difference between with and without the start-up circuit. (**20 points**)

3. From the simulation result, you will get the Iref in your design for the size you are using. From this, using the expression for Iref shown in Lecture 11, find out the KP value when VDD=1V, Temperature=27C. (**10 points**)

4. Using Cadence ADE-XL, simulate the circuit in the following conditions and check if the circuit starts without any problem. Measure the current through M4 (Iref) at 1 us and plot it over the following PVT corners.
    a) Process variation only: TT, SS, FF, SF, FS at VDD=1V and Temp=27C (**10 points**)
    b) Supply variation only: 0.8V, 0.9V, 1V, 1.1V, 1.2V at TT & Temp=27C (**10 points**)
    c) Temperature variation only: -40C, 0C, 25C, 50C, 100C at VDD=1V and TT (**10 points**)
    d) All PVT variations (TT, SS, FF, SF, FS, VDD=0.9V, 1V, 1.1V, Temp=-40, 0, 50, 100C) This will give you a set of 60 simulation results. (**10 points**)
    e) For the case c) at VDD=1, TT, plot gm vs. Temp for transistor M1. For this plot, use Tools->Result Browser->TranOP in ADE-XL window and select gm in M1 folder. (**10 points**)

    You goal is to reduce the Iref variation over PVT. Report the minimum and maximum currents as well as the mean and 1-sigma number for Iref variation over 60 PVT corner simulations.