EE141-Spring 2010 Digital Integrated Circuits

Lecture 9
Transistors

Guest Lecturer:
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Administrativia

- Midterm on Friday Febr 19 6:30-8pm in 2060 Valley LSB
  - Open book
  - Do not forget your important class material nor calculator
  - Covers from start of semester to optimization of complex logic – wires not included!
- Review session tomorrow Th 2/18 at 6:30pm
  - Room to be announced on web-site
- No lab this week
- Hw 4 due next week Friday

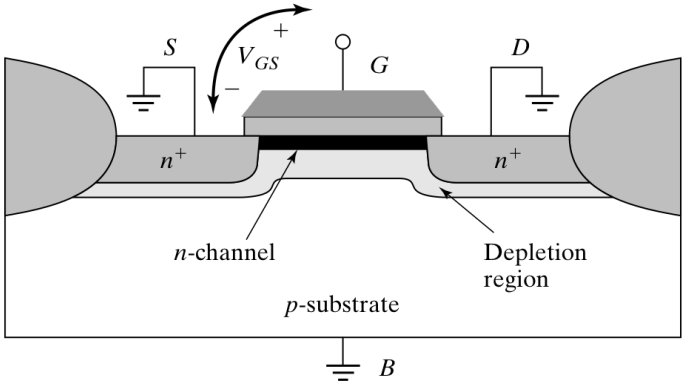
Class Material

- Last lecture
  - Wiring + first glimpse at transitors (threshold)
- Today's lecture
  - Transistor models
- Reading (Ch 3)

MOS Transistor

What do digital IC designers need to know?

Threshold Voltage: Concept



- With positive gate bias, electrons pulled toward the gate
- With large enough bias, enough electrons will be pulled to "invert" the surface (p→n type)
- Voltage at which surface inverts: “magic” threshold voltage V_T

The Threshold Voltage

- Threshold

$$V_T = \varphi_{FB} + 2\varphi_F + \frac{Q_B}{C_{ox}}$$ ← Depletion charge

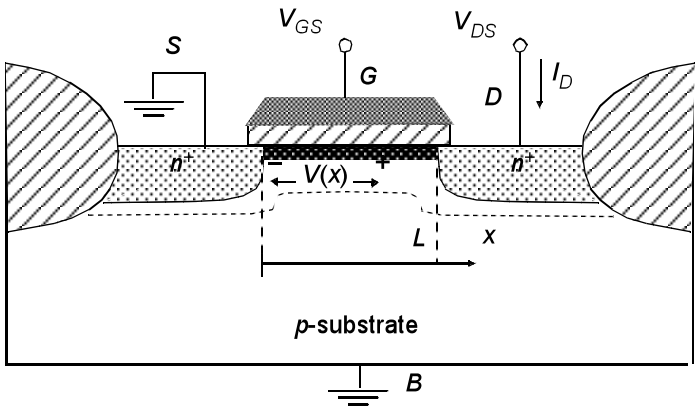
$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{2\varphi_F}\right)$$

- Fermi potential

$$\phi_F = \phi_T \cdot \ln\frac{N_A}{n_i}$$

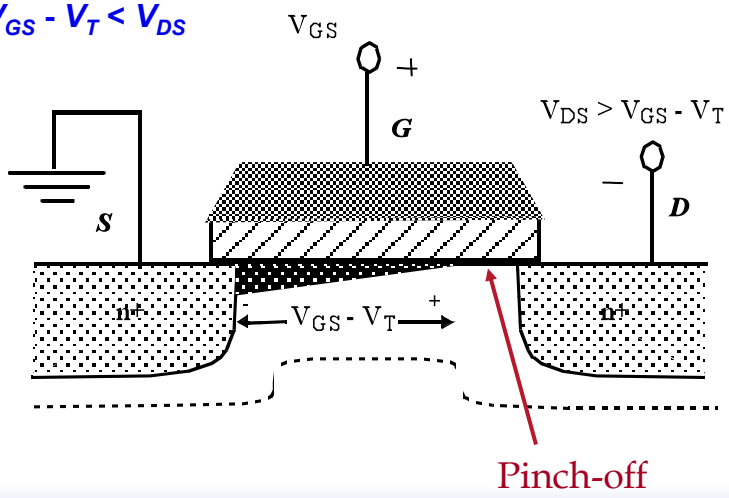
$2\Phi_F$ is approximately 0.6V for p-type substrates
γ is the body factor
V_{T0} is approximately 0.45V for our process

Transistor with Gate and Drain Bias



Transistor in Saturation

$0 < V_{GS} - V_T < V_{DS}$



Saturation

- For $(V_{GS} - V_T) < V_{DS}$, the effective drain voltage and current saturate:

$$V_{DS,eff} = (V_{GS} - V_T)$$

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

- Of course, real drain current isn't totally independent of V_{DS}
  - For example, approx. for channel-length modulation:

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

Modes of Operation

Cutoff:

$V_{GS} - V_T < 0$ $\quad I_D = 0$

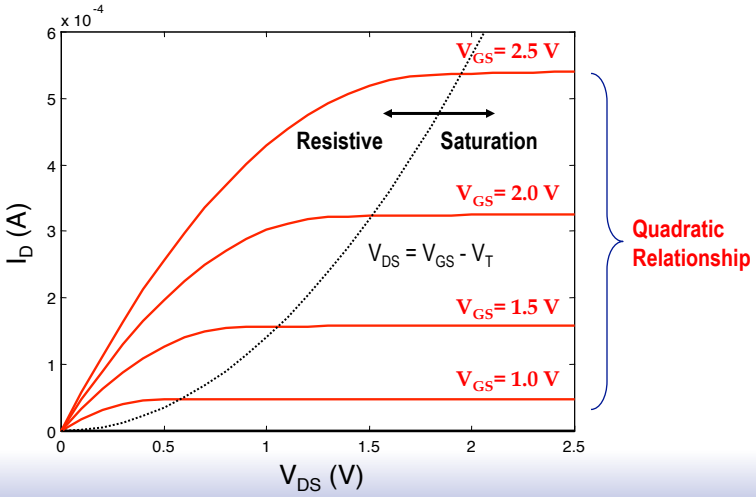
Linear (Resistive):

$V_{GS} - V_T > V_{DS}$ $\quad I_D = k'_n \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$

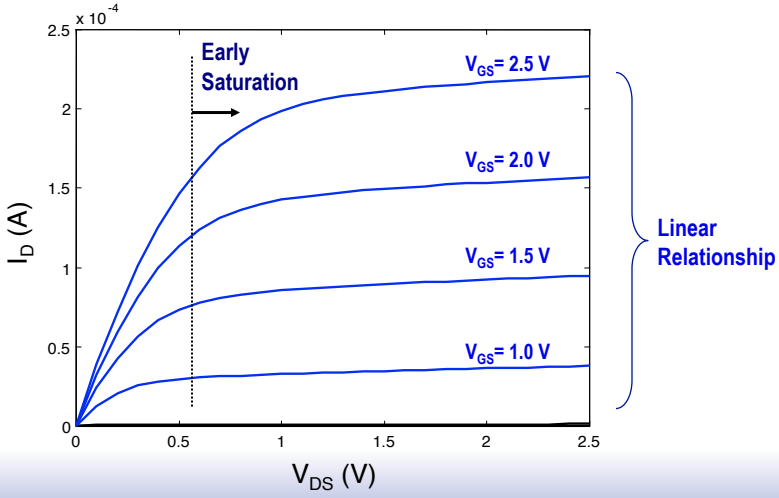
Saturation:

$0 < V_{GS} - V_T < V_{DS}$ $\quad I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$

Current-Voltage Relations: A Good Ol' Transistor

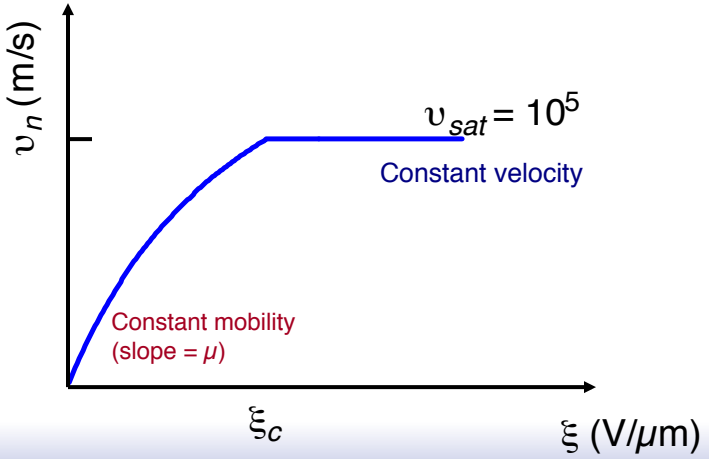


Current-Voltage Relations: The Deep Sub-Micron Transistor

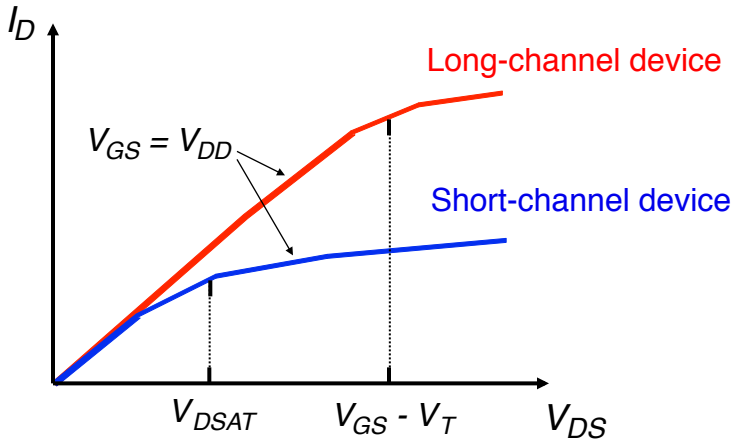


Velocity Saturation

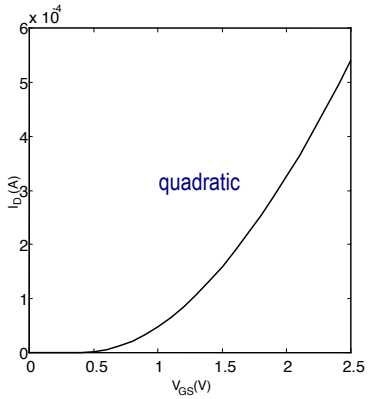
- Velocity saturates due to carrier scattering effects



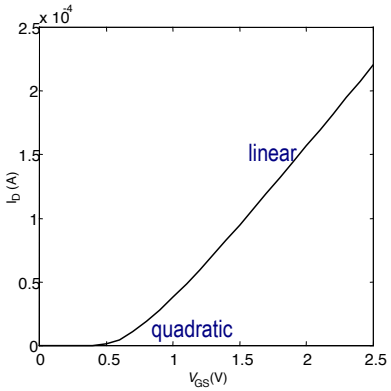
Velocity Saturation



I_D versus V_{GS}



Long Channel
(L=2.5μm)



Short Channel
(L=0.25μm)

Including Velocity Saturation

Approximate velocity:

$$\upsilon = \frac{\mu_n \xi}{1 + \xi/\xi_c} \quad \text{for} \quad \xi \le \xi_c$$

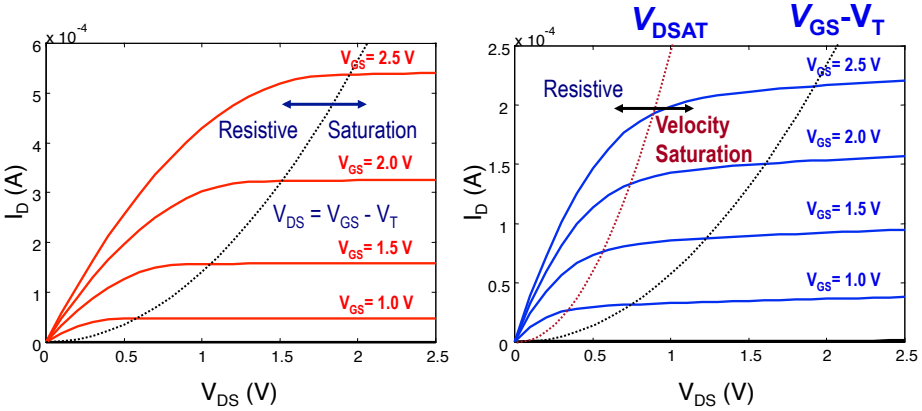
$$= \upsilon_{sat} \quad \text{for} \quad \xi \ge \xi_c$$

Continuity requires that: $\xi_c = 2\upsilon_{sat}/\mu_n$

Integrating to find the current again:

$$I_D = \frac{\mu_n C_{ox}}{1 + (V_{DS}/\xi_c L)} \left(\frac{W}{L}\right) \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Regions of Operation



Long Channel (L=2.5μm)

W/L=1.5

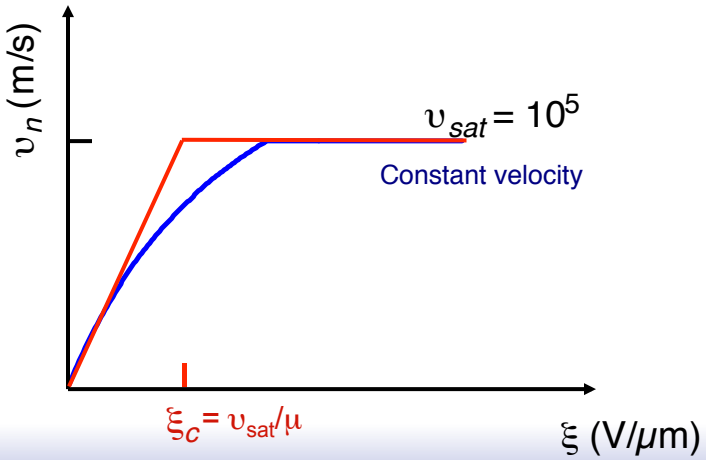
Short Channel (L=0.25μm)

Models, Models, Models…

- Exact behavior of transistor in velocity sat. somewhat challenging if want simple/easy to use models
- So, many different models developed over the years
  - v-sat, alpha, unified, V_T*, etc.
- Simple model for manual analysis desirable
  - Assume velocity perfectly linear until υ_{sat}
  - Assume V_{DSAT} constant

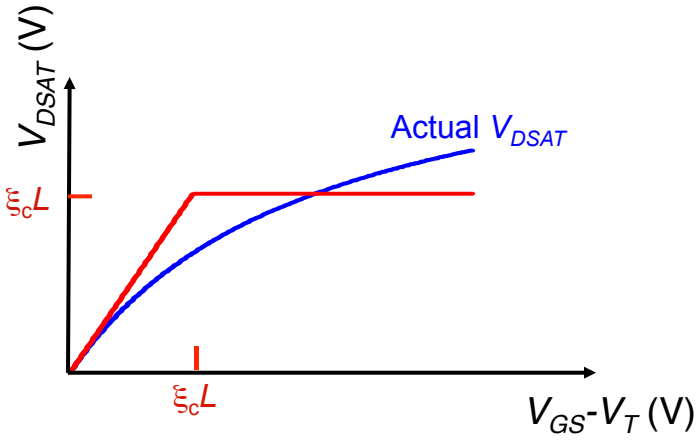
Simplified Velocity Saturation

- Assume velocity perfectly linear until hit υ_{sat}



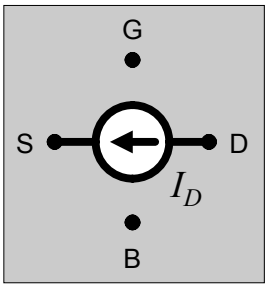
Simplified Velocity Saturation (cont'd)

- Assume $V_{DSAT} = \xi_c L$ when $(V_{GS} - V_T) > \xi_c L$



A Unified Model for Manual Analysis

define $V_{GT} = V_{GS} - V_T$



for $V_{GT} \leq 0$: $I_D = 0$

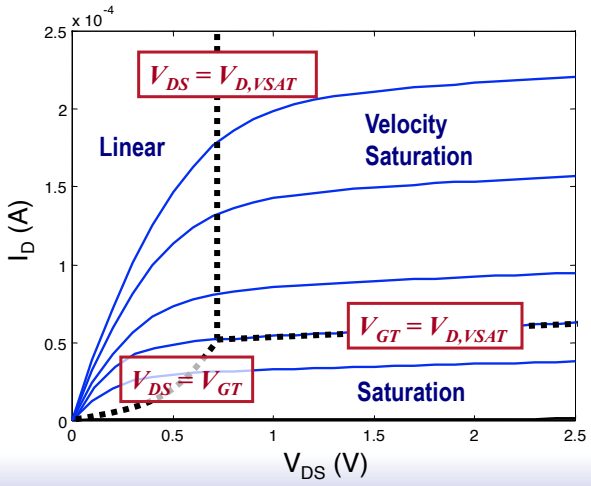
for $V_{GT} \geq 0$:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{DS,eff} - \frac{V_{DS,eff}^2}{2} \right) \cdot \left(1 + \lambda \cdot V_{DS}\right)$$

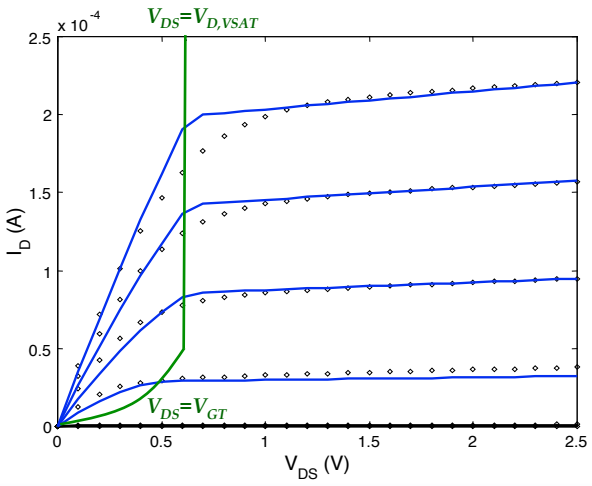
with $V_{DS,eff} = \min (V_{GT}, V_{DS}, V_{D,VSAT})$

Simplified Model

- Define $V_{GT} = V_{GS} - V_T$, $V_{D,VSAT} = \xi_c \cdot L$



Simple Model versus SPICE



One Last Simplification

- If device always operates in velocity sat.:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T - \frac{V_{D,VSAT}}{2} \right) V_{D,VSAT}$$

- "V_T*" model:

$$V_T^* \equiv V_T + \frac{V_{D,VSAT}}{2}$$

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T^* \right) V_{D,VSAT}$$

- Good for first cut, simple analysis

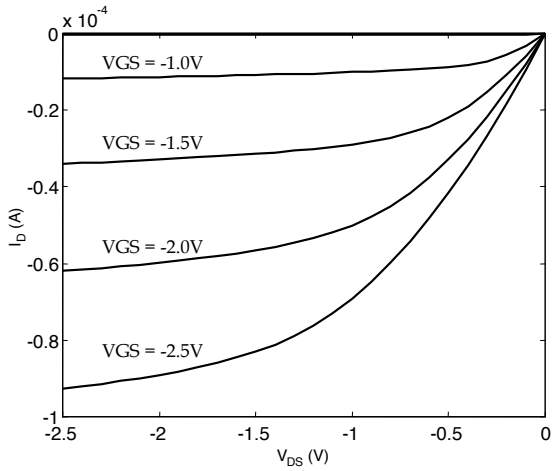
Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{VSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

Textbook: page 103

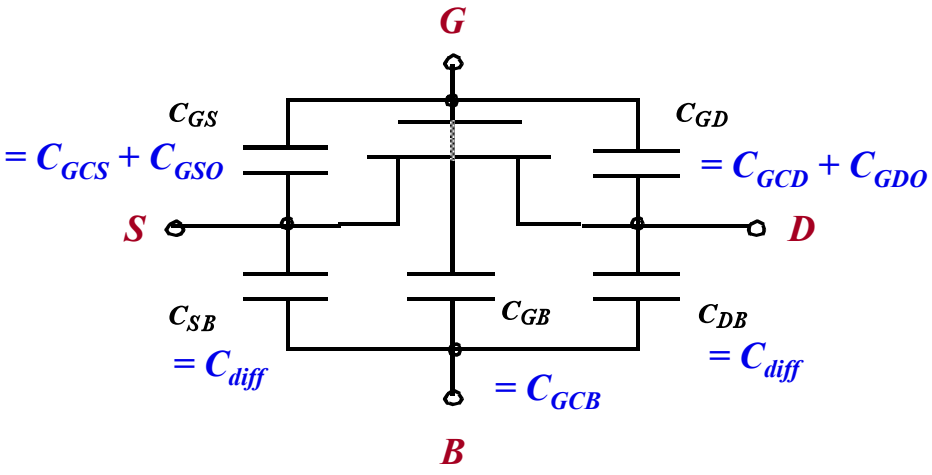
A PMOS Transistor



- All variables negative
- I prefer to work with absolute values – makes life easier.

MOS Capacitance

MOS Capacitances



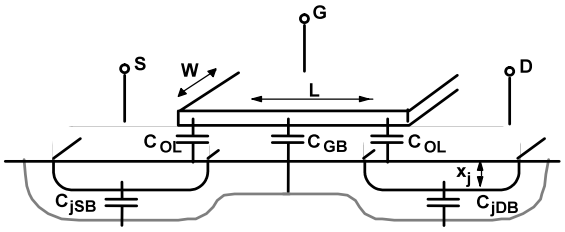
Gate Capacitance

- Capacitance (per area) from gate across the oxide is $W \cdot L \cdot C_{ox}$, where $C_{ox}=\varepsilon_{ox}/t_{ox}$

Gate Capacitance

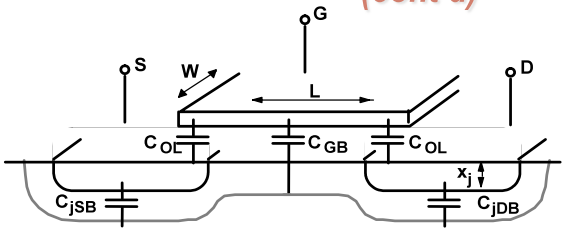
- Distribution between terminals is complex
  - Capacitance is really distributed
    - Useful models lump it to the terminals
  - Several operating regions:
    - Way off, off, transistor linear, transistor saturated

Transistor In Cutoff



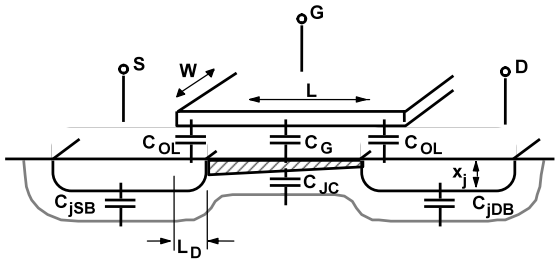
- When the transistor is off, no carriers in channel to form the other side of the capacitor.
  - Substrate acts as the other capacitor terminal
  - Capacitance becomes series combination of gate oxide and depletion capacitance

Transistor In Cutoff *(cont'd)*



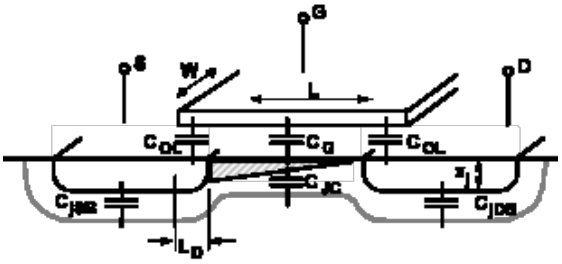
- When $|V_{GS}| < |V_T|$, total C_{GCB} much smaller than $W \cdot L \cdot C_{ox}$
  - Usually just approximate with $C_{GCB} = 0$ in this region.
- (If V_{GS} is "very" negative (for NMOS), depletion region shrinks and C_{GCB} goes back to ~$W \cdot L \cdot C_{ox}$)

Transistor in Linear Region



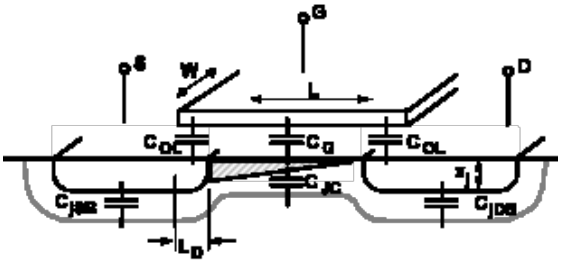
- Channel is formed and acts as the other terminal
  - C_{GCB} drops to zero (shielded by channel)
- Model by splitting oxide cap equally between source and drain
  - Changing either voltage changes the channel charge

Transistor in Saturation Region



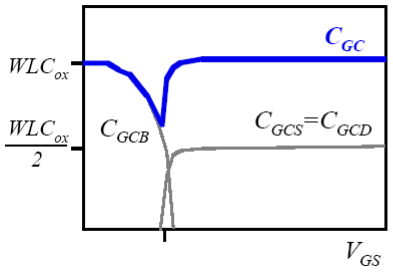
- Changing source voltage doesn't change V_{GC} uniformly
  - E.g. V_{GC} at pinch off point still V_{TH}
- Bottom line: $C_{GCS} \approx 2/3 \cdot W \cdot L \cdot C_{ox}$

Transistor in Saturation Region (cont'd)

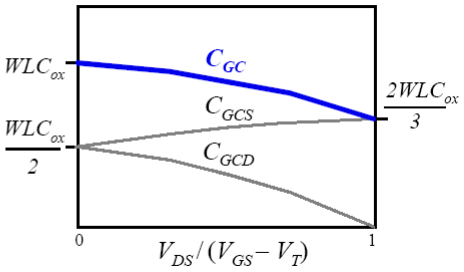


- Drain voltage no longer affects channel charge
  - Set by source and V_{DS_sat}
- If change in charge is 0, $C_{GCD} = 0$

Gate Capacitance

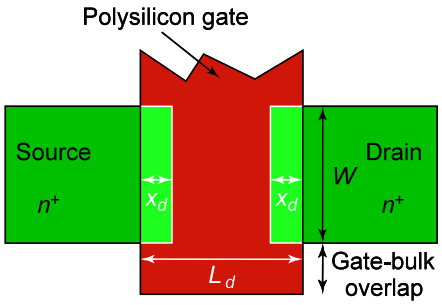


C_{gate} vs. V_{GS} (with $V_{DS} = 0$)

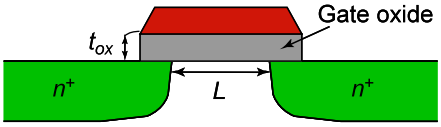


C_{gate} vs. operating region

Gate Overlap Capacitance



Top view

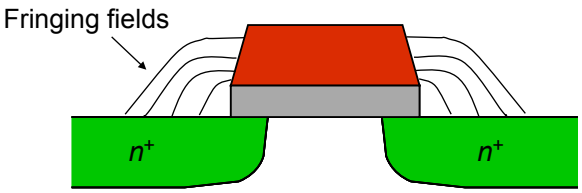


Cross section

$$C_O = C_{ox} \cdot x_d$$

Off/Lin/Sat → $C_{GSO} = C_{GDO} = C_O \cdot W$

Gate Fringe Capacitance



Cross section

- C_{OV} not just from metallurgic overlap – get fringing fields too
- Typical value: ~0.2fF·W(in μm)/edge