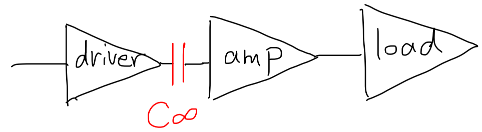
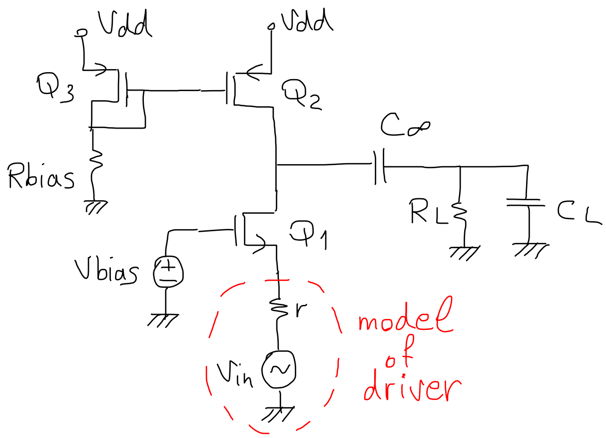
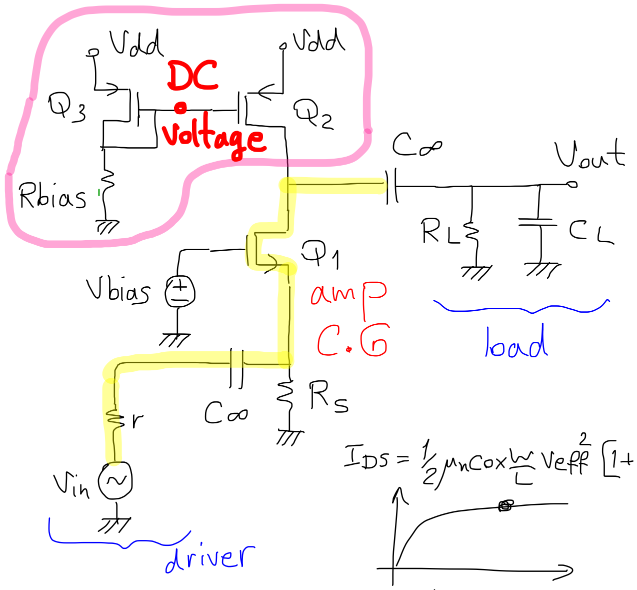
* Common Gate Amplifiers :







$I_{SD2} = \frac{1}{2}\mu_p C_{ox} \frac{W_2}{L_2}(V_{SG2}-V_{th})^2\left[1+\lambda_p\left(V_{SD2}-(V_{SG2}-V_{th})\right)\right]$

$I_{DS1} = \frac{1}{2}\mu_n C_{ox} \frac{W_1}{L_1}(V_{GS1}-V_{th})^2\left[1+\lambda_n\left(V_{DS1}-(V_{GS1}-V_{th})\right)\right]$

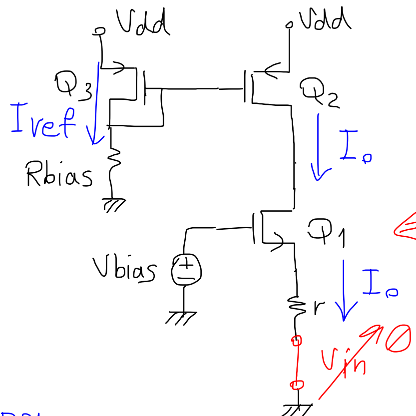
$* \; V_{SD2}+V_{DS1}+rI_{DS1} = V_{dd}$

$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}^2[1+\ldots$

$V_{DS} > V_{eff}$
$V_{GS} > V_{th}$

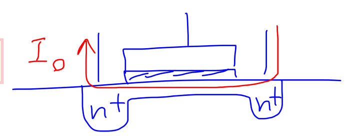
*DC Analysis

1. open caps
2. discard AC sources
3. find Iref
4. find I_o
5. Assume Q_1 is operating in the active region
6. write current equations and find V_{GS1}, V_{DS}, I_{DS1}
7. verify Q_1 operating point
8. find gm and rds



objective: find the operating point and small-signal parameters

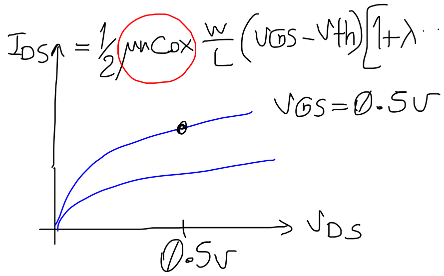
$V_{GS1} = V_{bias} - r.I_o$

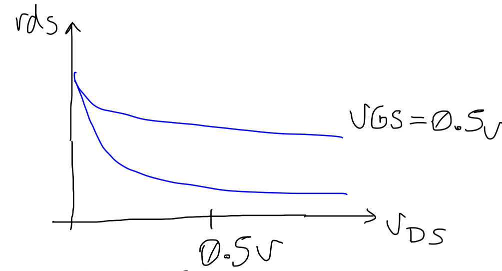


$\left\{ \begin{array}{l} g_m = \mu_n C_{ox}\frac{W}{L}V_{eff} \\ r_{ds} = \frac{1}{\lambda I_{DS}} \end{array} \right.$

* Note : Do not use transistor small-signal model during DC analysis

$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})[1+\lambda\cdots]$



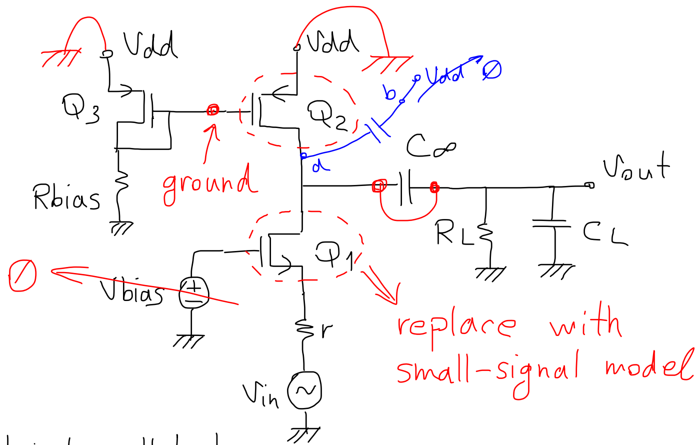


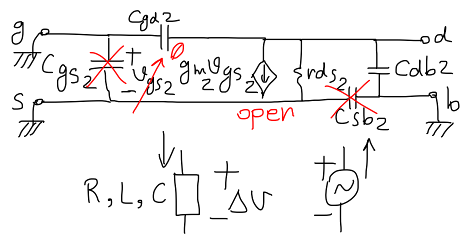
$r_{ds}\Big|_{\substack{V_{GS}=0.5V \\ V_{DS}=0.7V}} = \frac{1}{\lambda I_{DS}}$

$t_{ox}=2nm \Longrightarrow C_{ox} = \frac{\varepsilon_0\varepsilon_r}{t_{ox}}$ $\quad \varepsilon_0 = 8.854\times10^{-12}\,F/m$ $\quad 3.8<\varepsilon_r<4.2$

* AC analysis:

1. discard DC sources
2. short C_∞
3. replace transistors and current mirrors with their small-signal model



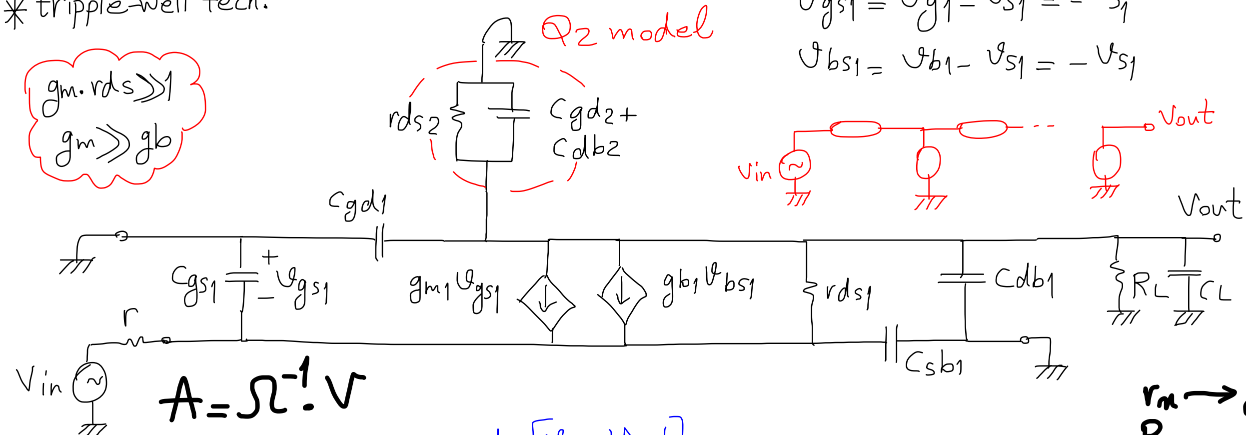


* tripple-well tech.

$g_m \cdot r_{ds} \gg 1$

$g_m \gg g_b$

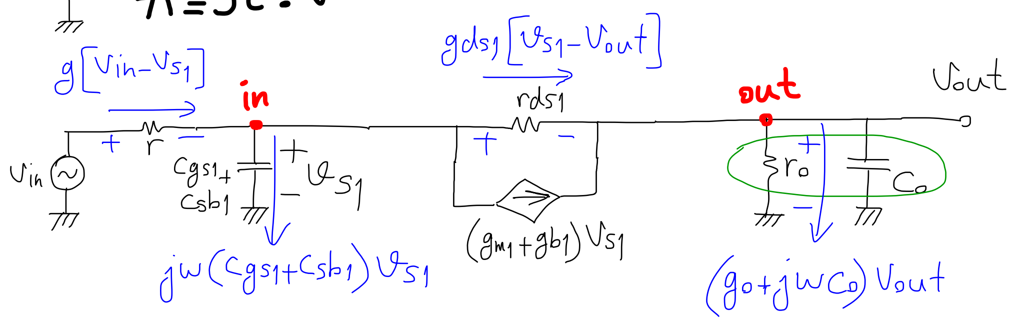
$$v_{gs1} = v_{g1} - v_{s1} = -v_{s1}$$
$$v_{bs1} = v_{b1} - v_{s1} = -v_{s1}$$



$$A = \Omega^{-1} \cdot V$$

$r_x \rightarrow g_x$

$R_x \rightarrow G_x$



$r_o = r_{ds2} \| R_L$

$C_o = C_{db1} + C_L + C_{gd2} + C_{db2} + C_{gd1}$

$$\text{KCL (in)}: \; g[V_{in} - V_{s1}] = jw(C_{gs1} + C_{sb1})V_{s1} + g_{ds1}[V_{s1} - V_{out}] + (g_{m1} + g_{b1})V_{s1} \quad \text{(EQ.1)}$$

$$\text{KCL (out)}: \; g_{ds}[V_{s1} - V_{out}] + (g_{m1} + g_{b1})V_{s1} = (g_o + jwC_o)V_{out} \quad \text{(EQ.2)}$$

$$\xRightarrow{\text{EQ.2}} V_{s1} = V_{out}\left[\frac{g_{ds1} + g_o + jwC_o}{g_{m1} + g_{b1} + g_{ds1}}\right] \quad \text{(EQ.3)}$$

$$\xRightarrow{\text{EQs.1,3}} g \cdot V_{in} = V_{out}\left[-g_{ds1} + \frac{g_{ds1} + g_o + jwC_o}{g_{m1} + g_{b1} + g_{ds1}}\left(g + g_{ds1} + g_{m1} + g_{b1} + jw(C_{gs1} + C_{sb1})\right)\right]$$

$$\Longrightarrow g \cdot V_{in} = V_{out}\left[-g_{ds1} + \frac{g_{ds1}+g_o+j\omega C_o}{g_{m1}+g_{b1}+g_{ds1}}\left(g+g_{ds1}+g_{m1}+g_{b1}+j\omega(C_{gs1}+C_{sb1})\right)\right]$$

$$\Longrightarrow \frac{V_{out}}{V_{in}} = \frac{g(g_{m1}+g_{b1}+g_{ds1})}{-g_{ds1}(g_{m1}+g_{b1}+g_{ds1}) + (g_{ds1}+g_o)(g+g_{ds1}+g_{m1}+g_{b1}) + j\omega\left[(g_{ds1}+g_o)(C_{gs1}+C_{sb1}) + C_o(g+g_{ds1}+g_{m1}+g_{b1})\right] + (j\omega)^2\left[C_o(C_{gs1}+C_{sb1})\right]}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{\overbrace{g(g_{m1}+g_{b1}+g_{ds1})}^{K1}}{\underbrace{g_{ds1}\cdot g + g_o(g+g_{ds1}+g_{m1}+g_{b1})}_{K2} + j\omega\Big[\underbrace{(g_{ds1}+g_o)(C_{gs1}+C_{sb1}) + C_o(g+g_{ds1}+g_{m1}+g_{b1})}_{K3}\Big] + (j\omega)^2\Big[\underbrace{C_o(C_{gs1}+C_{sb1})}_{K4}\Big]}$$

$\div$ $\div$ $\div$

$$\boxed{\frac{V_{out}}{V_{in}} = \frac{A_{v0}\left(1 \pm j\frac{\omega}{\omega_z}\right)}{\left(1+j\frac{\omega}{\omega_{p1}}\right)\left(1+j\frac{\omega}{\omega_{p2}}\right)} = \frac{A_{v0}}{1+j\omega\left[\frac{1}{\omega_{p1}}+\cancel{\frac{1}{\omega_{p2}}}\right] + (j\omega)^2\frac{1}{\omega_{p1}}\times\frac{1}{\omega_{p2}}}}$$

ignore

* Common Gate Amplifiers do not have zero frequency

$$A_{v0} = \frac{K1}{K2} = \frac{g(g_{m1}+\cancel{g_{b1}}+\cancel{g_{ds1}})}{g_{ds1}\cdot g + g_o(g+\cancel{g_{ds1}}+g_{m1}+\cancel{g_{b1}})} = \frac{g\cdot g_{m1}}{g\cdot g_{ds1} + \cdots}$$

$$g_o(g+g_{m1})$$

$$\omega_{p1} = \frac{K2}{K3}$$

$$\omega_{p2} = \frac{K3}{K4}$$

for a good PDK:

$$\begin{cases} g_m r_{ds} \gg 1 \\ g_m \gg g_b \end{cases}$$

$g_o = g_{ds2} + G_L$

$r_o = r_{ds2} \| R_L$

$a \| b = \frac{1}{a} + \frac{1}{b}$

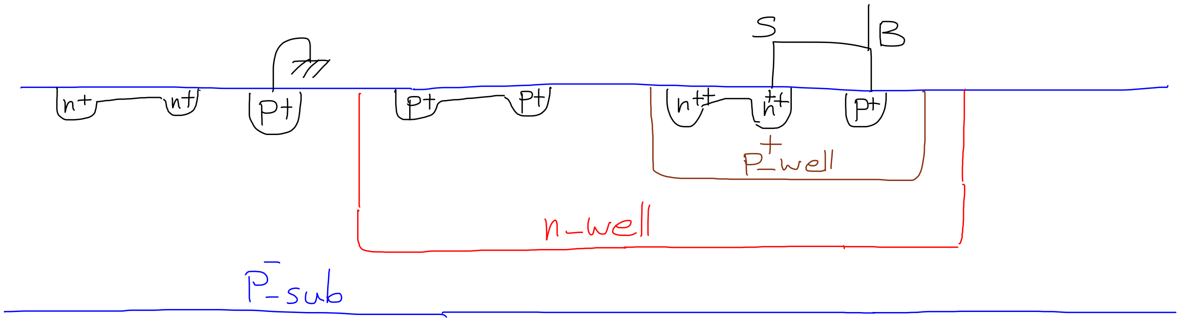
$a + b = \frac{1}{a} \| \frac{1}{b}$

$$A_{v0} = \frac{g\cdot g_{m1}}{\underbrace{g\cdot g_{ds1} + g\cdot g_o}_{g[g_{ds1}+g_{ds2}+G_L]} + g_{m1}g_o}$$

if $r \approx 0 \Rightarrow g \to \infty \Longrightarrow$

$$A_{v0} \approx \frac{g_{m1}}{g_{ds1}+g_{ds2}+G_L} = g_{m1}(r_{ds1}\|r_{ds2}\|R_L)$$

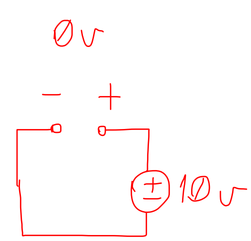
(non-inverting)



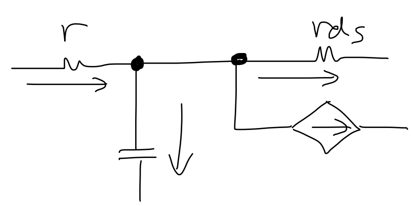
triple-well technology

$$\begin{cases} a_1 x_1 + a_2 x_2 + a_3 x_3 = k_1 \\ b_1 x_1 + b_2 x_2 + b_3 x_3 = k_2 \\ c_1 x_1 + c_2 x_2 + c_3 x_3 = k_3 \end{cases}$$

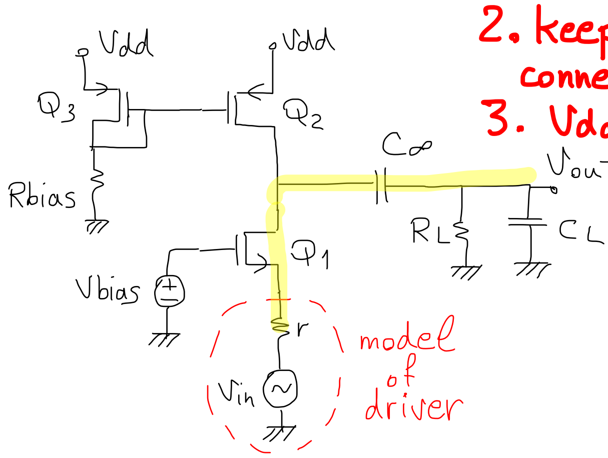
$$x_1 = \frac{\begin{vmatrix} k_1 & a_2 & a_3 \\ k_2 & b_2 & b_3 \\ k_3 & c_2 & c_3 \end{vmatrix}}{\begin{vmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ c_1 & c_2 & c_3 \end{vmatrix}}$$



$$x_1 = \frac{\begin{vmatrix} a_1 & k_1 & a_3 \\ b_1 & k_2 & b_3 \\ c_1 & k_3 & c_3 \end{vmatrix}}{\begin{vmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ c_1 & c_2 & c_3 \end{vmatrix}}$$



nmos C.G.



Rules :

1. nmos ⟷ pmos
2. keep the same connectivity
3. Vdd ⟷ gnd

pmos C.G.