Texas A&M University
Electrical Engineering Department

ECEN 665

Laboratory #3: Analysis and Simulation of a CMOS LNA

Objectives: To learn the use of s-parameter and periodic steady state (pss) simulation tools in spectre (cadence) in the characterization of the major figures of merit of an LNA: input and output match, noise figure, gain and IIP3. To understand the basic operation of a cascode CMOS LNA and analyze its performance trade-offs.
Cadence Simulator : In this and all the following lab exercises, we will use **Spectre** simulator of Cadence. Please ask your TA how to gain access to Spectre compatible model files.

1. Schematic setup

Using a library for CMOS 0.5um technology in cadence, create the schematic shown in figure 1. This is a well known cascode LNA topology with an output buffer to provide output impedance match. The component values are shown in tables 1-3.

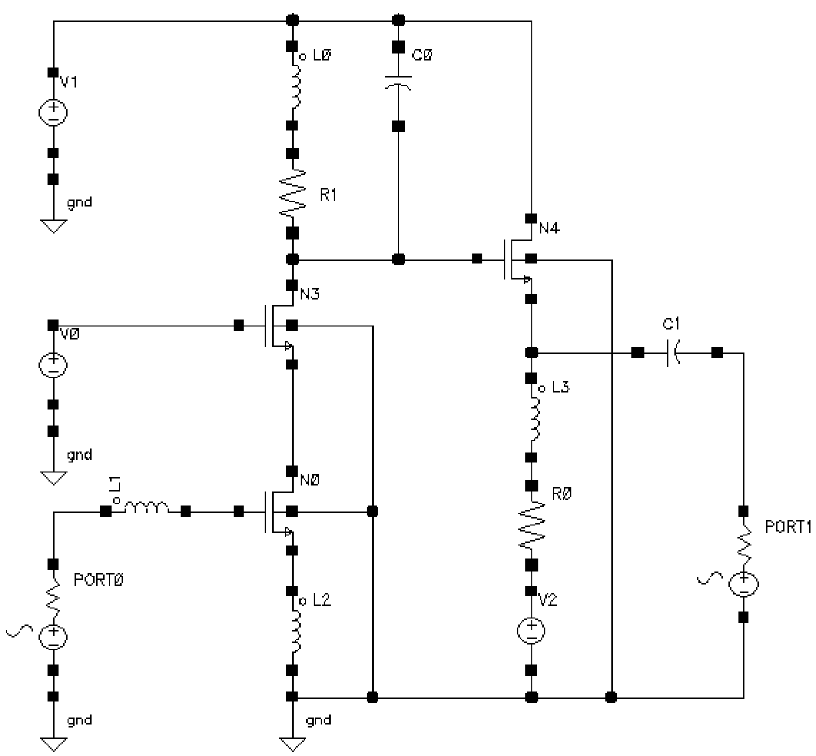

Figure 1. Cascode LNA schematic

Table 1. Transistor parameters

Transistor	W [um]	L [um]	Multiplicity
N0	24	0.6	10
N3	12	0.6	10
N4	9	0.6	10

Table 2. Component values

Component	Value
L0	6 nH
L1	16nH
L2	1nH
L3	20nH
R0	15ohm
R1	8.4 ohm
C0	900fF
C1	4pF
V0	2.8V
V1	3.5V
V2	0.8V

Table 3. Port parameters

Parameter	PORT0	PORT1
Cell name	psin	Psin
Frequency Name	F1	
Resistance	50ohms	50ohms
Port number	1	2
DC voltage	0.5V	
Source type	Sine	
Amplitude (dBm)	PRF	
Frequency	1.9GHz	
AC magnitude	1	

1.1 Briefly describe the role of each transistor and passive component in the LNA.

1.2 Describe in general terms, how is the input and output match implemented in this design.

1.3 Would the output buffer (transistor N4) and/or the output matching network to 50ohm be needed if the load of the LNA was a Mixer on the same chip? Explain.

2. S parameter simulation

S-parameter simulation will be used to measure the input and output match of the LNA as well as its small signal gain.

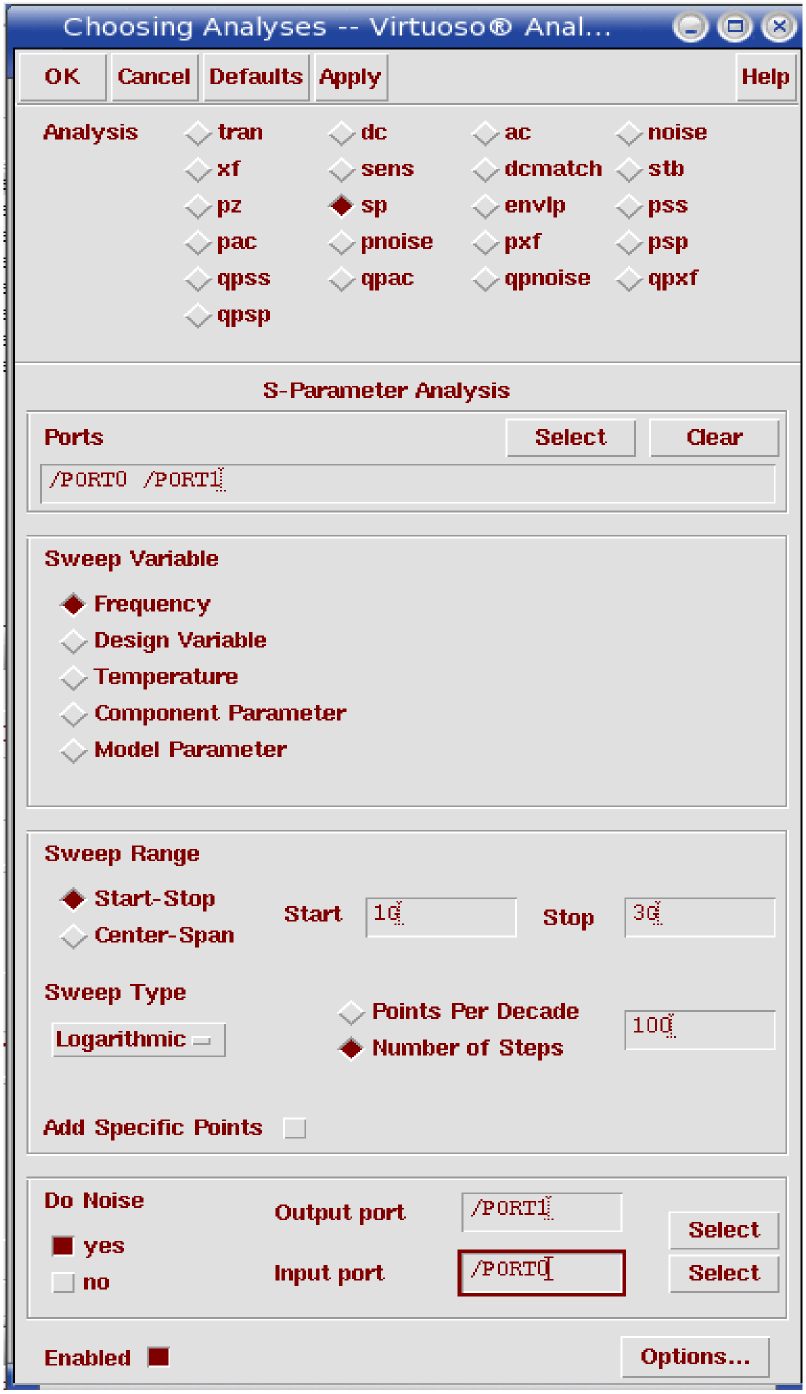

Figure 2. S-parameter simulation setup

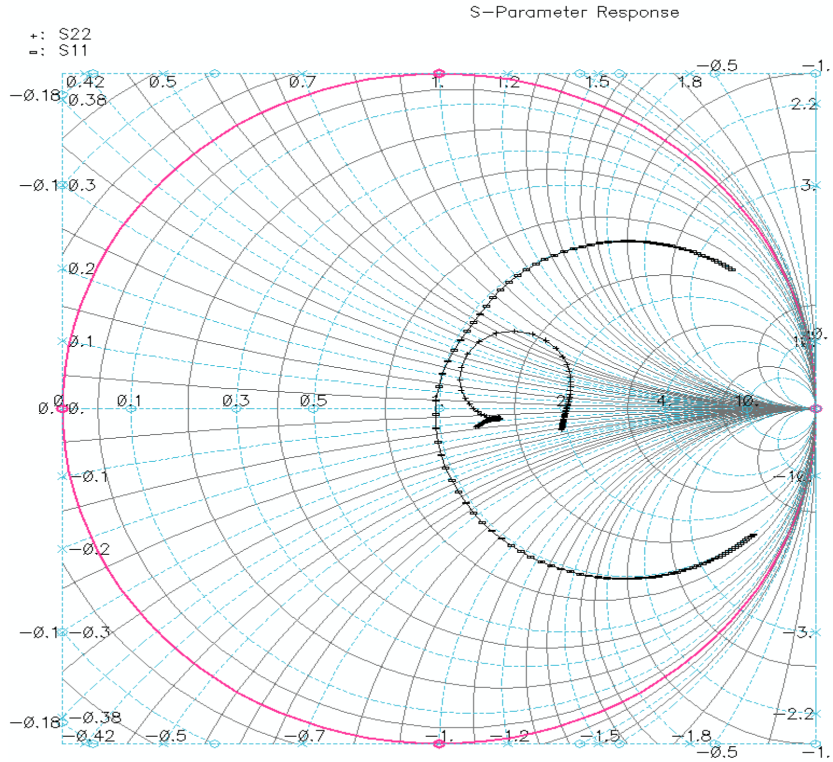

Figure 3. S11 and S22

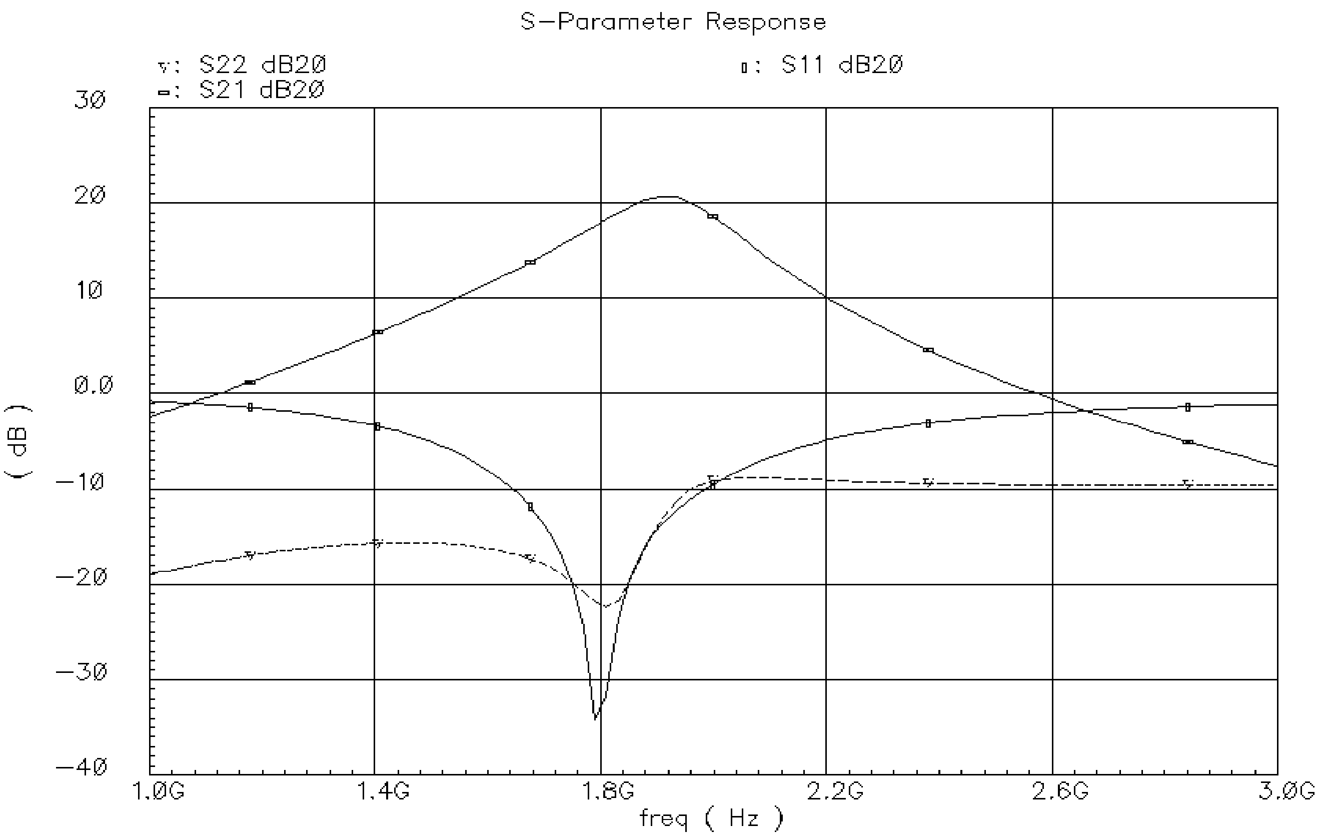

Figure 4. S-parameters for the 1.9GHz LNA

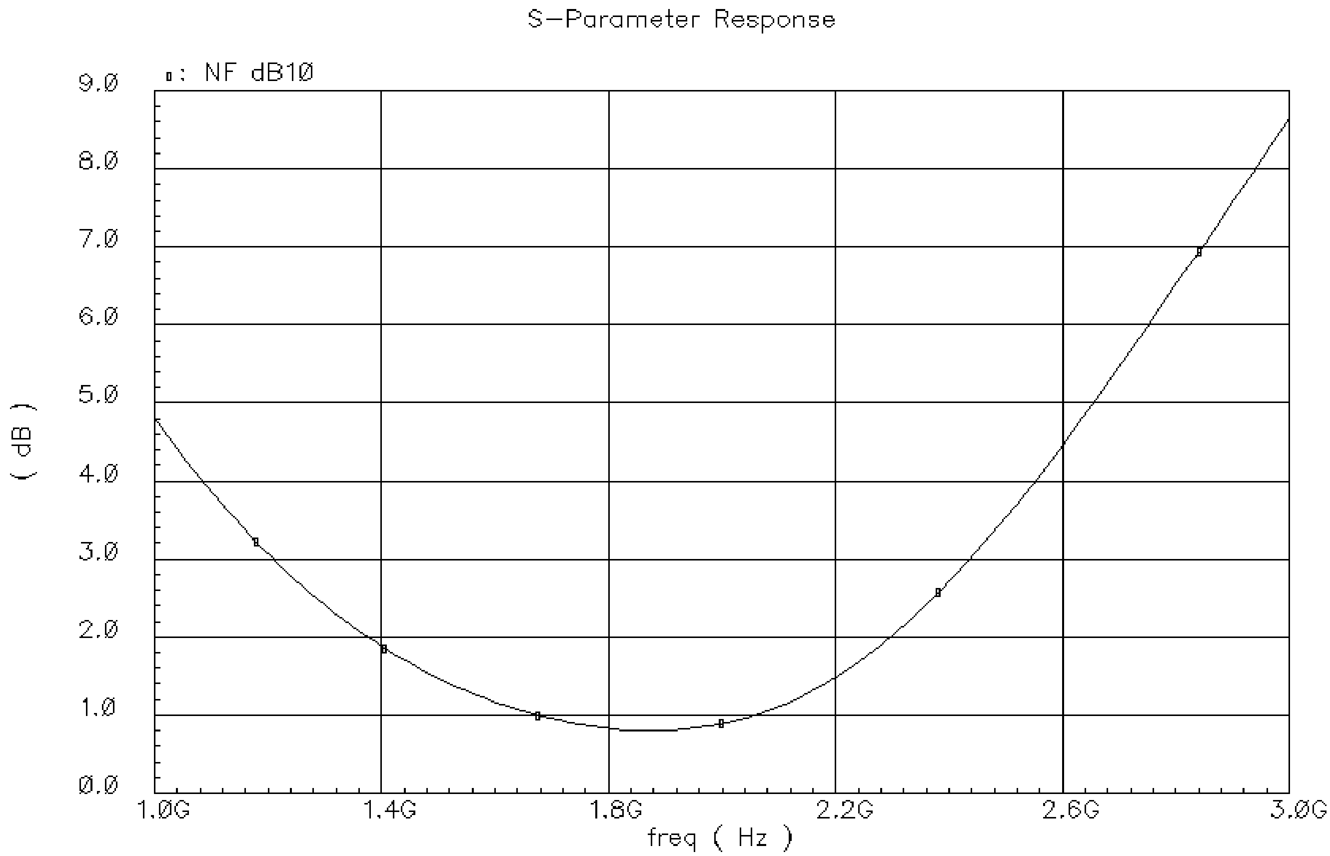

Figure 5. Noise figure (through s-parameter simulation) of the LNA

2.1 Run a DC Analysis and save the operating point. Display the operating point of transistor N0 and take note of its gm, vgs and cgs. Using these values calculate the theoretical gain, noise figure and input impedance of the LNA. Are the calculated values different from the S-parameter simulation results? Explain the differences. (Set PRF to -20dBm)

3. PSS simulation

A periodic steady-state analysis provides an accurate simulation of the transient behavior of a circuit. For the non-linear characterization of the LNA this is a preferred simulation method over the conventional transient analysis.

3.1 Single tone simulation

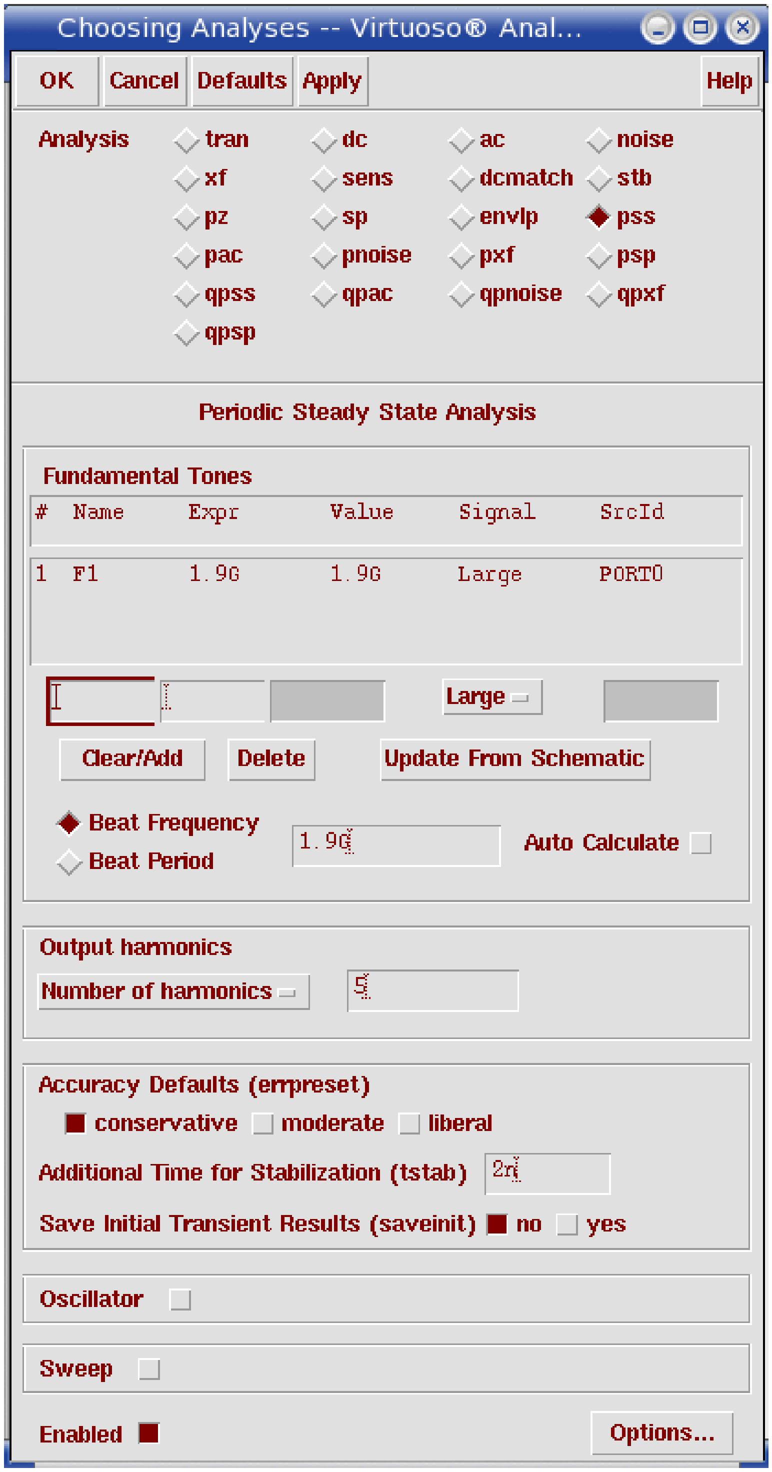

Figure 6. PSS simulation setup

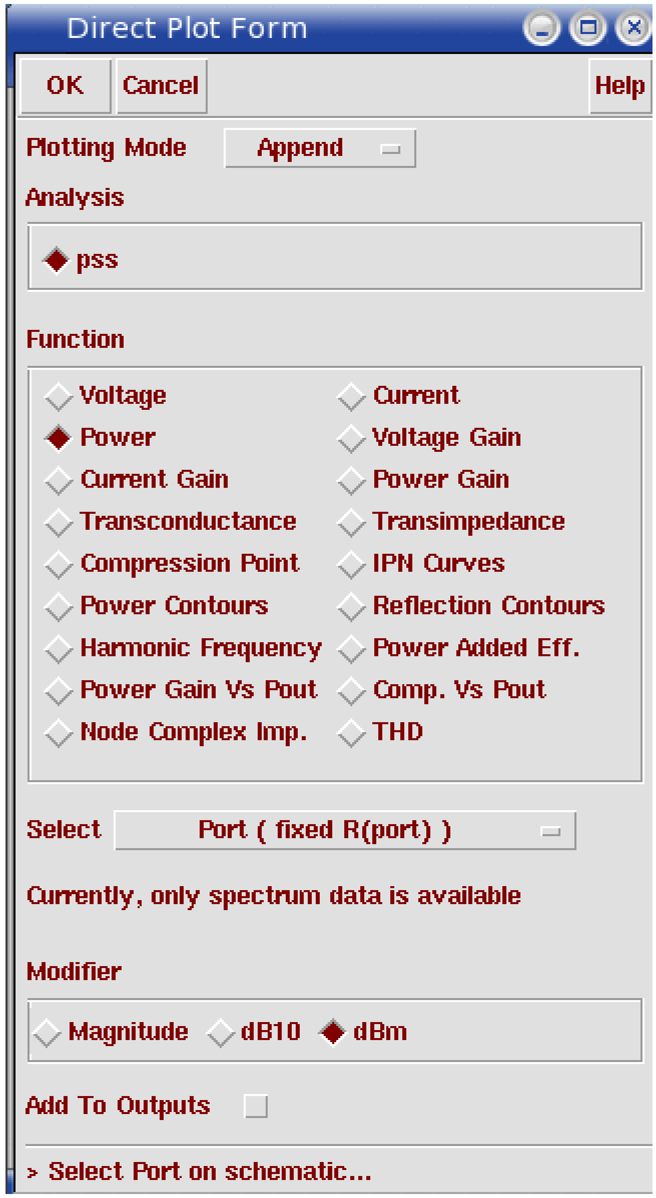

Figure 7. PSS results setup

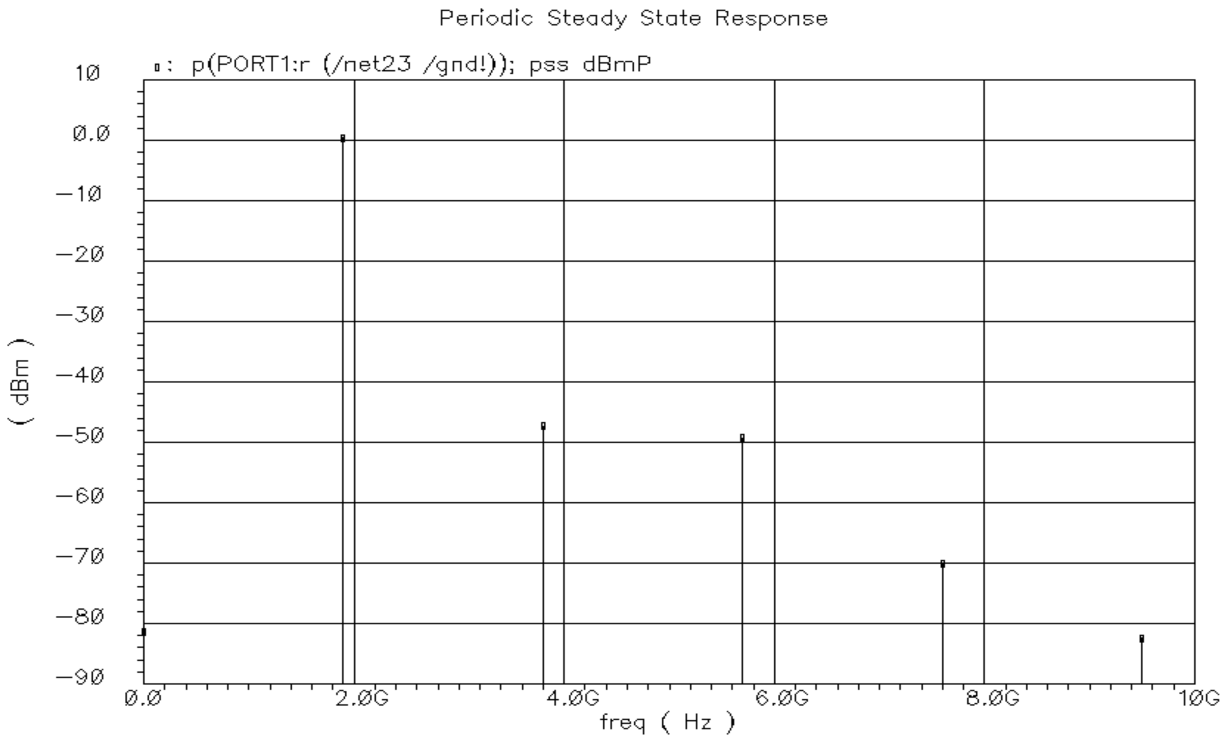

Figure 8. Output spectrum for a -20dBm 1.9GHz input

3.11 What is the power gain of the LNA for the fundamental tone? What is the HD2 and HD3? How do these 3 parameters change for an input of -40dBm and -5dBm?

3.2 Two tone simulation

PSS can also be employed for a two-tone test of the LNA. For this purpose, change the setting of the input port according table 4 and the pss setup according to figure 9. Notice that the input tones and the expected intermodulation products are the selected harmonics for the simulation.

Table 4. Port 1 parameters

Parameter	PORT0
Cell name	psin
Frequency name	F1
Second frequency name	F2
Resistance	50ohms
Port number	1
DC voltage	0.5V
Source type	Sine
Amplitude (dBm)	PRF
Frequency	1.85GHz
Amplitude 2 (dBm)	PRF
Frequency 2	1.95GHz
AC magnitude	1

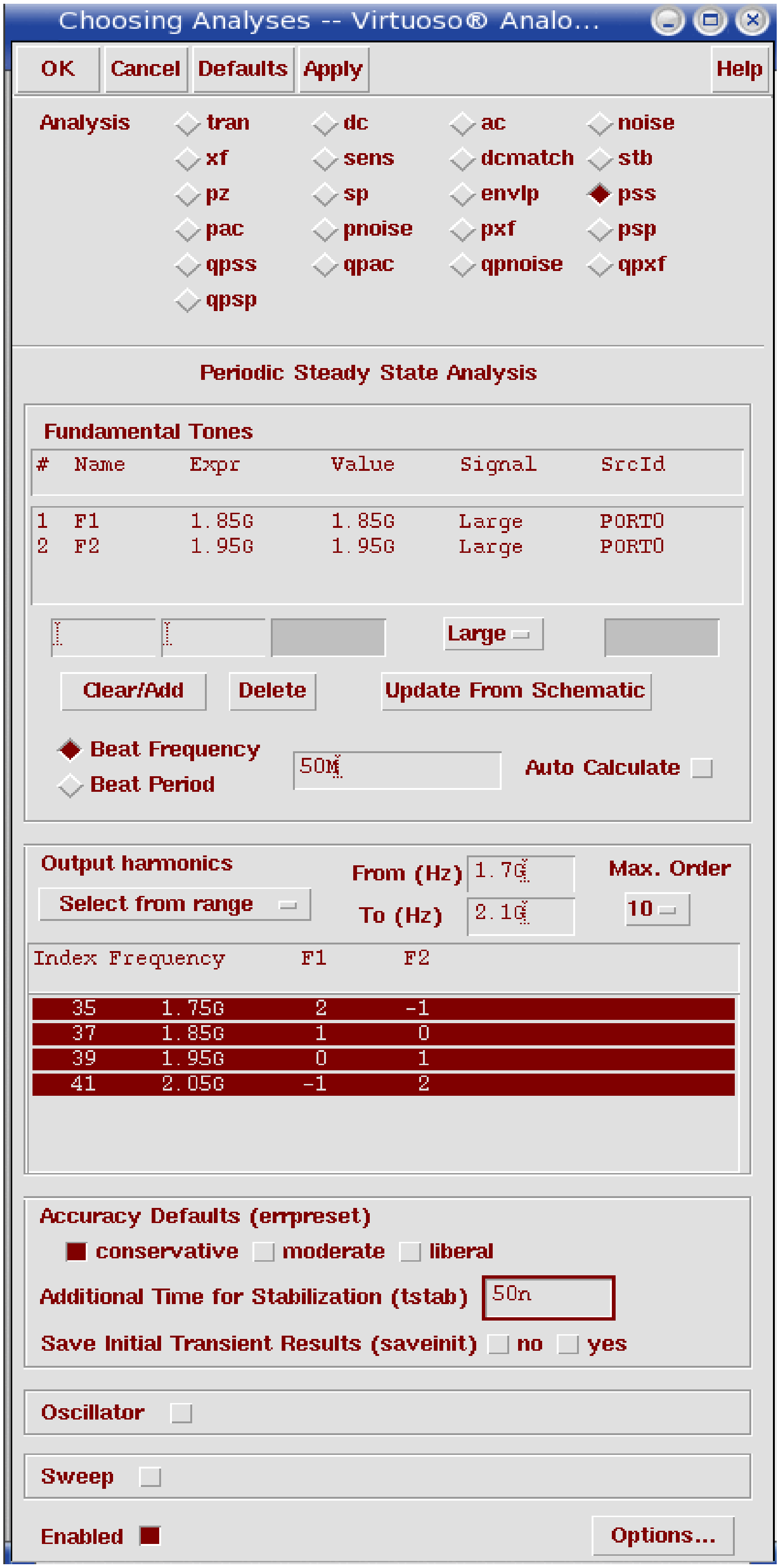

Figure 9. PSS simulation setup for a two tone test

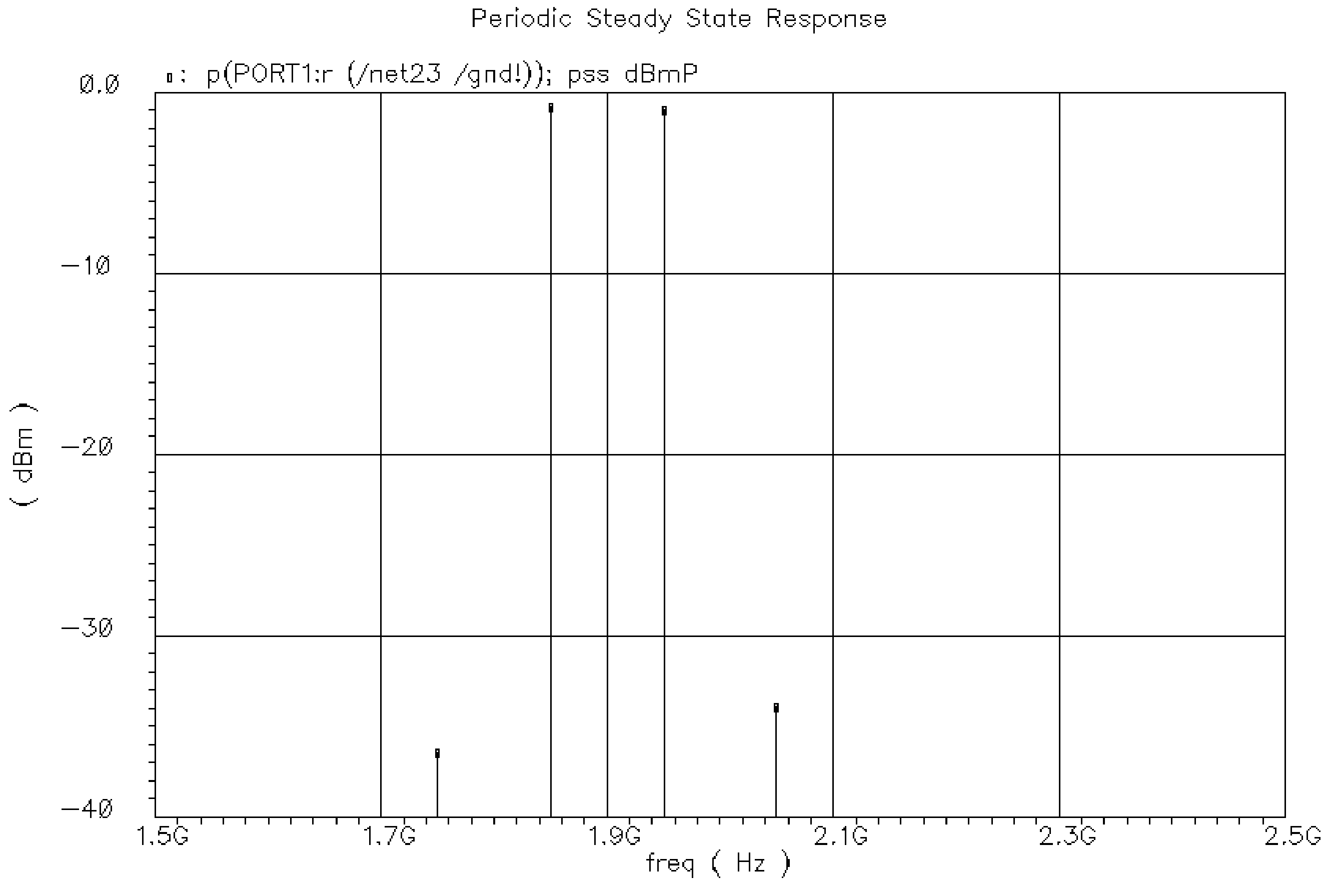

Figure 10. Two tone test output using PSS

3.21 From the PSS simulation results, what is the IIP3 of this LNA?

4. SPSS simulation

The swept periodic steady state (SPSS) is used to analyze the steady state transient behavior of the LNA while sweeping a certain design variable, for example the input power. In Spectre, SPSS is performed through PSS where Sweep option is enabled.

4.1 Single tone simulation

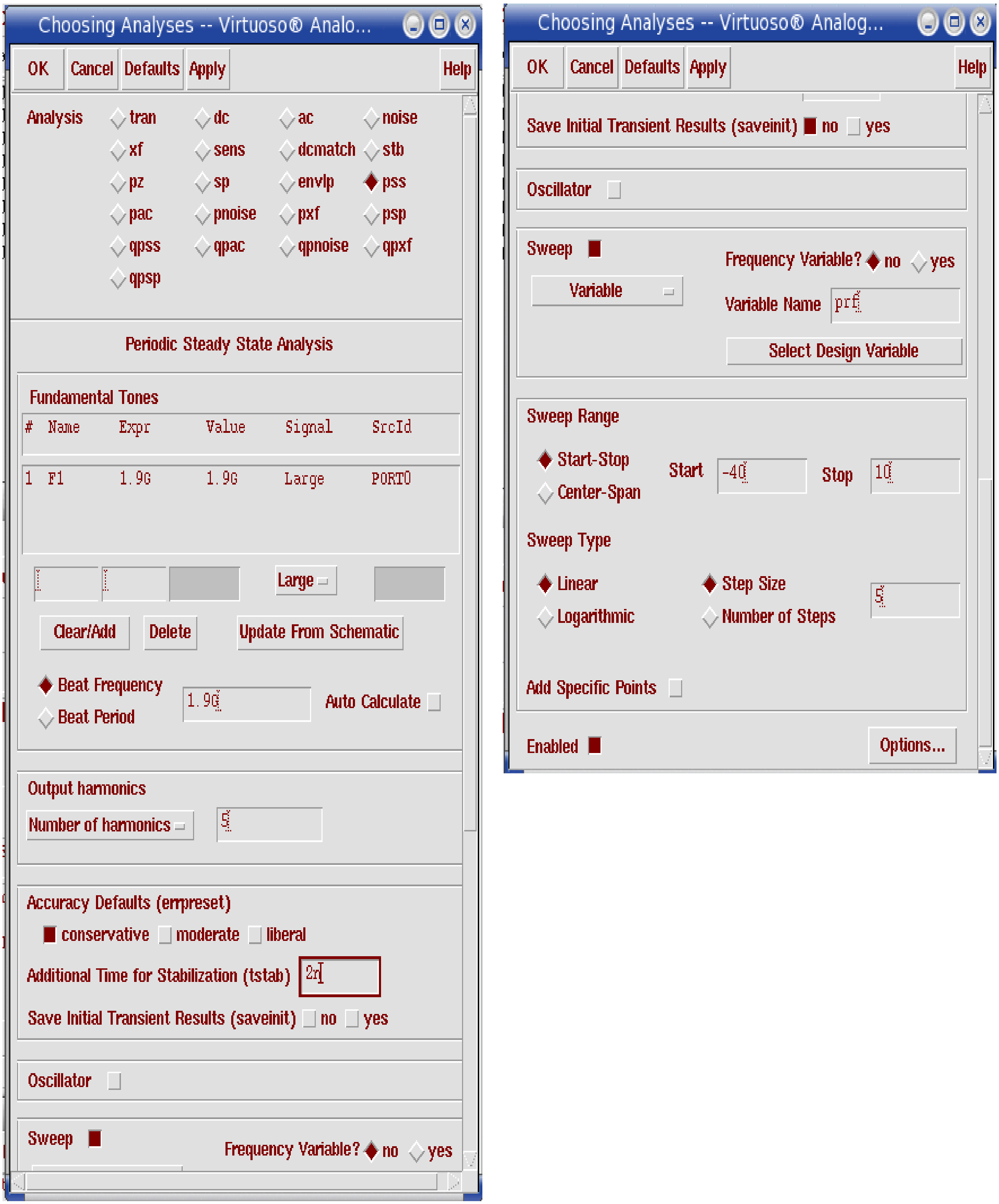

Figure 11. SPSS single tone simulation setup

Figure 12. SPSS single tone results setup for 1dB compression point (left) and voltage gain (right)

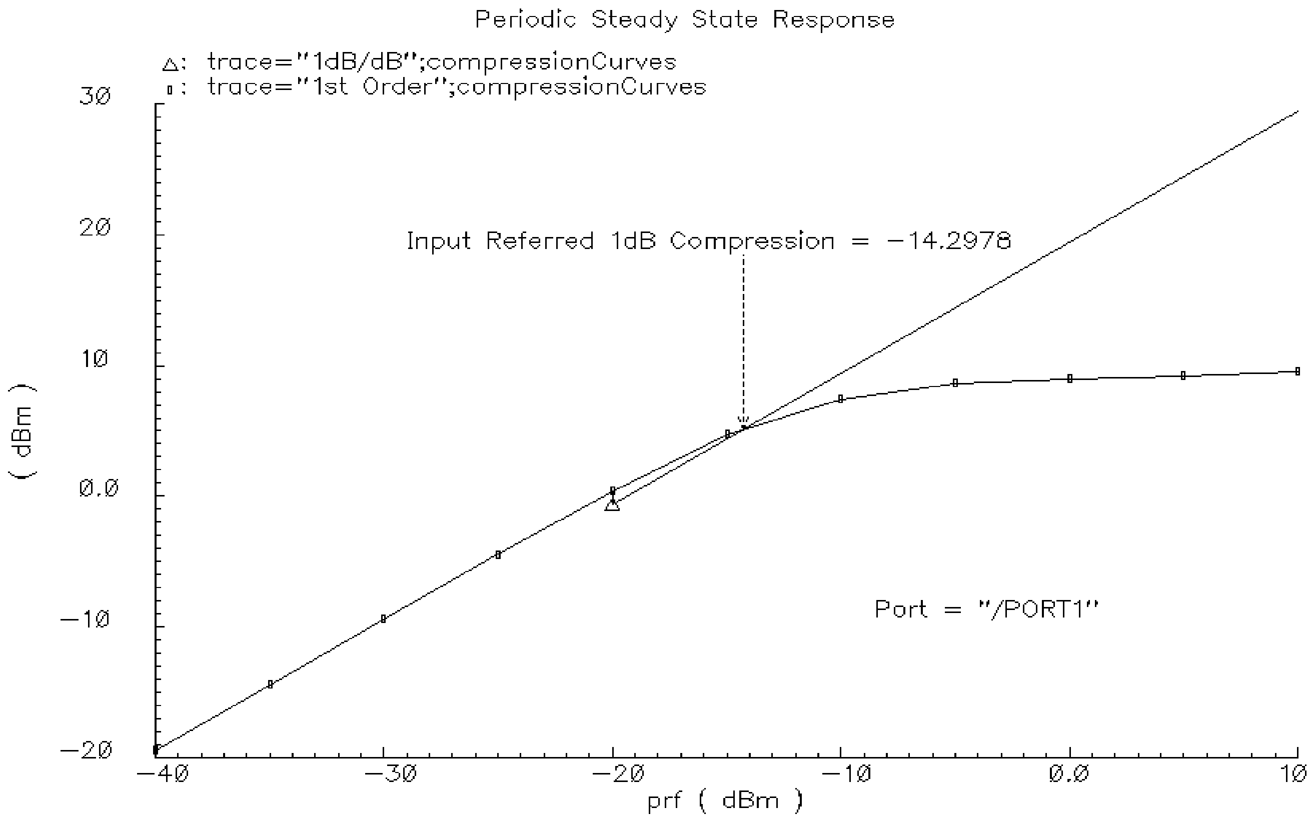

Figure 13. Input 1dB compression point

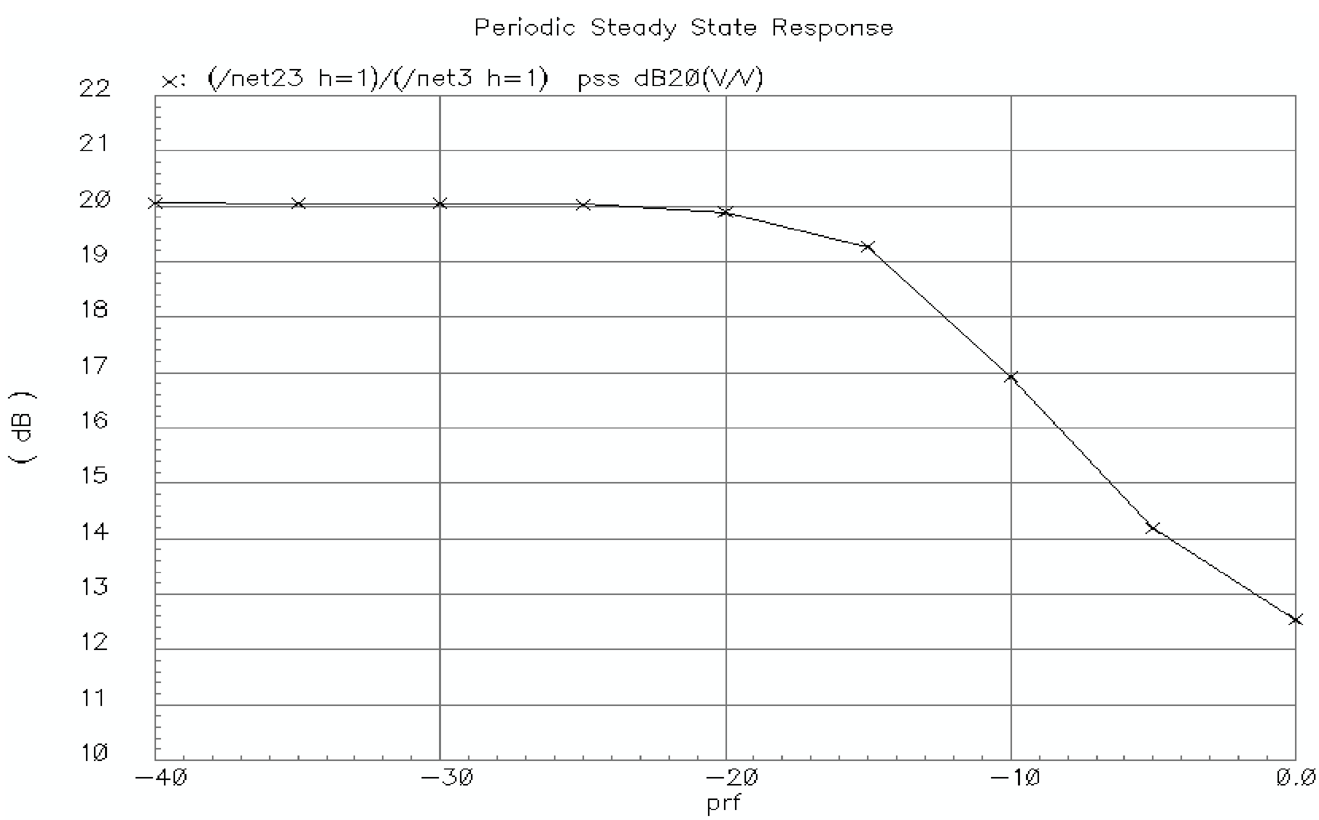

Figure 14. Gain Vs. Input power

4.2 Two tone simulation

This simulation setup allows you to observe how the intermodulation products grow with the input power level.

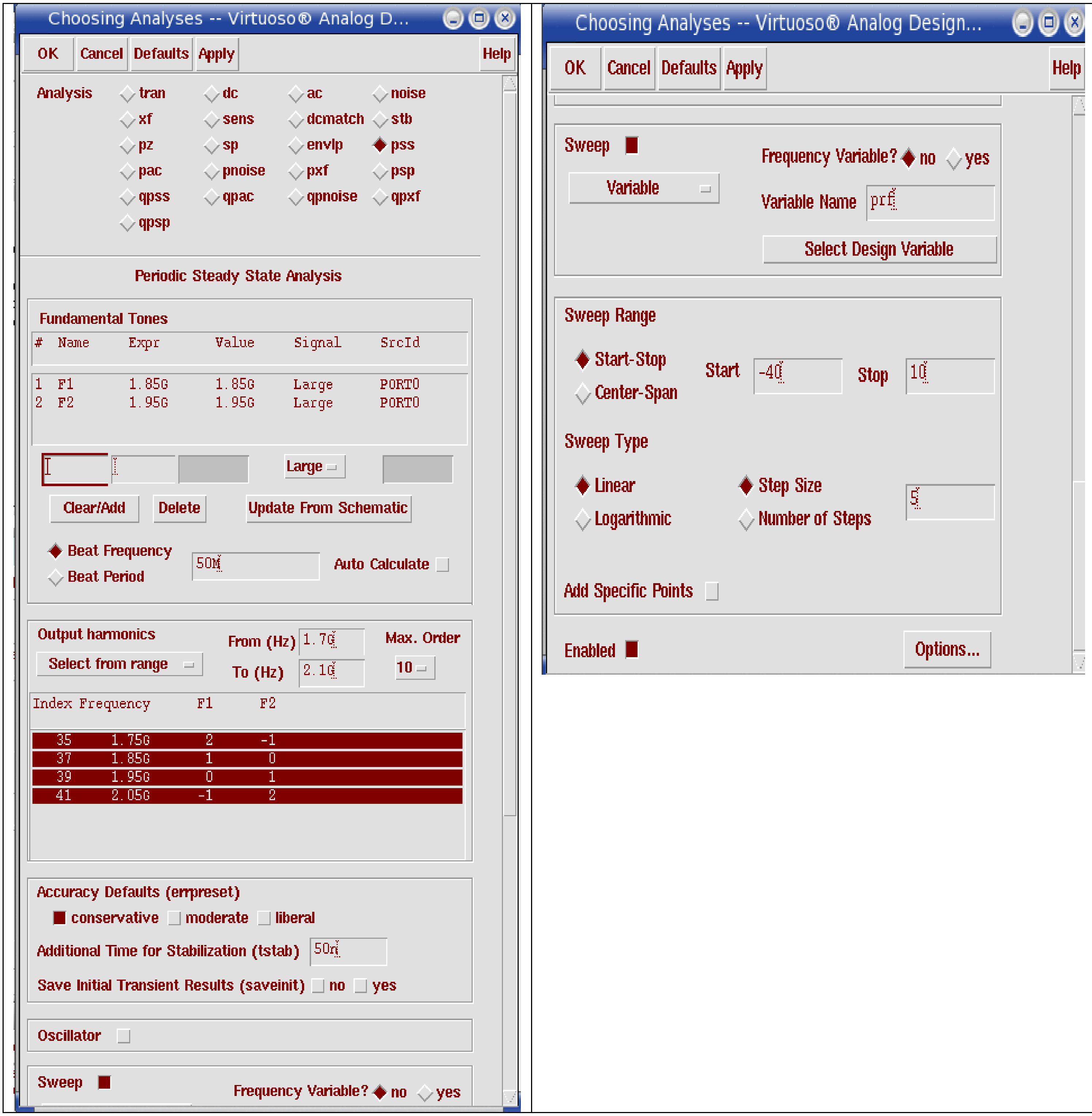

Figure 15. Two tone SPSS simulation setup

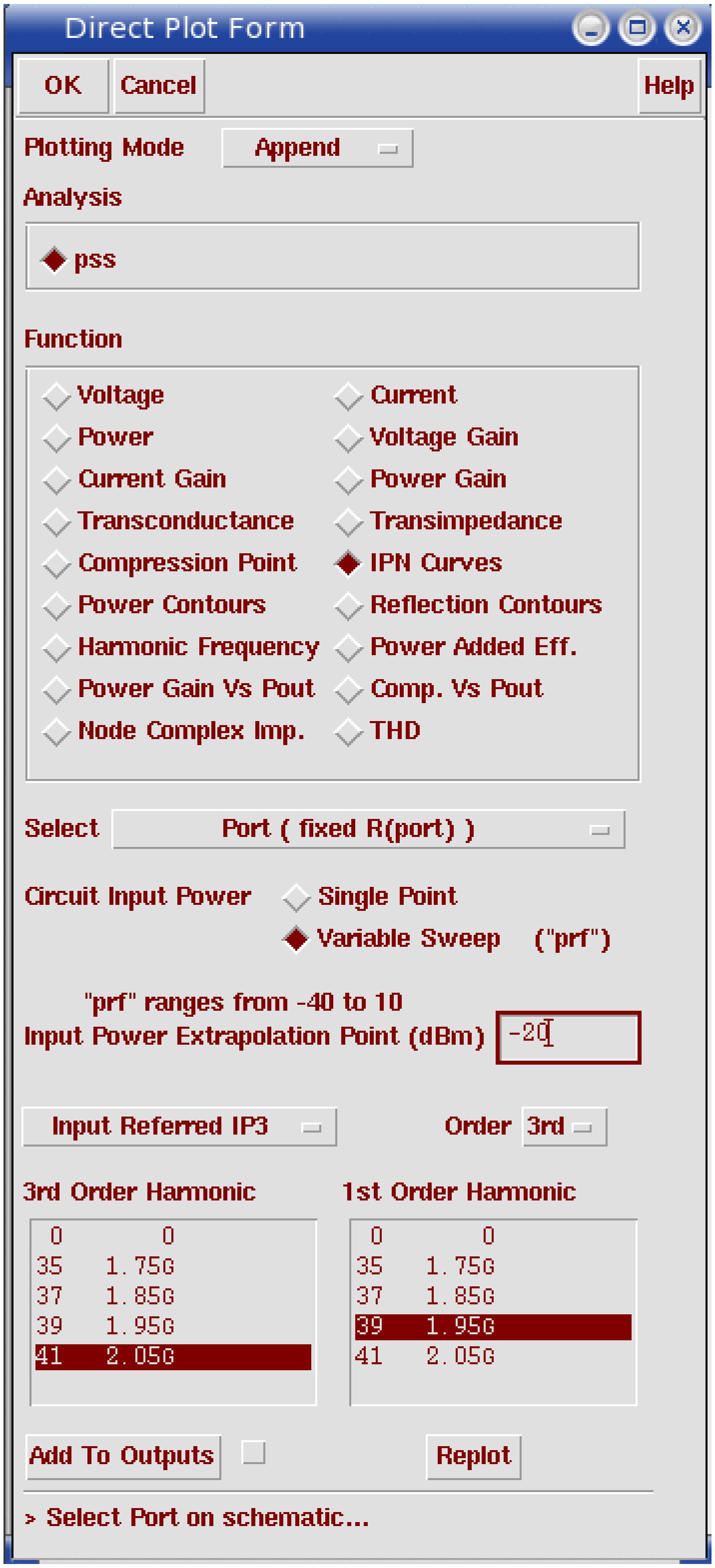

Figure 16. SPSS two tone results setup for output power and IIP3

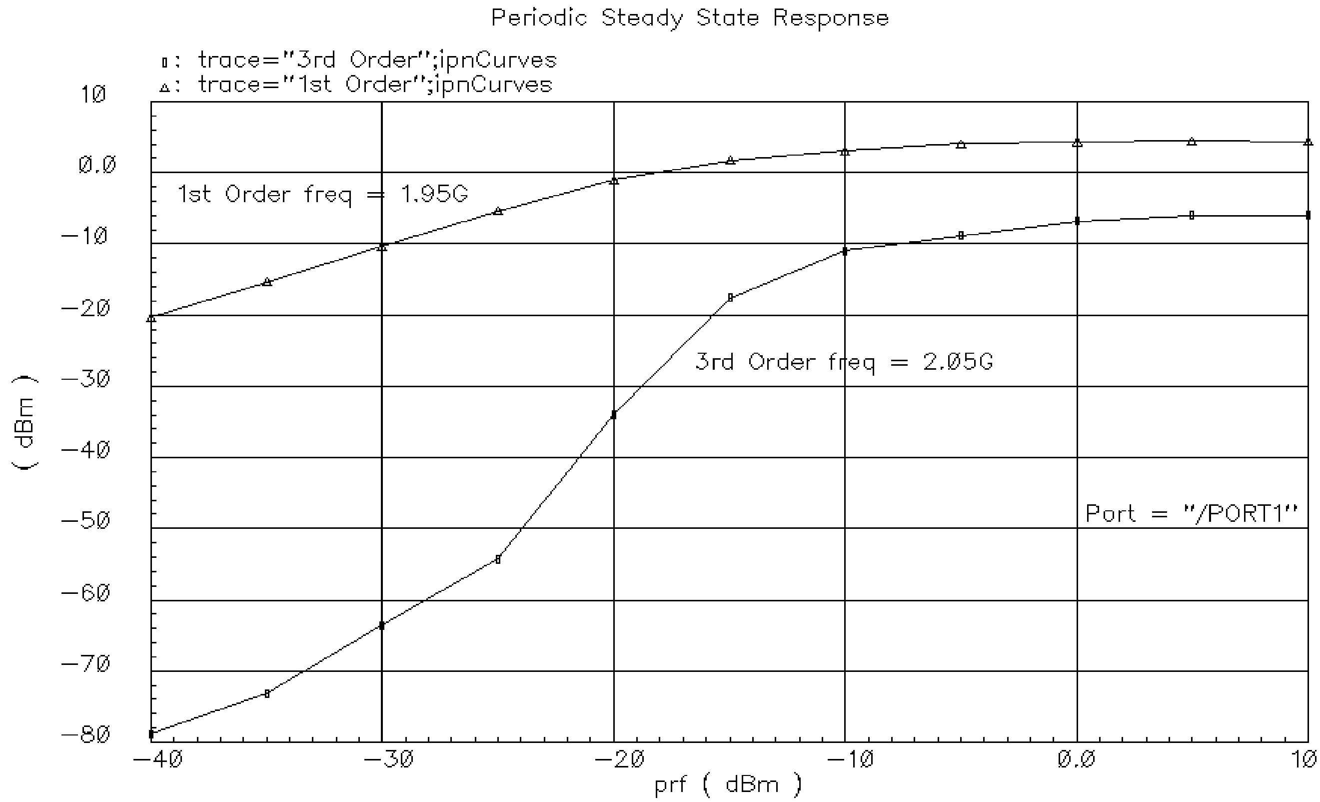

Figure 17. Main tones and intermodulation products

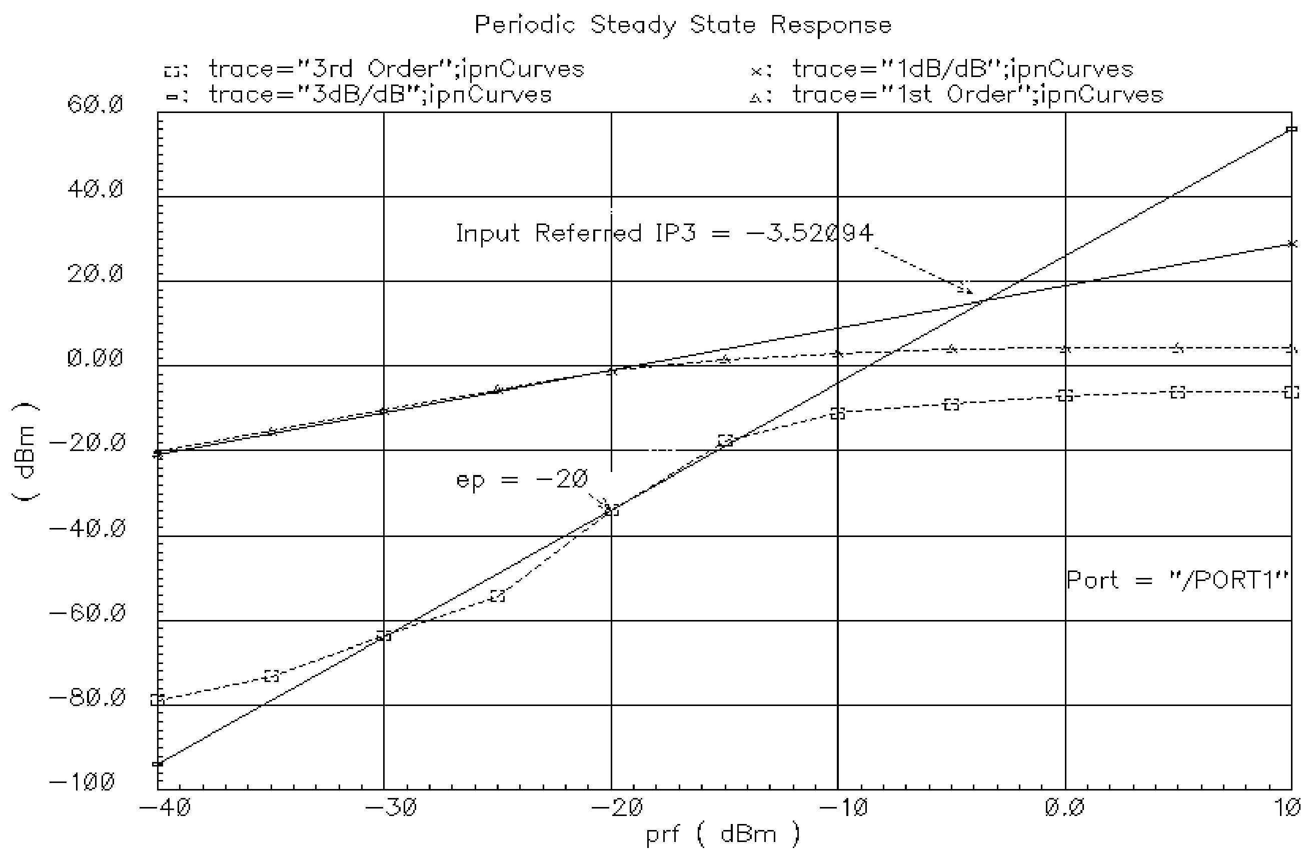

Figure 18. Extrapolated IIP3

4.21 How does the extrapolated IIP3 compare with your calculation from 3.21? Is the difference between the 1dB compression point and the IIP3 what you would expect?

4.22 The IIP3 of a cascode LNA can be estimated from the Vdsat of the input transistor and other parameters. Calculate the IIP3 and compare it with your simulation results.

4.23 Change the gate bias voltage of the cascode transistor (V0) to 2.3 V. What is the IIP3 now? Bring back this voltage to 2.8V and reduce the power supply (V1) to 2.7V and V2 to 0V. What is the new IIP3? What can you conclude about the relation between the bias conditions of the LNA and its linearity?

5. LNA Design Trade-Offs

5.1 Include a resistor in series with L1 and L2 so that they have a Q factor of 10 @ 1.9GHz. How and why does the NF change? Change the LNA design to improve the new NF by 0.5dB while keeping the Q of the inductors as 10 (that is, you may change the inductance value but not the Q). Justify your changes and report the overall performance (S parameters, NF and IIP3) of your new LNA design.

5.2 Starting from the 'realistic' model of the LNA (original design with a Q factor of 10 in L1 and L2), propose a change in the design parameters to obtain an IIP3 of +6dBm while keeping S21>20dB. Justify your changes and report the overall performance (S parameters, NF and IIP3) of your new LNA design.

5.3 Write your own conclusions among the NF, IIP3 and S21 trade-offs in a CMOS cascode LNA.

6. Design of a "Realistic" LNA

Following the procedure from the class notes and based on what you learnt from the "idealistic LNA" in this lab, design a 1.9 GHz CMOS cascode LNA using "realistic" inductors in **0.35um** technology to comply with the following specifications:

s21>10dB, NF<3dB, IIP3>0dBm, S11<-12dB.

Design all of the required inductors using ASITIC and for your simulations, employ the distributed model that can be obtained from ASITIC with the command **pix.**

In your report, describe your design procedure and include the simulation results and design parameters for all of the components and inductors. Discuss the effect of using the distributed model for the inductors rather than the simplified series resistance model we used in part 5.

Final Remarks:
You have two weeks to complete this lab, the deadline for the submission of your reports for this lab is the lab session after two weeks.