EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 21: Pipelined ADC 3

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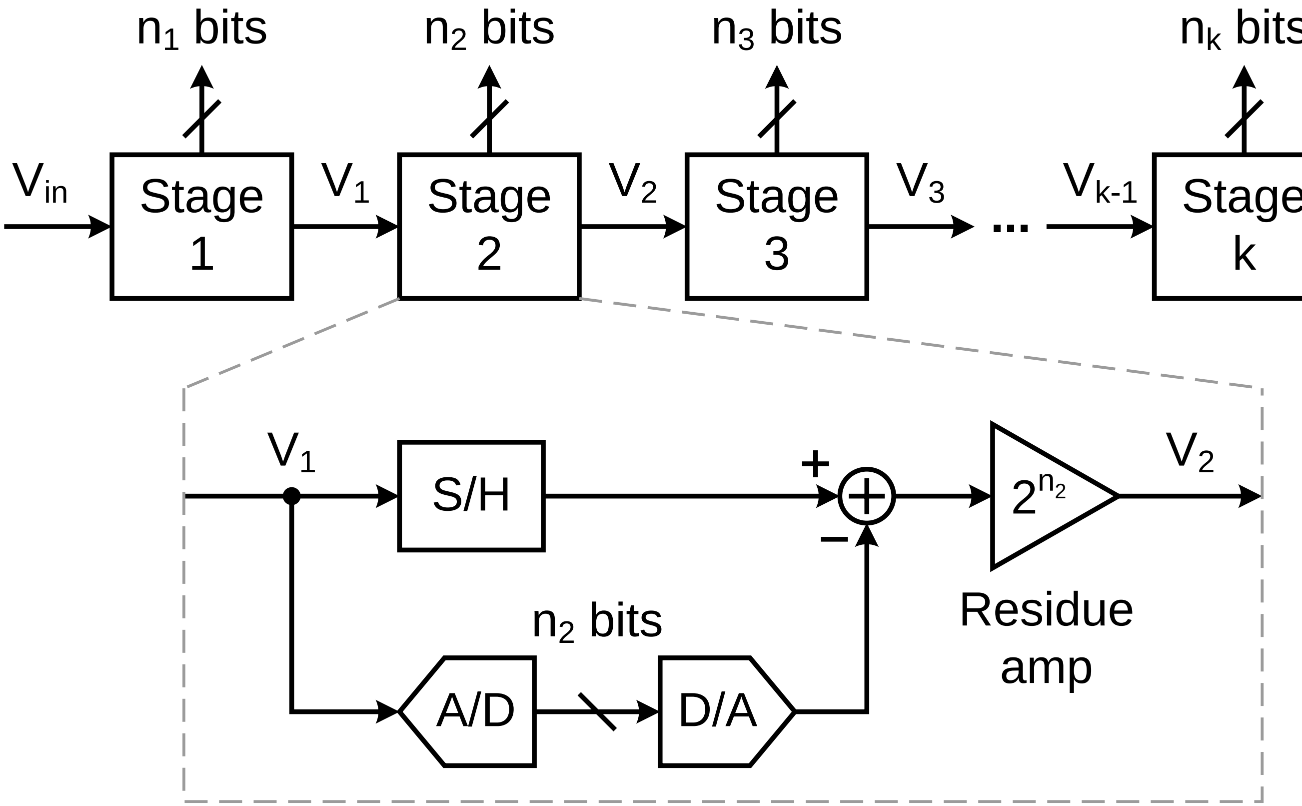
Agenda

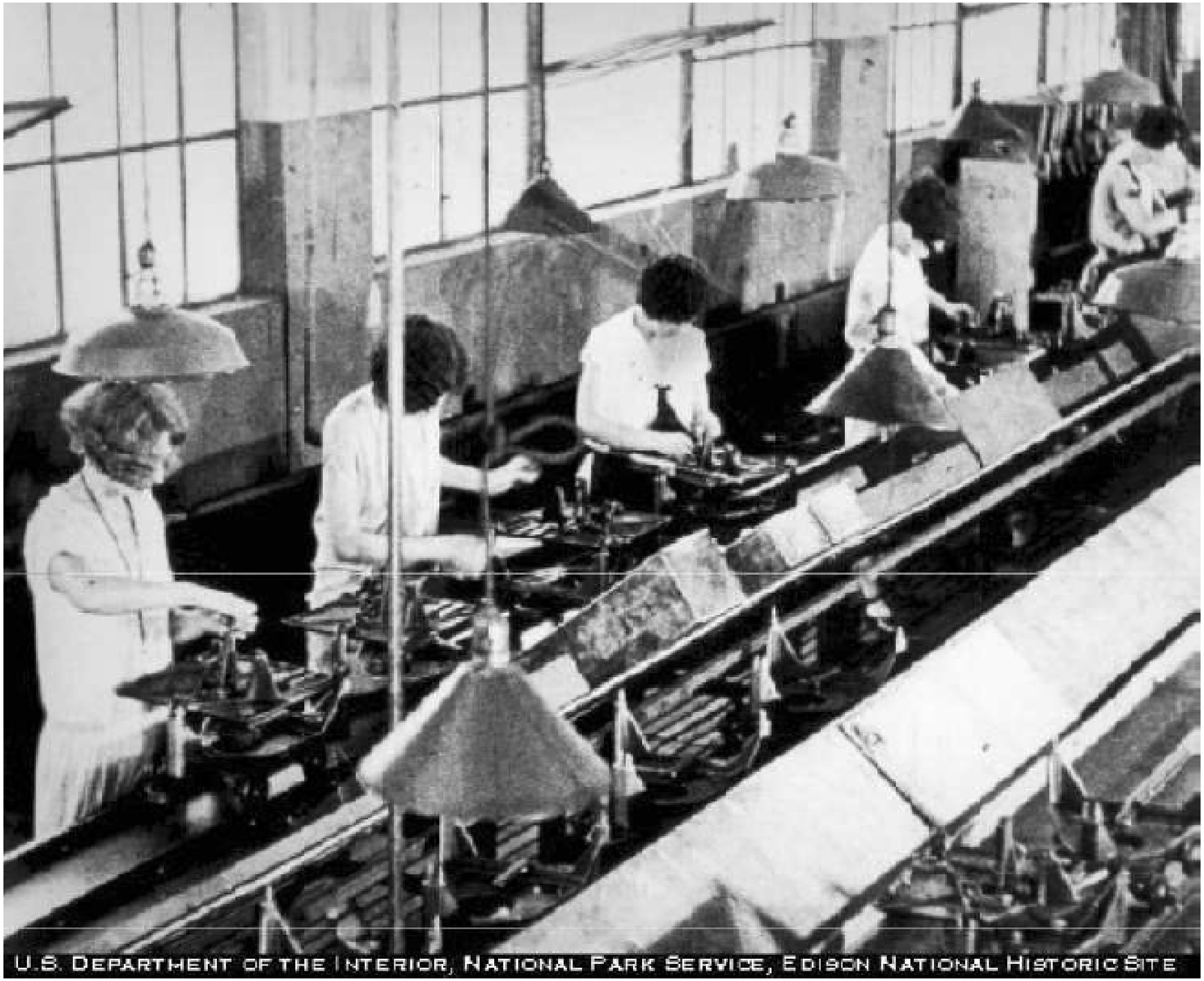
- Pipelined ADC Error Correction
  - Bit alignment
  - ADC Implementation Example

- OPAMP requirement
  - Gain
  - Bandwidth

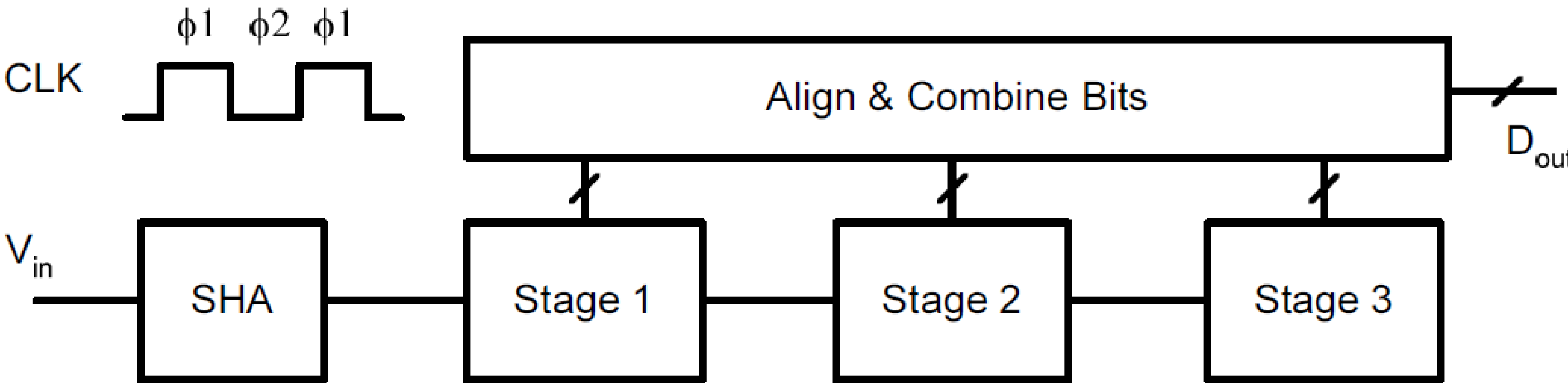
Pipelined ADC



Pipelining – Old Idea



Pipelined ADC

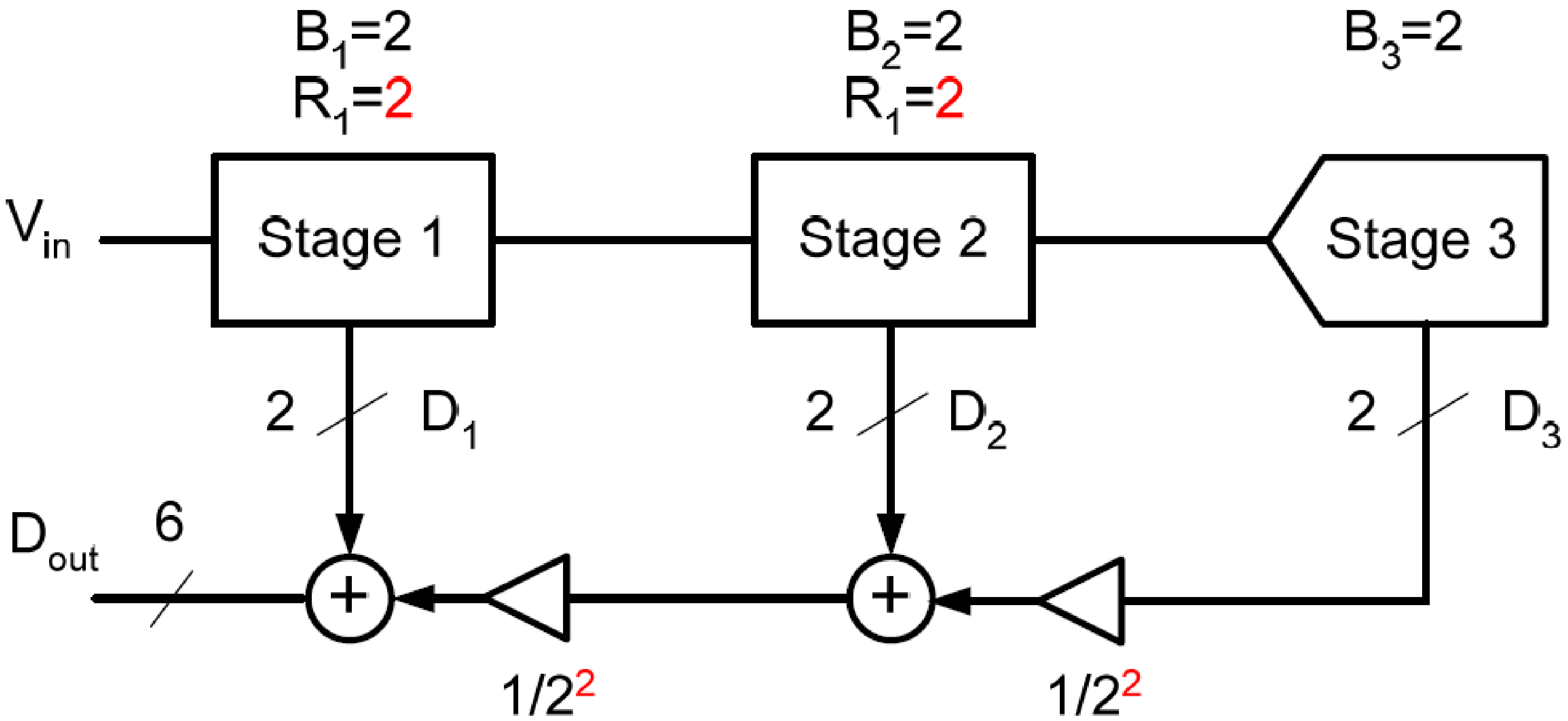


$\phi 1$	ACQUIRE	CONVERT	ACQUIRE	CONVERT
$\phi 2$	BUFFER	ACQUIRE	CONVERT	ACQUIRE

- Stages operate on the input signal like a shift register
- New output data every clock cycle, but each stage introduces ½ clock cycle latency

Combining the Bits

- Example1: Three 2-bit stages, no redundancy

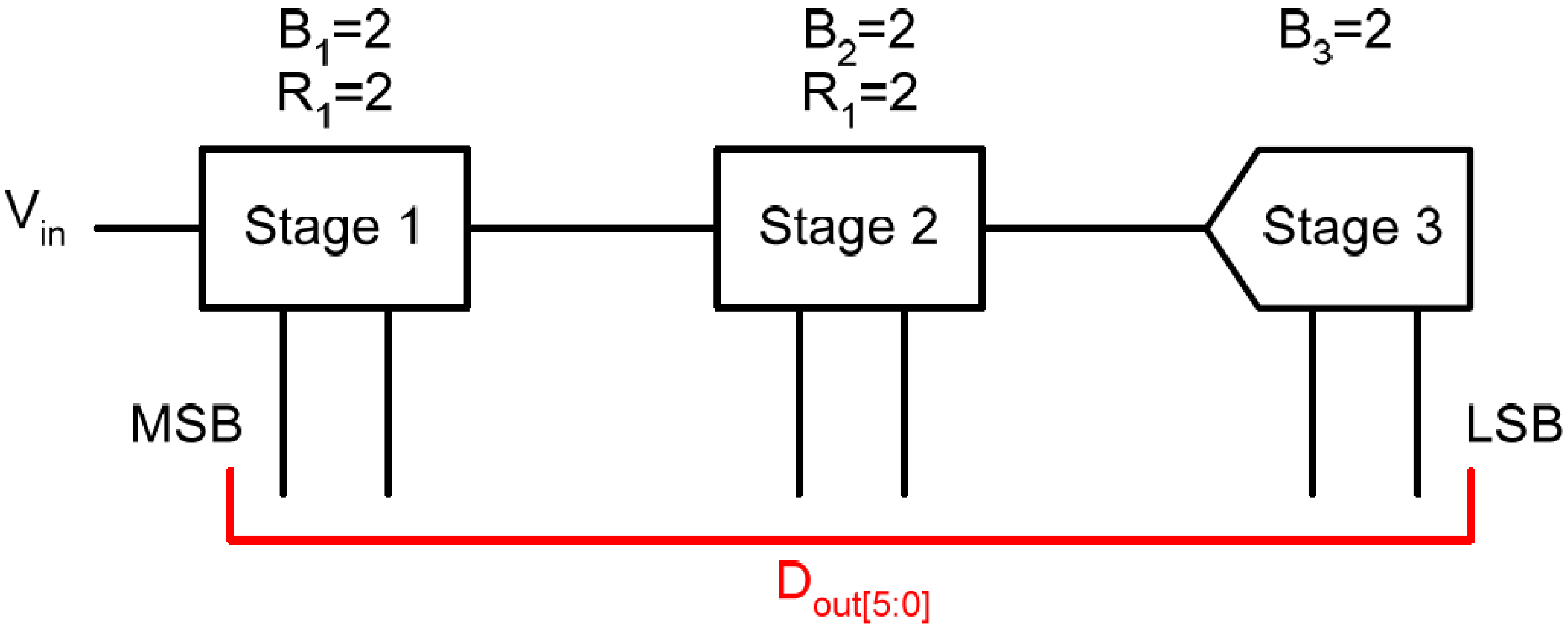


$$D_{out} = D_1 + \frac{1}{4} D_2 + \frac{1}{16} D_3$$

Combining the Bits

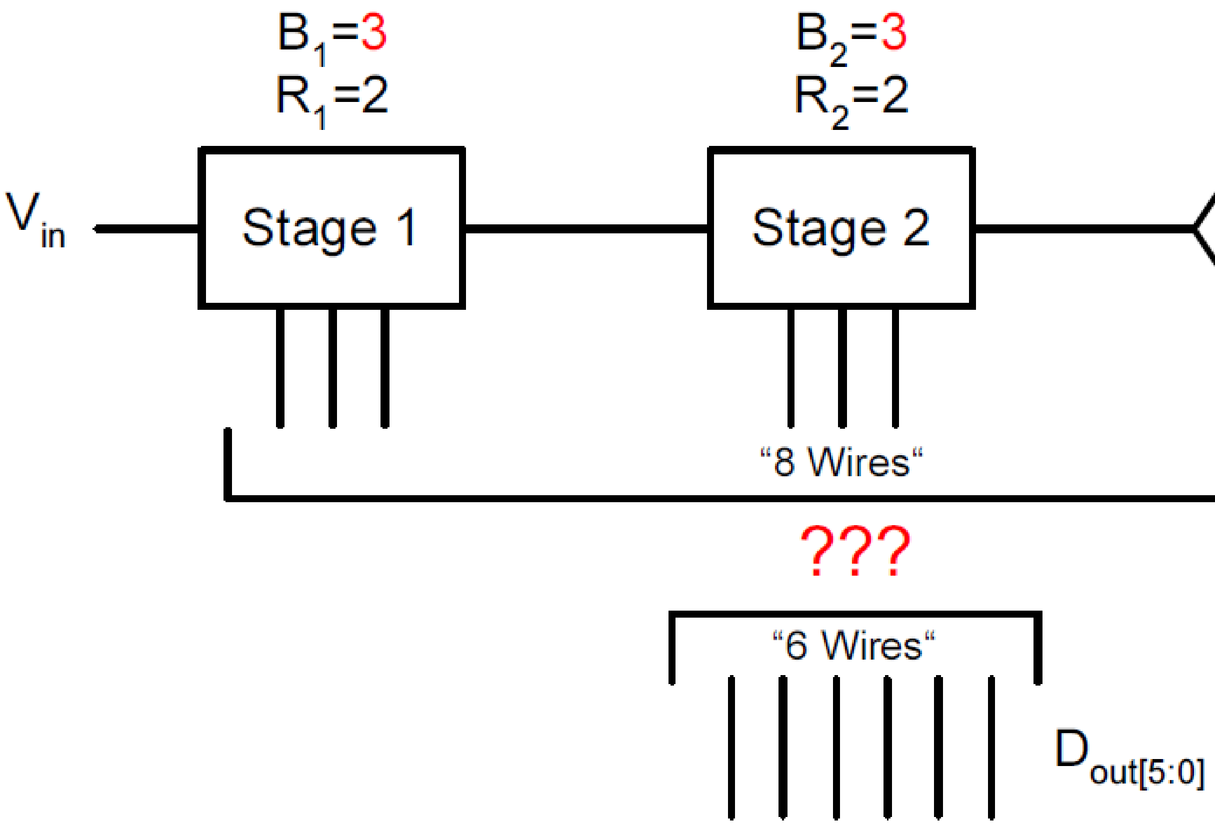
```
D1     XX
D2       XX
D3         XX
--------------
Dout   DDDDDD
```

- Only bit shifts
- No arithmetic circuits needed



Combining the Bits

- Example2: Three 2-bit stages, one bit redundancy in stages 1 and 2 (6-bit aggregate ADC resolution)

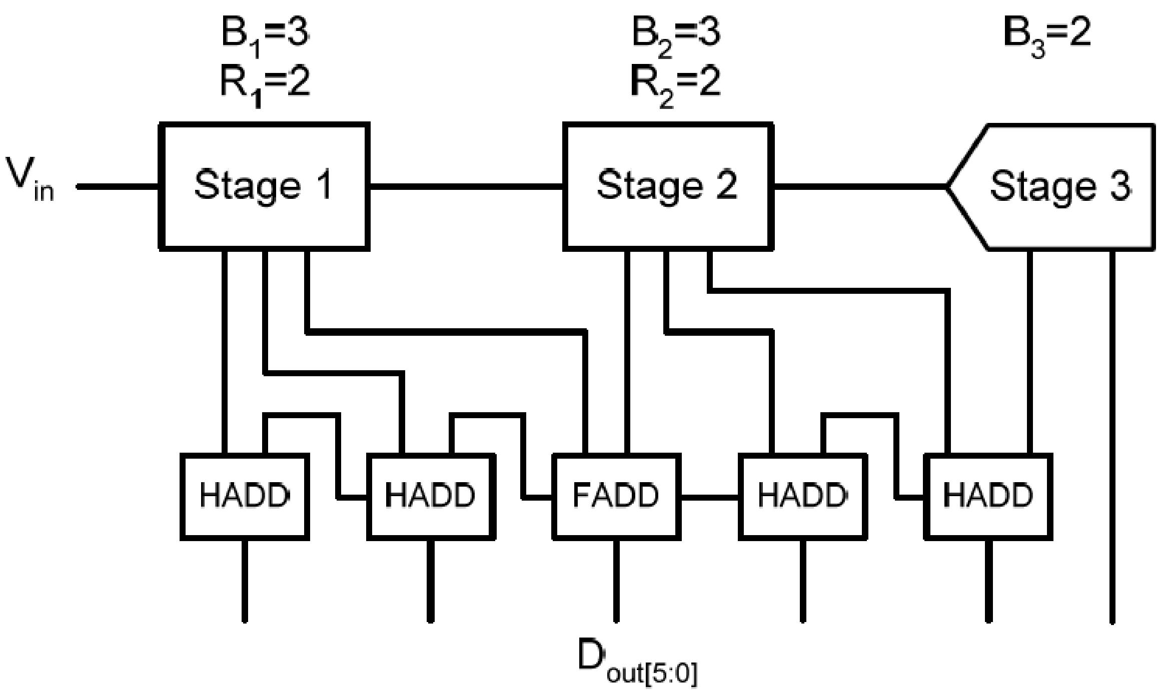


Combining the Bits

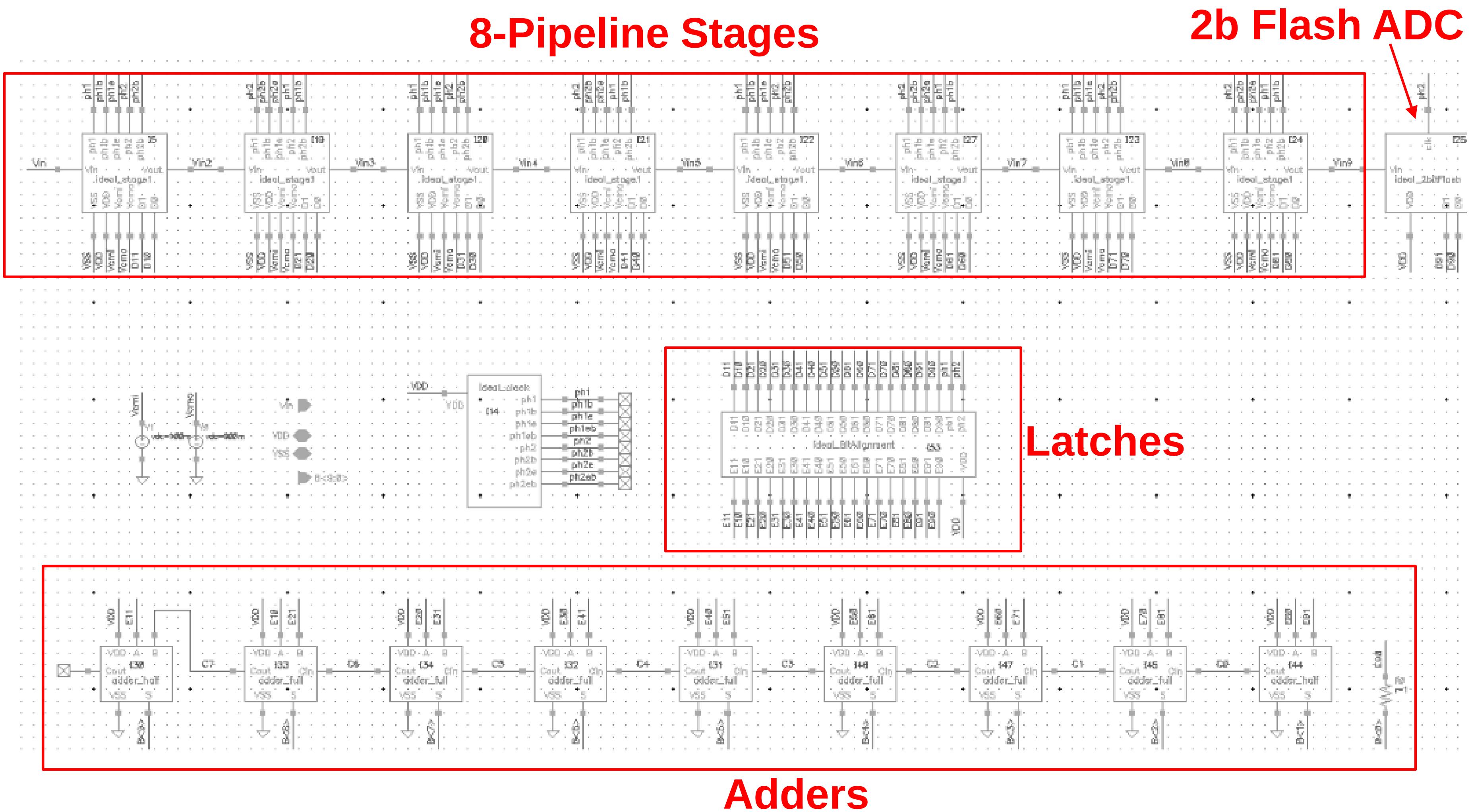
$$D_{out} = D_1 + \frac{1}{4}D_2 + \frac{1}{16}D_3$$

```
D1     XXX
D2        XXX
D3           XX
-------------------
Dout   DDDDDD
```

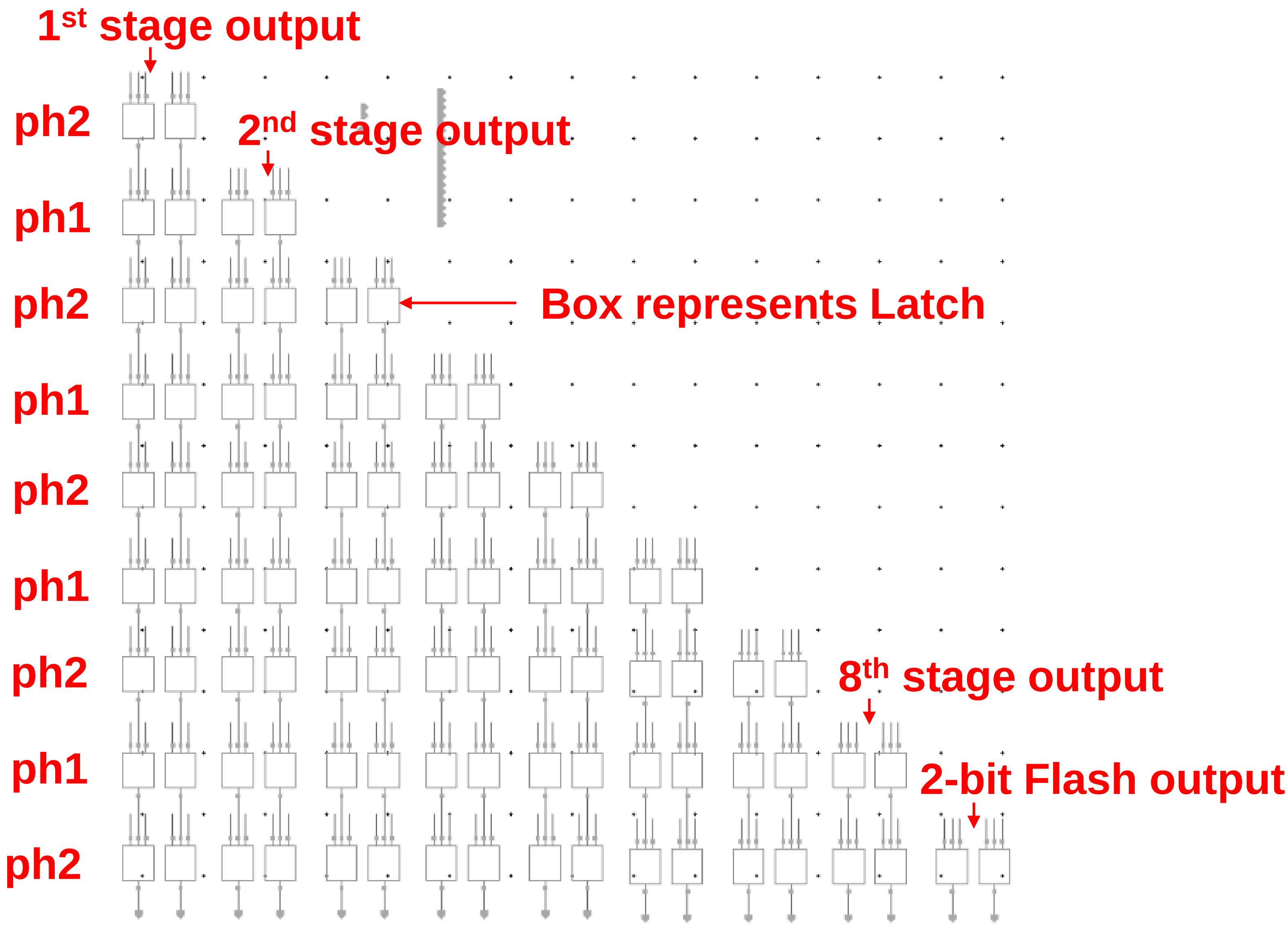
- Bits overlap
- Need adders (Still, no good reason for calling this "digital correction"...)



10-bit Pipelined ADC Implementation Example



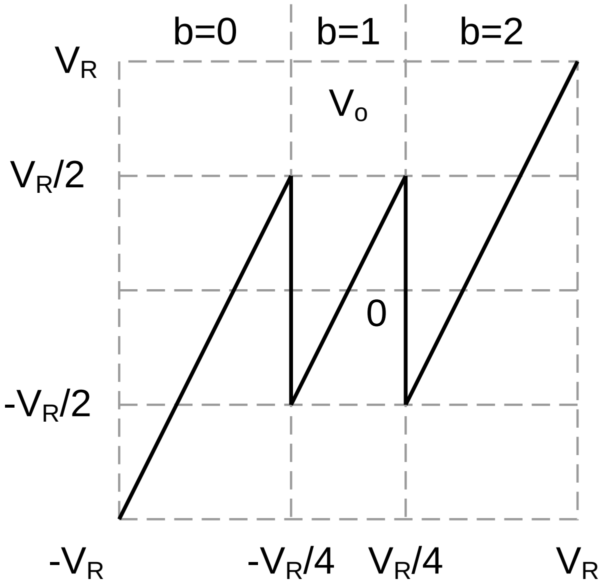
Stage Delay Structure Example

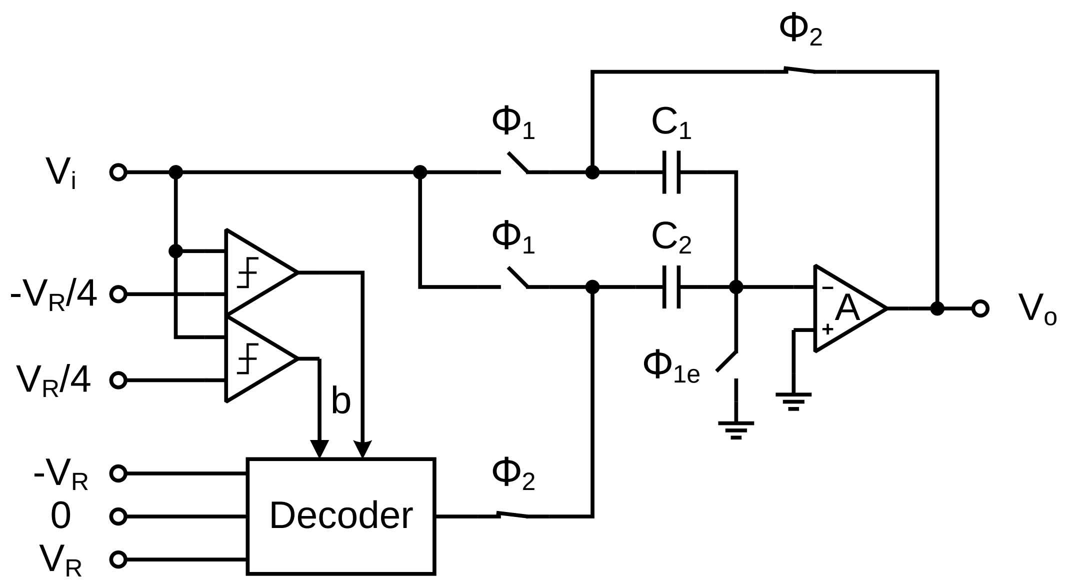


No. of Comparators and Inter-stage Gain

- Number of Comparators for redundant stage design
  - $2^N - 2$
  - 2-bit $\rightarrow 2^2 - 2 = 2$ Comparators
  - 3-bit $\rightarrow 2^3 - 2 = 6$ Comparators
- Inter-stage MDAC gain requirement
  - 2^{N-1}
  - 2-bit $\rightarrow 2^{2-1} = 2$
  - 3-bit $\rightarrow 2^{3-1} = 4$
- For MDAC gain of 4
  - $Q = C_1 \cdot V_1 = C_2 \cdot V_2$
  - Sample input signal into 4 capacitors during phase 1 : $Q_1 = 4C \cdot V_{in}$
  - Flip-around to 1 capacitor during phase 1 : $Q_2 = C \cdot V_{out}$
  - $Q_1 = Q_2 \rightarrow V_{out} = 4V_{in}$

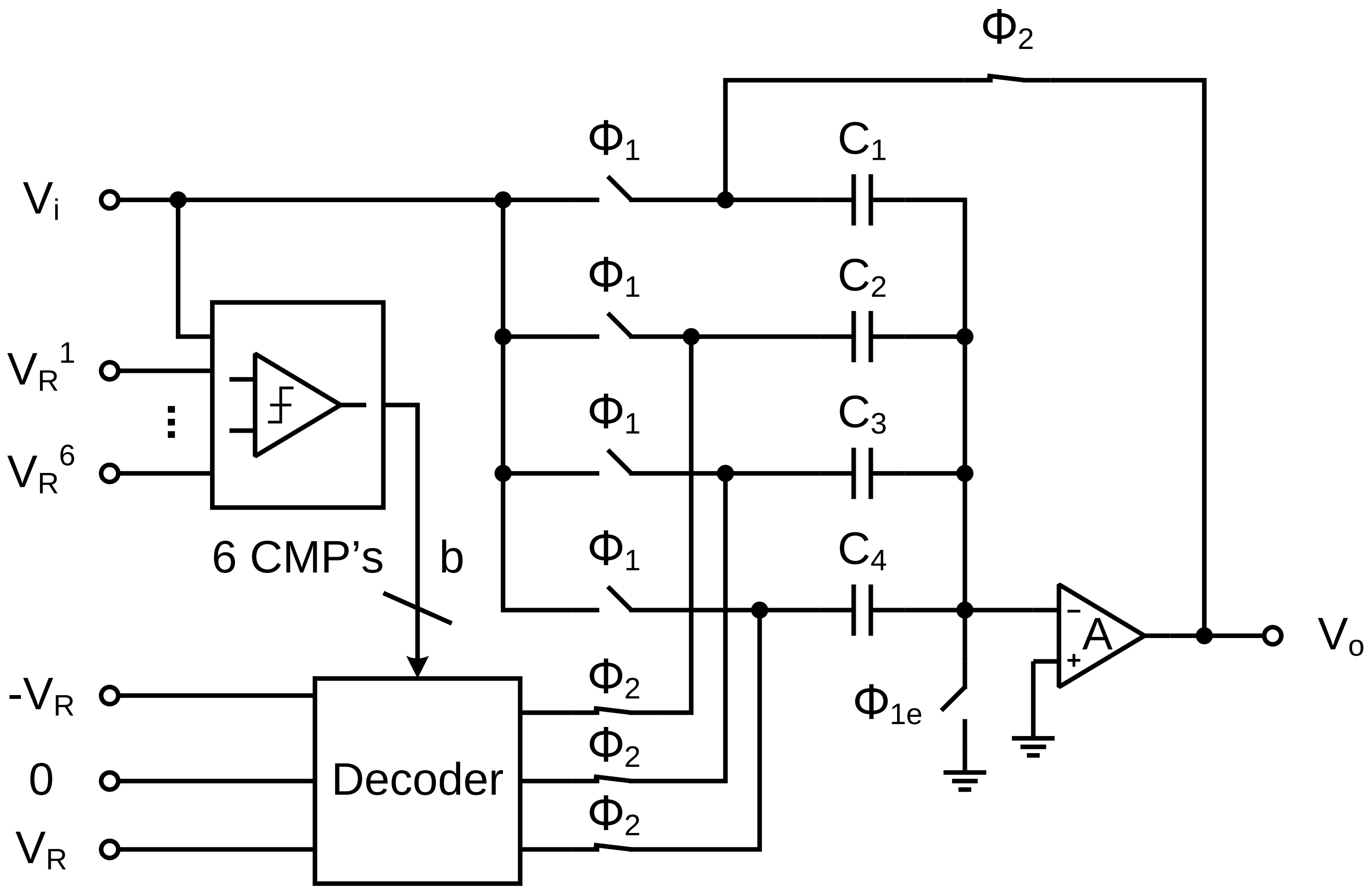
1.5-bit/Stage Pipelined ADC



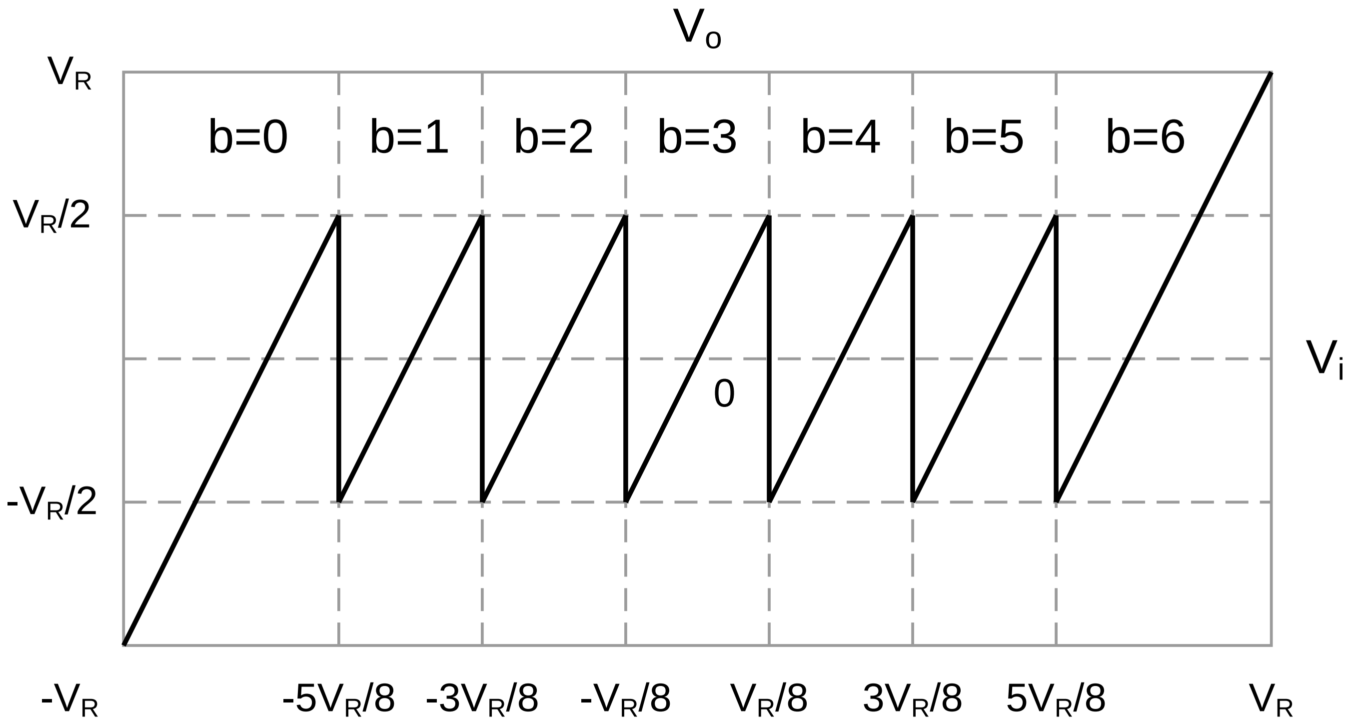


- 2X gain + 3-level DAC + subtraction all integrated
- Digital redundancy relaxes the tolerance on CMP/RA offsets

2.5-bit/Stage Pipelined ADC



2.5-bit/Stage Pipelined ADC



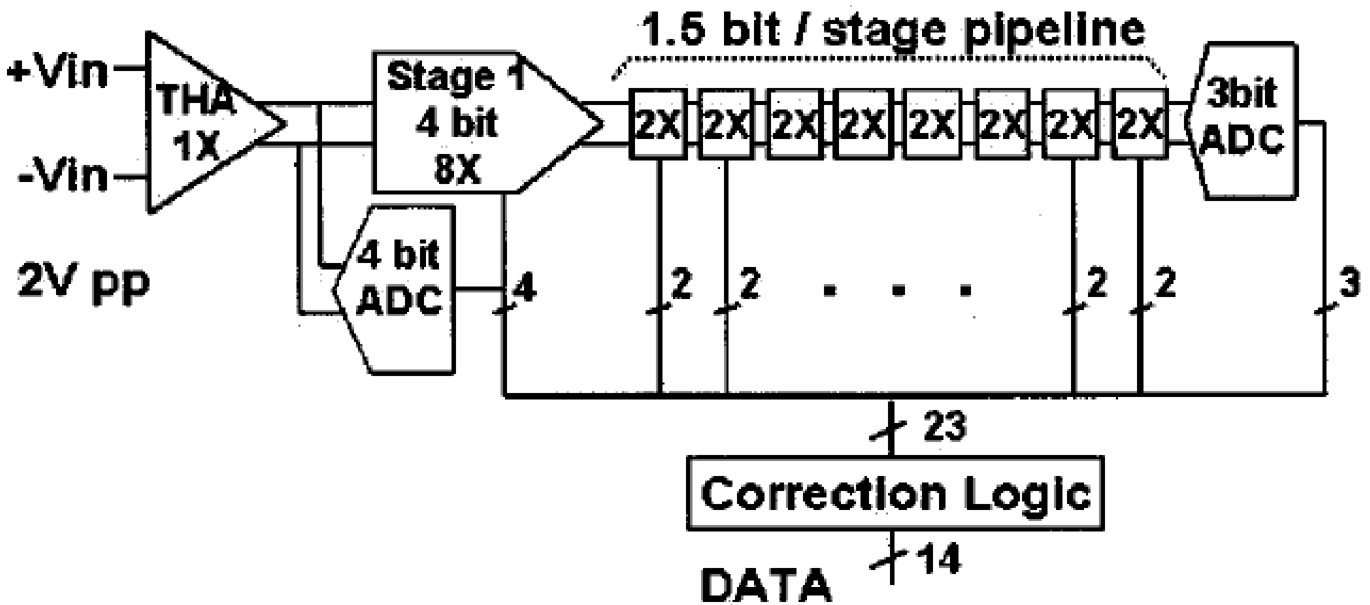
- 6 comparators + 7-level DAC are required
- Max tolerance on comparator offset is $\pm V_R/8$

Example 14-bit Pipelined ADC

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001

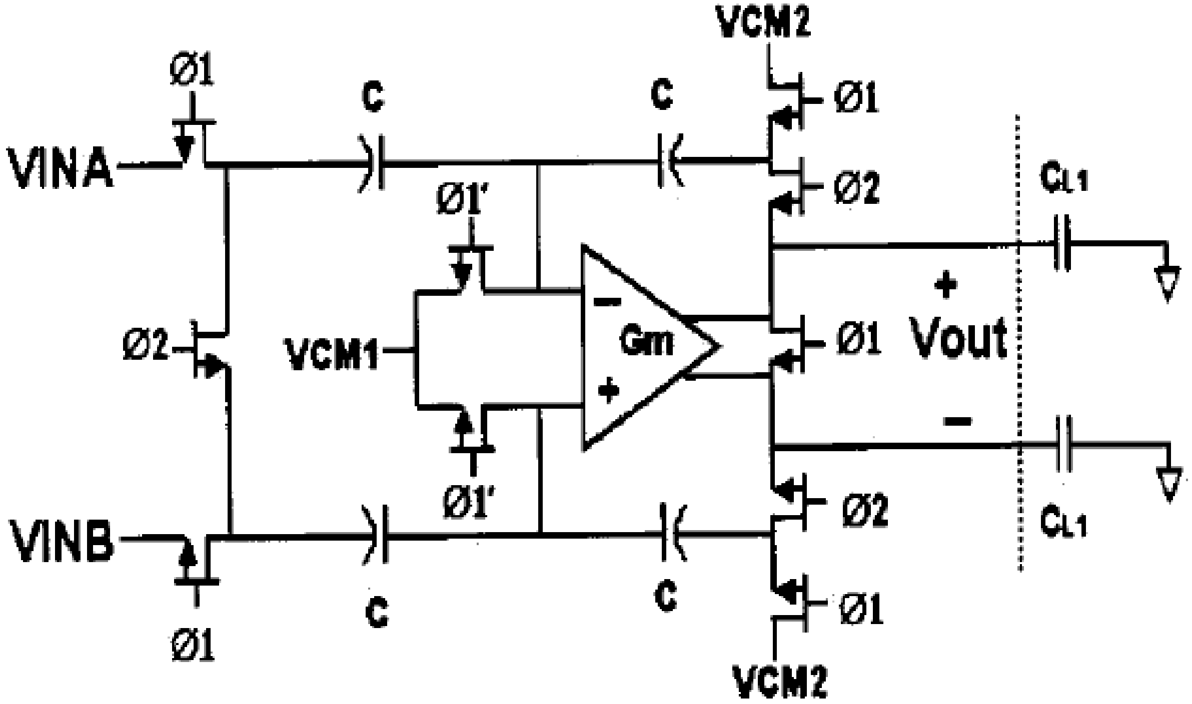
A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input

Wenhua (Will) Yang, *Member, IEEE*, Dan Kelly, *Member, IEEE*, Iuri Mehr, *Member, IEEE*, Mark T. Sayuk, *Member, IEEE*, and Larry Singer, *Member, IEEE*



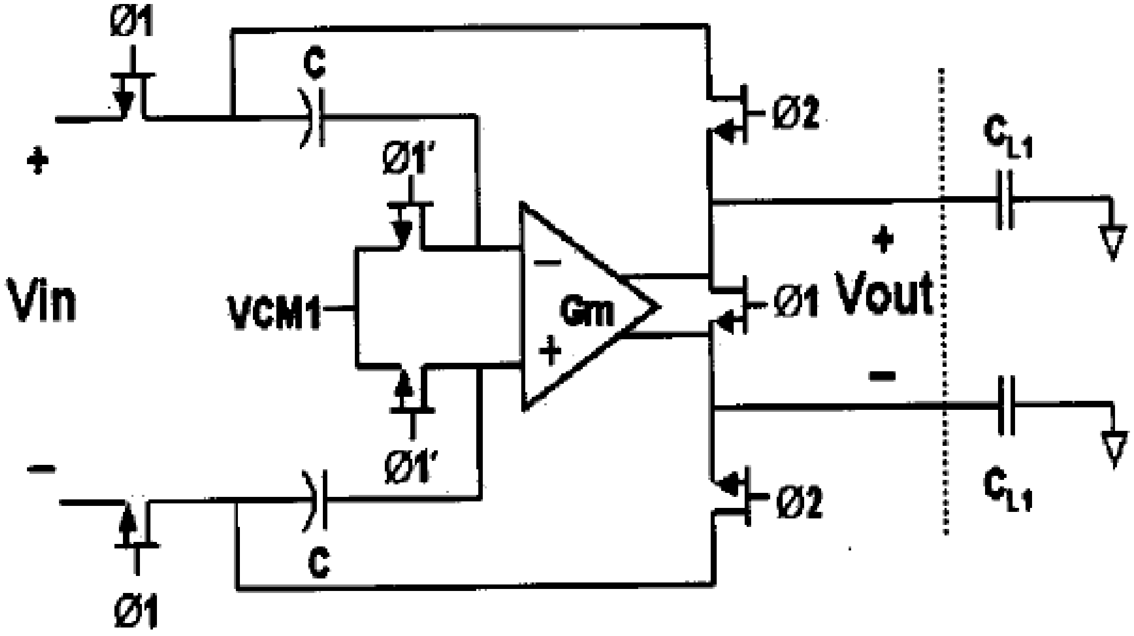
14-bit Pipelined ADC

Charge-redistribution THA



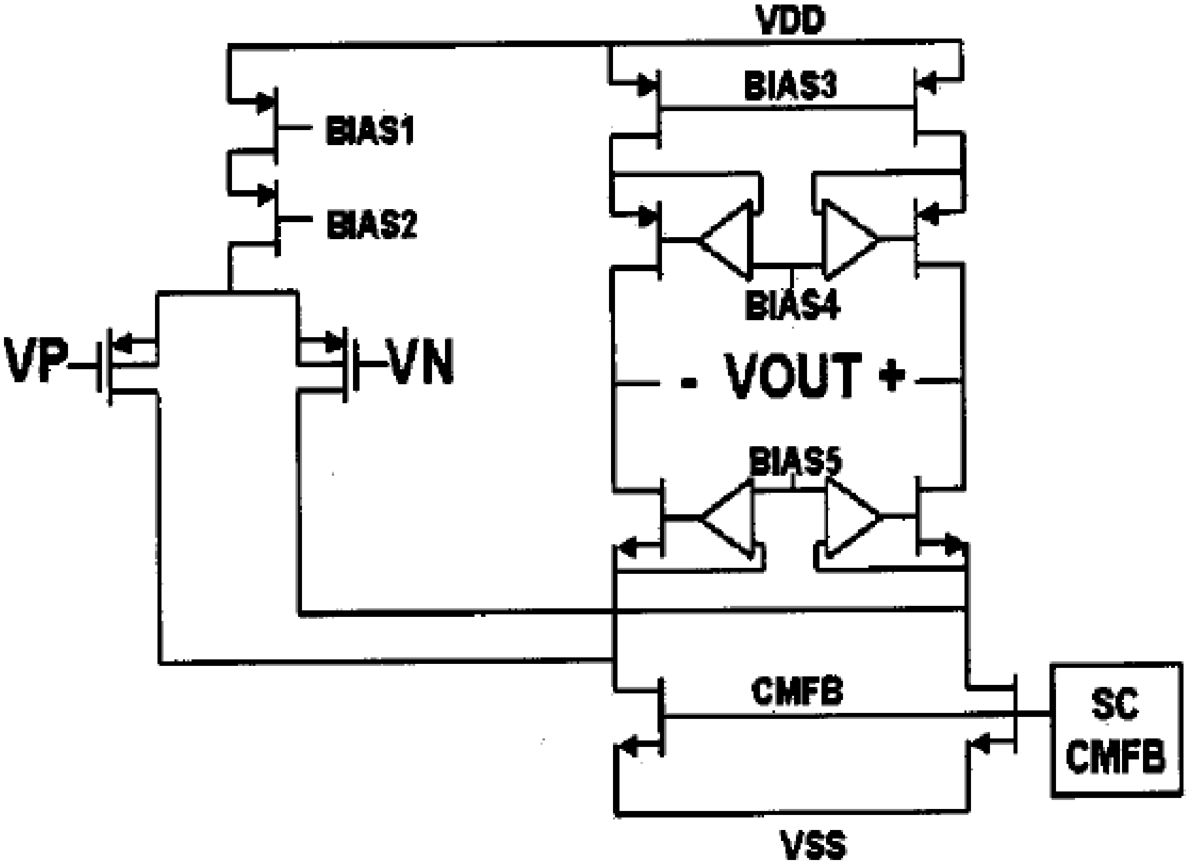
14-bit Pipelined ADC

Flip-around THA



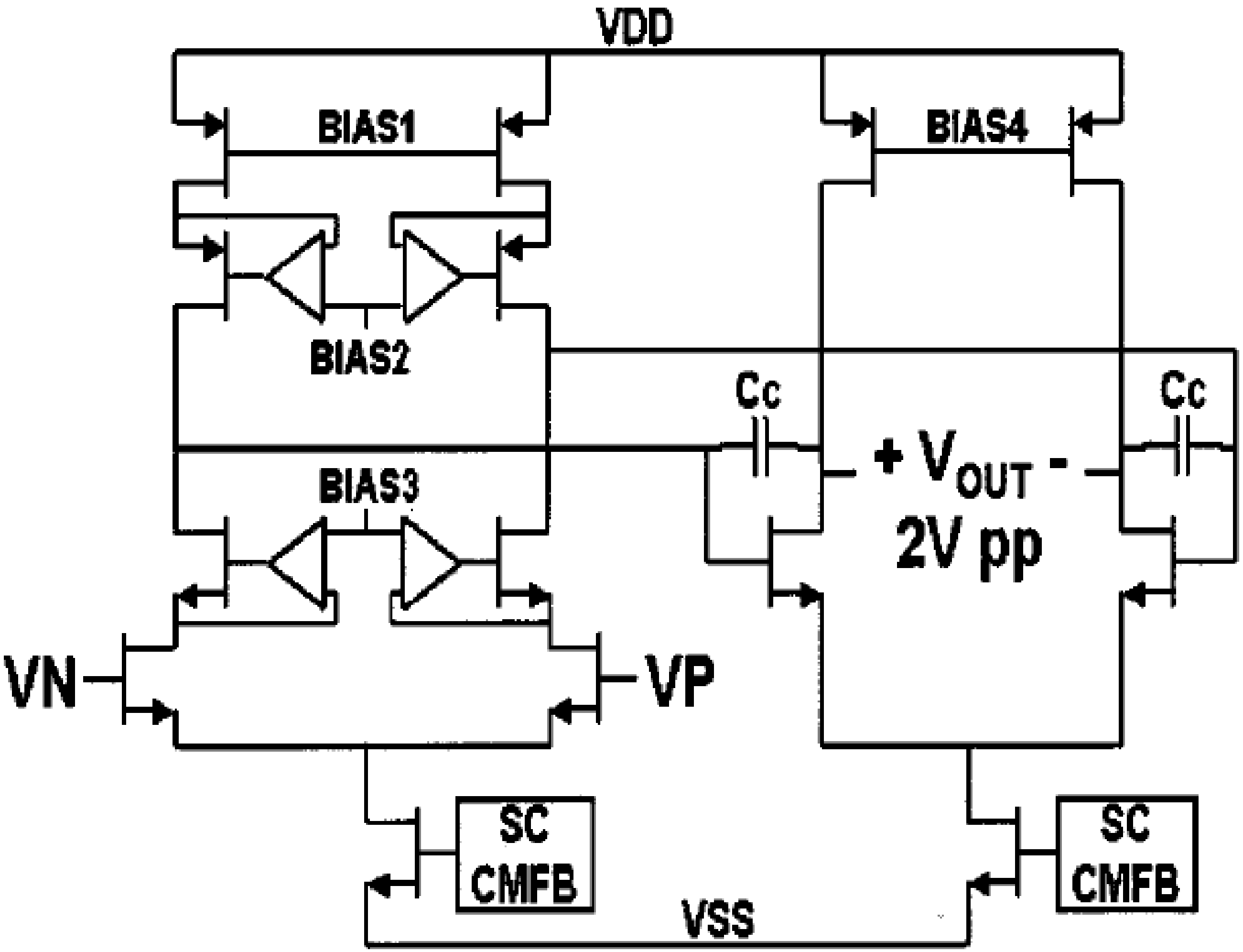
14-bit Pipelined ADC

Amplifier in Flip-around THA



14-bit Pipelined ADC

Amplifier in Stage 1



OPAMP Gain Requirement for N-bit ADC

OPAMP is always used in closed loop configuration.

OPAMP Closed-loop Response:

$$V_{\rm out} = G \times V_{\rm in} \left(\frac{1}{1 + \frac{1}{A \times \beta}} \right) \left(1 - e^{-\frac{t}{\tau}}\right)$$

Assume Gain Error should be less than ¼ LSB

$$\frac{1}{\beta A} < \frac{1}{\mathbf{4}} LSB \quad \rightarrow \quad \frac{1}{\beta A} < \frac{1}{\mathbf{4}} \frac{\boldsymbol{V_{FS}}}{\mathbf{2}^{\boldsymbol{N}}}$$

$$\boldsymbol{A} > \frac{\mathbf{4} \cdot \mathbf{2}^{\boldsymbol{N}}}{\beta \cdot \boldsymbol{V_{FS}}}$$

Resolution	Full Scale	Beta	Gain (dB)	Gain (dB)
N	V_{FS} (Volt)	β	4 ·2^(N) /(β·V_{FS})	20log(x)
10	1	1	4096	72
10	1	0.5	8192	78
11	1	1	8192	78
11	1	0.5	16384	84
12	1	1	16384	84
12	1	0.5	32768	90
13	1	1	32768	90
13	1	0.5	65536	96
14	1	1	65536	96
14	1	0.5	131072	102

OPAMP Bandwidth Requirement for N-bit ADC

Assume Settling Error should be less than 1/2 LSB

$$e^{-t/\tau} < \frac{1}{2}\,LSB \quad \rightarrow \quad e^{-t/\tau} < \frac{1}{2}\frac{\boldsymbol{V_{FS}}}{\boldsymbol{2^N}} \quad \rightarrow \quad \frac{t}{\tau} > (\boldsymbol{N+1})\boldsymbol{ln}(\boldsymbol{2}) - \boldsymbol{ln}(\boldsymbol{V_{FS}})$$

$$t = \frac{T_s}{2} = \frac{1}{2f_s}$$

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{2\pi\, f_{-3dB}} = \frac{1}{2\pi\,\beta\, f_u}$$

$$\frac{t}{\tau} = \frac{1}{2f_s}2\pi\,\beta\, f_u > \;(\boldsymbol{N+1})\boldsymbol{ln}(\boldsymbol{2}) - \boldsymbol{ln}(\boldsymbol{V_{FS}})$$

$$f_u > \frac{f_s}{\pi\beta}[(\boldsymbol{N+1})\boldsymbol{ln}(\boldsymbol{2}) - \boldsymbol{ln}(\boldsymbol{V_{FS}})]$$

$$\boldsymbol{ln}(\boldsymbol{2}) = 0.\boldsymbol{693}$$

Resolution	Full Scale	Beta	Sampling Rate	UGB	UGB(MHz)	fu/fs
N	V_{FS} (Volt)	β	fs	fu	fu	fu = k fs
10	1	1	1.00E+08	2.43E+08	243 MHz	fu = 2.5 fs
10	1	0.5	1.00E+08	4.85E+08	485 MHz	fu = 5 fs
11	1	1	1.00E+08	2.65E+08	265 MHz	
11	1	0.5	1.00E+08	5.30E+08	530 MHz	
12	1	1	1.00E+08	2.87E+08	287 MHz	fu = 3 fs
12	1	0.5	1.00E+08	5.74E+08	574 MHz	fu = 6 fs
13	1	1	1.00E+08	3.09E+08	309 MHz	
13	1	0.5	1.00E+08	6.18E+08	618 MHz	
14	1	1	1.00E+08	3.31E+08	331 MHz	fu = 3.3 fs
14	1	0.5	1.00E+08	6.62E+08	662 MHz	fu = 6.6 fs