EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 1: Introduction

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ENG-259

Course Information

Instructor:	Sang-Soo Lee, PhD Carnegie Mellon University		
Time:	Class : Monday, Wednesday 6:00 – 7:15 pm		
	Office Hour : Monday, Wednesday 4:30 – 5:30 pm		
	Other time by appointment		
Lab ISA:	Sreya Yeleswarapu, sreyatejasvi.yeleswarapu@sjsu.edu		
Lab Time:	Monday	3 – 5 PM	Sreya
	Wednesday	3 – 5 PM	Sreya

Prerequisites

- Analog Circuit
  - ✓ EE223 or equivalent
- Digital Signal Processing
  - ✓ Basic signal processing knowledge
- Digital Circuit
  - ✓ Basic knowledge of gate/transistor-level logic design (logic family, sequential logic, etc.)
  - ✓ Some knowledge of Verilog-A is helpful for the project
- CAD Tools
  - ✓ Cadence Spectre
  - ✓ Matlab

Cadence Spectre

- Homework and project will use Cadence Spectre simulation extensively

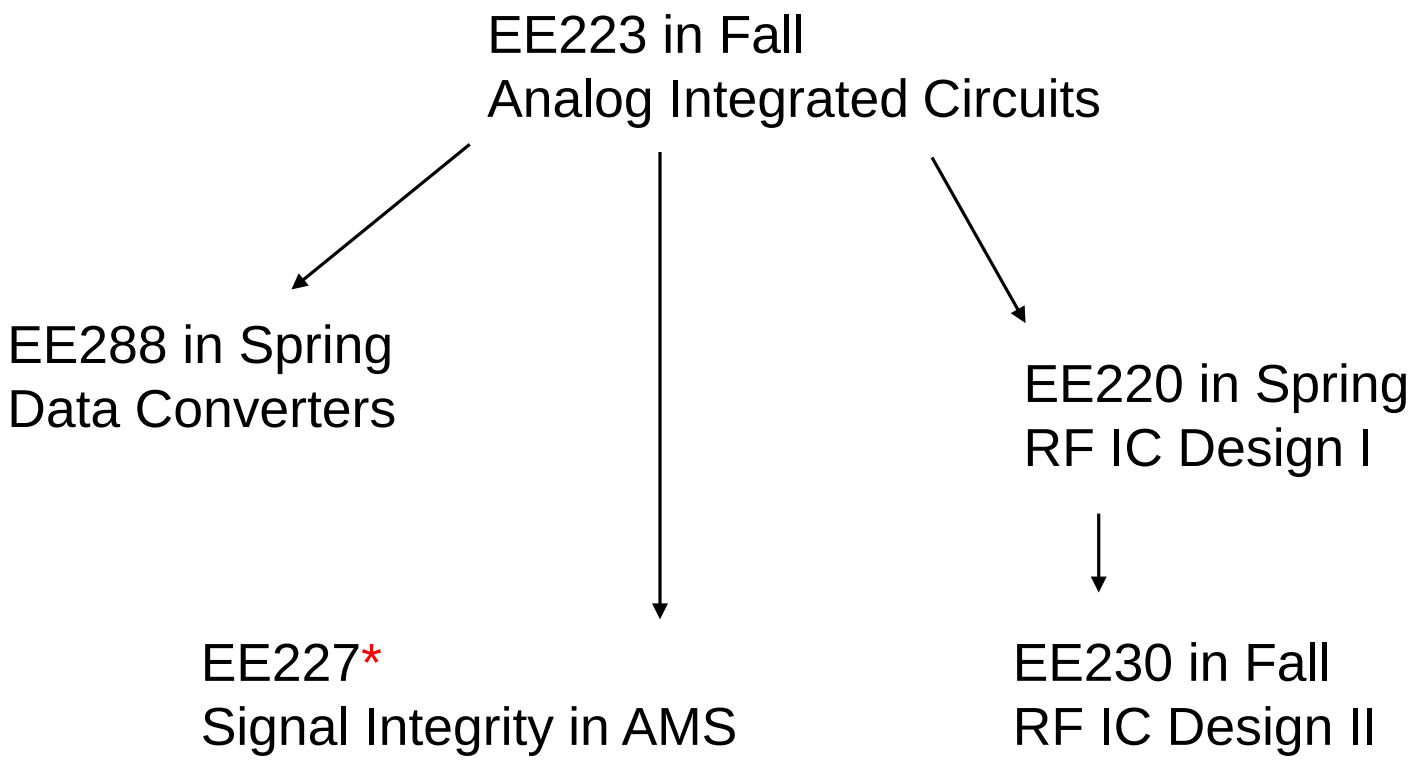
- To Set up your Cadence environment

  See the files in “cadence” folder in EE288 Course Canvas

- TA Lab hours : 3-5 PM on Monday, Wednesday

- Additional Cadence Spectre Tutorials
  - If you have no experience in Cadence, please check Youtube videos such as
  - https://www.youtube.com/watch?v=u0WgSMa1hrc&list=PLK2eyR1C9gjr7j-YoL_-JwJmjU6lNZGTO

Analog Course Sequence at SJSU



* Not Offered this Semester due to small number of enrollment

Course Goals

- Learn key ADC & DAC structures widely used in industry
- Learn the circuit building blocks to construct ADCs
- Learn the key metrics to measure ADC & DAC
- Design a 10-bit Pipelined ADC to get the experience that will give you enough knowledge to build more complex ADC structures

Course Outline (not in order)

1. Introduction on ADC architectures
2. Signal Sampling, Quantization, and Reconstruction
3. ADC Metrics – Static and Dynamic Performance
4. OPAMP Review
5. Review of Switched-Capacitor Circuits
6. Comparators
7. Flash ADC
8. DAC – Resistor, Current, Charge based
9. SAR ADC
10. Sample-and-Hold Amplifier (SHA)
11. Pipelined ADC
12. Oversampled data converters
13. Advanced ADC architectures and figure-of-merit (FoM)
14. Data converter testing and benchmarks

Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	Finish Flash ADC
28-Feb	DAC Architectures - Resistor, R-2R
5-Mar	DAC Architectures - Current steering, Segmented
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

Grading

- Homework 30%
  - Essentially a mini design project running Cadence Simulations
  - Each HW will be due in 2 weeks
  - Submit electronically via email by 6PM on due date
- Midterm 30%
  - March 21 – subject to change
- Project 40%
  - 10-bit 100MS/s Pipelined ADC in 0.18um CMOS
  - Team of 2 students
  - Okay to work alone, but not okay to work in a team of 3 or more
  - Presentation + Report

Textbook and References

- Textbook: No required textbook. Lecture notes, slides, and papers will be posted on Canvas.

- References
  1. M. Pelgrom, *Analog-to-Digital Conversion*, Springer, 2017
  2. van de Plassche, Rudy J., *CMOS Integrated A/D and D/A Converters*, Kluwer, 2003
  3. Gustavsson, Wikner, Tan, CMOS Data Converters for Communications, Kluwer, 2000.
  4. B. Razavi, Data Conversion System Design, IEEE Press, 1995. (Available on IEEE explorer)
  5. F. Maloberti, “Data Converters, Springer, 2007

Why This Course?

- Data conversion is difficult
- Data converters have a huge market
- The demand for higher performance in data converters keeps growing
- Cost issues make it desirable to build data converters in mainstream VLSI technologies rather than dedicated “analog” processes. This creates more difficulties in the design.

Data Converter Applications

- Consumer electronics
  - Audio, TV, Video
  - Digital Cameras
  - Automotive control
  - Appliances
  - Toys
- Communications
  - Mobile Phones
  - Personal Data Assistants
  - Wireless Transceivers
  - Routers, Modems





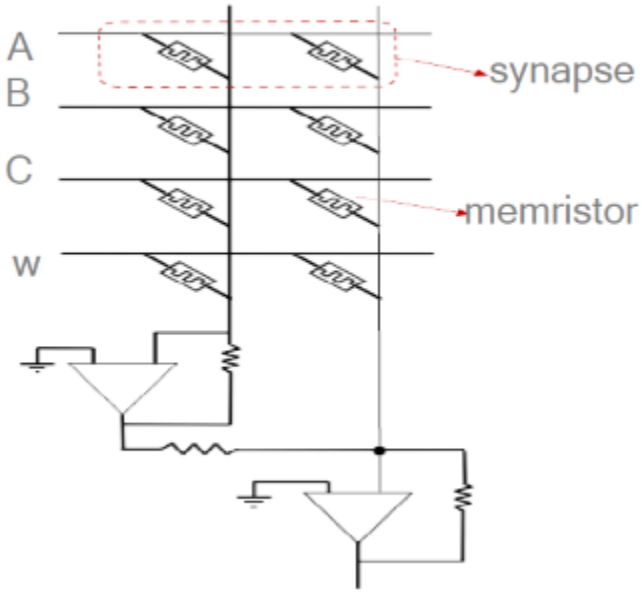


Data Converter Applications

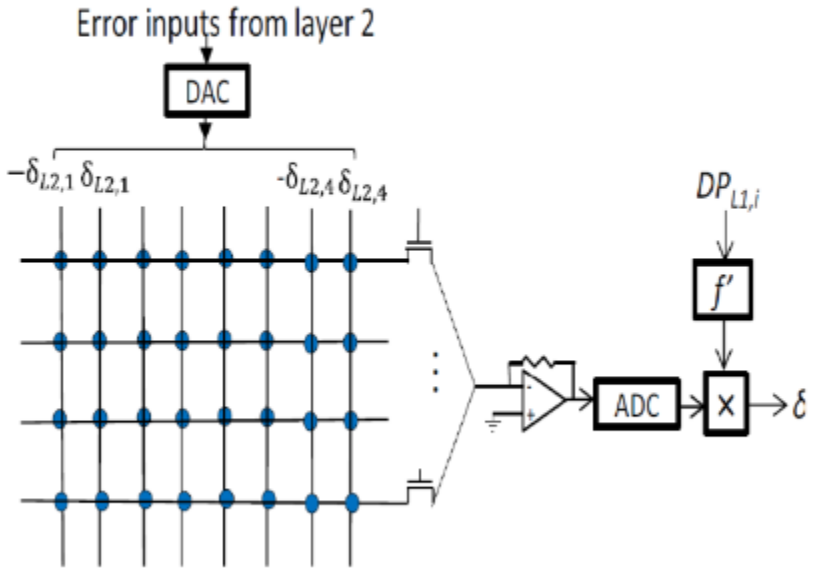
- Computing and Control
  - Storage media
  - Sound Cards
  - Data acquisition cards
- Instrumentation
  - Lab bench equipment
  - Semiconductor test equipment
  - Scientific equipment
  - Medical equipment

Deep Neural Networks

On-chip Training of Memristor Based Deep Neural Networks, Raqibul Hasan, Neural Networks (IJCNN), 2017 International Joint Conference on



Memristor based neuron circuit



Implementing back propagation phase

ISSCC 2018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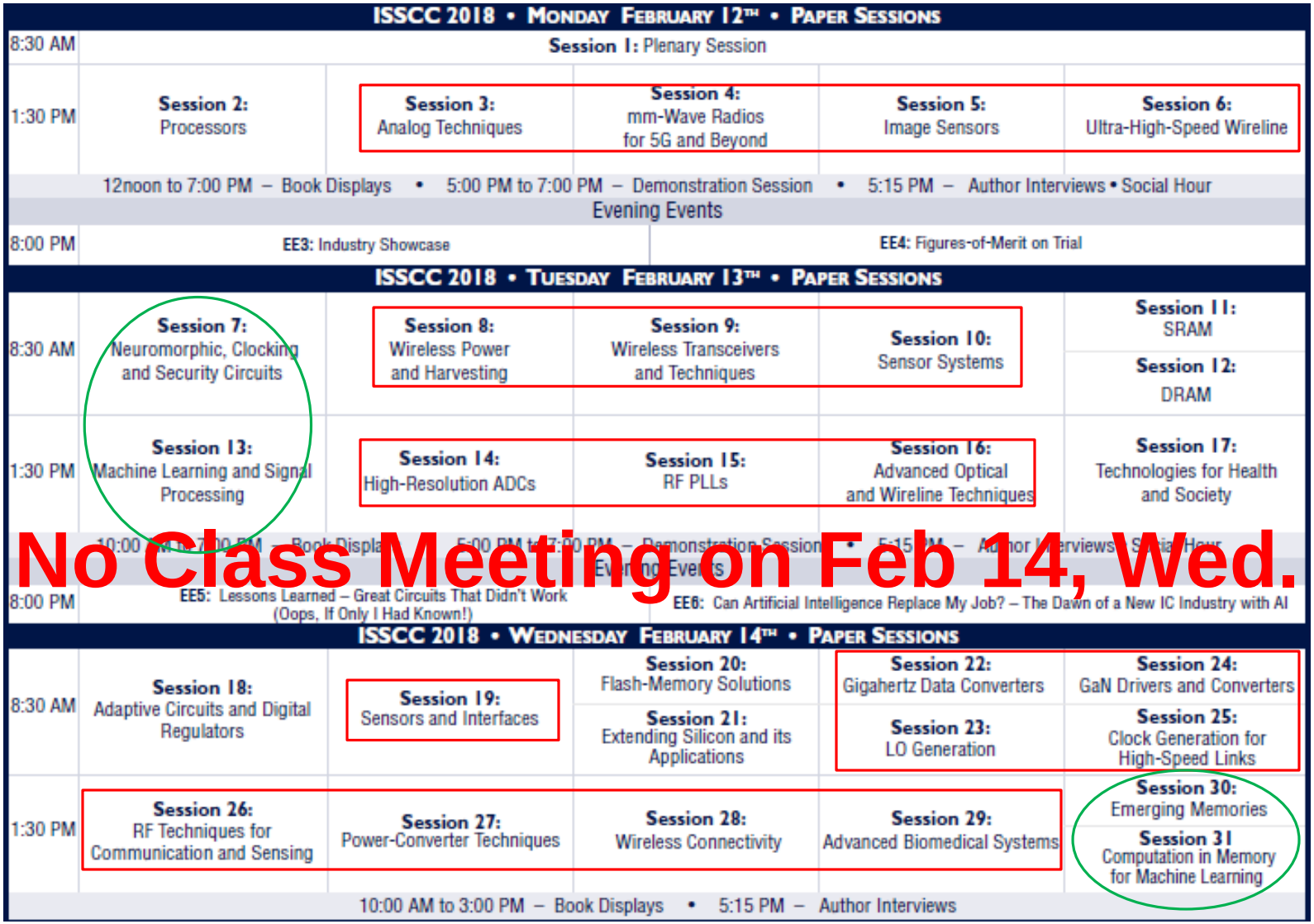
UNIVERSITY OF PENNSYLVANIA
2018 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE
FEBRUARY
11, 12, 13, 14, 15
CONFERENCE THEME:
SILICON ENGINEERING A SOCIAL WORLD
SAN FRANCISCO
MARRIOTT MARQUIS HOTEL
NEW THIS YEAR!
INDUSTRY SHOWCASE;
Impact of ICs on Product Design
5-DAY PROGRAM
SUNDAY ALL-DAY
2 FORUMS: INTELLIGENT ENERGY SYSTEMS FOR IoT; FINFETs & FDSOI IN MIXED-SIGNAL DESIGN
10 TUTORIALS: LOW-JITTER PLLs FOR WIRELESS; NV FOR MEMORY, LOGIC, & AI; BASICS OF QUANTUM COMPUTING; ECC 56 /NVM; HYBRID DESIGN OF ADCs; CMOS SINGLE-PHOTON DETECTION; ADAPTIVE & RESILIENT CIRCUITS; SWITCHED-MODE POWER-CONVERTER DESIGN; DIGITAL mW TRANSMITTERS; ADC-BASED SERIAL LINKS
2 EVENING EVENTS: GRADUATE STUDENT RESEARCH IN PROGRESS; WORKSHOP ON CIRCUITS FOR SOCIAL GOOD
THURSDAY ALL-DAY
4 FORUMS: CIRCUITS/ARCHITECTURES FOR WIRELESS SENSING/RADAR/IMAGING; TECHNIQUES FOR mm-WAVE MULTI-ANTENNA SYSTEMS; ADVANCED OPTICAL COMMUNICATIONS; ENERGY-EFFICIENT ANALOG
SHORT-COURSE: HARDWARE FOR MACHINE LEARNING INFERENCE

ISSCC 2018 Analog-Related Sessions



ISSCC 2018 • Monday February 12th • Paper Sessions

8:30 AM	**Session 1:** Plenary Session				
1:30 PM	**Session 2:** Processors	**Session 3:** Analog Techniques	**Session 4:** mm-Wave Radios for 5G and Beyond	**Session 5:** Image Sensors	**Session 6:** Ultra-High-Speed Wireline

12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE3:** Industry Showcase	**EE4:** Figures-of-Merit on Trial

ISSCC 2018 • Tuesday February 13th • Paper Sessions

8:30 AM	**Session 7:** Neuromorphic, Clocking and Security Circuits	**Session 8:** Wireless Power and Harvesting	**Session 9:** Wireless Transceivers and Techniques	**Session 10:** Sensor Systems	**Session 11:** SRAM **Session 12:** DRAM
1:30 PM	**Session 13:** Machine Learning and Signal Processing	**Session 14:** High-Resolution ADCs	**Session 15:** RF PLLs	**Session 16:** Advanced Optical and Wireline Techniques	**Session 17:** Technologies for Health and Society

10:00 AM to 7:00 PM – Book Displa… 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM	**EE5:** Lessons Learned – Great Circuits That Didn't Work (Oops, If Only I Had Known!)	**EE6:** Can Artificial Intelligence Replace My Job? – The Dawn of a New IC Industry with AI

ISSCC 2018 • Wednesday February 14th • Paper Sessions

8:30 AM	**Session 18:** Adaptive Circuits and Digital Regulators	**Session 19:** Sensors and Interfaces	**Session 20:** Flash-Memory Solutions **Session 21:** Extending Silicon and its Applications	**Session 22:** Gigahertz Data Converters **Session 23:** LO Generation	**Session 24:** GaN Drivers and Converters **Session 25:** Clock Generation for High-Speed Links
1:30 PM	**Session 26:** RF Techniques for Communication and Sensing	**Session 27:** Power-Converter Techniques	**Session 28:** Wireless Connectivity	**Session 29:** Advanced Biomedical Systems	**Session 30:** Emerging Memories **Session 31** Computation in Memory for Machine Learning

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

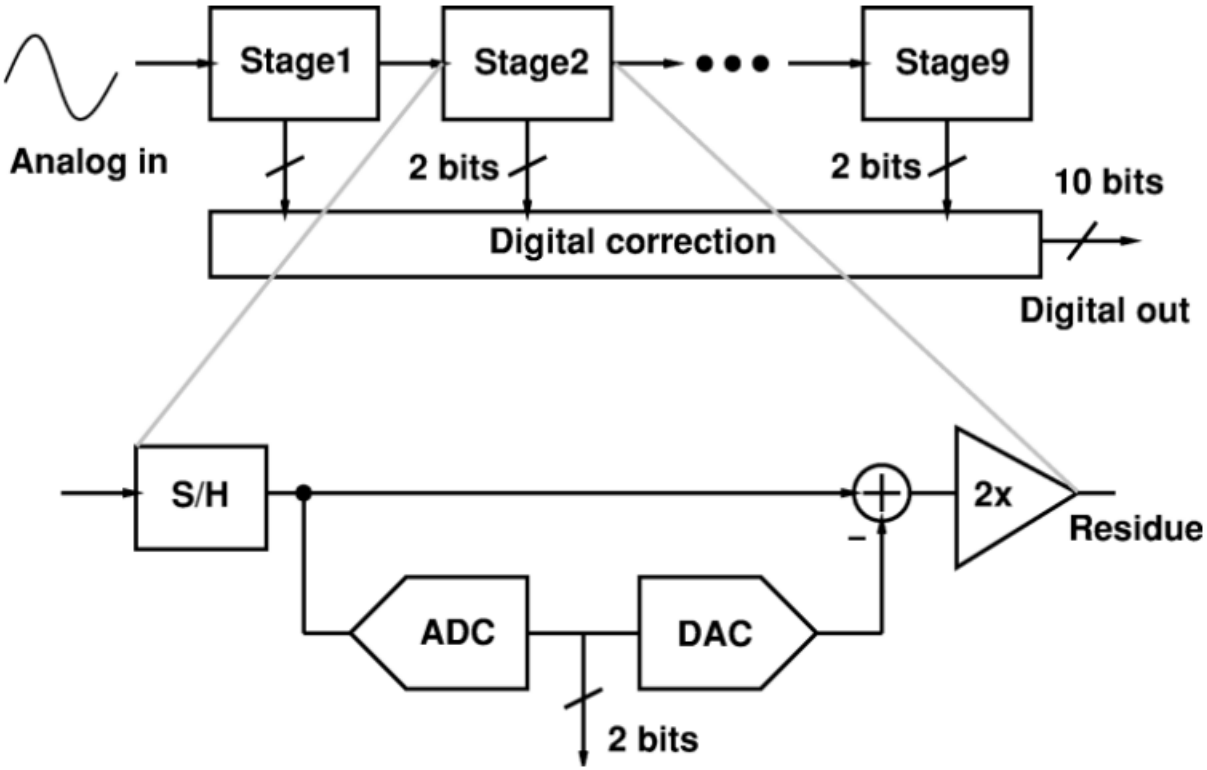
No Class Meeting on Feb 14, Wed.

Homework Topics

- HW#1 1/29 Monday
  - 10-bit ADC and DAC using ideal components
- HW#2 2/12 Monday
  - 4-bit Flash ADC using ideal components
- HW#3 2/26 Monday
  - 4-bit Flash ADC using Real components
- HW#4 3/12 Monday
  - 4-bit SAR ADC using Real components
- HW#5 4/4 Wednesday
  - 1.5-bit Pipeline Stage using ideal OPAMP
- HW#6 4/18 Wednesday
  - 10-bit Pipelined ADC using ideal OPAMP

Project: 10-bit Pipelined ADC

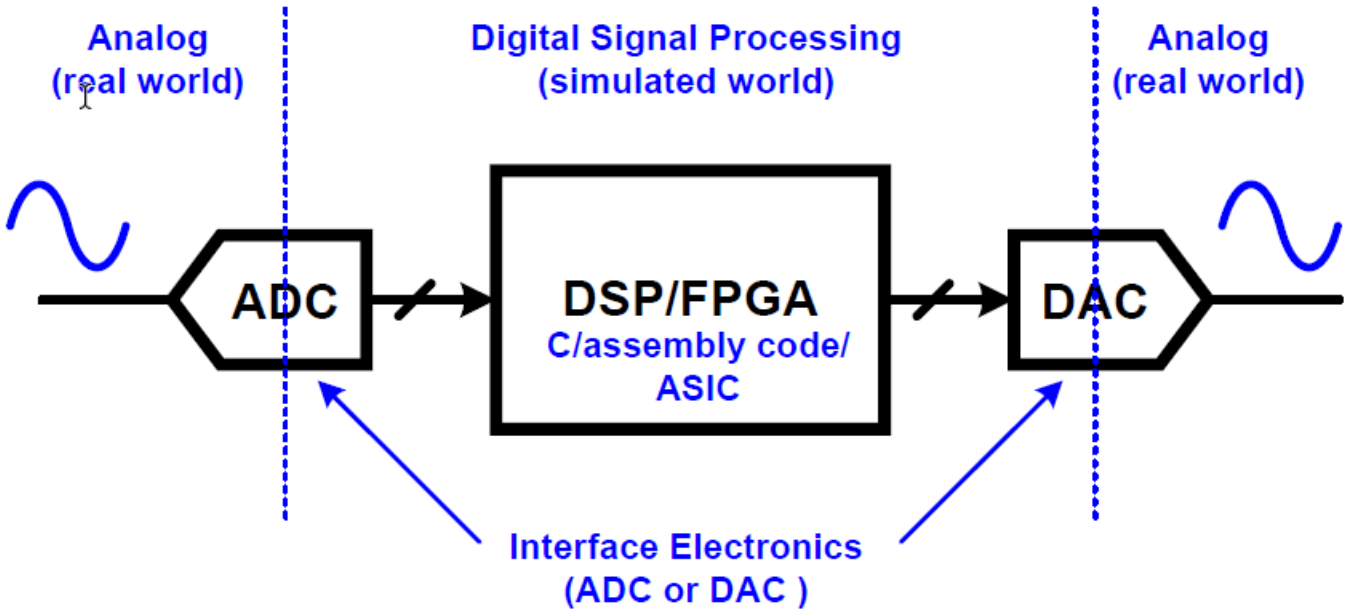
Use Real Fully-Differential Opamp



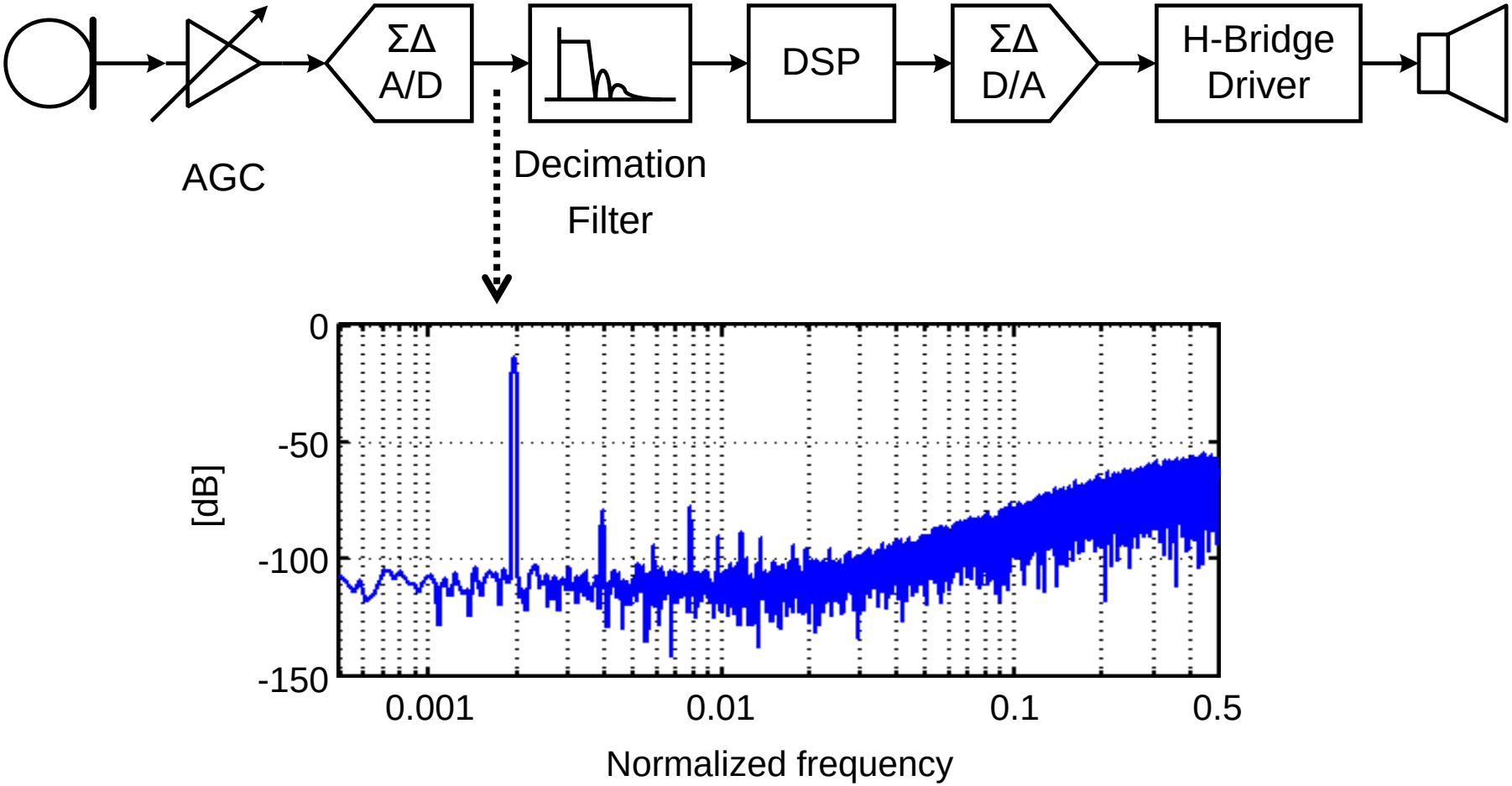
[Ref. 1] A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.

Why Data Converter?

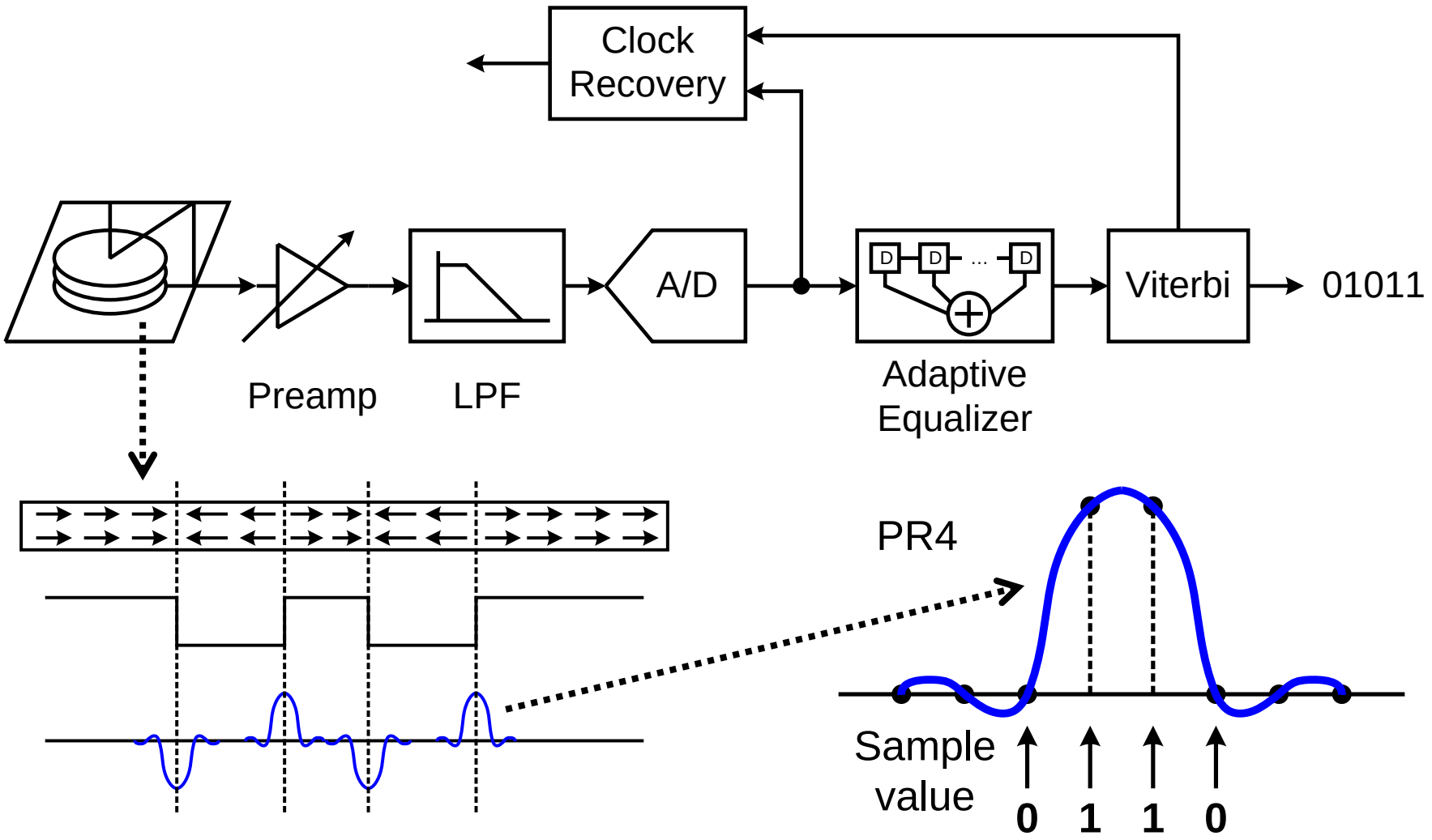
- Real world signals are analog
- Technology scaling is good for digital
- Lots of computation can be done cheap in digital domain
- Many benefits in processing data using efficient DSP algorithms



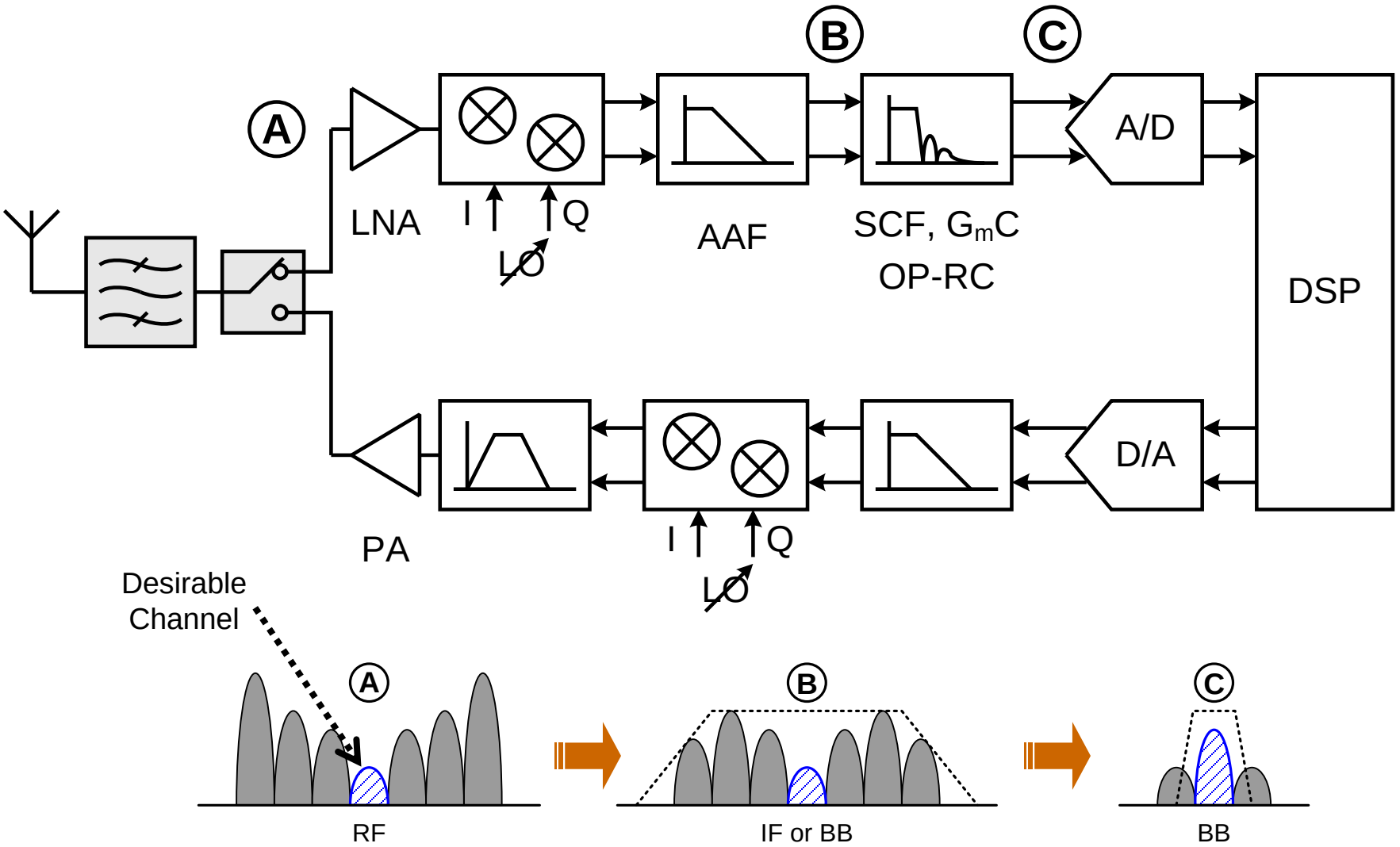
Example 1: Mixed-Signal Hearing Aid



Example 2: PRML Read Channel



Example 3: RF Transceiver



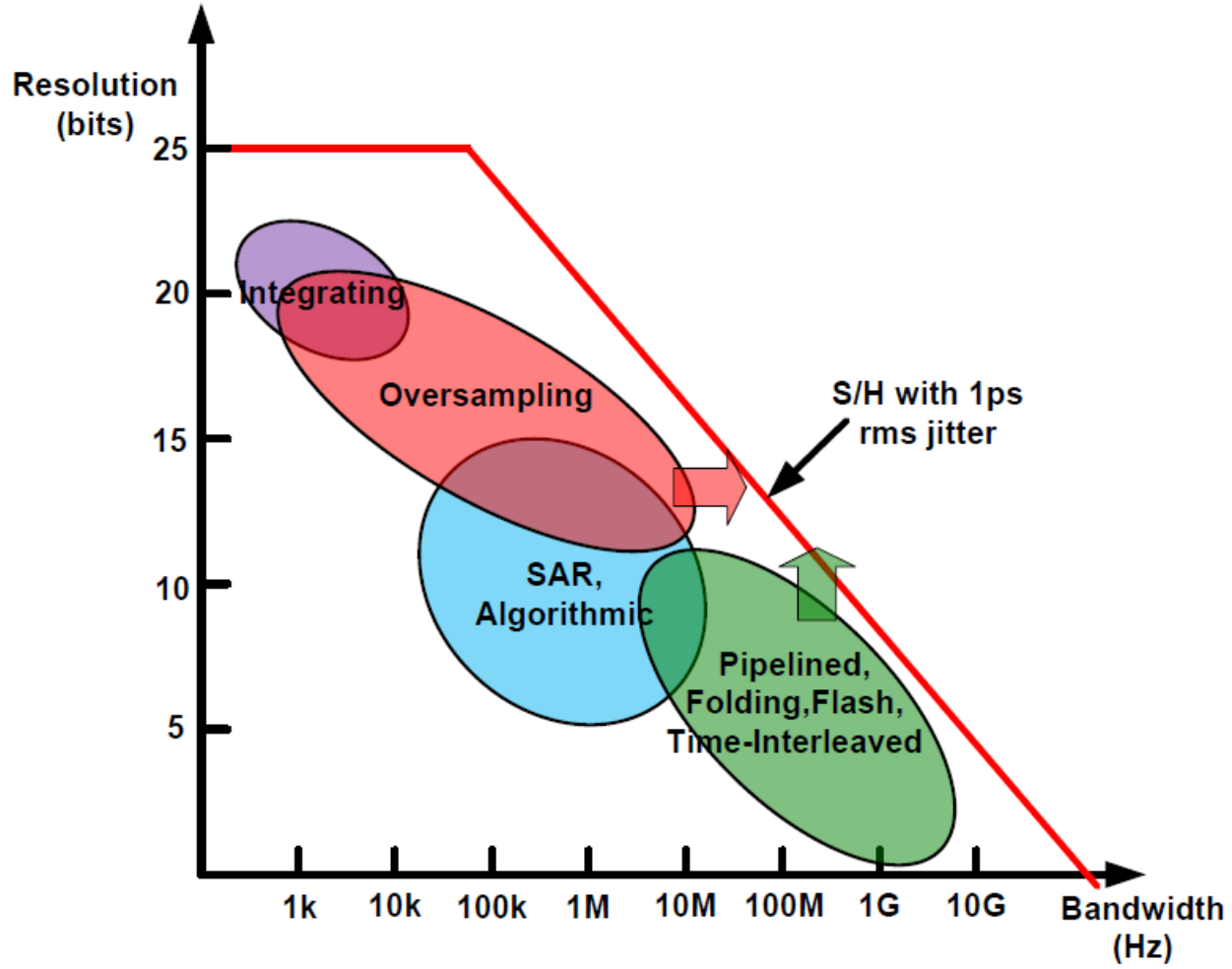
More ADC Examples

Any application using a sensor and/or an actuator

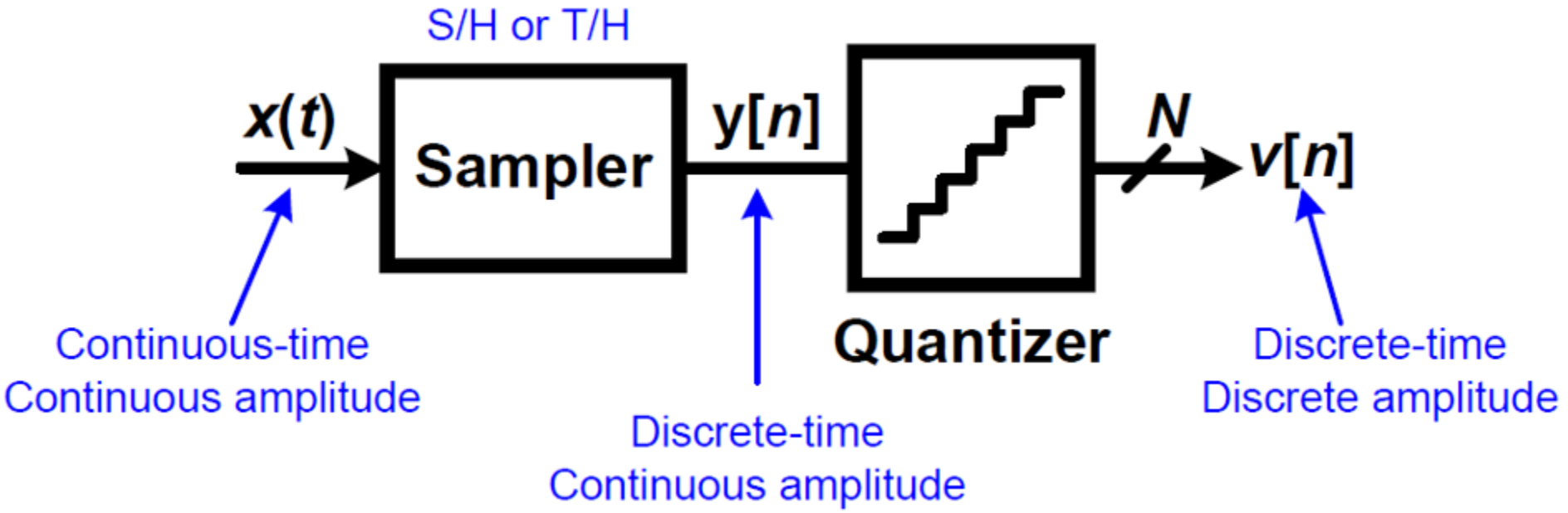
- DSL and Cable Model
- Serial/Optical links
- Audio recording and players
- Smartphone Camera
- Biomedical sensors
- IoT

Speed and resolution requirements vary with the application

ADC Architectures

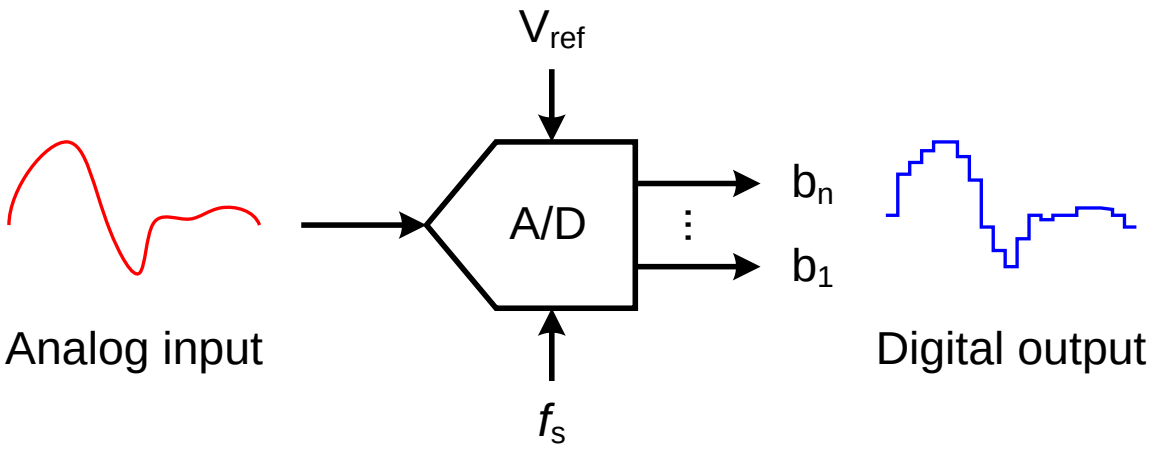


Analog-To-Digital Converter (ADC)



Nyquist-Rate ADC

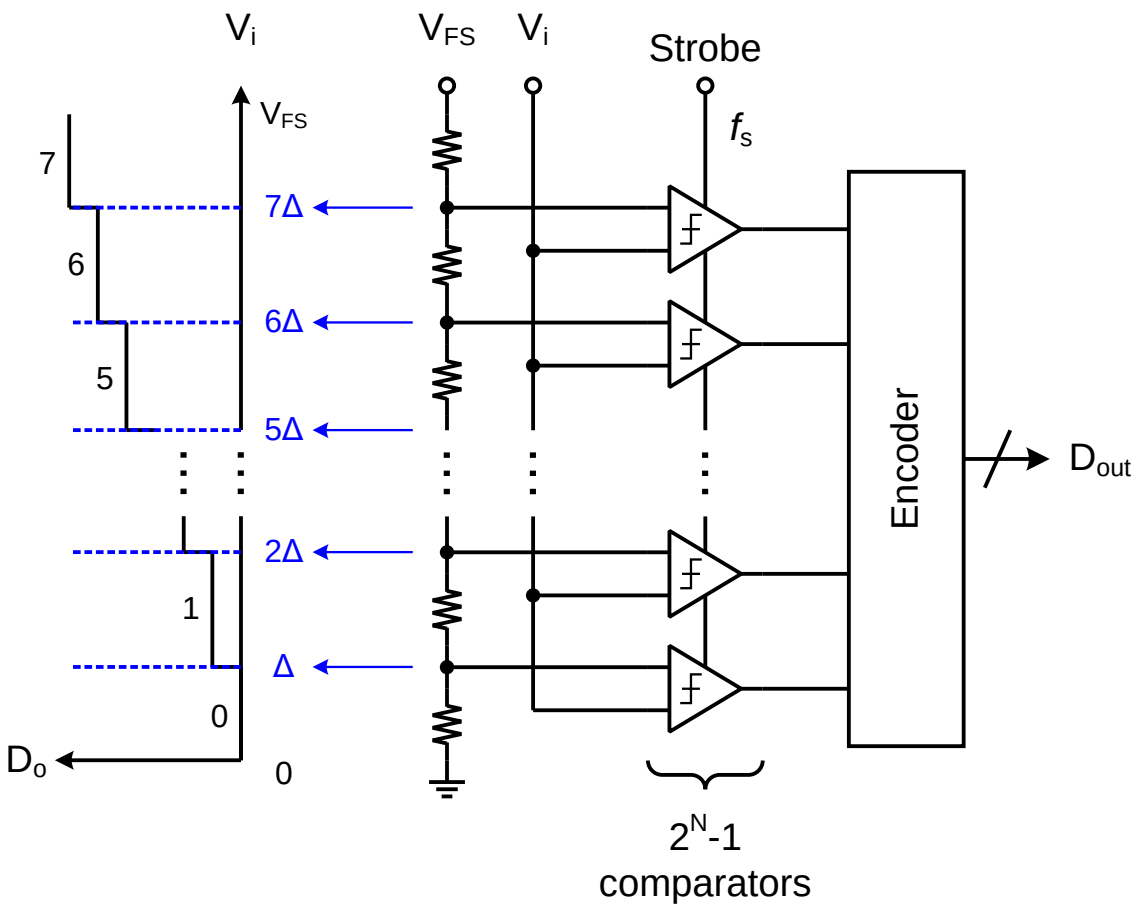
- Digitizes input signal up to Nyquist frequency ($f_N=f_s/2$)
- Sampling rate, f_s should be greater than twice the input bandwidth
- Each sample is digitized to the maximum resolution of converter



Nyquist-Rate ADC Types

- Fastest
  - Flash
- Slowest
  - Integrating (Serial)
- Slow
  - Successive approximation
  - Algorithmic (Cyclic)
- Medium
  - Sub-ranging
  - Pipeline
- Others
  - Folding & Interpolating
  - Interleaving (of flash, pipeline, or SAR) ← fastest
  - Hybrid (Pipelined SAR with Time-Interleaving) ← Getting popular

Flash ADC



- Reference ladder consists of 2^N equal size resistors
- Input is compared to 2^N-1 reference voltages
- Massive parallelism
- Very fast ADC architecture
- Throughput = f_s
- Latency = 1 T = $1/f_s$
- Complexity = 2^N