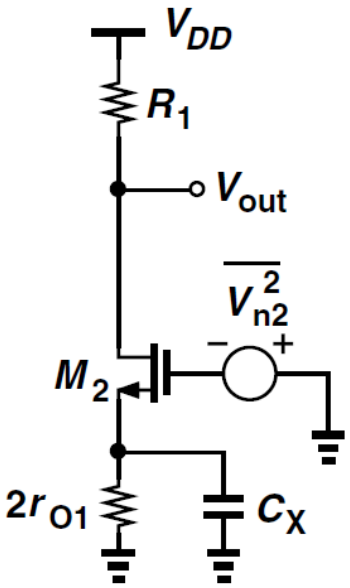
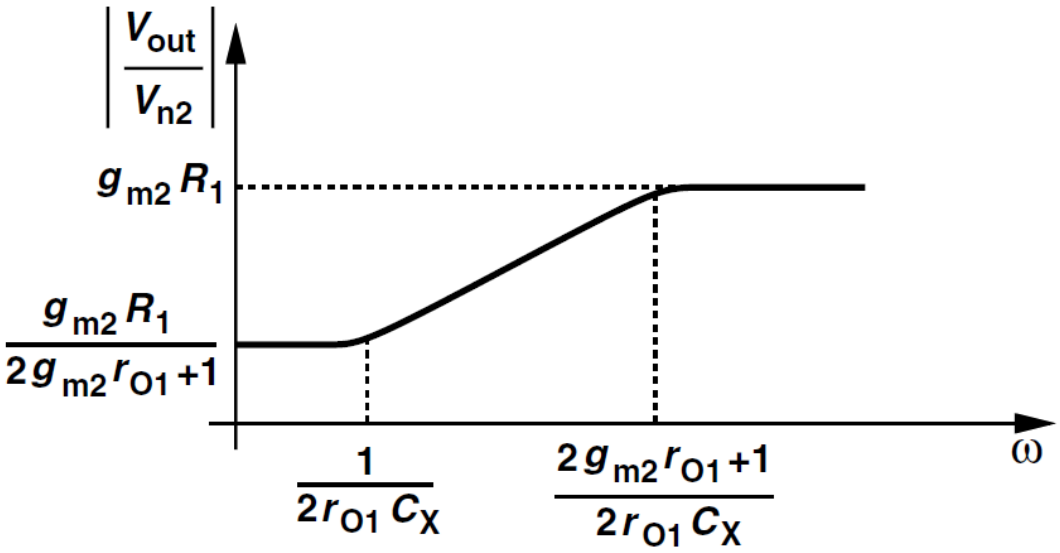
EE230-02 RFIC II
Fall 2018

Lecture 8: LNA3

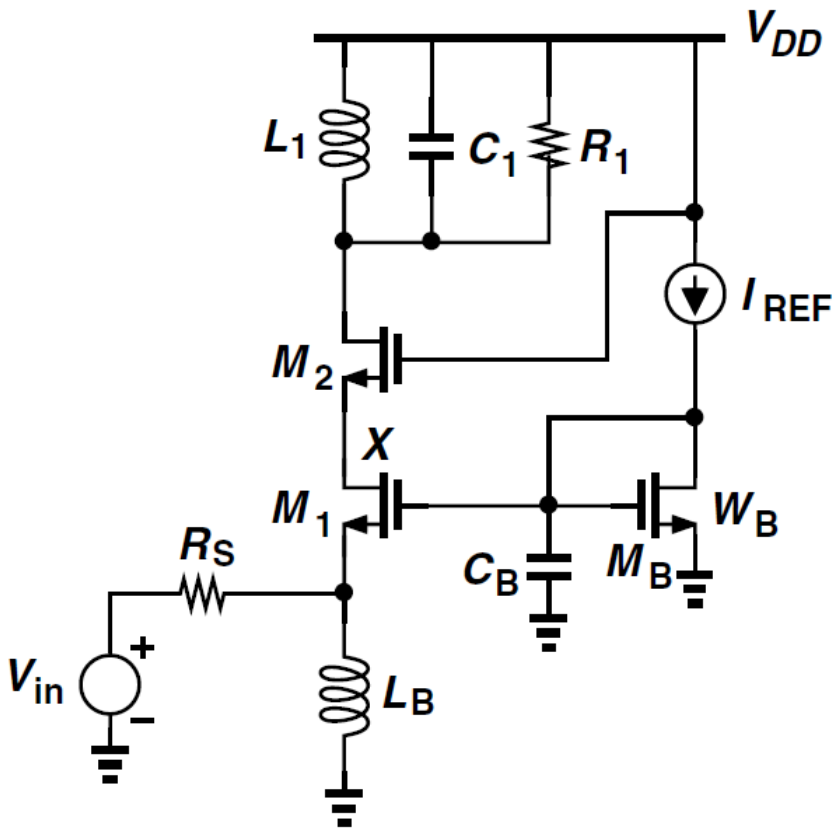
Prof. Sang-Soo Lee
sang-soo.lee@sjsu.edu
ENG-259

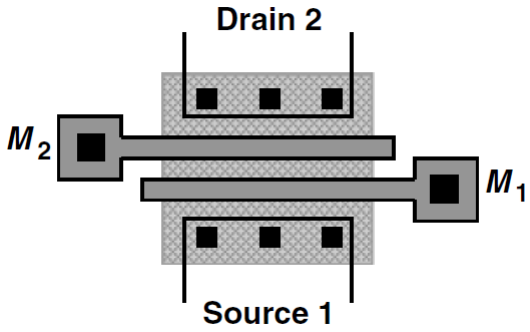
Noise From M_2





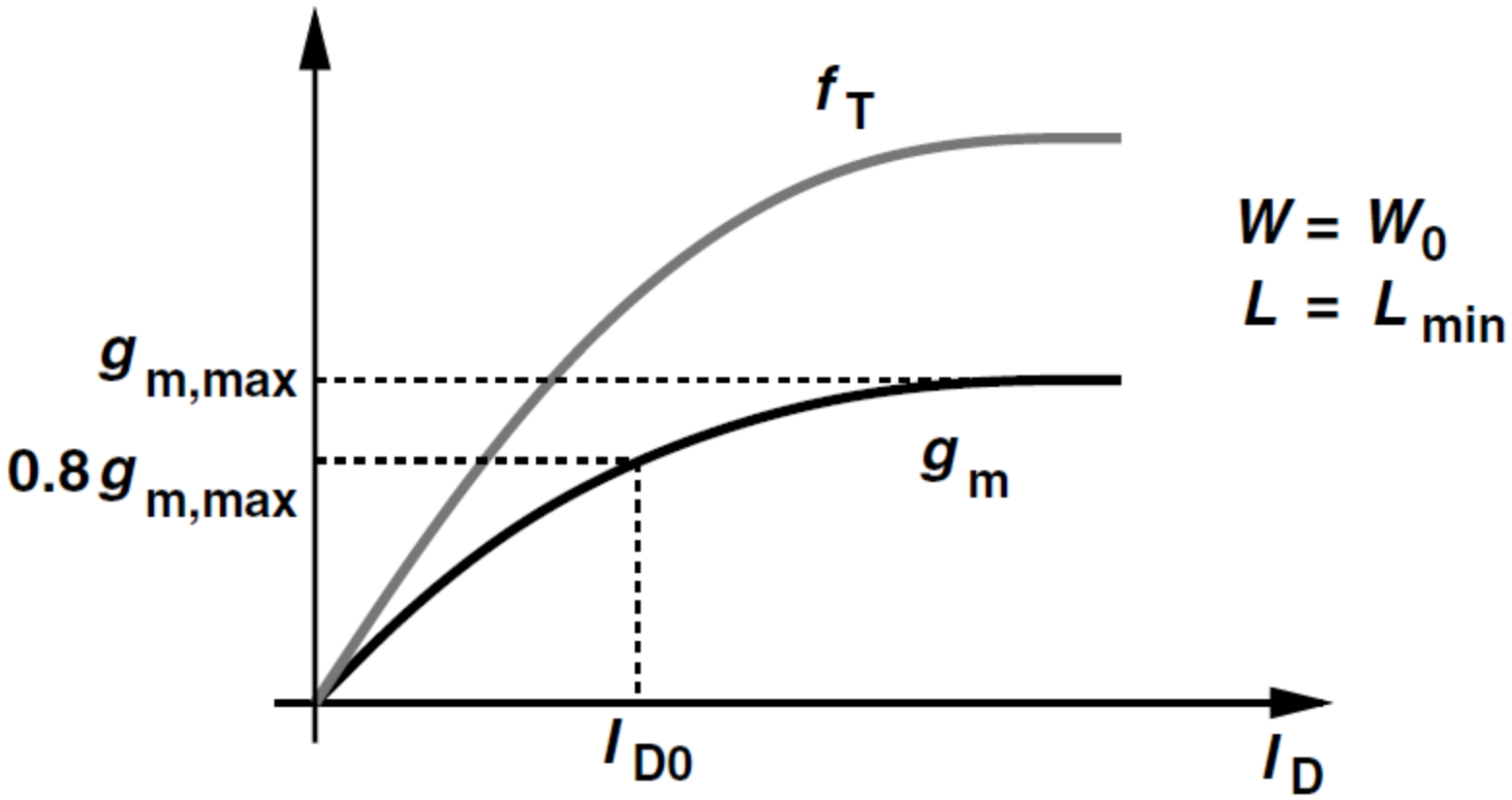
Biasing of CG Stage



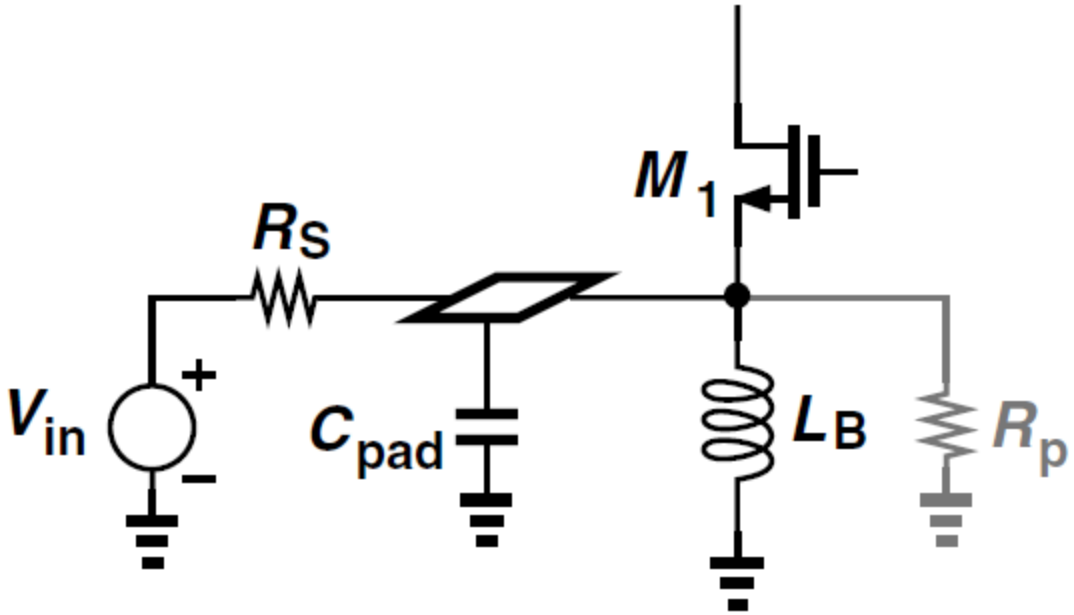


In order to avoid the noise-headroom trade-off imposed by R_B, and also cancel the input capacitance of the circuit, CG stages often employ an inductor for the bias path. Illustrated in Fig. 5.24 with proper biasing for the input transistor, this technique minimizes the additional noise due to the biasing element (L_B) and significantly improves the input matching. In modern RF design, both L_B and L_1 are integrated on the chip.

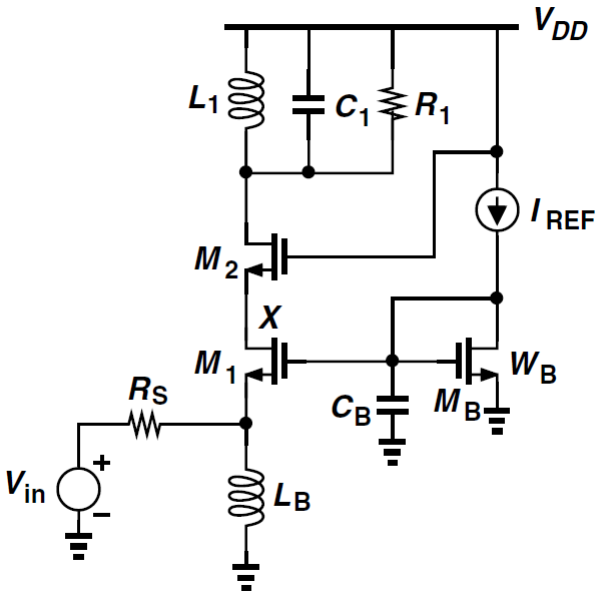
g_m and f_T vs I_D



Pad Capacitance on CG Stage



Design Procedure of CG Stage



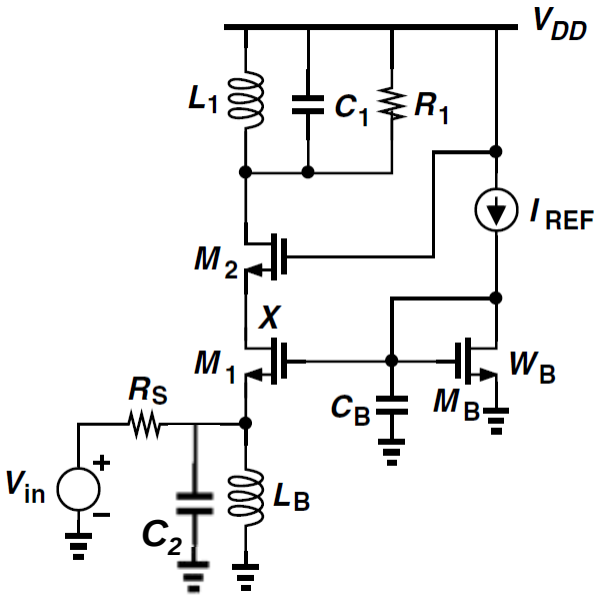
Given:

- Frequency of operation, ω_o
- Supply voltage, V_{DD}

1. Bias current of M_1 to get $1/g_m = 50\ \Omega$
2. L_B to resonate with $C_{pad} + C_{SB1} + C_{GS1}$
3. Let $I_B = 0.1 \sim 0.2\ I_{REF}$, C_B to provide <<50 Ω
4. L_1 to resonate with $C_{GD2}+C_{DB2}$
5. LNA gain proportional to $R_1=Q\omega L_1$

- NF of around 3 dB
- Gain of $V_{out}/V_{in} = R_1/(2R_S)$

CG Stage Design Example



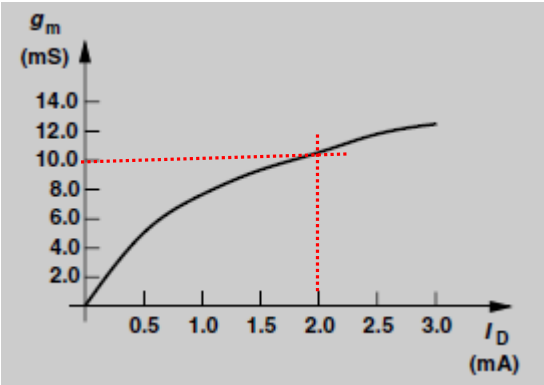
Design the LNA

$f_o = 5.5\ GHz\ in\ 65nm\ technology$

For 802.11a receiver

Assume $C_1 = C_2 = 80$ fF

g_m vs I_D for NMOS with W/L = 10μm/60nm



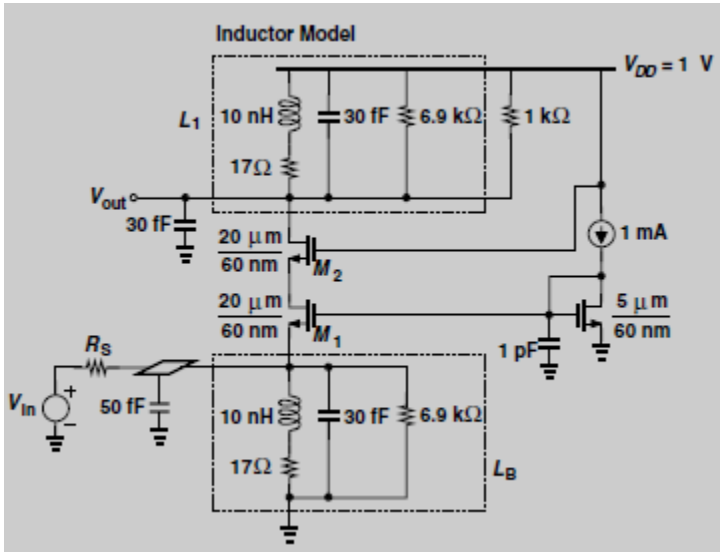
To obtain 50 Ω input resistance,

We double the width and drain current of M_1.

W/L of M_1 = 20μm/60nm.

From C_1 = 80 fF capacitance. → L_B = 10 nH

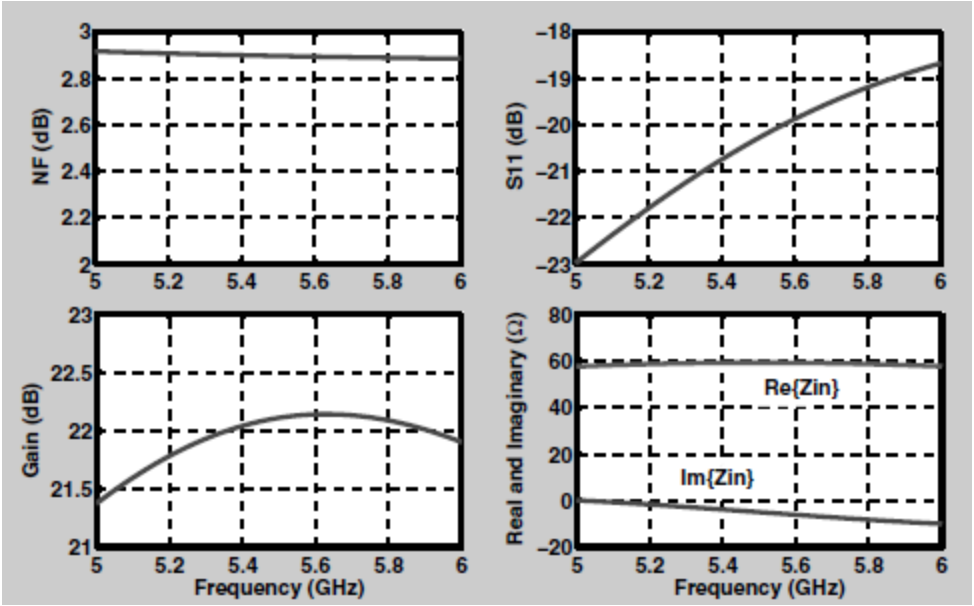
CG Stage Design Example



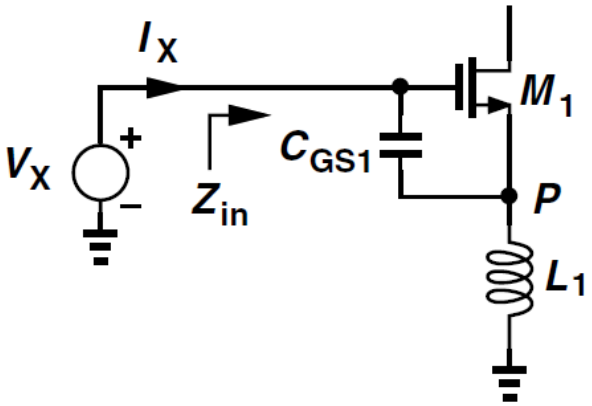
From a total load capacitance of 80 fF
→ L_B = 10 nH

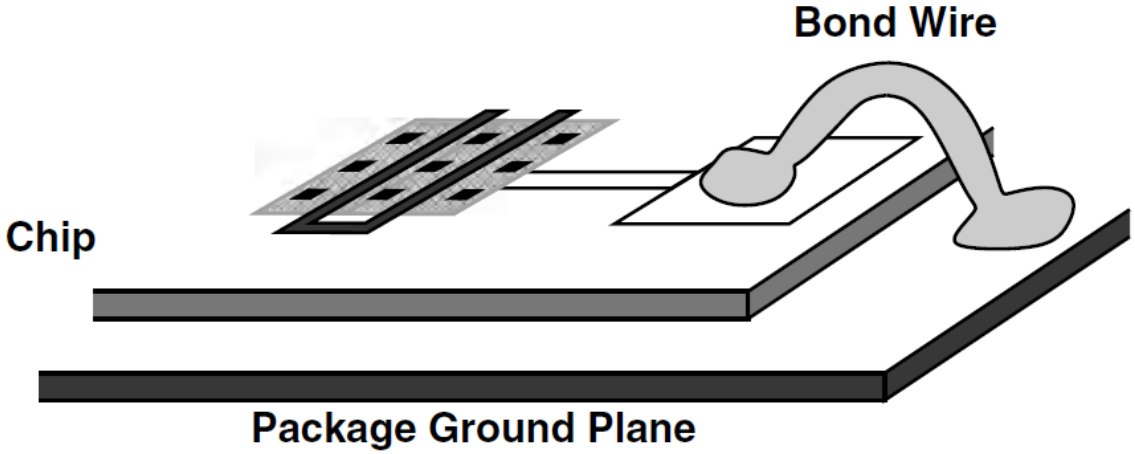
With the inductor Q of 20, the gain is high and the BW is not enough.

Therefore, add additional resistor of 1 kΩ.



Common Source with Inductive Degeneration





$$V_X = V_{GS1} + V_P = I_X/(C_{GS1}s) + \left(I_X + \frac{g_m I_X}{C_{GS1}s}\right) L_1 s$$

$$\frac{V_X}{I_X} = \boxed{\frac{1}{C_{GS1}s} + L_1 s} + \boxed{\frac{g_m L_1}{C_{GS1}}}$$

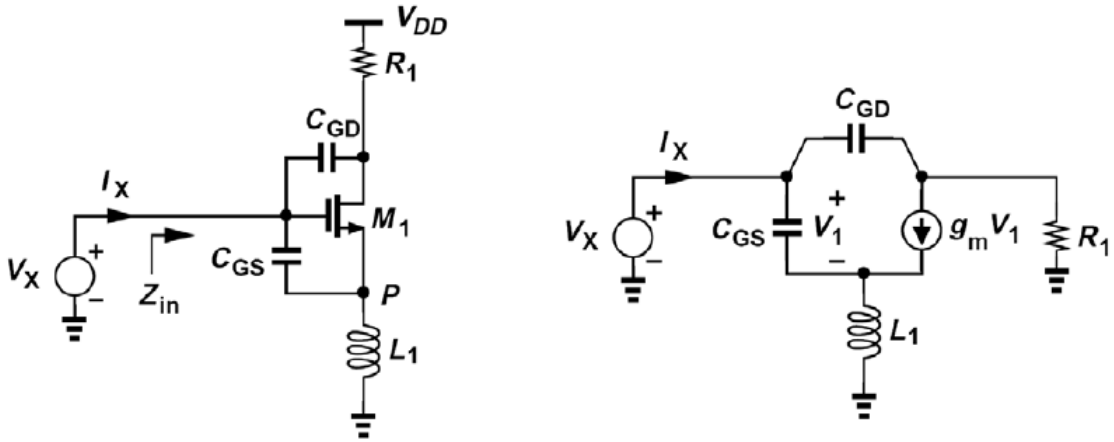
Resonate $\quad 50\ \Omega$

$$g_m/C_{GS1} \approx \omega_T\ (= 2\pi f_T)$$

$\longrightarrow$ L_1 will be small

Common Source with Inductive Degeneration

Determine the input impedance of the circuit shown below (left) if C_{GD} is not neglected and the drain is tied to a load resistance R_1. Assume $R_1 \approx 1/g_m$ (as in a cascode).



$$V_X = V_1 + (V_1 C_{GS} s + g_m V_1) L_1 s$$

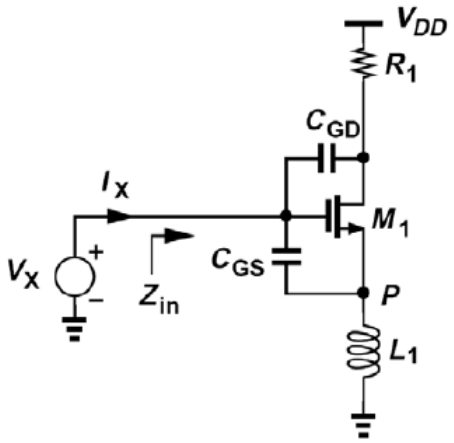
$$V_X = (I_X - V_1 C_{GS} s - g_m V_1) R_1 + (I_X - V_1 C_{GS} s) \frac{1}{C_{GD} s}$$

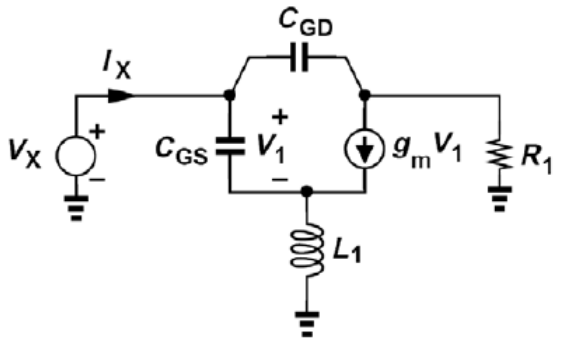
$$\frac{V_X}{I_X} = \frac{\left(R_1 + \frac{1}{C_{GD} s}\right)(L_1 C_{GS} s^2 + g_m L_1 s + 1)}{L_1 C_{GS} s^2 + (R_1 C_{GS} + g_m L_1) s + g_m R_1 + C_{GS}/C_{GD} + 1}$$

$$\frac{V_X}{I_X} \approx \left(\frac{1}{C_{GS} s} + L_1 s + \frac{g_m L_1}{C_{GS}}\right)\left[1 - \frac{2C_{GD}}{C_{GS}} - L_1 C_{GD} s^2 - \left(R_1 C_{GD} + g_m L_1 \frac{C_{GD}}{C_{GS}}\right) s\right]$$

Common Source with Inductive Degeneration

Determine the input impedance of the circuit shown below (left) if C_{GD} is not neglected and the drain is tied to a load resistance R_1. Assume $R_1 \approx 1/g_m$ (as in a cascode).



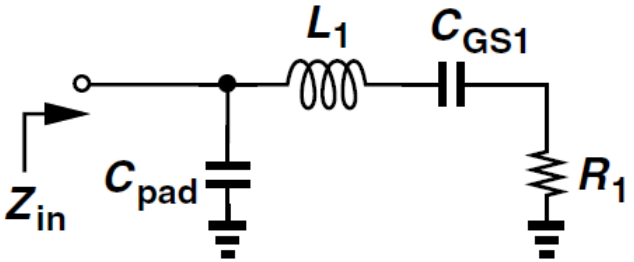


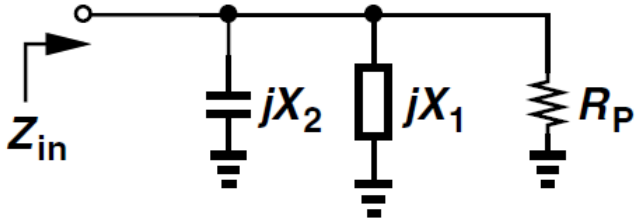
$$\frac{V_X}{I_X} \approx \left(\frac{1}{C_{GS}s} + L_1 s + \frac{g_m L_1}{C_{GS}}\right)\left[1 - \frac{2C_{GD}}{C_{GS}} - L_1 C_{GD} s^2 - \left(R_1 C_{GD} + g_m L_1 \frac{C_{GD}}{C_{GS}}\right) s\right]$$

Assuming that the first two terms are dominant, we may reduce input resistance to be close to 50ohm

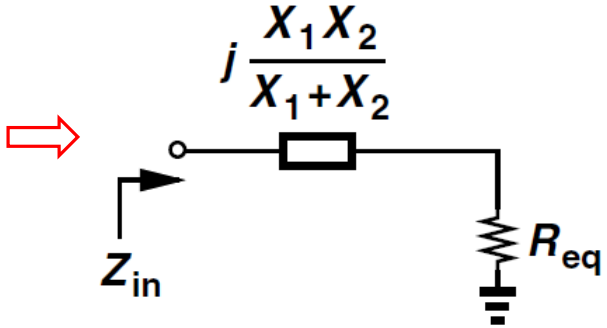
Effect of Pad Capacitance

- In addition to C_{GD}, the input pad capacitance of the circuit also lowers the input resistance.





$$R_P = \frac{X_1^2}{R_1}$$



$$R_{eq} = \left(\frac{X_1 X_2}{X_1 + X_2}\right)^2 \cdot \frac{1}{R_P} = \left(\frac{X_2}{X_1 + X_2}\right)^2 R_1$$

Assume $L_1\omega \ll 1/(C_{GS1}\omega) + 1/(C_{pad}\omega)$

$$R_{eq} \approx \left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 R_1$$

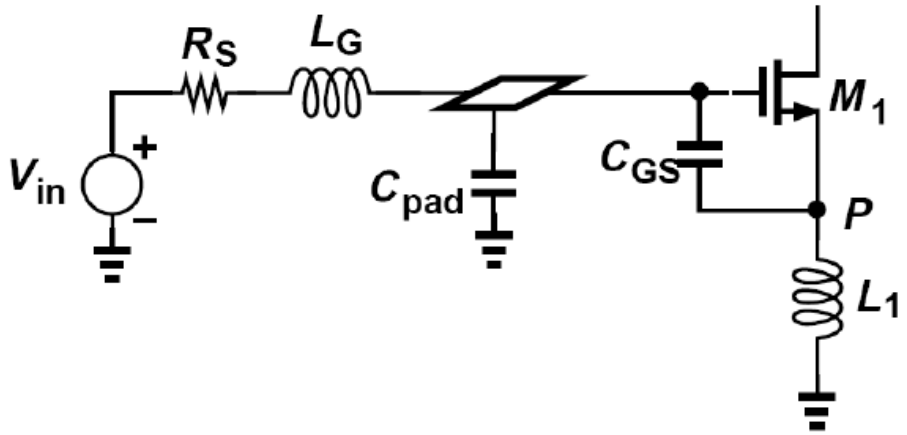
Req is reduced by a factor of 4 from R1, if Cgs ~ Cpad.

Req is reduced by a factor of 10 from R1, if Cgs ~ 0.5*Cpad.

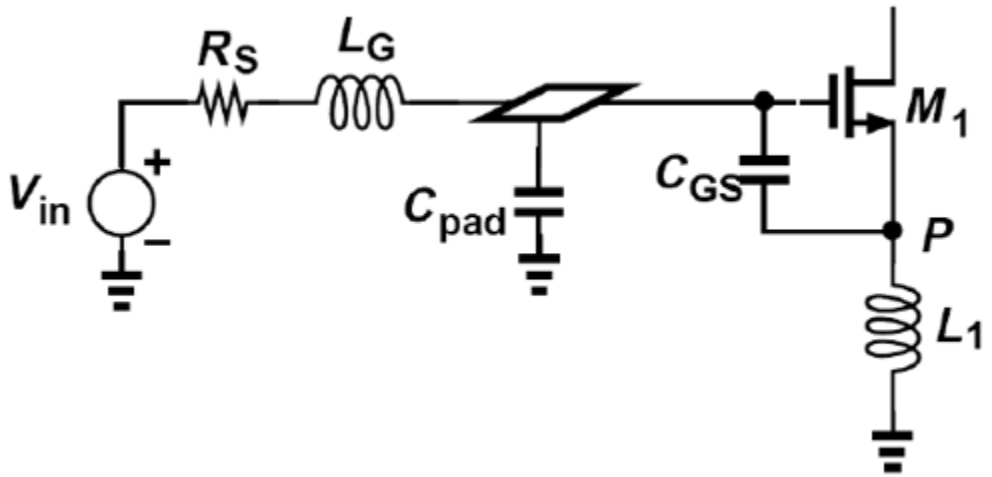
Two Observations on Effect of Pad Capacitance

- First, the effect of the gate-drain and pad capacitance suggests that the transistor f_T need not be reduced so much as to create $R_1 = 50\ \Omega$.

- Second, since the degeneration inductance necessary for $Re\{Z_{in}\} = 50\ \Omega$ is small and likely will not be sufficient to resonate with $C_{GS1} + C_{pad}$, another inductor must be placed in series with the gate.



L_G Example



Assume a 5-GHz LNA requires L_G = 2 nH.
If L_G is integrated on the chip and Q of the inductor is 5, what happens to the noise figure?

$Q = \omega L_G / R = 5 \rightarrow R = \omega L_G / Q = 12.6\ \Omega$

Therefore, noise figure will be degraded considerably.
For this reason, L_G is typically placed off-chip.