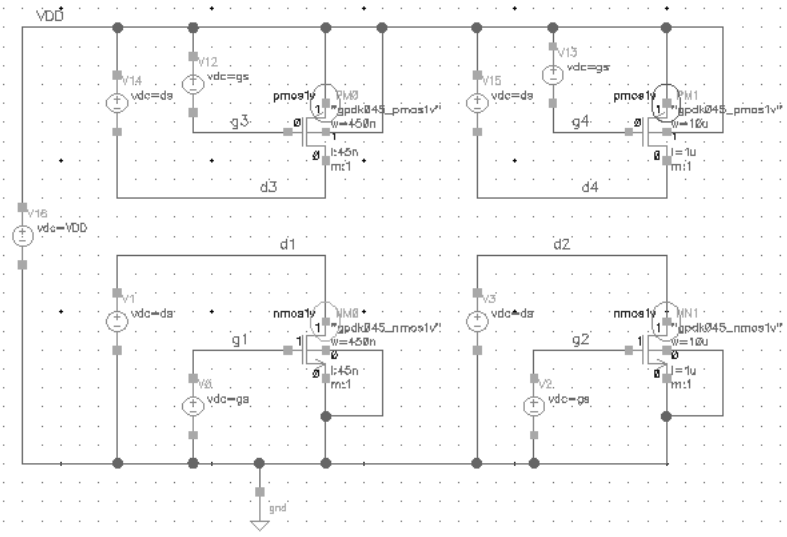
EE223 Homework #1 Aug 29, 2018

Due: Sept 12, 2018 6:00PM
Homework will not be received after due.

In this homework, you will extract some of the key MOSFET parameters used in EE223 circuit design. For all the problems, extract the required data and plots for both NMOS (nmos1v, nmos2v) and PMOS (pmos1v, pmos2v) devices. You must submit the screenshot of your schematics and plots for all the problems below.

1. Ids-Vds Characteristics (10 points)
    a) Draw a schematic similar to below (device sizes with W/L=450n/45n and 10u/1u) and run Cadence Spectre simulations to solve this problem. First, you will create Ids-Vds curves for nmos1v and pmos1v. To run an initial simulation, set Vds=1V, Vgs=1V. Sweep Vds from 0V to 1V in 10mV step. Run a dc sweep and plot the results. Once you verified your simulation is working, do a parametric analysis by selecting Tools->Parametric Analysis. Here you sweep Vgs from 0V to 1V in 200mV step. You should be able to get the Ids-Vds characteristic curves. Make screenshot of your results.
    b) Repeat the above for nmos2v and pmos2v transistors. Size of the transistor is W/L=1u/0.18u. Here you set Vds=Vgs=1.8V initially. Then Sweep Vds from 0V to 1.8V in 10mV step. Do a parametric analysis by sweeping Vgs from 0V to 1.8V in 300mV step. Make screenshot of your results.
2. Ids-Vgs Characteristics (10 points)
    a) Using the same schematic, you used in Problem 1, run Cadence Spectre simulations to solve this problem. First, you will create Ids-Vgs curves for nmos1v and pmos1v. To run an initial simulation, set Vds=1V, Vgs=1V. Sweep Vgs from 0V to 1V in 10mV step. Run a dc sweep and plot the results. Once you verified your simulation is working, do a parametric analysis by selecting Tools->Parametric Analysis. Here you sweep Vds from 0V to 1V in 200mV step. You should be able to get a family of Ids-Vgs curve for various Vds values. Use Cadence Calculator to perform derivative on Ids with respect to Vgs. This will give you the plot for gm vs. Vgs. Make screenshot of your results.
    b) Repeat the above for nmos2v and pmos2v transistors. Here you set Vds=Vgs=1.8V initially. Then Sweep Vgs from 0V to 1.8V in 10mV step. Do a parametric analysis by sweeping Vds from 0V to 1.8V in 300mV step. Make screenshot of your results.



3. Vt dependence on Channel Length (10 points)

a) Draw a schematic similar to below (W/L=WN/LN for NMOS and W/L=WP/LP for PMOS) and run Cadence Spectre simulations to solve this problem. First, you will create Vt vs. L curves for nmos1v and pmos1v. To run an initial simulation, set Vds=1V, Vgs=1V, WN=WP=1um and LN=LP=45nm. Run a dc sweep simulation by sweeping LN from 45nm to 1um in 45nm step while keeping LP=45nm. To plot the threshold voltage vs channel length, you have to create a file called saveop.scs in your Cadence launch directory. The saveop.scs file will include the following two lines:

save NM0:all
save PM0:all

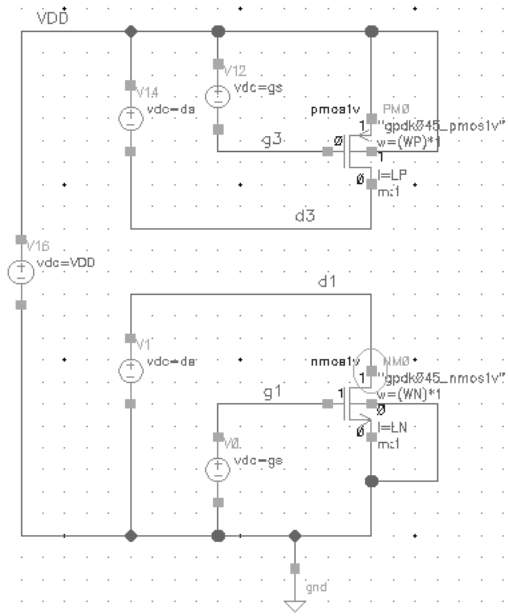
NM0 and PM0 are the name of the transistors you are using in your simulation.
Once you created saveop.scs file, launch ADE_L and choose setup->Simulation Files and then add saveop.scs in Definition Files portion. This should give you all the data necessary to plot various transistor parameters from the simulation. If you want to plot the threshold voltage in your dc sweep simulation, choose Tools->Result Brower and then check the "dc" portion in the lower left corner of the browser window. Make plots and create the screenshot. Now repeat the simulation this time by sweeping LP from 45nm to 1um in 45nm step while keeping LN=45nm. Make plots and create the screenshot.

b) Repeat the above for nmos2v and pmos2v transistors. Here you initially set Vds=Vgs=1.8V, WN=WP=1um and LN=LP=180nm. Run a dc sweep simulation by sweeping LN from 180nm to 1um in 180nm step. Make screenshot of your results. Repeat the simulation this time by sweeping LP from 180nm to 1um in 180nm step while keeping LN=180nm.

4. Vt dependence on Channel Width (10 points)

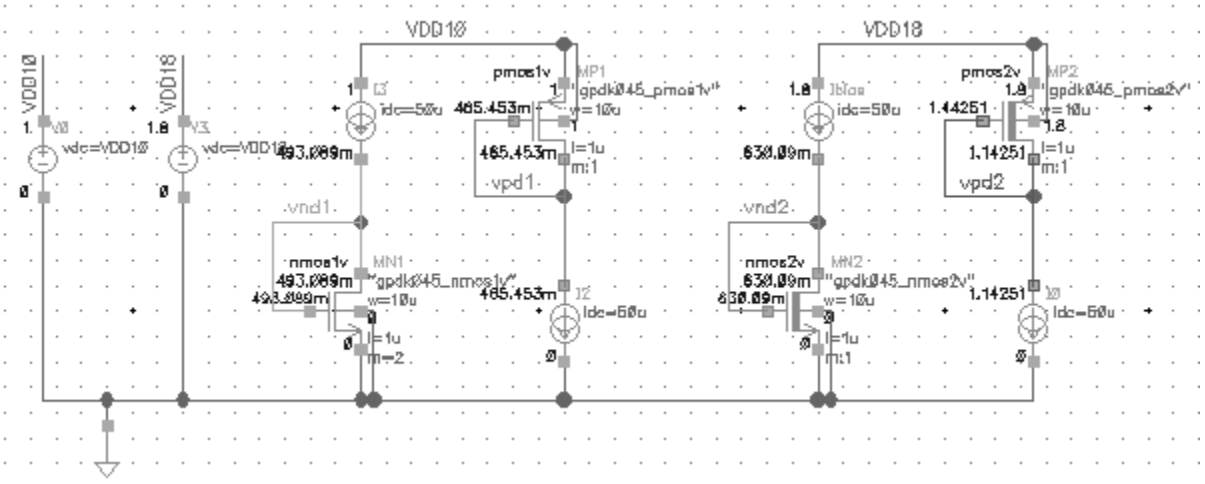
a) Using the same schematic, you used in Problem 3, initially set Vds=1V, Vgs=1V, WN=WP=1um and LN=LP=45nm. Sweep WN from 120 nm to 1.2um in 120nm step. Plot Vt vs. W and create a screenshot. Repeat the sweep for WP for the same range. Plot the result.

b) Repeat the above for nmos2v and pmos2v. This time you have to set Vds=Vgs=1.8V, WN=WP=1um and LN=LP=180nm initially. Then sweep W from 320nm to 2um in 320nm step. Do the sweep for both WP and WN one at a time and plot the results.



5. MOS parameter extraction (10 points)

a) Draw a schematic similar to below (device sizes with W/L=10um/1um and all the current sources are 50uA). Run a DC simulation to find out various transistor parameters at a given operating condition. From the operating point results, fill out the form shown below.



parameter	source	nmov1v	pmos1v	nmos2v	pmos2v
Id	given				
Vth	from sim				
Vdsat	from sim				
Vth+Vdsat	calculation				
Vgs	from sim				
2Id/Vdsat	calculation				
gm	from sim				
gds	from sim				
gm/gds	calculation				
gain (dB)	20 log (gm/gds)				
betaeff	from sim				
KP (= μCox)	calculation				

Note that "betaeff = (W/L) * KP"

b) For the circuit shown above, sweep temperature from -40C to 160C in 40C step and plot Vt vs. Temp and KP vs. Temp for all transistors.