# EE288 Data Conversions/Analog Mixed-Signal ICs
# Spring 2018

## Lecture 15: DAC Introduction

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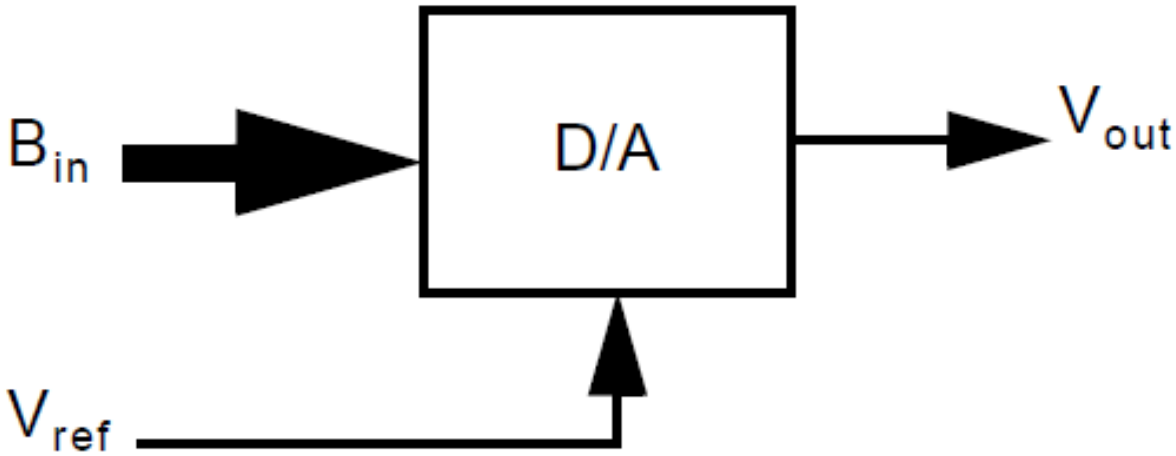
# Course Schedule – Subject to Change

| Date | Topics |
|---|---|
| 24-Jan | Course introduction and ADC architectures |
| 29-Jan | Converter basics: AAF, Sampling, Quantization, Reconstruction |
| 31-Jan | ADC dynamic performance metrics, Spectrum analysis using FFT |
| 5-Feb | ADC & DAC static performance metrics, INL and DNL |
| 7-Feb | OPAMP and bias circuits review |
| 12-Feb | SC circuits review |
| 14-Feb | Sample and Hold Amplifier - Reading materials |
| 19-Feb | Flash ADC and Comparators: Regenerative Latch |
| 21-Feb | Comparators: Latch offset, preamp, auto-zero |
| 26-Feb | ~~Finish Flash ADC~~ |
| 28-Feb | ~~DAC Architectures - Resistor, R-2R~~ |
| 5-Mar | ~~DAC Architectures - Current steering, Segmented~~ |
| 7-Mar | ~~DAC Architectures - Capacitor-based~~ |
| 12-Mar | ~~SAR ADC with bottom plate sampling~~ |
| 14-Mar | SAR ADC with top plate sampling |
| 19-Mar | Midterm Review |
| 21-Mar | Midterm exam |
| 26-Mar | Spring break |
| 28-Mar | Spring break |
| 2-Apr | Pipelined ADC stage - comparator, MDAC, x2 gain |
| 4-Apr | Pipelined ADC bit sync and alignment using Full adders |
| 9-Apr | Pipelined ADC 1.5bit vs multi-bit structures |
| 11-Apr | Fully-differential OPAMP and Switched-capacitor CMFB |
| 16-Apr | Single-slope ADC |
| 18-Apr | Oversampling & Delta-Sigma ADCs |
| 23-Apr | Second- and higher-order Delta-Sigma Modulator. |
| 25-Apr | Hybrid ADC - Pipelined SAR |
| 30-Apr | Hybrid ADC - Time-Interleaving |
| 2-May | ADC testing and FoM |
| 7-May | Project presentation 1 |
| 8-May | Project presentation 2 |
| 14-May | Final Review |
| 20-May | Project Report Due by 6 PM |

**DAC 1**

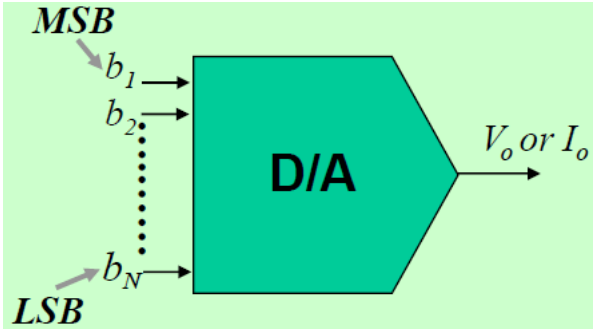
**Midterm Exam on March 21**

# DAC




$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = V_{ref} B_{in}$$

# DAC




$$N = \#\ of\ bits$$

$$V_{FS} = full\ scale\ output$$

$$\Delta = min.\ step\ size \rightarrow 1LSB$$

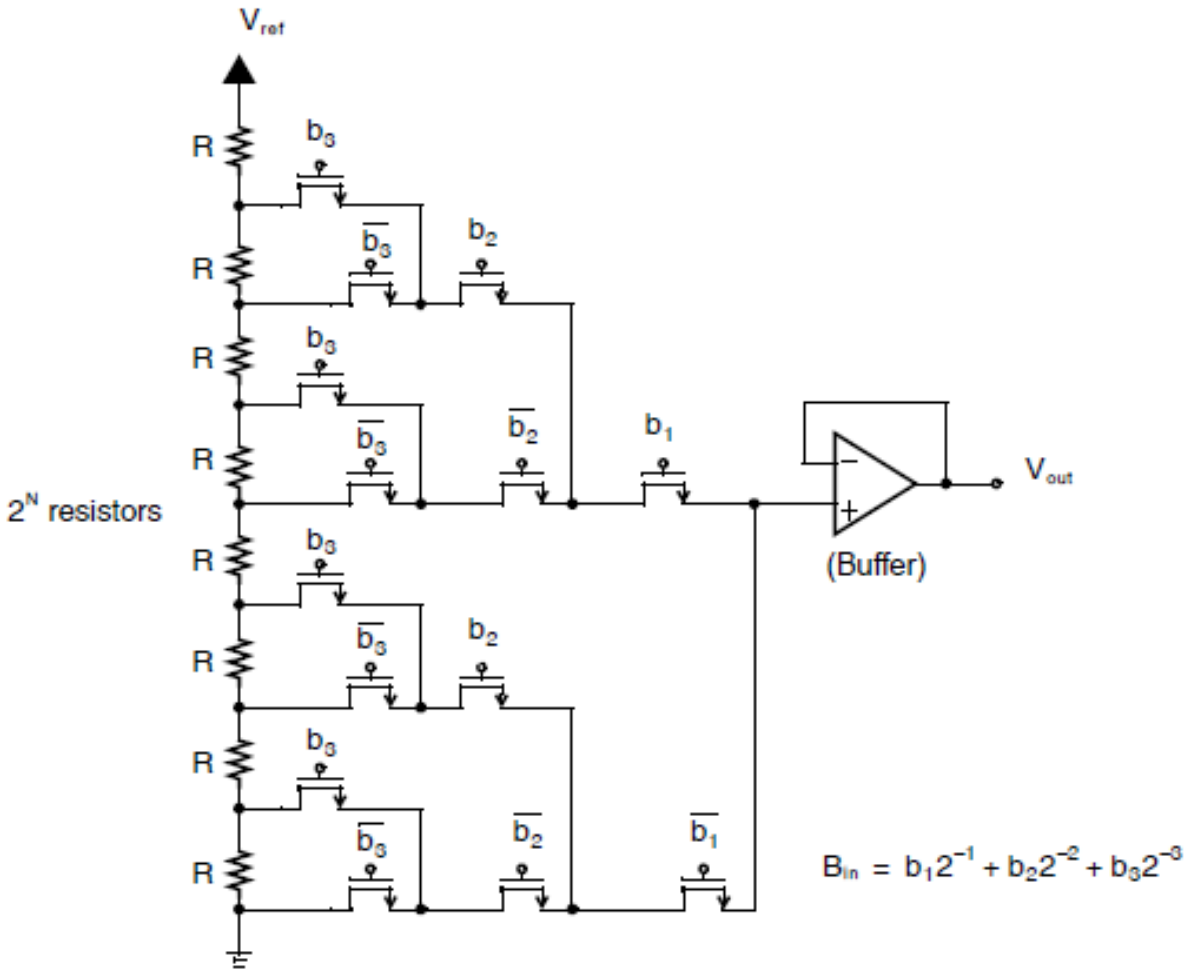
$$\Delta = \frac{V_{FS}}{2^N}$$

$$or\ N = log_2 \frac{V_{FS}}{\Delta} \rightarrow resolution$$

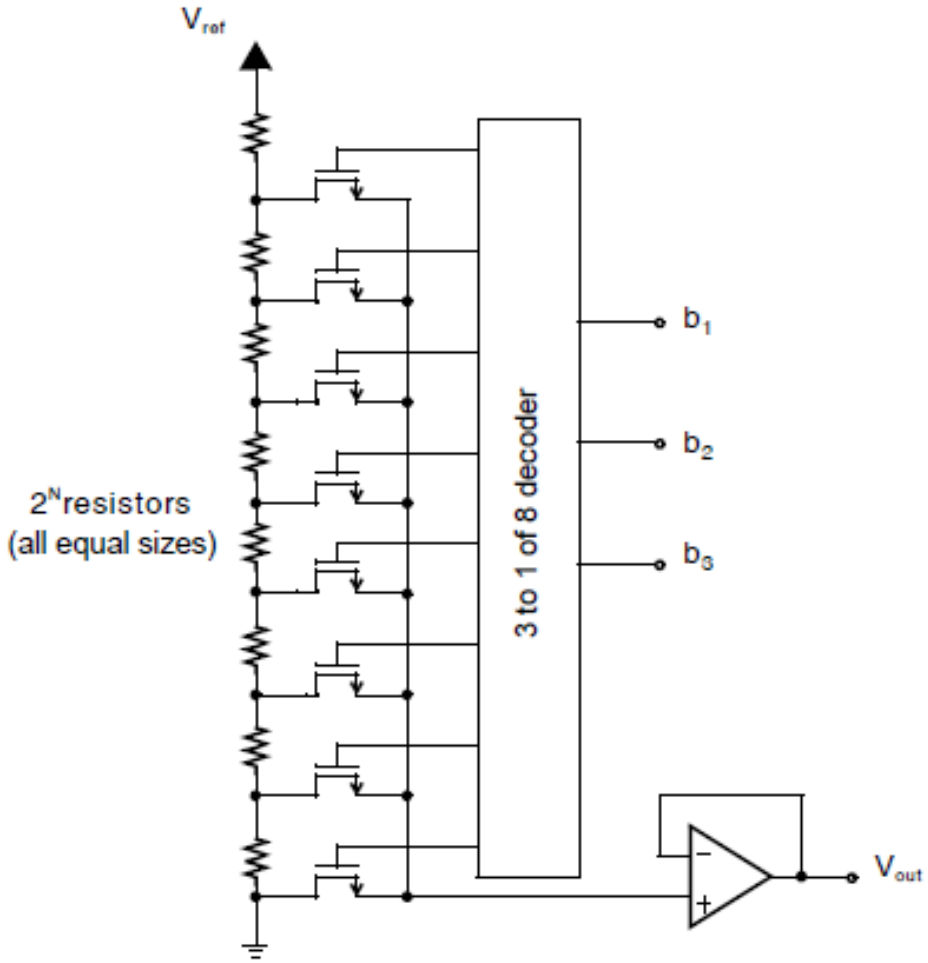
# DAC Architectures

- Various D/A architecture
  - Resistor string DAC
  - Charge Redistribution DAC
  - Current source type
- Static performance
  - Limited by component matching
  - Architectures
    - Unit element
    - Binary weighted
    - Segmented
  - Performance improvement via dynamic element matching
- Dynamic performance
  - Limited by timing errors causing glitches

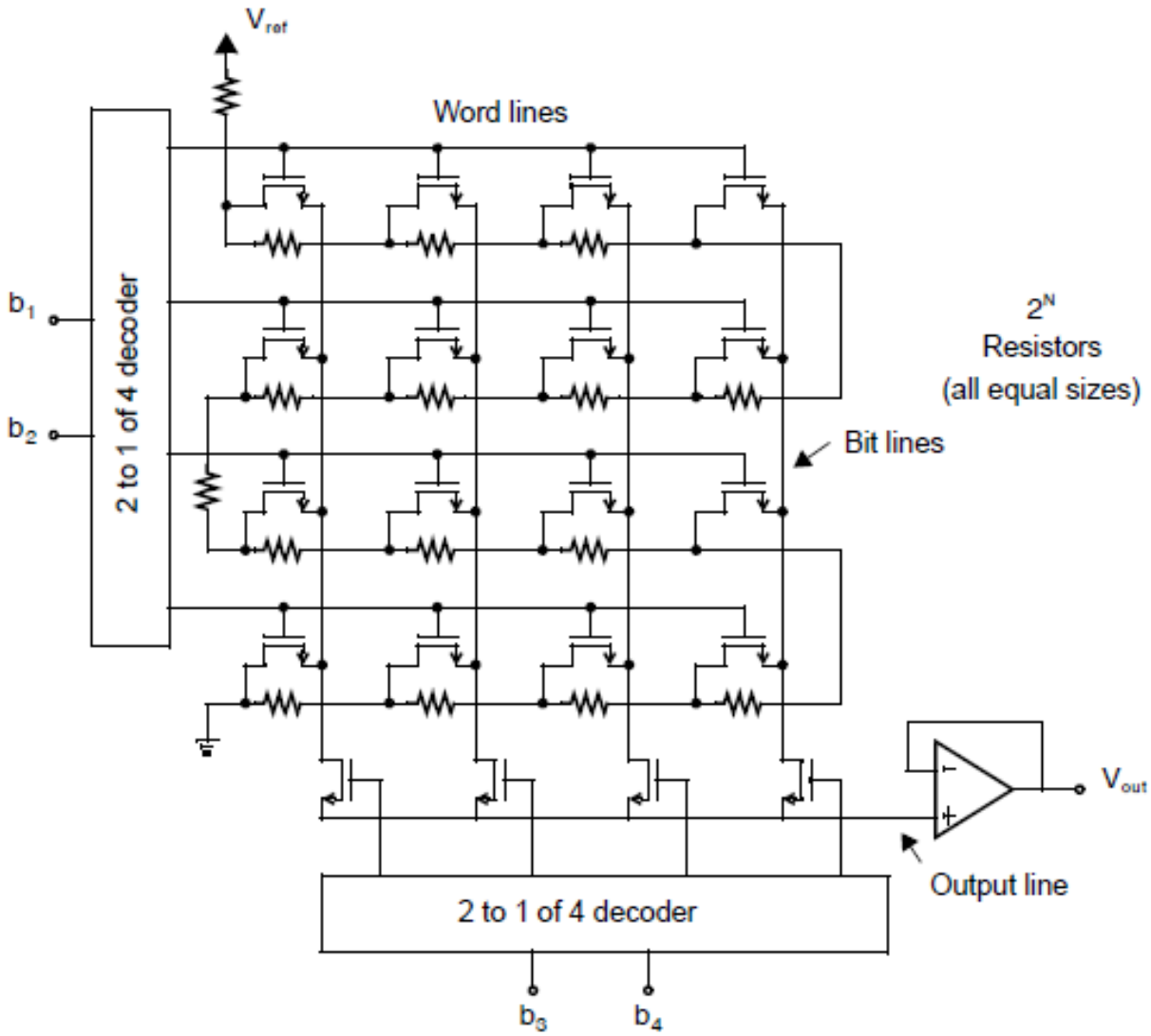
# Resistor String DAC



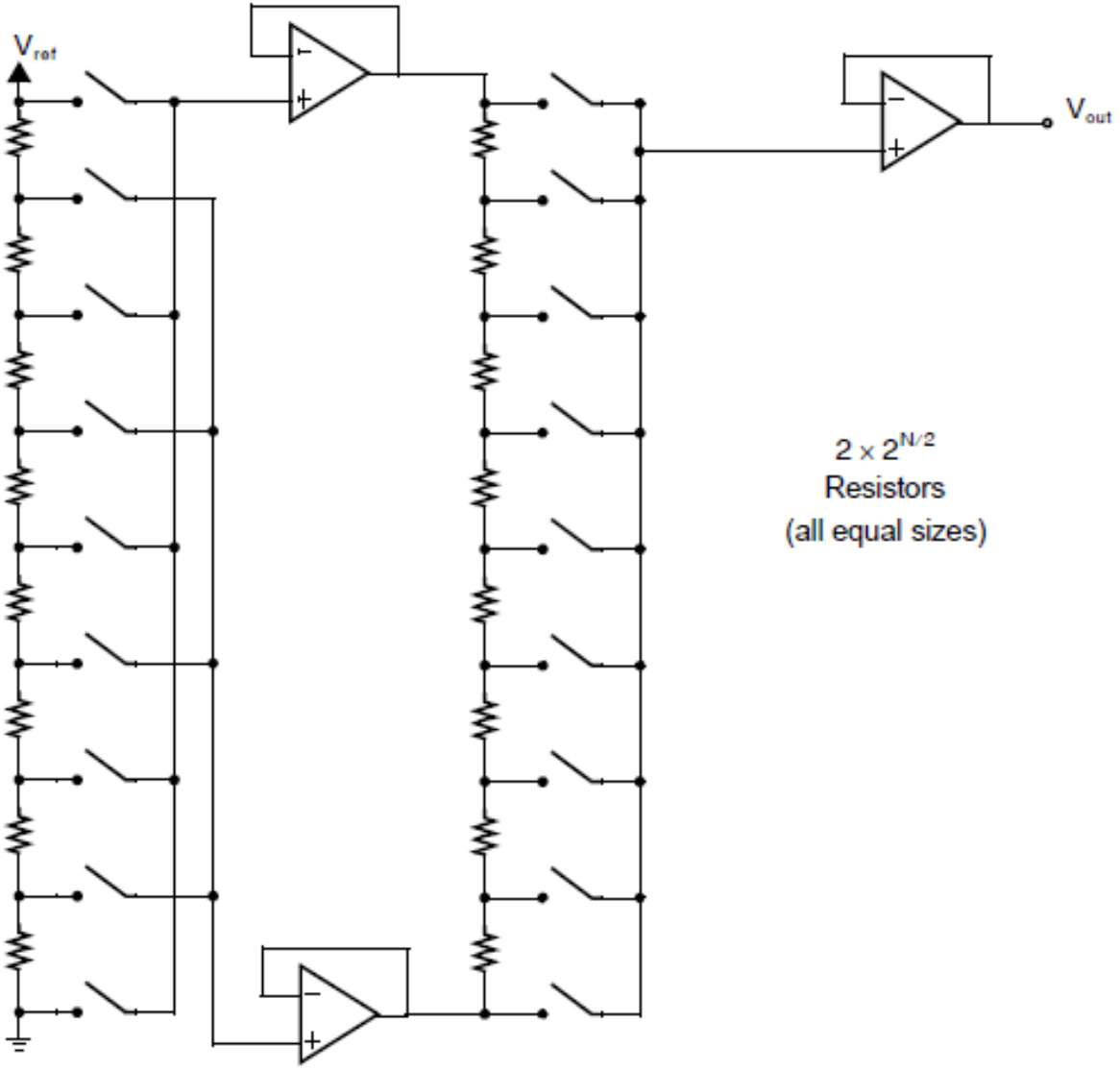
# Resistor String DAC with Decoder



# Folded Resistor String DAC

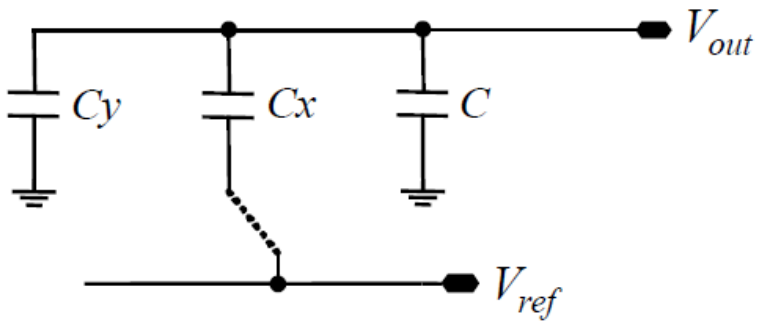


# Multiple Resistor String DAC



# Charge Redistribution DAC

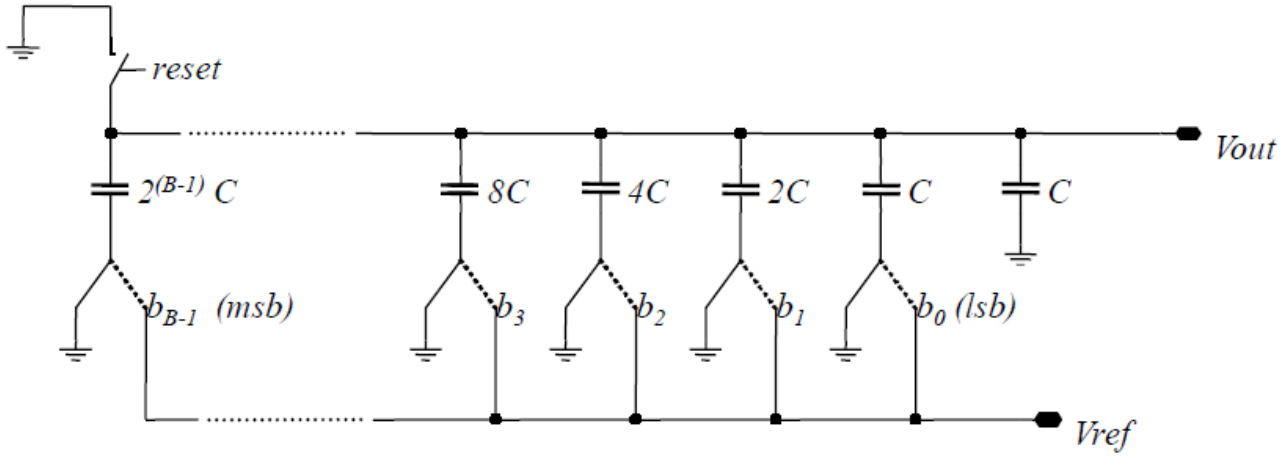
- DAC operation based on capacitive voltage division




$$V_{out} = \frac{Cx}{Cx + Cy + C} V_{ref}$$

→ Make *Cx* & *Cy* function of incoming DAC digital word

# Charge Redistribution DAC

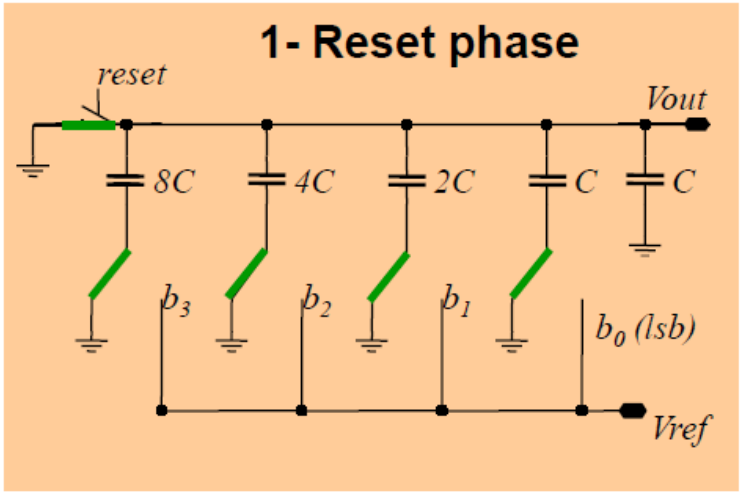


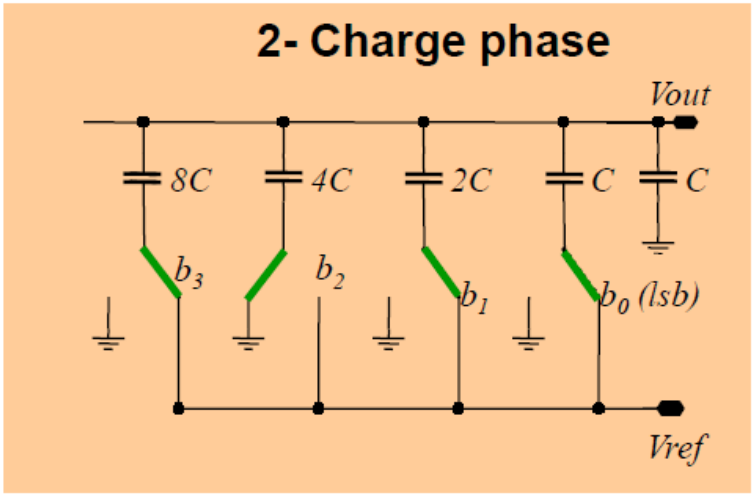

- E.g. "Binary weighted"
- B+1 capacitors & B switches (Cs built of unit elements → $2^B$ units of C)

$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C} V_{ref}$$

# Charge Redistribution DAC

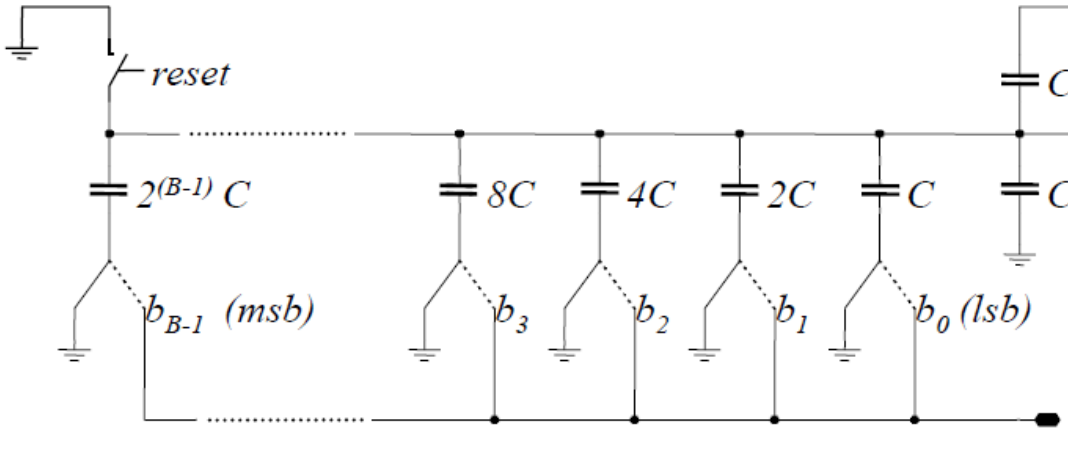
## Example: 4Bit DAC- Input Code 1011




$$V_{out} = \frac{2^0 C + 2^1 C + 2^3 C}{2^4 C} V_{ref} = \frac{11}{16} V_{ref}$$

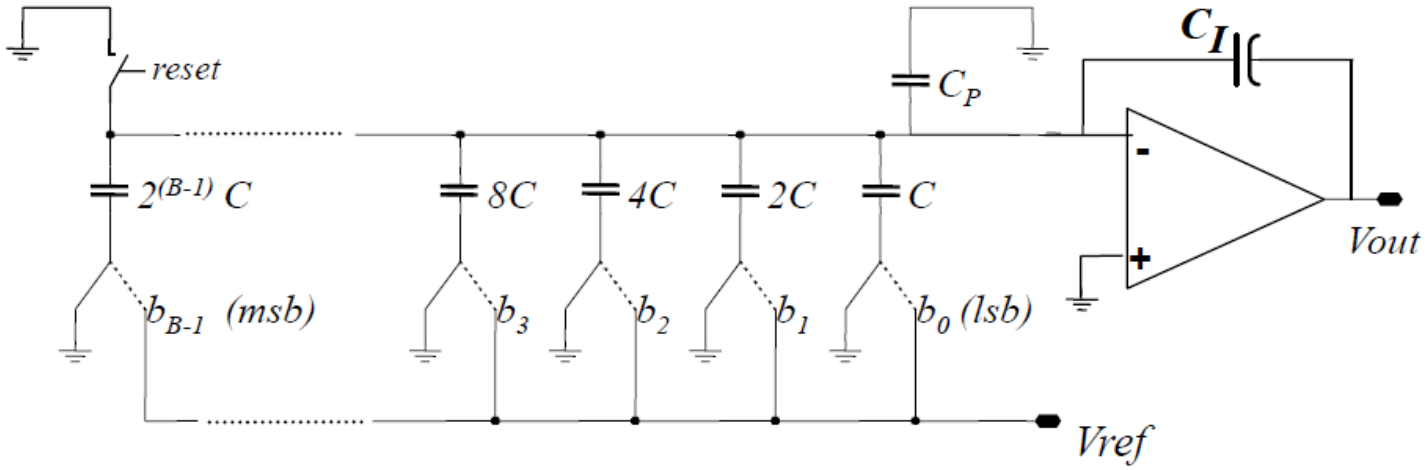
# Charge Redistribution DAC




$$V_{out} = \frac{\sum_{i=0}^{B-1} b_i 2^i C}{2^B C + C_P} V_{ref}$$

- Sensitive to parasitic capacitor @ output
  - If $C_p$ constant → gain error
  - If $C_p$ voltage dependant → DAC nonlinearity
- Large area of caps for high DAC resolution (10bit DAC ratio 1:512)
- Monotonicity depends on element matching (more later)

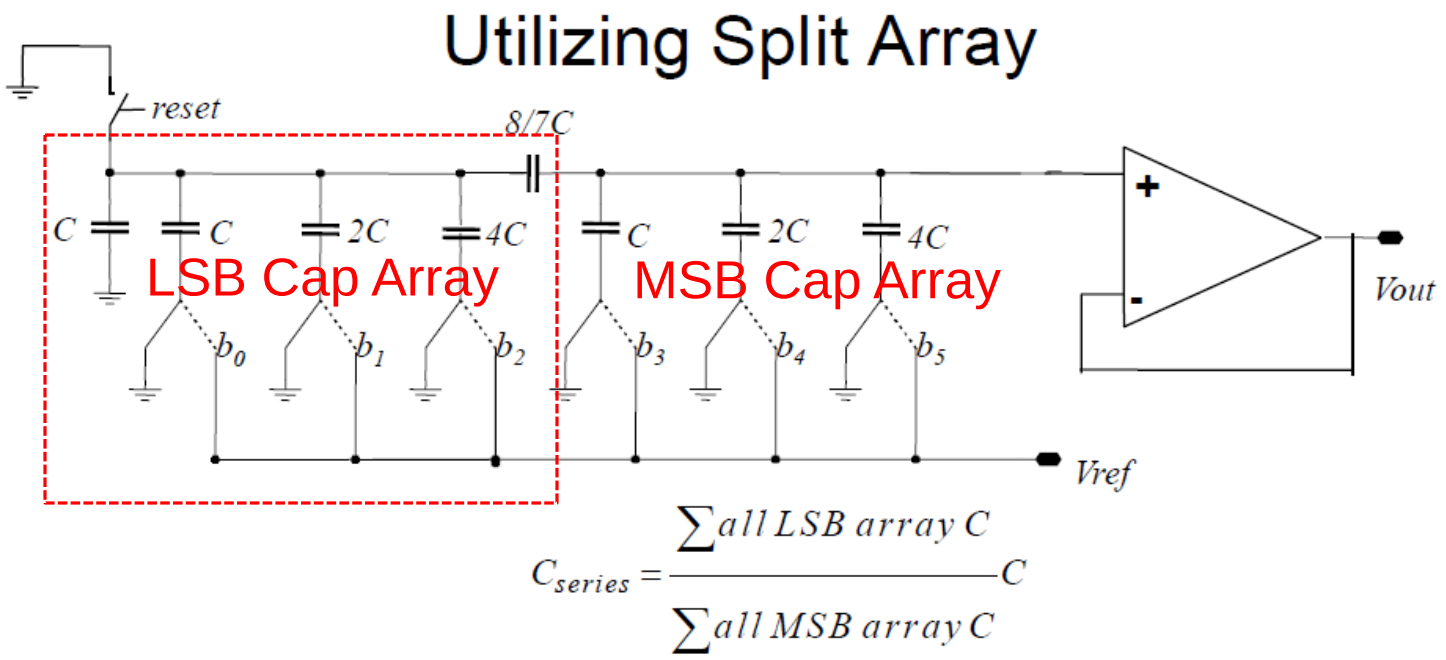
# Charge Redistribution DAC




$$V_{out} = -\frac{\sum_{i=0}^{B-1} b_i 2^i C}{C_I} V_{ref}, \quad C_I = 2^B C \rightarrow V_{out} = -\frac{\sum_{i=0}^{B-1} b_i 2^i}{2^B} V_{ref}$$

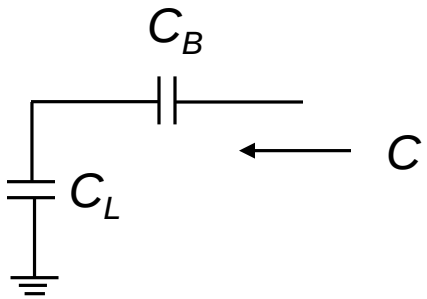
- Opamp helps eliminate the parasitic capacitor effect by producing virtual ground at the sensitive node since $C_P$ has zero volts at start & end
  - Issue: opamp offset & speed- also double capacitor area

# Charge Redistribution DAC with Split Cap




- Split array→ reduce the total area of the capacitors required for high resolution DACs
  - E.g. 10bit regular binary array requires 1024 unit Cs while split array (5&5) needs 64 unit Cs
  - Issue: Sensitive to series capacitance parasitic capacitor

# Bridge Cap




$$C = \frac{C_B C_L}{C_B + C_L}$$

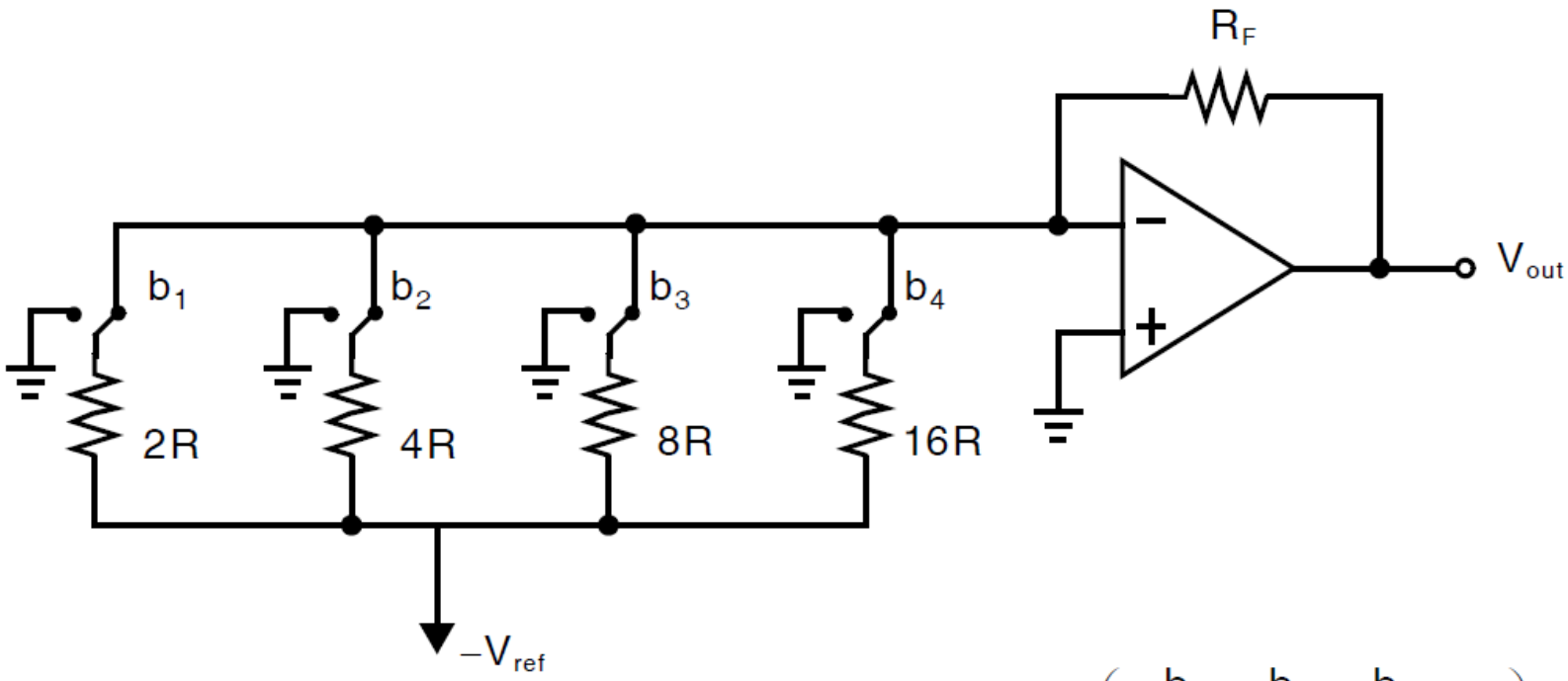
$$C_B + C_L = C_B C_L$$

$$C_B(C_L - 1) = C_L$$

$$C_B(C_L - 1) = C_L$$

$$C_B = \frac{C_L}{C_L - 1}$$

# Current Based DAC using Binary Weighted R



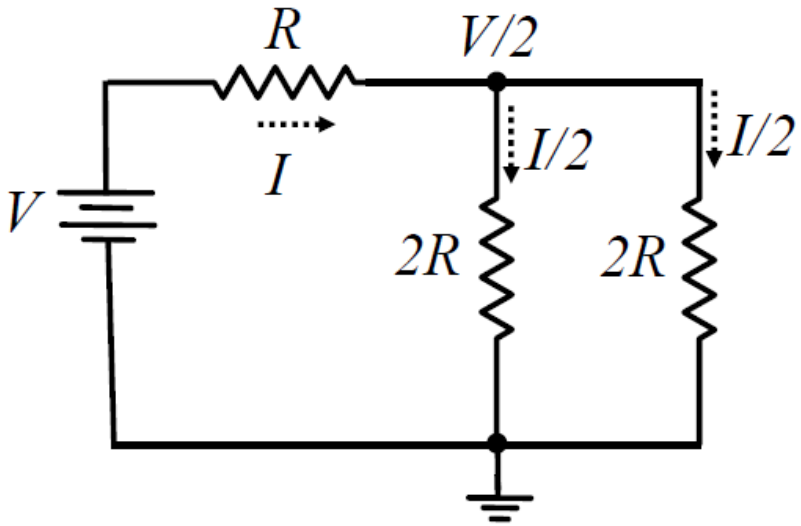

$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \dots\right)$$

$$= \left(\frac{R_F}{R} V_{ref}\right) B_{in}$$

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots$$

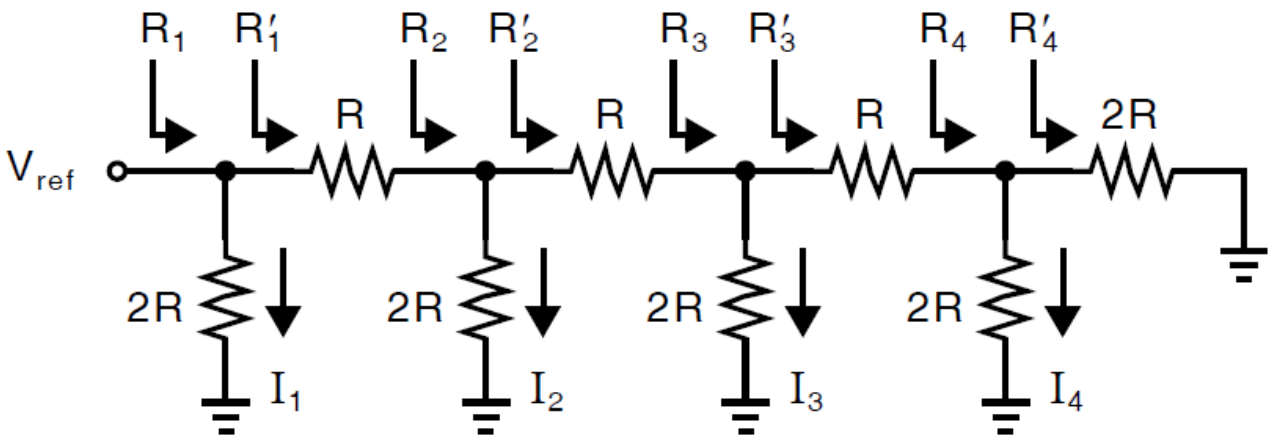
# Current Based DAC using R-2R Ladder

- R-2R DAC basics:
  - Simple R network divides both voltage & current by 2




Increase # of bits by replicating circuit

# R-2R Resistance Ladder




$$R_4' = 2R$$

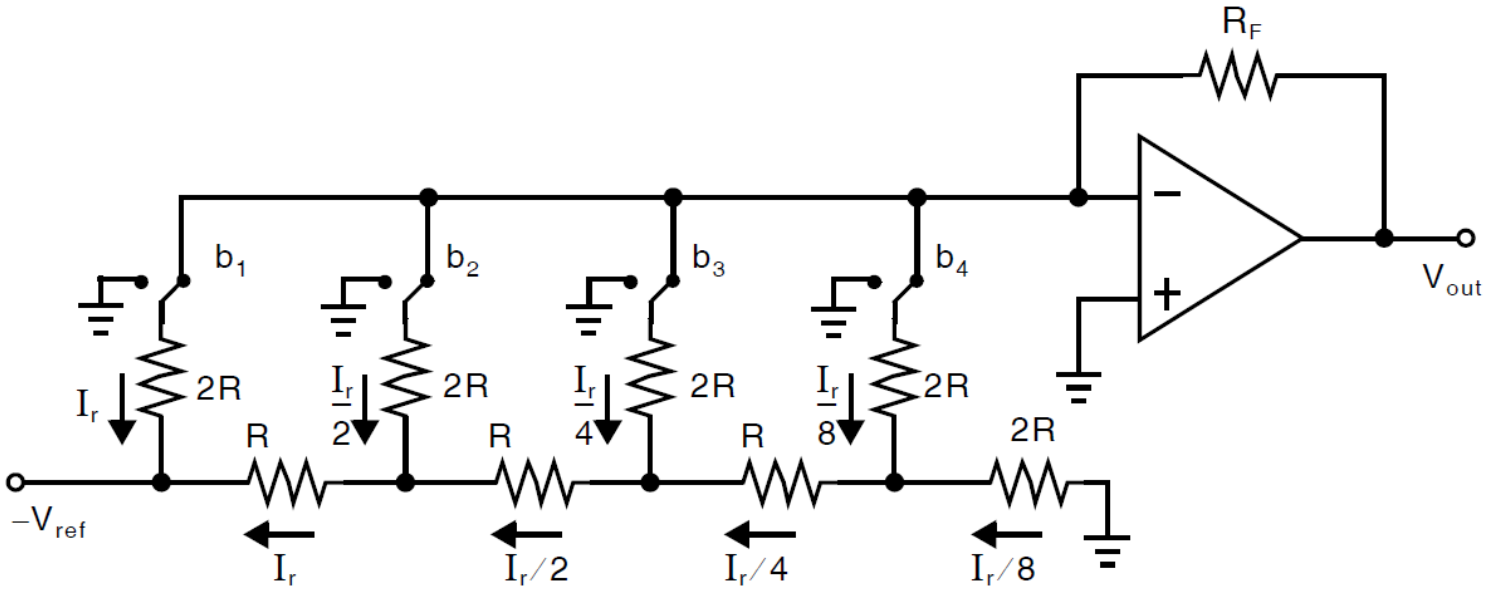
$$R_4 = 2R \parallel 2R = R$$

$$R_3' = R + R_4 = 2R$$

$$R_3 = 2R \parallel R_3' = R$$

$$I_1 = \frac{V_{ref}}{2R} \qquad I_2 = \frac{V_{ref}}{4R} \qquad I_3 = \frac{V_{ref}}{8R}$$

# Current Based DAC using R-2R Ladder

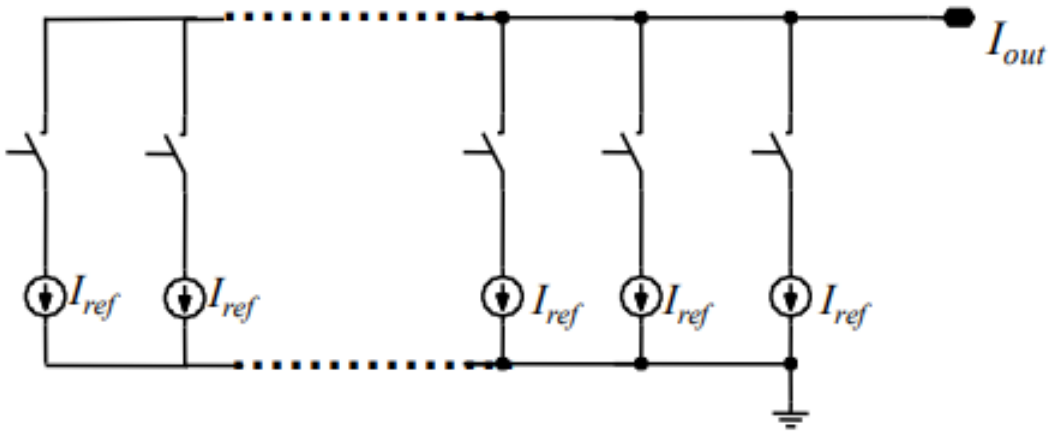



$$I_r = V_{ref}/(2R)$$

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref}\left(\frac{R_F}{R}\right) \sum_{i=1}^{N} \frac{b_i}{2^i}$$

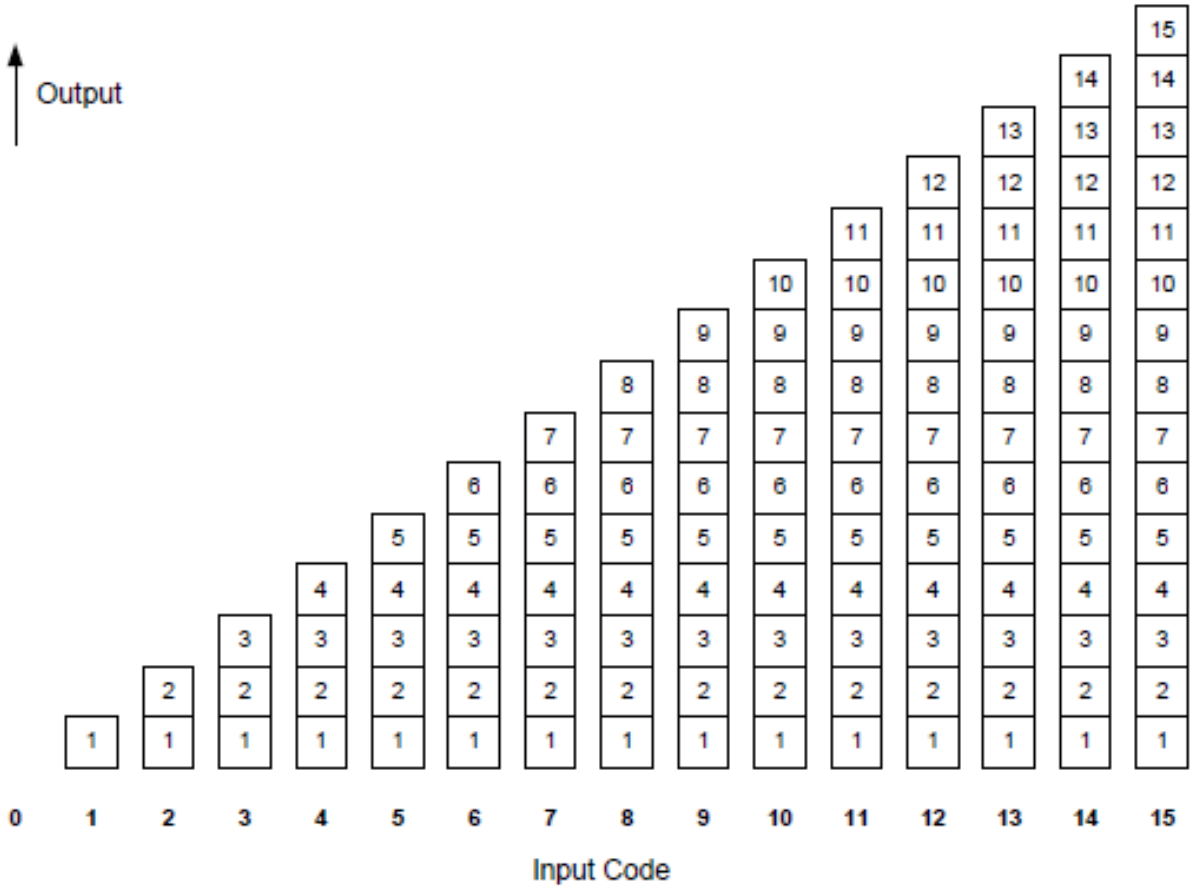
***Key Point:*** *R-2R ladder D/A converters produce binary-weighted currents without the need for a complete array of binary-weighted resistors. Instead, only 2:1 component ratios are needed, a significant savings for high-resolution converters.*

# Unit Element Current Source DAC

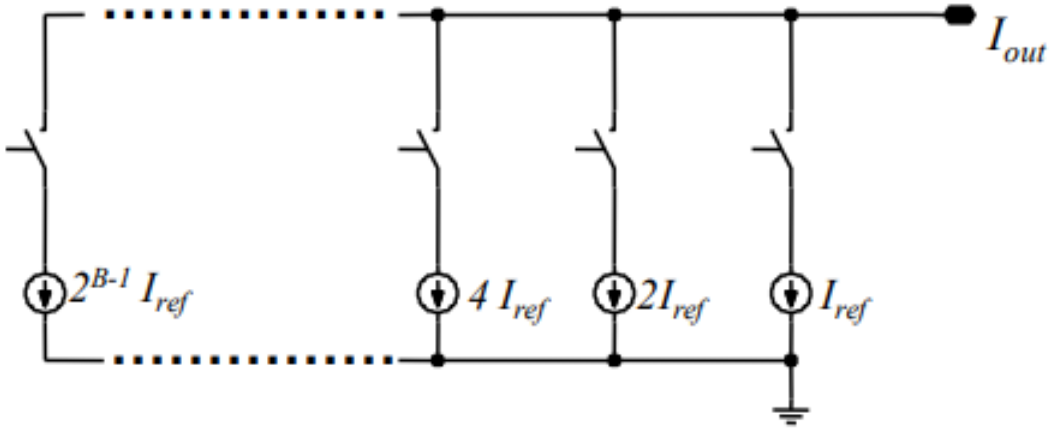



- "Unit elements" or thermometer
- $2^B$-1 current sources & switches
- Suited for both MOS and BJT technologies
- Monotonicity does not depend on element matching and is guaranteed
- Output resistance of current source → gain error
  - Cascode type current sources higher output resistance → less gain error

# Unit Element DAC Principle

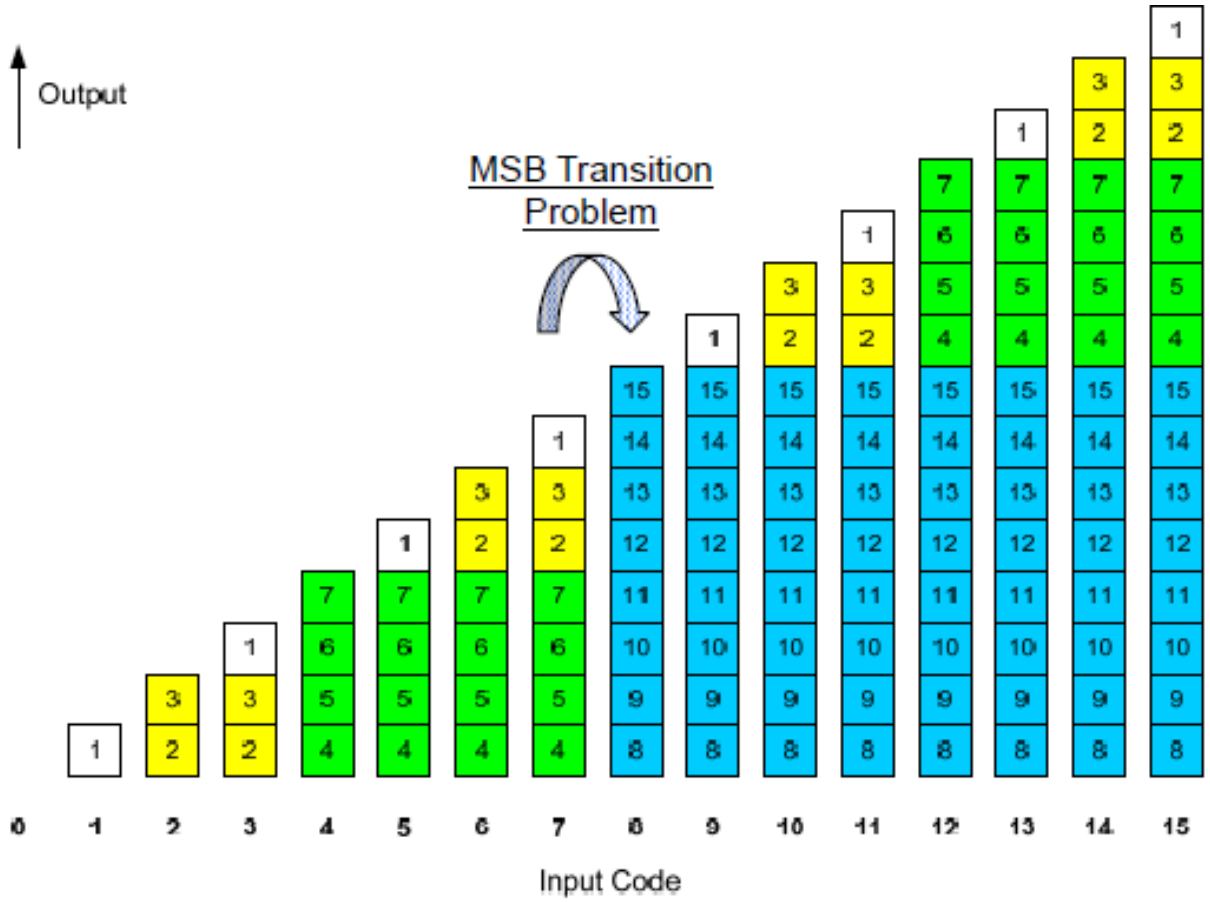


# Binary Weighted Current Source DAC

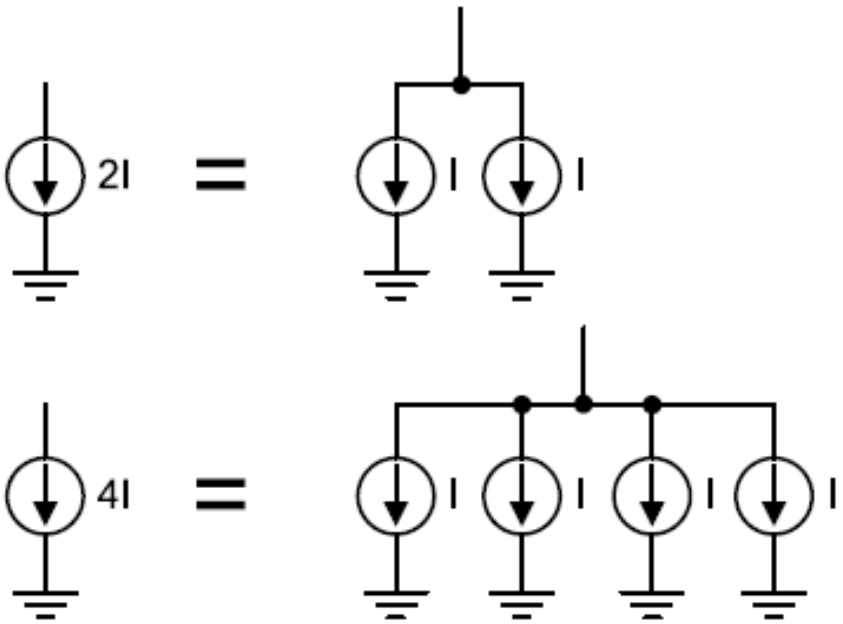



- "Binary weighted"
- B current sources & switches ($2^B$-1 unit current sources but less # of switches)
- Monotonicity depends on element matching →not guaranteed

# Binary Weighted DAC Principle

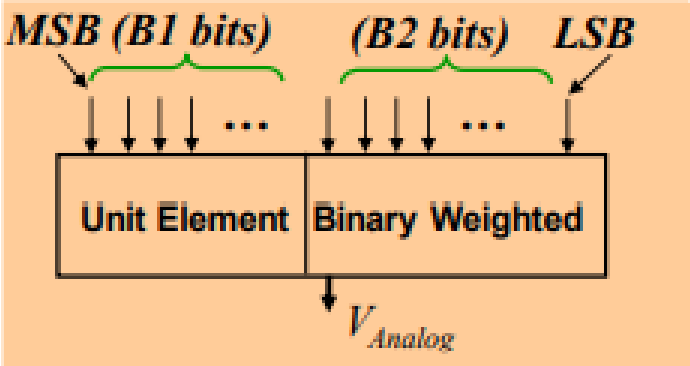


# Implementation of Weighted Elements



# Segmented DAC

- Objective:
  Compromise between unit-element and binary-weighted DAC




- Approach:
  $B_1$ MSB bits → unit elements
  $B_2$ LSB bits → binary weighted

$B_{Total} = B_1 + B_2$

- INL: unaffected same as either architecture
- DNL: Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with ($B_2$+1) # of bits
- Number of switched elements: $(2^{B1}-1) + B_2$