University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

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WeFr 2-3:30pm

We, April 22, 2:00-3:30pm

EECS 141: SPRING 09—MIDTERM 2

NAME	Last First

SID	

Problem 1 (10):

Problem 2 (9):

Problem 3 (11):

Total (30)	

PROBLEM 1: MOS TRANSISTORS (10 Points)

An MOS device can operate in one of the four regions:

a. cut off;
b. linear;
c. saturation;
d. velocity saturation.

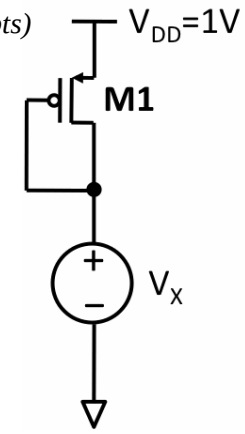
Transistor parameters are:

NMOS: $V_T = 0.3V$, $V_{D,VSAT} = 0.3V$, $k = \mu C_{OX} = 100\mu A/V^2$, $\lambda = 0$, $\gamma = 0$

PMOS: $V_T = -0.3V$, $V_{D,VSAT} = -0.5V$, $k = \mu C_{OX} = -50\mu A/V^2$, $\lambda = 0$, $\gamma = 0$

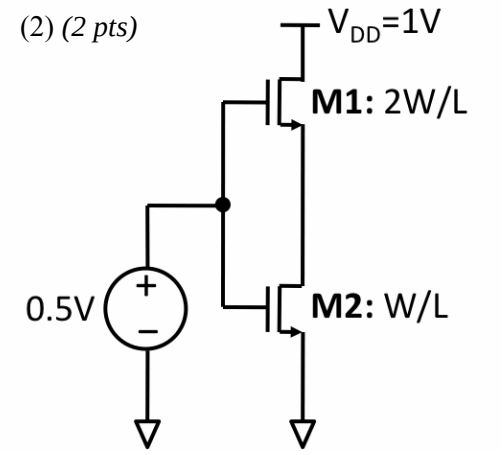
Determine regions of operation of the devices shown below.

(1) *(2 pts)*



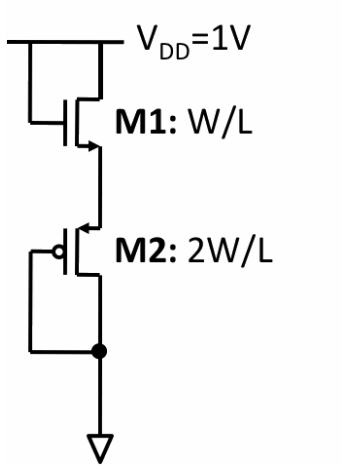
Device	V_X	Region of Operation
M1	**0.5V**	
	0.1V	

(2) *(2 pts)*



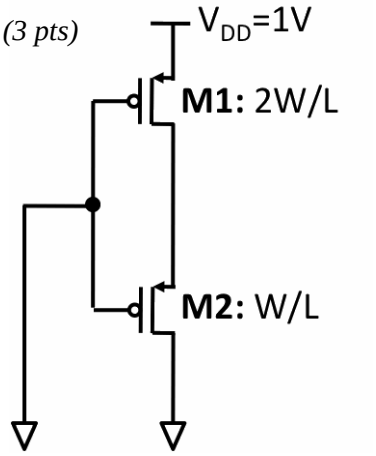
Device	Region of Operation
M1	
M2	

(3) *(3 pts)*



Device	Region of Operation
M1	
M2	

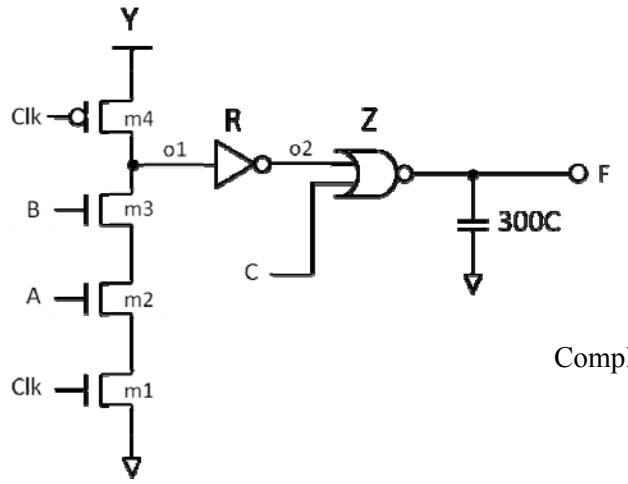
(4) *(3 pts)*



Device	Region of Operation
M1	
M2	

PROBLEM 2 – Dynamic Logic (9 Points)

Given the logic network below that is composed of a dynamic CMOS gate Y, a static CMOS inverter gate R, and a static CMOS NOR gate Z:



Complex logic network.

(1) Size the transistors of the first-stage dynamic CMOS gate Y such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What is logical effort of Y for input A and B? (Freebee!) (1 pt)

m1=m2=m3=

m4=

LE_A= LE_B=

(2) Determine the logic function F of the logic network in terms of input A, B, and C. (Another freebee!) (1 pt)

F=

(3) It is reasonable to first assume that the critical path for the output F high-to-low transition is from the input A to the output F. Size the gate Y, R, and Z to minimize the propagation delay T_{HL} **from the input A to the output F**. Assume the input capacitance of the input A cannot exceed 4C, where C is the input capacitance of a unit size inverter. (3 pts)

Y=

R=

Z=

(4) Now let's turn to the output F low-to-high transition. Identify the critical path of the network for the output low-to-high transition and explain your choice. Calculate the propagation delay T_{LH} by using the same transistor sizes you found in (3). Assume $\gamma = 1$. (2 pts)

The critical path is

$T_{LH} =$ t_{p0}

(5) What are the activity factors of nodes o1, o2, and F if $P(A=0) = P(B=0) = P(C=0) = 0.25$? (2 pts)

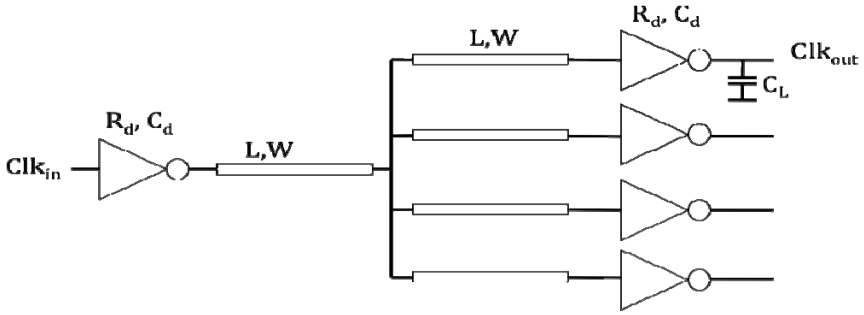
$\alpha_{o1(0->1)} =$

$\alpha_{o2(0->1)} =$

$\alpha_{F(0->1)} =$

PROBLEM 3: Wire Delay (11 points)

Consider the clock distribution network plotted below. Assume the following design parameters: R_d and C_d are the drive resistance and output capacitance of the inverters, and equal 1 kΩ and 4 fF, respectively. You may assume that $\gamma = 1$ (that is input and output capacitance of the inverter are identical). Wires are characterized by their sheet resistance and area capacitance r_w = 0.06 Ω/sq, c_w =0.04 fF/μm^2 . The fringing capacitance can be ignored. Each wire segment has a length L of 5 mm, while its width W is kept as a variable. The load capacitance C_L equals 10 fF.



a. Derive an expression for the delay between nodes Clk_{in} and Clk_{out} as a function of the wire width W. Carefully identify each component of the delay.
HINT: Think Elmore! (6 pts)

t_p =

b. Derive the wire width W that minimizes the delay. (3 pts)

$W =$

c. Check for each of the following statements if it is TRUE or FALSE or DOES NOT MATTER (2 Pts):

- The delay between Clkin and Clkout can be further reduced by partitioning the wires into shorter segments and introducing inverters in between.

  TRUE ☐ FALSE ☐ DOES NOT MATTER ☐

- Introducing inverters along the length of the wire helps to reduce power comsumption.

  TRUE ☐ FALSE ☐ DOES NOT MATTER ☐

- Using Gold instead of Copper for the wires would reduce the delay.

  TRUE ☐ FALSE ☐ DOES NOT MATTER ☐

- Suspending the wire in free space rather than surrounding them with SiO2 would reduce the delay.

  TRUE ☐ FALSE ☐ DOES NOT MATTER ☐