UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey *Homework #1: Circuit Simulation* *EECS 141*
Due Friday, January 29, 5pm, box in 240 Cory

1. Plots of schematics

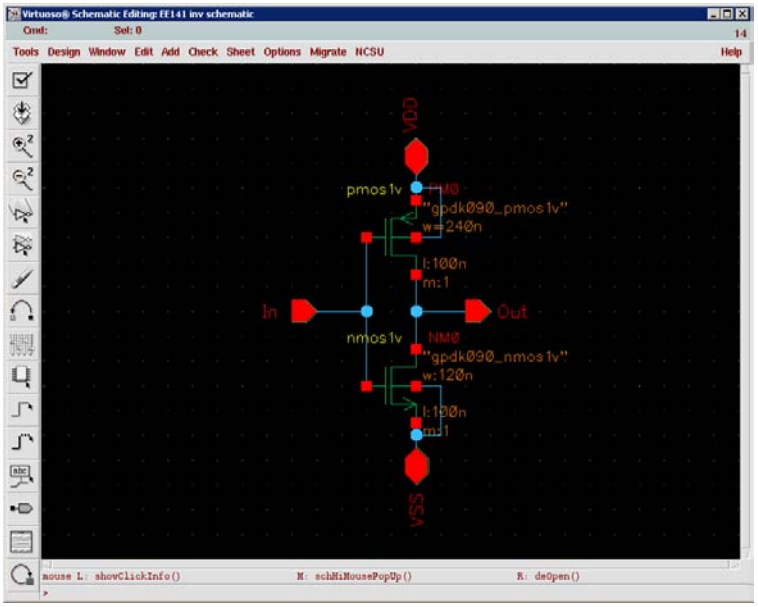

Figure 1: Schematic of the inverter

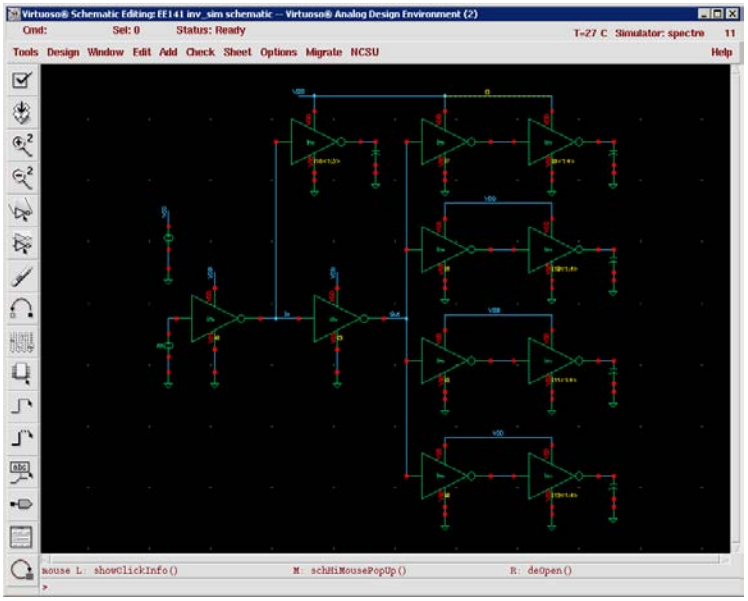

Figure 2: Schematic for the simulation

2. Transient response of the inverter

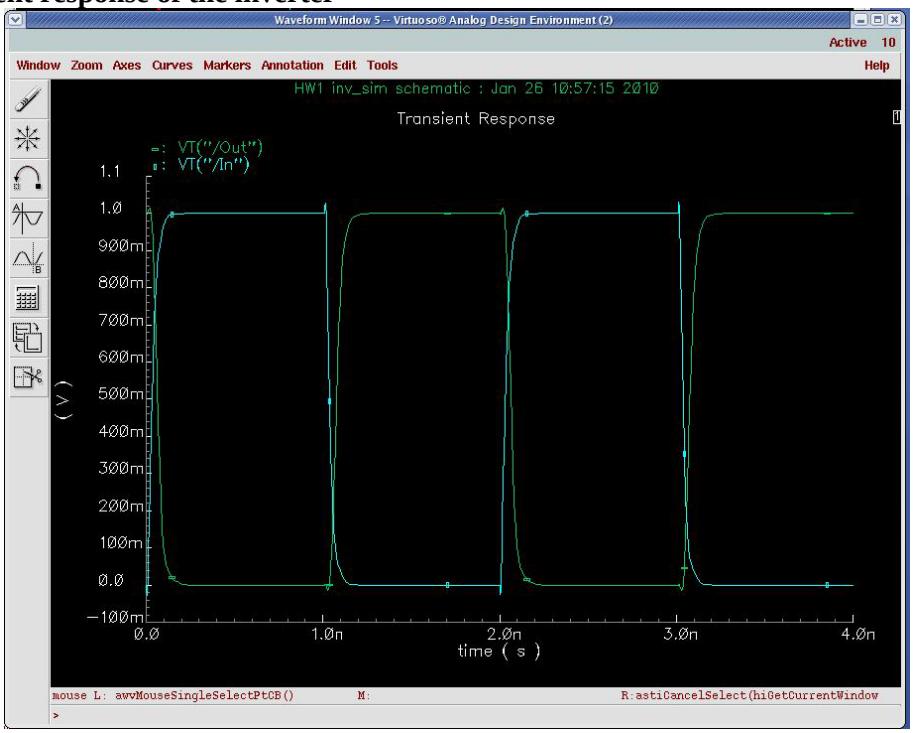

Figure 3: Complete transient response of the inverter

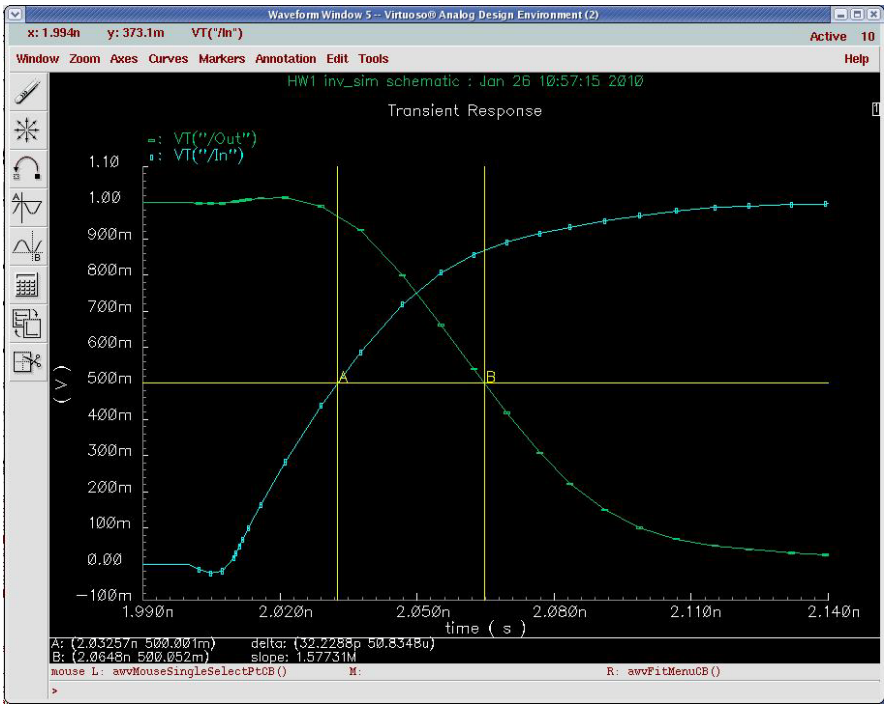

Figure 4: Inverter delay for the rising signal edge at input

Delay for the rising edge at input: 32.23 ps

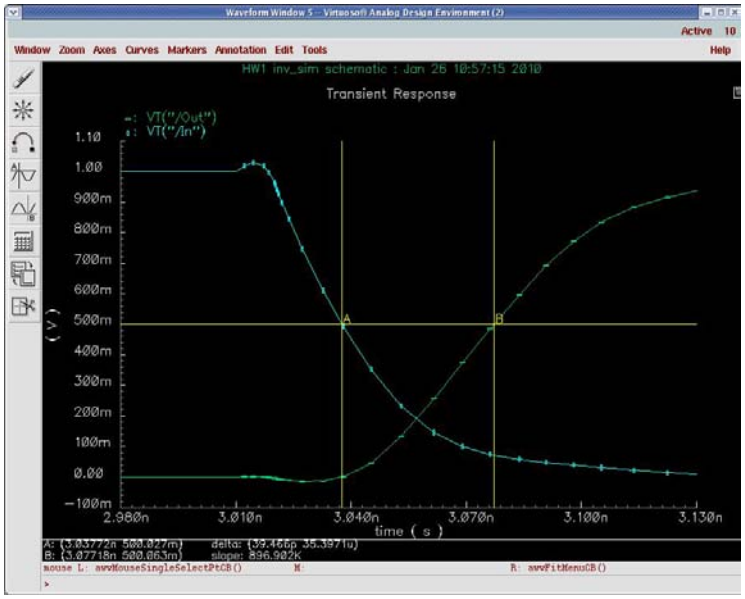

Figure 5: Inverter delay for the falling signal edge at input

Delay for the falling edge at input: 39.47 ps

3. Voltage-Transfer Characteristic

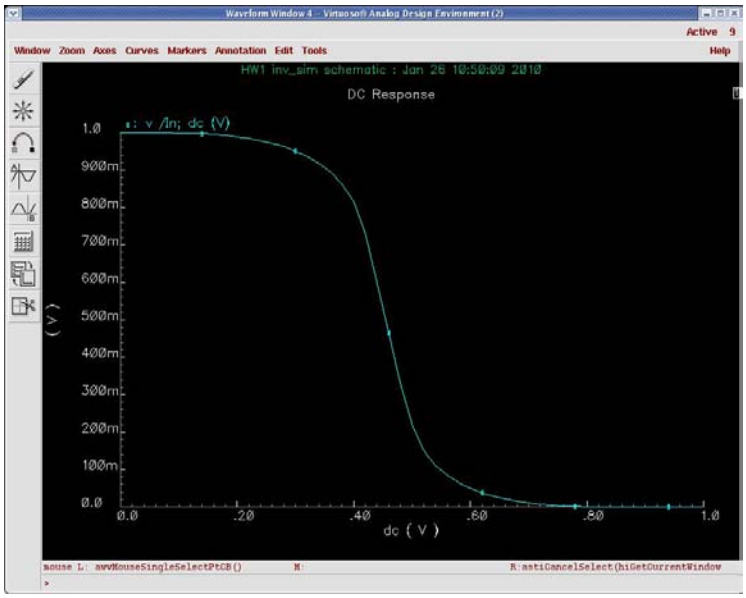

Figure 6: Voltage-transfer characteristic of the inverter