LC-tank CMOS Voltage-Controlled Oscillators using High Quality Inductors Embedded in Advanced Packaging Technologies

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Table of Contents

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LIST OF TABLES

LIST OF FIGURES

SUMMARY

This dissertation focuses on high-performance LC-tank CMOS VCO design at 2 GHz. The high-Q inductors are realized using wiring metal lines in advanced packages. Those inductors are used in the resonator of the VCO to achieve low phase noise, low power consumption, and a wide frequency tuning range.

In this dissertation, a fine-pitch ball-grid array (FBGA) package, a multichip module (MCM)-L package, and a wafer-level package (WLP) are incorporated to realize the high-Q inductor. The Q-factors of inductors embedded in packages are compared to those of inductors monolithically integrated on Si and GaAs substrates. All the inductors are modeled with a physical, simple, equivalent two-port model for the VCO design as well as for phase noise analysis. The losses in an LC-tank are analyzed from the phase noise perspective.

For the implementation of VCOs, the effects of the interconnection between the embedded inductor and the VCO circuit are investigated. The VCO using the on-chip inductors is designed as a reference. The performance of VCOs using the embedded inductor in a FBGA and a WLP is compared with that of a VCO using the on-chip inductor. The VCO design is optimized from the high-Q perspective to enhance performance. Through this optimization, less phase noise, lower power consumption, and a wider frequency tuning range are obtained simultaneously.

CHAPTER I

INTRODUCTION

1.1 INTRODUCTION TO VOLTAGE-CONTROLLED OSCILLATOR

Oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency (RF) circuits. While oscillators can be anything that exhibits periodically time-varying characteristics, this dissertation is concerned with an electrical signal at a specific frequency. When it is used for frequency translation, we often refer to an oscillator as the local oscillator (LO).

When used with a mixer, the LO allows frequency translation and channel selection of RF signals. The front-end of a typical transceiver is shown in Figure 1.1. The mixers and LO are used to down-convert the RF signal to a lower, intermediate frequency (IF), or to up-convert the IF signal to a higher RF frequency. Because the IF frequency is usually fixed, the channel of interest is selected by varying the frequency of the LO.

The LO is often implemented as a phase-locked loop (PLL) in which a voltage-controlled oscillator (VCO) is phase-locked to a high-stability crystal oscillator. A typical PLL is made up of a VCO, low-pass loop filter, phase detector, and frequency divider, as shown in Figure 1.2. Because the PLL is involved in frequency translation and channel selection, its spectral purity affects the performance of an overall wireless system. Within the loop bandwidth of the PLL, the output has all the noise characteristics of the reference signal, the phase detector, the loop filter, the divider, and the VCO. Outside the loop

bandwidth, the output retains the noise characteristics of the VCO. Therefore, the spectral purity of the PLL output depends heavily on that of the VCO. Its spectral purity is generally characterized by its amount of phase noise.

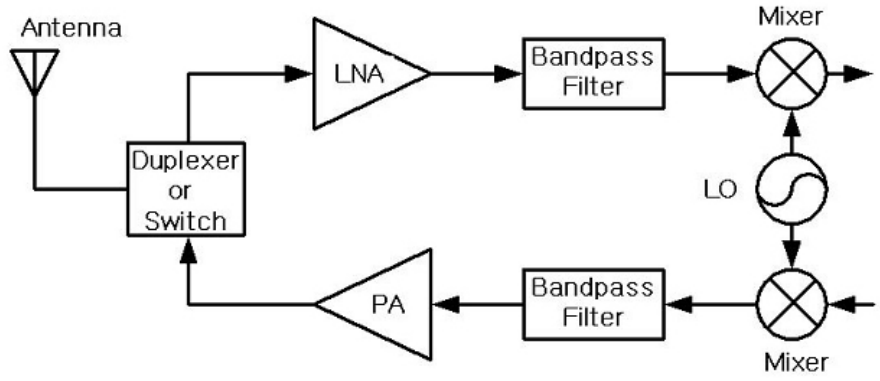


Figure 1.1 Simplified block diagram of a typical RF front-end transceiver chain.

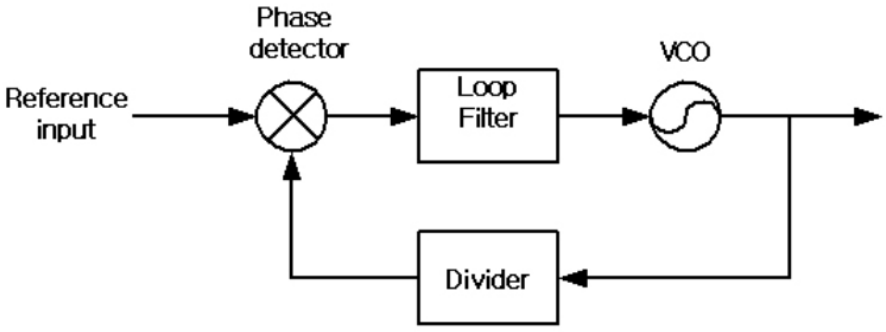


Figure 1.2 Simplified block diagram of a typical phase-locked loop.

With an increasing number of wireless users and ensuing demand for more efficient usage of frequency resources, the frequency spectrum has become the most important resource in wireless communications. Because wireless transceivers rely heavily on frequency conversion by the LOs, the spectral purity of both the receiver and transmitter of the LO affects the maximum number of available channels and users. In the receiver, the phase noise of the LO limits its ability to detect a weak signal when there is a strong signal in an adjacent channel. Therefore, this phase noise affects not only selectivity, but also the sensitivity and dynamic range of the wireless receiver system. In the transmitter, phase noise results in energy being transmitted outside of the desired band. For these reasons, high spectral purity (low phase noise) is required for the LO in a wireless transceiver [1].

Several specifications to evaluate the performance of a VCO are available, such as oscillation frequency, frequency tuning range, phase noise, and power consumption. Phase noise is the most critical among these specifications. Because of the need for low phase noise characteristic in current wireless systems, a resonator is commonly used for a VCO design. The resonator determines oscillation frequency. When composed of an inductor and a capacitor, the resonator is often referred to as an LC-tank. For frequency tuning, a voltage-controlled capacitor such as a varactor allows variation of the oscillation frequency.

Traditionally, a VCO has been implemented as a stand-alone module separate from other PLL circuit blocks and combined on the PCB board in a hybrid manner. Moreover, it is usually encapsulated using tinned iron to isolate the VCO from external noise. A VCO needs to be a separate module for several reasons. RF front-end circuits such as

power amplifiers (PAs), low-noise amplifiers (LNAs), mixers, and switches have been designed predominantly in III-V compound semiconductor technologies. However, unlike other RF circuits, a Si BJT has been accepted generally as the best candidate for an oscillator because of its low flicker noise and high gain characteristics. Moreover, only an LC-tank consisting of off-chip high-Q passive components enables an oscillator to meet the stringent phase noise specifications for wireless handset applications. Using Si BJTs and off-chip passive components forces it to be a separate module.

Even though wireless mobile technology has grown tremendously during the last 15 years, customers continue to demand ever smaller and less expensive electronic wireless products. The most attractive approach to meet these growing demands is a Si-based single-chip radio [2-3]. The technological advances in the field of Si-based integrated circuits (ICs) allow a high level of integration at low cost. With the minimum feature size of CMOS approaching nano-scale and the emergence of SiGe wide bandgap technology on Si substrate, a Si-based RF front-end module has been considered as a possible solution because of excellent active device frequency characteristics [4-5]. Even though a Si-based single-chip radio already had been proposed, it suffered from several drawbacks that needed to be overcome. One of the most critical drawbacks of Si technology is the poor quality (Q) of the passive components; this shortcoming results from the thin metallization process and lossy Si substrate. Poor-quality passive components, especially low-Q inductors prevent the Si-based single-chip radio from being the best solution.

High-Q inductors are essential in RF circuits to preserve the energy of the RF signals. In a PA, LC networks are used for the input, output, and inter-stage matching. When the matching networks are lossy, energy is lost, and output power, gain, and efficiency

deteriorate. For an LNA, a source inductive degeneration is commonly used to obtain 50Ω input matching. It is evident that the lossy inductor at the gate directly increases the noise figure. The inductor at the source terminal also requires high quality to ensure low noise characteristics [6]. The phase noise of an LC-tank VCO mainly depends on the Q-factor of the inductor in the resonator [7]. In addition to phase noise, a high-Q inductor entails low power consumption and wide frequency tuning characteristics.

1.2 MOTIVATION FOR DISSERTATION

The Si-based single-chip radio implementation for a wireless system results in a new environment for the LC-tank VCO, which has not been integrated into a transceiver before because of the poor quality of on-chip passive components. Great effort has gone into different approaches to overcoming this problem. Si-based IC technology has been improved to achieve high-Q passive components. A metal-insulator-metal (MIM) configuration has been used to realize a high-Q capacitor. As for the inductor, a thick metallization process has been incorporated for the top metal layer to reduce the series resistance of an inductor layer. To minimize the parasitic effects of the substrate, the distance has been increased between the top metal layer and the Si substrate. Even a Si substrate with high resistivity was incorporated. And recently favorable attention has focused on growing SiO_2 in the. However, all of the above-mentioned approaches to producing a high-Q inductor increase cost, which is opposite to the reason that the single-chip solution was proposed in the first place.

Si-based micro-electro-mechanical system (MEMS) technologies have also been used to implement the high-Q inductor. Copper plating provides high conductivity and thick

metallization. Surface micro-machining technologies enable the inductor layer to hang over air. The Si substrate effects can be reduced by bulk micro-machining technologies. But even if the MEMS inductor shows a very high-Q characteristic, cost and reliability are obstacles to its commercial adoption.

One proposed solution that can meet low-cost and high-performance requirements simultaneously is the use of metal layers in a package. An inductor embedded in such a package shows a high-Q characteristic because the metal layer is made of highly conductive thick copper and the inductor layer can be located far from the conductive substrate. Ultimately, such an IC should be packaged as a commercial product. Because such a package solves the technical and quality problems others have encountered and is suitable for commercialization, this approach is the most cost-effective solution proposed so far and can accelerate the advent of a Si-based single-chip radio implementation. Although this approach includes a single chip, it is slightly different because it incorporates a package solution. This solution combines a Si-based single-chip approach with a high-Q inductor packaging technology. Therefore, it can be called a Si-based single-chip package solution that simultaneously provides lower cost, smaller size, and higher performance.

In this dissertation, the 0.35 μm CMOS IC technology, along with the advanced packaging technologies, is used to demonstrate a Si-based single-chip package solution. The high-Q inductors embedded in advanced packages such as a fine-pitch ball-grid array (FBGA), a multichip module (MCM), and a wafer-level package (WLP) are presented. The quality of each embedded inductor is compared with that of the on-chip inductors on both Si and GaAs substrates. These high-Q inductors are used in the LC-tank for the

VCO. The VCO is co-designed with the high-Q inductor embedded in a package to achieve not only low cost and small size but also high- performance including low phase noise, low power consumption, and a wide frequency tuning range. The performance of the VCOs using embedded inductors is compared with that of the VCO using an on-chip inductor.

1.3 ORGANIZATION OF DISSERTATION

Chapter two gives an overview of LC-tank VCOs. The basic theory of the oscillator operation is described, and the LC-tank VCO topologies are presented. Starting from one-transistor topology, the differential topologies with CMOS cross-coupled pairs are discussed. The specifications of a VCO such as frequency tuning, phase noise, and power consumption are described in detail. Chapter three presents on-chip inductor characteristics. The general loss mechanisms in an inductor are explained, and then, the simple, physical-based, equivalent inductor model with frequency-dependent series resistance is presented. The quality of spiral inductors implemented on both Si and GaAs substrates are compared with the quality of inductors embedded in packages. Chapter four shows the implementation of high-Q inductors embedded in advanced packages such as FBGA, MCM, and WLP. Each package technology is described in detail, giving insight into high-Q inductor design. The embedded inductors are designed, measured, and characterized by the inductor model developed in Chapter three. Chapter five presents VCO co-design and implementation using the embedded inductors. The effect of the interconnection between the embedded inductor and the VCO circuitry on the inductor-Q is discussed. The performance of a VCO influenced by the high-Q inductor is described

analytically. Experimental results of the LC-tank CMOS VCOs with the different inductor topologies are presented. All the VCOs are compared in terms of performance. The optimized VCO design to enhance performance is presented from the high-Q inductor perspective. Finally, Chapter six concludes the dissertation with a discussion of possible future work.

CHAPTER II

LC-TANK VOLTAGE-CONTROLLED OSCILLATOR DESIGN

2.1 OVERVIEW OF OSCILLATOR OPERATION

In this chapter, we focus on the analysis of oscillators whose oscillation frequency is determined by the resonant frequency of a parallel LC-tank. An electrical oscillator generates a periodically time-varying signal when supplied with only DC power. An oscillator usually can be considered either as a two-port, feedback system or as two connected one-port circuits. Which viewpoint is used often depends on personal preference or which is most convenient for circuit analysis.

To generate a periodic output, the oscillator circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. Most RF oscillators can be viewed as a feedback system, as shown in Figure 2.1. A frequency-selective network is included in the loop so as to stabilize the frequency. It is called a resonator, which is usually realized with a parallel LC-tank.

Considering the simple, linear feedback system shown in Figure 2.1, the overall transfer function from input to output is expressed as

$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s) \cdot F(s)}. \tag{2.1}$$

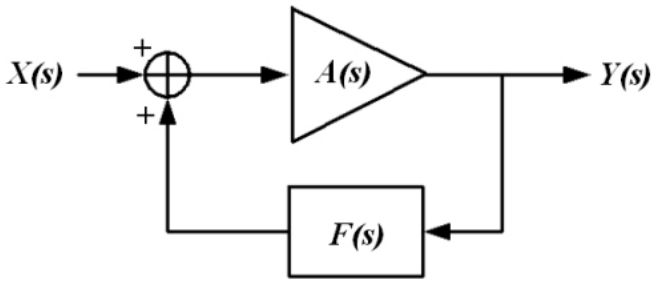


Figure 2.1 Positive feedback system with frequency-selective network *F(s)*.

This system provides a periodic output at frequency s_o without any input as long as

$$A(s_0) \cdot F(s_0) = 1 \tag{2.2}$$

which is known as the Barkhausen criterion. *A(s)·F(s)* is often called the loop gain.

For (2.2) to be satisfied, the magnitude of the loop gain must be equal to one and the phase shift in the loop must be equal to zero. Typically, the magnitude of an initial loop gain is designed to be greater than one to guarantee oscillation. Then, as the magnitude of the periodic signal increases, the magnitude of the loop gain is reduced to one by non-linearity in the amplifier in its steady-state operation.

Another way to view an oscillator is given in Figure 2.2. The oscillator is divided into two one-port networks. One is an active circuit network and the other is a resonator network. To achieve steady-state oscillation, the equivalent parallel resistance R_P of the resonator must be balanced with the negative resistance $-R_A$ produced by the active circuit. When this condition is satisfied, the circuit becomes lossless, and generate oscillation. Essentially, any energy dissipated in R_P is compensated for with the energy produced by the active circuits.

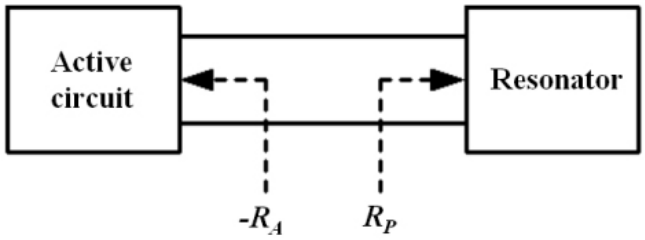


Figure 2.2 One-port view of an oscillator.

2.2 LC-TANK DIFFERENTIAL VCO TOPOLOGIES

Most discrete RF oscillators have only one transistor. This is for two reasons. One is to minimize noise; the other is to lower the cost. In IC technologies, while the first reason is still valid, the second reason has become of little concern, but the first still influences design. In this section, oscillator topology using only one transistor is discussed. Then, starting from the one-transistor oscillator, the cross-coupled differential topology, so-called the negative-g_m oscillator, are introduced. A Si substrate is so conductive that noise from other circuitry is flowing through the substrate. Therefore, for the Si-based single-chip approach to work, a VCO should be realized by means of a differential topology provides common-mode noise rejection. All versions of the cross-coupled differential topology are shown in the following sections.

2.2.1 One-transistor Oscillator Topology

In Figure 2.3, LC oscillators including one active MOS transistor and an LC-tank at the collector of a transistor are shown. The configuration of Figure 2.3 (a) has direct

feedback applied from the drain to the source. The direct feedback path from the tank to the source entails the resistive loading effect seen at the source terminal, $1/g_m$. This loading effect reduces the loaded Q of the tank and the loop gain and results in disturbing the oscillation condition mentioned in section 2.1. Therefore, the source impedance must be transformed to a higher value, as shown in Figure 2.3 (b) [8].

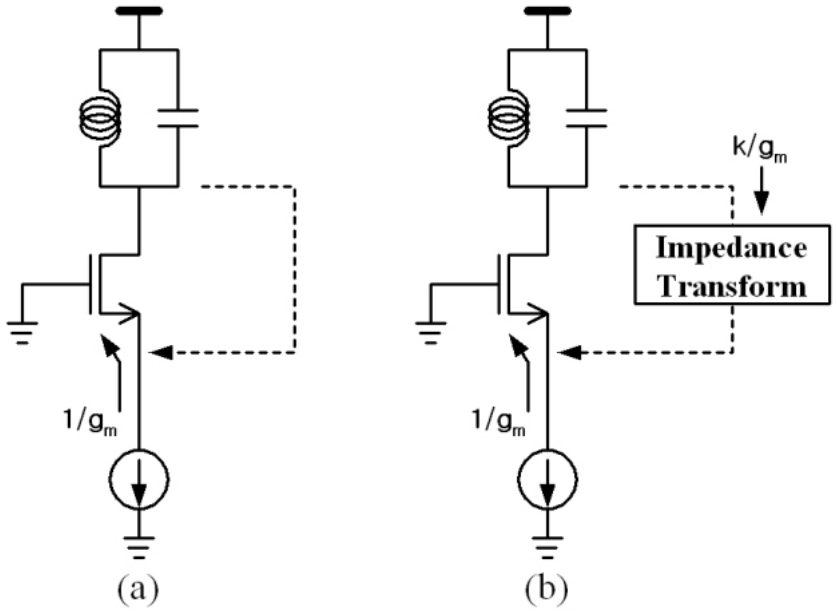


Figure 2.3 (a) Direct feedback from drain to source, (b) feedback with an impedance transformer.

The required impedance transformation can be achieved by using either capacitive or inductive dividers, as illustrated in Figure 2.4. A circuit that uses a capacitive divider is called a Colpitts oscillator, and one that uses an inductive divider is called a Hartley oscillator. The equivalent parallel resistance in the tank is approximately expressed as

$(1+C_1/C_2)^2/g_m$ in Figure 2.4 (a) and $(1+L_2/L_1)^2/g_m$ in Figure 2.4 (b), which enhances the loaded resonator Q. The Colpitts oscillator includes one inductor, so that it is more frequently used than the Hartley oscillator [8].

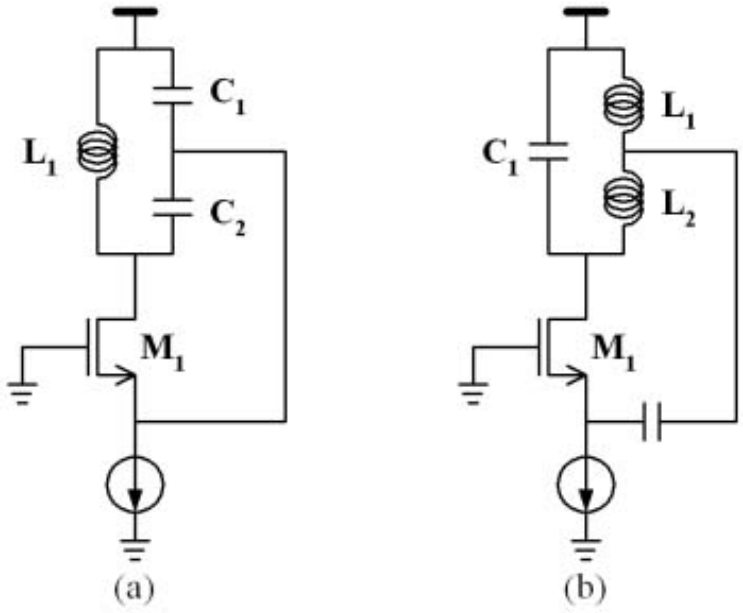


Figure 2.4 (a) Colpitts and (b) Hartley oscillators.

The resonance frequency is $\omega_r = 1/\sqrt{L_{eq} \cdot C_{eq}}$, in which L_{eq} and C_{eq} are the equivalent inductance and capacitance in the parallel tanks of Figure 2.4. There are some trade-offs regarding inductance value. To achieve the desired large voltage swing that produces low phase noise, it is necessary to increase inductance because the equivalent parallel resistance of the tank is expressed by $\left(L_{eq} \cdot \omega_r\right)^2 / R_s$. However, this is only valid when the increasing degree of inductance is dominant compared with that of increasing series

resistance. Moreover, the tank capacitance becomes limited by inductor parasitics, which in turn makes it difficult to vary the oscillation frequency by adding a variable capacitor to the oscillator.

Because the transistor M_1 is the main noise source in the oscillators of Figure 2.4, it should be optimized in terms of size and the biasing. The gate and drain thermal noise can be minimized by increasing device size and decreasing the bias current of the transistor [8]. However, the former causes parasitic capacitance, and the latter lowers the voltage swing. Hence, a compromise is usually necessary.

These topologies have several drawbacks. One is that the ratio of the capacitors and inductors needs to be large so that their effect on the loaded Q of the tank is negligible. A second is that these topologies provide a single-ended output but wireless transceiver systems usually operate with differential signals because of a double-balanced mixer configuration. And a third is that the common-mode noise from the supply and the substrate directly affect phase noise when the oscillator is integrated in a Si-based single chip. Therefore, the oscillator needs to use a differential topology to allow a Si-based single-chip approach.

2.2.2 Evolution of Cross-Coupled Differential Topology

The signal fed back from the drain of a transistor to its source must pass through an impedance transformer to avoid degradation of a loaded Q of the tank. A passive divider network transforms the impedance to a higher value in both the Colpitts and Hartley oscillators.

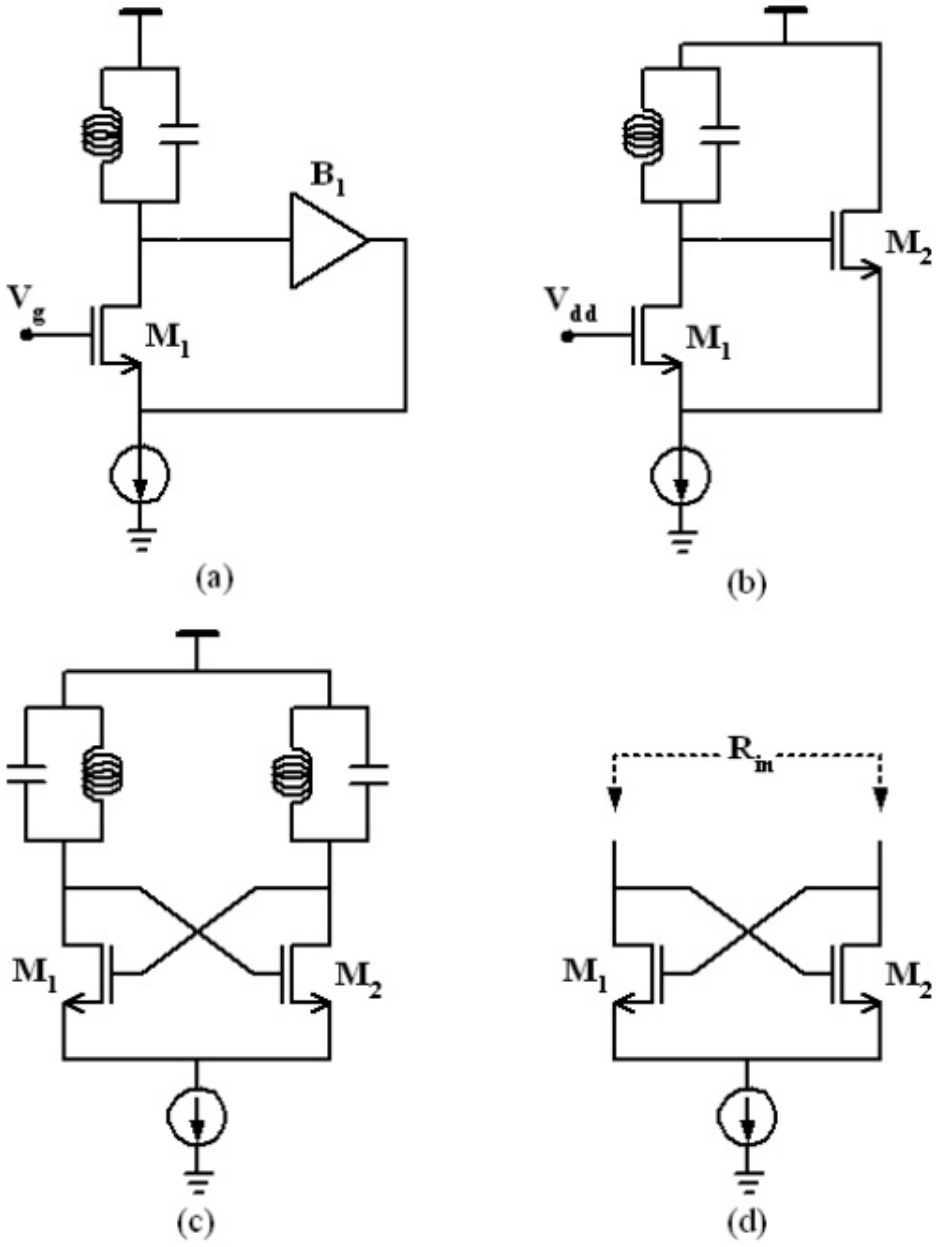


Figure 2.5 A one-transistor oscillator using a feedback from drain to source (a) with an active buffer in feedback loop, (b) with a source follower as a buffer. (c) Cross-coupled differential topology. (d) Negative resistance of a cross-coupled pair.

In both types of oscillators, the passive network can be replaced by an active buffer (B_1) between the drain and the source, as shown in Figure 2.5 (a). The buffer presents high impedance to the tank. In Figure 2.5 (b), a source follower is used for the buffer. The gate of M_1 can be biased to V_{dd}, the same dc voltage as the gate of M_2. The oscillator can employ one more LC-resonators to operate differentially, as shown in Figure 2.5 (c). This configuration is called a cross-coupled differential oscillator or a negative-g_m oscillator [8].

The cross-coupled feedback oscillator of Figure 2.5 (c) can be considered as a one-port implementation. Negative resistance is seen at the drain of M_1 and M_2, as shown in Fig 2.5 (d). Negative resistance is expressed by [9]

$$R_{in} = -\frac{2}{g_m}. \tag{2.3}$$

Thus, if R_{in} is less than or equal to the equivalent parallel resistance of the tank, the circuit oscillates.

2.2.3 NMOS or PMOS Core Cross-Coupled Differential Topology

According to the MOS device type for the cross-coupled pair and the location of a tail current source, there are four versions of a cross-coupled differential configuration. The differential oscillators with a cross-coupled NMOS pair and a tail current are shown in Figure 2.6 (a), and (b). The differential oscillators with a cross-coupled PMOS pair with a tail current are shown in Figure 2.6 (c) and (d). Each cross-coupled pair can have a tail current either at the source or at the drain terminal.

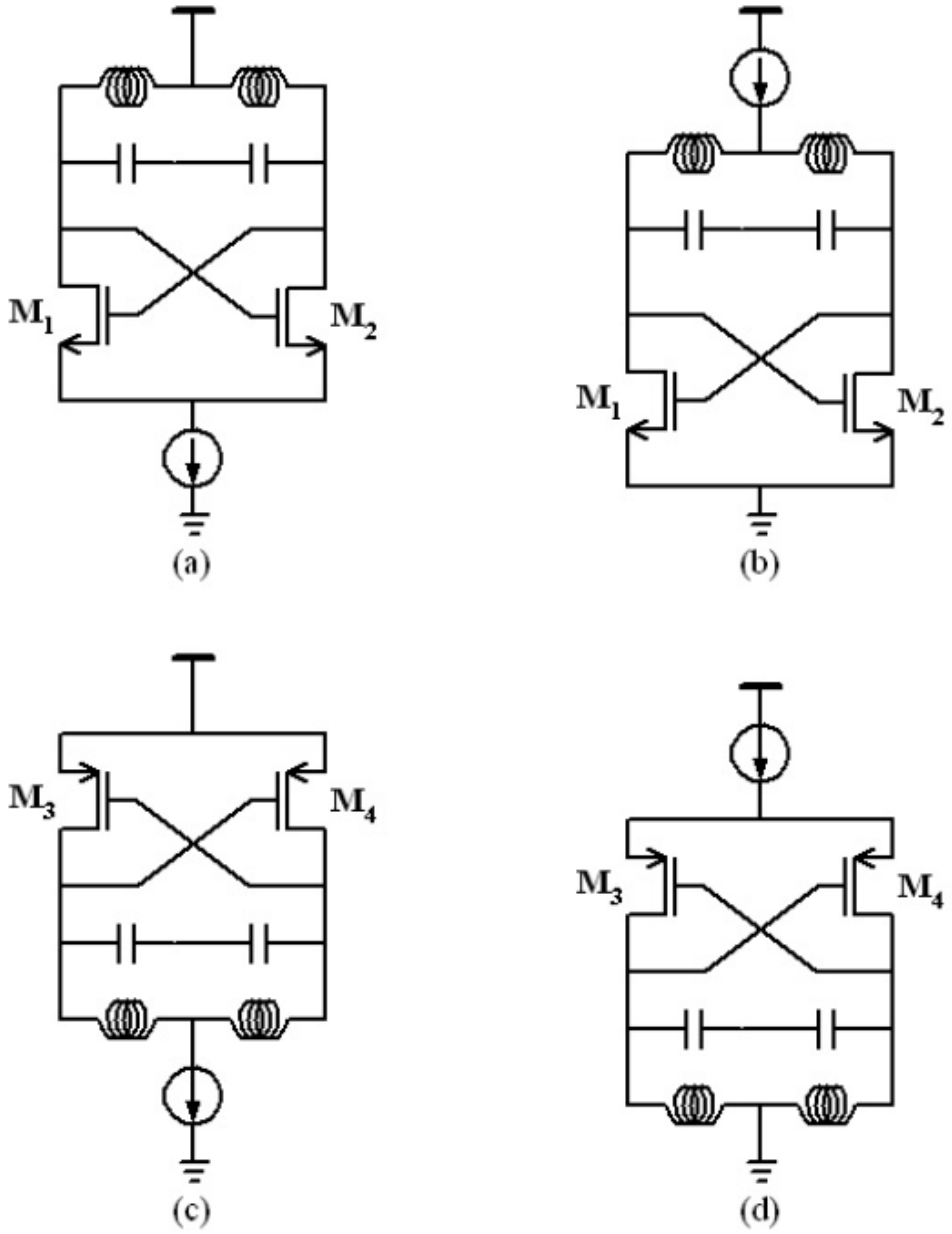


Figure 2.6 Cross-coupled differential topology (a) with an NMOS pair and a tail current at the source, (b) with an NMOS pair and tail current at the drain, (c) with a PMOS pair and a tail current at the drain, (d) with a PMOS pair and a tail current at the source.

A PMOS cross-coupled pair has been adopted in a VCO design claiming low noise characteristics of a PMOS device itself [10]. The hot carrier effect is known to be small in a PMOS [11]. This is critical in a CMOS process in which hot electron noise is significant. Flicker noise of a PMOS is ~10 times smaller than that of a NMOS for the same transistor dimension. Considering that a PMOS transistor has a lower mobility, the flicker noise of a PMOS should be lower at a given current and g_m because of a large gate area. For these reasons, it has been reported that a VCO using a cross-coupled PMOS pair shows low phase noise characteristics [12].

2.2.4 CMOS Core Cross-Coupled Differential Topology

Instead of only a NMOS or PMOS pair, a CMOS pair can be used to achieve more positive gain, as shown in Figure 2.7 (a). Both NMOS and PMOS pairs generate negative resistance to the LC-tank, R_{inn} and R_{inp}, respectively. Therefore, the total negative resistance provided by a CMOS pair is given by

$$R_{negative\ total} = R_{inn} // R_{inp} = -\frac{2}{g_{m12} + g_{m34}}. \tag{2.4}$$

It is known that the flicker noise of an active device is up-converted, and then, generates the phase noise region with a slope of –30dB/decade, the so-called $1/f^3$ phase noise region. This region can be suppressed when the rising and falling time of the oscillation waveform is equal [13]. Therefore, waveform symmetry needs to be carefully considered in a VCO design, especially in using a device with high flicker noise like a MOS. Symmetry of the rising- and falling-time of the oscillation waveform is possible when the device sizes of NMOS and PMOS pairs are designed to be $g_{m12} = g_{m34}$.

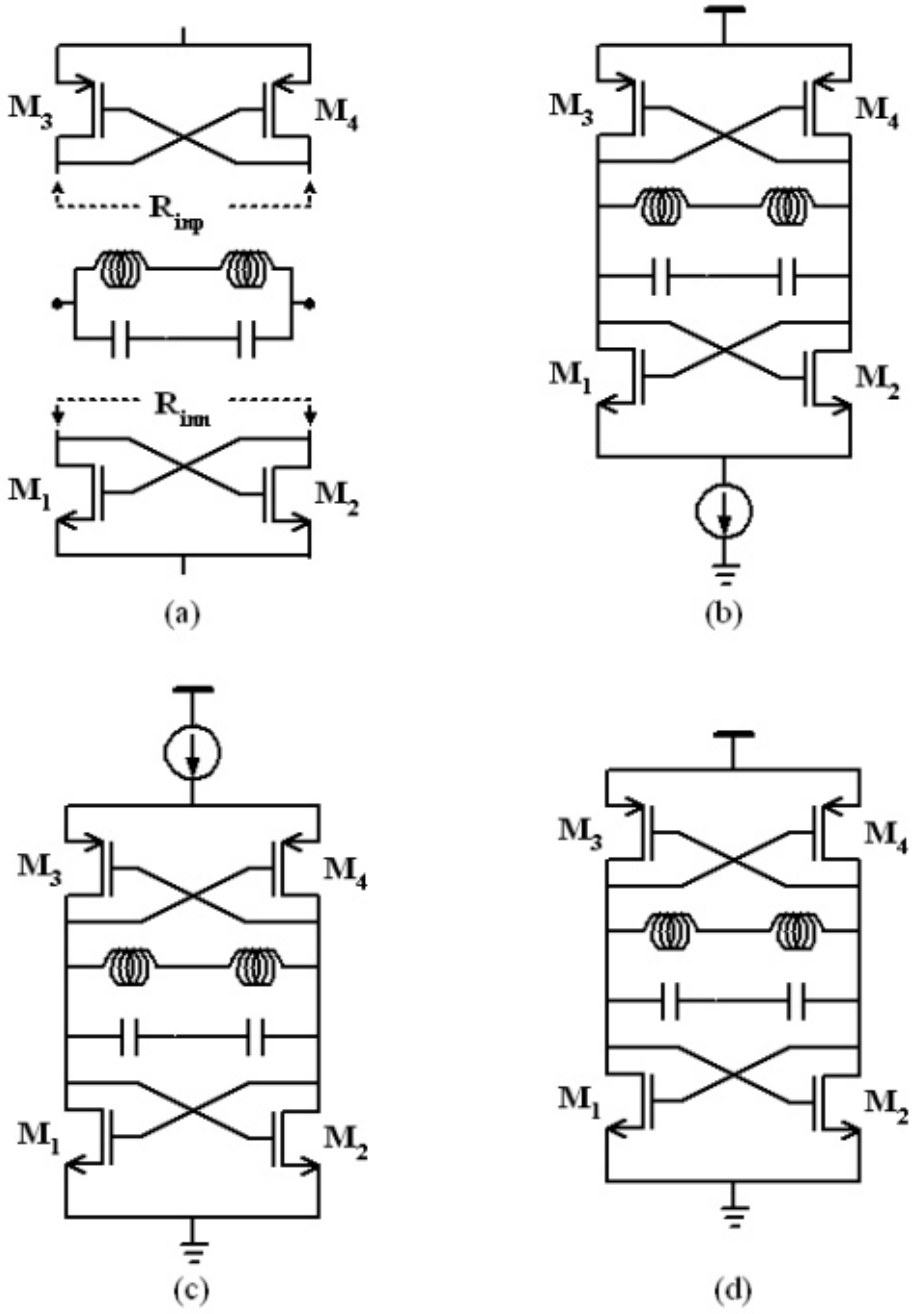


Figure 2.7 (a) Total negative resistance of CMOS cross-coupled pair. CMOS Cross-coupled differential topology (a) with a tail current at the source of NMOS pair, (c) with a tail current at the source of PMOS pair, (d) without a tail current.

However, there are several drawbacks to a CMOS cross-coupled differential topology. One is that when the tail current source is used together with a CMOS cross-coupled pair, it is hard to go below 3V with the supply voltage because at least 1V is necessary for each pair and a current source to ensure proper operation. Obviously, the use of two or more active devices in addition to the NMOS or PMOS pair increases the noise sources and the parasitics so much that phase noise performance and frequency tuning characteristics are affected.

As shown in Figure 2.7, the tail current source can be located at the source of either an NMOS or a PMOS pair. Tail current is one of the noise sources in a VCO circuit. A slow, random fluctuation of the tail current induces a frequency change directly related to phase noise [14]. Because of the mixing mechanism of a VCO circuit, flicker noise from the tail current source is up-converted to the LC-tank and results in phase noise. Tail current is generally considered the most significant source of flicker noise in a cross-coupled differential oscillator. The contribution of a NMOS or PMOS pair is small because of the switching operation of the oscillator. Flicker noise is correlated noise and can exist only in systems with memory. This noise is usually higher than the contribution of the single tail transistor alone, because the bias network also contributes to the fluctuation of the tail current. Therefore, it has been reported that CMOS cross-coupled differential topology without the tail current source, as depicted in Figure 2.7 (d), shows low phase noise characteristics [15]. In addition, the supply voltage can be reduced for low power consumption.

2.3 SPECIFICATIONS OF VCO

There are several specifications representing VCO performance; oscillation frequency, frequency tuning range, phase noise at a specific offset frequency, and power consumption. As mentioned in Chapter one, phase noise is the most critical among the specifications for a VCO. In addition, because of battery limitation on mobile devices, low power consumption is required as well. However, a trade-off exists between power consumption and phase noise. The semi-empirical phase noise model, known as the Leeson model, is given by [7]

$$L(\Delta\omega) \propto \frac{N}{P_S \cdot Q_L} \cdot (\frac{\omega_o}{\Delta\omega})^2 . \tag{2.5}$$

where N is the noise factor, P_S is the signal power at the resonator, Q_L is the effective quality factor of the resonator with all the loadings in place, ω_o is the oscillation frequency, and $\Delta\omega$ is an offset frequency from the carrier. From (2.5), it is easily noted that the more signal power, the better the phase noise performance.

Oscillation frequency and frequency tuning depend on the application. Both specifications should cover the application bandwidth. The frequency tuning range tends to be wider to cover multibands. The frequency tuning range also is related to phase noise. Usually frequency tuning is achieved by a varactor. To gain a wide tuning range requires a large varactor, which means additional noise in the circuit and additional substrate parasitics. This illustrates that all the specifications are closely related to each other.

To evaluate a designed VCO compared with other VCOs in terms of performance, one of the general Figure-Of-Merit (FOM) formulas is expressed as [16]

$$FOM = L(\Delta\omega) - 20 \cdot \log[(\frac{\omega_0}{\Delta\omega})] + 10 \cdot \log(\frac{P_{diss}}{1mW}) . \tag{2.6}$$

Equation (2.6) includes phase noise, $L(\Delta\omega)$ at an offset frequency of $\Delta\omega$, oscillation frequency, ω_0, and power consumption of the core circuit, P_{diss}. However, this equation does not include the frequency tuning range (FTR) characteristics. Therefore, to make a fair comparison among VCOs, the FOM formula, including the FTR (%) per a control voltage range (*Vcon*) has been proposed as [17]

$$FOM_T = L(\Delta\omega) - 20 \cdot \log(\frac{\omega_0}{\Delta\omega}) + 10 \cdot \log(\frac{P_{diss}}{1mW}) - 10\log(\frac{FTR}{Vcon}) \quad (2.7)$$

2.3.1 Phase Noise

2.3.1.1 Definition of Phase Noise

Phase noise is generally characterized in the frequency domain. The output of an ideal oscillator may be expressed as $Vout(t)=V_0\ cos[\omega_0 t+\phi_0]$, where the amplitude, V_0, the frequency, ω_0, and phase reference, ϕ_0, are all constants. The spectrum of an ideal oscillator consists of an impulse at ω_0, as shown in Figure 2.8 (a). However, in a practical oscillator the output is more generally given by [18]

$$V_{out} = V_0(t) \cdot f[\omega_0 t + \phi_0(t)] \quad (2.8)$$

where $V_0(t)$ and $\phi_0(t)$ are functions of time and f is a periodic function that represents the steady-state output waveform of the oscillator. The output spectrum has power around ω_0 if the waveform, f, is not sinusoidal, as shown in Figure 2.8 (b).

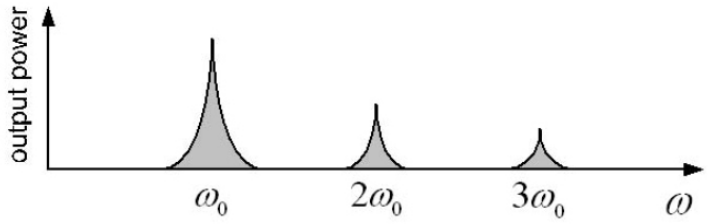
As a consequence of the random fluctuations represented by $V_0(t)$ and $\phi_0(t)$, the spectrum will have sidebands close to the oscillation frequency, which is called phase noise, as shown in Figure 2.9. To quantify phase noise, we consider a unit bandwidth (1Hz) at an offset $\Delta\omega$ from the carrier, calculate the noise power in the band, and divide

this result by the carrier power. This is the single-sided spectral noise density in units of dBc/Hz as

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{noise\ \ power\ in\ a\ 1Hz\ bandwidth\ \ at\ \ frequency\ \ \omega_0 + \Delta\omega}{carrier\ \ power} \right] \quad (2.9)$$

Spectral density is usually specified at one or a few offset frequencies. To be a meaningful parameter, both the noise density and the offset frequency need to be mentioned.

(a)



(b)

Figure 2.8 Spectrum of (a) an ideal oscillator and (b) a real oscillator.

If one plots $L(\Delta\omega)$ for a free-running oscillator as a function of $\Delta\omega$ on a logarithmic scale, regions with different slopes may be observed, as shown in Figure 2.10. At large

offset frequencies, there is a flat noise floor. At small offset frequencies one may recognize regions with a slope of –30 dB/dec and –20 dB/dec [18].

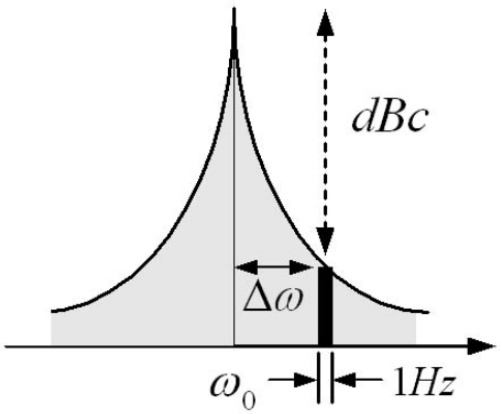


Figure 2.9 Phase noise in an oscillator output spectrum.

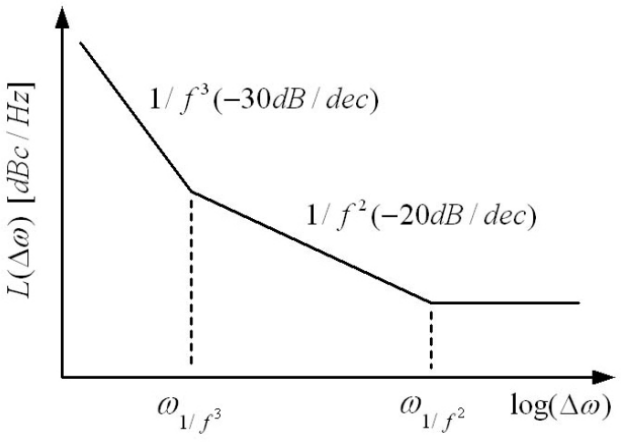


Figure 2.10 Typical phase plot for a free running oscillator.

2.3.1.2 Effect of Phase Noise in Wireless System

To understand the importance of phase noise in a wireless system, consider a typical transceiver shown in Figure 2.11, in which the LO provides the carrier signal for both the receiver and the transmitter. If the LO has high phase noise, both down-converted and up-converted signals are corrupted. This is illustrated in Figure 2.12 and Figure 2.13.

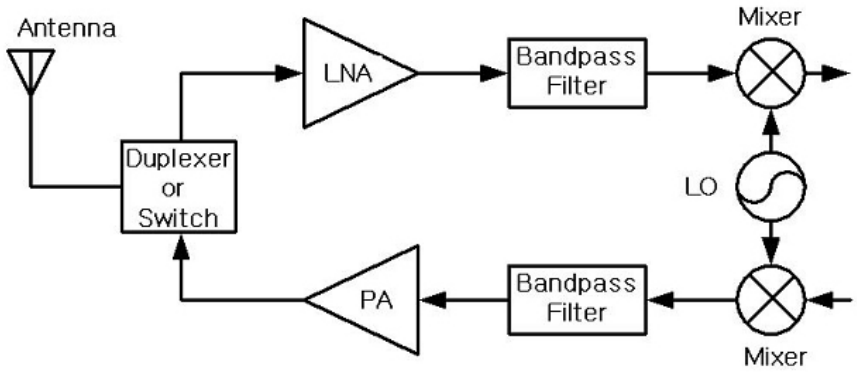


Figure 2.11 Typical front-end transceiver.

In an ideal case, the signal is convolved with an impulse and translated to a lower frequency without any signal distortion. However, in reality, the desired signal may be accompanied by a large interferer in an adjacent channel, and the LO has phase noise such as that shown in Figure 2.12. When these two signals are mixed with the LO output, the down-converted signal will consist of two overlapping spectra. The desired signal suffers from significant noise because of the tail of the interferer. This effect is called reciprocal mixing [1].

In the transmitter, the effect is slightly different. The situation in Figure 2.13 illustrates the problem when a noiseless receiver must detect a weak signal at frequency ω_2, while a powerful, nearby transmitter generates a signal at frequency ω_1 with substantial phase noise. The desired signal will be corrupted because of the phase noise tail of this transmitter [1].

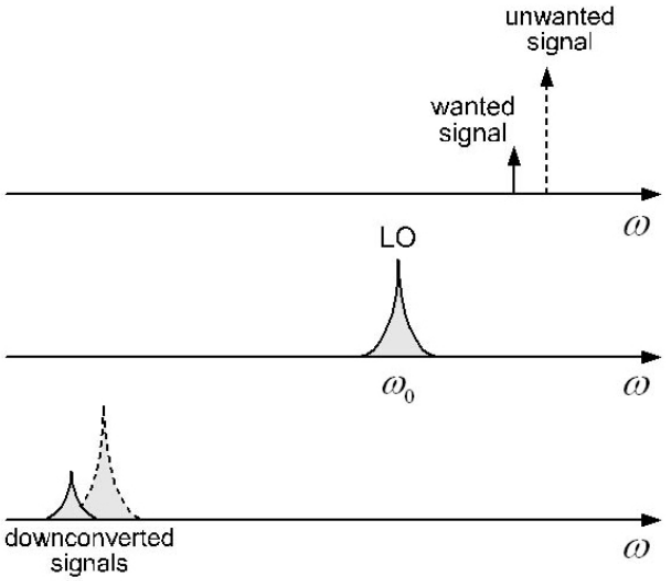


Figure 2.12 Effect of oscillator phase noise in a receiver

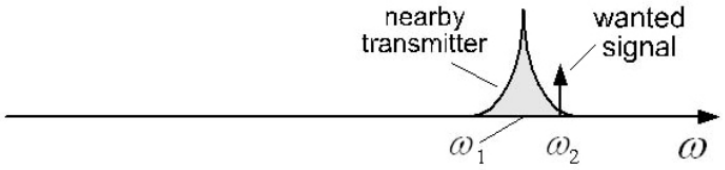


Figure 2.13 Effect of oscillator phase noise in a transmitter.

2.3.1.3 Phase Noise Models

Leeson's phase noise model, reported in 1966, is well known [7]. Leeson's model was extended in 1995 by J. Craninckx [19]. Even if Leeson's model has the empirical parameter, the model nevertheless provides the physical information to improve phase noise. It predicts phase noise as

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{2FkT}{P_S} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L \cdot \Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{3.7}$$

where F is an empirical parameter, k is Boltzman's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_L is the effective quality factor of the tank with all loading accounted for, $\Delta\omega$ is the offset from the carrier, and $\omega_{1/f3}$ is the frequency of the corner between $1/f^2$ and $1/f^3$ region, as shown in Figure 2.10.

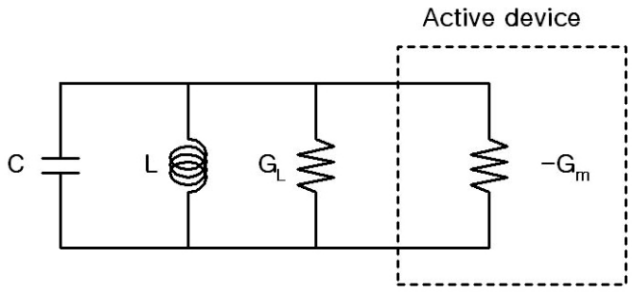


Figure 2.14 Equivalent one-port circuit for an LC oscillator.

The existence of a $1/f^2$ region can be predicted by the equivalent circuit, as shown in Figure 2.14. The impedance of a parallel RLC tank, for $\Delta\omega << \omega_0$, is easily calculated to be

$$Z(\omega_0 + \Delta\omega) \approx \frac{1}{G_L} \cdot \frac{1}{1 + j2Q_L \cdot \frac{\Delta\omega}{\omega_0}} \tag{3.8}$$

where G_L is the parallel parasitic conductance of the tank.

To maintain oscillations, the average energy provided to the tank by the active device side should be equal to the energy losses in the resonator circuit. Therefore, the active device side can be modeled as an effective parallel negative conductance, $-G_m$. For steady-state oscillation, the equation $G_m=G_L$ should be satisfied. When this condition holds, the net impedance of the oscillator model shown in Figure 2.14 is given by

$$Z(\Delta\omega) = \frac{v_{out}(\omega_0 + \Delta\omega)}{i_{in}(\omega_0 + \Delta\omega)} = -j\frac{1}{G_L} \cdot \frac{\omega_0}{2Q_L \cdot \Delta\omega} \tag{3.9}$$

The total equivalent parallel resistance of the tank has an equivalent mean square noise current density of $i_n^2/\Delta f = 4FkTG_L$. F is the device's excess noise number, which is a post-fitting parameter derived from measured data. Using the effective noise current power, the phase noise in the $1/f^2$ region of the spectrum can be calculated as [18]

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\overline{v_{noise}^2}}{v_{signal}^2}\right) = 10 \cdot \log\left(\frac{\frac{1}{2} \cdot |Z(\Delta\omega)|^2 \cdot \frac{\overline{i_n^2}}{\Delta f}}{\frac{1}{2} \cdot V_0^2}\right) = 10 \cdot \log\left[\frac{2FkT}{P_S} \cdot \left(\frac{\omega_0}{2Q_L \cdot \Delta\omega}\right)^2\right] \tag{3.10}$$

This expression of phase noise (3.10) is very useful for gaining a fundamental understanding of the critical factors for low phase noise.

This model can be extended in terms of the loaded-Q of the resonator in Figure 2.15. The losses in the LC-tank are represented by three resistances: the series resistance of the inductor (R_L), the series resistance of the capacitance (R_C), and equivalent parallel resistance (R_P) including all of the loading effect. By describing all the losses in the resonator individually, this model gives more insight on phase noise from the resonator perspective [19].

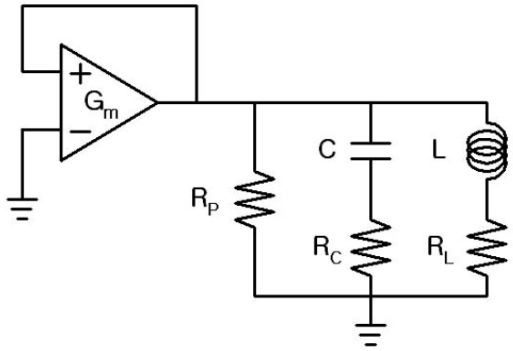


Figure 2.15 Equivalent circuit for an LC oscillator.

For the circuit of Figure 2.15, phase noise can be expressed as

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{kT \cdot R_{eff}\left(1+A\right)\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2}{\frac{1}{2}\cdot V_0^2}\right] \tag{3.11}$$

where A is an empirical fitting parameter, and R_{eff} is the effective series resistance, given by

$$R_{eff} = R_L + R_C + \frac{1}{R_P (C \cdot \omega_0)^2} \tag{3.12}$$

where R_L, R_C, R_P, and C are shown in Figure 2.15. While it is easy to obtain the series resistance, R_L and R_C, care should be taken to find R_P not only because of the substrate parasitics of both the inductor and the varactor but also because all of the loading effects from the active circuitry. (3.12) gives insight into an LC-tank design to achieve low phase noise.

2.3.2 Voltage-Controlled Frequency Tuning

Most wireless applications require a tunable oscillator, which means its output frequency is a function of a control input, usually a voltage. An ideal VCO is a circuit whose output frequency is a linear function of its control voltage (V_{con}), as shown in Figure 2.16,

$$f_{out} = f_o + K_{VCO} \cdot V_{con} \tag{3.13}$$

where, f_o is the oscillation frequency at $V_{con} = 0$ and K_{VCO} represent the gain or sensitivity of the circuit. The achievable range, $f_2 - f_1$, is called the frequency tuning range [9].

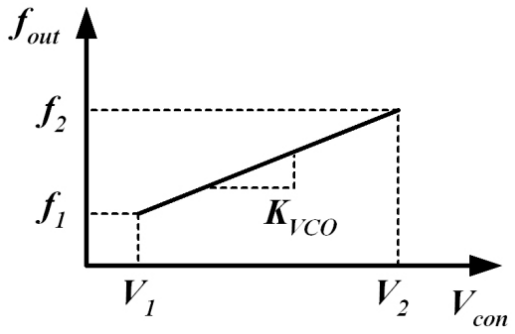


Figure 2.16 Definition of K_{VCO}

Frequency tuning is required not only to cover the whole application bandwidth but also to compensate for variations of the center frequency of the VCO that are caused by the process and by temperature. The oscillation frequency of an LC-tank VCO is approximately equal to $f_{osc} = 1/\left(2\pi\sqrt{LC}\right)$, so that only the inductor and capacitor values can be varied to tune the oscillation frequency. Even though there is an active inductor changing its inductance value when DC voltage is applied, it is generally such a noisy device that a VCO with an active inductor shows poor phase noise. Consequently, oscillators typically are tuned by changing the capacitance value in the tank through the use of a voltage-dependent capacitor, which is a varactor.

Two types of varactors are available for the Si process. One is a reversed-bias pn junction diode, and the other is MOS cap varactor. The pn junction diode suffers from several drawbacks. First, the n-well material has a high resistivity, creating a resistance in series with the reversed-biased diode and lowering the quality of the varactor. Second, the n-well incorporates a substantial substrate capacitance. This results in a constant capacitance to the tank and limits the tuning range.

It is well known that an MOS transistor with drain, source, and bulk (D,S,B) connected together realizes an MOS capacitor with a capacitance value dependent on the voltage V_{BG} between bulk and gate, as illustrated in Figure2.17 (a). With this PMOS varactor, the tuning capability of the circuit is impaired by the non-monotonicity of the capacitance value, as shown in Figure 2.17 (d) (—). There are two ways to obtain an almost monotonic function for the capacitance value. One is to ensure the MOS varactor not to operate in the accumulation region, and the other is not to operate in the inversion

region with values of V_G. The former is called an inversion mode MOS varactor and the latter an accumulation mode MOS varactor [20].

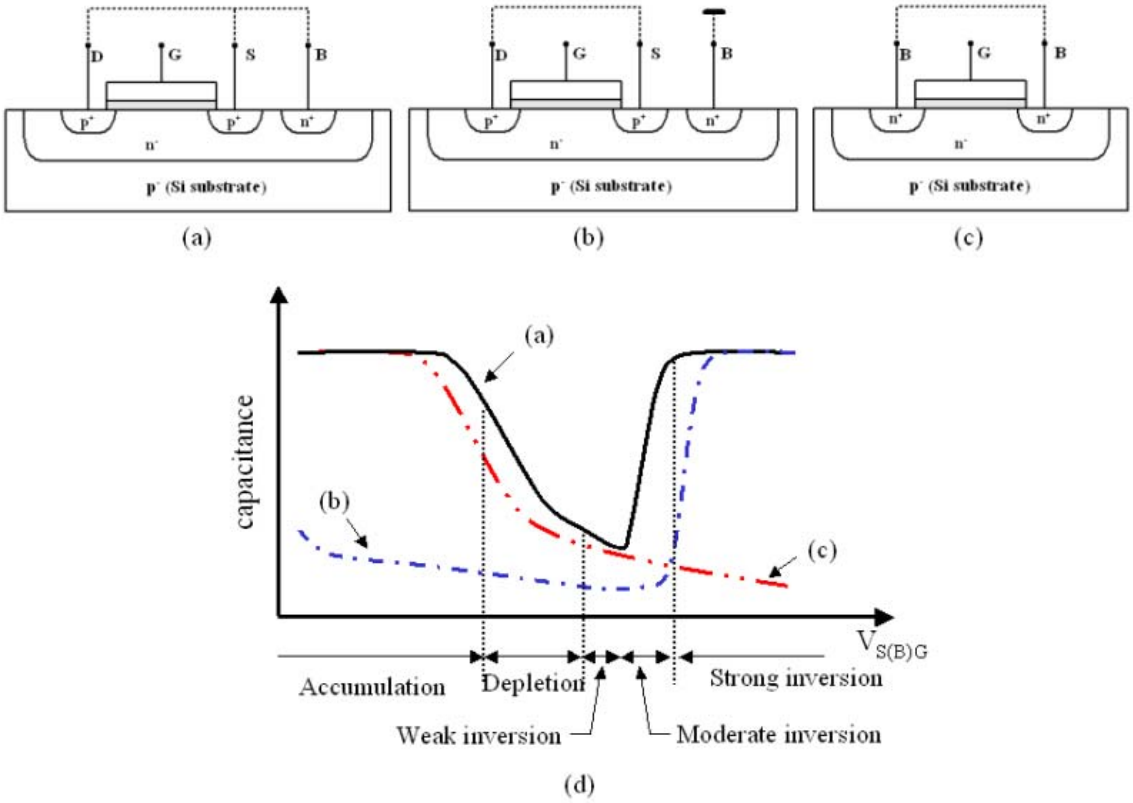


Figure 2.17 Configurations of three types of MOS varactors; (a) PMOS varactor, (b) inversion mode MOS varactor, (c) accumulation mode MOS varactor. (d) Capacitance values as a function of $V_{S(B)G}$.

An inversion mode MOS varactor can be realized by removing the connection between D-S and B, and connecting B to the highest dc voltage available in the circuit, as depicted in Figure 2.17 (b). This capacitor has the advantage of a lower parasitic resistance than the PMOS varactor but has a drawback of being more sensitive to

substrate-induced noise, because it cannot be implemented in a separate p-well. A more attractive alternative is to only use the MOS device in the depletion and accumulation regions, which is called an accumulation mode MOS varactor. This solution allows for the implementation of a MOS capacitor with large tuning range with much lower parasitics. This can be accomplished with the removal of the D-S diffusion from the MOS device, and implementation of the bulk contacts (n+) in the places left by D-S, as shown in Figure 2.17 (c), which minimizes the parasitic n-well resistance. Because of the advantages mentioned above, the accumulation mode varactor shows a wide tuning range as well as low phase noise characteristics [20]. In this dissertation, the accumulation mode MOS varactor is used for all VCO designs.

2.3.3 Power Consumption

Mobile devices are required to have long standby times, indicating a need for low power consumption. In a VCO design, it is difficult to have low phase noise with low power consumption simultaneously because the tank voltage amplitude is proportional to the current flowing. Therefore, there is a trade-off between phase noise and power consumption. It is presented in the Leeson's phase noise model.

The voltage amplitude of the tank for the CMOS cross-coupled differential topology shown in Figure 2.7 (d) can be expressed by assuming that the differential stage switched from one side to the other. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair can be modeled as a current source switching between I_{total} and $-I_{total}$ in parallel with an RLC tank. R_{eq} is the equivalent parallel resistance of the tank. The tank amplitude can be approximated as

$$V \approx I_{total} \cdot R_{eq} . \tag{3.14}$$

This is referred to as the current-limited operation because tank amplitude mainly depends on the total current flowing and the tank's equivalent resistance. However, (3.14) becomes invalid when the tank amplitude becomes the supply voltage through an increase of I_{total}. This operation is called the voltage-limited operation [18]. With current-limited operation, as the current increases (consuming more power), the phase noise lowers because the tank amplitude is increasing simultaneously.

CHAPTER III

ON-CHIP INDUCTORS

With the growth of commercial mobile wireless communication systems such as cellular, personal communications services (PCS), wireless local area networks (WLAN), satellite communications, and the global positioning system, customers' demands for smaller size and lower cost products have continuously increased. For this reason, modern mobile products require a multifunctional, highly integrated monolithic microwave integrated circuits.

Traditionally, inductors have been incorporated as discrete off-chip components, often as small surface-mount parts. Although such inductors have extremely good quality, it is desirable to remove as many discrete off-chip components as possible because of size and cost problems. Therefore, monolithic on-chip inductors play an important role in highly integrated circuits for wireless communication systems.

On-chip inductors are often used as narrow-band loads, resonators, and matching networks in RF circuits. The use of high-Q inductors improves circuit performance in terms of noise figures, insertion loss, gain, and efficiency. Therefore, even if the issues are not the exactly same, both Si- and GaAs- based IC technologies require high-Q on-chip inductors.

3.1 LOSS MECHANISMS IN INDUCTOR

Loss mechanisms should be investigated to design the high-Q inductor. The quality of an on-chip inductor depends on design parameters such as shape, width, thickness, spacing, and diameter as well as on the material properties used to implement an inductor. The losses in the inductor can be categorized into two domains. One is metal losses, and the other is substrate losses. The metal losses include the finite conductivity of the metal, current crowding at the edge because of the skin effect, and proximity effects because of the presence of a nearby metal layer. And substrate losses include the parasitics, eddy current, and radiation effects.

3.1.1 Metal Losses

Inductors are usually implemented with metal layers of aluminum (Al) in Si-based IC technologies and of gold (Au) in GaAs-based IC technologies. The conductivity of Al and Au metal is around 2.5×10^7 and 4×10^7 (1/Ωm), respectively. An inductor is wound using metal conductors with finite conductivity. Hence, the conductivity and the geometry of inductor metal layers determine the quality of inductors, especially at lower frequencies. The different metallization process is one of the reasons that inductors of GaAs-based MMICs show higher quality than Si-based MMICs. Most of the reactive energy is stored in the magnetic field of the inductor, but the energy is lost to heat in the volume of the conductors.

Because of the finite conductivity of metal layers there are resistive losses in metal windings. For rectangular-shaped conductors, the dc resistance can be expressed as

$$R_{DC} = \frac{l}{\sigma\, w\, t} \tag{3.1}$$

where σ, l, w, and t is the conductivity, length, width and thickness of the conductor. The thickness and conductivity of the metal layer are process parameters that limit design freedom. To provide a high-Q inductor, most of IC process foundries are building up special processes incorporating more conductive and thicker metallization.

Now Si-based processes provide more than four interconnection metal layers including a thick top metal layer. Such a metal layer is used for high-speed digital building blocks and clock lines. Thus, this option is widely available in the CMOS standard digital processes. Most RFIC designers are using this thick top metal layer as an inductor implementation. Because this top metal layer resides on top of a thick insulator, it ensures minimum parasitic capacitance to the substrate. Modern Si-based IC processes are opening up the possibility of designing structures with many different layers and complicated geometries.

Electro-migration in metal layers is another problem, setting an upper boundary for maximum safe current density. Although electro-migration with AC currents is less problematic, this remains one of the important limitations preventing integration of inductors for matching networks of a power amplifier. The necessary metal width would require large areas that would result in low self-resonant frequencies.

At low frequencies, DC resistance dominates with a constant current density as shown in Figure 3.1 (a). The magnitude of fields and currents decreases exponentially with penetration into the conductor at higher frequencies, which is called the skin effect. The skin effect results in current flowing in the outer area of the conductor, as illustrated

in Figure 3.1 (b). This reduces the effective cross sectional area of the conductor and causes a frequency-dependent increase in the series resistance. The rate of increase can be estimated by the effective depth of penetration (δ) of the current, which is skin depth,

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{3.2}$$

where f, μ, and σ represent the frequency in Hz, permeability in H/m, and conductivity in 1/Ωm.

At higher frequencies, magnetic fields penetrate the metal conductors and generate eddy current. The eddy current in the metal conductors reduces flux coupling that results in the reduction of the inductance value at higher frequencies [21]. A non-uniform current distribution is generated and is referred to as the proximity effect, as depicted in Figure 3.1 (c) [22].

When the inductor has multi-turns, the magnetic field in the vicinity of a particular conductor can be written as the sum of two terms, the self-magnetic field and the neighbor-magnetic field. Therefore, the increase in resistance of any particular conductor can be attributed to the skin effect as well as the proximity effect.

Figure 3.1 Visual representation of the effect on current distribution in the cross-section of inductor layer; (a) DC, (b) skin effect, and (c) proximity effect.

3.1.2 Substrate Losses

On-chip inductors may reside near a substrate. The substrate is a major source of loss and frequency limitation because of the conductive nature of Si in contrast to the insulating nature of GaAs. While the resistivity of Si substrate is commonly 10~20 Ωcm, that of GaAs substrate is $10^6 \sim 10^7$ Ωcm.

The conductive nature of the Si substrate creates various loss mechanisms. First, electric energy is coupled to the substrate through the displacement current. This displacement current flows through the substrate to nearby grounds, either at the surface or backside of the substrate. Second, the time-varying magnetic field generates a current in the substrate that is called the substrate eddy current. Current flowing in the lossy substrate generates ohmic losses. These are then reflected back to the inductor in a frequency-dependent way by increasing series resistance. Since the eddy current flows in the opposite direction of current flow in the inductor, the eddy current generates an opposing magnetic field. As a result, the series inductance of the inductor decreases.

A Si-based process consists of one or more conductive layers in the substrate. Conductive layers are added to the bulk substrate by various fabrication processes, such as diffusion, chemical vapor deposition, ion implementation and epitaxial growth. Oxide layers are grown for insulation between the metal layers and to insulate the metal layers from the substrate. In general, the more conductive the substrate layers are, the higher the substrate losses are. For a heavily conductive substrate, even though the magnetic and electric fields do not penetrate the substrate substantially, the surface currents flow on the substrate opposing magnetic fields that cause lower inductance value. Therefore, IC designers and process engineers should ensure that as few as possible conductive

substrate layers are located under or near an inductor. This is unfortunately not always possible because of planarization constraints. Furthermore the thickest possible oxide layer should be placed under the device to minimize substrate capacitance. This not only minimizes the losses, but also maximizes the self-resonance frequency of the inductor. Self-resonance will occur because of substrate capacitance and the inter-winding capacitance. Most bipolar and CMOS substrates come with a standard resistivity value of 10~20 Ωcm. With this value of resistivity, electrically induced losses dominate the substrate losses in the 1~10 GHz frequency range. In such a case, one must ensure that no conductive n or p wells appear below the device.

All other loss mechanisms can be lumped into radiation. Electromagnetically induced losses occur at much higher frequencies at the point where the physical dimensions of the device approach the wavelength at the frequency of interest. This frequency is actually difficult to quantify because of the various propagation mechanisms of the substrate. If propagation into the air is considered, the free-space wavelength is the appropriate factor. Electromagnetic propagation into the substrate occurs at lower frequencies because of the lower propagation speed, roughly by a factor of $\sqrt{\varepsilon_{Si}}$. Since $\varepsilon_\gamma \approx 11.9$ in Si, this is slightly slower than propagation in air. Furthermore, waves can propagate partially in the lossless oxide as well. Because the substrate is heavily conductive, the wave is confined to the oxide and the substrate acts like a lossy ground plane.

3.2 INDUCTOR MODEL

The lack of an accurate model for on-chip inductors presents one of the most challenging problems for Si-based RFICs. Various approaches for modeling inductors on

Si substrate have been reported in the past several years [23-26]. A compact, physical model is required for inductor design insights and optimization as well as for the circuit performance analysis. The difficulty of physical modeling comes from the complexity of high-frequency phenomena such as the skin effect, the proximity effect in the metal conductors, and the eddy current on the Si substrate.

In this dissertation, a physical, very compact, two-port equivalent inductor model is developed. The inductor model is used not only for the VCO design, but also for phase noise analysis of the VCO. Figure 3.2 (a) shows the most common Π model consisting of nine elements. The inductance and resistance of the inductor are represented by the series inductance, *Ls*, and the series resistance, *Rs*, respectively. The overlap between the spiral and the underpass allows direct capacitive coupling between the two terminals of the inductor. This is modeled by the coupling capacitance, *Cc*. The oxide capacitance between the spiral and the Si substrate is modeled by *Cox*. The capacitance and resistance of the Si substrate are modeled by *Csi* and *Rsi*, respectively. The substrate parasitic model components, *Cox*, *Csi*, and *Rsi* can be represented by two equivalent parameters, *Rsub* and *Csub*, as illustrated in Figure 3.2 (b). This inductor model is used for all the simulations during the VCO designs in this dissertation. Because differential topology is used for the VCO design, the center between the two inductors is virtually grounded, so that the VCO can be analyzed with the inductor model of Figure 3.2 (c). For phase noise analysis of the VCO, the inductor is also modeled like Figure 3.2 (d).

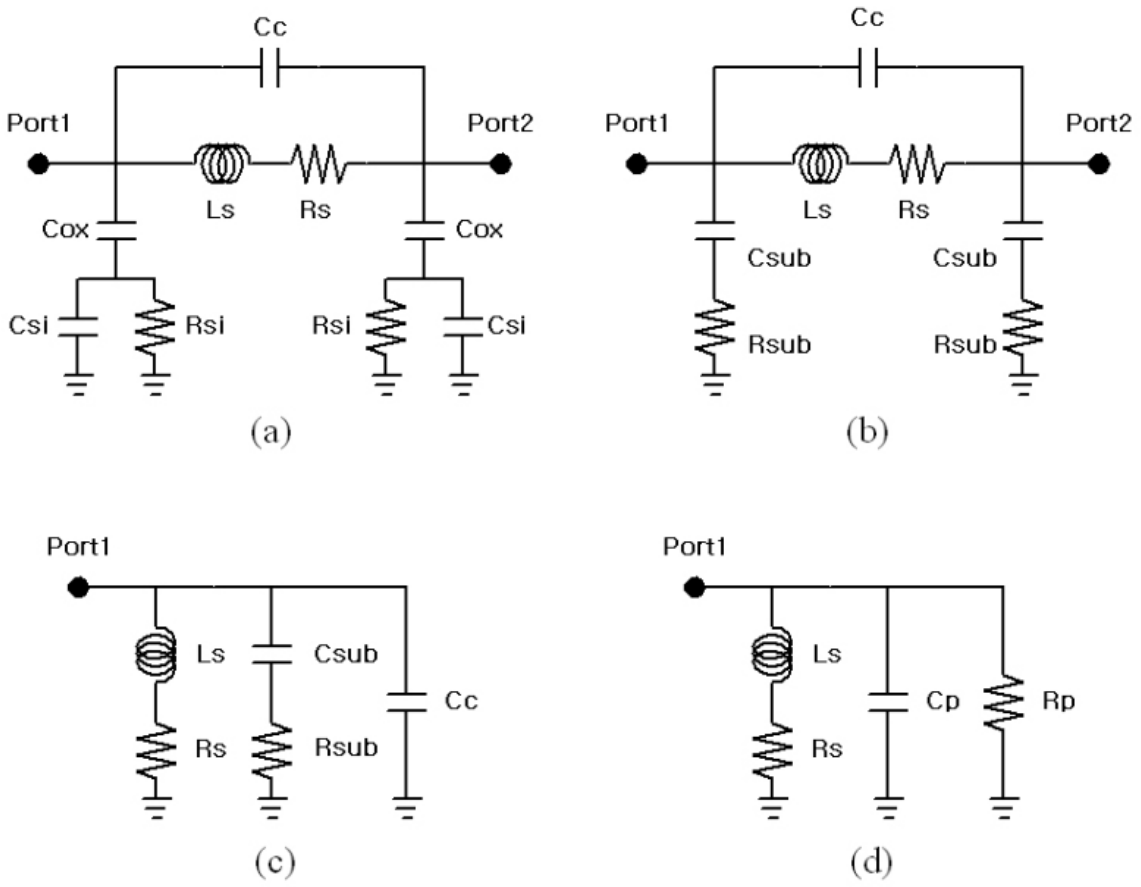


Figure 3.2 Inductor models: (a) conventional Π model, (b) model with equivalent substrate parasitics, (c) one-port model with the other port grounded, (d) model for phase noise analysis.

3.2.1 Series Inductance (*Ls*)

Even though the inductance value is slightly varied as the frequency increases, it is considered as a constant because it is mainly decided by the inductor geometry. Total inductance consists of the self-inductance and the mutual inductance. The self-inductance of a conductor layer with a rectangular cross-section area can be expressed as [27]

$$L_{self}(nH) = 2l\left(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right) \tag{3.3}$$

where l, w, and t are length, width, and thickness, respectively in cm. The mutual inductance between two parallel conductors can be calculated using

$$L_{mutual}(nH) = 2lQ \tag{3.4}$$

where l is length in cm and Q is the mutual inductance parameter, which can be computed with

$$Q = \ln\left[\frac{l}{GMD} + \sqrt{1+\left(\frac{l}{GMD}\right)^2}\right] - \sqrt{1+\left(\frac{GMD}{l}\right)^2} + \frac{GMD}{l}. \tag{3.5}$$

In (3.5), GMD donates the geometric mean distance between the conductors, which is approximately equal to the pitch of the conductors. An expression of GMD is given as

$$\ln GMD = \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \cdots \tag{3.6}$$

where w and d are the conductor width and pitch in cm, respectively. Based on Grover's formulas, Greenhouse developed an algorithm for computing inductance of planar rectangular spirals [28]. The Greenhouse method states that the overall inductance of a spiral can be computed by summing the self-inductance of each conductor segment and the positive and negative mutual inductance between all possible conductor segment pairs. More practically the inductance value of the model parameter can be found from measurement at very low frequency.

3.2.2 Series Resistance (*Rs*)

The series resistance, *Rs*, represents the metal loss mechanism described in the section of 3.1.1. The series resistance can be expressed as DC resistance by (3.1) when the thickness of the inductor metal layer is less than the effective thickness defining the area of current flowing, t_{eff}, [29]

$$t_{eff} = \delta \cdot \left(1 - e^{-t/\delta}\right) \tag{3.7}$$

where t is the thickness of metal layer and δ is the skin depth defined by (3.2). However, when the metal thickness is larger than t_{eff}, the series resistance should be express considering the effective current flowing area

$$R_{AC} \approx \gamma \cdot \frac{l}{\sigma\, w\, t_{eff}} \approx \gamma \cdot \frac{l}{2\sigma\, \delta\, (w+t)} \tag{3.8}$$

where δ is the skin depth and γ is a factor including the proximity effect and the substrate eddy current effect. γ is usually 2~3.

3.2.3 Substrate Parasitics (*Rsub*, *Csub*)

The substrate parasitics of the inductor on the Si substrate can be physically modeled by a three-element network consisting of *Cox*, *Rsi*, and *Csi*, as shown in Figure 3.2 (a). *Cox* represents the oxide capacitance whereas *Rsi* and *Csi* represent the Si substrate resistance and capacitance, respectively. The physical origin of *Rsi* is the Si conductivity which is predominately determined by the majority carrier concentration. *Csi* models the high frequency capacitive effects occurring in the semiconductor.

In this dissertation, the inductors realized by different processes such as GaAs IC technology and packaging technologies are modeled. Therefore, for a fair comparison

among the inductors implemented in different processes, the substrate parasitics of all the inductors are modeled using equivalent *Rsub* and *Csub*. The substrate equivalent parasitics, *Rsub* and *Csub*, are approximately proportional to the area occupied by the inductor and can be estimated by

$$Csub \approx \frac{1}{2} \cdot l \cdot w \cdot Cunit \qquad Rsub \approx \frac{2}{l \cdot w} \cdot Runit \tag{3.9}$$

where *Cunit* and *Runit* are capacitance and resistance per unit area for the substrate parasitics. The area of the spiral is equal to the product of the spiral length (*l*) and width (*w*). The factor of the two accounts for the fact that the substrate parasitics are assumed to be distributed equally at the two ends of the inductor. *Cunit* and *Runit* are functions of the substrate resistivity and inter-dielectric thickness. Those are extracted from the measurement results.

3.2.4 Quality Factor of Inductor

The performance indices for the quality of an inductor need to be defined to perform a study of an integrated on-chip inductor. In general, the complex power delivered to a one-port network at a frequency is given by [30]

$$P = \frac{1}{2} \oint_S E \times H \cdot ds = P_l + 2j\omega(W_m - W_e) \tag{3.10}$$

where P_l represents the average power dissipated by the network and W_m and W_e represent the time average of the stored magnetic and electric energy. The input impedance can be defined as follow

$$Z_{in} = R + jX = \frac{V}{I} = \frac{VI^*}{|I^2|} = \frac{P_l + 2j\omega(W_m - W_e)}{(1/2)|I^2|} \tag{3.11}$$

If $W_m > W_e$ the device exhibits an inductive characteristic. If $W_m < W_e$ the device exhibits a capacitive characteristic. The quality (Q) factor is the traditional measure of how the behavior of a real passive device resembles the ideal. It has the following general definition

$$Q = 2\pi \frac{E_{stored}}{E_{dissipated}} \tag{3.12}$$

where E_{stored} is the maximum energy stored per cycle, whereas $E_{dissipated}$ is the energy dissipated per cycle. From (3.11) with T equal to the cycle time

$$Q = 2\pi \frac{(W_m - W_e)}{P_l \cdot T} = \frac{\omega(W_m - W_e)}{P_l}. \tag{3.13}$$

Using the fundamental definition of Q-factor for inductors and the equivalent model of Figure 3.3, the Q-factor is expressed as [31]

$$\begin{aligned} Q &= 2\pi \times \frac{\left| \ Peak\ \ Magnetic\ \ Energy - Peak\ \ Electric\ \ Energy \ \right|}{Energy\ \ Loss\ \ in\ \ One\ \ Oscillatio\, n\ \ Cycle} \\ &= \frac{\omega \cdot Ls}{Rs} \times \frac{Rp}{Rp + \left[\left(\frac{\omega \cdot Ls}{Rs}\right)^2 + 1 \right] \cdot Rs} \times \left(1 - \frac{Rs^2 \cdot Cp}{Ls} - \omega^2 \cdot Ls \cdot Cp \right) \end{aligned} \tag{3.14}$$

where the first term represents the magnetic energy stored along with the ohmic loss. The second represents the substrate loss. The last describes self-resonance. Practically the Q-factor can be extracted from the measurement. With the input impedance, Z11, from the measurement, the Q-factor can be calculated by

$$Q = \frac{\mathrm{Im}\ (Z11)}{\mathrm{Re}\ (Z11)} \tag{3.15}$$

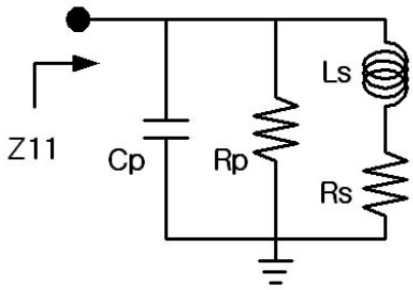
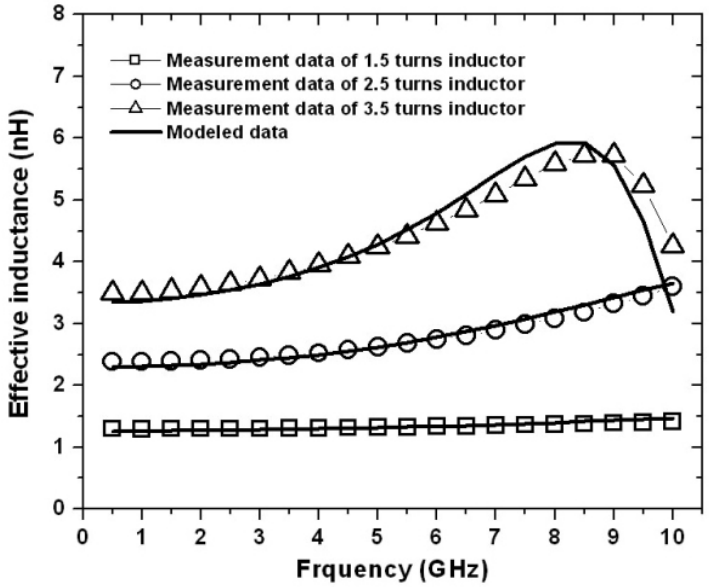


Figure 3.3 One-port, the simplest, equivalent inductor model.

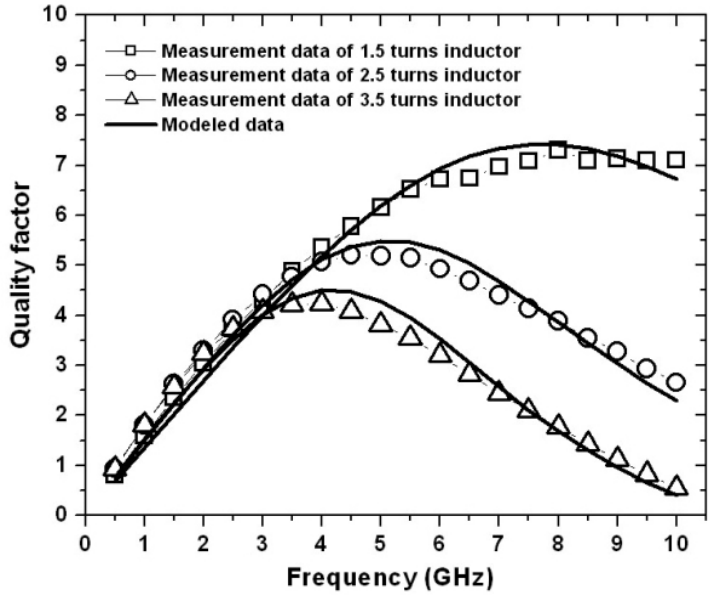
3.3 Experimental Results of On-chip Inductors

On-chip inductors on both Si and GaAs substrate have been designed, measured, and characterized by physical modeling to examine the inherent low Q-factor of the on-chip inductors in terms of material properties and geometries. Both are commercial processes presenting very reasonable values.

On-chip inductors on Si substrate have been implemented using a standard, commercial CMOS process with five metal layers. For metallization, Al with a conductivity of 2.5×10^7 S/m is incorporated. The top metal layer, which has a thickness of 1 μm, is used for the inductor design. The thickness of the inter-dielectric material, SiO_2, between the inductor layer and the Si substrate is 5 μm. The Si substrate has a resistivity of 10 Ω·cm. The width and spacing of inductor layers are designed by 10 μm and 2 μm, respectively. The outer diameter is 160 μm. Inductors with the number of 1.5, 2.5, 3.5 turns are designed. The inductances are in the range of 1.2 ~ 3.4nH, as listed in Table 3.1. Even though the maximum Q-factors are between 4 and 7 around 4~7 GHz, the Q-factors of three inductors at 2GHz are 3, as shown in Figure 3.4. Because of thin Al metallization and the conductive substrate, the on-chip Si inductors show low Q-factors.



(a)



(b)

Figure 3.4 Measurement and model data of Si on-chip inductors: (a) effective inductances and (b) Q-factors.

Table 3.1 Model parameters of Si on-chip inductors.

Turns	Ls (nH)	Rs (Ω)	Csub (fF)	Rsub (Ω)	Cc (fF)
1.5	1.26	5.8	25	340	12
2.5	2.3	9.5	42	220	20
3.5	3.35	13.6	53	170	24

An on-chip inductor on a GaAs substrate is designed and compared with the Si on-chip inductor from a quality perspective. The GaAs inductor is implemented using a commercial GaAs IC process with three metal layers. The metal is Au with a conductivity of 4×10^7 S/m. Three metal layers have a thickness of 0.6, 2, and 4 μm, respectively. For the inductor design, the last two metal layers are stacked to reduce the series resistance resulting in 6 μm thick. For the inter-dielectric material, BCB showing low dielectric constant and low loss is incorporated with a thickness of 1 μm. The dielectric constant and loss tangent of the substrate are 2.8 and 0.0006, respectively. The GaAs substrate, which is considered semi-insulating, has a loss tagent of 0.0006. The width and spacing of the inductor layer are designed as 10 μm, and the outer diameter as 160 μm. 3.25 turns were used to obtain 1.5 nH. The maximum Q-factor is 16 at 7 GHz, as shown in Figure 2.5. Because of the semi-insulating nature of the substrate, inter-dielectric material with low dielectric constant and low loss, and thick Au metallization, a GaAs on-chip inductor shows higher Q-factor than a Si on-chip inductor.

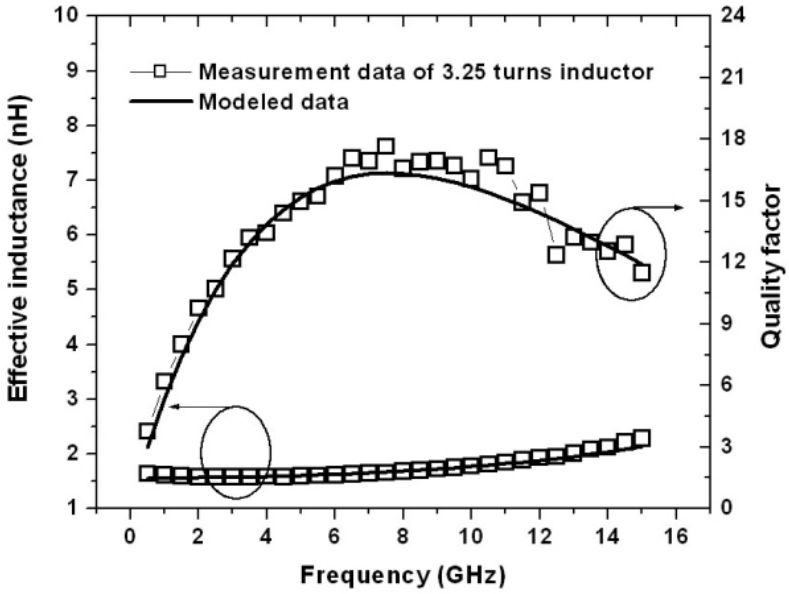


Figure 3.5 Measurement and model data of a GaAs on-chip inductor.

Table 3.2 Model parameters of a GaAs on-chip inductor.

Turns	Ls (nH)	Rs (Ω)	Csub (fF)	Rsub (Ω)	Cc (fF)
3.25	1.55	$1.42\sqrt{f}$	3	3000	20

3.4 HIGH-Q INDUCTOR TECHNIQUES ON SI SUBSTRATE

It is well known that GaAs IC technology provides a good quality inductor because of its semi-insulating substrate and thick Au metal layer. The GaAs inductor exhibits a Q-factor of about 20. However, for RF ICs, the trend is moving gradually toward Si-based IC technologies. Therefore, a lot of special approaches have been published to achieve a

high-Q inductor on Si substrate. From a physical standpoint, the way to do this is easy to describe: If the inductor is far from the Si substrate and has a thick metallization, the Q-factor will increase. However, standard CMOS Si technology provides a thickness of SiO_2 of less than 5 μm and a metal layer of around 1~3 μm thick. Hence, it is difficult to get a Q-factor of more than 5 for an inductor in the standard CMOS process. This is too lossy to design RF circuits meeting stringent wireless specifications.

To fabricate a high-Q inductor for RF applications, advanced Si processes have been developed. The processes can be categorized into two categories. One approach is to reduce the series resistance (Rs) of the inductor layer, and the other is to suppress the substrate parasitics (Rsub, Csub). To lower the series resistance, Cu alloy is used rather than pure Al because of the high conductivity of Cu. An alternative for small series resistance is to stack the metal layers vertically [32]. Si-based IC process foundries usually provide at least four metal layers with a maximum 3 μm-thick top metal. By stacking all the metal layers, a thickness of 5μm is almost achievable. However, this stacking approach increases substrate parasitics.

Efforts to cope with substrate parasitics focus either on the substrate itself or on the distance between the substrate and the metal layer. In working with the substrate itself, a highly resistive Si substrate of up to 500 Ω·cm [32] is used in comparison to the conventional one of only 15~20 Ω·cm. The usual way to place the top metal layer far from the substrate is to deposit thick inter-dielectric SiO_2. The thickness of SiO_2 has recently grown up to 10 μm. Even a thick SiO_2 is grown in the substrate below the inductor layer [33].

To achieve small series resistance and low substrate parasitics, a post-process has been suggested [34]. After finishing the standard Si process, a thick, low-loss dielectric material with a low dielectric constant is coated on the wafer. Then, a thick, highly conductive Cu metal layer is plated for the inductor. Although the Q-factor of the inductor goes up to around 20 with all these advanced processes, all these special non-standard processes increase the cost, and thus, weaken the need for moving toward Si-based IC technologies.

A simple technique, without any additional processes, like a patterned-ground-shield (PGS) has been proposed to suppress the eddy current effects resulting from the conductive nature of Si substrate [31]. However, the improvement is not enough to design high performance RFICs.

For some time, a bond wire has been considered as a good candidate for a high-Q inductor. Originally the bond wire played the role of an interconnection between the chip and the package lead frame. Because the diameter of the bond wire is usually 25 μm thick, and the bond wire is far from the substrate, it exhibits a high Q-factor. Generally, the bond wire shows 0.7 nH/mm. To obtain larger inductance, a longer bond wire is required, which causes reproducibility and reliability issues. Therefore, it is hard to obtain inductances above 1nH. In the literature of [35], a bond wire as an inductor is discussed in detail.

Micro-electro-mechanical system (MEMS) technologies have been incorporated to overcome the shortcomings of a low-Q Si inductor. The inductor hanging in air is implemented by the Si surface micro-machine technology using a sacrificial metal layer [36]. A bulk Si micro-machine technology also has been incorporated to achieve a high-Q

inductor. Si substrate etching, below the inductor layer, has been processed [37]. Even the back side of Si substrate is etched to reduce substrate effects [38]. However, MEMS techniques need additional process steps that are not cost effective. Furthermore, reliability issues with MEMS techniques create a critical yield problem.

CHAPTER IV

HIGH-Q INDUCTOR EMBEDDED IN A MULTI-LAYER IC PACKAGE

4.1 INTRODUCTION TO IC PACKAGING TECHNOLOGIES

The primary functions of an IC package are to protect, power, and cool the microelectronic devices and to provide electrical and mechanical connections between the IC and the outside world. The package is generally fabricated independent of the ICs. When IC fabrication is finished, the next step is packaging. First, the IC is mounted inside of the package. Then, the pads on the IC are connected to corresponding input/output (I/O) terminal pads in the package by the use of Au or Al wire-bonds. The I/Os are the connections that pass electronic signals in and out of the chip. Once the IC die is wire-bonded to the package, the whole structure is molded with a plastic material. Only the package I/O terminals are seen, and everything else is sealed [39].

There are roughly two categories of packages. One is a single-chip package (SCP), and the other is a multichip package (MCP), usually called a multichip module (MCM). A SCP supports a single microelectronic device. One of the popular SCPs is ball grid array (BGA) package. If a package includes more than one active device, it is called a MCM. System designers may use a combination of SCPs and MCMs to meet the specific application needs of the system. The MCM was developed from the traditional hybrid package. The substrate or carrier is the key element in the MCM. The substrate provides

the mechanical attachment for the chips, handles the inter-chip signals, provides power and ground for all chips, and interfaces the module with the next level system elements. Recently, wafer-level packaging (WLP) technology, which can be categorized as a SCP, is being referred to as the current path for the development of future packages [39].

Thick Au, Ag, or Cu metallization is commonly used for the wiring metal layer in a package. In some cases, the multi-layer configuration is incorporated for multiple I/Os and interconnections. The multi-layer feature and thick metallization with high conductivity make it possible to implement the high-Q inductor in a package [40-45]. In the following sections, each package is described in detail. The design, implementation, measurement, and characterization of the embedded inductor in each package are presented.

4.2 SINGLE-CHIP PACKAGE

A single-chip package is a package including only a single microelectronic device. The main function of a SCP is to enable the device or chip within the package to perform its designed function reliably. Every SCP must provide an efficient signal transmission and power distribution among ICs or subsystems on the board. It should enable the device to be attached to the next level of packaging through proper interconnections. When heat is generated by the device during its operation, the package should dissipate it effectively. The package should protect the device from external forces that may damage the device.

SCPs may be classified into two types by means of the methodology used in assembling the packages to the printed wiring board (PWB). One is a pin-through-hole

package, and the other is a surface-mount package. While the pin-through-hole packages have pins that can be inserted into holes in the PWB, the surface-mount packages are not inserted into the PWB, but are mounted on the surface of the PWB. The surface-mount packages have the advantage of higher packing density compared to the pin through-hole package because the surface mount packages can be mounted on both sides of the PWB.

Surface-mount packages fit into two categories that are defined by the location of I/Os. While the surface-mount technology (SMT)-peripheral has I/Os distributed along the sides of the package, surface-mount technology (SMT)-area array has I/Os distributed in an area array under the package surface to achieve more I/O connections.

Traditionally, packages have leads that can be attached to the PWB. In the late 1980s, packages with solder balls were developed as an alternative to packages with leads. The I/Os can be increased substantially by using solder balls under the surface-mount packages in an area array. One example of the SMT-area array is a ball-grid array (BGA) package.

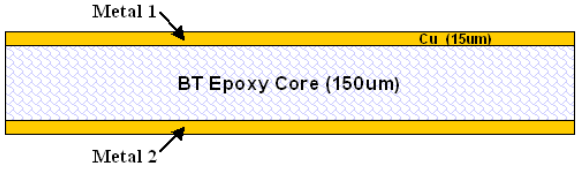
4.2.1 Fine-Pitch Ball-Grid Array Package

A fine-pitch ball-grid array (FBGA) is a BGA package with fine pitch size between the solder ball pads. The size and performance limitations of packages with leads distributed peripherally are overcome by a BGA package. A BGA package can accommodate the addition of pins with very little increase in the size of the package itself. Therefore, less space is occupied on the PWB by the I/O pins. Furthermore, the signal line in a package and the height of the interconnection solder balls is shorter than in lead-

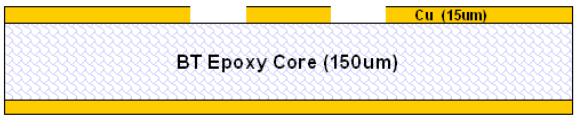
frame packages. This helps to improve the overall electrical performance by reducing the parasitics created by the leads in the package.

Usually a FBGA package has a multi-layer feature because the multi-layers are required to realize the array of solder ball pads. To make a fine pitch size between pads the metallization process needs to have a fine design rule. In addition, the metal layer is a thick copper. Because of a multi-layer configuration with a fine design rule and a thick copper metallization, a high-Q inductor can be realized in the FBGA package.

The process flow of a FBGA package is illustrated in Figure 4.1. The substrate is a common two-metal-layer board with a thickness of 150 μm, as shown in Figure 4.1 (a). The substrate core is made up of BT-epoxy, and both sides of the substrate are covered with a 15μm thick copper layer. First, the copper layers are patterned to make pads for wire-bonding (Figure 4.1 (b)). Then, the via-hole processes are followed (Fig 4.1 (c)). The diameter of a via-hole is 100 μm. The launching- and landing-pad for via-process are 250 μm. For the interconnection between two layers, 10 μm thick copper is plated so that the total thickness of both metal layers becomes 25 μm (Fig 4.1 (d)). After plating, solder masks with a thickness of 30 μm are laminated on both sides (Fig 4.1 (e)). The solder mask layers are patterned for pad opening (Fig 4.1 (f)). Using Ag-epoxy, an IC chip is mounted (Fig 4.1 (g)), and then wire-bonding is performed (Fig 4.1 (h)). Finally it is encapsulated by EMC (epoxy molding compound) material as shown in Figure 4.1 (i).



(a)



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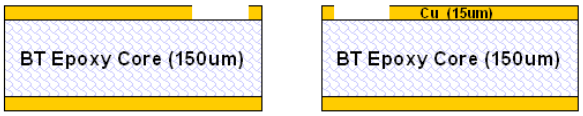

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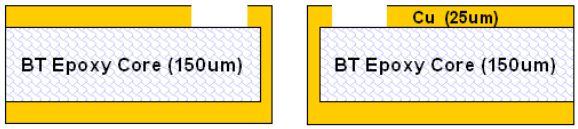
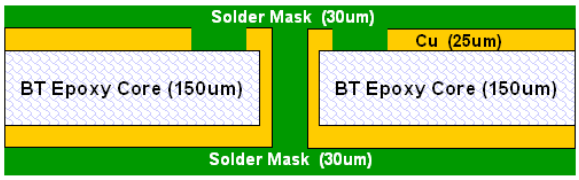


(d)

Figure 4.1 Process flow of a FBGA package: (a) substrate, (b) substrate patterning, (c) via-hole process, (d) copper plating, (e) solder mask laminating, (f) solder mask patterning, (g) IC chip mounting, (h) wire-bonding, (i) molding.



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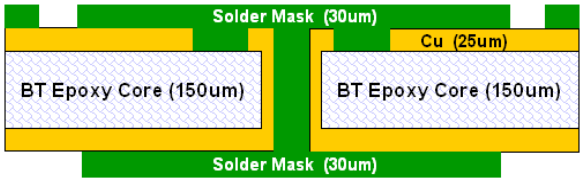

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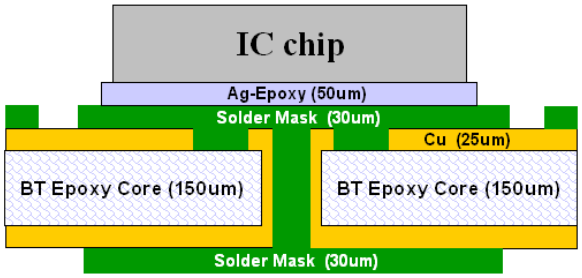
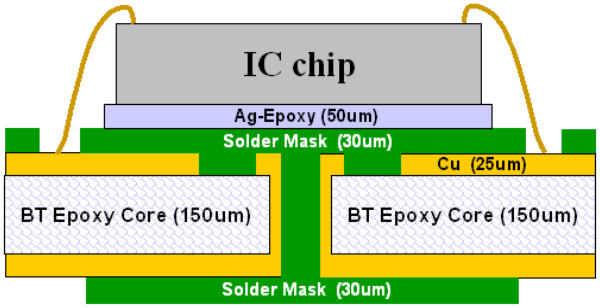


(g)

Figure 4.1 (continued) Process flow of a FBGA package: (a) substrate, (b) substrate patterning, (c) via-hole process, (d) copper plating, (e) solder mask laminating, (f) solder mask patterning, (g) IC chip mounting, (h) wire-bonding, (i) molding.



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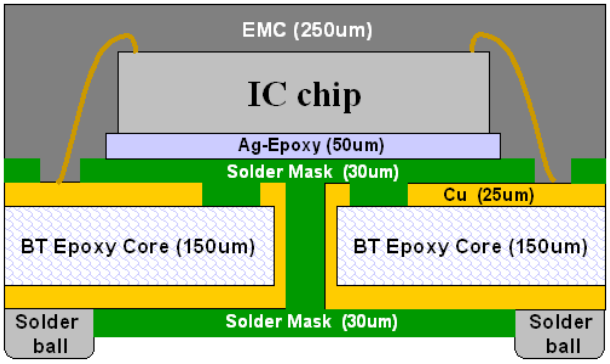


(i)

Figure 4.1 (continued) Process flow of a FBGA package: (a) substrate, (b) substrate patterning, (c) via-hole process, (d) copper plating, (e) solder mask laminating, (f) solder mask patterning, (g) IC chip mounting, (h) wire-bonding, (i) molding.

4.2.2 Experimental Result of High-Q Inductor Realization in a FBGA Package

A high-Q inductor is implemented in a FBGA package using wiring metal lines, which is called a FBGA inductor. The metal layer 1 in Figure 4.1 is used for the inductor layer, and the ground layer is designed using metal layer 2. There is no ground plane

under the inductor layer. This is called a hollow ground plane configuration, to avoid substrate parasitics. The dielectric constant and loss tangent are 4.6 and 0.016, respectively. The thickness of an inductor metal layer and a solder mask layer are 25 μm and 30 μm, respectively. The width and spacing of an inductor is designed as 80 μm, the minimum feature size. The top view of the implemented inductor, the cross section of the implemented inductor from A to A*, and the cross-section of the via-hole is shown in Figure 4.2, Figure 4.3, and Figure 4.4, respectively.

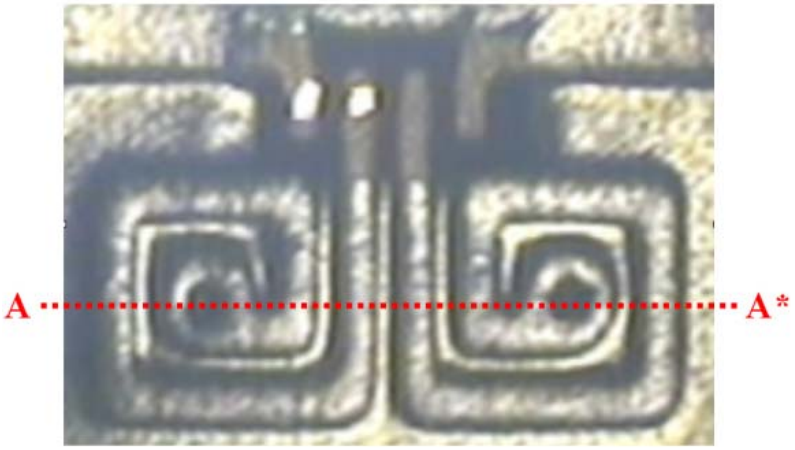


Figure 4.2 Top view of the implemented FBGA inductor.

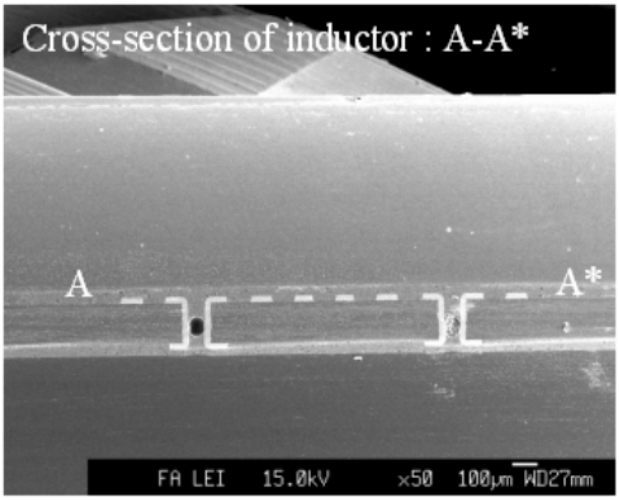


Figure 4.3 Cross section of the implemented FBGA inductor from A to A* in Figure 4.2.

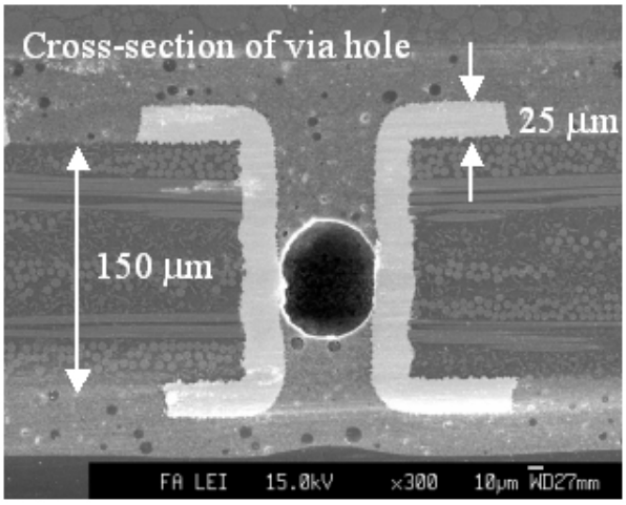


Figure 4.4 Cross section of the via-hole.

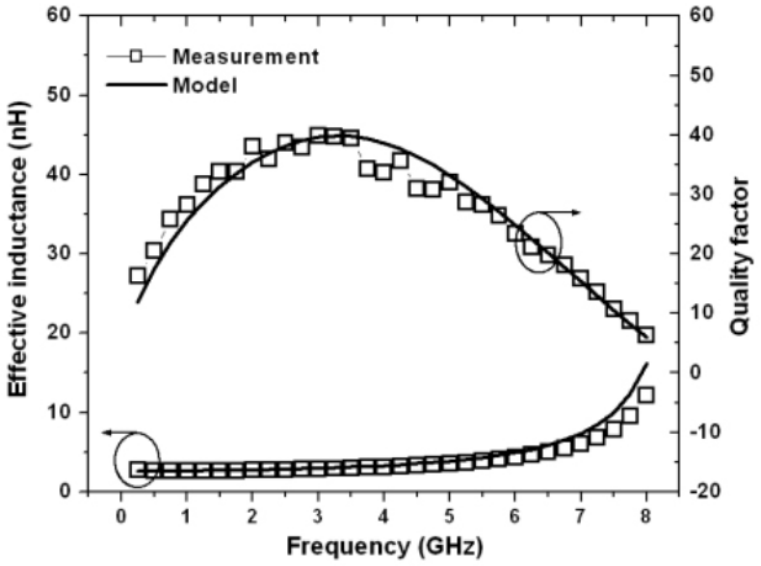


Figure 4.5 Measurement and model data of the implemented FBGA inductor.

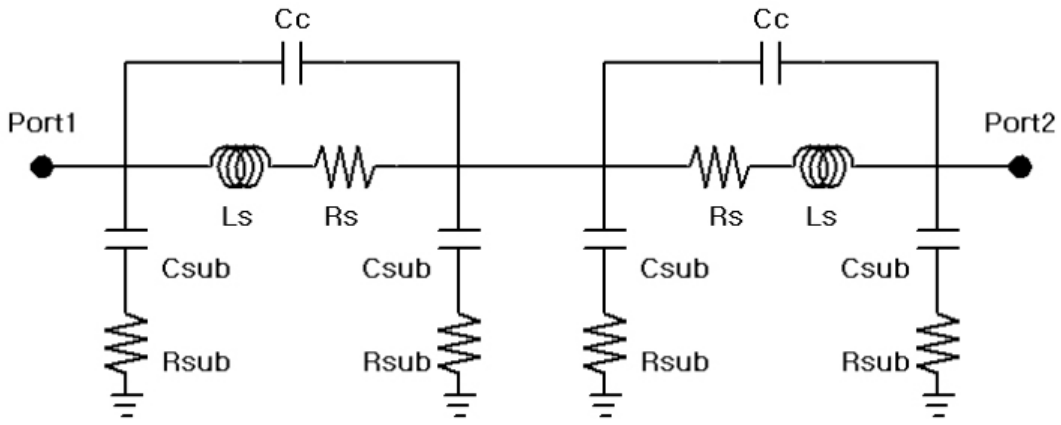


Figure 4.6 Model for the implemented FBGA inductor.

Table 4.1 Model parameters of the implemented FBGA inductor.

Turns	Ls (nH)	Rs (Ω)	Csub (pF)	Rsub (Ω)	Cc (pF)
3	1.3	$0.285\sqrt{f}$	0.004	4000	0.24

The measured (□) and modeled (—) data (effective inductance and Q-factor) of the implemented FBGA inductor are shown in Fig 4.5. The inductor is designed by combining two identical inductors in series, so that the model illustrated in Figure 4.6 is used for modeling. Each inductor has 1.5 turns and is connected through a via-hole. The model parameters are listed in Table 4.1. The total inductance of the inductor is 2.6 nH, and the maximum Q-factor is 40 at the frequency of 3 GHz. The self-resonant frequency is more than 10 GHz.

4.3 MULTICHIP PACKAGE

An attractive implementation of integrated systems is to separate the whole system into multiple IC chips and to use a multichip package (MCP) to interconnect these different IC chips. At the same time, MCM technology can also be used to integrate a large number of the required passive components.

A multi-chip package (MCP) or multi-chip module (MCM) is defined as a single unit containing more than two IC chips and an interconnection substrate. The main function of an MCM is signal interconnection and I/O management for each IC chip. The MCM integrates IC chips so closely that the overall volume and weight are less than the

integration of individually packaged ICs. The substrate or carrier is the key element in a MCM. The substrate provides the mechanical attachment for the chips, handles the inter-chip signals, provides power and ground for all chips, and interfaces the module with the next level system elements.

The MCM is useful when overall system functionality cannot be achieved in a single chip. As this integration continues rapidly, finally it may be possible to integrate all the functionality into a single chip. In this case of a single-chip integration, a single-chip package will be necessary. Until the realization of a single-chip integration, MCM will be required. Currently, the integration of all the required functionality into a single chip results in complex technical requirements that involve high development and manufacturing costs. Because MCMs use less complex chips and can be repaired, MCMs are considered a less expensive package that can be developed easier and faster. Therefore, until a single chip approach can be performed with high yield and low cost, the MCM will remain a good candidate for system packaging.

MCM technologies may be divided into three major categories depending upon the materials or multi-layer processing method. These three categories are:

1) MCM-L: laminated thick organic layers on a FR-4 core substrate.
2) MCM-C: co-fired ceramic layers.
3) MCM-D: deposited thin film layers on a Si, alumina, or glass substrate carrier.

Each type of MCM has its own position in the technological hierarchy. MCM-L evolved from a conventional PWB technology. Compared to conventional PWBs, advanced processing techniques result in smaller feature size and allow the incorporation of blind vias as well as buried vias. The use of both vias increases the wiring density of

components. MCM-L is the least expensive package, however, it has the lowest density among three MCM package types. MCM-L is also known as chip-on-board (COB).

The MCM-C substrates have been derived from traditional thick-film fabrication techniques in pursuit of enhanced performance and increased packaging density. In the traditional thick-film process, the features are created by screen-printing. This limits the line widths and spaces that can be achieved. An alternate and more advanced ceramic processing method is the co-fired technique. Co-fired ceramic technology is divided into two categories based on their firing temperature. One is a low temperature co-fired ceramic (LTCC), and the other is a high temperature co-fired ceramic (HTCC). To permit firing at low temperatures, the ceramic contains a large amount of glass. The glass reduces the fusing point and also lowers the relative dielectric constant, which improves circuit performance at high frequencies. Furthermore, the large amount of glass in the dielectric yields thermal expansion close to that of Si and GaAs. However, the glass also reduces thermal conductivity.

Although MCM-Ds are the most expensive, they typically provide high packaging density. Therefore, MCM-Ds can be cost competitive, especially in large volume. In MCM-Ds, both the metal and dielectric layers are sequentially deposited in the form of thin-films and patterned by a photolithography. Typically, Si wafers are used as the MCM-D substrate because of low cost. Feature sizes such as conductor widths, gaps, and vias can be less than 25 μm. Table 4.2 present a comparison of the three MCM types [39].

The feasibility of a high-Q inductor embedded in MCM packaging substrates has already been reported many times in recent literature. The MCM-D technology with a

thin dielectric film also has been investigated for high-Q inductor realization in [40-41]. Inductors implemented in LTCC substrates have been published in [42-43].

Table 4.2 Comparison of three MCM types.

Design parameters	MCM-L	MCM-C	MCM-D
Feature size (line /space) (mm)	125/125	100/125	20/20
Via size (μm)	250	200	20
Dielectric constant	3.5~4.5	5.2~7.8	2.9
Dielectric thickness (μm)	112	100	1~10

4.3.1 MCM-L Organic Package

The MCM-L organic packaging technology used in this thesis incorporates low-cost materials and processes. The core substrate is laminated with two thin organic layers on both sides. The core substrate is a double-sided FR-4 board. The dry film epoxy (Shipley Dynavia 2000) is used for the inter-dielectric material. A copper metallization is performed. An unfilled via process is used for connecting two layers.

Figure 4.7 depicts the process flow of a MCM-L organic package, and the cross-section of the substrate is shown in Figure 4.8. The substrate is a common FR-4 board with a thickness of 1 mm, as shown in Figure 4.7 (a). Both sides of the substrate are covered with a 12 μm-thick copper layer. First, the copper layers are patterned for wiring metal lines (Figure 4.7 (b)), and the dry film epoxy is laminated (Figure 4.7 (c)). Then, the via-hole processes are followed (Fig 4.1 (d)). The diameters of a via-hole and a

landing pad are 100 μm and 200 μm, respectively. As shown in Figure 4.8, the via process is unfilled via. For the second metal layer and the interconnection between two layers, 10 μm thick copper is plated (Fig 4.1 (e)). Lamination, via, plating processes are followed once more to make another redistribution metal layer (Fig 4.1 (f), (g), (h))

(a)

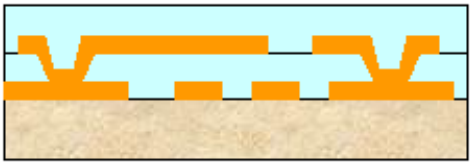
(b)

(c)

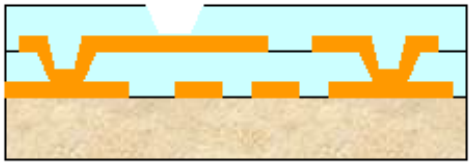
Figure 4.7 Process flow of MCM-L: (a) FR-4 core substrate, (b) circuitize 1st Cu layer, (c) laminate 1st dielectric layer, (d) photo-define 1st vias, (e) Plate vias and circuitize 2nd Cu layer, (f) laminate 2nd dielectric layer, (g) photo-define 2nd vias, (h) Plate vias and circuitize 3rd Cu layer.

(d)

(e)



(f)



(g)

Figure 4.7 (continued) Process flow of MCM-L: (a) FR-4 core substrate, (b) circuitize 1st Cu layer, (c) laminate 1st dielectric layer, (d) photo-define 1st vias, (e) Plate vias and circuitize 2nd Cu layer, (f) laminate 2nd dielectric layer, (g) photo-define 2nd vias, (h) Plate vias and circuitize 3rd Cu layer.

(h)

Figure 4.7 (continued) Process flow of MCM-L: (a) FR-4 core substrate, (b) circuitize 1st Cu layer, (c) laminate 1st dielectric layer, (d) photo-define 1st vias, (e) Plate vias and circuitize 2nd Cu layer, (f) laminate 2nd dielectric layer, (g) photo-define 2nd vias, (h) Plate vias and circuitize 3rd Cu layer.

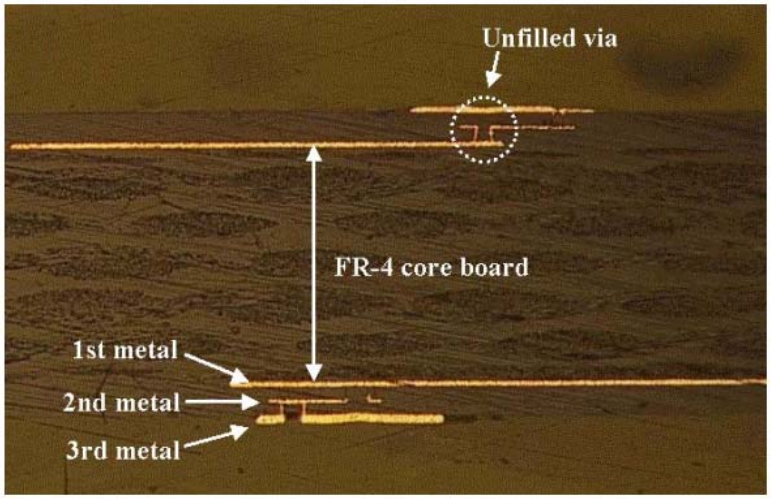


Figure 4.8 Cross section of a MCM-L package.

4.3.2 Experimental Result of High-Q Inductor Realization in a MCM-L Organic Package

A high-Q inductor is implemented in a MCM-L package using wiring metal layers, which is called a MCM-L inductor. The loss tangent and dielectric constant of the core substrate are 0.009 and 3.7, respectively. The inter-dielectric material has a loss tangent of 0.026, and a dielectric constant of 3.2, and a thickness of 80 μm. The inductor layer is designed in the second metal layer and the hollow ground plane in the third metal layer. The conductivity of the Cu metal is 5×10^7 S/m. The width of the inductor layer is 100 μm, and the outer diameter is 700 μm. Because of the thick inter-dielectric organic material and thick Cu metallization, an embedded MCM-L inductor shows high-Q. Figure 4.9 shows the top view of the MCM-L inductor. The inductance is 1.8 nH, and the maximum Q-factor is around 60 at 2.5 GHz as shown in Figure 4.10. The model in Figure 4.11 is used for inductor modeling, and the model parameters are listed in Table 4.2.

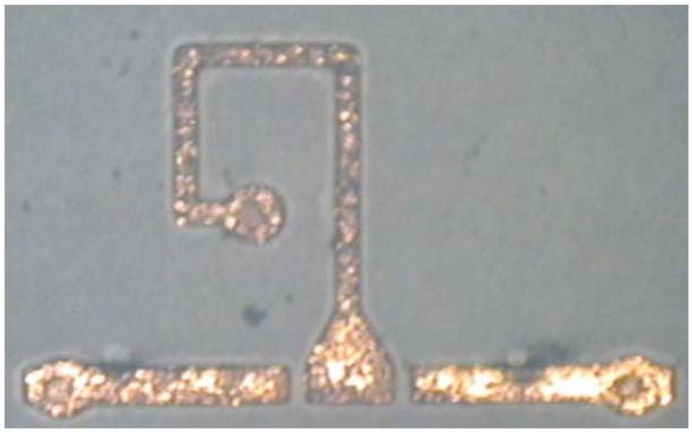


Figure 4.9 Top view of the implemented MCM-L inductor.

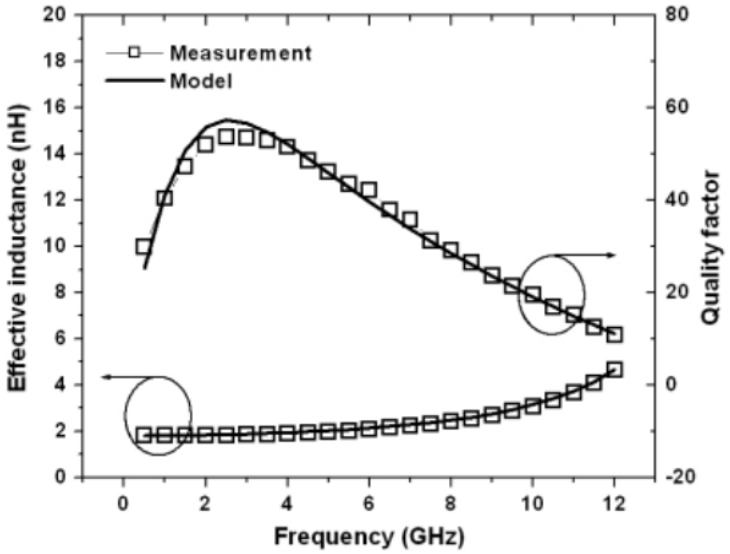


Figure 4.10 Measurement and model data of the implemented MCM-L inductor.

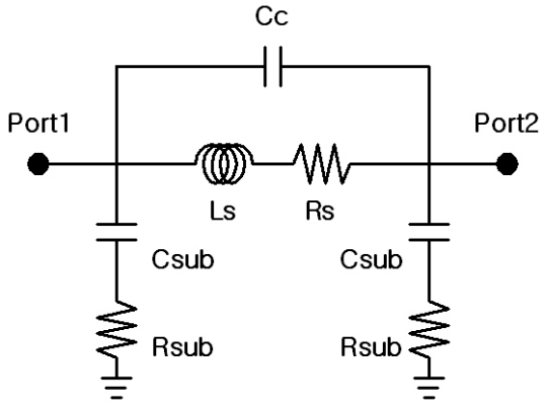


Figure 4.11 Model for the implemented MCM-L inductor.

Table 4.2 Model parameters of the implemented MCM-L inductor.

Turns	Ls (nH)	Rs (Ω)	Csub (pF)	Rsub (Ω)	Cc (pF)
1.25	1.8	$0.25\sqrt{f}$	0.02	4500	0.06

4.4 WAFER-LEVEL PACKAGE

A Wafer-level package (WLP) is an IC package formed at the wafer level on the wafer. A conventional IC packaging proceeds by the following steps: wafer fabrication, dicing into ICs, Individual IC assembly into packaging. However, in this new WLP process, front-end IC fabrication and back-end IC assembly can be performed at the wafer foundry simultaneously. The basic concept is to take the wafer immediately after fabrication, form IC connections with a few more process steps, perform testing, and singulate into packaged ICs.

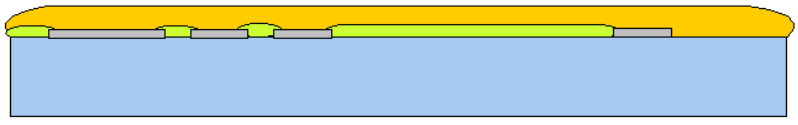
A WLP is expected to provide a number of benefits. It provides the smallest system size, because it is a chip size package. It reduces cost of packaging and testing, because all the connections and testing are done at wafer level. There is no under-fill because of compliancy of the leads or other ways to achieve reliability. Furthermore, the short lead length improves electrical performance. The two most important factors driving the WLP are size benefits for portable products and cost benefits for all products.

WLP does have few drawbacks. Since the interconnection must be located in the active area of the die, very high I/O ICs would require very small solder balls with fine pitch or large die size, which weakens the benefits of a WLP. Although it is technically feasible to manufacture such small solder balls, they would require very high density

PWB to interconnect. With WLP, all of the ICs are packaged at wafer level. This results in defective ICs being packaged.

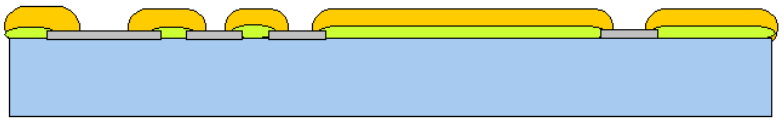
The overall process of a WLP is illustrated in Figure 4. 12. This process incorporate two passivation layers and one redistribution metal layer. Figure 4.12 (a) is the wafer after fabrication. The on-chip pads are opened to be connected with redistribution metal layer. First, the wafer is deposited by the passivation layer, Polybenzoxazole (PBO) (Figure 4.12 (b)), and the pasivation opening is performed for interconnection (Figure 4.12 (c)). Then redistribution metal layer is plated with Cu (Figure 4.12 (d)). To simplify the WLP, only one metal layer is incorporated, so that the via interconnection, inductor layer, and solder ball pads are designed using same metal layer. Another passivation layer is deposited and opened (Figure 4.12 (e) and (f)). The last process step is solder ball attaching (Figure 4.12 (g)).

(a)

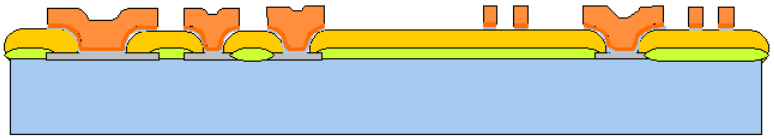


(b)

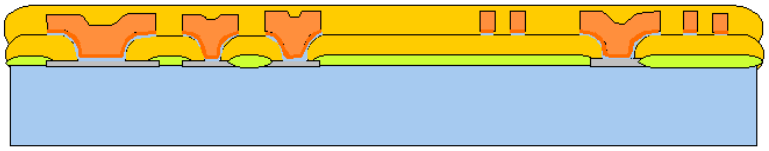
Figure 4.12 Process flow of a WLP: (a) wafer after fabrication, (b) deposit 1st passivation layer, (c) 1st passivation layer opening, (d) Cu plating of redistribution metal layer, (e) deposit 2nd passivation layer, (f) 2nd passivation layer opening, (g) solder ball attaching.



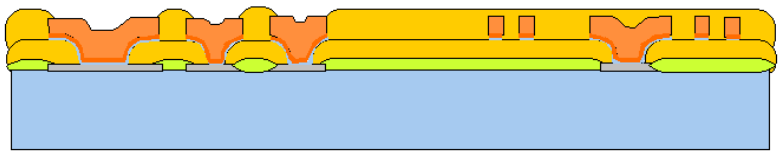
(c)



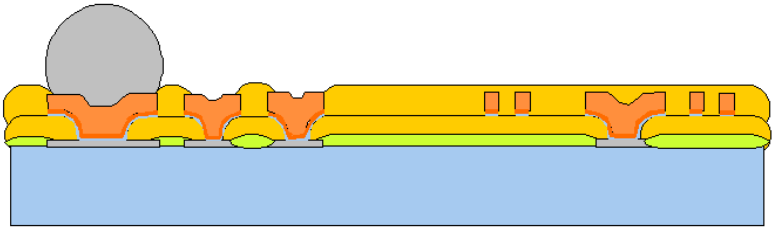
(d)



(e)



(f)



(g)

Figure 4.12 (continued) Process flow of a WLP: (a) wafer after fabrication, (b) deposit 1st passivation layer, (c) 1st passivation layer opening, (d) Cu plating of redistribution metal layer, (e) deposit 2nd passivation layer, (f) 2nd passivation layer opening, (g) solder ball attaching.

4.4.1 Experimental Results of High-Q Inductor Realization in a WLP

A high-Q inductor is implemented in a WLP using redistribution metal layers, which is called a WLP inductor. The top view and the cross-section view are shown in Figure 4.13 and Figure 4.14. The inductor is designed above the VCO circuit to save the die size. The loss tangent and dielectric constant of PBO are 0.01 and 2.9, respectively. Two passivation layers are designed with different thickness as shown in Figure 4.16. The first one is 12 μm, and the second is 5 μm. Since the thickness of the first passivation layer affect the substrate parasitics, it is designed thicker than the second. The thickness of the Cu plating is 9.5 μm. The width and spacing of the inductor layer are designed as 25 μm, the minimum feature size. The WLP inductor is connected to the VCO circuit through the pads on the chip. Hence, the pad's parasitics become a part of the WLP inductor. The size of the on-chip pad is designed as 80 μm. The inductance is 2 nH, and the maximum Q-factor is around 9 at 1.5 GHz as shown in Figure 4.17. The model in Figure 4.18 is used for inductor modeling, and the model parameters are listed in Table 4.3. The on-chip pads for the interconnection are included in the inductor model. Those are modeled by Rpad and Cpad.

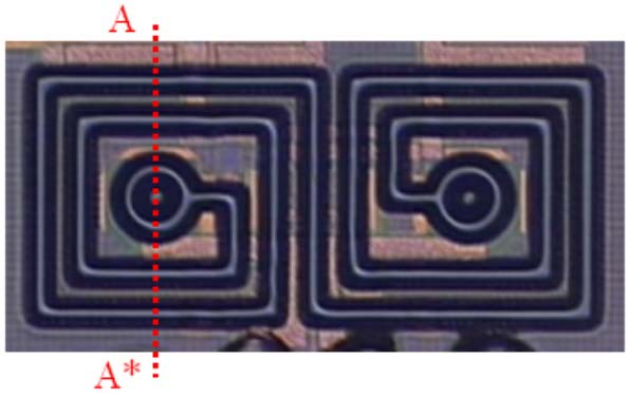


Figure 4.13 Top view of the implemented WLP inductor.

Figure 4.14 Cross section of the implemented WLP from A to A* in Figure 4.13.

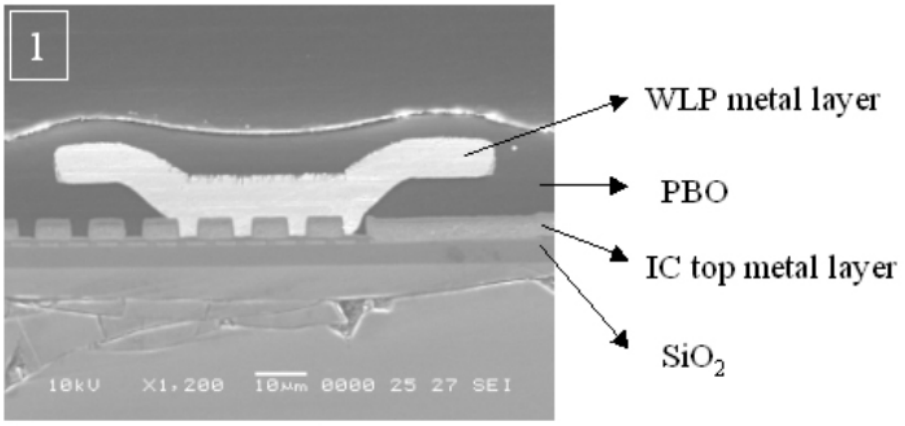


Figure 4.15 Cross section of via-hole for the interconnection between the WLP and the VCO circuitry.

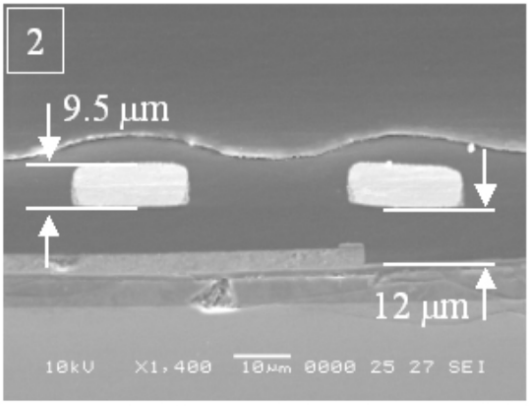


Figure 4.16 Cross section of the inductor layer.

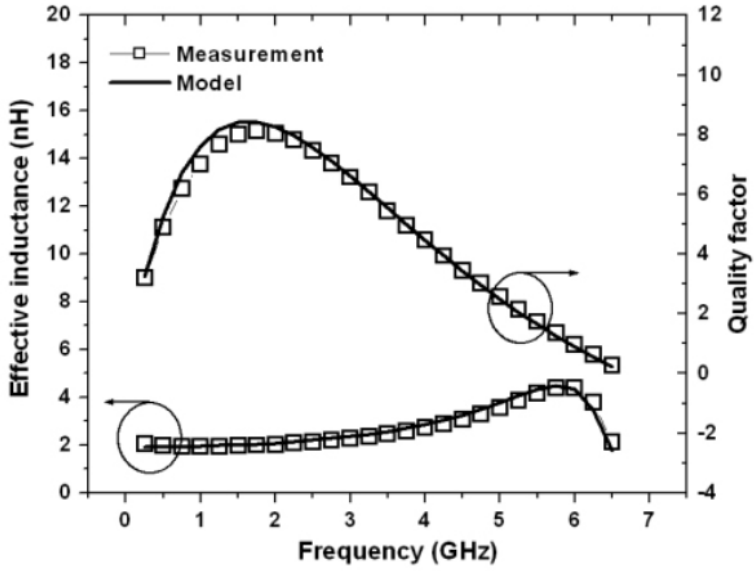


Figure 4.17 Measurement and model data of the implemented MCM-L inductor.

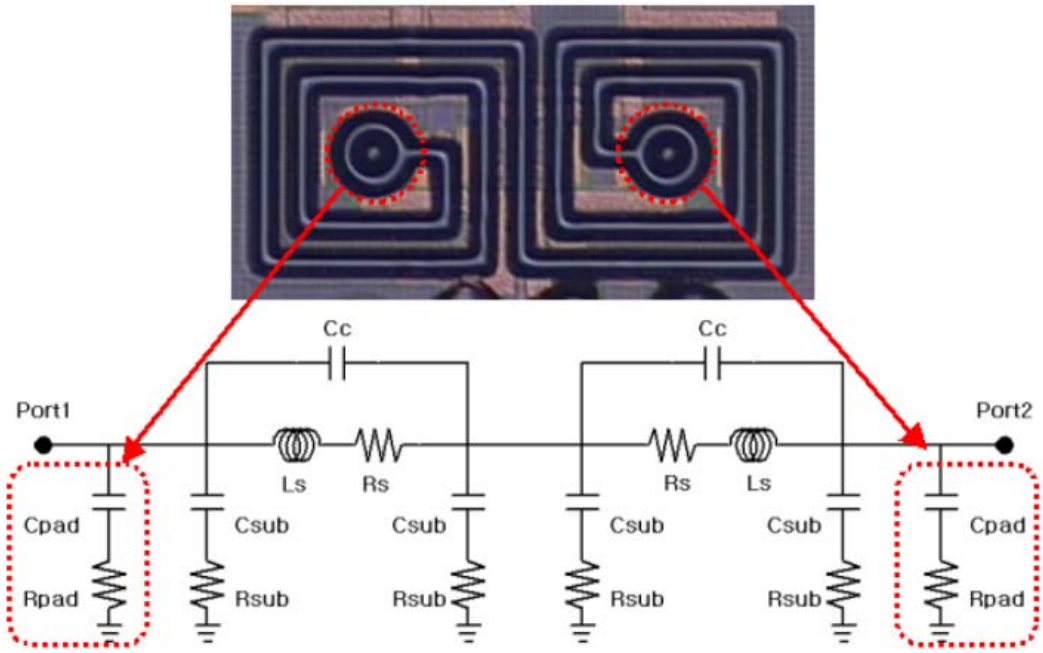


Figure 4.18 Model for the implemented WLP inductor.

Table 4.3 Model parameters of the implemented WLP inductor.

Turns	Ls (nH)	Rs (Ω)	Csub (pF)	Rsub (Ω)	Cpad (pF)	Rpad (Ω)	Cc (pF)
4	1	$0.727\sqrt{f}$	0.35	1200	0.15	30	0.3

CHAPTER V

HIGH PERFORMANCE LC-TANK CMOS VCO IMPLEMENTATION FOR A SI-BASED SINGLE-CHIP PACKAGE APPROACH

In order to satisfy the increasing demands of customers, modern electronic wireless products must not only be smaller and less expensive, they also must have high performance. A Si-based single-chip radio offers an opportunity to satisfy these demands on size and cost, but it falls short in delivering high performance. This is because such radios have poor quality inductors. High-Q inductors are essential in RF circuits to meet the stringent RF specifications. Therefore, great effort has been made to develop a high-Q inductor, as described in Chapter three. In this dissertation, the shortcoming in performance is surmounted through a Si-based single-chip package radio solution that also confers size and cost benefits.

In Chapter four, high-Q inductor schemes using advanced packaging technologies such as FBGA, MCM-L, and WLP were shown. These high-Q inductor schemes enable a Si-based single-chip package solution to achieve high performance. A VCO needs low loss LC-tank resonators in order for it to have low phase noise, low power consumption, and a wide tuning range, which depends on the Q-factor of an inductor in the resonator.

In this dissertation, LC-tank VCOs in 0.35μm CMOS technology, in which the inductor is implemented using the wiring metal layer in packages (FBGA and WLP), are presented.

The LC-tank CMOS VCO using an on-chip inductor (on-chip VCO) is also implemented as a reference design. The critical specifications such as phase noise, power consumption, and frequency tuning range of the on-chip VCO are compared to those of VCOs using an embedded inductor in packages. Furthermore, a VCO design optimized from the perspective of a high-Q inductor is presented.

5.1 CHIP-TO-PACKAGE INTERCONNECTION EFFECT ON EMBEDDED INDUCTORS

The inductor embedded in a package should be connected through the pads on the chip. Therefore, the parasitics from pads are directly connected to the resonator node, so that the effects should be investigated. The pads parasitics can be modeled with the capacitance and resistance. By including the parasitics of the pad, the Q-factor of the embedded inductor is decreased.

5.1.1 WLP Inductor

The WLP inductor is implemented above the VCO circuitry not only to save die size but also to shorten as much as possible the interconnection with the VCO. Therefore, the WLP inductor and the VCO circuit should be co-designed simultaneously. The inductor is connected to the VCO resonator through a via-hole, as illustrated in Figure 4.12. The landing pad for the via-hole has the substrate parasitics, and can be modeled by *Rpad* and *Cpad* as shown in Figure 5.1. The larger the pad, the larger the parasitics. Figure 5.2 shows the dependency of the size of a via-pad on the parasitic values. The diameter of the via-pad used for the fabrication is 80 μm. The values of the extracted model parameters,

Rpad and *Cpad*, are 30 Ω, and 0.15 pF, respectively. The parasitics degrade the Q-factor of the WLP inductor, as shown in Figure 5.3. Hence, the micro-via is required to avoid degradation of the Q-factor of the WLP inductor. In Figure 5.3, the via-pad parasitics have less effect on the Q-factor of the WLP inductor below 2 GHz because in this frequency range series resistance is more dominant than the substrate parasitics. The VCOs in this dissertation are designed to operate at a frequency of 2 GHz so as to be less affected by the via-pads.

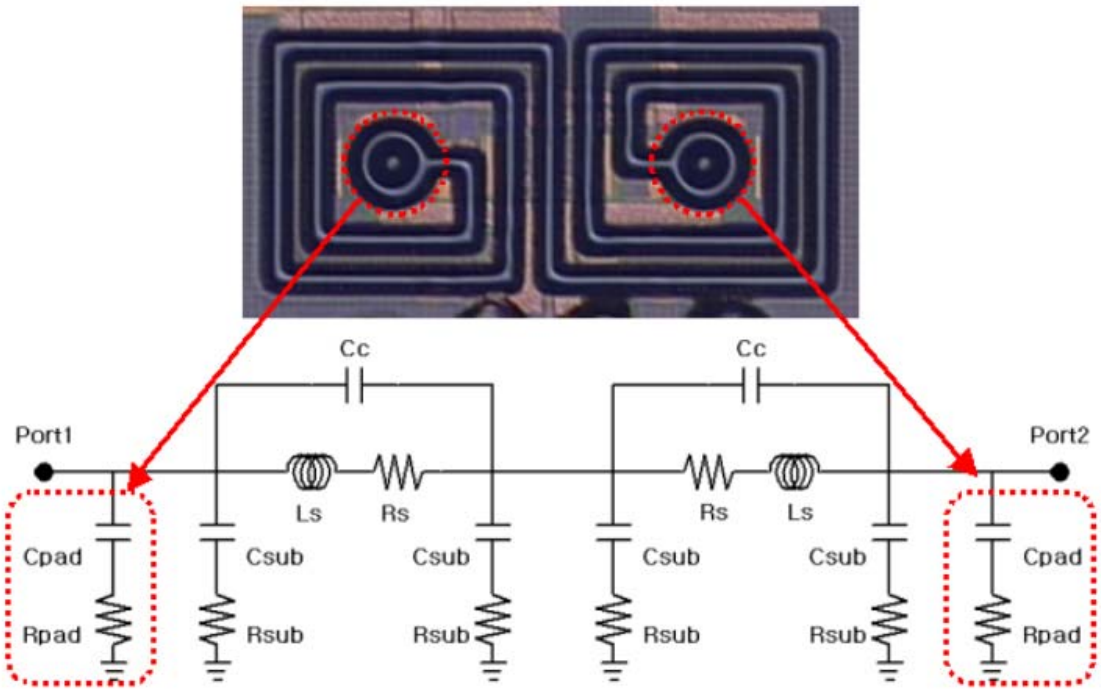


Figure 5.1 WLP inductor model including the via-pad parasitics.

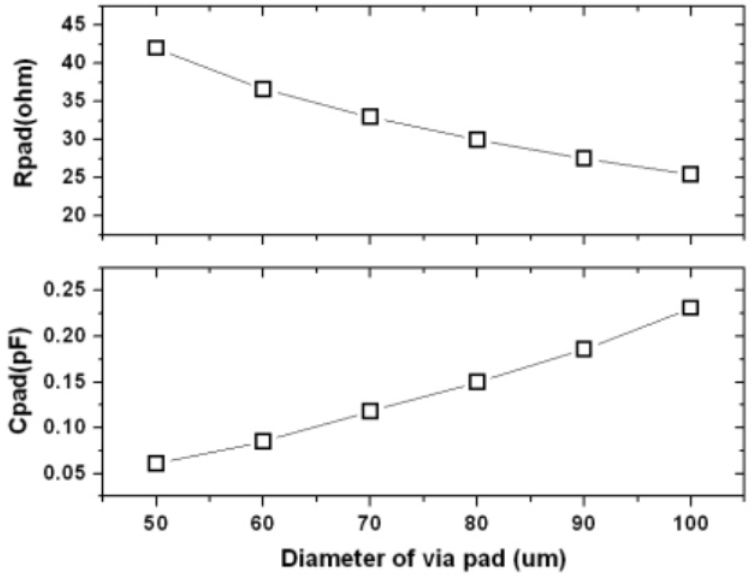


Figure 5.2 Model parameter values of via-pad versus a diameter.

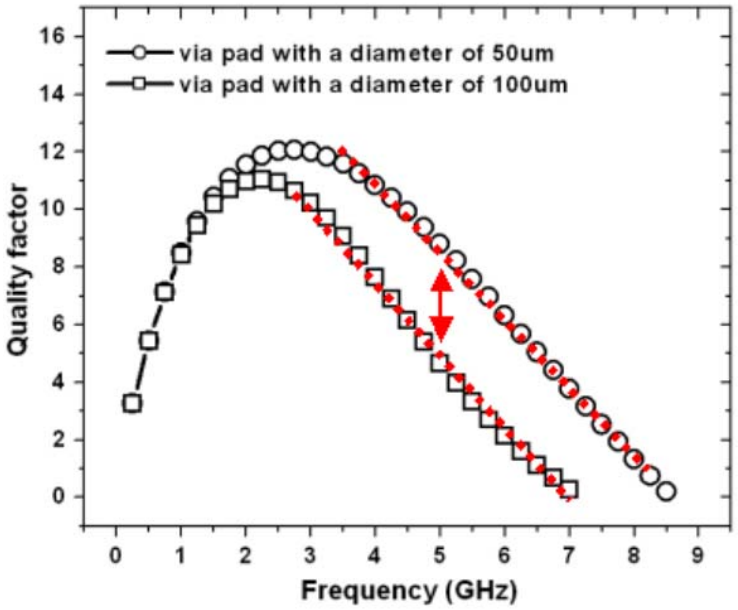


Figure 5.3 Q-factors of the WLP inductors with different diameters of a via-pad.

5.1.2 FBGA Inductor

The interconnection between the FBGA inductor and the VCO circuit is realized through the bond wire, as shown in Figure 5.4. Therefore, the bond wires and bonding pads are the part of the inductor for the resonator so that those can be modeled with *Rw*, *Lw*, *Rpad*, and *Cpad*, as depicted in Figure 5.4. As in the case of the via-pads for the WLP inductor, the diameter of the bonding pads is 80 μm. Considering the length and quality of the wire-bond, *Rw* and *Lw* are modeled by 0.05 Ω and 0.2 nH, respectively. The degradation of the Q-factor is illustrated in Figure 5.5.

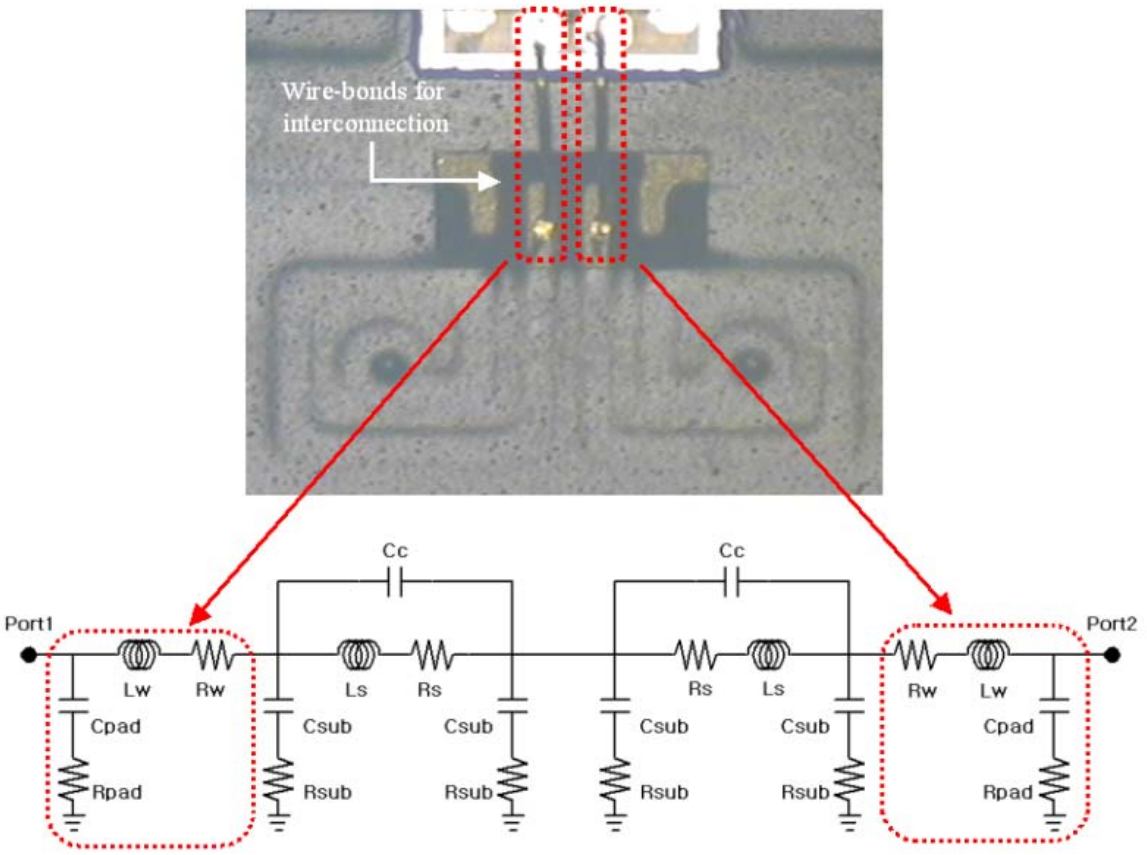


Figure 5.4 FBGA inductor model including the parasitics of bond wires and bonding pads.

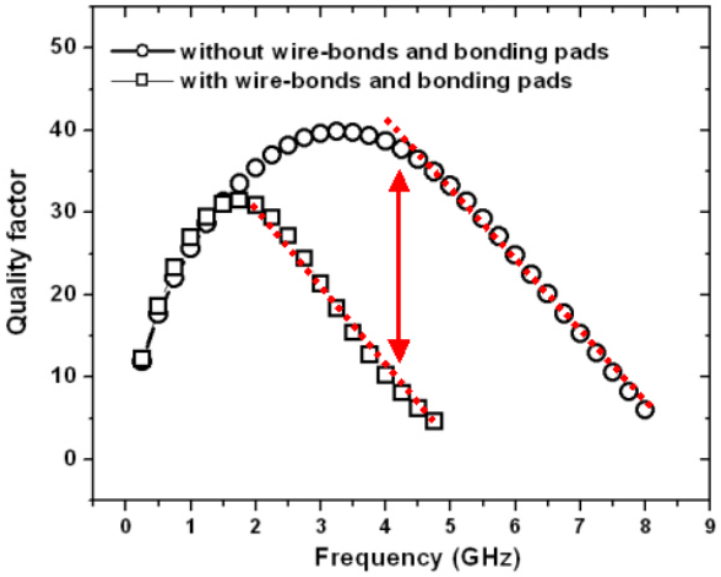


Figure 5.5 Q-factors of the FBGA inductors including the parasitics of bond wires and bonding pads.

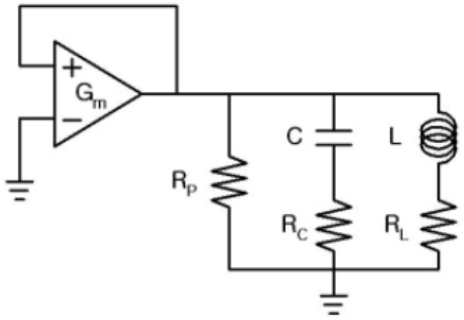
5.2 Effects of High-Q Inductor on VCO Performance

A high-Q inductor is required to implement a high performance LC-tank VCO, especially in the Si-based process. In this section, the effects of the high-Q inductor on the VCO performance are discussed. The high-Q inductor provides not only low phase noise but also low power consumption and a wide frequency tuning range.

5.2.1 Phase Noise Perspective

It already has been described in Chapter two that the phase noise of an LC-tank VCO depends more on the quality of the tank than anything else. The phase noise of a Si-based LC-tank VCO with the integrated on-chip inductor is especially limited by the Q-factor of the inductor. This is one of the bottlenecks to achieving a Si-based single-chip radio.

Here, we focus on the resonator and analyze what factor limits phase noise. This analysis uses the model published by J. Craninckx in 1995, as shown in Figure 5.6.

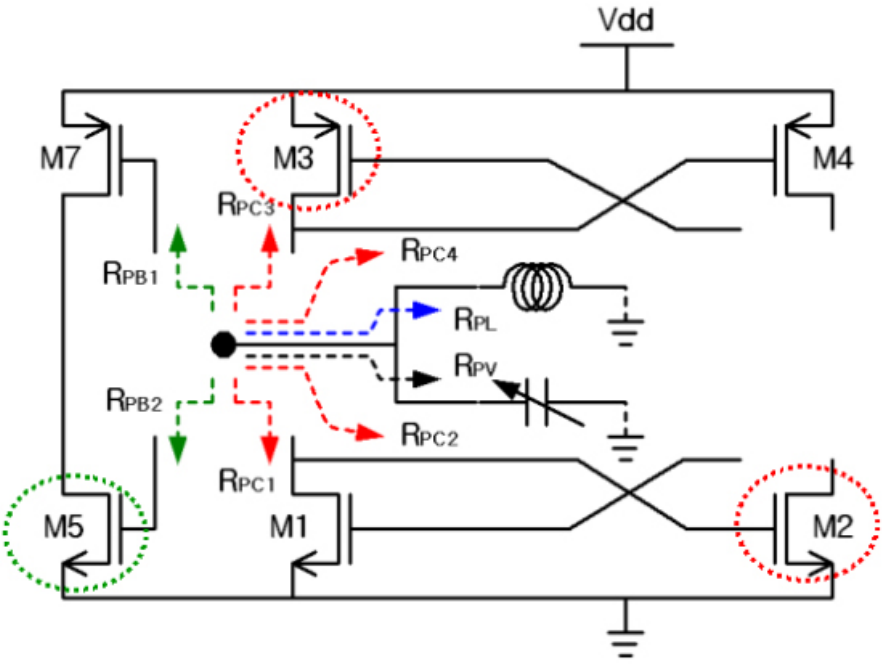


$$L(\Delta\omega) = 10 \cdot \log\left[\frac{kT(1+A)\cdot R_{eff}\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2}{\frac{1}{2}\cdot V_0^2}\right]$$

$$R_{eff} = R_L + R_C + \frac{1}{R_P(C\cdot\omega_0)^2}$$

Figure 5.6 Phase noise model by J. Craninckx.

The conceptual schematic of an LC-tank oscillator is depicted in Figure 5.6. The schematic consists of the ideal positive feedback amplifier with a gain of G_m and the LC resonator with the ideal L, C components and lossy components represented by R_L, R_C, and R_P. In the phase noise expression, $L(\Delta\omega)$, the resonator loss is described as the effective resistance, R_{eff}, which is made up of three resistive components R_L, R_C, and R_P. Therefore, the phase noise analysis from a resonator perspective can be performed through three resistances. The VCO topology incorporated in this thesis is depicted in Figure 5.7. The series resistances of the inductor and the varactor (R_L and R_C) are obvious and the equivalent parallel resistance (R_P) can be expressed by four resistive impedances R_{PL}, R_{PV}, R_{PC}, and R_{PB} in parallel.



$$R_{eff} = R_L + R_C + \frac{1}{R_p (C \cdot \omega_0)^2}$$

$$R_P = R_{PL} // R_{PV} // R_{PC} // R_{PB}$$

$$R_{PB} = R_{PB1} // R_{PB2}$$

$$R_{PC} = R_{PC1} // R_{PC2} // R_{PC3} // R_{PC4}$$

Figure 5.7 Effective resistance of the actual LC-tank VCO topology.

Because of the switching characteristics of the differential pair, the active devices, M2, M3, and M5, are turned on at the same time as M1, M4, and M7 are turned off. The impedances toward the turned-off devices (R_{PC1}, R_{PC4}, R_{PB1}) are very high. The impedance toward the buffer stage (R_{PB2}) is also very high because of its small size. The

parallel substrate parasitics of the varactor are high because the control voltage is applied to the source/drain terminal, which is susceptible to substrate parasitics. Even, R_{PC2} and R_{PC3} are lower than R_{PL} with the active device sizes of the 2GHz VCO in this thesis. Therefore, the total equivalent parallel parasitic resistance, R_P, mainly depends on R_{PC2} and R_{PC3}.

The main loss factor in the LC-tank for phase noise is investigated by calculation using R_{eff}, as shown in Table 5.1. Three different inductor technologies are incorporated in the comparison. For the on-chip inductor, the series resistance (R_L) is the main factor for R_{eff}. However, when the series resistance goes lower below 1 Ω, the third term, $1/R_P(C\cdot\omega_0)^2$, becomes dominant. Therefore, even though the Q-factor of the FBGA inductor is three times higher than that of the WLP inductor because of the lower series resistance and higher parallel resistance, phase noise improved by only 1.4 dB which is actually in the measurement error range. Based on this analysis, when the Q-factor of the inductor is more than 10 at 2 GHz, $R_{PC2} // R_{PC3}$ is the dominant factor for phase noise in terms of the LC-tank loss. To achieve higher $R_{PC2} // R_{PC3}$, the CMOS technology with a smaller gate length is required. 0.13 μm, 0.18 μm, 0.25 μm CMOS may provide the same gain with smaller device sizes and result in high impedances. Therefore, when the series resistance of the inductor is less than 1 Ω, the limiting factor for the phase noise of a 2 GHz VCO is no longer inductor loss but the active device's impedances.

Table 5.1 Comparison of three inductor technologies on phase noise contribution.

Inductor	Si on-chip	WLP	FBGA
Q @ 2GHz	3	10	30
$R_L\,(\Omega)$	**6**	**1**	**0.4**
$R_C\,(\Omega)$	0.4	0.4	0.4
$R_{PL}\,(\Omega)$	**1.1k**	**1.3k**	**4k**
$R_P\,(\Omega)$	200	210	235
$\frac{1}{R_P(C\cdot\omega_0)^2}$	**1.7**	**1.6**	**1.4**
$R_{eff}\,(\Omega)$	**8.1**	**3**	**2.2**
V_o	v	1.5 v	1.5 v
Phase noise (dBc/Hz)	$PN_{on\text{-}chip}$	$PN_{on\text{-}chip}$ – ***6 dB***	$PN_{on\text{-}chip}$ – ***7.4 dB***

5.2.2 Power Consumption Perspective

When the high-Q inductor is used in the LC-tank, less feedback gain may be required to guarantee oscillation. Feedback gain depends on the amount of current flowing and on the size of the device. Because the VCO topology in this thesis does not include the tail bias circuitry for low power consumption and low phase noise, the bias current is under the control of the supply voltage for any given device size. As the Q-factor of the inductor increase, the supply voltage can decrease. Consequently, low power consumption and low phase noise can be obtained simultaneously. These effects are simulated by increasing the thickness of the inductor metal layer from 1 to 5 μm. For

simulation purposes, the substrate parasitic values are fixed and only the thickness of the inductor metal layer is increased. The Q-factor of the inductor at 2GHz is proportional to the metal thickness because the Q-factor at the frequency mainly depends on the series resistance of the layer. When the Q-factor increases from 2.5 to 13, the minimum power consumption for the VCO decreases from 7.2 mW to 3 mW, as shown in Figure 5.8. The phase noise improvement is simulated with the harmonic balance simulation in ADS. Even though the VCO consumes less power, the phase noise decreases because of the reduction of series resistance, as shown in Figure 5.9. When the Q-factor is more than 10, the improvement of phase noise starts to saturate, as mentioned in the previous section.

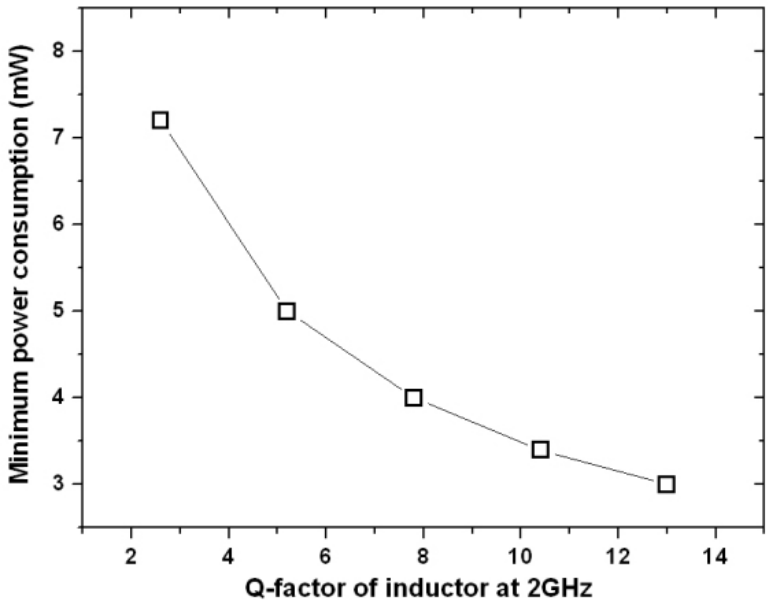


Figure 5.8 Minimum power consumption versus the Q-factor of an inductor.

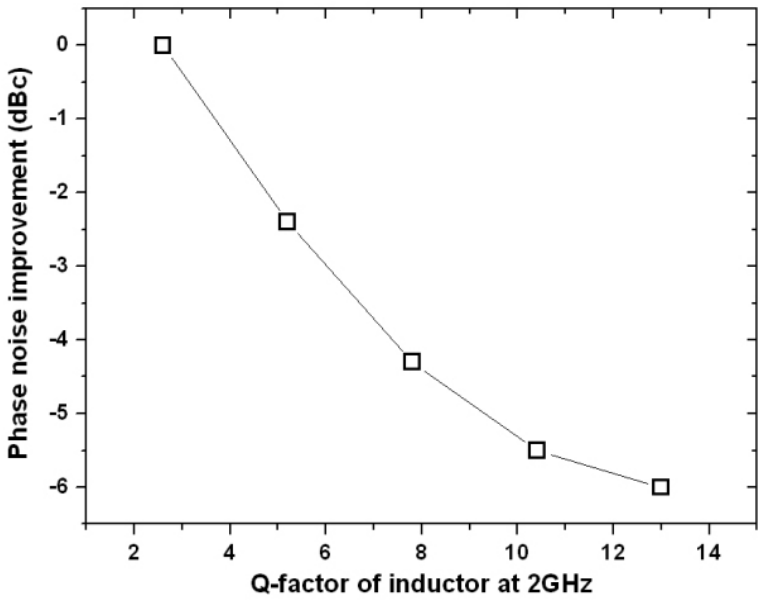


Figure 5.9 Phase noise improvement versus the Q-factor of an inductor.

5.2.3 Tuning Range Perspective

The Q-factor of the inductor affects the frequency tuning range of a VCO. To understand this effect on frequency tuning, another definition of Q needs to be considered. In Figure 5.10, the circuit is considered as a feedback system and the phase of the open-loop transfer function, $\phi(\omega)$, is examined at resonance. The Q is then defined as [46]

$$Q = \frac{\omega_0}{2}\left|\frac{d\phi(\omega)}{d\omega}\right|. \tag{5.1}$$

This is called the open-loop Q. The higher Q is, the steeper the phase slope is. It is a measure of how much the closed-loop system opposes variation in the frequency of oscillation. Therefore, a high-Q inductor reduces the tuning range. This is shown in the simulation results in Figure 5.11. In the simulation, as in the case of the previous section,

only the thickness of the inductor metal layer is increased to obtain the high Q-factor. When the Q-factor increases from 2.5 to 13, the tuning range of the VCO decreases by an amount ranging from 15.5 % to 19 %, as shown in Figure 5.11.

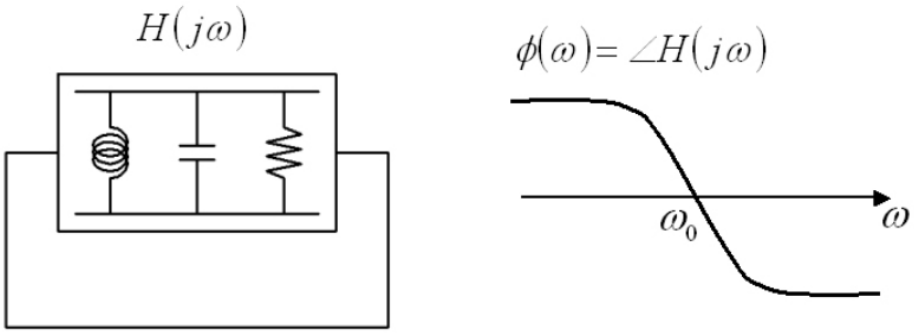


Figure 5.10 Definition of Q-factor based on open-loop phase slope.

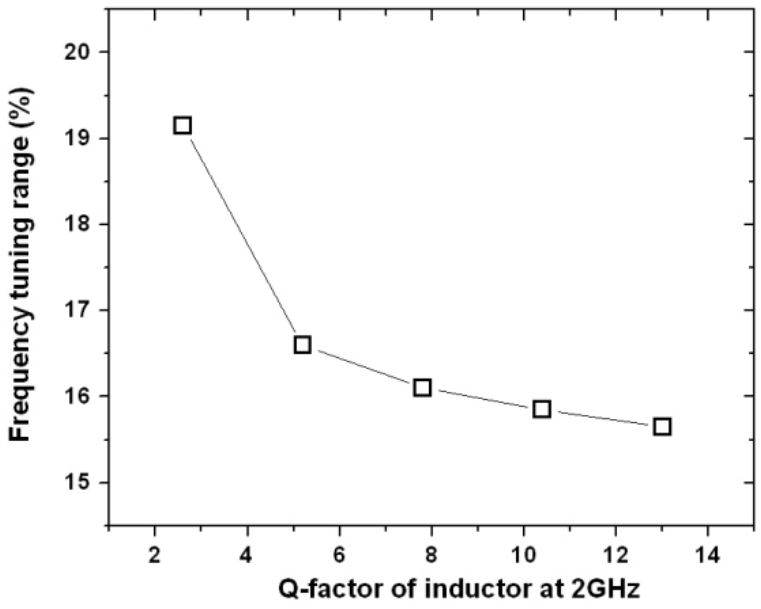


Figure 5.11 Frequency tuning range versus the Q-factor of the inductor.

5.3 EXPERIMENTAL RESULTS OF LC-TANK CMOS VCO USING ON-CHIP INDUCTOR

The schematic of the LC-tank CMOS VCO is shown in Figure 5.12. The differential topology with both NMOS and PMOS cross-coupled pairs was chosen because of its several advantages. Compared to the differential configurations using only a single cross-coupled pair (NMOS core or PMOS core), the dual cross-coupled pair helps to generate a symmetric oscillation waveform at the resonator node. This ensures equal rising and falling time of the oscillation waveform, which helps to suppress the flicker noise up-conversion. The bias circuitry for the tail current was removed not only for low power consumption but also for low phase-noise.

The negative resistance provided by the cross-coupled NMOS (M1, M2) and PMOS (M3, M4) is given by

$$R_{negaitve} = \frac{-2}{g_m} = \frac{-2}{g_{m12} + g_{m34}}$$

In order to achieve symmetry in the oscillation waveform, the NMOS and PMOS devices are designed to be $g_{m12} = g_{m34}$. A buffer stage is designed using simple inverters (M5-M7 and M6-M8) to isolate the resonator node from other circuitry. The inductors, L1 and L2, are designed to have a total inductance value of 3nH in a symmetric configuration. A frequency tuning is achieved by the accumulation-mode MOS varactors (Cvar1 and Cvar2). The gate terminals of the varactors are connected to the resonator node, and the control voltage (Vcon) is biased to the source/drain terminal because the substrate parasitic at the source/drain terminal is detrimental to the resonator-Q. Vcon is changed up to the supply voltage. The schematic in Figure 5.12 is used for all the VCO designs in

this thesis. For design optimization for high-Q inductor characteristic, only the supply voltage and device sizes of NMOS and PMOS are modified.

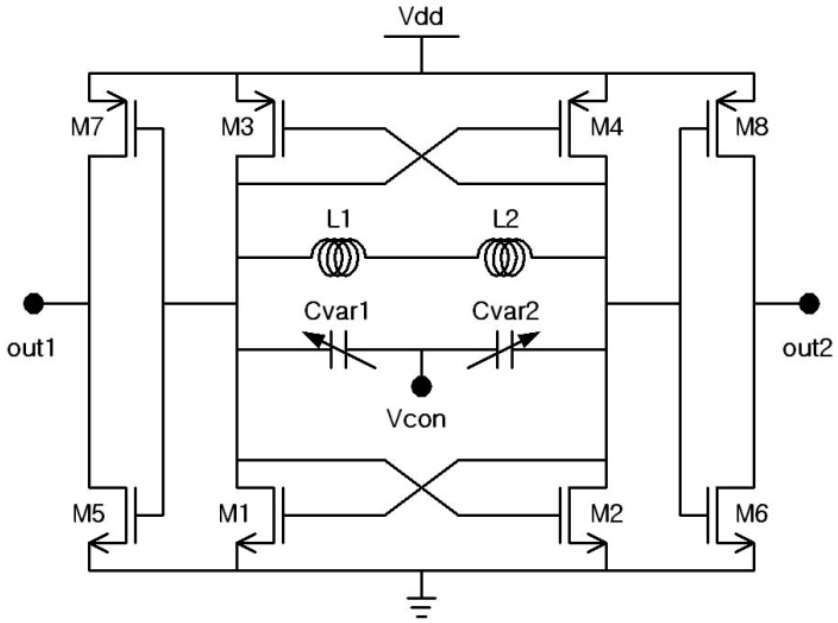


Figure 5.12 Schematic of the VCO.

The VCO design parameters such as the device sizes of active MOS devices and varactors, are listed in Table 5.2, and the photograph of the on-chip VCO is shown in Figure 5.13. The supply voltage chosen is 1.8 V. It is hard to go below a supply voltage of 1.8V because the knee voltage of active MOS device is around 0.9 V, which means at least 0.9 V is required to operate the MOS device in the saturation region. Operating active MOS devices in the triode region reduces not only the feedback gain but also the resonator-Q. With the given 0.35 μm CMOS process, the total width of NMOS and

PMOS for VCO core is chosen as 80 μm and 240 μm, respectively. These device sizes generate the same negative resistances from NMOS and PMOS core, thus making a symmetric rising- and falling- waveform.

Table 5.2 Design parameters of the on-chip VCO, WLP VCO1, and FBGA VCO.

	Devices	Design
VCO core	M1, M2	NMOS 0.35 μm × 10 μm × 8
	M3, M4	PMOS 0.35 μm × 10 μm × 24
Buffer	M5, M6	NMOS 0.35 μm × 10 μm × 2
	M7, M8	PMOS 0.35 μm × 10 μm × 6
Varactor	Cvar1, Cvar2	A-MOS 0.35 μm × 5 μm × 50 × 4

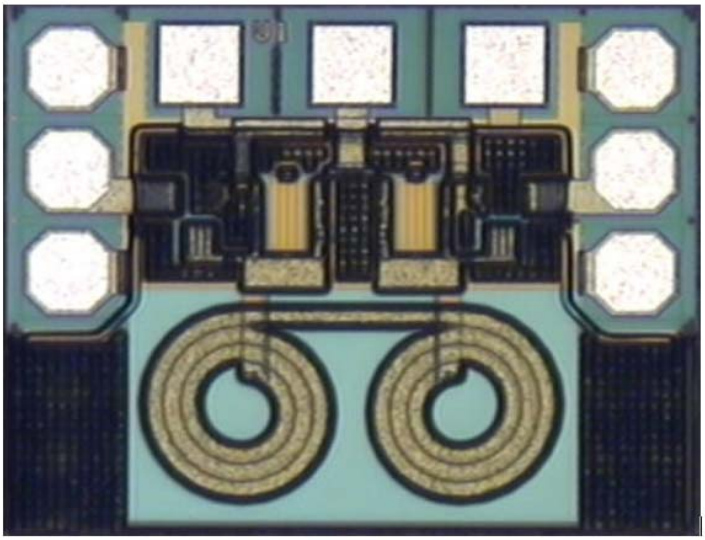


Figure 5.13 Photograph of the on-chip VCO.

The tail bias current source is not incorporated into the VCO topology, as depicted in Figure 5.12, for low power consumption and low phase noise as was mentioned earlier in Chapter two. In this case, the bias current can be changed by varying the supply voltage. Changing the bias current affects VCO performance. It affects not only power consumption, but also oscillation frequency, tuning range, and phase noise. The higher supply voltage is, the more power consumption is. It is obvious. The oscillation frequency and tuning range are affected because of the parasitic capacitances between the gate and drain terminal of both the NMOS and the PMOS. With the increase of the supply voltage, the parasitic capacitances are increased. Therefore the oscillation frequency decreases as shown in Figure 5.14. The tuning range is also limited because the parasitic capacitances are connected in parallel with the LC-tank.

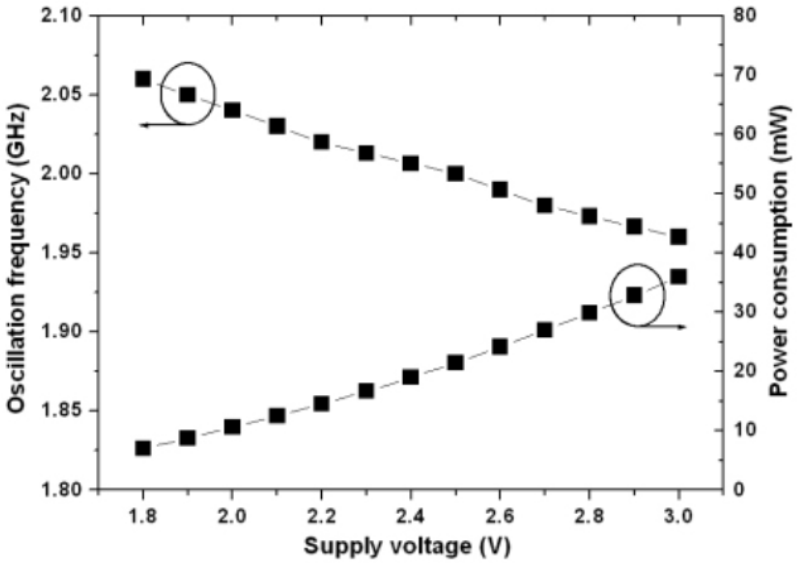


Figure 5.14 Power consumption and oscillation frequency versus the supply voltage.

Supply voltage affects the phase noise performance. As described in Chapter two, if the VCO is in the current-limited mode of operation, the phase noise reduces as the current increases because of the higher tank voltage amplitude that is engendered. In Figure 5.15, phase noise is diminishing until the supply voltage becomes 2.5 V, and then it starts to saturate. Thus, the current-limited mode of operation can be defined below 2.5 V. The best phase noise performance can be achieved with the supply voltage of 2.5 V. However, the power consumption and tuning range are sacrificed. Therefore, the device size and supply voltage need to be optimized for the VCO performance in terms of the resonator-Q.

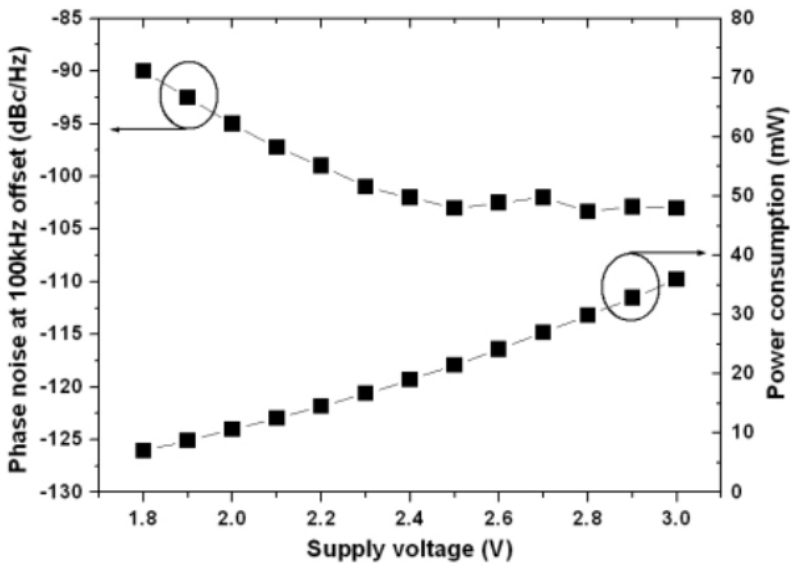


Figure 5.15 Power consumption and phase noise versus the supply voltage.

On-chip VCO performance is measured with a supply voltage of 1.8 V. The oscillation frequencies and output powers that occur with a variation of control voltage are shown in Figure 5.16. With the given device sizes listed in Table 5.2, the current flowing is 4 mA. Therefore, the total power consumption is 7.2 mW. The center frequency is 2.24 GHz. The tuning range is 317 MHz (14.2 %) with control voltage from 0 to 1.8 V. The output power is around –13.5 dBm with the variation of ±1 dBm. The overall spectrum of VCO up to 26.5 GHz at the control voltage of 0 V is shown in Figure 5.17. It is noted that no harmonics are seen in the spectrum, which is good for the performance of wireless systems. The phase noise performance is measured using offset frequencies from 10 kHz to 1 MHz. Figure 5.18 shows phase noise plot with a control voltage of 0 V. The phase noise is –85, -91.5, and -114 dBc/Hz at offset frequencies of 60, 100, and 600 kHz, respectively. The phase noise at the offset frequency of 600 kHz with a variation of the control voltage is shown in Figure 5.19. Minimum phase noise is shown occurring at the control voltage of 0 V. The notch point is shown in Figure 5.19 at 0.8 V where the varactor is zero biased.

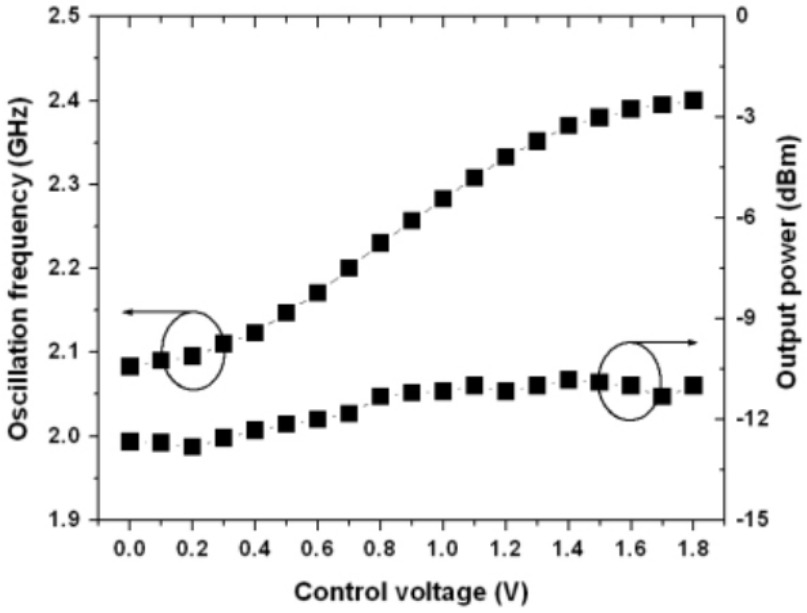


Figure 5.16 Oscillation frequencies and output powers versus the control voltage.

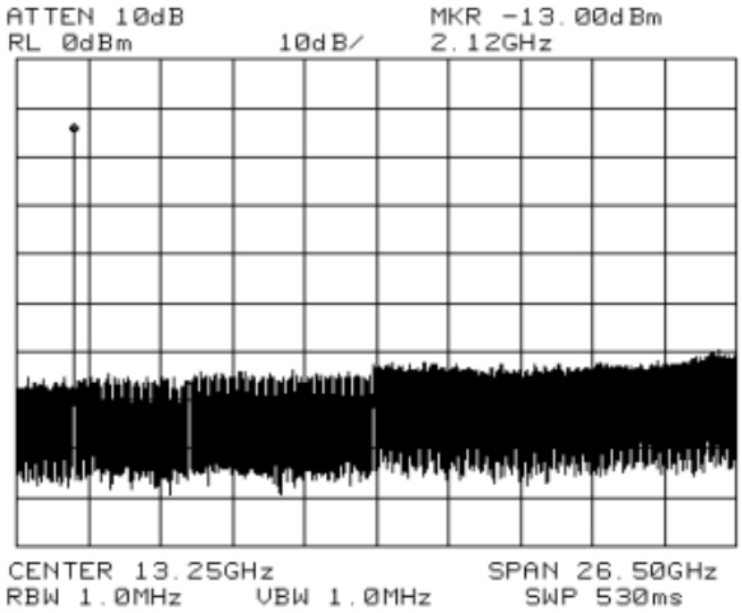


Figure 5.17 Overall spectrum of the VCO at the control voltage of 0 V.

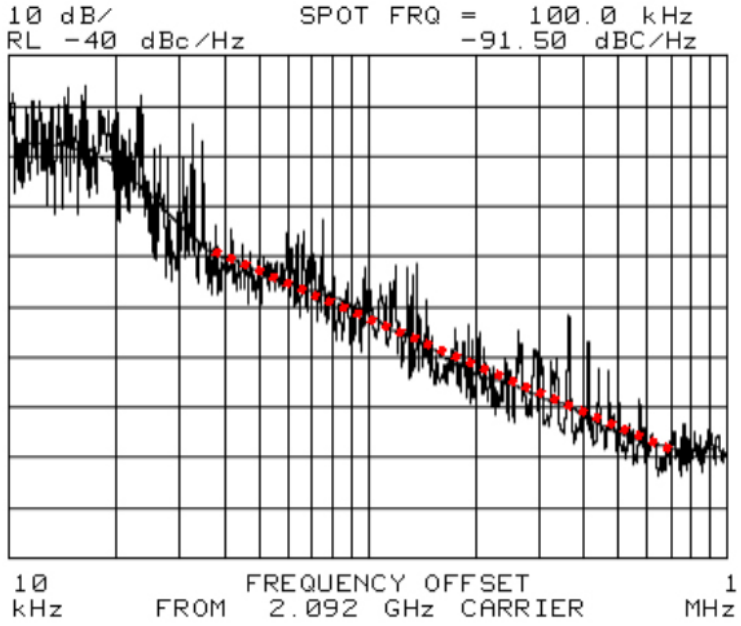


Figure 5.18 Phase noise plot at the control voltage of 0 V.

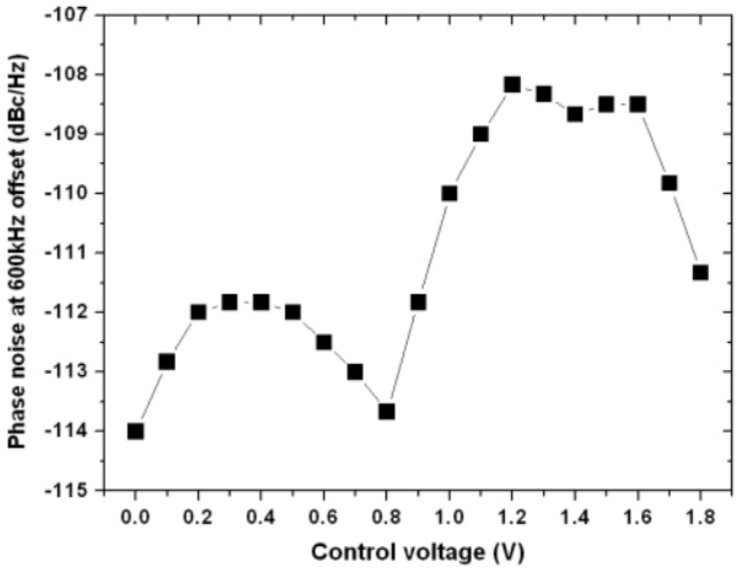


Figure 5.19 Phase noise at the offset frequency of 600 kHz versus the control voltage.

5.4. EXPERIMENTAL RESULTS OF LC-TANK CMOS VCO USING WLP INDUCTOR

The CMOS VCO with an LC-tank using an inductor created by the redistribution metal line of a WLP is implemented. The photograph is shown in Figure 5.20. The WLP inductor is implemented above the VCO circuitry to reduce the die size and the interconnection length between the WLP inductor and the VCO. The four solder ball pads at each corner are designed with a diameter of 200 μm. This VCO is designed with the same sizes of the active devices and varactors as listed in Table 5.2 (WLP VCO1). The Q-factor of the WLP inductor is 10 at 2GHz.

A supply voltage of 1.5 V is applied to operate the WLP VCO1. A current of 1.9 mA flows so that total dc power consumption is 2.9 mW. The power consumption of WLP VCO1 is reduced by 60 % compared to that of the on-chip VCO. The oscillation frequencies and output powers that occur when control voltage is varied are shown in Figure 5.21. The center frequency is 2.04 GHz. The tuning range is 253 MHz (12.4 %) with the control voltage from 0 to 1.5 V. The output power is around –14 dBm with the variation of ±0.5 dBm. The phase noise of the WLP VCO1 that occurs with variations in control voltage is shown and compared with that of the on-chip VCO in Figure 5.22. The phase noise of the WLP VCO1 is lower than that of the on-chip VCO by a minimum of 4 dB and a maximum 6 dB. The performance of the WLP VCO1 is listed and compared to that of the on-chip VCO in Table 5.3. While better phase noise and lower power consumption are obtained, the tuning range is reduced because of the high-Q characteristic of the WLP inductor.

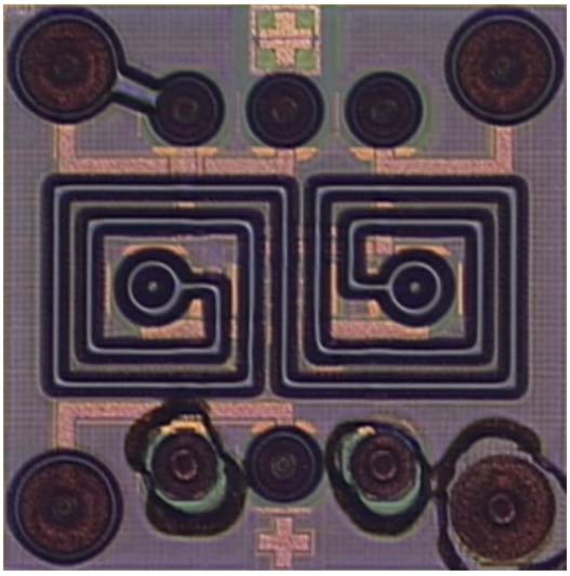


Figure 5.20 Photograph of the WLP VCO1.

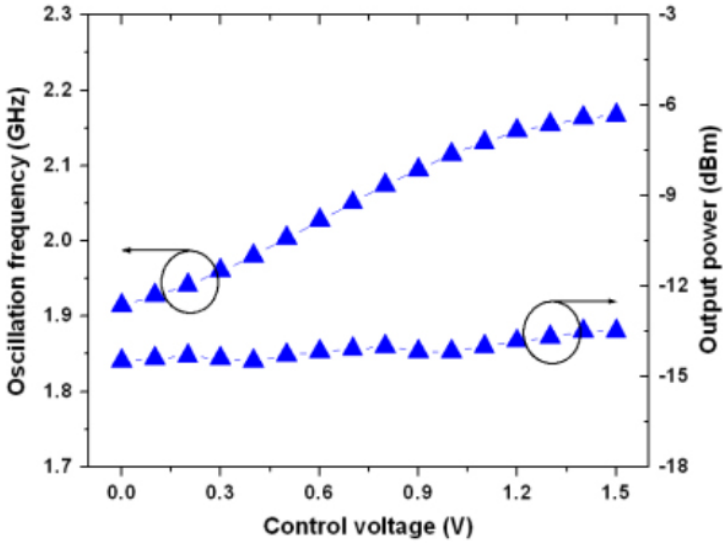


Figure 5.21 Oscillation frequencies and output powers versus the control voltage.

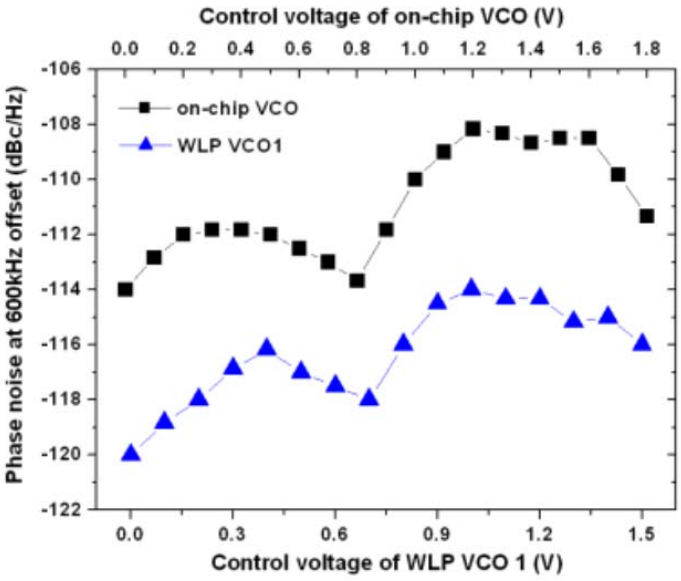


Figure 5.22 Phase noise of the WLP VCO1 and the on-chip VCO at the offset frequency of 600 kHz versus the control voltage.

Table 5.3 Performance comparison between the on-chip VCO and the WLP VCO1.

	On-chip VCO	WLP VCO1	Comparison
Power consumption	7.2 mW	2.9 mW	-60 %
Center frequency	2.24 GHz	2.04 GHz	-
Tuning range	317 MHz	253 MHz	-20 %
Output power	-13.5±1 dBm	-14±0.5 dBm	-
Phase noise	-108 ~ -114 dBc/Hz	-114 ~ -120 dBc/Hz	-4 ~ -6 dB
FOM_T	-185.2	-194.6	-9.4

5.5. EXPERIMENTAL RESULTS OF LC-TANK CMOS VCO USING FBGA INDUCTOR

The CMOS VCO with an LC-tank using the inductor realized by the wiring metal layer of a FBGA package is implemented (FBGA VCO). The photograph is shown in Figure 5.23. The inductor is implemented next to the VCO chip and connected with the VCO by the bond-wire. Thus, the bond-wire is the part of the inductor. Although the Q-factor of the bond-wire inductors is so high that it is no longer a relevant consideration, the bonding pads generate substrate parasitics and thereby greatly reduce the Q-factor at frequencies above 2 GHz, as illustrated in Figure 5.5. However, the FBGA VCO is designed at 2 GHz, so that the bonding pads have less effect on the VCO performance. The Q-factor of the FBGA inductor is around 30 at 2 GHz.

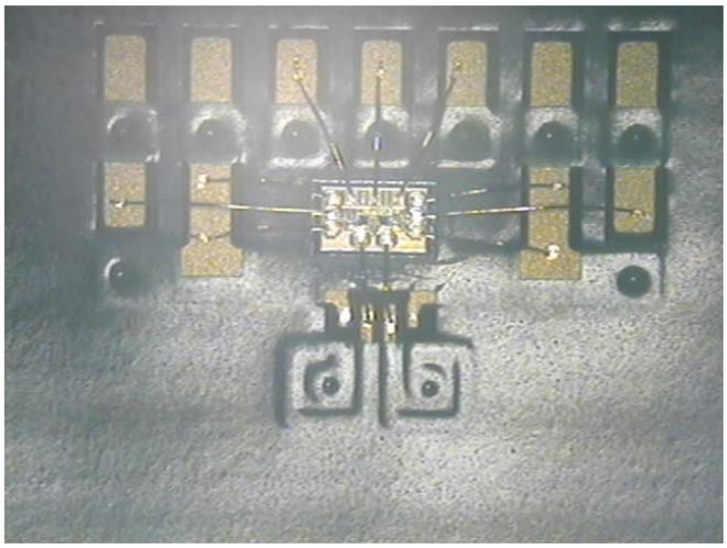


Figure 5.23 Photograph of the FBGA VCO.

This FBGA VCO is designed with the same sizes of active devices and varactors, as are listed in Table 5.2. Because the Q-factor of the FBGA inductor is higher than that of the WLP inductor, the dc power consumption is lower than WLP VCO1. A supply voltage of 1.4 V is applied to operate the FBGA VCO. The current of 1.64 mA flows, so that total dc power consumption is 2.3 mW. The power consumption of FBGA VCO is reduced by 21 % compared to that of the WLP VCO1. The oscillation frequencies and output powers that occur with variations of the control voltage are shown in Figure 5.24. The center frequency is 2.03 GHz. The tuning range is 260 MHz (12.8 %) with a control voltage of from 0 to 1.4 V. The output power is around –12.5 dBm with a variation of ±0.5 dBm.

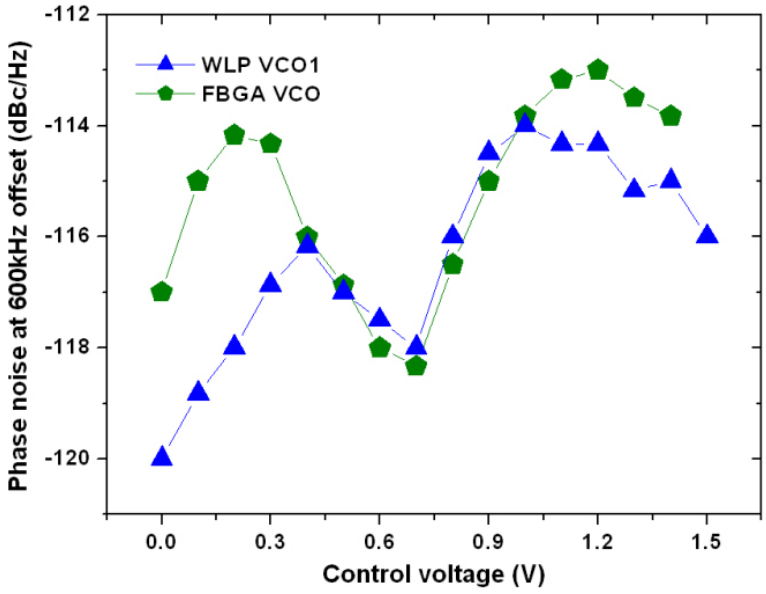


Figure 5.24 Oscillation frequency and output power versus the control voltage.

The phase noise of the FBGA VCO with the variation of the control voltage is shown in Figure 5.25 and compared with that of the WLP VCO1. According to the phase noise analysis in section 5.2, the FBGA VCO is expected to show 1.5 dB better phase noise than the WLP VCO1. However, the phase noise performances of both VCOs are almost the same within the control voltage range of between 0.4 V and 1.0 V. However, with control voltages of less than 0.3 V and more than 1.1 V, the phase noise of the FBGA VCO is worse than that of the WLP VCO1. This could happen because the bond-wires for the interconnection between the VCO and the FBGA inductor break the symmetry of the VCO circuit. The performance of the FBGA VCO is listed and compared to that of the WLP VCO1 in Table 5.4.

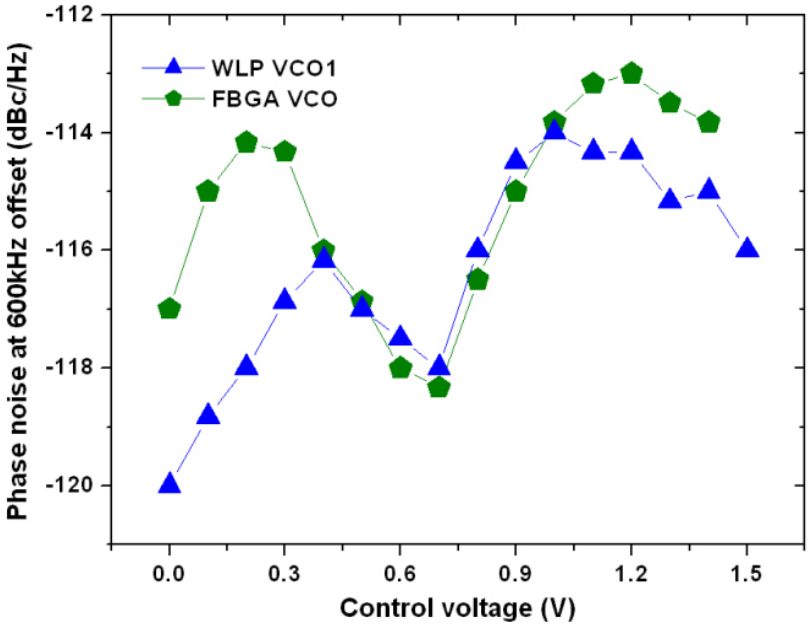


Figure 5.25 Phase noise of the FBGA VCO and the WLP VCO1 at the offset frequency of 600 kHz versus the control voltage.

Table 5.4 Performance comparison between the WLP VCO1 and the FBGA VCO.

	WLP VCO1	FBGA VCO	Comparison
Power consumption	2.9 mW	2.3 mW	-21 %
Center frequency	2.04 GHz	2.03 GHz	-
Tuning range	253 MHz	260 MHz	-
Output power	-14±0.5 dBm	-12.5±0.5 dBm	-
Phase noise	-114 ~ -120 dBc/Hz	-113 ~ -118.5 dBc/Hz	0 ~ +3 dB
FOM_T	-194.6	-193	+1.6

5.6 EXPERIMENTAL RESULTS OF OPTIMIZED WLP VCO

The VCO designs in the previous sections used the same sizes of active devices and varactors as listed in Table 5.2, which means that only the on-chip inductor is replaced by the high-Q embedded inductor in a package. As a result, although the lower power consumption and lower phase noise are achieved, the tuning range is reduced because of the high-Q characteristics of the embedded inductors. The reduction of tuning range can be avoided with the optimization of the VCO design (WLP VCO2). The sizes of the active devices, especially in the VCO core, and of the varactors are optimized to improve the tuning range. Since the Q-factor of the embedded inductor is higher than that of the on-chip inductor, the smaller active devices can be used to obtain the same feedback gain as in the VCO that uses the on-chip inductor. The sizes of the active devices and

varactors for the optimized VCO design are listed in Table 5.5. The active devices are half-sized by design compared with the on-chip VCO. In this case, the parasitic capacitances are reduced, which permits an increase in the size of the varactors to obtain the same oscillation frequency. The VCO design using smaller active devices and larger varactors results in not only an improved tuning range but also in the lower power consumption.

A supply voltage of 1.7 V is applied to operate the WLP VCO2. The current of 1.1 mA flows so that total dc power consumption is 1.87 mW, which is lower than the WLP VCO1. The power consumption of WLP VCO2 is reduced by 74 % compared to that of the on-chip VCO. The oscillation frequencies and output powers that occur with variations in control voltage are shown in Figure 5.26. The center frequency is 2.16 GHz. The tuning range is 385 MHz (17.8 %) with the control voltage from 0 to 1.7 V. Output power is around –12.5 dBm with a variation of ±1 dBm. The phase noise of the WLP VCO2 with variations of the control voltage is shown and compared to that of the on-chip VCO in Figure 5.27. Phase noise of the WLP VCO2 is lower than that of the on-chip VCO by a minimum 4 dB and a maximum 10 dB. The phase noise plot of WLP VCO2 with offset frequencies from 10 kHz to 1 MHz at the control voltage of 0 V is shown and compared to that of the on-chip VCO in Figure 5.28. Phase noise is improved by 12, 10, and 6 dB at the offset frequency of 60, 100, 600 kHz, respectively. The performance of the WLP VCO2 is listed and compared to that of the on-chip VCO in Table 5.6. The performance of the WLP VCO2 is compared to that of the recently published 0.35 μm CMOS VCOs with a oscillation frequency around 2 GHz, as listed in Table 5.7.

Table 5.5 Design parameters of the WLP VCO2.

	Devices	Design
VCO core	M1, M2	NMOS 0.35 μm × 10 μm × 4
	M3, M4	PMOS 0.35 μm × 10 μm × 12
Buffer	M5, M6	NMOS 0.35 μm × 10 μm × 2
	M7, M8	PMOS 0.35 μm × 10 μm × 6
Varactor	Cvar1, Cvar2	A-MOS 0.35 μm × 5 μm × 50 × 5

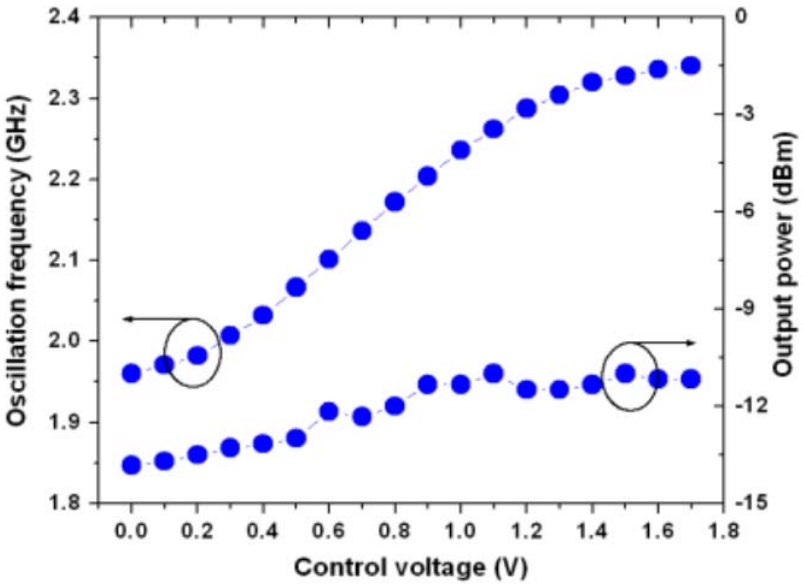


Figure 5.26 Oscillation frequencies and output powers versus the control voltage.

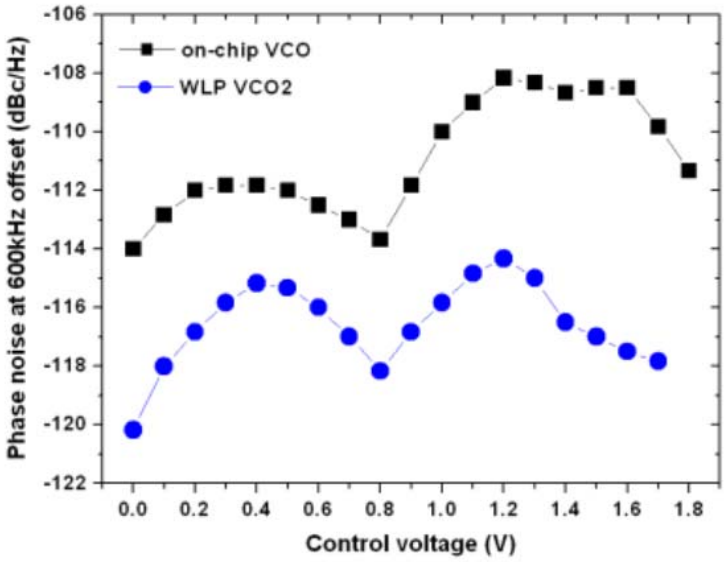


Figure 5.27 Phase noise of the WLP VCO2 and the on-chip VCO at the offset frequency of 600 kHz versus the control voltage.

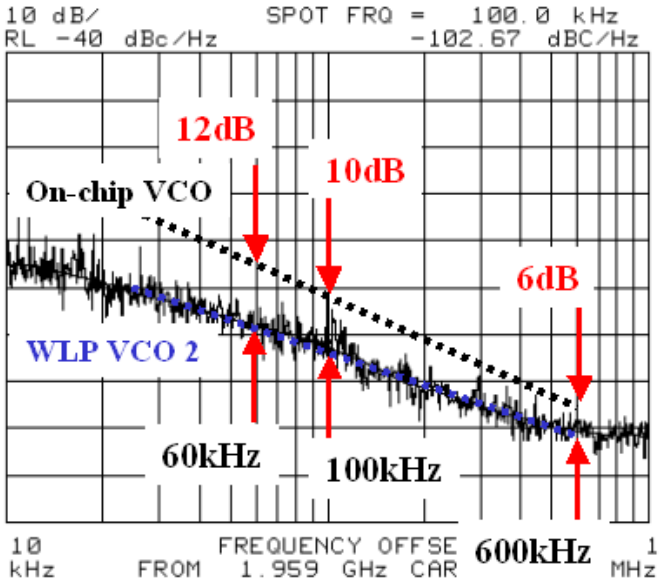


Figure 5.28 Phase noise plot at the control voltage of 0 V.

Table 5.6 Performance comparison between the on-chip VCO2 and the WLP VCO2.

	On-chip VCO	WLP VCO2	Comparison
Power consumption	7.2 mW	1.87 mW	-74 %
Center frequency	2.24 GHz	2.16 GHz	-
Tuning range	317 MHz	385 MHz	+21.5 %
Output power	-13.5±1 dBm	-12.5±1 dBm	-
Phase noise	-108 ~ -114 dBc/Hz	-114 ~ -120 dBc/Hz	-4 ~ -10 dB
FOM_T	-185.2	-197.7	-12.5

Table 5.7 Performance comparison with recently published 0.35μm CMOS VCOs around the oscillation frequency of 2GHz

Reference	[47]	[48]	[49]	[50]	WLP VCO2
Oscillation frequency (GHz)	2.03	1.93	2.4	2	1.96
Power Consumption (mW)	10	27.6	13.5	12.6	**1.87**
*Phase noise @ 1MHz (dBc/Hz)	-122	-127	-125	-130	-125
Tuning range (MHz)	720	107	250	370	385

*Phase noise is extrapolated with a slope of –20dB/decade

CHAPTER VI

CONCLUSION AND FUTURE WORK

6.1. TECHNICAL CONTRIBUTIONS AND IMPACT OF THE DISSERTATION

The increasing demands of customers for smaller size and lower cost for modern electronic mobile devices, are forcing RF IC designers to look for a better technical approach than the conventional hybrid radio. One of the attractive solutions is a Si-based single-chip radio. This approach has been considered to be feasible because of the technical advances in the field of Si-based ICs. The technical advances include not only the high-level integration by scaling but also the band-gap engineering on Si substrate. With the nano-scale CMOS and SiGe HBT, a Si-based single-chip radio has been considered feasible at least in terms of the frequency response of the active device.

In spite of great advances from an active device perspective, a Si-base single-chip remains a challenging proposition because of the poor quality of the passive components on the Si-substrate. The Q-factor of the passive components, especially the inductor, is crucial to designing high performance RF ICs. The lossy LC-matching networks affect the gain, output power, and efficiency of a power amplifier. The lossy inductor in a low-noise amplifier degrades the noise performance. A high-Q inductor guarantees the low phase noise, low power consumption, and wide tuning range in an LC-tank VCO. There is no doubt that a Si-based IC technology is an attractive solution of demands for low cost and small size. However, a low-Q inductor restricts the Si-based single-chip radio from being the best solution in terms of performance. This situation limits the wireless

applications that can be realized by the Si-based single-chip approach. Truly, this approach is first applied to wireless applications with somewhat loose specifications like the Wireless Local Area Network (WLAN).

For this reason, Si-based IC technologies have been developed to obtain a high-Q inductor. Thick metallization, a thick SiO_2 inter-dielectric layer, more metal layers, and a highly resistive Si substrate are all incorporated in a solution that increases cost, which is diametrically opposed to the reasons originally advanced for Si-based single-chip radios. Even Si-based micro-electro-mechanical system (MEMS) technologies have been used to implement a high-Q inductor, however, those are still in a research domain.

In this dissertation, a Si-based single-chip approach is slightly modified to be a much better solution. As a final step, the fabricated single-chip should be packaged that it can be commercialized. Therefore, in this dissertation a high-Q inductor implementation is addressed by using wiring metal lines in a package, which can be called a Si-based single-chip package solution. This approach yields not only small size and low cost, but also high performance, which means that it can be applied to mobile handset applications having stringent specifications.

The feasibility and theoretical analysis of the approach outlined in this dissertation is performed with a VCO circuit. It is generally accepted that a high-Q inductor provides low phase noise in a VCO. In addition to dealing with phase noise, this dissertation also shows that a high-Q inductor entails low power consumption and wide frequency tuning characteristics.

Technically, the 0.35 μm CMOS IC technology is used for VCO design. For the inductors, three different technologies are incorporated: on-chip inductor, FBGA inductor,

and WLP inductor. A VCO using the on-chip inductor is designed for a reference. The VCOs using the embedded high-Q inductor in a FBGA and a WLP are implemented and compared with the on-chip VCO in terms of performance. The limitations of this Si-based single-chip package approach on an LC-tank CMOS VCO are analytically and experimentally verified from the point of view of active and passive device.

We have not only presented the quality of the embedded inductor itself but also investigated the interconnection effects with a real IC. Even if an embedded inductor shows good quality, when it is connected to an IC, its quality is degraded. As a result, the interconnection limits the usable frequency range of the embedded inductor, and this limitation comes from the on-chip pad characteristics. Therefore, the critical factors for the usable frequency limit of an embedded inductor lie in the IC process parameters such as substrate doping, the number of metal layers, and the diameter of a pad. Furthermore, in the case of a WLP, the via-process of a WLP should be compatible with the size of the on-chip pad. Considering the IC and package process used in this dissertation, the maximum frequency not affected by the on-chip pad parasitics is 2 GHz, thereby, the VCOs are designed at 2 GHz.

The dominant loss factor in an LC-tank on phase noise has been investigated. When the Q-factor of the inductor is very low, the series resistance of the inductor layer is a limiting factor for phase noise. As the Q-factor increases, the impedances toward the active devices become more dominant. Therefore, in the case of 2 GHz CMOS VCO, when the series resistance of the inductor layer goes below 1 Ω, a smaller gate length of CMOS technology is necessary to improve phase noise.

Three VCOs with the on-chip inductor, WLP inductor, and FBGA inductor are designed with the same size of the active core devices and varactors, which are called an on-chip VCO, WLP VCO1, and FBGA VCO, respectively. Compared with the on-chip VCO, the WLP VCO1 shows phase noise improvement of 4 ~ 6 dB and the reduction of power consumption by 60 %. However, the frequency tuning range is reduced by 20 %.

The performance of the FBGA VCO is compared with that of the WLP VCO1. The Q-factor of the FBGA inductor is three times higher than that of the WLP inductor. While the power consumption is reduced by 21 %, the phase noise performance is almost the same or even slightly worse. This is because the symmetry of the VCO circuit is disturbed by the bond wires for the interconnection between the VCO and the FBGA inductor. Consequently, even though the FBGA inductor shows a higher Q-factor than the WLP inductor, the WLP inductor proves to be a better inductor because the phase noise improvement begins to saturate at over a Q-factor of 10, and the symmetry of the VCO circuit is not guaranteed with the FBGA inductor.

While low power consumption and better phase noise are achieved with the WLP VCO1 and the FBGA VCO, the frequency tuning range is reduced by 20 %. This drawback was overcome by the optimization in size of the active core devices and varactors. Because of a high-Q characteristic, the smaller devices can be used for the VCO core to obtain the same feedback gain as in the case of a low-Q inductor. Therefore, the WLP VCO2 has been designed with active devices half the size of those used with the WLP VCO1. To make a similar oscillation frequency of around 2 GHz, the size of the varactors is increased by 25 %. As a result, lower power consumption, comparable phase noise, and wider tuning range are obtained at the same time by this design optimization.

Finally, the contributions of this dissertation can be summarized as follows.

1. The advantages of the Si-based single-chip package approach are analytically and experimentally verified compared with the Si-based single-chip approach by the implementation of the LC-tank CMOS VCO at 2 GHz.
2. High-Q inductors using wiring metal lines of advanced packaging technologies such as FBGA, MCM-L, and WLP are implemented and characterized.
3. The Q-factor of the embedded inductors is compared with that of the on-chip inductors on Si and GaAs substrates implemented by commercially available IC processes.
4. The LC-tank CMOS VCOs using the high-Q inductor embedded in a FBGA and a WLP are implemented and compared with the VCO using an on-chip inductor in terms of performance such as phase noise, power consumption, and frequency tuning range.
5. The dominant loss factor in the LC-tank limiting phase noise improvement of CMOS 2 GHz VCO is analytically investigated and experimentally proven.
6. Design optimization of an LC-tank CMOS VCO from a high-Q inductor perspective to achieve low phase noise, low power consumption, and wide tuning range is performed and experimentally proven.
7. It is experimentally shown that not only a high-Q inductor but also the symmetry of the VCO circuit is critical to obtaining low phase noise.

6.2. SCOPE OF FUTURE RESEARCH

The work described in this dissertation represents a starting point for many interesting and challenging possible future research directions. The phase noise analysis on the LC-tank in a CMOS cross-coupled differential VCO topology has been performed and experimentally proven in this dissertation. When the Q-factor of the inductor becomes more than 10 at 2 GHz (or the series resistance of the inductor layer goes below 1 Ω), the main factor limiting phase noise is not the inductor, but the impedances of the active core devices. Therefore, it would be interesting to do research on the active device side. In this dissertation, a 0.35 μm CMOS process was used. The effects on phase noise with 0.25, 0.18, or 0.13 μm CMOS processes and a high-Q inductor would be a valuable work. As gate length scales down, the noise characteristics would change. Thus, comparing the phase noise of the VCOs implemented in different gate length technologies requires not only the loss analysis in a resonator but also the noise analysis of active devices, which is very challenging.

Another interesting research topic would be interconnection issues. As shown in this dissertation, the interconnection between the FBGA inductor and the VCO circuit affects phase noise. Research on interconnections that would not disturb the symmetry of the VCO circuit also would be interesting.

The last interesting issue is the varactor. When phase noise is measured by sweeping the control voltage, the notch point is observed at the zero-biased point of the varactor. This indicates that the characteristic of the varactor affects phase noise. Usually the effect of the varactor characteristics on phase noise are not considered seriously because the

bottleneck has been the inductor. However, the inductor is not a bottleneck anymore with an embedded inductor, thus, it would be interesting to do research on the varactor side.

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APPENDIX

AUTHOR'S PUBLISHED WORK

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VITA

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