UNIVERSITY OF CALIFORNIA, BERKELEY

College of Engineering

Department of Electrical Engineering and Computer Sciences

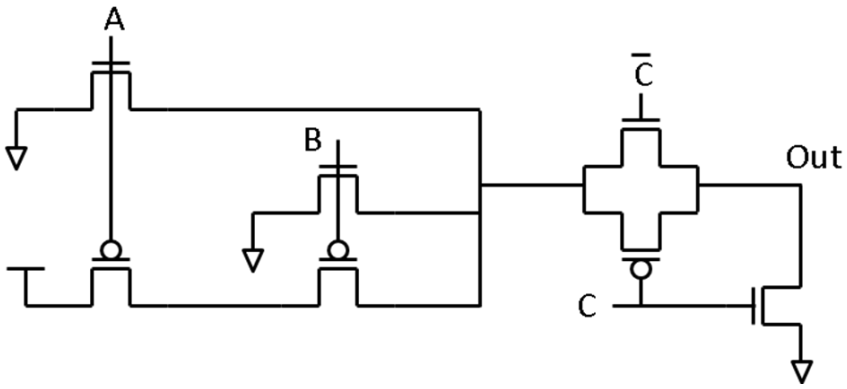
Jan M. Rabaey **Homework #7** **EECS 141 (SP10)**

Due Monday, April 5, 5pm, box in 240 Cory

[PROBLEM 1] Logic Styles and Logical Effort (30 pts)

In this problem, you can assume that $C_D = C_G$ = 2fF/um, and R_{eqNMOS} = 10kΩ, R_{eqPMOS} = 20kΩ, for the minimum-size NMOS and PMOS transistors (size=1).

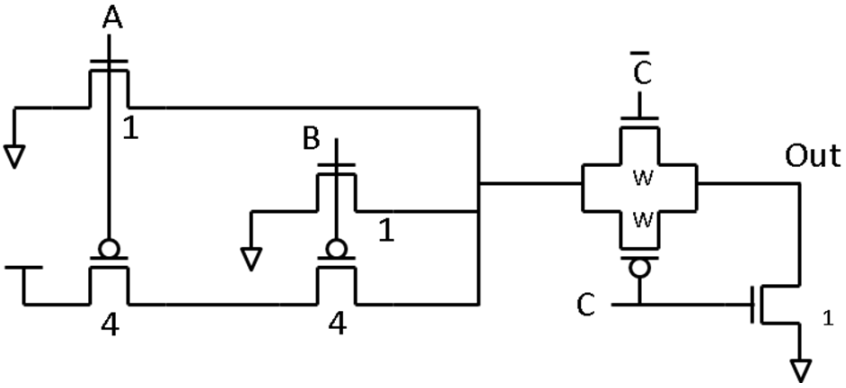
(a) What logical function does the gate shown below perform? (5 pts)



Solution:

The logical function: $Out = \overline{C} \cdot \overline{(A+B)} = \overline{A+B+C}$

(b) Given the sizing show below, what value of W would you use in order to make the worst-case LE of the C input equal to half of the LE of A and B inputs (i.e., LE_C=1/2 LE_A) What would be the LE of the C input in this case? (5 pts)



Solution:

The worst case resistance of the stage is the same for the cases of input A, B, C.

So LE_C=1/2 LE_A means the input cap for C is ½ of the input cap for A.

$Ci_{n,C}$ = ½ $C_{in,A}$ => (W+1)=2.5 => W =1.5

LE_C = {(2/4+2/4+1/1.5)xReqx2.5 C_G} / (Reqx3C_G) = 1.38

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Note: here the equivalent resistance for the transmission gate (controlled by C and C_bar) is ~= Req,NMOS / W.

A Brief Explanation:

For pull-up direction:

R(transmission gate)= 2 RN // RP =1/w [2 Req,NMOS // Req,PMOS]
= 1/w [Req,NMOS]

Here we put "2RN" in the calculation is because NMOS is weaker in pull-up direction in the transmission gate.

For pull-down direction:

R(transmission gate)= RN // 2 RP =1/w [Req,NMOS // 2Req,PMOS]
= 1/w * 4/5 [Req,NMOS] ~= 1/w [Req,NMOS]

Here we put "2RP" in the calculation is because PMOS is weaker in pull-down direction in the transmission gate.

According to the above explanation, we approximate the equivalent resistance for transmission gate to be "ReqNMOS / W" in both pull-up and pull-down directions.

If you want to know more about LE and Req calculation of transmission gate, please see the scanned pages from "Logical Effort" book by Sutherland that attached in Namseog's email.

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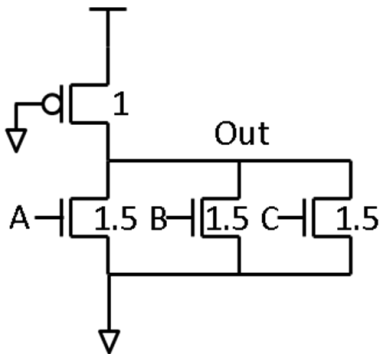
(c) Use **ratioed logic** to implement the same logic function in (a). Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2/1). **The size of load PMOS is 1.** What is the LE of input A, B and C for H->L transiton? (10 pts)

Solution:



In order to have the same pull down strength in worst case, A, B C should have size of 2.

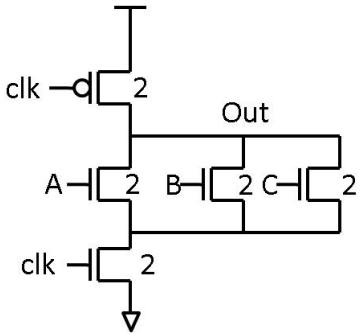
(Rn/W)/ (1-1/2W)=Rn => W =1.5

$LE_{HL,A}=LE_{HL,B}=LE_{HL,C}=1/2$

(d) Use **dynamic logic** to implement the same logic function in (a). Size the transistors such that the worst-case drive strength for all inputs is the same as a

unit inverter (PMOS to NMOS ratio is 2/1). The size of the evaluation NMOS transistor (connected to clock in pull-down network) is the same as the size of other NMOS transistors in PDN. What is the LE of input A, B and C during evaluation phase? (10 pts)

Solution:

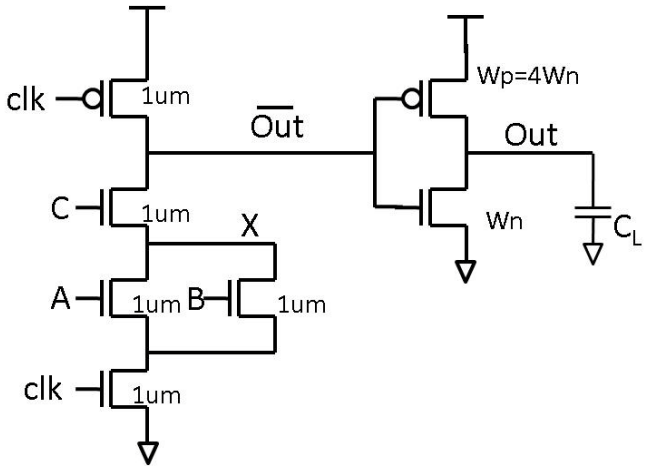


$LE_A=LE_B=LE_C=2/3$

[PROBLEM 2] Dynamic Logic Design (45 pts)

In this problem, you can assume that VDD = 1.2 V, $C_D = C_G$ = 2fF/um.

(a) In the domino gate shown below, what is the minimum Wn necessary to ensure that the gate does not fail due to charge sharing? You can assume that the V_{IH} of the inverter is ¾ VDD, and none of the source/drain regions have been shared (10 pts)



Solution:

Capacitance at node X:

$C_x = C_{DB} + C_{DA} + C_{DC} + C_{GC}$ = 3um x 2fF/um + 1um x 2fF/um = 8fF

Capacitance at node $\overline{out}$:

$$C_{\overline{out}} = C_{DC} + C_{D,pmos} + 5W_nC_G = 4fF + Wn \cdot 10fF/um$$

$$\text{Charge Sharing}: V_{DD} \times C_{\overline{out}} = V_{new}(C_{\overline{out}} + C_x)$$

$$V_{new} = \frac{C_{\overline{out}}}{C_{\overline{out}} + C_x} \times V_{DD}$$

$$V_{new} \geq \frac{3}{4}V_{DD} \Rightarrow \frac{4fF + W_n 10fF/um}{4fF + W_n 10fF/um + 8fF} \geq \frac{3}{4}$$

$$W_n \geq 2um$$

********** Alternative Solution **********

If you divide C_{Gc} evenly on both drain and source sides,

$C_x = C_{DB} + C_{DA} + C_{DC} + 0.5\ C_{GC}$ = 3um x 2fF/um + 0.5x 1um x 2fF/um = 7fF

$$C_{\overline{out}} = 0.5C_{GC} + C_{DC} + C_{D,pmos} + 5W_nC_G = 1fF + 4fF + Wn \cdot 10fF/um$$

$$\text{Charge Sharing}: V_{DD} \times C_{\overline{out}} = V_{new}(C_{\overline{out}} + C_x)$$

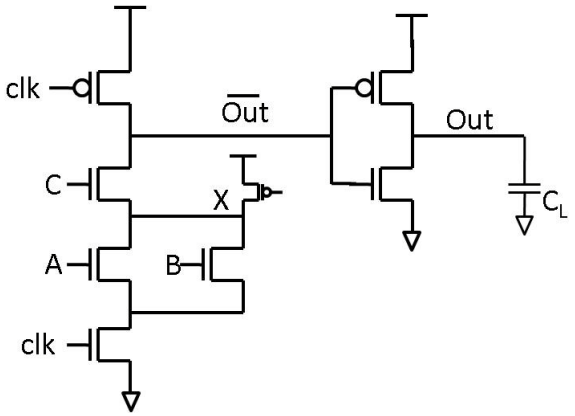
$$V_{new} = \frac{C_{\overline{out}}}{C_{\overline{out}} + C_x} \times V_{DD}$$

$$V_{new} \geq \frac{3}{4}V_{DD} \Rightarrow \frac{5fF + W_n 10fF/um}{5fF + W_n 10fF/um + 7fF} \geq \frac{3}{4}$$

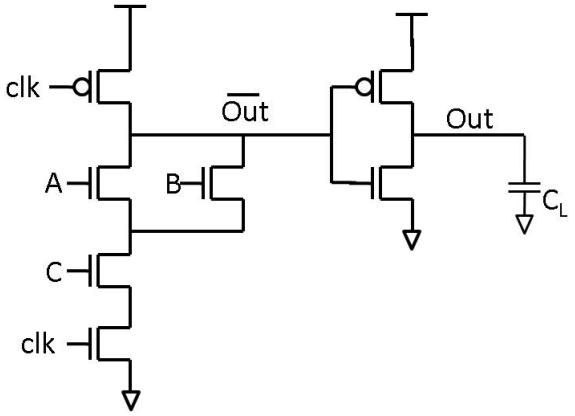
$$W_n \geq 1.6um$$

(b) In order to mitigate the charge sharing issue, what can we change in the gate from (a)? You should explain your changes and draw new transistor-level schematics of the gate (no sizing necessary). (15 pts)

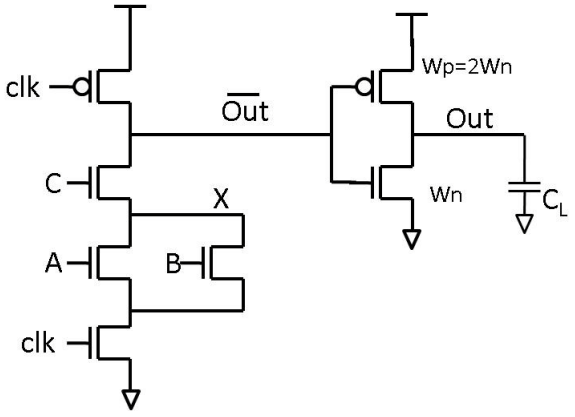
Solution:
1:Pre-charge the internal node:



2: re-order the gate to increase $C_{\overline{out}}$



3: reduce the P/N ratio (skew) of inverter to reduce V_{IH}. (This does not reduce charge sharing, but reduce its impact on the output



(c) On the evaluation phase, what is the worst case delay of the dynamic gate in (a) as a function of R_{eqNMOS}, R_{eqPMOS}, C_G and C_L? R_{eqNMOS}, and R_{eqPMOS} are the equivalent resistances of minimum size NMOS and PMOS. You can assume C_D = 0 and ignore the slope effect. (10 pts)

Solution:

$$t_{pLH} = 0.69 \times (R_{eq,NMOS} \times C_G + 2R_{eq,NMOS} \times C_G + 3R_{eq,NMOS} \times 5WnC_G + \frac{R_{eq,PMOS}}{4Wn} \times C_L)$$

********** Alternative Solution **********
If you divide C_G evenly on both drain and source sides,

$$t_{pLH} = 0.69 \times (R_{eq,NMOS} \times 0.5C_G + 2R_{eq,NMOS} \times C_G + 3R_{eq,NMOS} \times (5WnC_G + 0.5C_G) + \frac{R_{eq,PMOS}}{4Wn} \times C_L)$$

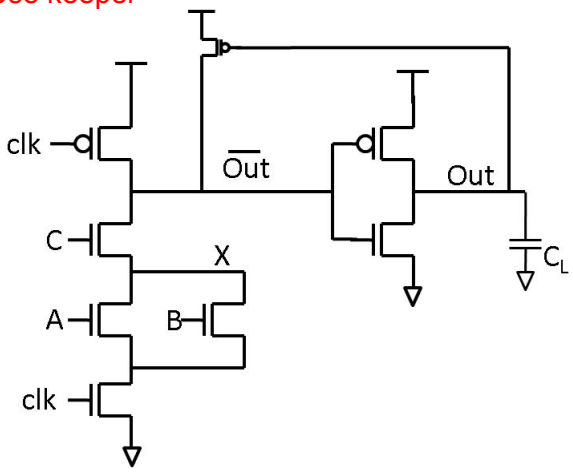
(d) What are the activity factor of node Out if P(A=0) = P(B=0) = P(C=0) = 0.25? (Bonus 5 pts)

Solution:
These 5 points are bonus points.

$$\alpha_{0->1} = P(A=0) \cdot P(B=1) \cdot P(C=1) + P(A=1) \cdot P(B=0) \cdot P(C=1) +$$
$$P(A=1) \cdot P(B=1) \cdot P(C=1) = \frac{9}{64} + \frac{9}{64} + \frac{27}{64} = \frac{45}{64} = 0.703$$

(e) Charge leakage at node $\overline{\text{Out}}$ may cause problems. What is the solution to resolve this issue? (5 pts)

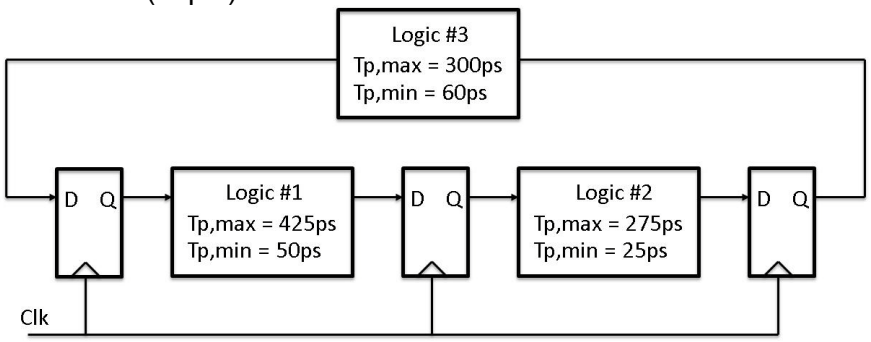
Solution:
Use keeper



[PROBLEM 3] Timing (30pts)

In this problem we will be examining the pipeline shown below. The minimum and maximum delays through the logic are annotated on the figures, and the registers have the following properties: $t_{clk\text{-}q}$ = 50ps, t_{setup} = 25ps, and t_{hold} = 40ps. You can assume that the clock has no jitter.

(a) What is the minimum clock cycle time of this pipeline? Are there any hold time violations? (10pts)



Solution:

Minimum clock cycle: Logic # 1 has the largest $T_{p,max}$,

$t_{clk\text{-}q} + T_{p,max(Logic\#1)} + t_{setup} < T_{cycle}$

=> 500ps < T_{cycle}. The minimum clock cycle is 500ps

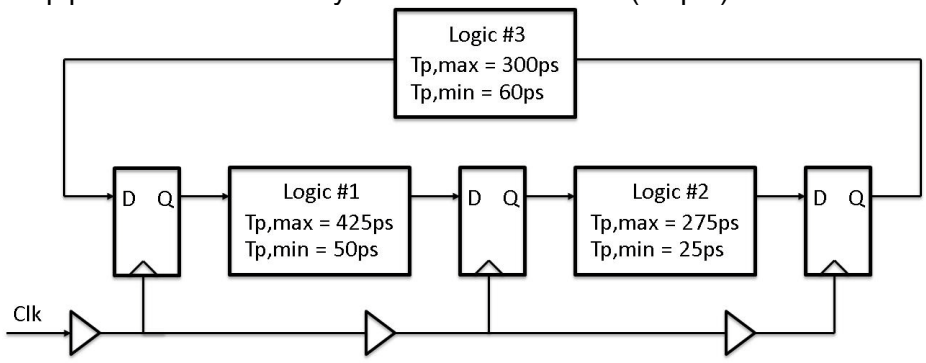
Check hold time violation:

Logic #2 has the smallest $T_{p,min}$,

$t_{clk\text{-}q} + T_{p,min(Logic\#2)} > t_{hold}$

=> No hold time violation.

(b) Now we insert the repeaters for distributing the clock signal to three registers. Assume that the delay of each repeater is nominally 50ps and each repeater's delay varies randomly by +/- 20%, now what is the minimum clock cycle time of this pipeline? Are there any hold time violations? (10 pts)



Solution:

Minimum clock cycle:

Logic # 1 has the largest $T_{p,max}$, and the worst-case skew is 40ps:

$t_{clk\text{-}q} + T_{p,max(Logic\#1)} + t_{setup} - t_{repeater} < T_{cycle}$

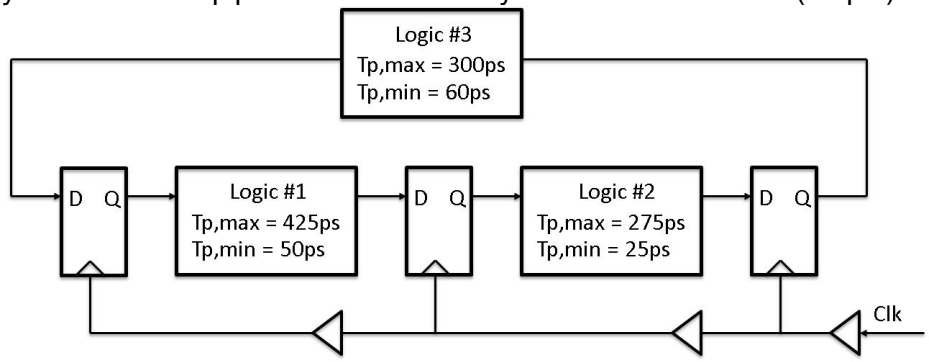
=> 460ps < T_{cycle}.

Logic # 3 has negative skew, and the worst-case skew is 120ps:
$t_{clk\text{-}q} + T_{p,max(Logic\#3)} + t_{setup} + t_{repeater} + t_{repeater} < T_{cycle}$
=> 50ps + 300ps + 25ps + 120ps < T_{cycle}.
=> 495ps < T_{cycle}.

The minimum clock cycle is 495ps

Check hold time violation:
Logic #2 has the smallest $T_{p,min,}$ and the worst-case skew is 60ps:
We have the constraint "$t_{clk\text{-}q} + T_{p,min(Logic\#2)} > t_{hold} + t_{repeater}$"
But we find 50ps + 25ps -60ps < t_{hold}
=> **Hold time violation!!**

(c) Under the same conditions (i.e., 50ps nominal inverter delay and +/-20% delay variation), if we feed the clock from the other direction, what is the minimum clock cycle time of this pipeline? Are there any hold time violations? (10 pts)



Solution:

Minimum clock cycle:
Logic # 1 has the largest $T_{p,max}$, and the worst-case repeater delay is 60ps:
$t_{clk\text{-}q} + T_{p,max(Logic\#1)} + t_{setup} + t_{repeater} < T_{cycle}$
=> 560ps < T_{cycle}. The minimum clock cycle is 560ps

Check hold time violation:
Logic #2 has the smallest $T_{p,min,}$ and the worst-case repeater delay is 60ps:
We have the constraint, "$t_{clk\text{-}q} + T_{p,min(Logic\#2)} > t_{hold} - t_{repeater}$ "
50ps + 25ps + 60ps > t_{hold}
=> No hold time violation.

Logic #3:
We have the constraint "$t_{clk\text{-}q} + T_{p,min(Logic\#3)} - t_{repeater} - t_{repeater} < t_{hold}$-"
But we find 50ps + 60ps -120ps < t_{hold}
=> **Hold time violation!!**