

Cadence Tutorial

This is a simple tutorial on using the Cadence version 6.1.6 for creating an inverter. This tutorial covers setting up the environment, and designing a simple inverter from beginning to LVS clean.

First, log into a computer in the lab. This can be done sitting in the lab, using VNC, or through ssh. If using ssh, use the -Y option to ensure all the X11 comes back to your computer.

Start a terminal session. (Right click, and select terminal). Items you should type are shown in a typewriter style font. The stylized ↵ indicates the carriage return or the enter key. Create a directory for the 45nm sub-threshold work. I'll use st45 for sub-threshold forty five.

```
mkdir st45↵.Change to that directory cd st45↵.
```

copy the setup data to the directory (there is a period typed before the carriage return)

```
cp ~morris/setup45/* .↵
```

Check and see the correct files were copied

```
ls↵
```

You should get

```
cds.lib s45 s45.csh
```

start Cadence 6.1 with the following command

```
./s45↵
```

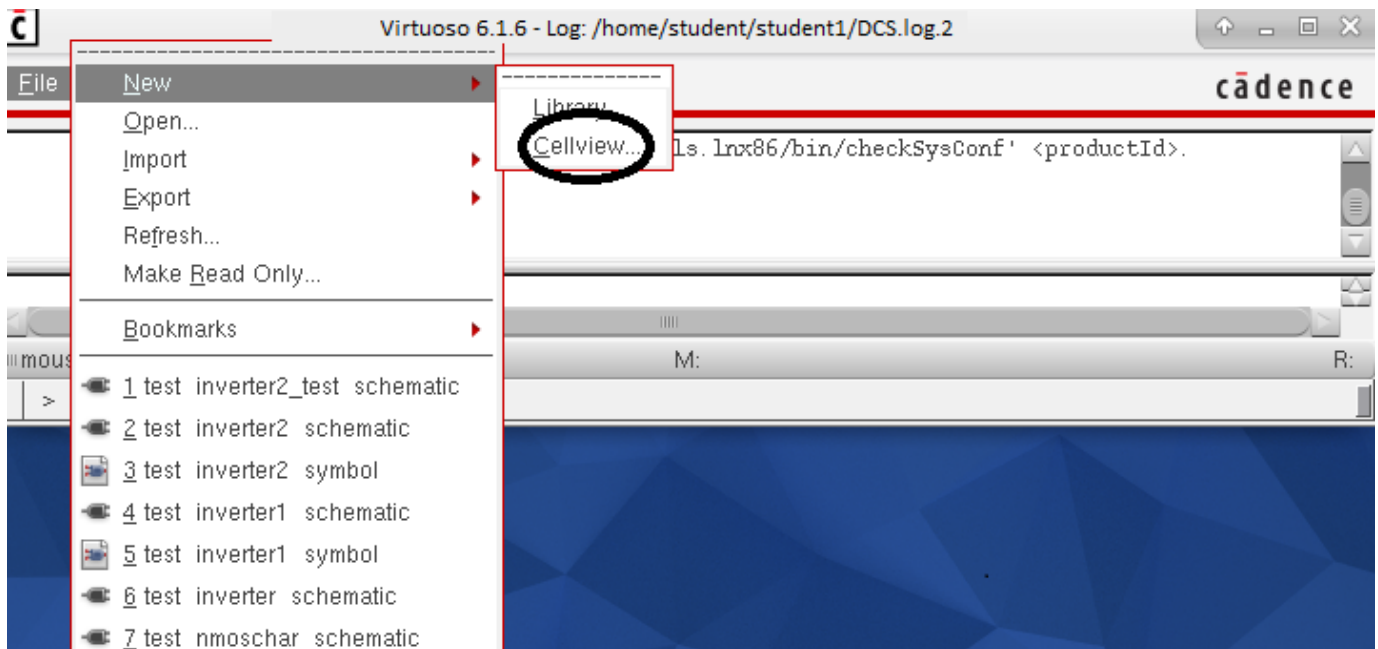
This will set up an environment and start the cadence system

Feature Size Available

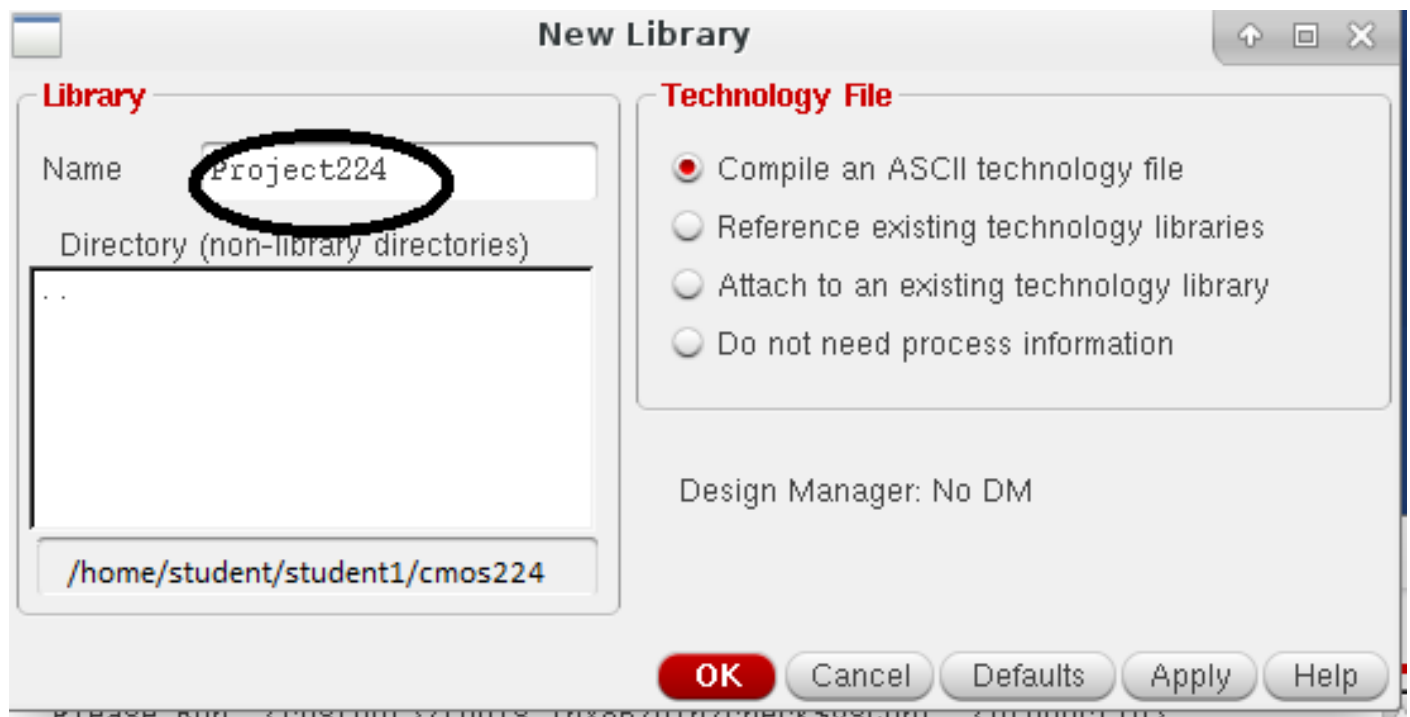
- 45nm technology is used
- Minimum width is 120nm
- Minimum Sizing is 1.5:1

How to start?

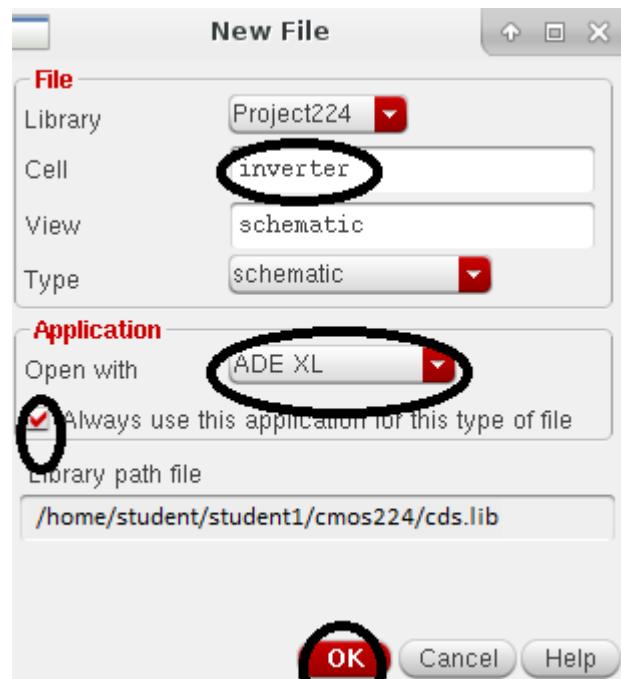
To start, we have to create our library
Click on file<New<Library.



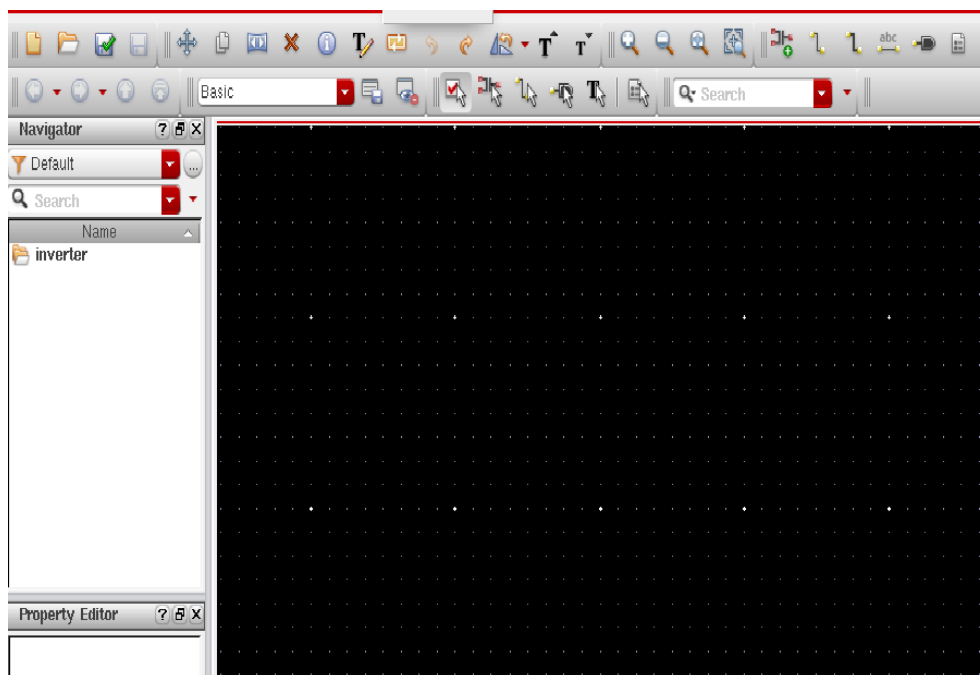
Add name of the Library: Project224 (you can take any name).



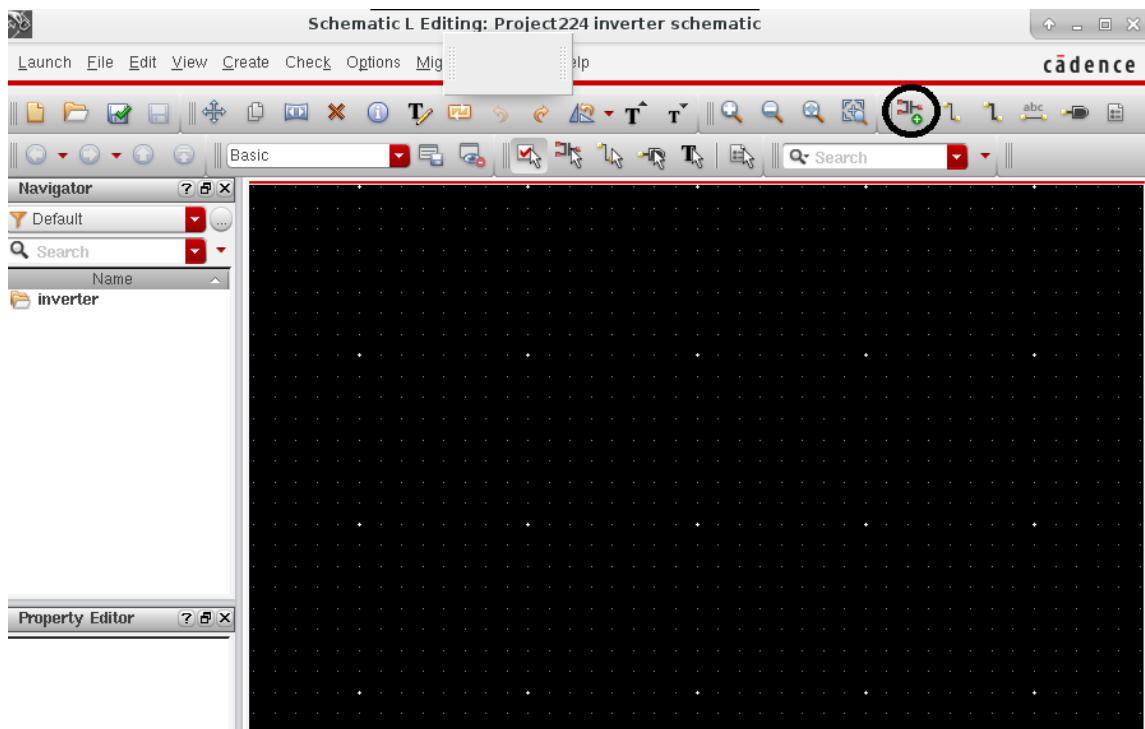
To implement an inverter, first create cell view
Click File<New<Cellview



Add cell name "inverter"
In application: Open with "ADE XL".
Check the box
Click OK



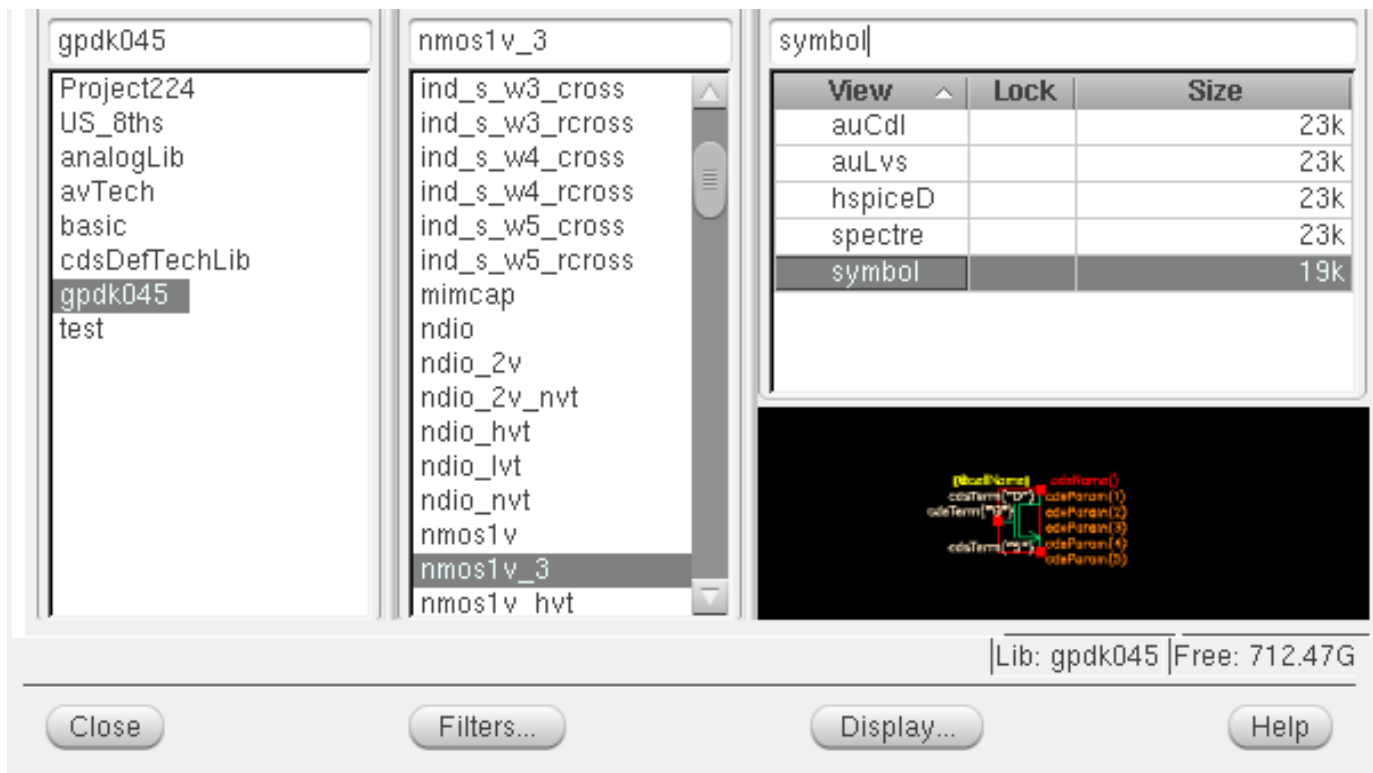
Above screen will be open (where we design the circuit)



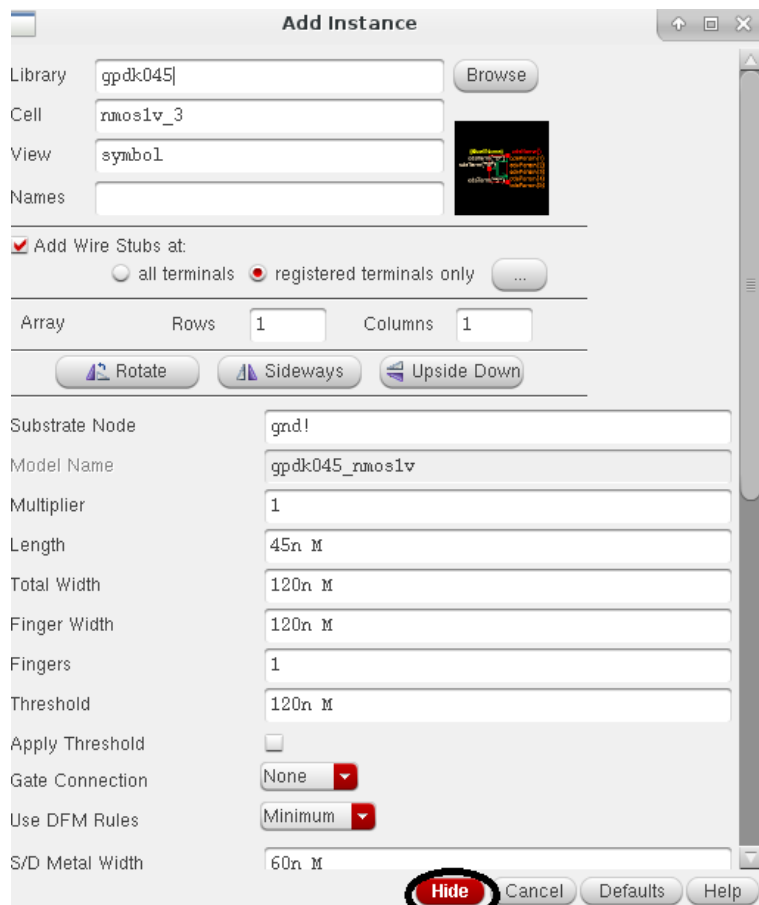
First, add a N transistor. Select a component by clicking on the transistor symbol. (Highlighted above with a black circle)



This gives a small selection screen. Click Browse to select the library.

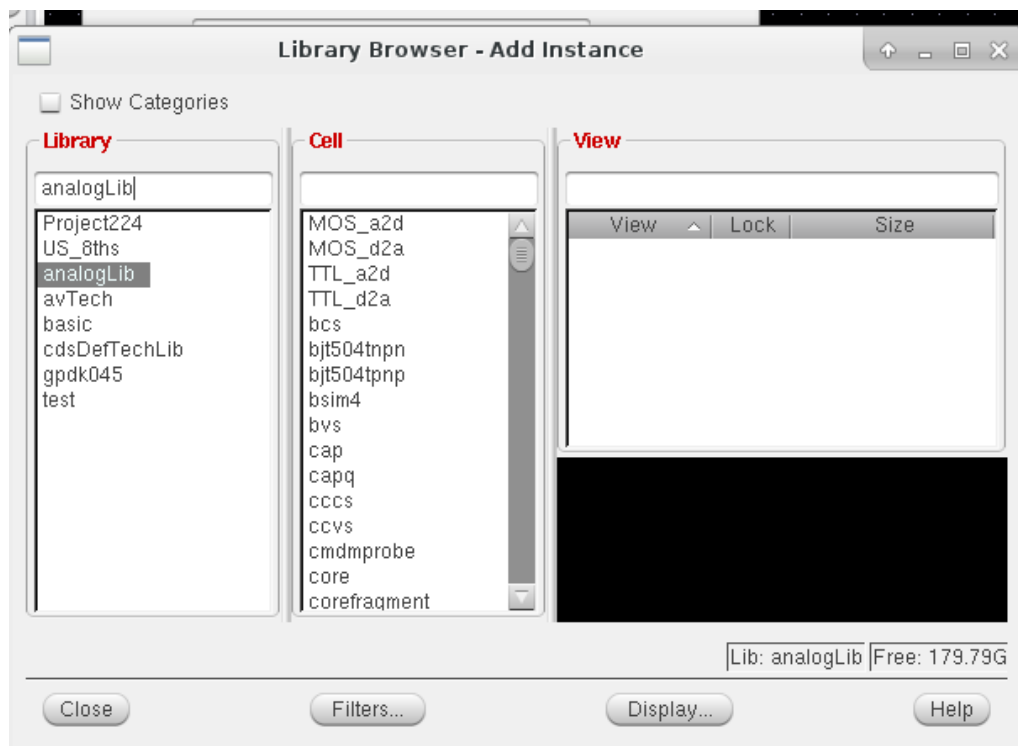


Now select gpdK045, then the transistor for this inverter N transistor. In this case, a nmos 1 Volt 3 terminal transistor with a high voltage threshold (nmos1v_hvt_3). Then select the symbol for inclusion in the schematic

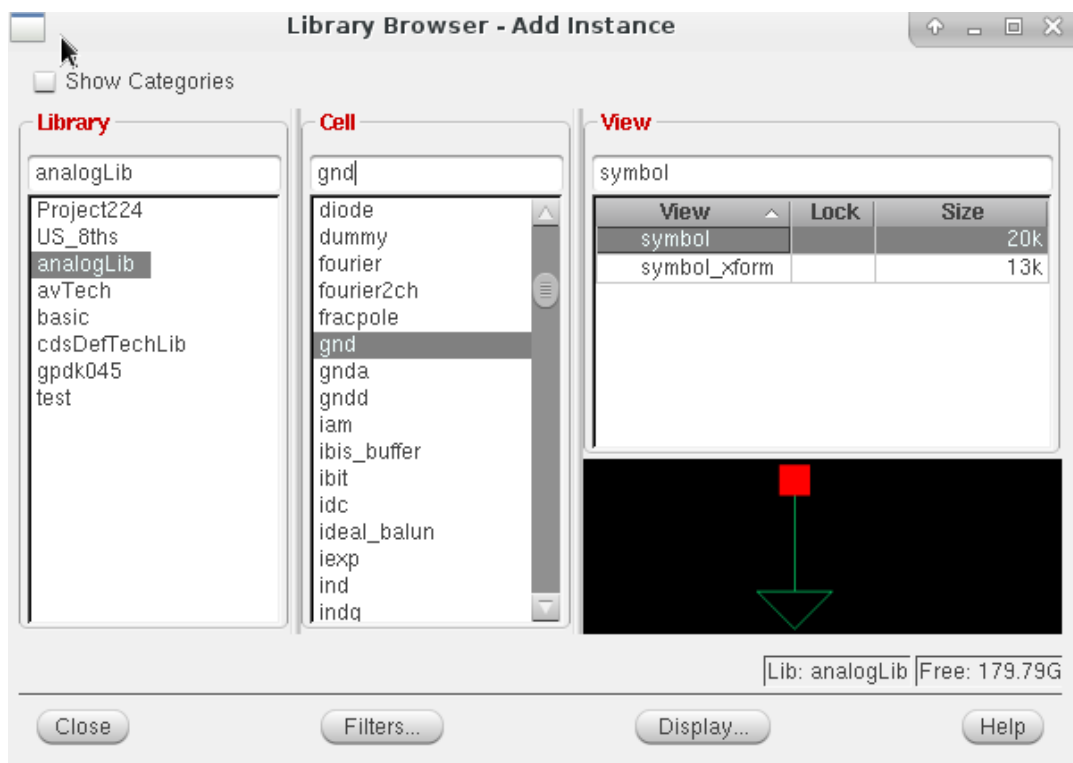


Click Hide

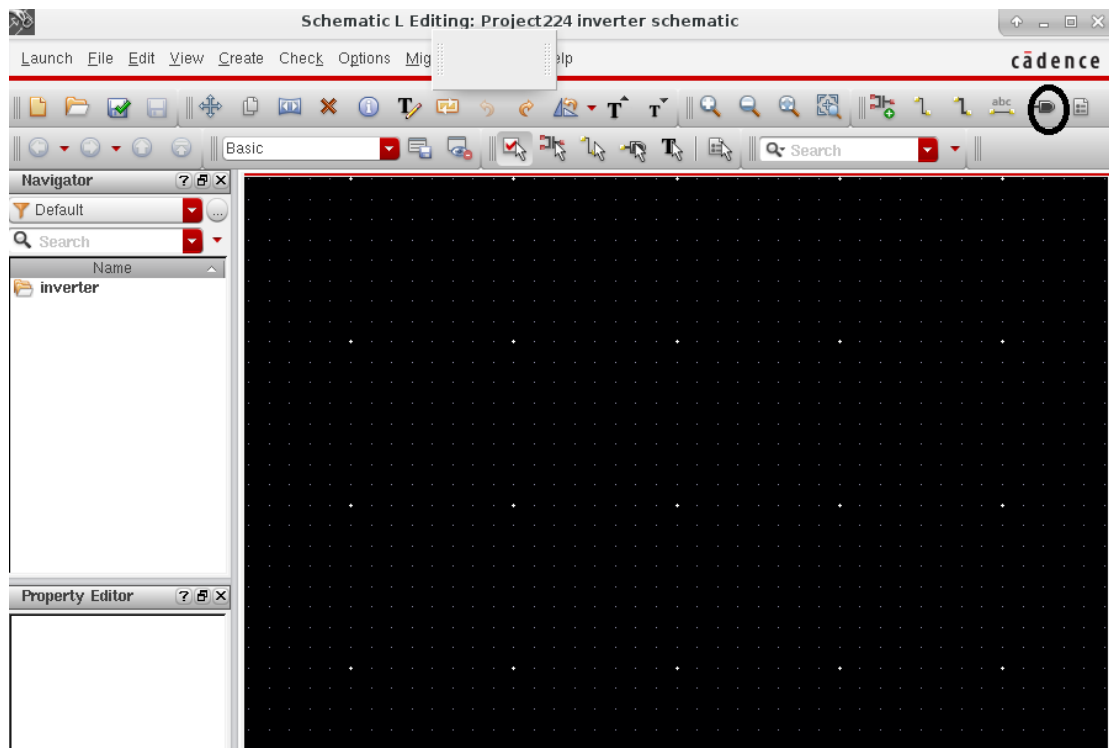
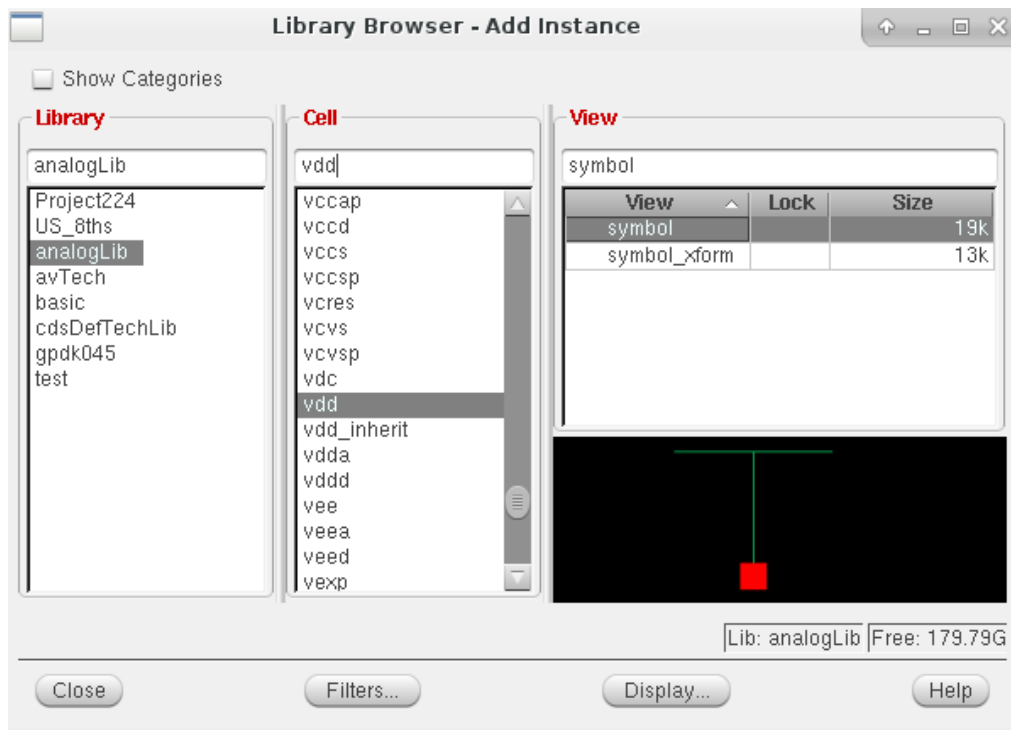
Similarly select for p-transistor and put the symbol on the screen



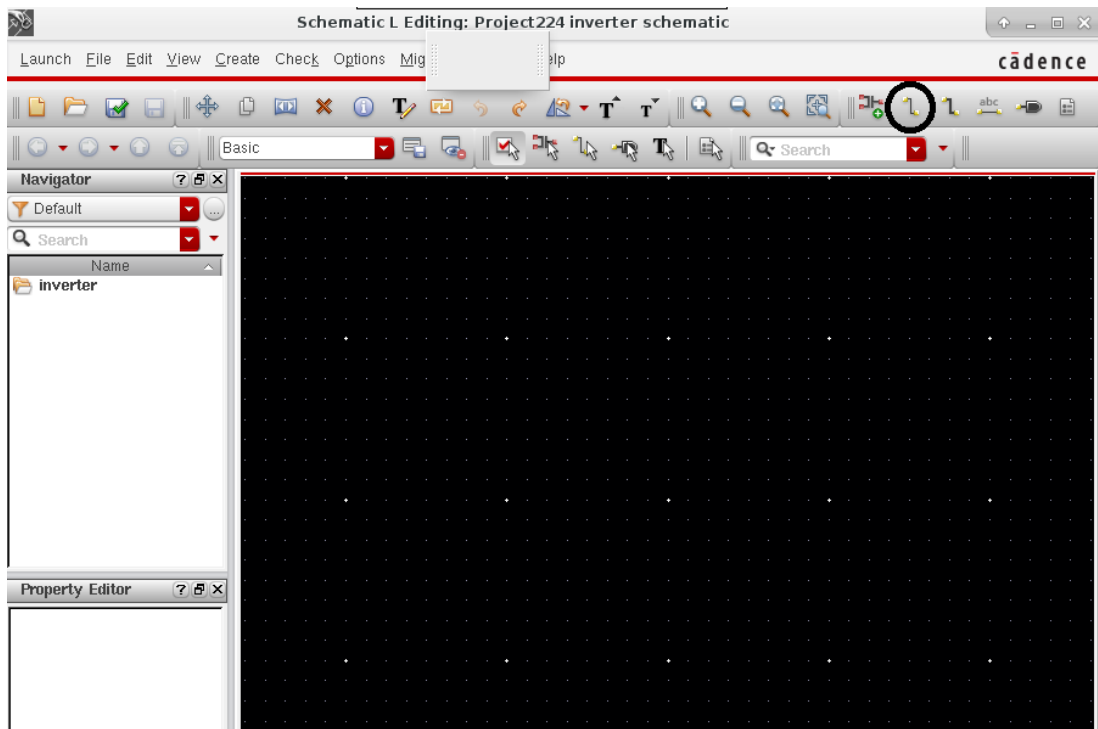
Now select a component for Vdd and Gnd. And place them on the schematic. These are found in analogLib.



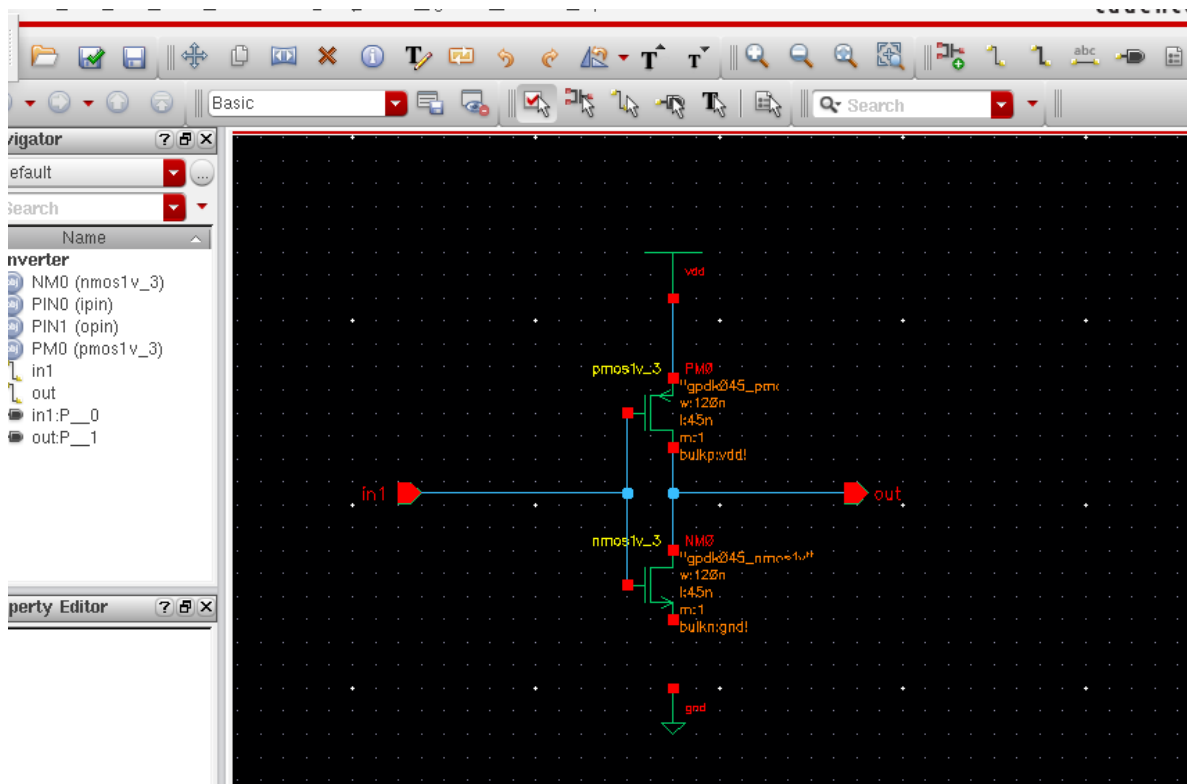
Click on Close



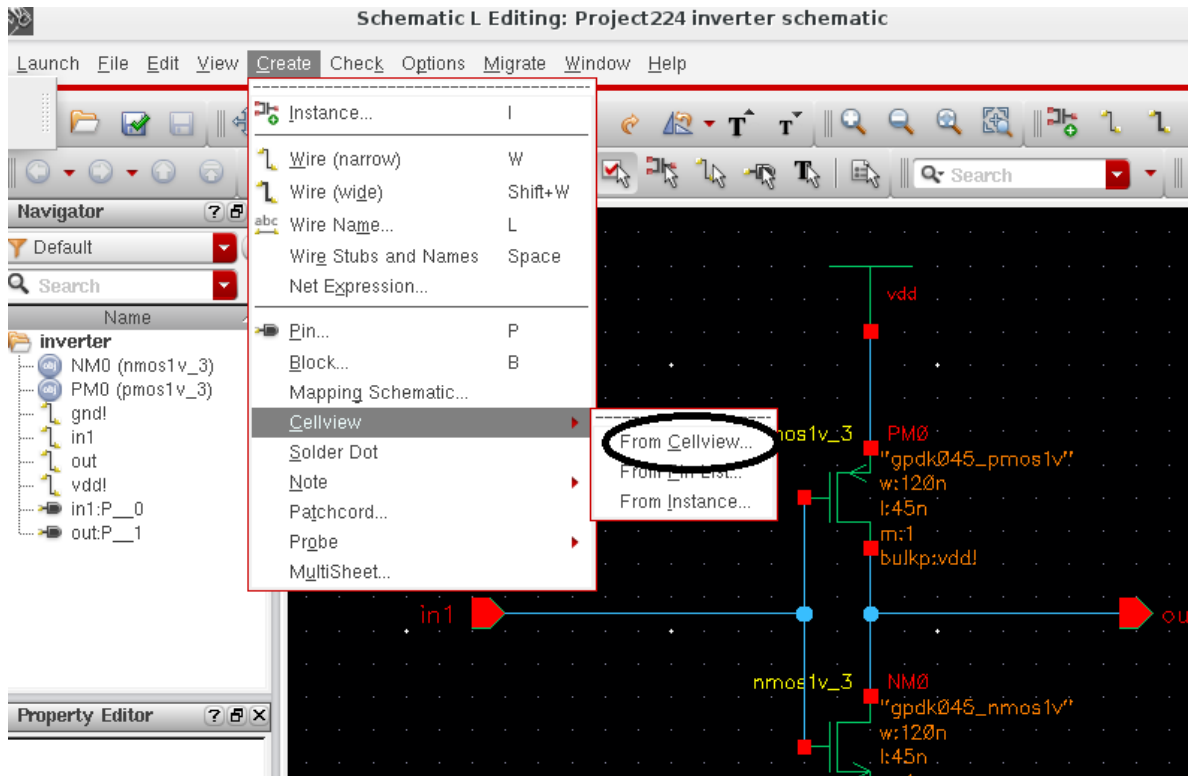
Select the input and output pin from the icon highlighted above with black circle.



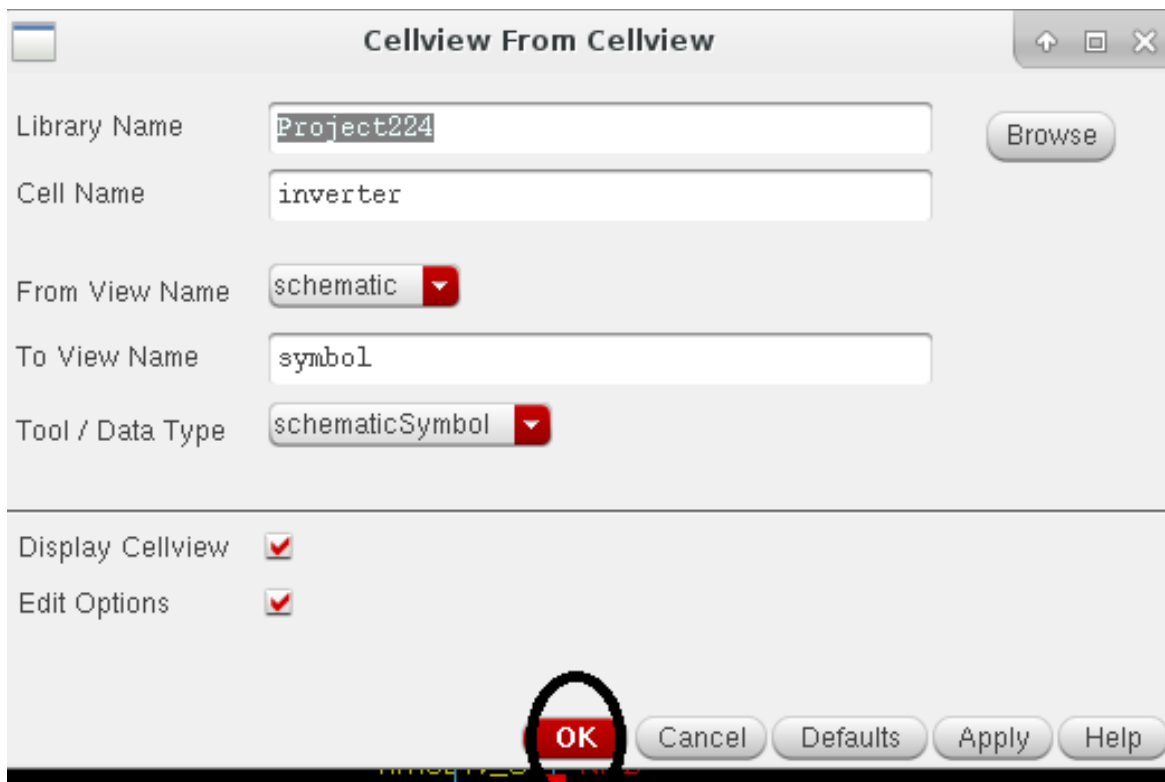
Select the thin wire to connect the components.



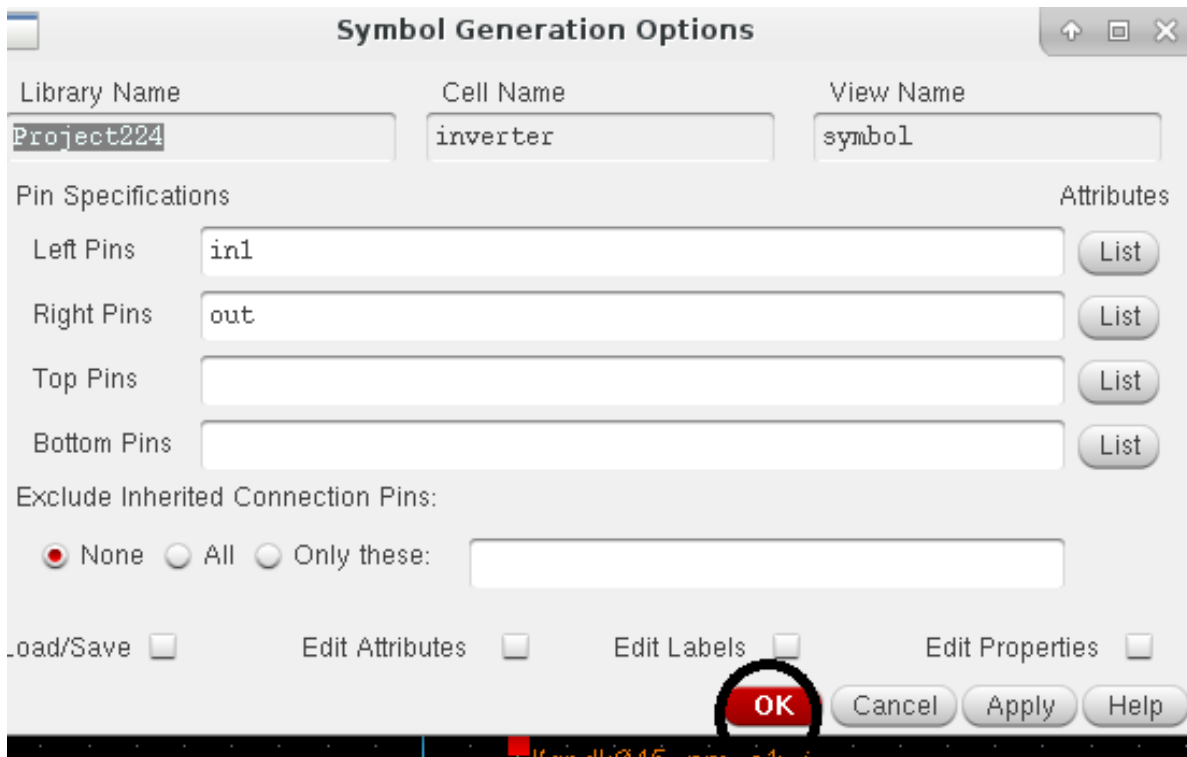
Now we have to create instance
For this click on create<cellview<from cellview



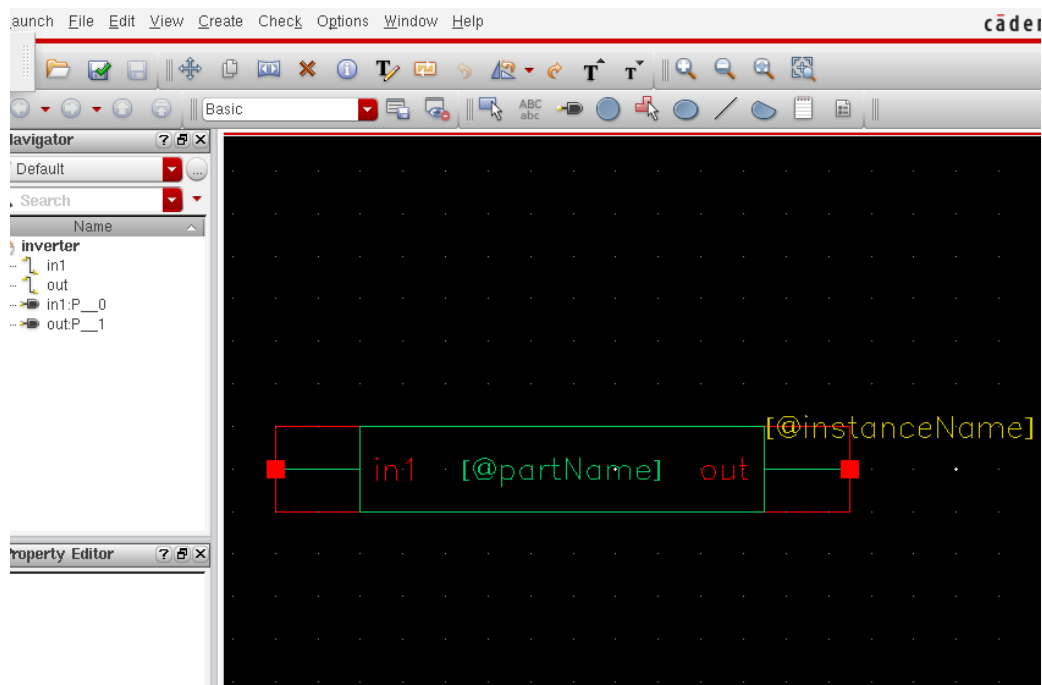
Click ok



Click ok.



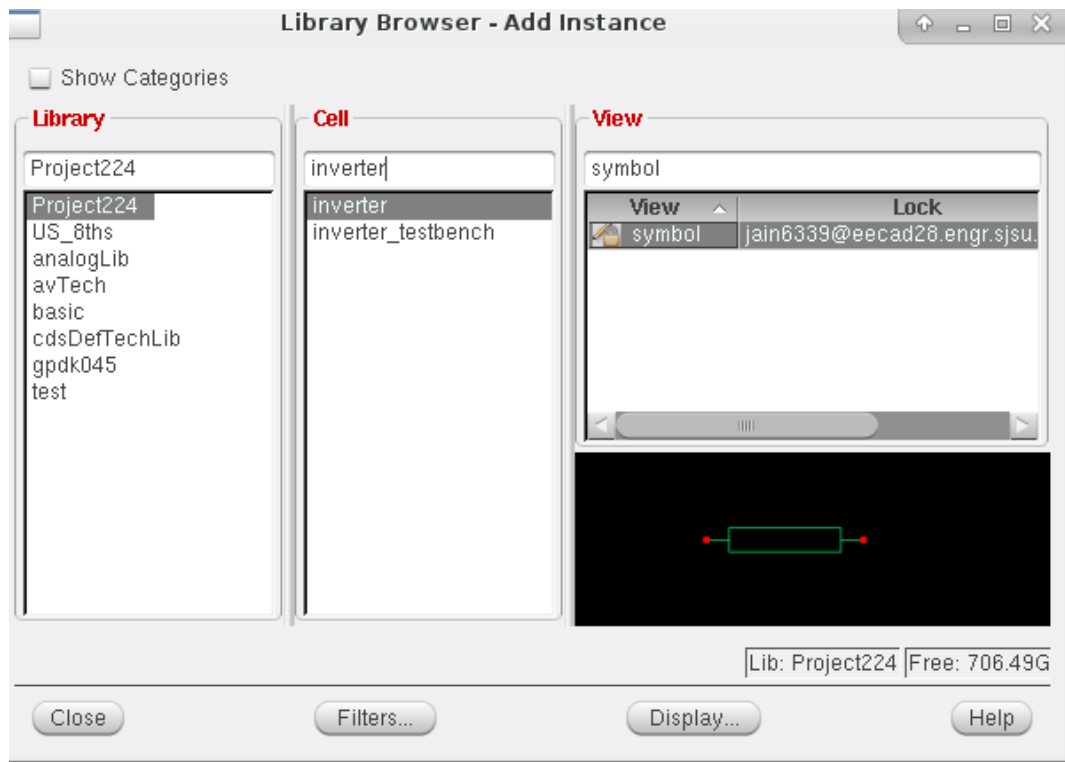
Instance will be created as shown below.



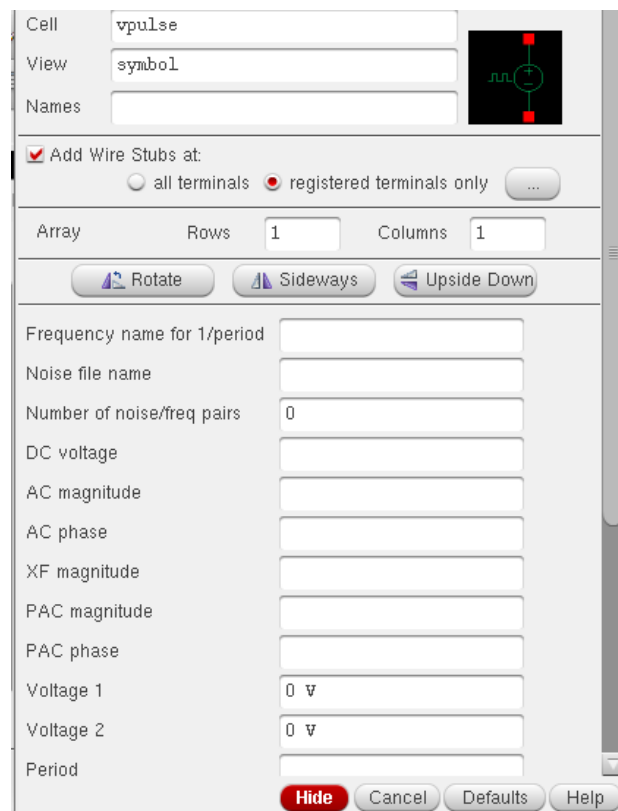
Close this window and open a new cell and name it (inverter_testbench in this case)

Again click on instance in the toolbar and select the library

Project224<inverter<symbol and click on close.



For the input select vpulse from the library.
And click on Hide.



For the supply select vdd, gnd and vdc from the analoglibrary

The 'Add Instance' dialog box is shown with the following settings:

- Library: analogLib
- Cell: vdd
- View: symbol
- Names: (empty)
- ☒ Add Wire Stubs at:
 - ☐ all terminals
 - ☒ registered terminals only
- Array: Rows 1, Columns 1
- Buttons: Rotate, Sideways, Upside Down

A small preview window on the right shows a red square terminal connected to a green wire.

The 'Add Instance' dialog box is shown with the following settings:

- Library: analogLib
- Cell: vdc
- View: symbol
- Names: (empty)
- ☒ Add Wire Stubs at:
 - ☐ all terminals
 - ☒ registered terminals only
- Array: Rows 1, Columns 1
- Buttons: Rotate, Sideways, Upside Down

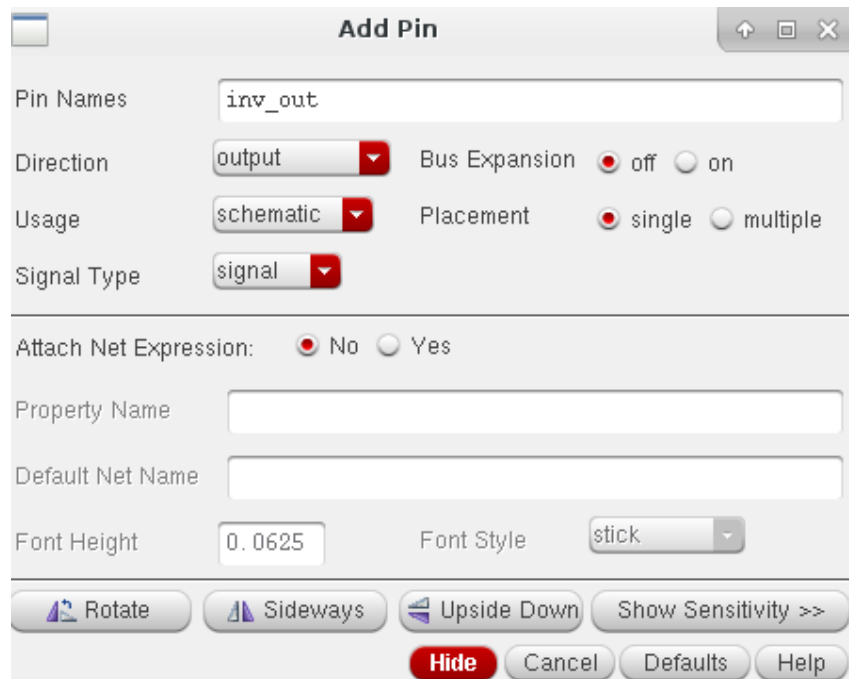
A small preview window on the right shows a green circle terminal with a red square at the top and bottom.

Below the array settings, there are several input fields for noise and temperature parameters:

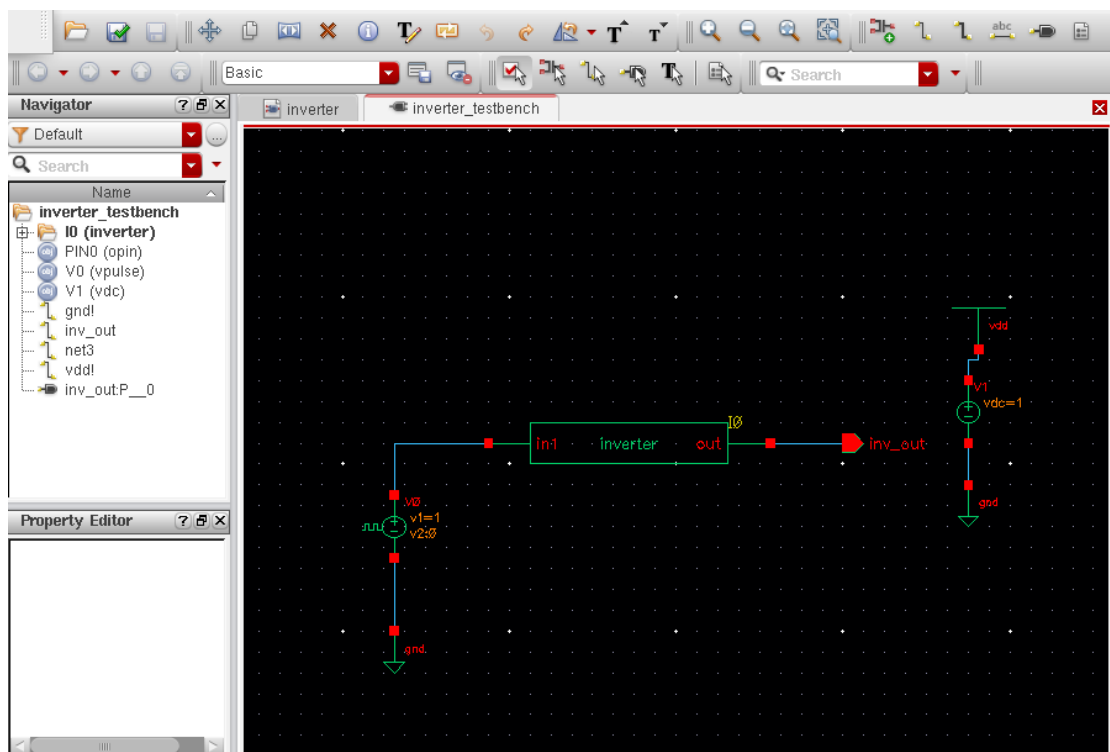
- Noise file name: (empty)
- Number of noise/freq pairs: 0
- DC voltage: 1 V
- AC magnitude: (empty)
- AC phase: (empty)
- XF magnitude: (empty)
- PAC magnitude: (empty)
- PAC phase: (empty)
- Temperature coefficient 1: (empty)
- Temperature coefficient 2: (empty)
- Nominal temperature: (empty)

At the bottom, there are buttons: Hide, Cancel, Defaults, and Help.

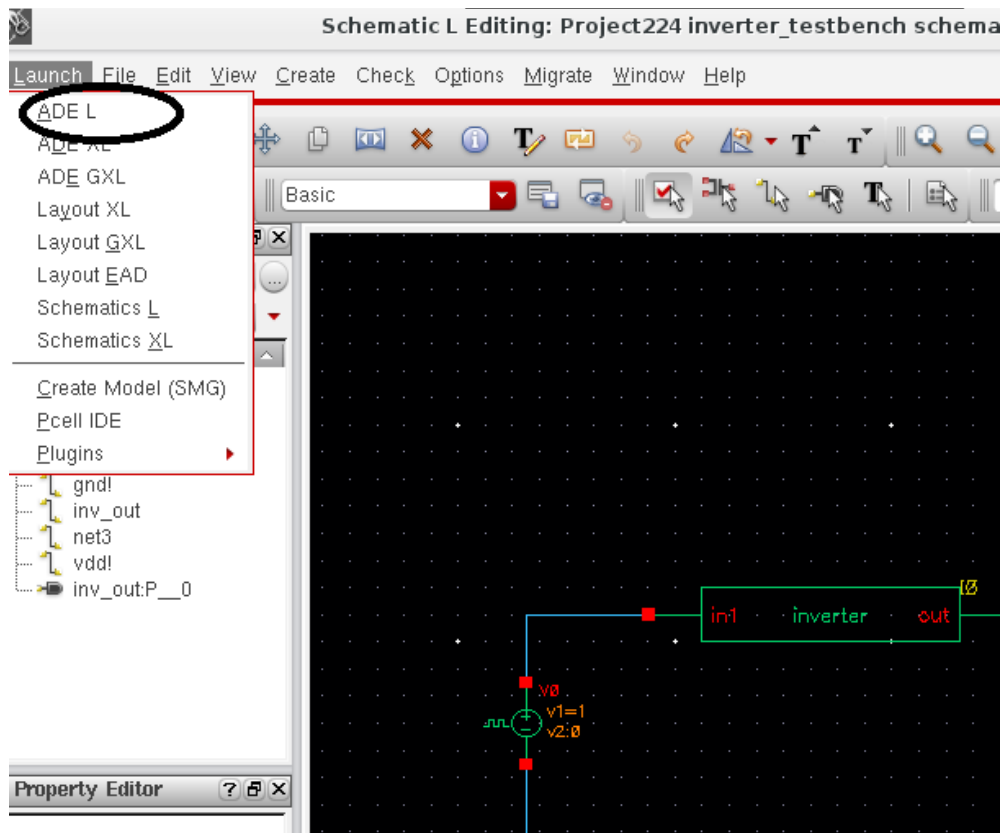
Change the dc voltage to 1volt to bias the circuit.



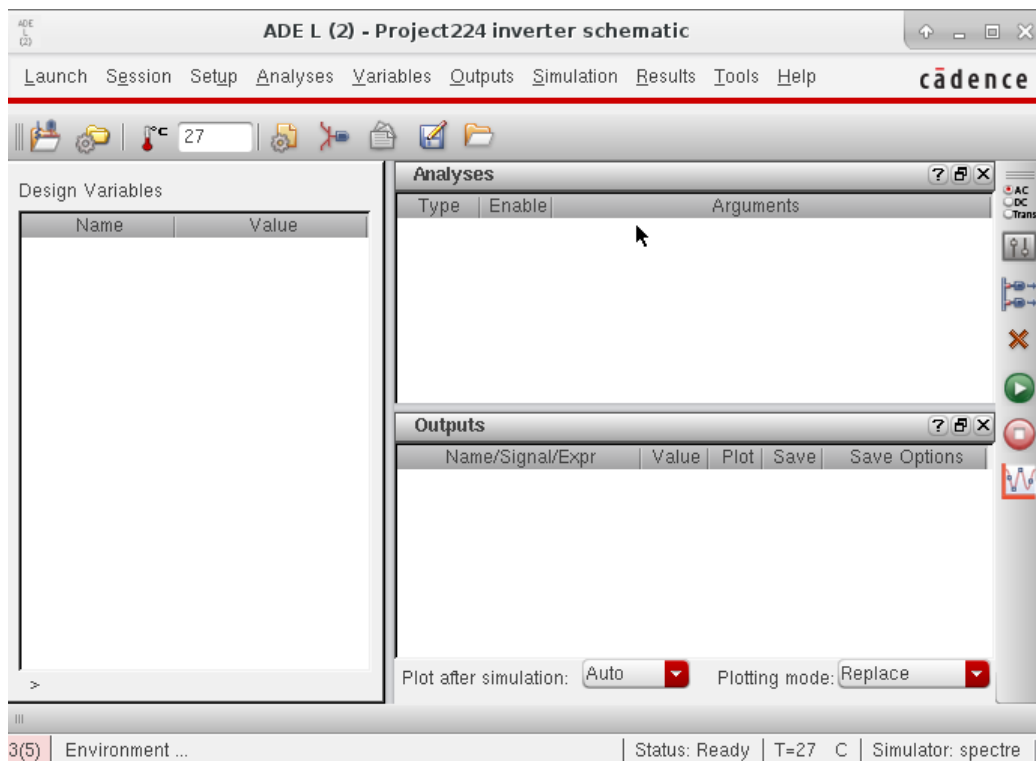
Add output pin to the circuit as done before and name the pin.



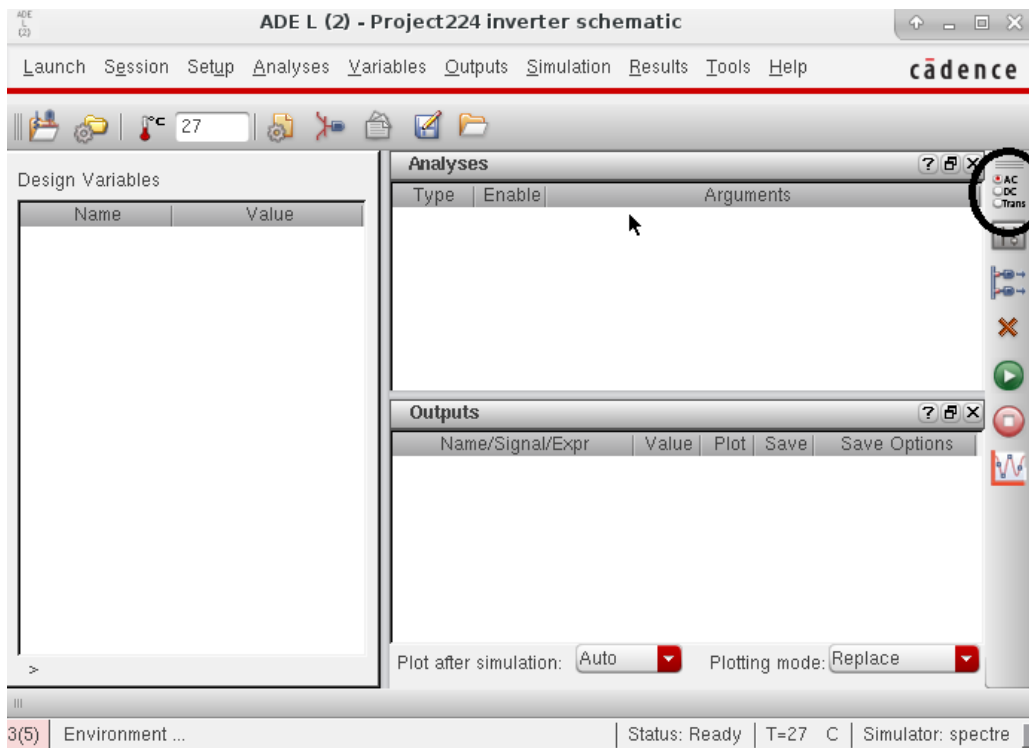
This is the complete circuit.



Click launch<ADE L
Following window will open

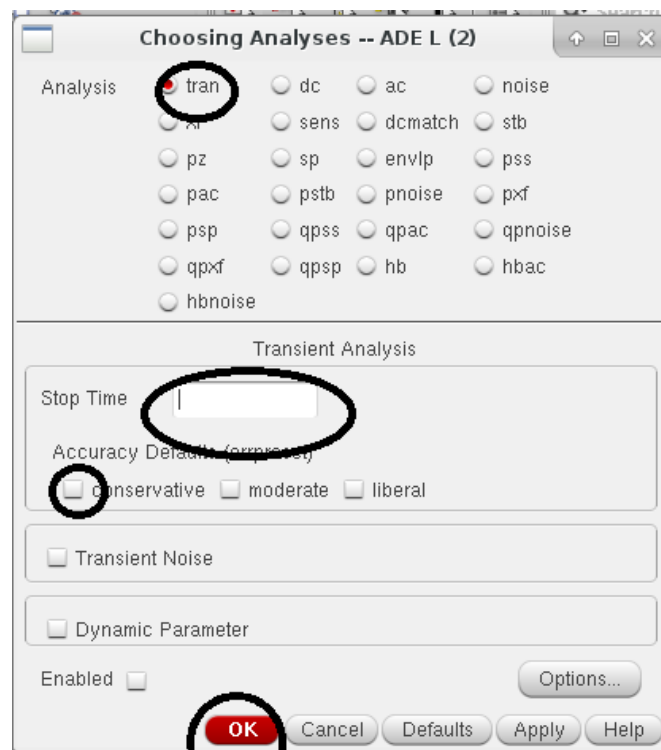


Click on selected icon highlighted by black circle.



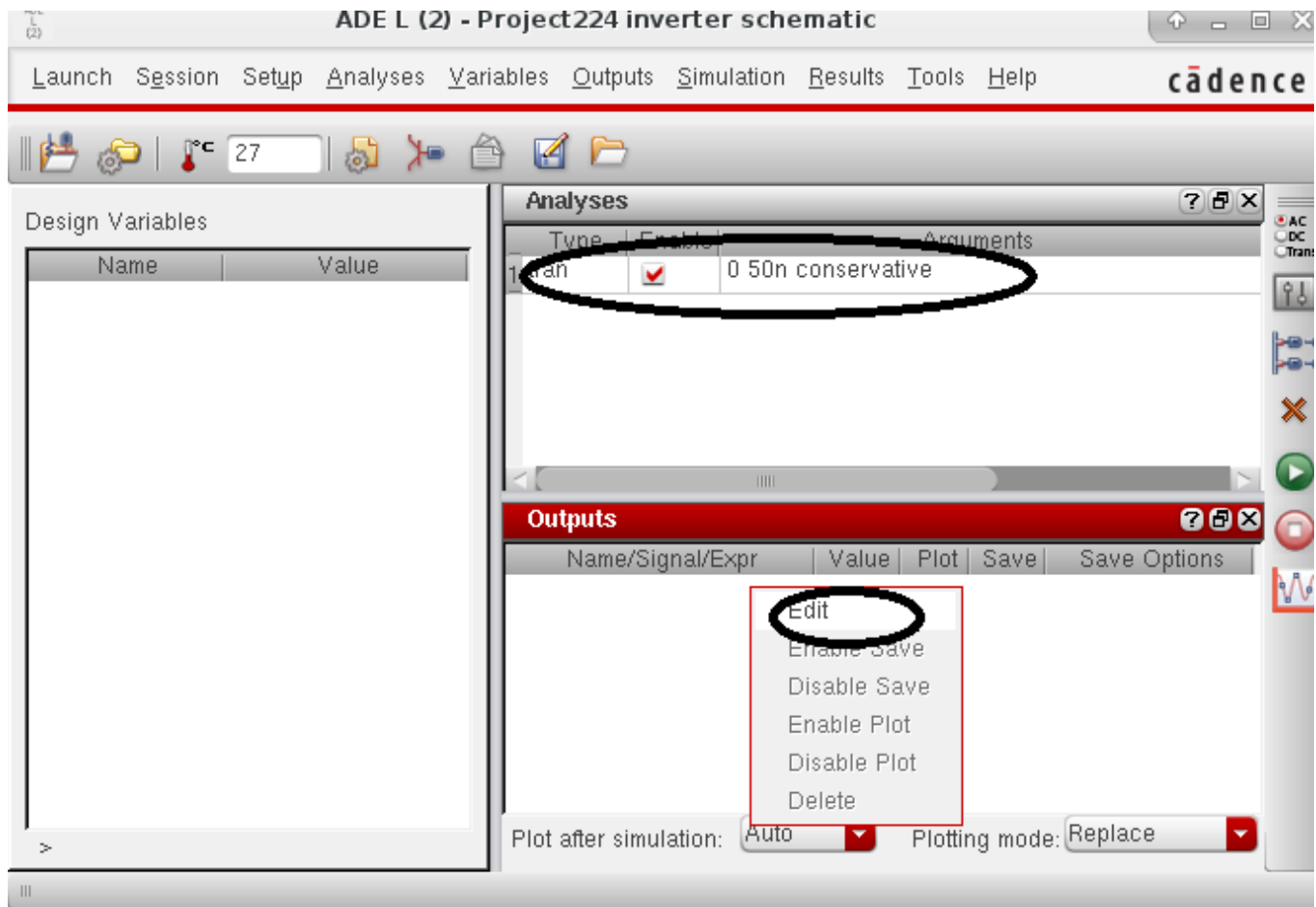
Following screen will open

As we are doing transient analysis select the “trans”. Enter the stop time let say 100nsec here
And check the conservative box and click ok.



Go back to the ADE launch cell. You will notice an input is added in the analyses block

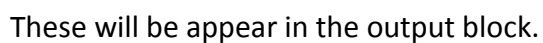
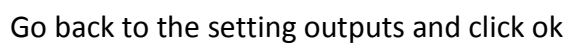
Right click in the output tab. Click on the edit (highlighted with black circle).

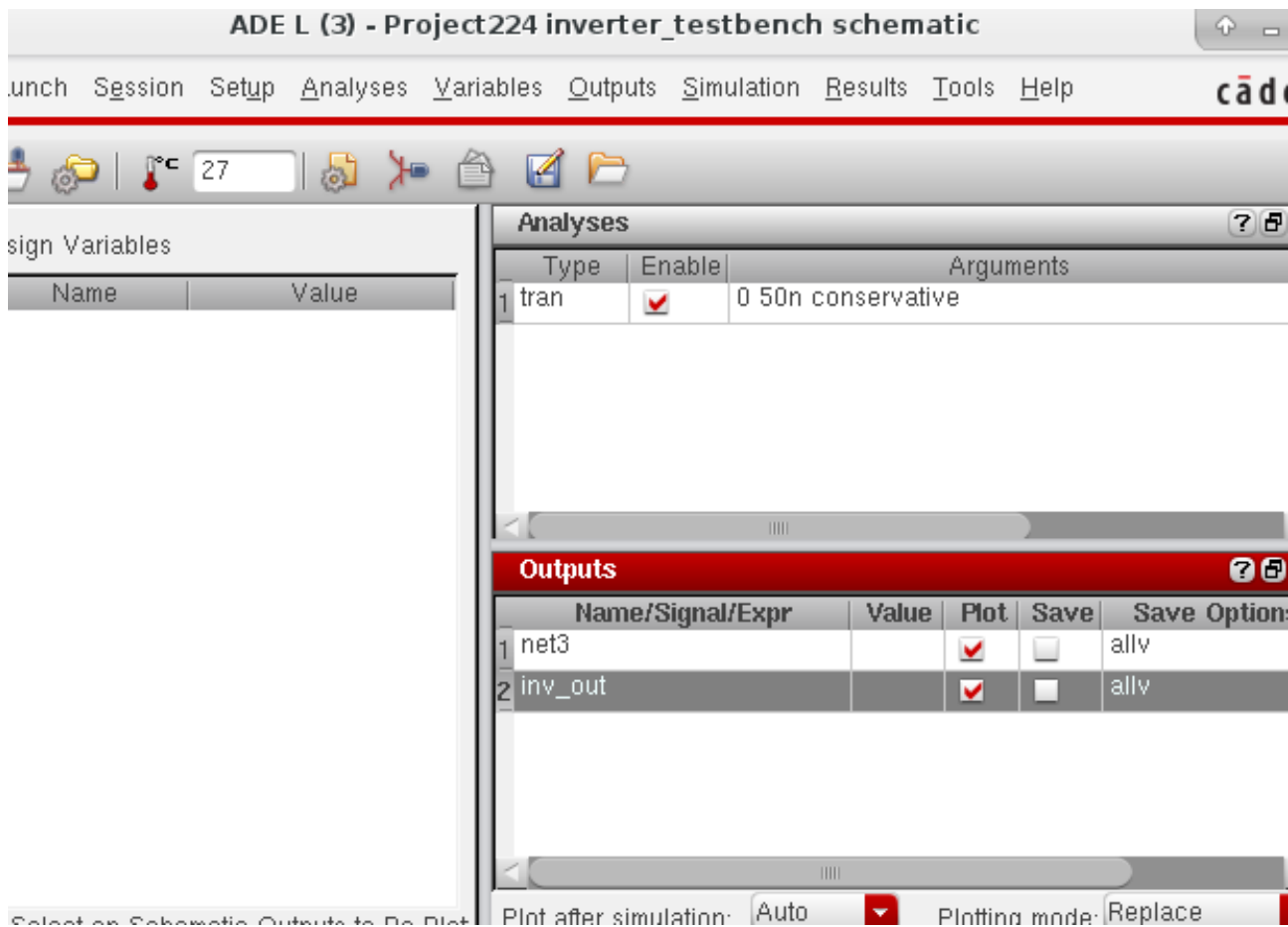


Following screen will open

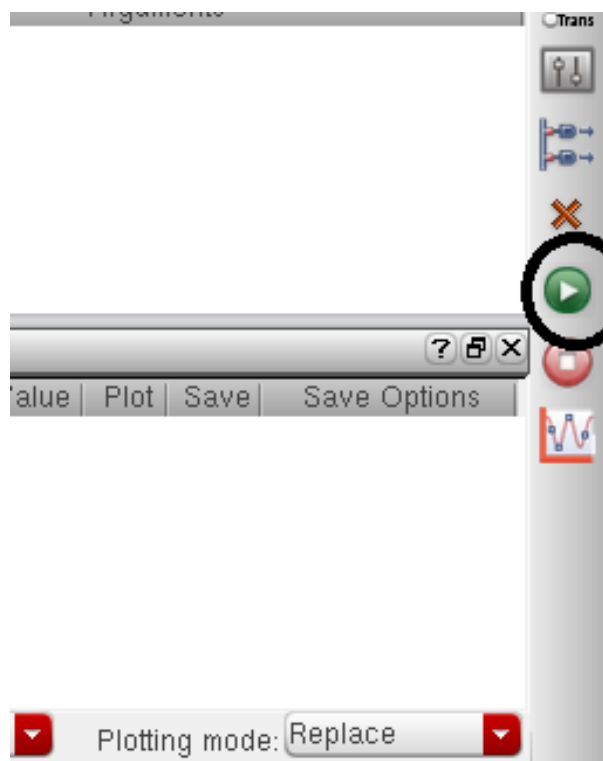


Click on From Schematic and go back to Schematic
Select the input and output wire on the schematic.

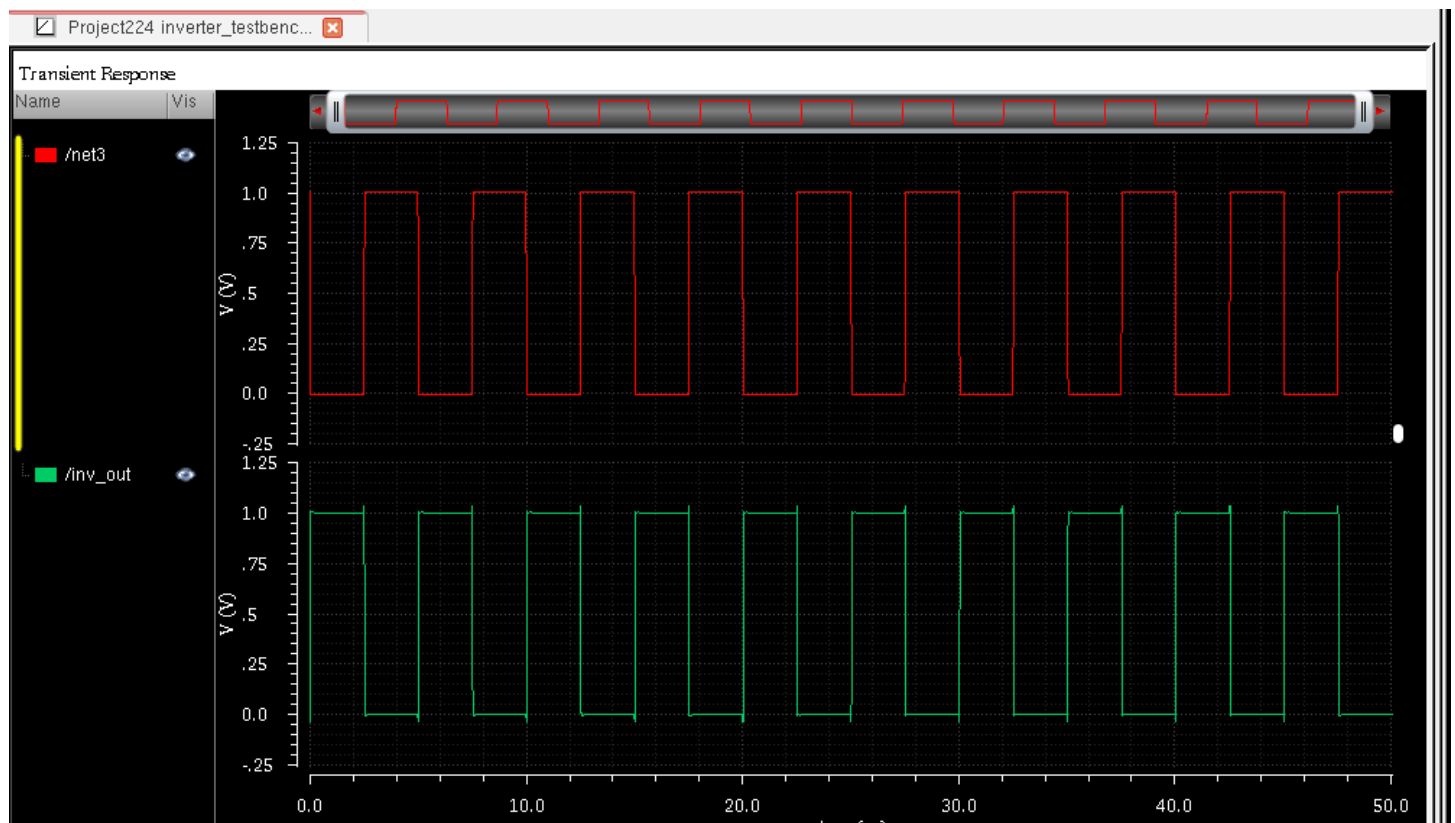




Click on the green play button to simulate (highlighted with black circle).

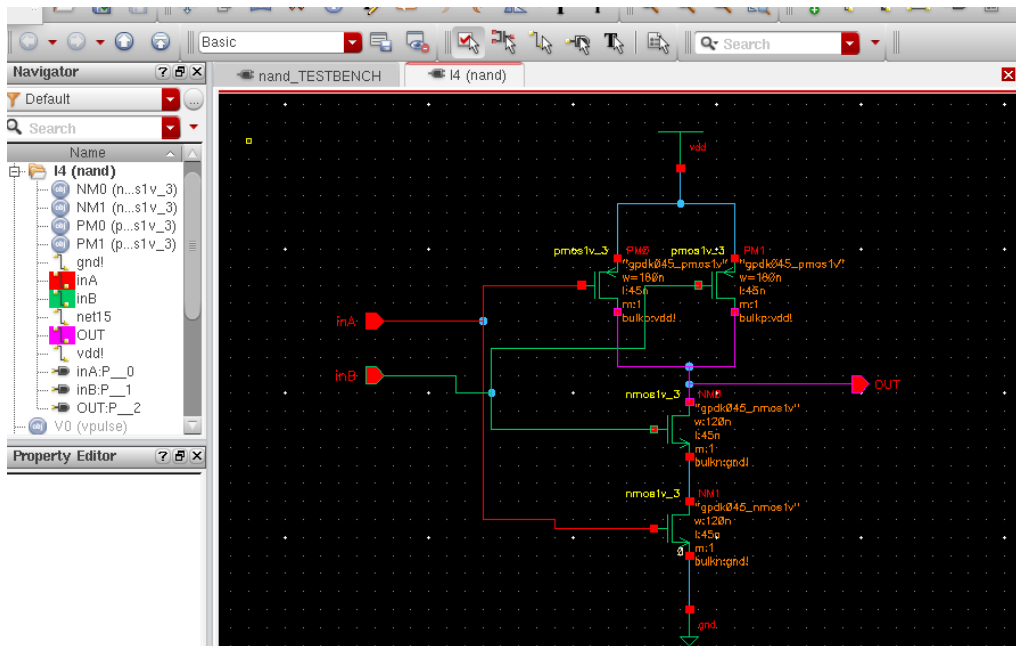


We will get the output.

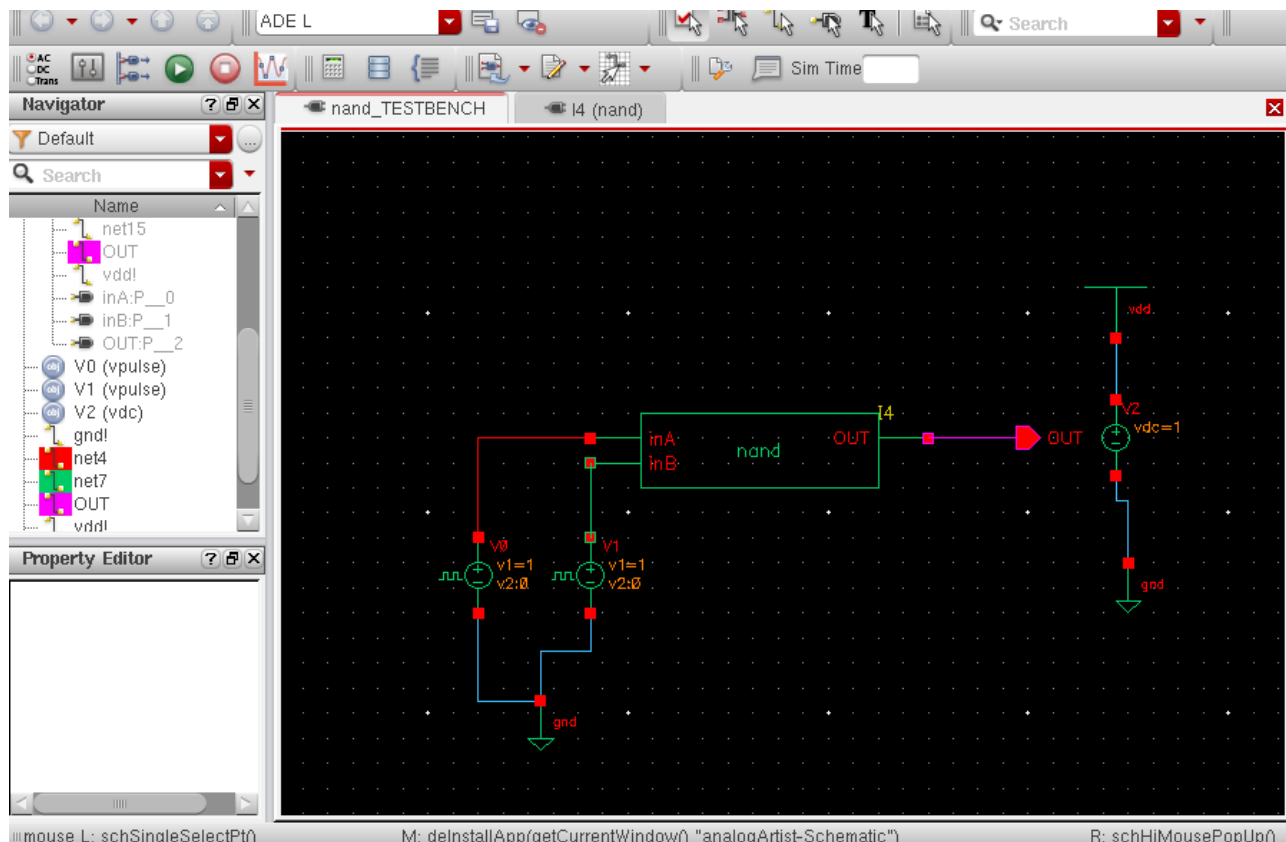


Implementation of NAND gate

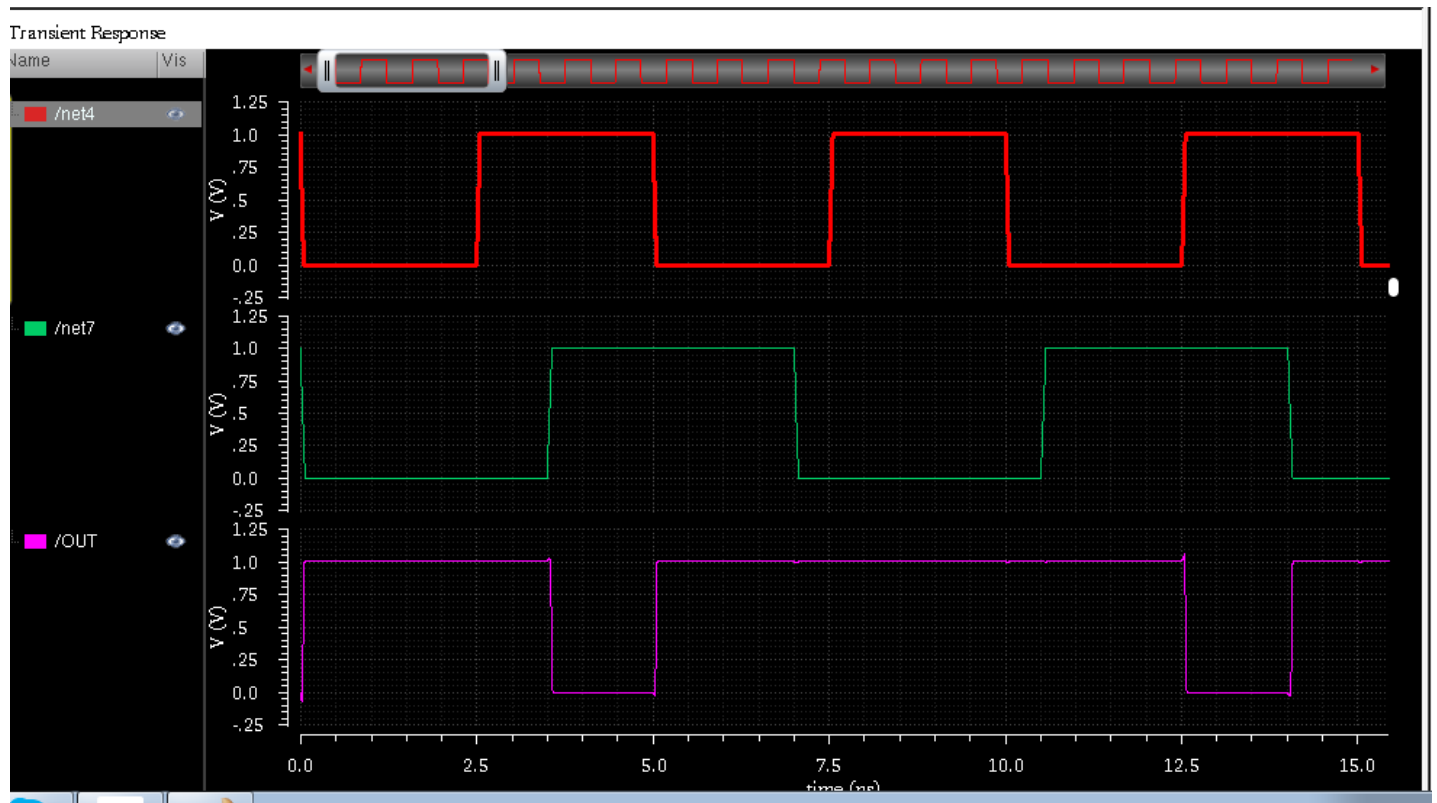
First make the circuit of nand gate by following same step as to make the inverter.



Implement the test bench for the NAND gate following the same steps as for inverter.

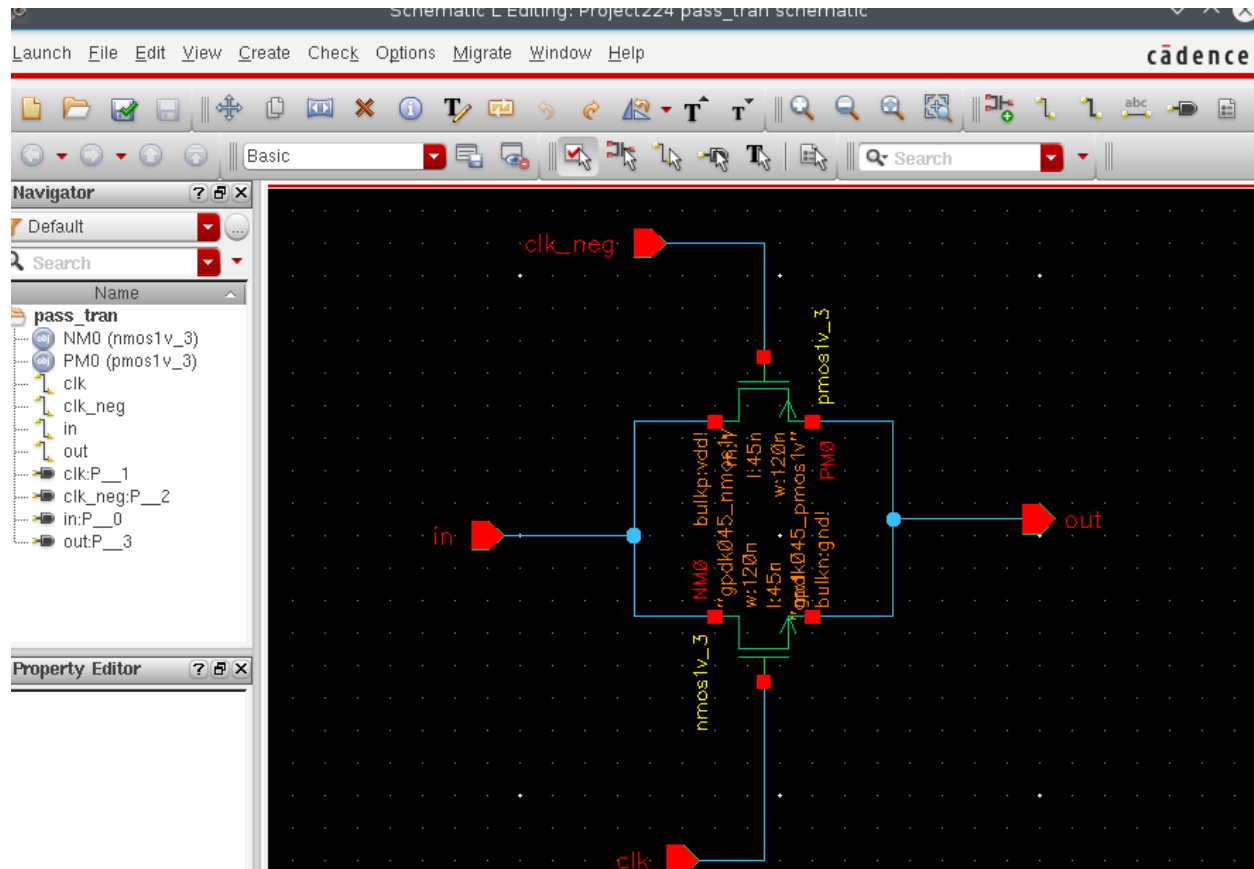


Simulate the output using the same steps as for inverter.
Output will appear as shown below

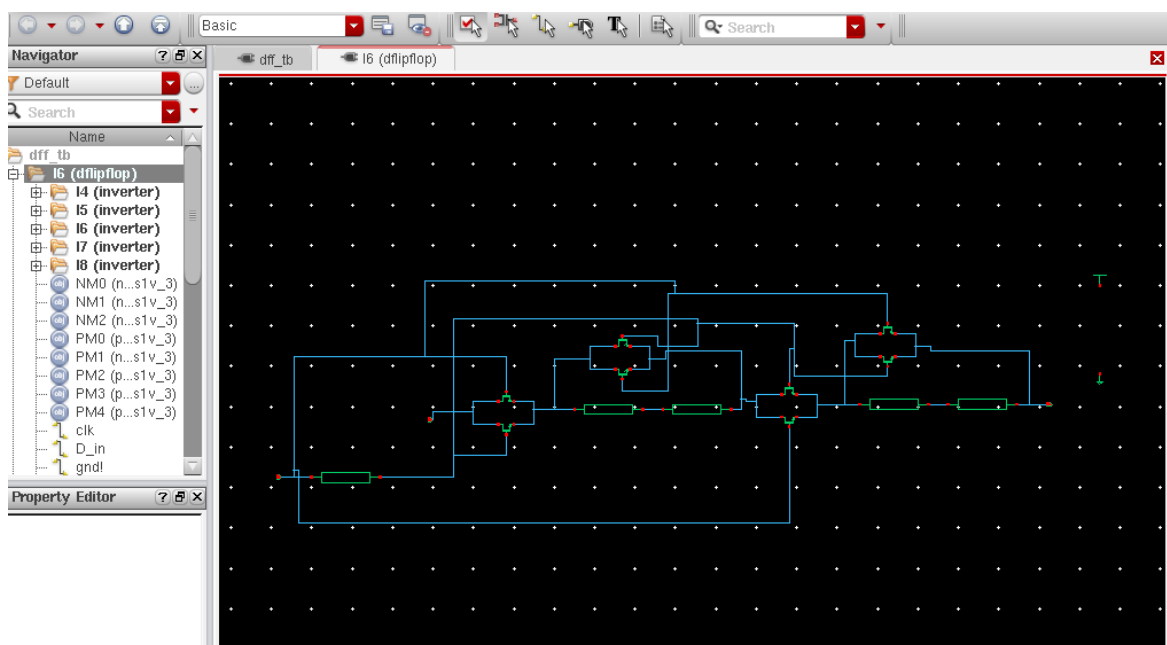


Implementation of Master-slave Flipflop

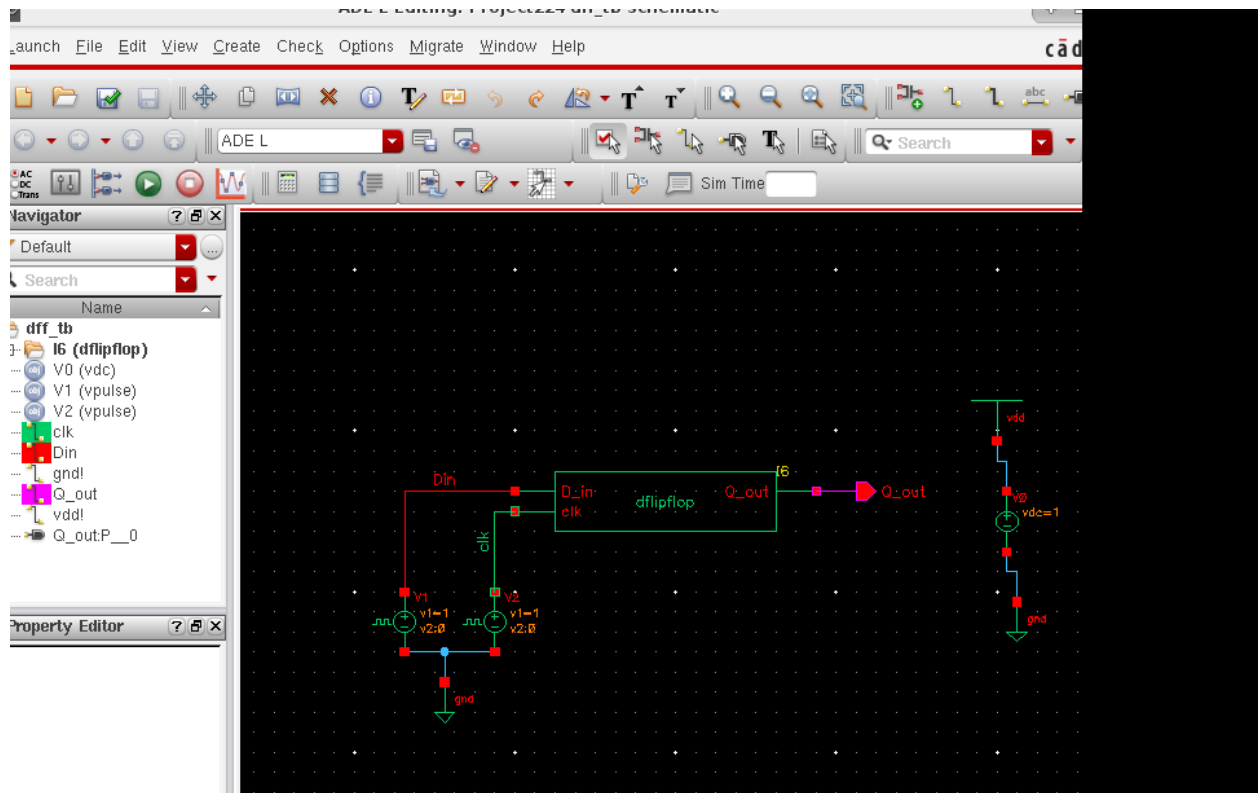
For this we first have to make a pass transistor following the same steps as above.



For making Master-slave D-flipflop we use pass transistor and inverter instance.
Following circuit will be implemented



Prepare testbench for the flipflop (following the same steps)



After making the circuit, Output will be simulated and will be appeared as follows

