EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 10: SC and Bootstrapped Clock Circuits

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ENG-259

Course Schedule – Subject to Change

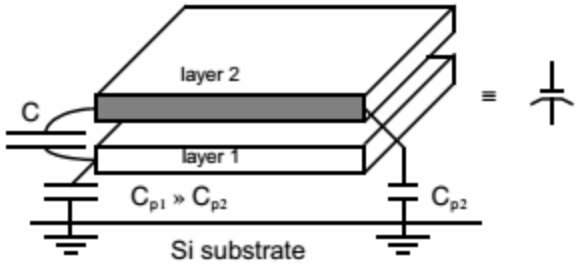
Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	~~Finish Flash ADC~~
28-Feb	DAC Architectures - Resistor, R-2R
5-Mar	DAC Architectures - Current steering, Segmented
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

S&H and Bootstrap circuits

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

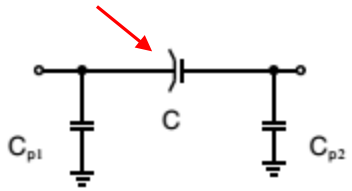
Basic Building Blocks of Switched-Capacitor Circuits

- OPAMP (OTA)
- Capacitor
- Switch
- Clock



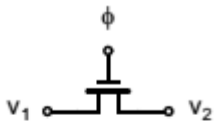
(a)

Bottom Plate

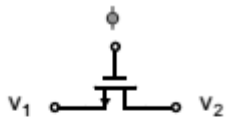


$C_{p1} > C_{p2}$

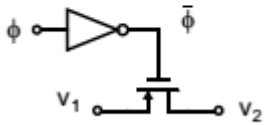
(b)



(a)



(b)



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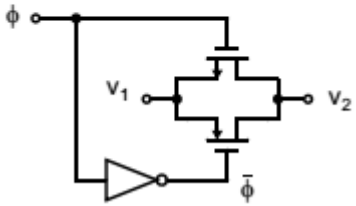

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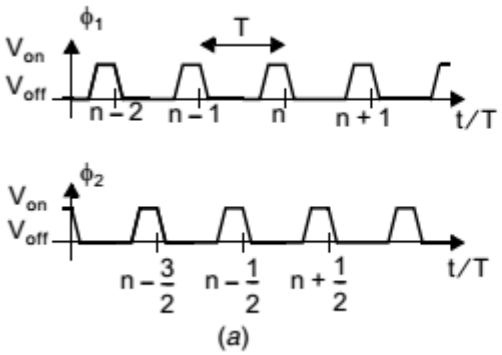
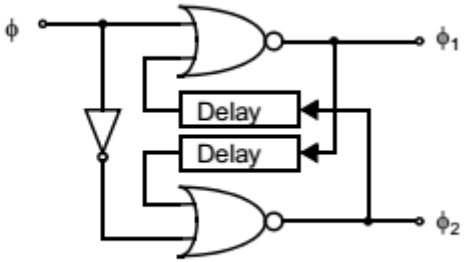


(a)

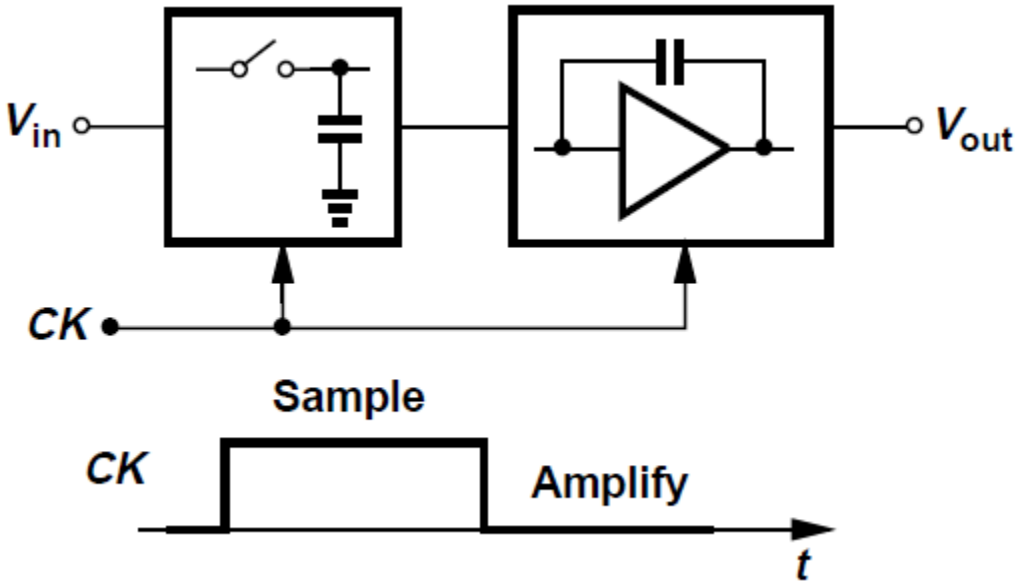
$f_s \equiv \frac{1}{T}$



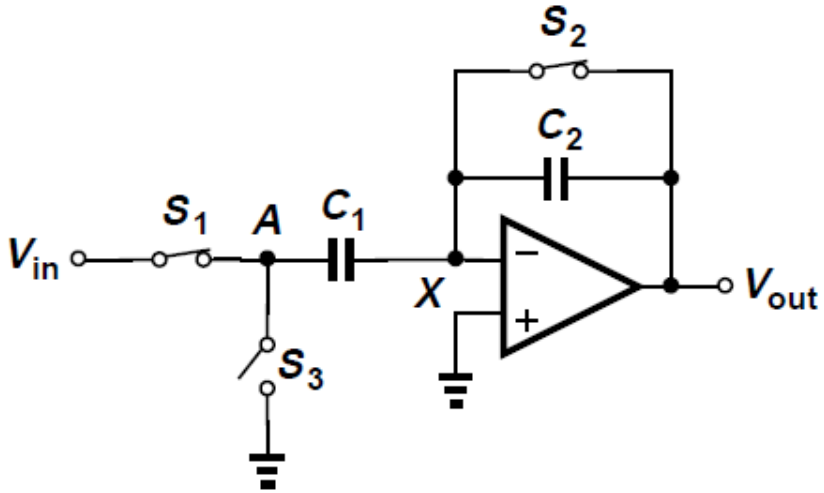
(b)

General Considerations

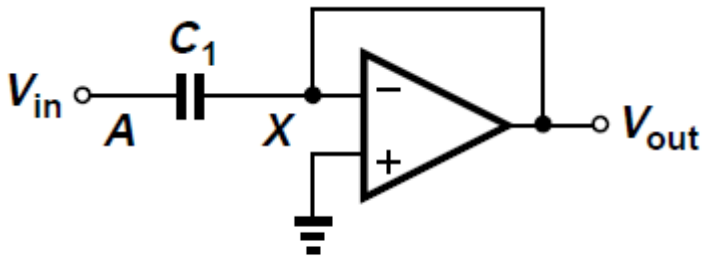
- Switched-capacitor amplifiers operate in two phases: Sampling and Amplification
- Clock needed in addition to analog input V_{in}



SC Amplifier



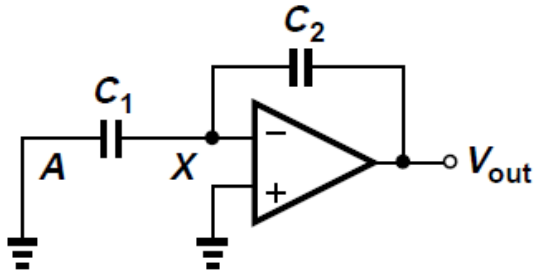
S_1, S_2 on, S_3 off



(a)

Sampling Phase

S_1, S_2 off, S_3 on

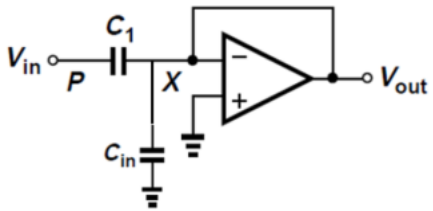


(b)

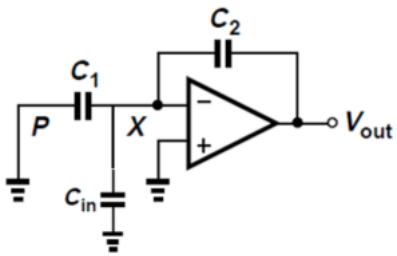
Amplifying Phase

SC Amplifier

Ø1

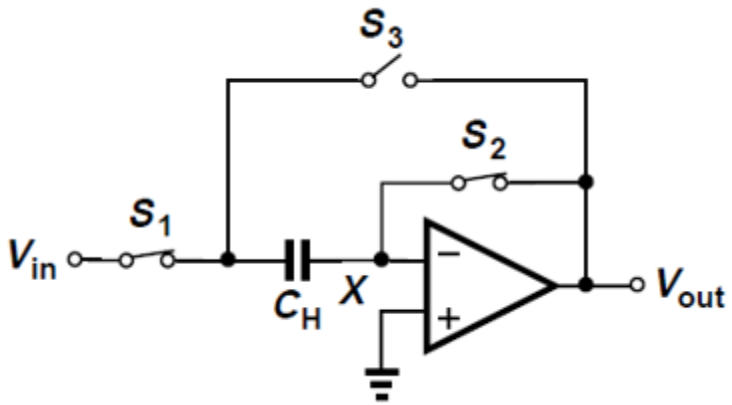


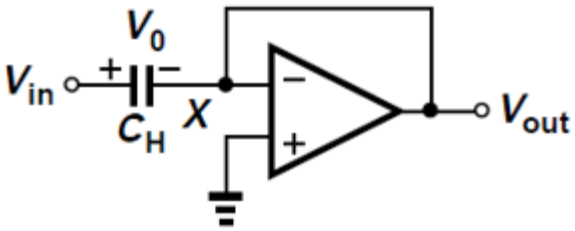
Ø2



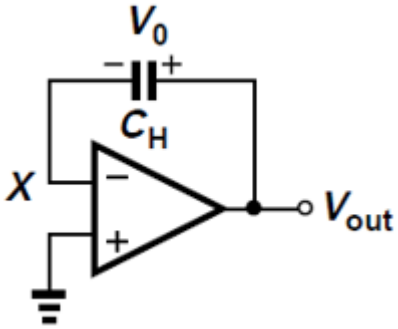
$$Q_1 = C_1(0 - V_{in})$$
$$Q_2 = (C_1{+}C_{in})V_x + C_2(V_x - V_{out})$$
$$V_x = \frac{V_{out}}{-A}$$
$$Q_1 = Q_2$$
$$C_1(0 - V_{in}) = (C_1{+}C_{in})V_x + C_2(V_x - V_{out}) = (C_1{+}C_{in})\left(\frac{V_{out}}{-A}\right) + C_2\left(\frac{V_{out}}{-A} - V_{out}\right)$$
$$-C_1V_{in} = -C_1\frac{V_{out}}{A} - C_{in}\frac{V_{out}}{A} - C_2\frac{V_{out}}{A} - C_2V_{out}$$
$$C_1V_{in} = \left(\frac{C_1 + C_{in} + C_2}{A} + C_2\right)V_{out} = C_2\left(\frac{C_1 + C_{in} + C_2}{C_2A} + 1\right)V_{out} = C_2\left(\frac{1}{\beta A} + 1\right)V_{out}$$
$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2\left(\frac{1}{\beta A} + 1\right)} \approx \frac{C_1}{C_2}\left(1 - \frac{1}{\beta A}\right)$$

Sample and Hold Amplifier – Flip Around S/H





Sample



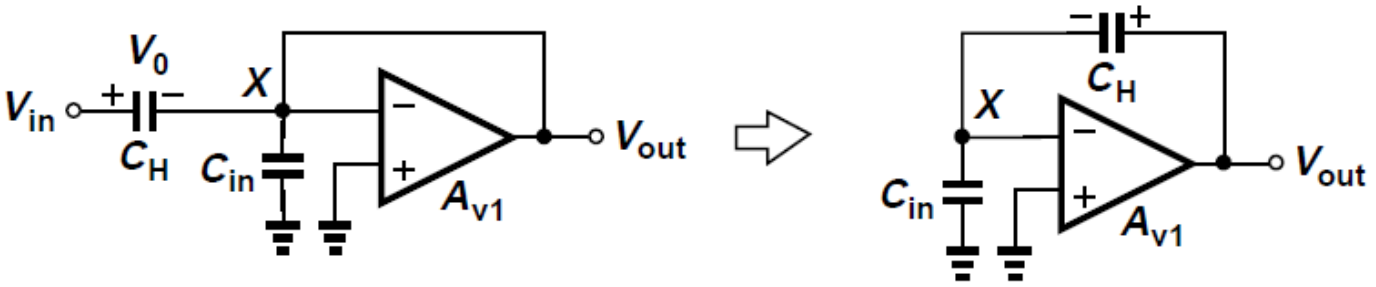
Amplify

Flip Around S/H

Precision Considerations:

- Output in amplification mode

Flip Around Sample & Hold

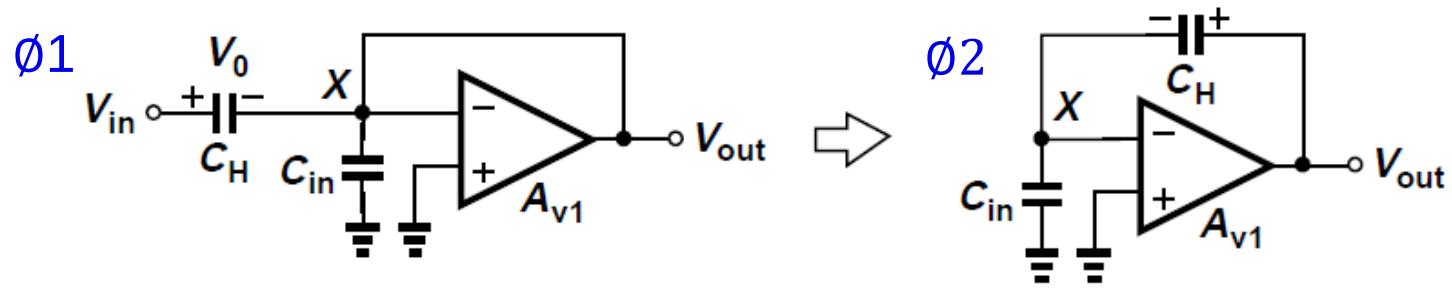


$$V_{out} = \frac{V_0}{1 + \frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H} + 1\right)}$$

$$\approx V_0\left[1 - \frac{1}{A_{v1}}\left(\frac{C_{in}}{C_H} + 1\right)\right]$$

Derive this using charge conservation

Flip Around S/H



Charge conservation during Ø1 and Ø2

During Ø1, total charge at node X is $Q1 = C_H(0-V_{in})$

During Ø2, total charge at node X is $Q2 = C_{in}V_x + C_H(V_x-V_{out})$

Let Q1 = Q2

$-V_{in}C_H = C_{in}V_x + C_H(V_x-V_{out}) = (C_{in} + C_H)V_x - C_HV_{out}$

$V_x(-A_{v1}) = V_{out}$

$-V_{in}C_H = (C_{in} + C_H)(-V_{out}/A_{v1}) - C_HV_{out}$

$V_{in}C_H = (C_{in} + C_H)(V_{out}/A_{v1}) + C_HV_{out}$

$V_{in}C_H = [(C_{in} + C_H)/A_{v1} + C_H]V_{out}$

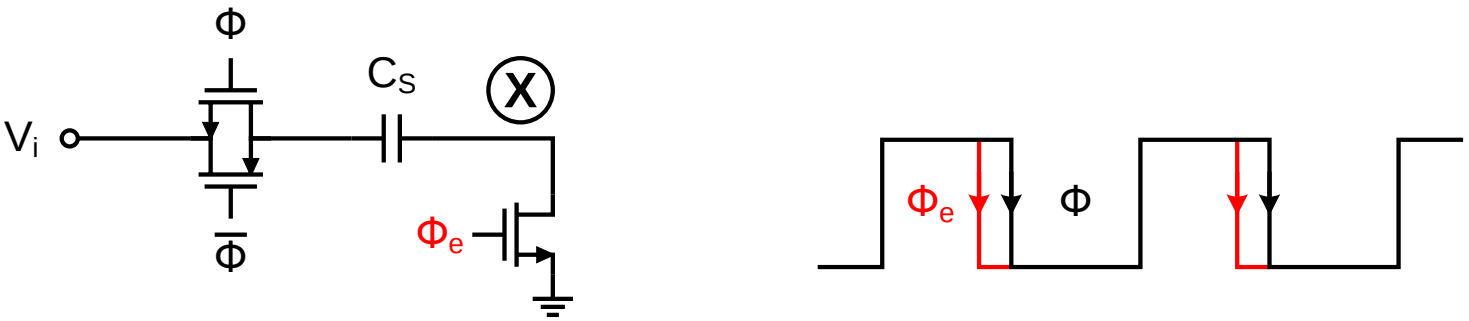
$V_{in} = [(C_{in} + C_H)/(C_HA_{v1}) + 1]V_{out}$

$V_{out}/V_{in} = 1/[(C_{in} + C_H)/(C_HA_{v1}) + 1] = 1/[1 + 1/(\beta A_{v1})]$

$$\beta = \frac{C_H}{C_H + C_{in}}$$

$$V_{out} \approx V_0\left[1 - \frac{1}{\beta A_{v1}}\right]$$ ← *To reduce gain error, Increase βA_V*

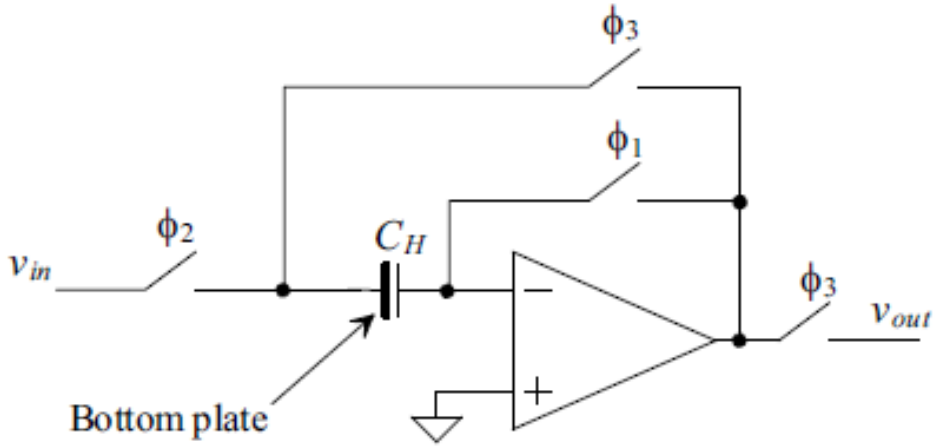
Bottom-Plate Sampling

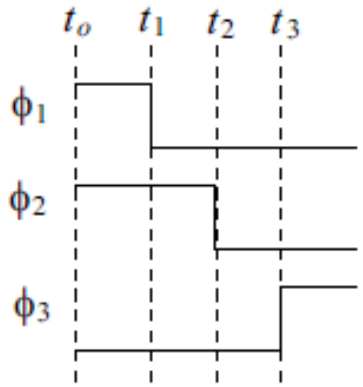


- AC-ground switch opens slightly earlier than input switches
- Signal-independent CF and CI of switch Φ_e to the first order!
- Input switch can be further bootstrapped
- Typical for applications of more than 8-bit resolution

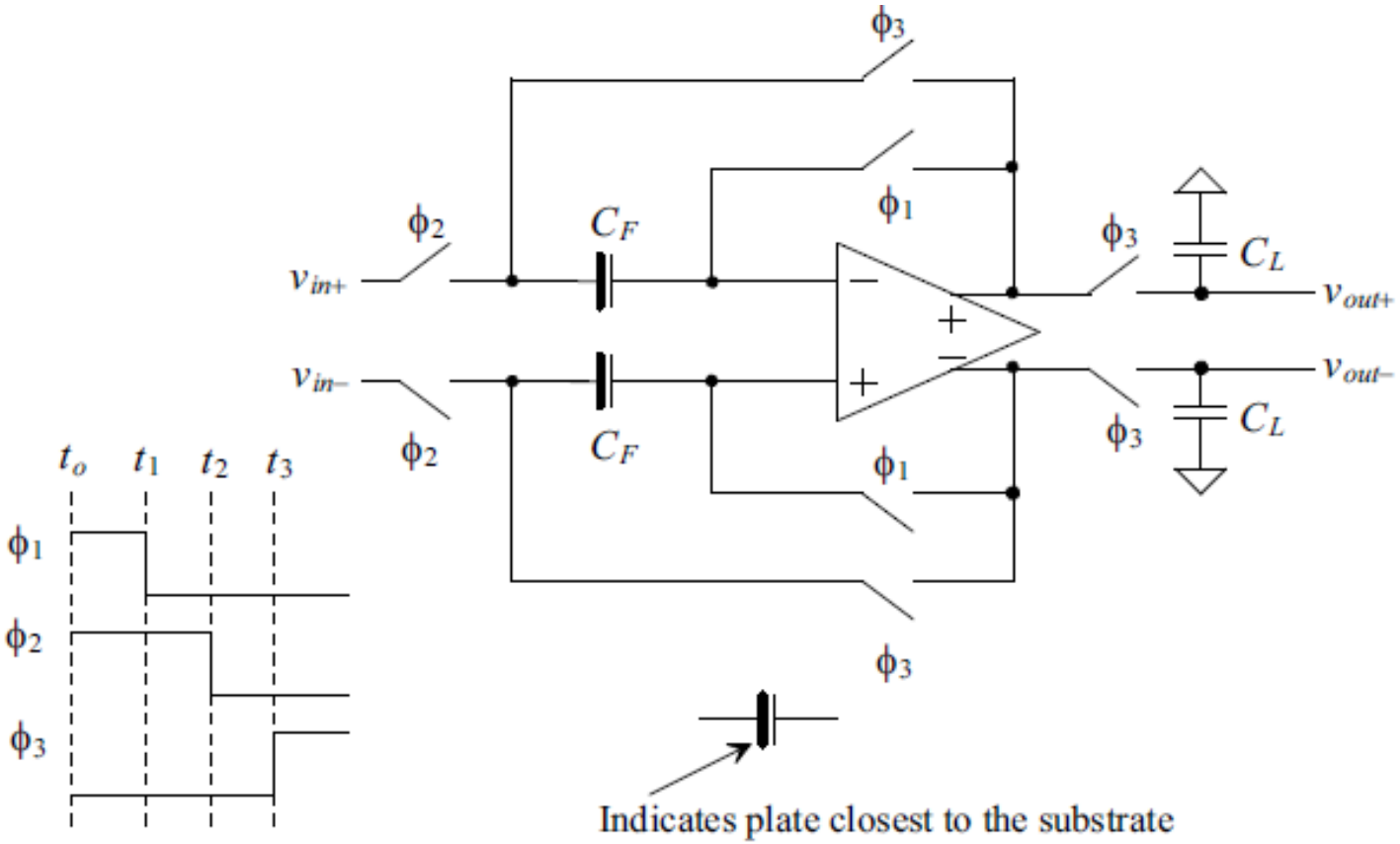
- Less tracking bandwidth due to more switches in series
- Signal swing at node X is not entirely zero!

SHA Timing for Bottom Plate Sampling

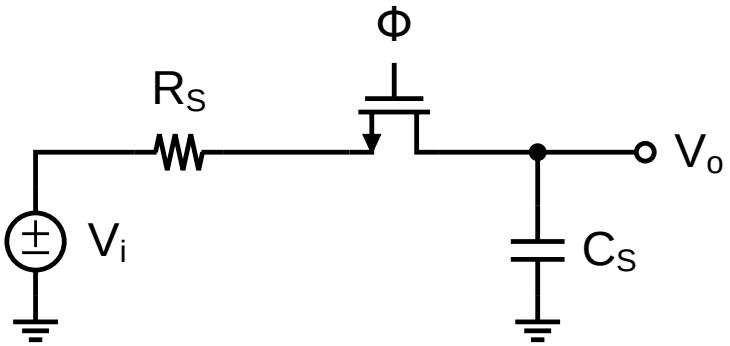




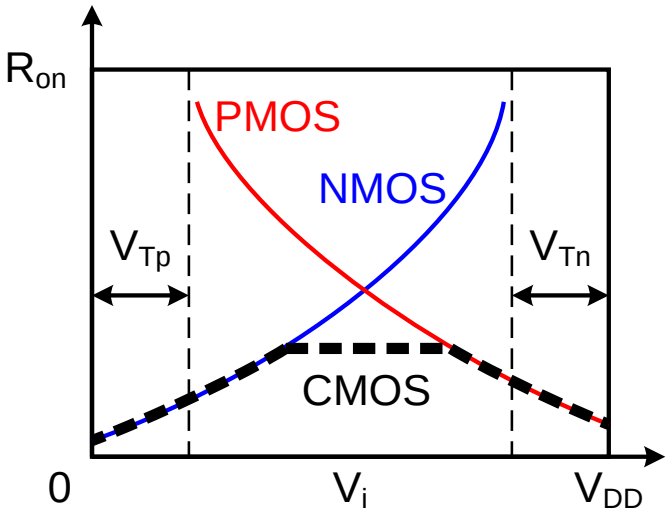
Fully Differential S/H



Recap: Signal-Dependent Switch Ron

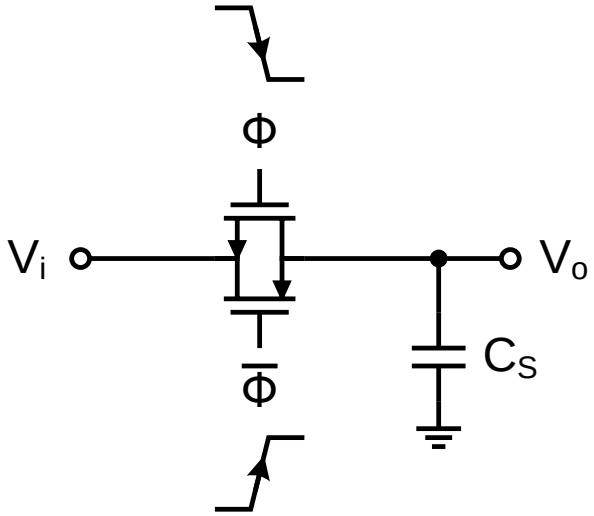


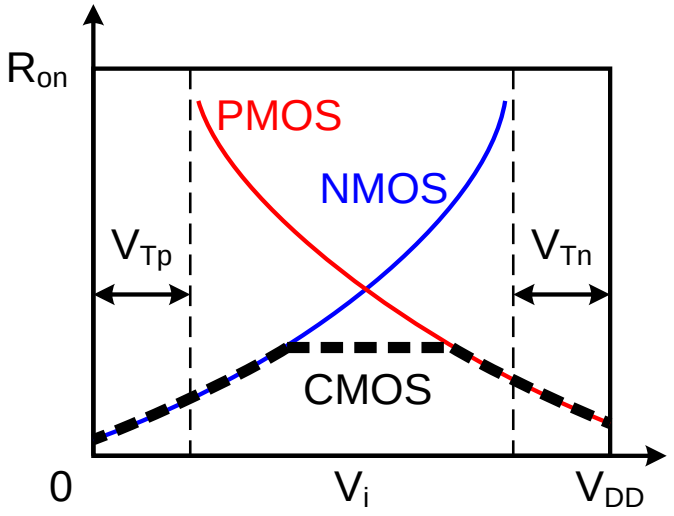
$$R_{on}^{-1} = \mu C_{ox} \frac{W}{L}\left(V_{DD} - V_{th} - V_i\right)$$



- Signal-dependent R_{on} → signal-dependent TBW → extra waveform distortion
- Neither signal-dependent R_{on} nor dispersion is of concern if TBW is sufficiently large (>> f_{in}, depending on the target accuracy)

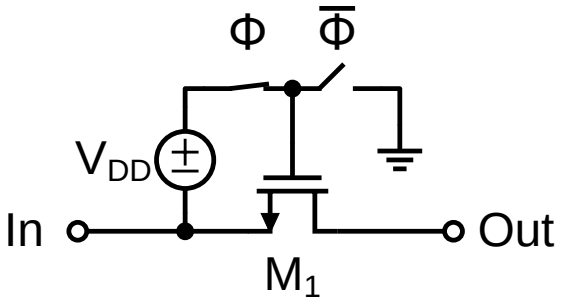
Recap: CMOS Switch

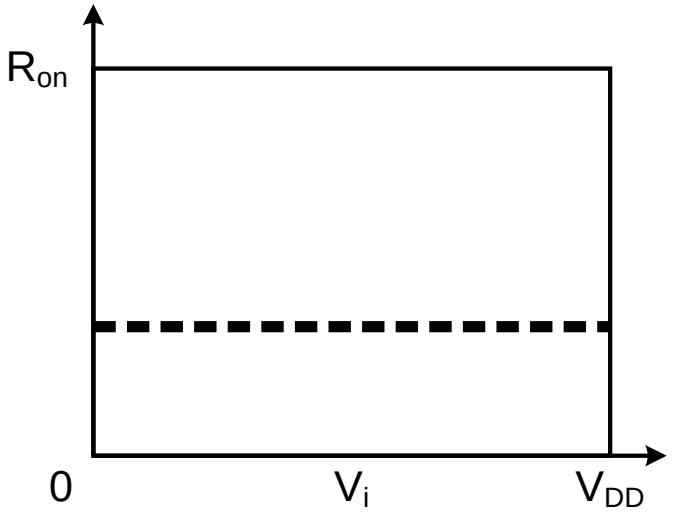




- R_{on} still depends on V_{in} and is sensitive to N/P mismatch
- Large parasitic cap due to PMOS switch for symmetric R_{on}
- Clock rising/falling edge alignment

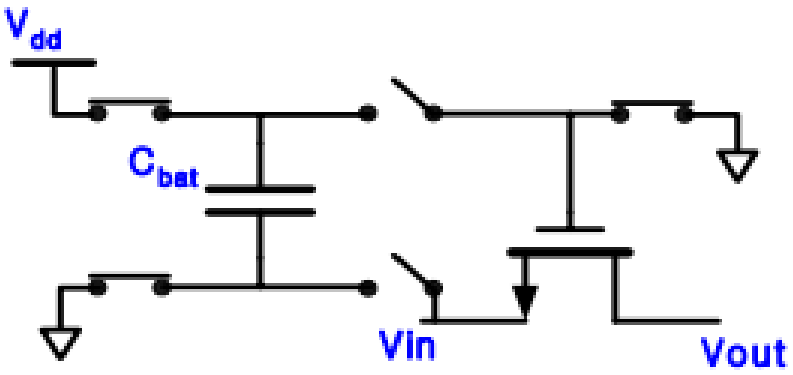
Clock Bootstrapping



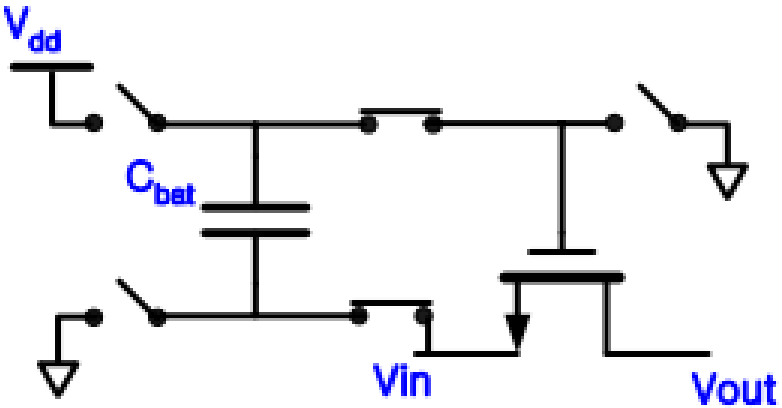


- Constant gate overdrive voltage $V_{GS} = V_{DD}$ for the switch
- R_{on} is not dependent on V_{in} to the first order (body effect?)
- NMOS device only with less parasitic capacitance

Clock Bootstrapping



(a)

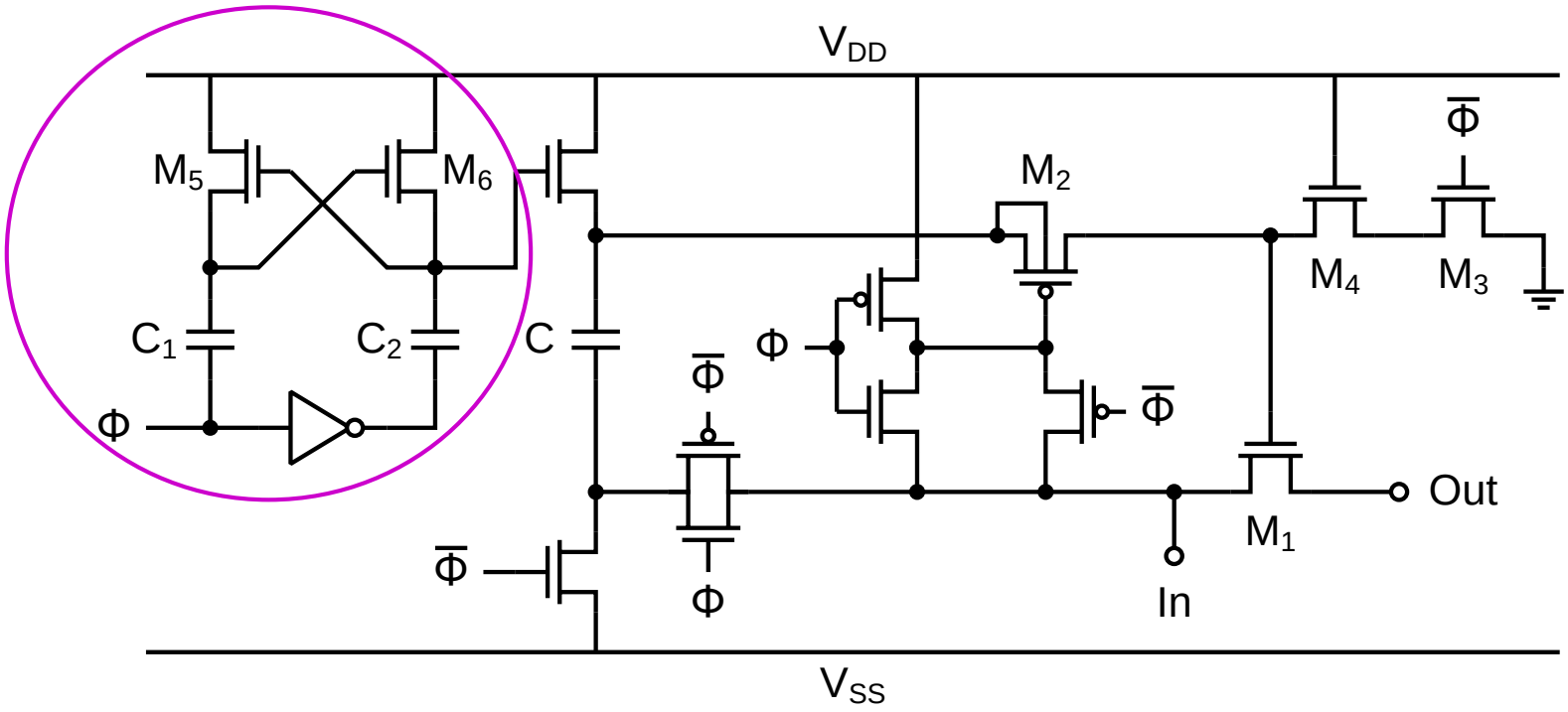


(b)

Clock Bootstrapping

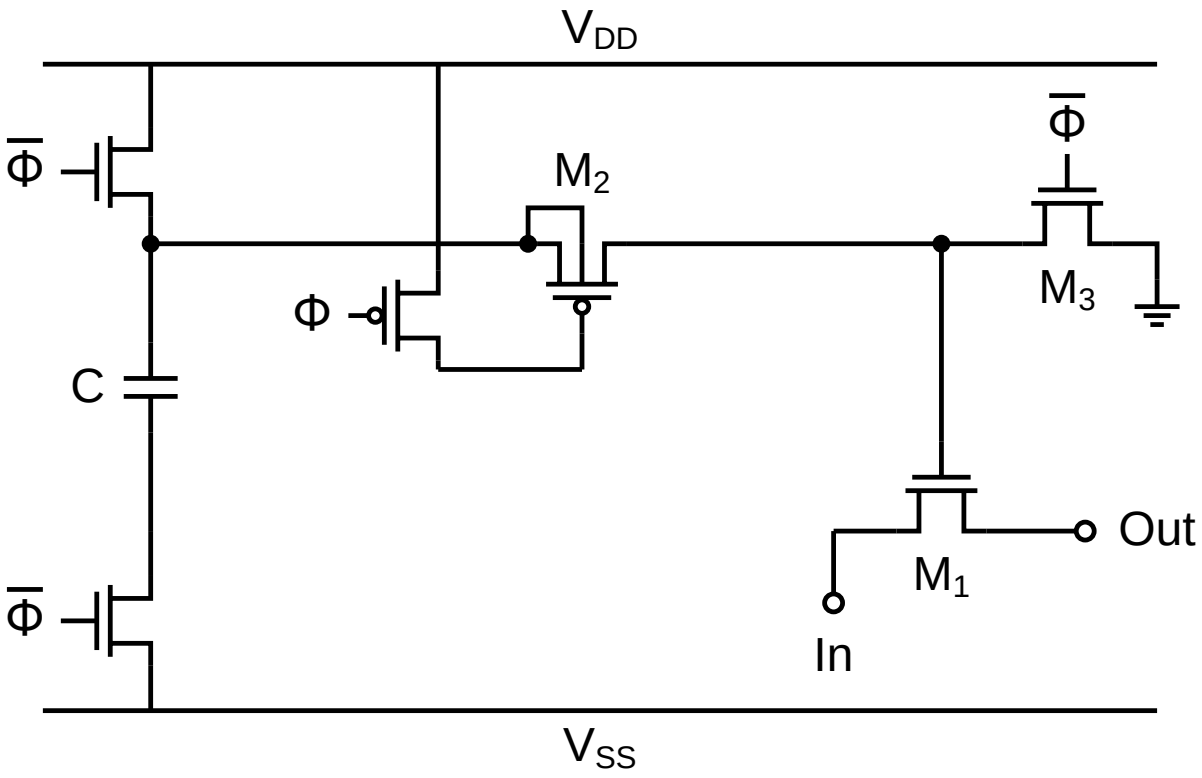
Nakagome Charge Pump

Y. Nakagome et al., “An experimental 1.5 V 64 Mb dram,”
IEEE J. Solid-State Circuits, vol. 26, pp. 465–472, Apr. 1991

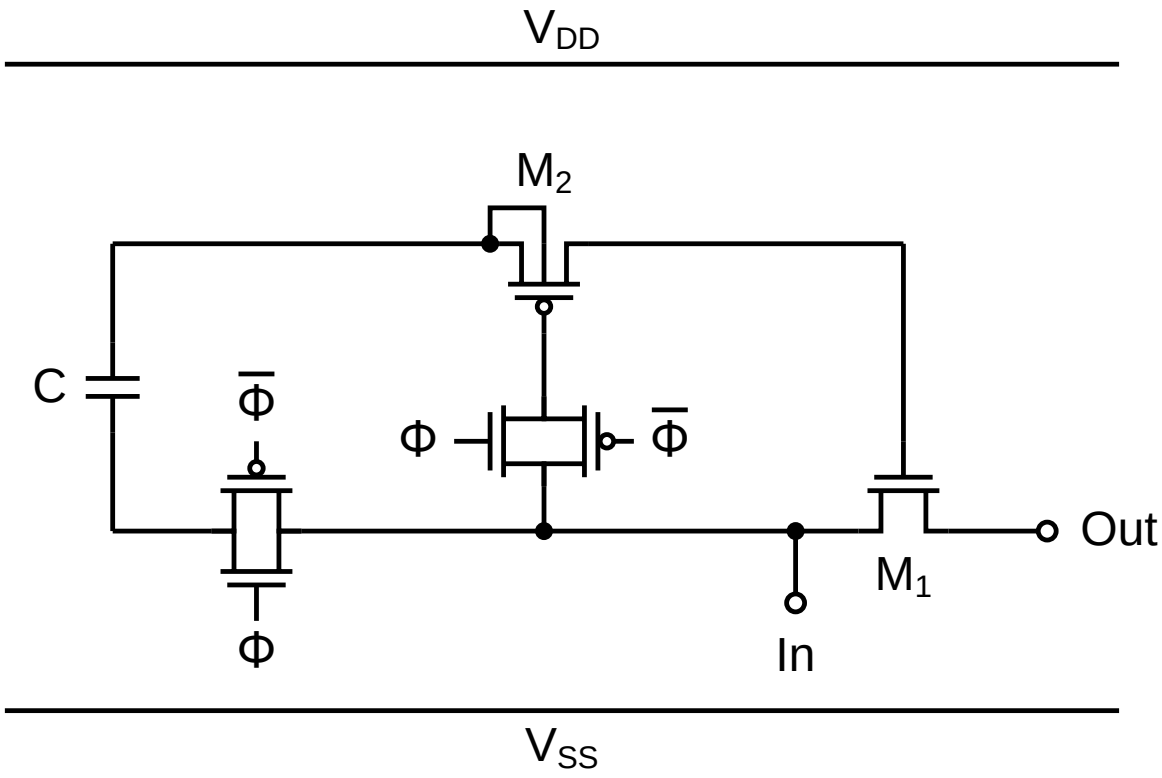


Ref: A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline ADC,”
IEEE Journal of Solid-State Circuits, vol. 34, issue 5, pp. 599-606, 1999.

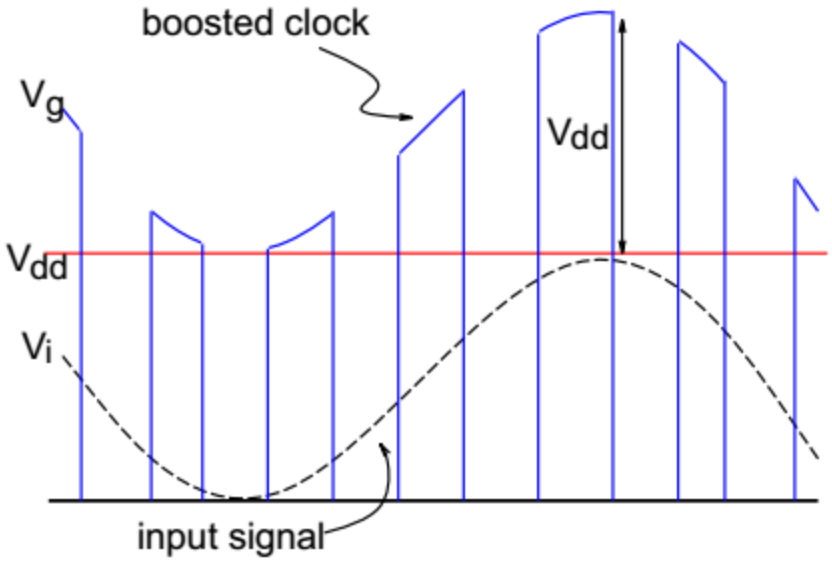
Clock Bootstrapping (Φ=0)



Clock Bootstrapping (Φ=1)

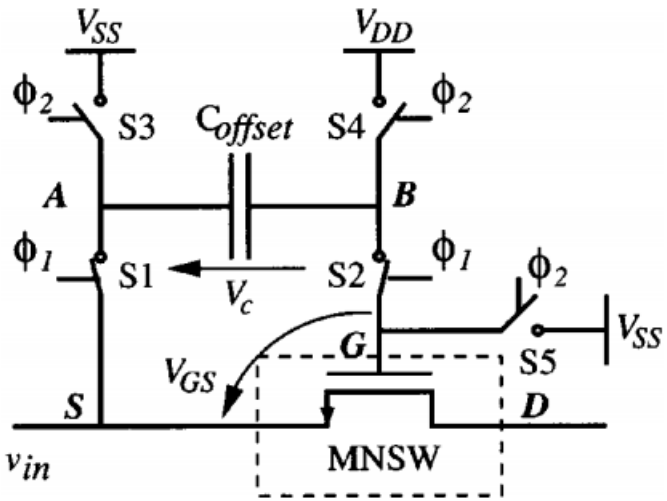


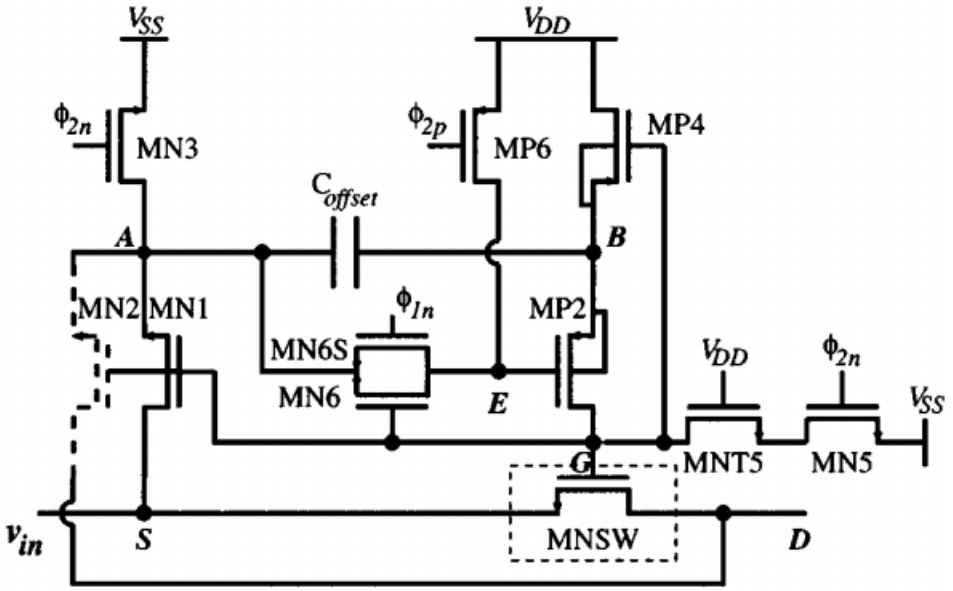
Clock Bootstrapping



Another Clock Bootstrap Circuit

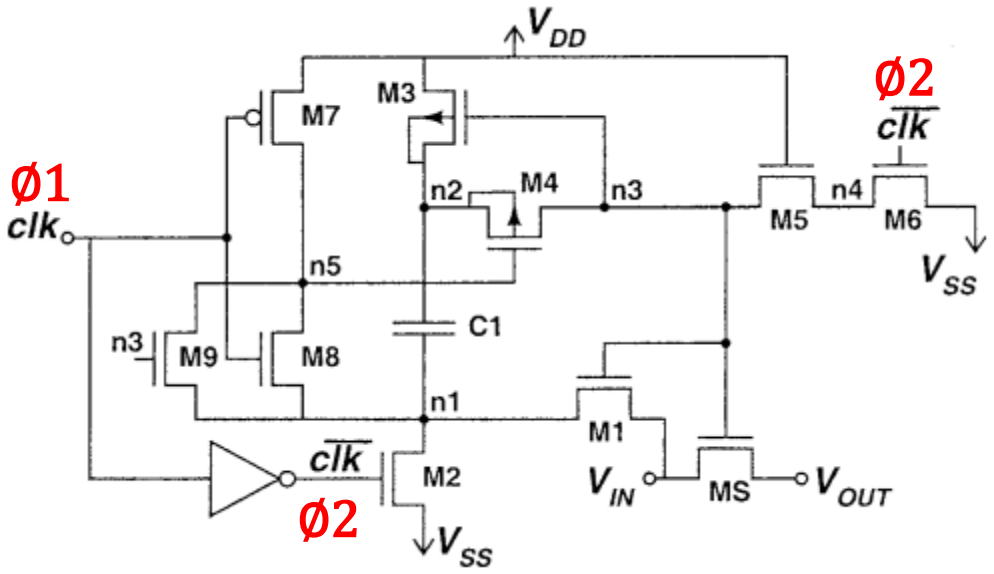
Mohamed Dessouky and Andreas Kaiser, “Very Low-Voltage Digital-Audio ΔΣ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping,”
IEEE J. Solid-State Circuits, vol. 36, pp. 349–355, Mar. 2001



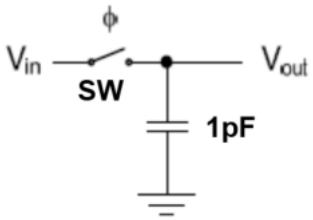


Another Clock Bootstrap Circuit

M. Waltari, et.al., “A Self-Calibrated Pipeline ADC with 200 MHz IF-Sampling Frontend,” *Analog Integrated Circuits and Signal Processing*, vol. 37, pp. 201–213, 2003



Homework #3 on 10-bit S/H



SW types

- ideal_swn from ee288lib
- CMOS TG – nmos2v & pmos2v
- Bootstrapped – nmos2v & pmos2v

VDD = 1.8V

- Sampling clock ϕ, fs = 100 MHz with 1.8V square wave.
- ideal_clock in ee288lib
- Input sine wave signal range 0.4V ~ 1.4V
- Input signal frequency at fin = (cycles/N) * fs
  where cycles=7 and N=64 for 64-point FFT

Summary of what you need to submit electronically:

1. Schematics of your design – use white background
2. Transient simulation results showing all relevant signal waveforms
3. FFT spectrum plots for different switch types
4. Summary table showing the ENOB, SNR, SFDR for all cases
5. Summary of what you learned on this homework problem