EE223 Analog Integrated Circuits
Fall 2018

Lecture 3: Review of Basics2

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ENG-259

HW #1

All homework problems should be done individually
and submitted by 6PM on the due date.

Submission: Email to sang-soo.lee@sjsu.edu
File name convention: EE223HW#1_your_name

- HW#1 – Cadence exercise → Due: Sept 12, Wed 6PM
- HW#2 – Single Stage Amplifier
- HW#3 – Beta Multiplier with Startup circuit
- HW#4 – OTA
- HW#5 – Two stage opamp

Analog Design Philosophy 1

- Never rely on absolute accuracy
  - R variation ~ ±20%, C variation ~ ±10%
  - Always use relative accuracy, typically 0.1 ~ 2%
- Always use the same W and L, same orientation for accurate matching
  - Do not vary W to control current value
  - Do not run the metal line over matched transistor pairs
  - Do not use minimum L for matched transistors
  - Use higher L/W ratio (preferably 10 or larger) for matched resistors
  - Try to use unit resistor with same W and L for resistors need matching
- Watch out for IR drop as current flows
  - For biasing, use current distribution rather than voltage distribution
- Watch out for nonlinearity due to body effect in Source Follower
- Avoid excess bandwidth and watch out for flicker noise
- Avoid a loop in cascode bias circuit. Check start up condition

Analog Design Philosophy 2

- In N-well CMOS process, tie the bulk of the PMOS differential pair to its own well if at all possible
- Make sure that all the transistors are in Saturation unless they are designed for linear operation
- Use differential circuit architecture as much as possible
- For 10-bit accuracy
  - Amplifier requires 7 time constants to settle
  - Unity gain frequency (GBW) of the amplifier should be more than 1.1 times the signal frequency of operation
- Simulate over PVT (corner and worst cases), and understand the weak point in the circuit
- Amplifier stability check
  - Make sure to check both phase and gain margins
  - Use transient simulation to verify ac stability
- Implement register programmability if unsure about process variations
- Make sure that the logic level is well defined for digital circuits used in analog blocks

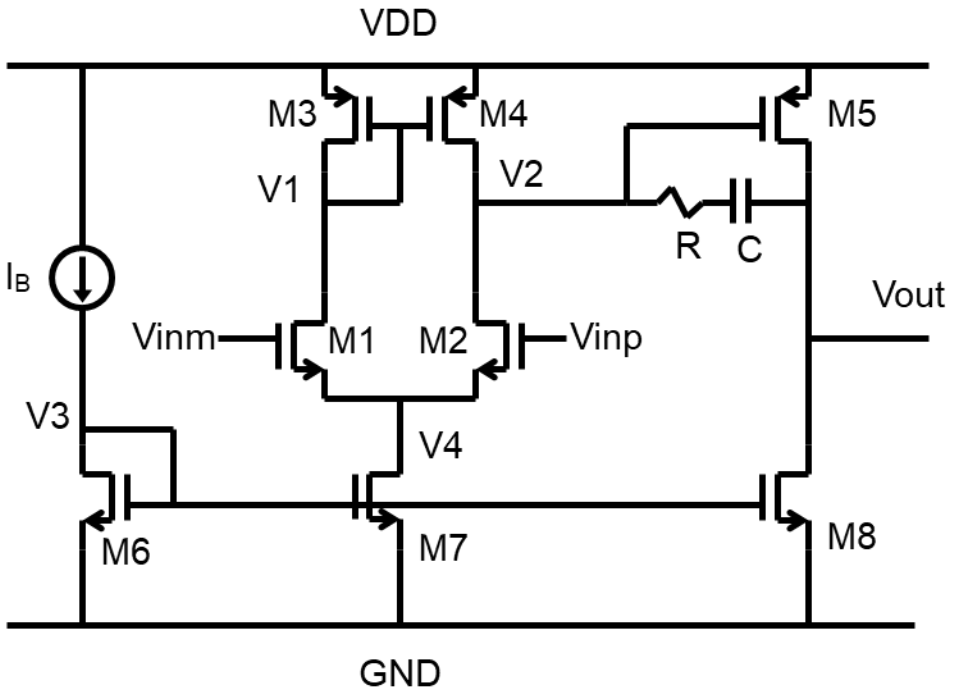
Chip Design Hierarchy

- System design – define spec
- Building Block – define block spec
- Circuit design
- Device/Components modeling & design
  - Resistors
  - Capacitors
  - PN Diodes
  - Transistors : Bipolar (NPN & PNP)
    CMOS (NMOS & PMOS)

Circuit Design Consideration

- Performance
  - Small-signal response
    - Gain, bandwidth
  - Large-signal response
    - Settling time, delay
  - Sensitivity over PVT (process, voltage supply, temperature)
  - Stability
- Basic design tasks
  - AC circuit: signal path
  - DC circuit: Biasing
- General design approach
  - Generally designed from output to input

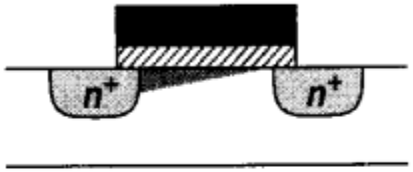
Two-Stage OPAMP



Abstraction Levels in Circuit Design

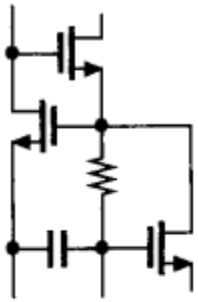
[Razavi]

Device



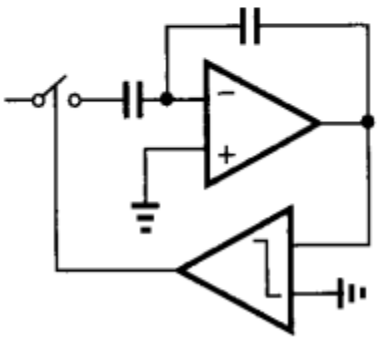
(a)

Circuit



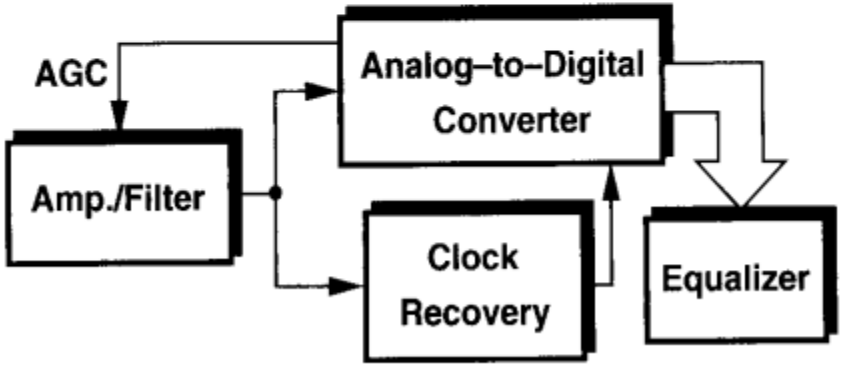
(b)

Architecture



(c)

System



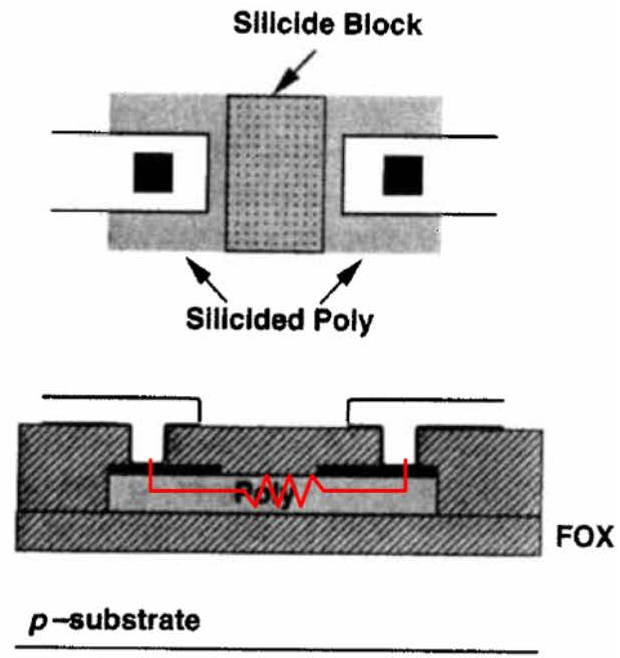
(d)

Device Types

- Active
  - MOS Transistors
  - Bipolar Transistors
  - Diodes
- Passive
  - Resistors
  - Capacitors
  - Inductors
- Interconnect

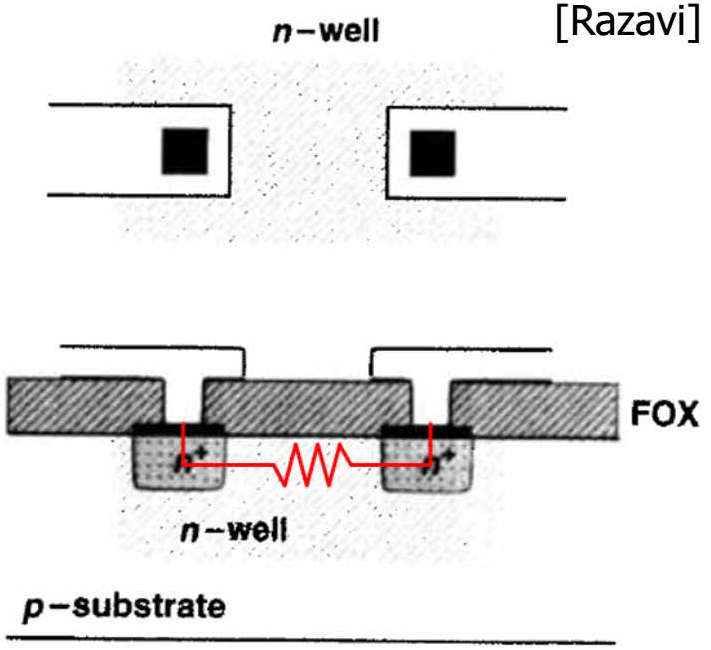
Resistors

Poly Resistor

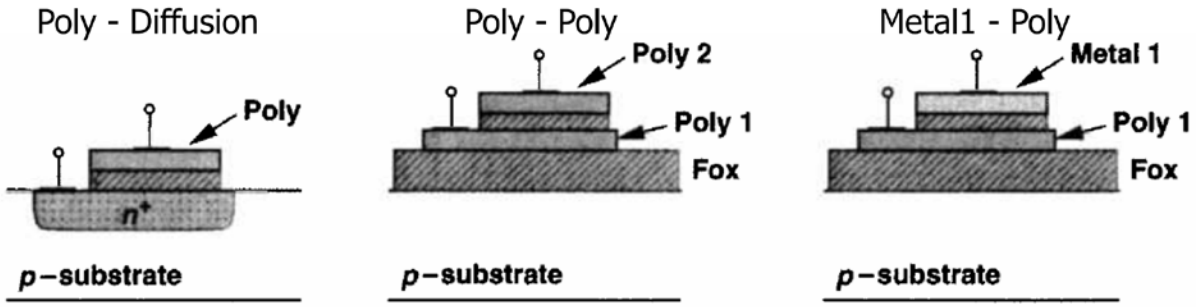


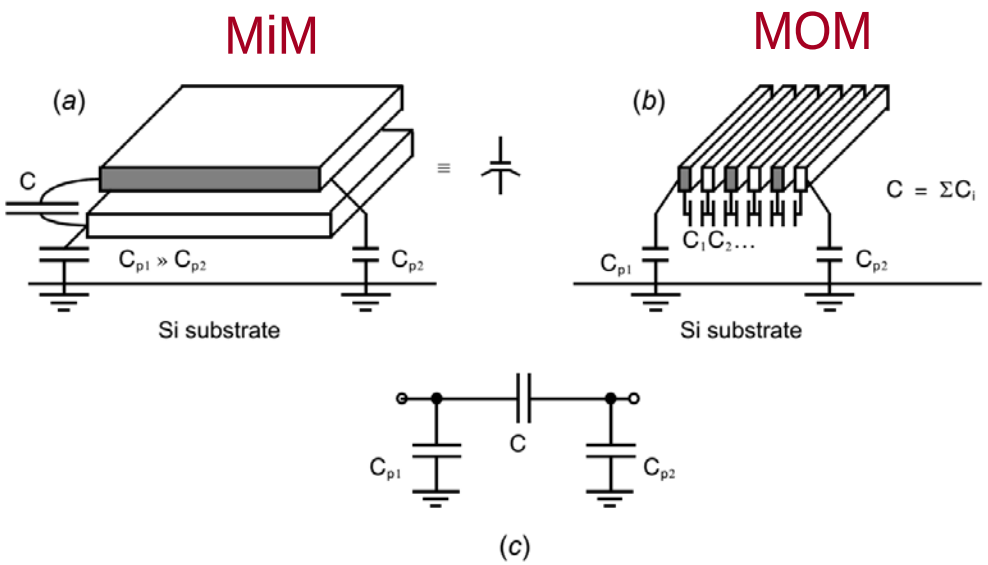
Nwell Resistor

[Razavi]



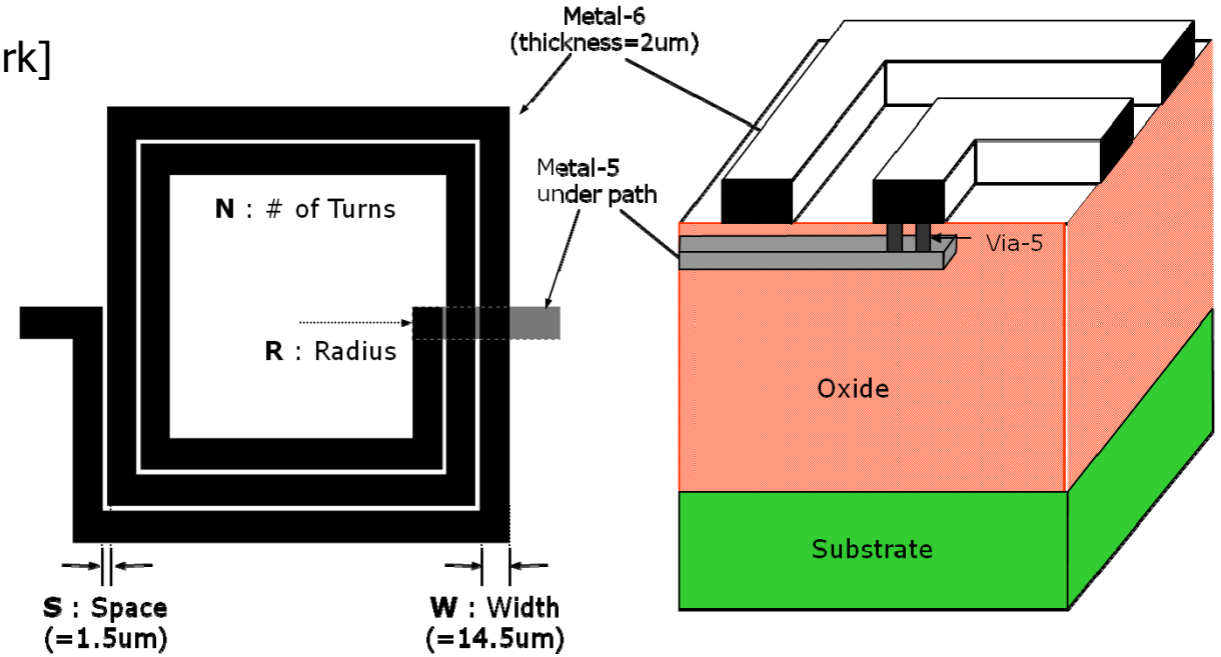
Capacitors


Poly - Diffusion
Poly
n+
p–substrate
Poly - Poly
Poly 2
Poly 1
Fox
p–substrate
Metal1 - Poly
Metal 1
Poly 1
Fox
p–substrate


MiM
MOM
(a)
C
≡
$C_{p1} \gg C_{p2}$
C_{p2}
Si substrate
(b)
$C = \Sigma C_i$
$C_1 C_2 \ldots$
C_{p1}
C_{p2}
Si substrate
C
C_{p1}
C_{p2}
(c)

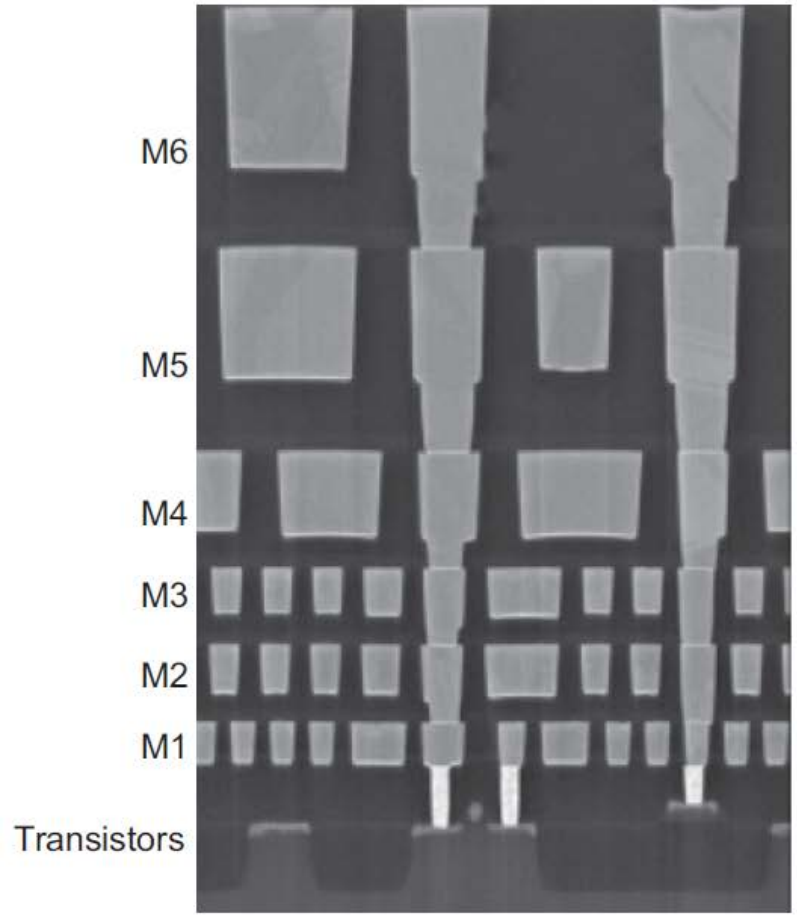
Inductors

[Silva/Park]

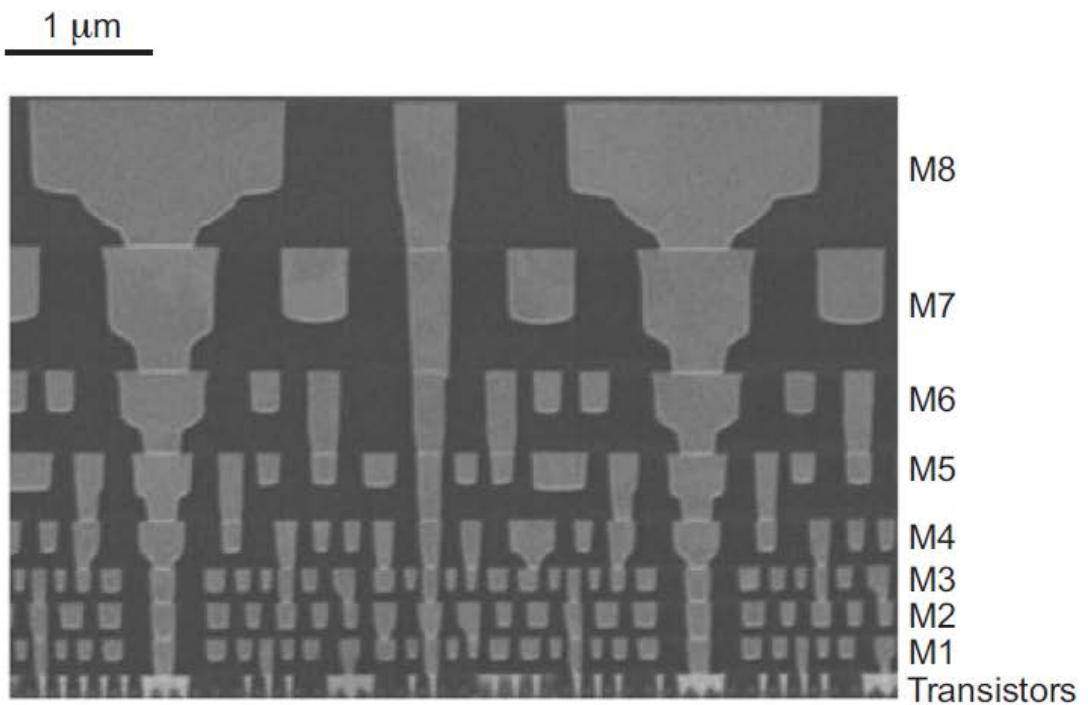


- Inductors are generally very large
  - A typical inductor area (100μm x 100μm)
- Essential component in RF circuits

Interconnect



90nm



45nm

Interconnect

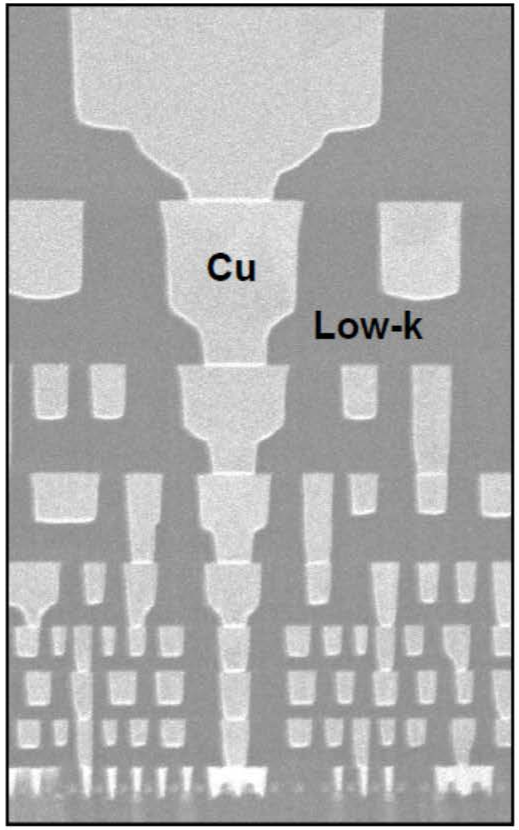
Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

Tight pitch on lower layers

- Maximum density for local interconnects

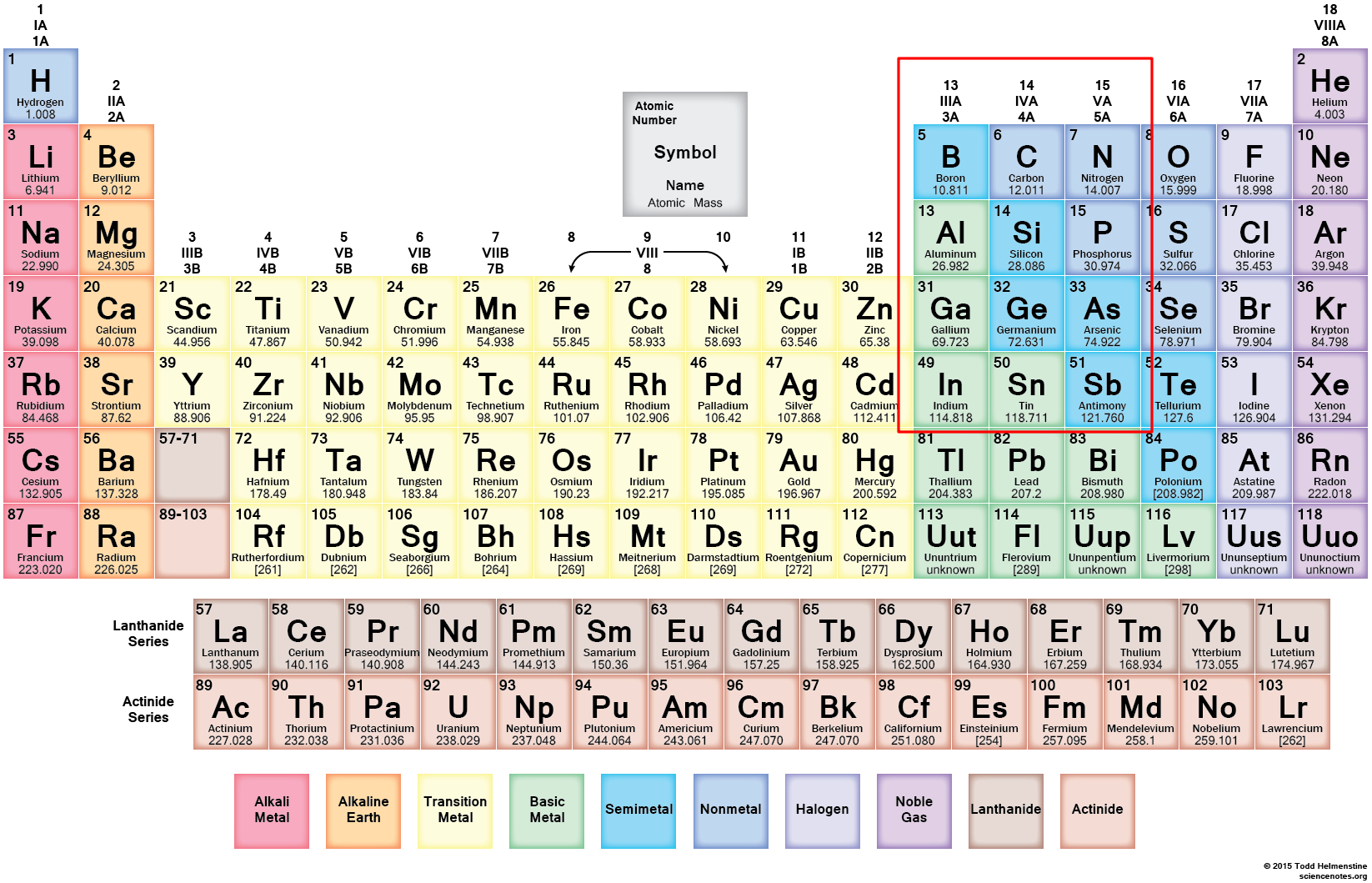
[Bohr ISSCC 2009]



	Pitch (nm)
M8	810
M7	560
M6	360
M5	280
M4	240
M3	160
M2	160
M1	160

45nm

Periodic Table of the Elements



pn Junction

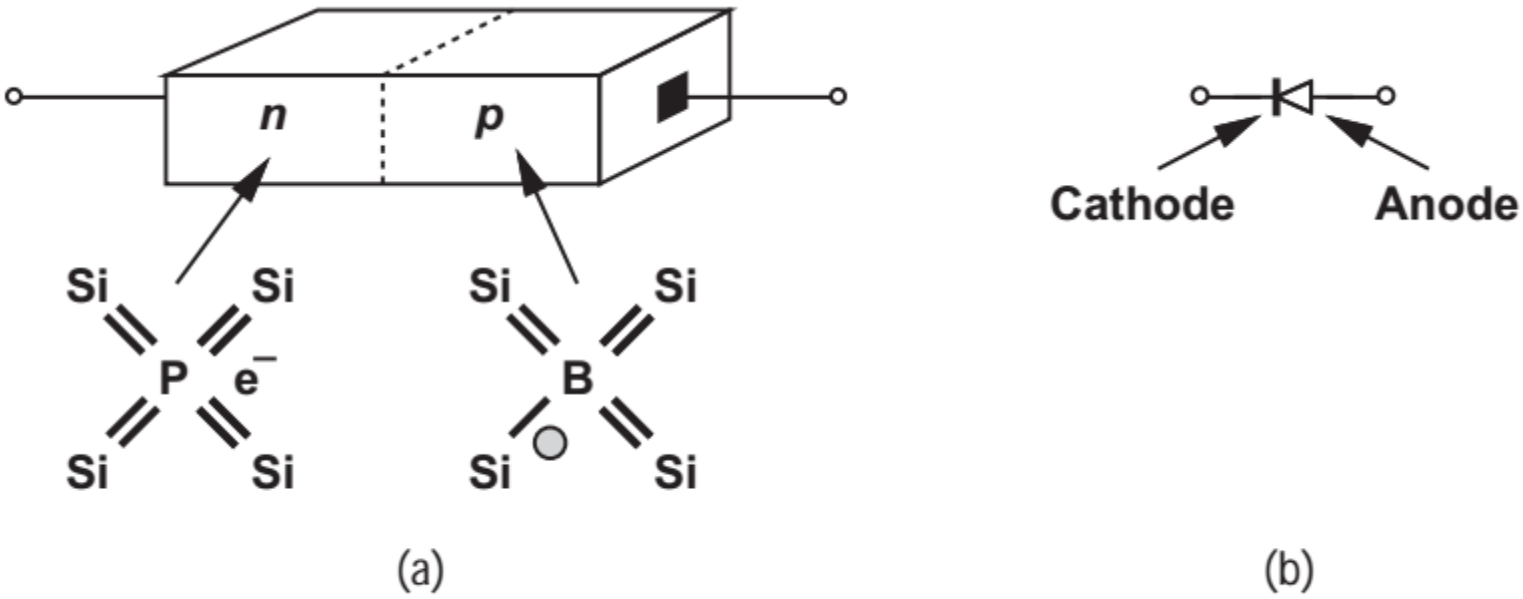


Figure 2.16 *pn* junction.

pn Junction

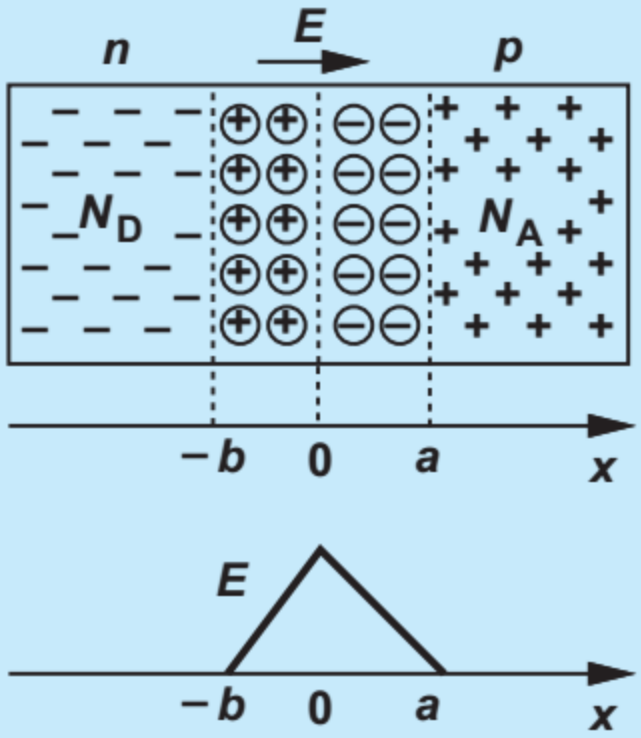


Figure 2.21 Electric field profile in a *pn* junction.

pn Junction in Reverse Bias

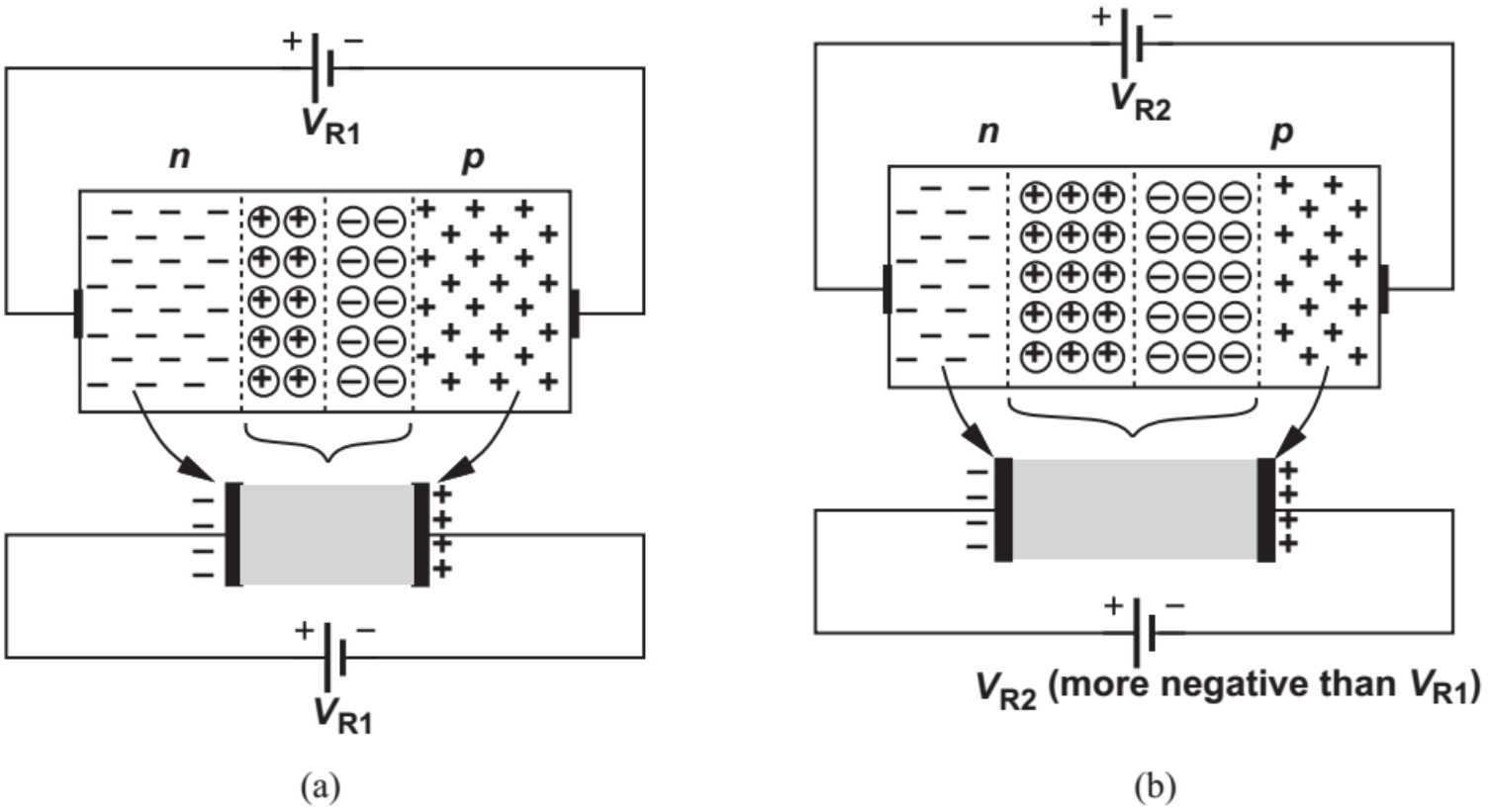


Figure 2.24 Reduction of junction capacitance with reverse bias.

Junction Capacitance in Reverse Bias

$$C_j = \frac{C_{j0}}{\sqrt{1 - \frac{V_R}{V_0}}}$$

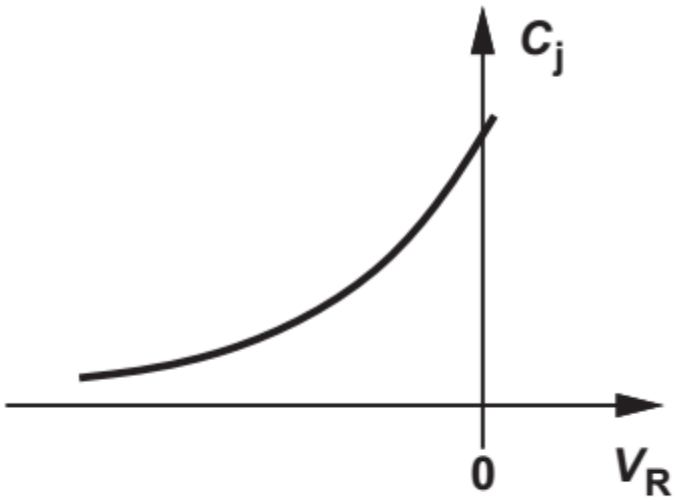
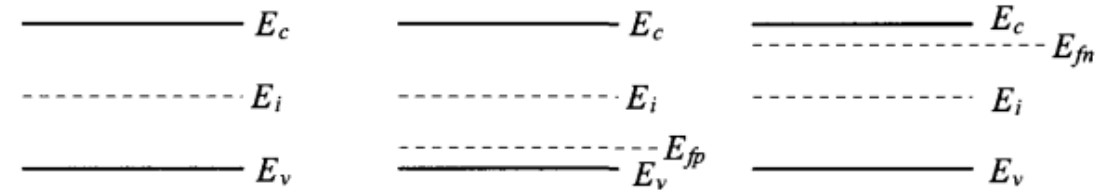
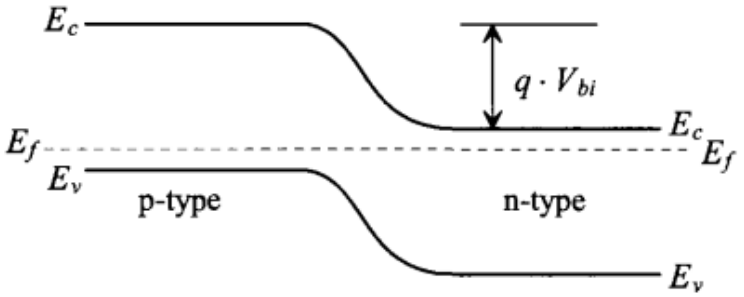


Figure 2.25 Junction capacitance under reverse bias.

PN Junction Energy Band Diagram



(a) Intrinsic silicon (b) p-type silicon (c) n-type silicon



(d) A pn-junction diode

$$V_{bi} = \frac{E_{fn} - E_{fp}}{q} = \frac{kT}{q} \cdot \ln \frac{N_A N_D}{n_i^2}$$

Diode I/V Characteristics

$$I_D = I_S\left(\exp\frac{V_D}{V_T} - 1\right)$$

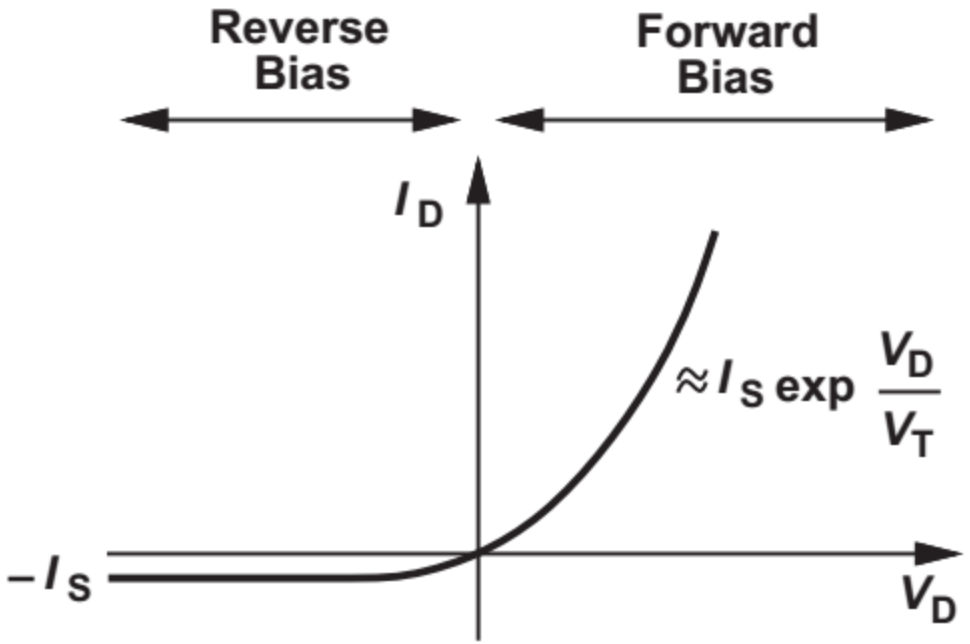
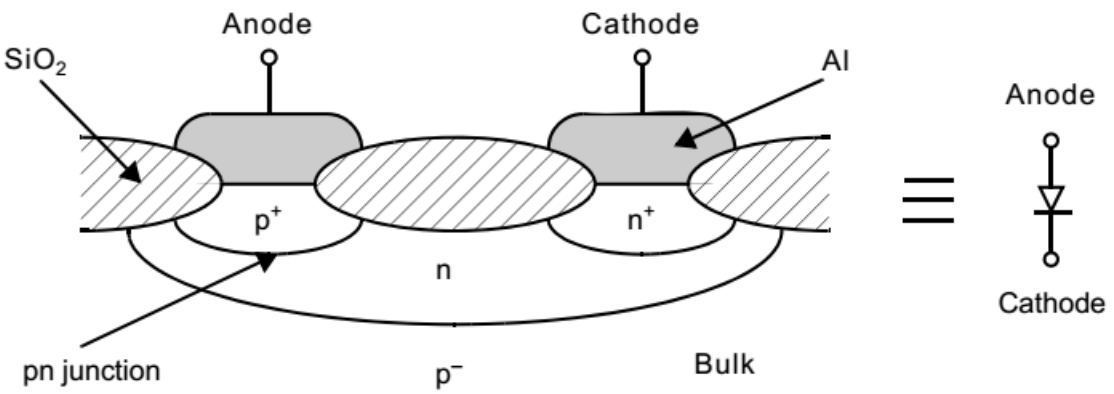
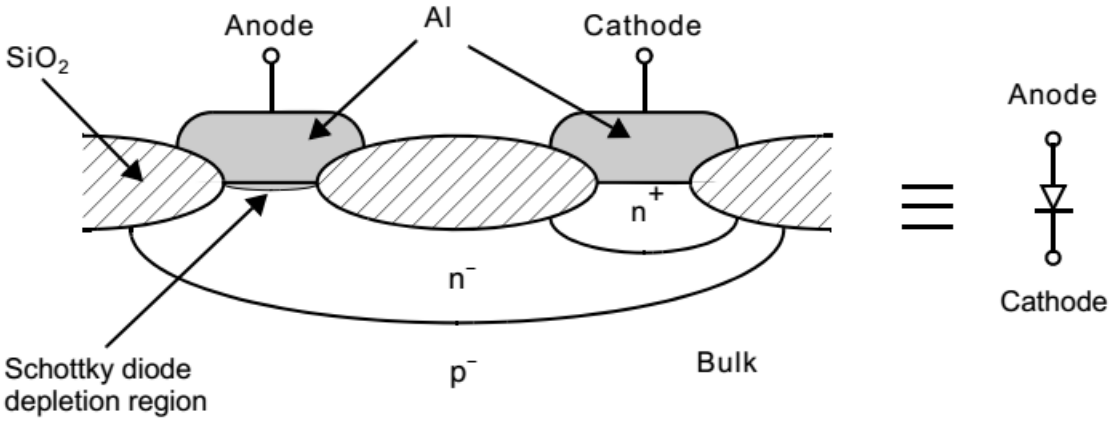


Figure 2.31 I/V characteristic of a *pn* junction.

Diodes





Typical values:

$P^+=10^{17}$-10^{19} acceptors /cm^3

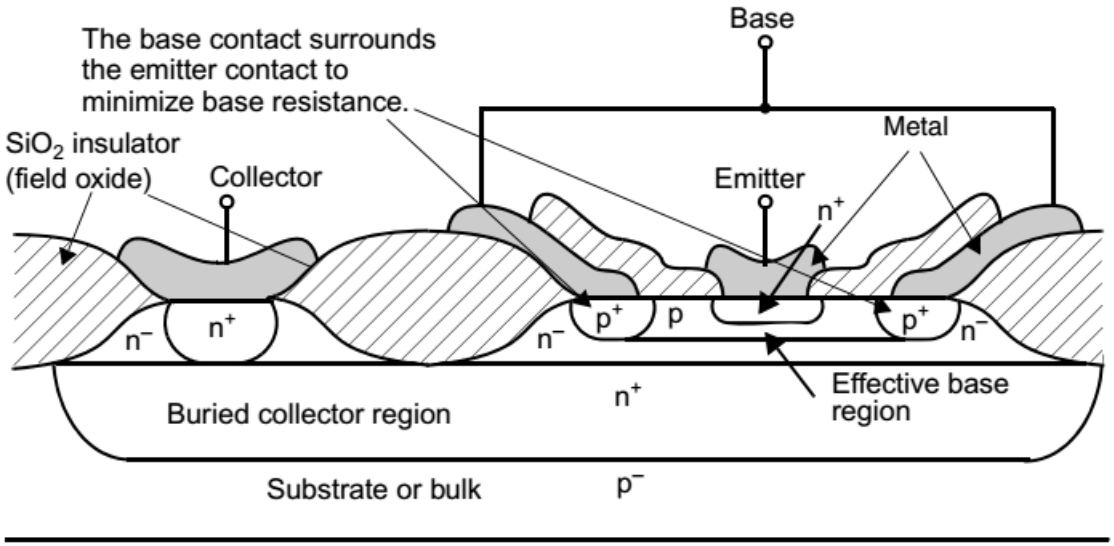
$P=10^{15}$-10^{17} acceptors /cm^3

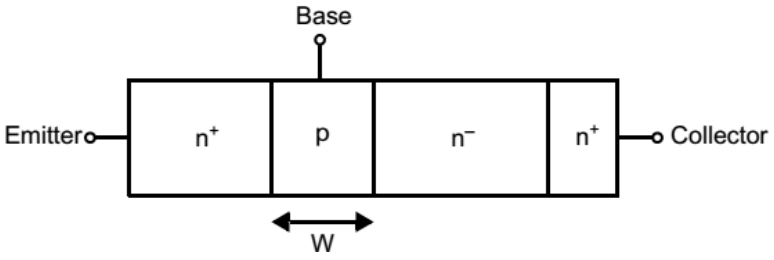
$N=10^{16}$-10^{18} donors/cm^3

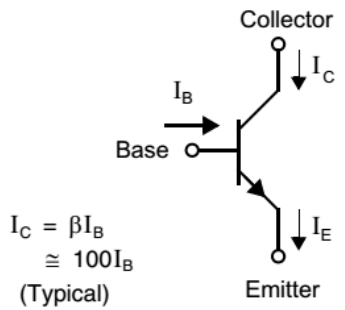
$N^+=10^{17}$-10^{19} donors/cm^3

Metal $\rightarrow$ $5x10^{22}$ electrons/cm^3

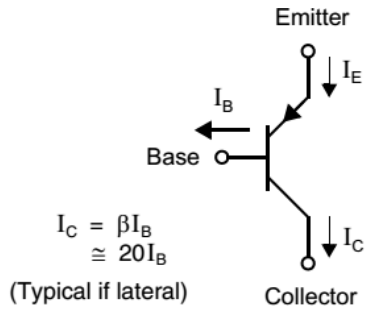
Bipolar Transistors







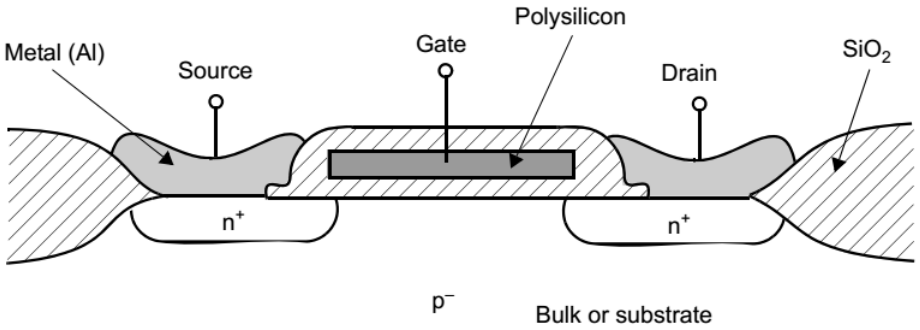
(*a*) npn



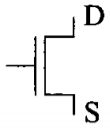
(*b*) pnp

MOS Transistor Symbol

NMOS cross-section

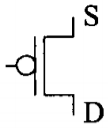


NMOS symbol

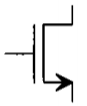


(a) NMOS device with body tied to ground.

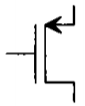
PMOS symbol



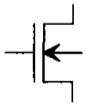
(b) PMOS device with body tied to VDD.



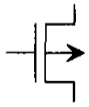
(c) Bipolar-derived NMOS symbol with body tied to ground.



(d) Bipolar-derived PMOS symbol with body tied to VDD.



(e) NMOS symbol where the arrow indicates the p-substrate to n-channel diode.



(f) PMOS symbol where the arrow indicates the n-well to p-channel diode.

NMOS Structure

Figures from Microelectronic Circuits, 7th Edition, by Sedra and Smith, Oxford University Press, 2015.

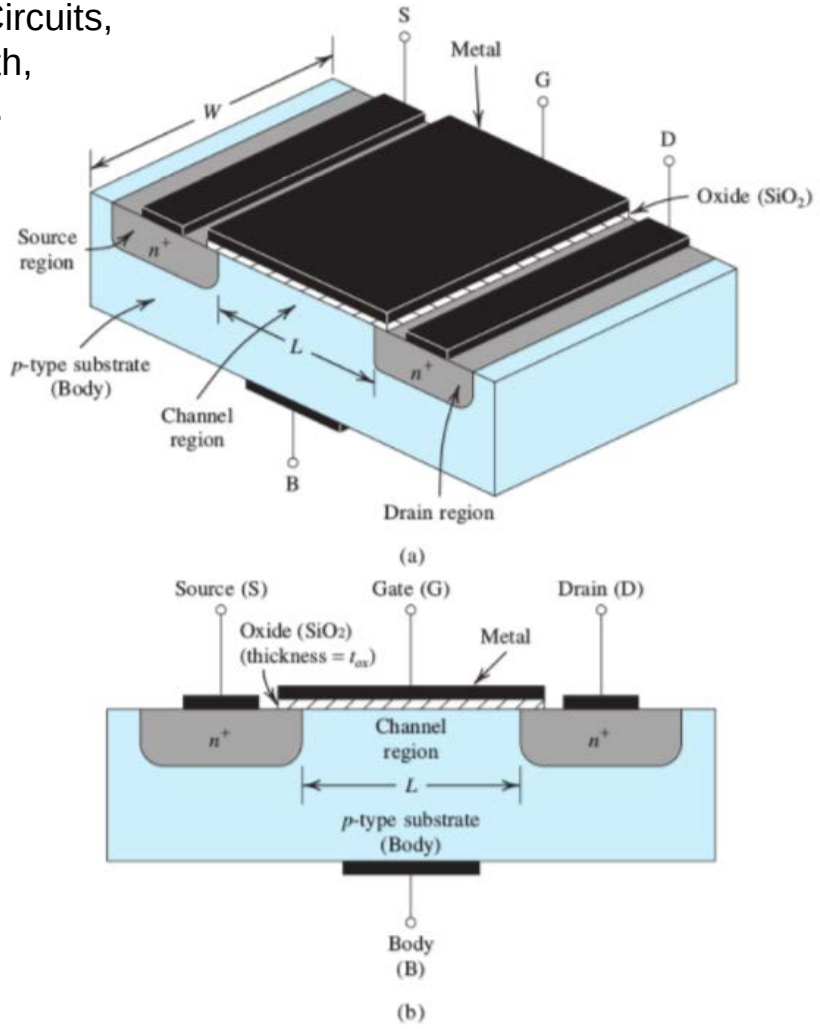
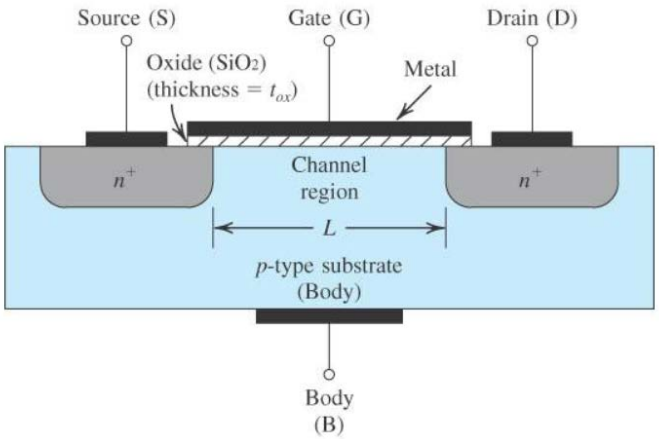
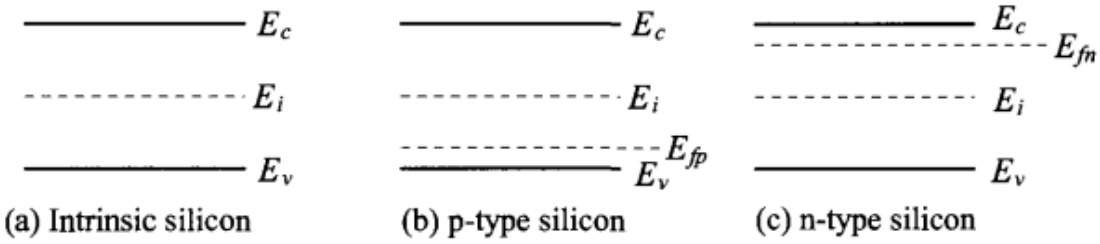
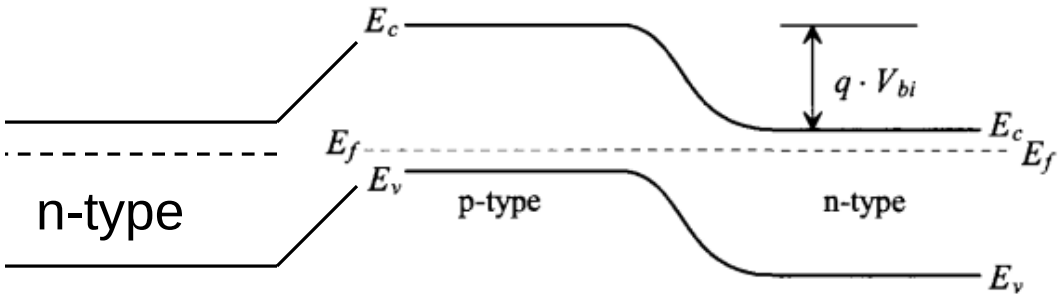


Figure 5.1 Physical structure of the enhancement-type NMOS transistor: (**a**) perspective view; (**b**) cross section. Typically $L = 0.03$ μm to 1 μm, $W = 0.05$ μm to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.

NMOS



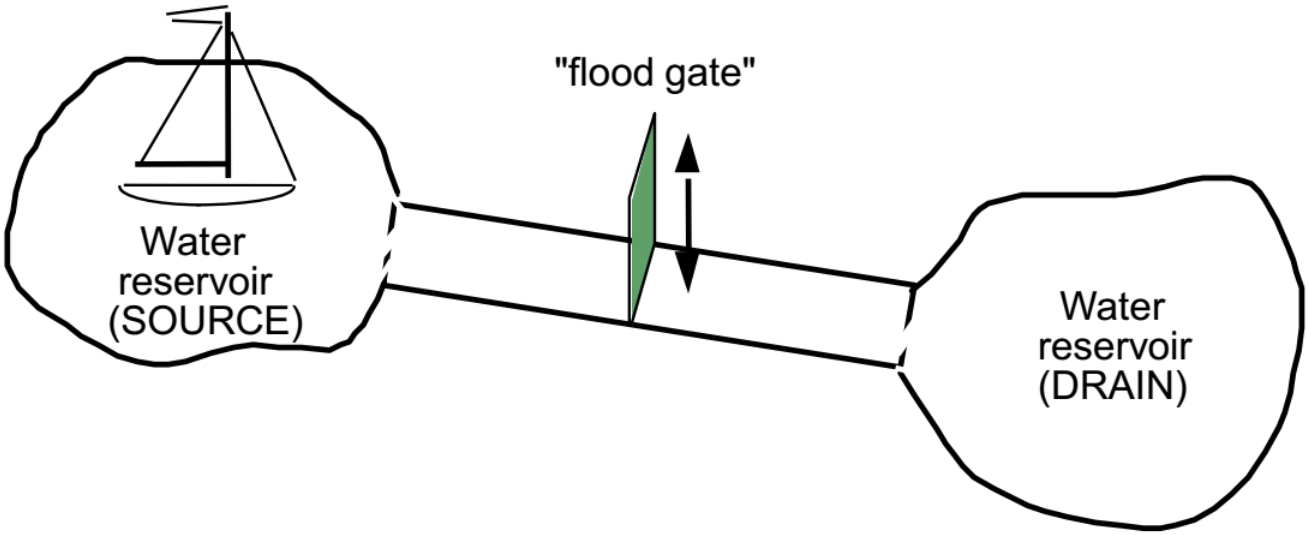




n+ Source p- substrate n+ Drain

MOSFET Analogy

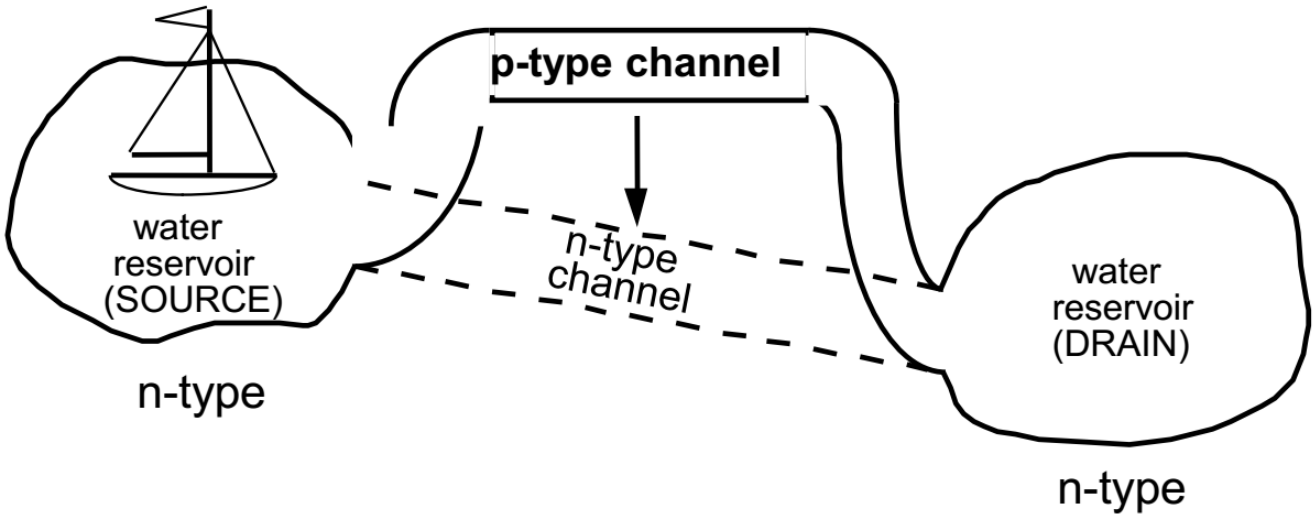
- A MOSFET transistor is nothing more than a voltage controlled switch!
- A transistor is just like a light switch on a wall, except that a voltage is used to turn the switch on and off instead of a lever.
- A good analogy to a transistor is two lakes connected by a canal.



- The "flood gate" regulates the flow of water between the two lakes (source and drain).
- A real transistor switches the flow of electric current on and off instead of water.

MOSFET Operation

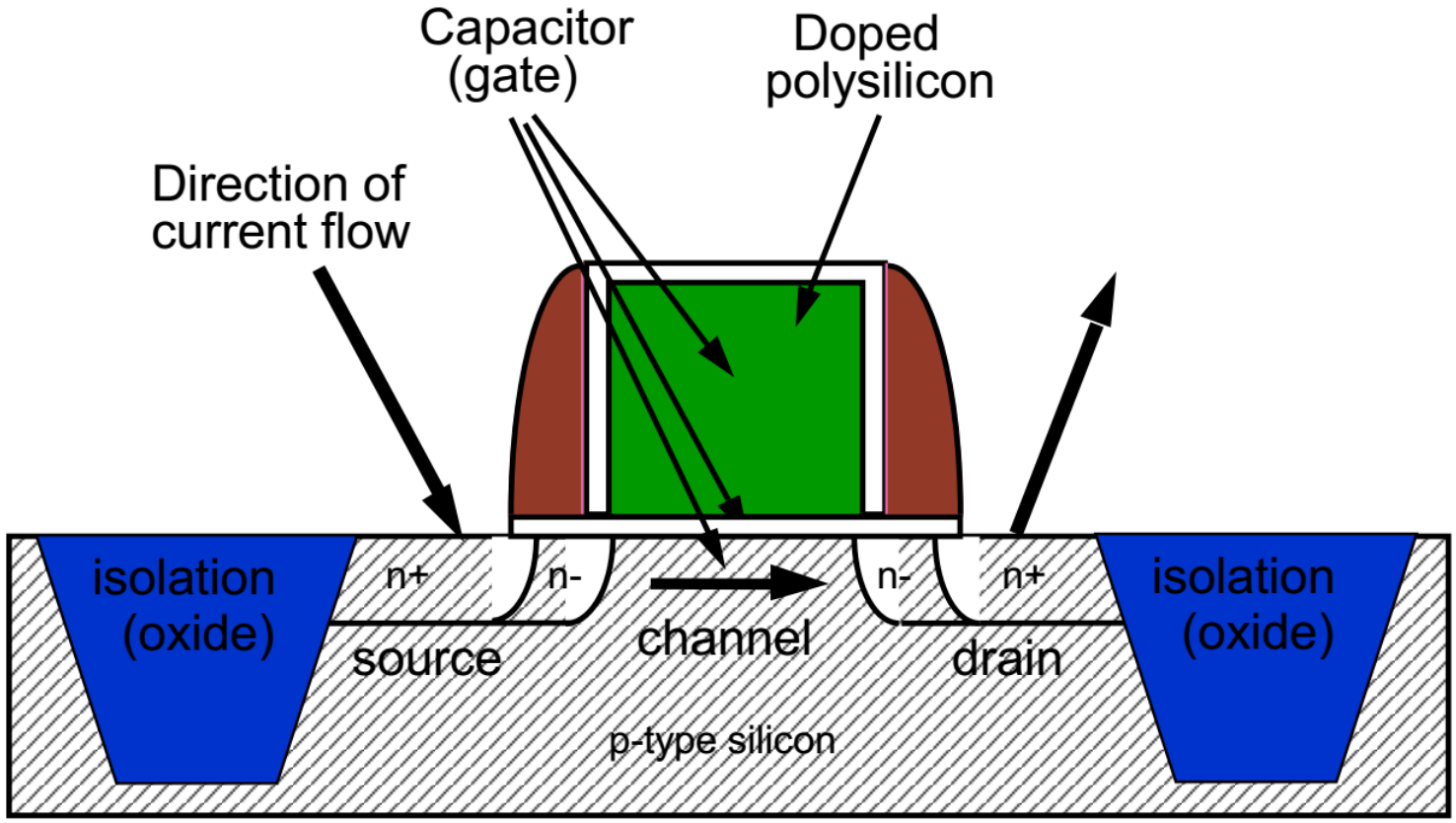
- Current (water) will not flow from an n-type reservoir to a p-type region because it would have to flow *uphill*.



- Only way we can get water from one n-type reservoir to another is by way of a *n-type channel.*
- By using a capacitor and applying a positive voltage to that capacitor, we can change the apparent conductivity of the channel from p to n and turn the transistor on.
- In reality, the drain is usually at a lower elevation than the source so the water will flow downhill to the drain.

MOSFET Operation

- A MOS transistor is nothing more than a voltage-controlled switch.
- A MOS transistor is really just a capacitor with two extra terminals.



NMOS I_d-V_{ds} Characteristics

$$i_D = k_n'\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

$$V_{DSsat} = V_{OV} = V_{GS} - V_t$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)V_{OV}^2$$

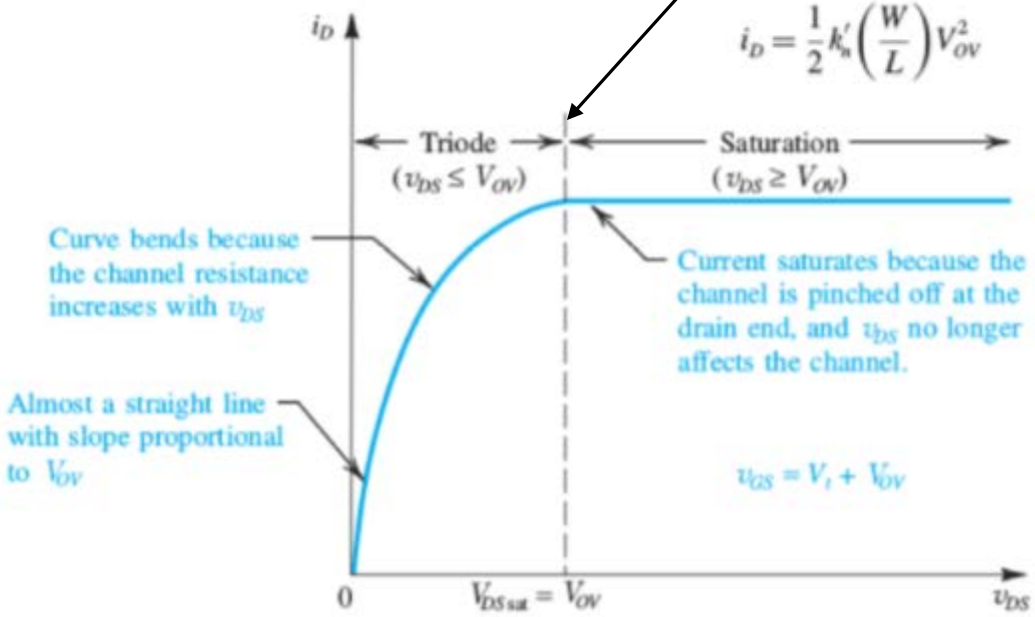


Figure 5.7 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$

NMOS I-V Characteristics

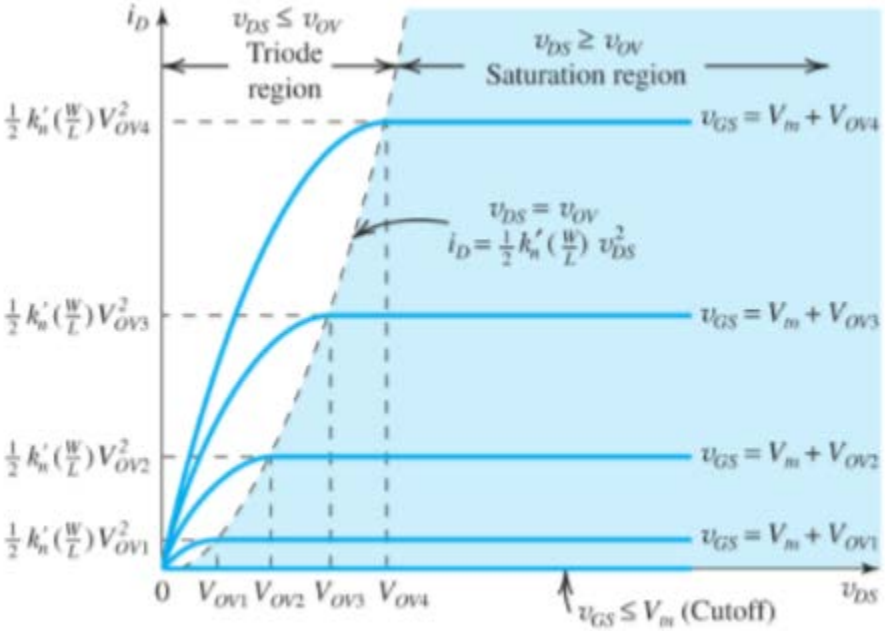


Figure 5.13 The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor.

Channel Length Modulation

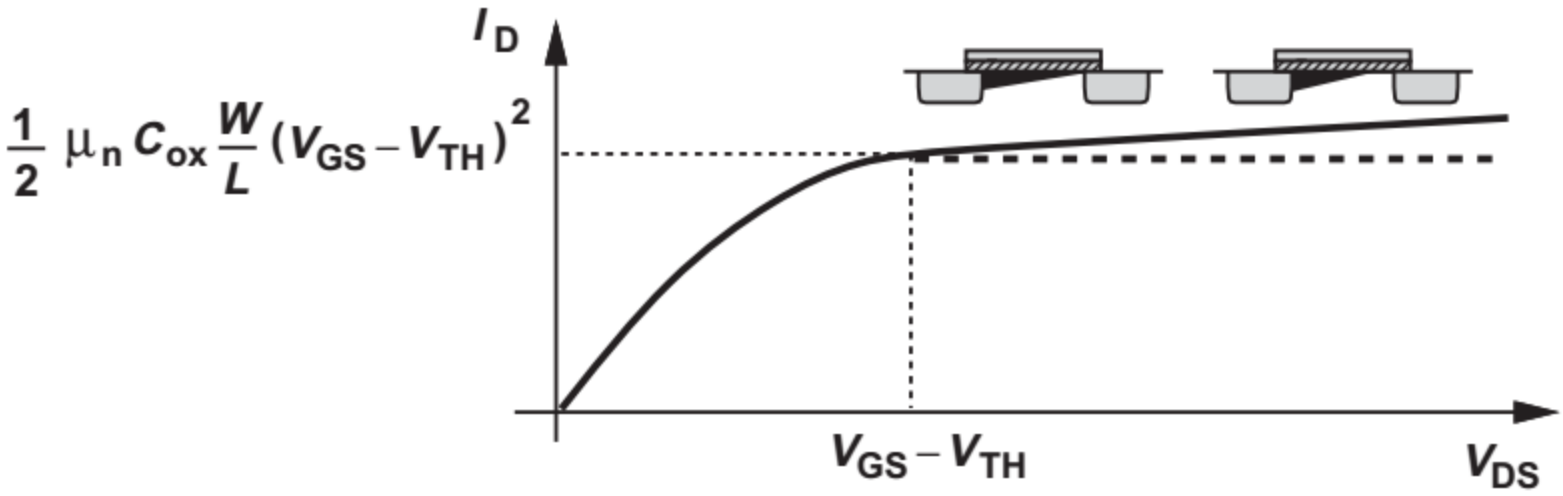


Figure 6.25 Variation of I_D in saturation region.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) \qquad r_O = \frac{\Delta V_{DS}}{\Delta I_D}$$

Channel Length Modulation

$$r_O = \frac{\Delta V_{DS}}{\Delta I_D}$$

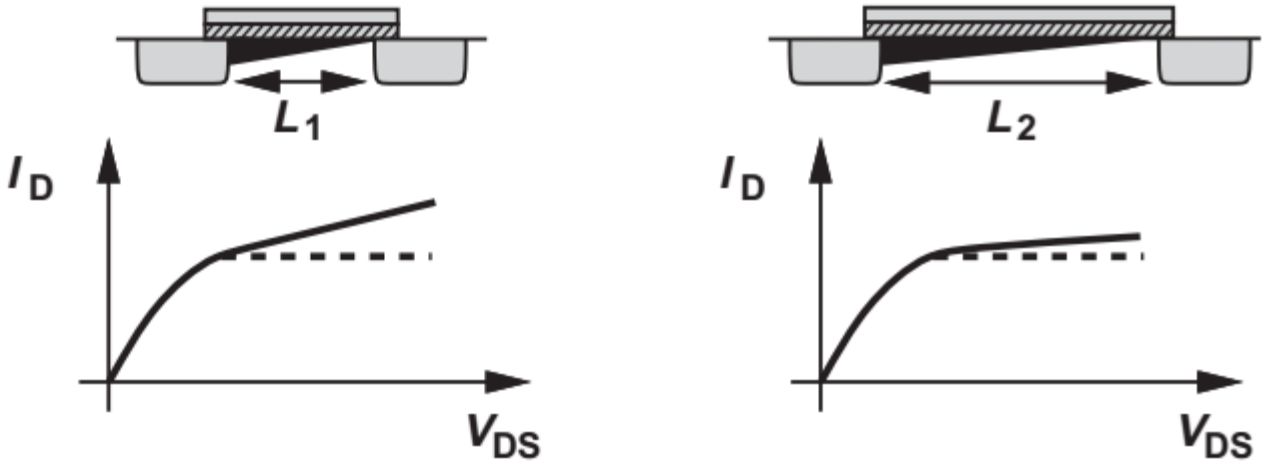


Figure 6.26 Channel-length modulation.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

MOS Transconductance in Saturation

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

Body Effect

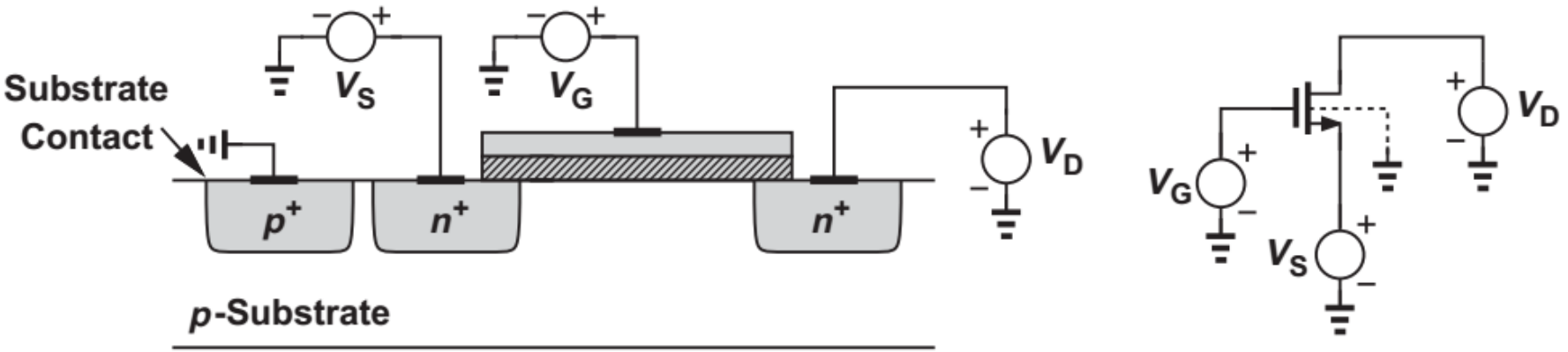


Figure 6.28 Body effect.

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|})$$

$$\gamma = \sqrt{2q\epsilon_{si}N_{sub}}/C_{ox}$$