

# **On-Chip Spiral Inductors for Silicon-Based Radio-Frequency Integrated Circuits**

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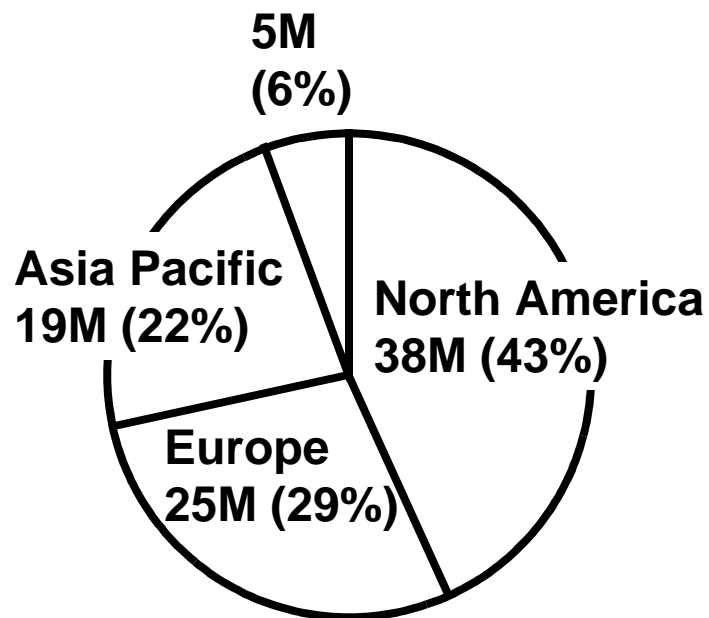
# Outline

- Overview
- A physical model for on-chip inductors
- Effects of process and layout parameters
- Design methodology
- Inductors with patterned ground shields
- Substrate noise coupling
- Conclusions

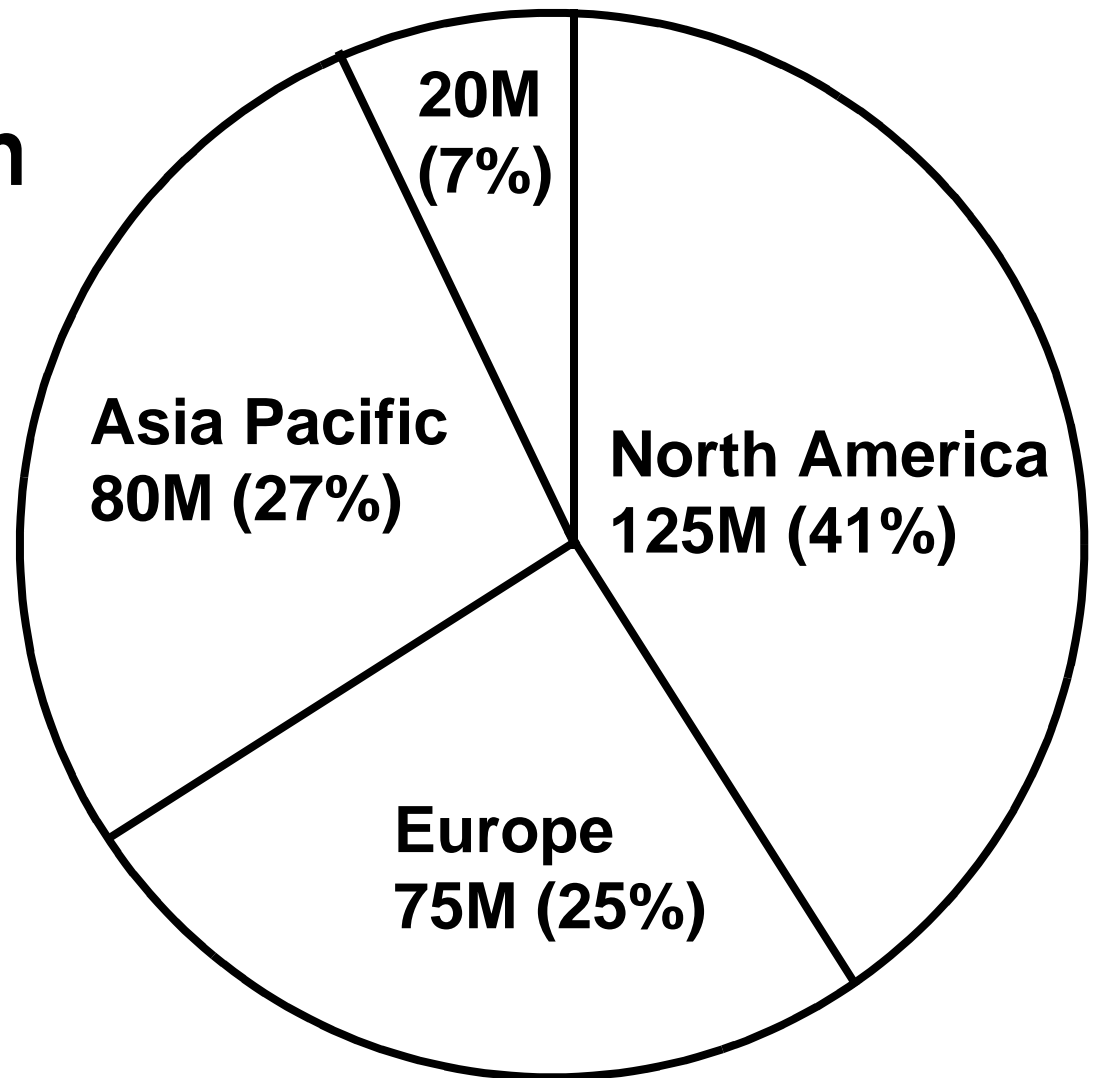
# Worldwide Wireless Market

**36% Annual Growth**

(Source: CTIA, 1996.)

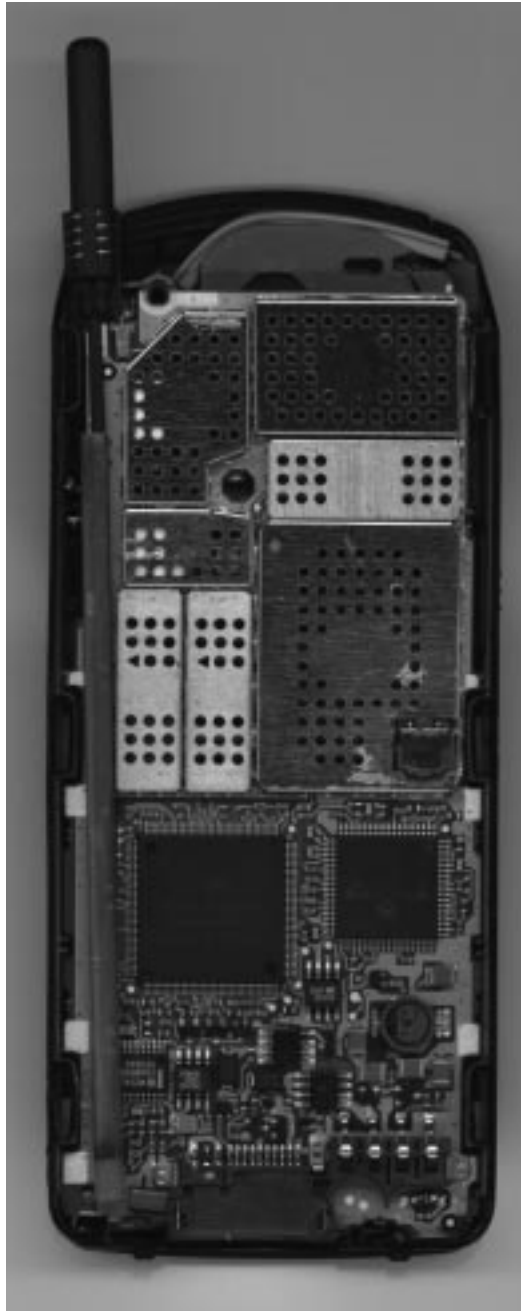


**1996 Total: 87M**



**2000 Total: 300M**

# A Typical Cellular Phone



## RF front-end component count:

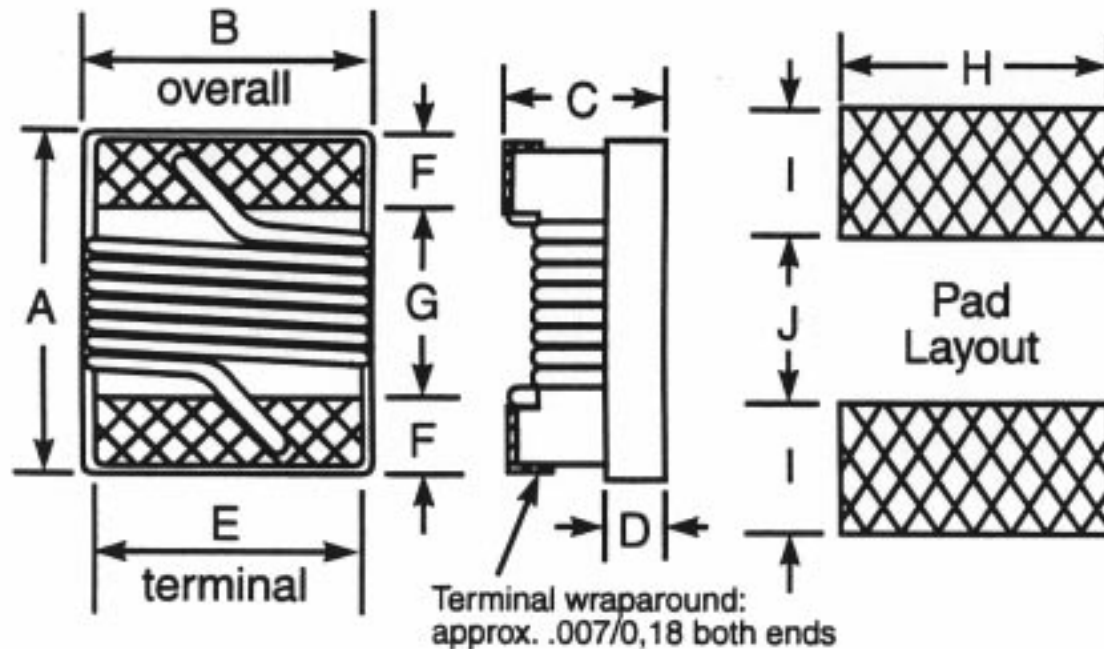
Inductor	11
Capacitor	>100
Resistor	>50
IC	5
Transistor	12
Crystal	1
Filter	2

(Source: Bosch, 1997.)

# Advantages of Integration

- **Cost: assembly and packaging**
- **Power: fewer parasitics**
- **Design Flexibility: signals stay on chip**
- **Size**
- **Reliability**
- **Tolerance**

# Discrete Inductors



- L: 2 to 20 nH  
(2 to 10%)

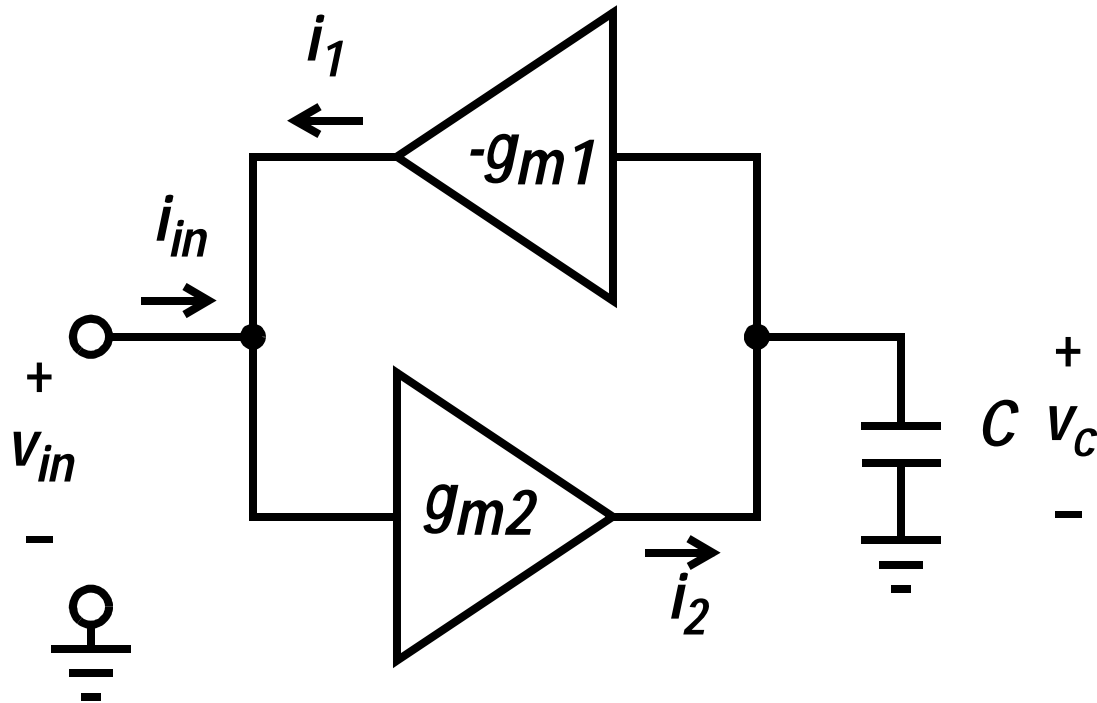
- Q: 50 to 200  
(1 to 2 GHz)

- srf: 4 to 10 GHz

A	B	C	D	E	F	G	H	I	J	
Max.	Max.	Max.	Ref.							
.071	.044	.040	.015	.030	.013	.034	.040	.025	.025	inch
1,80	1,12	1,02	0,38	0,76	0,33	0,86	1,02	0,64	0,64	mm

(Source: Coilcraft, 1997.)

# Active Inductors



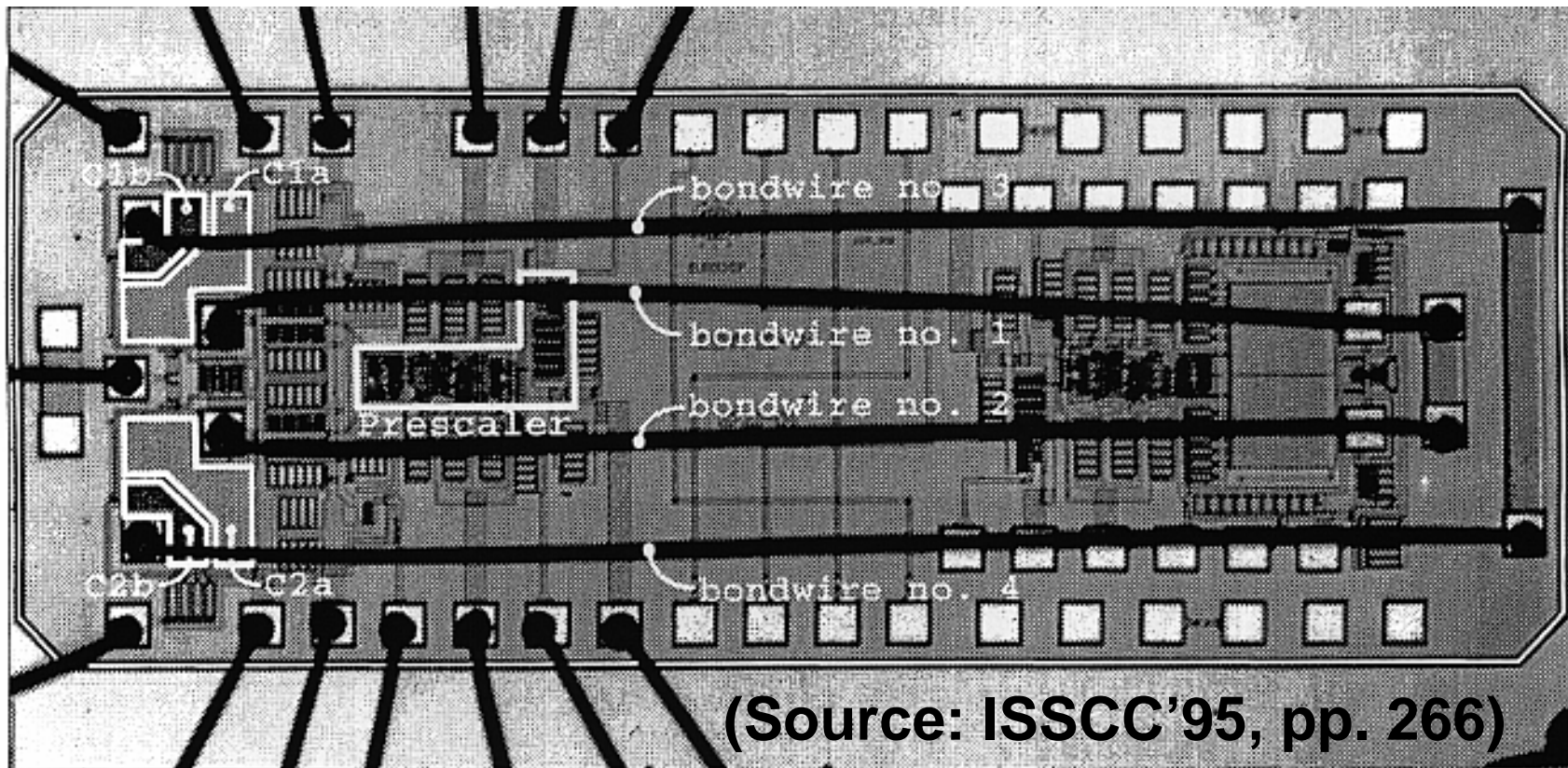
- Excess Noise
- Extra Power
- Limited Linearity

$$L = \frac{C}{g_{m1}g_{m2}}$$



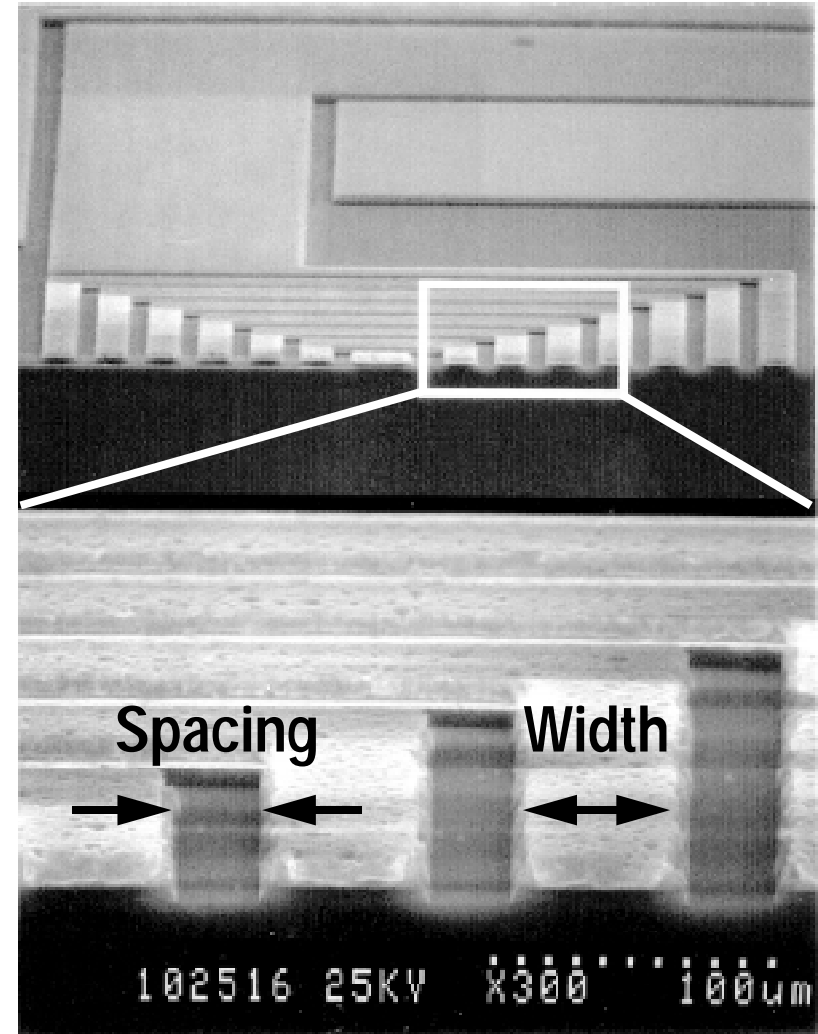
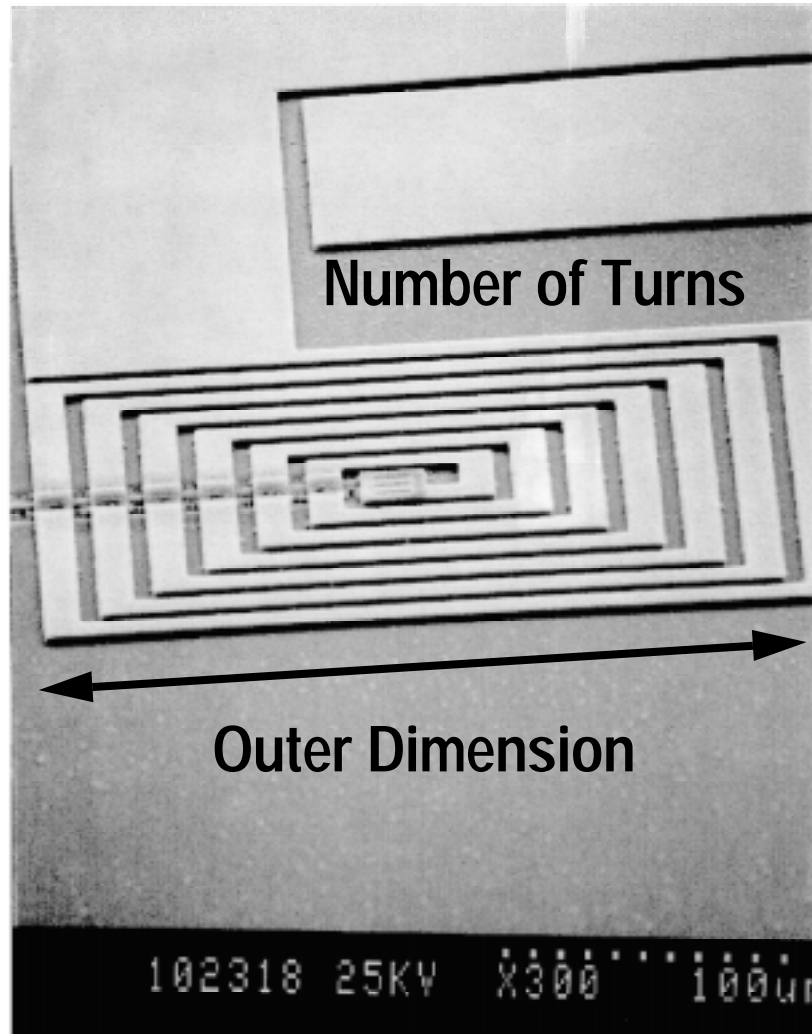
# Bond Wire Inductors

- Predictability
- Unwanted Couplings
- Repeatability
- Limited Inductance

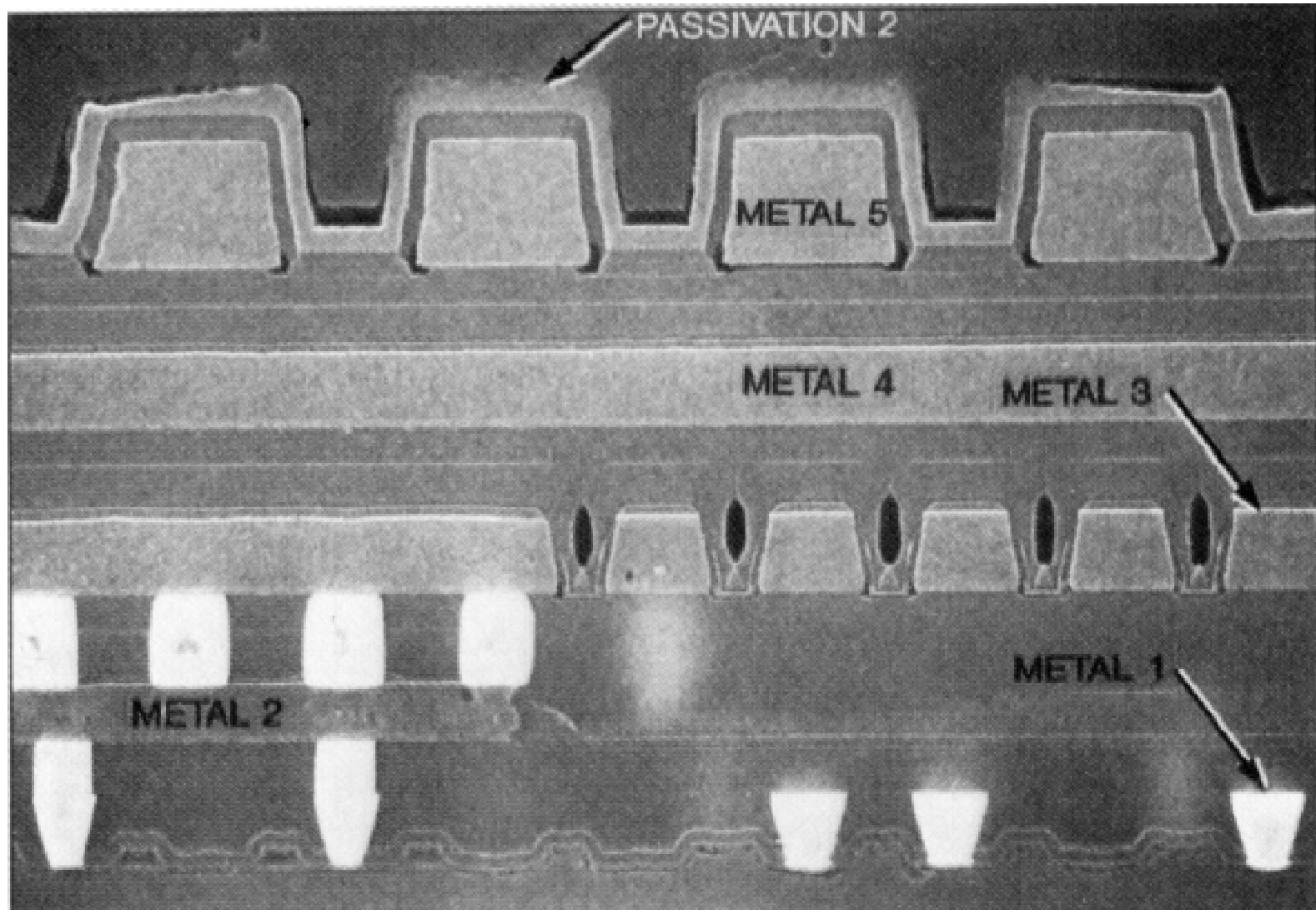




# A Typical Planar Spiral Inductor

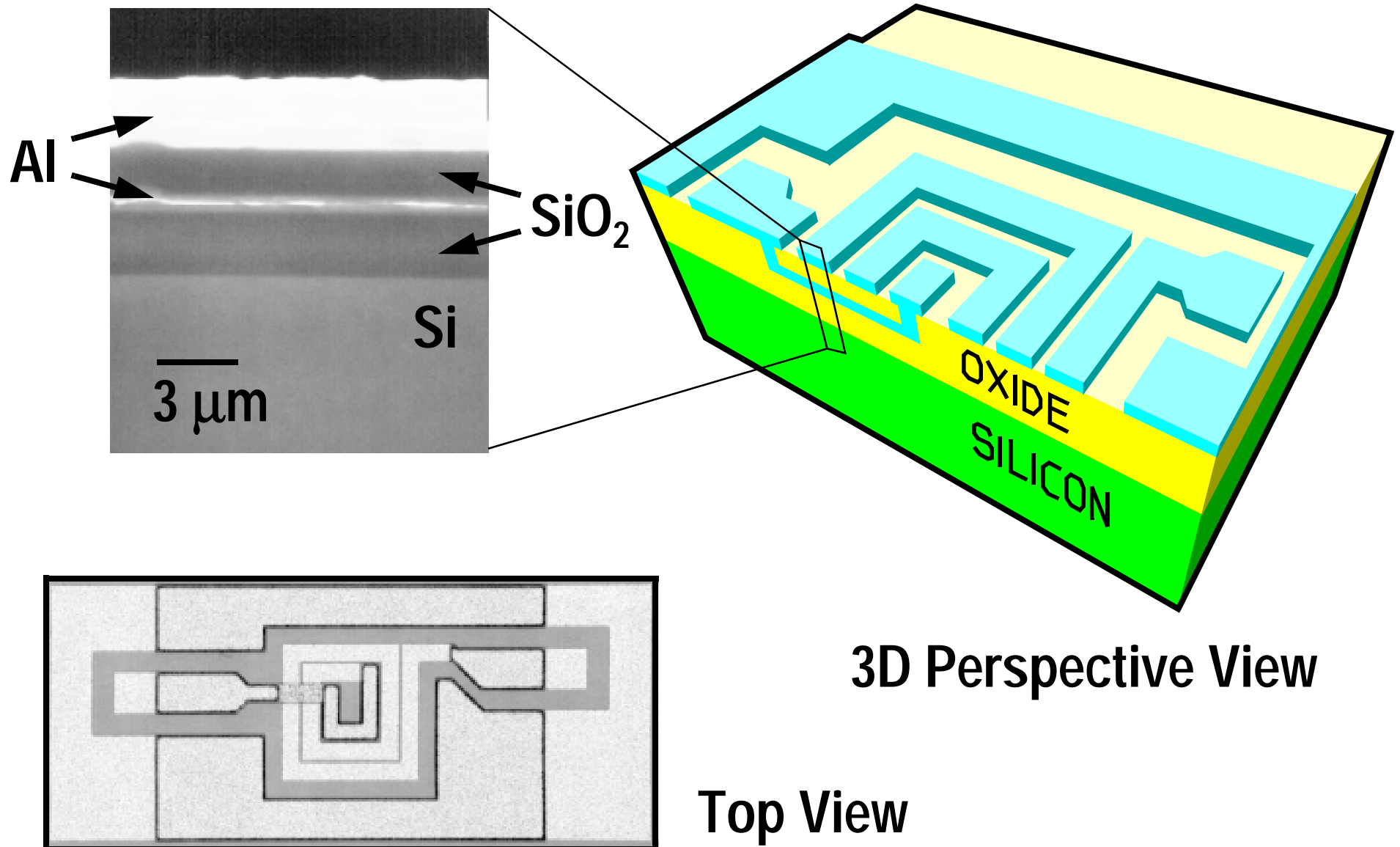


# Multilevel Interconnects

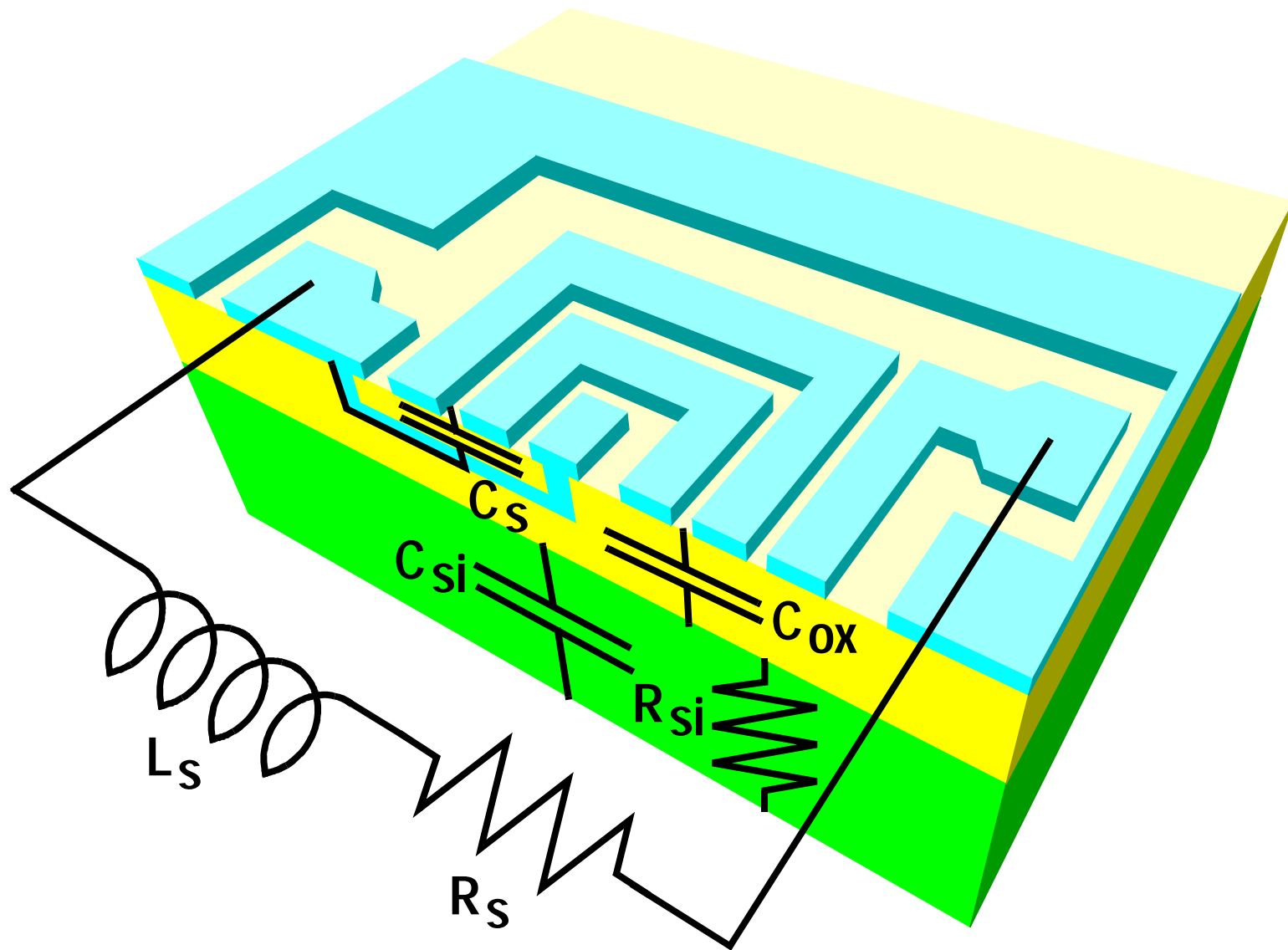


(Source: *Semiconductor International*, 1997.)

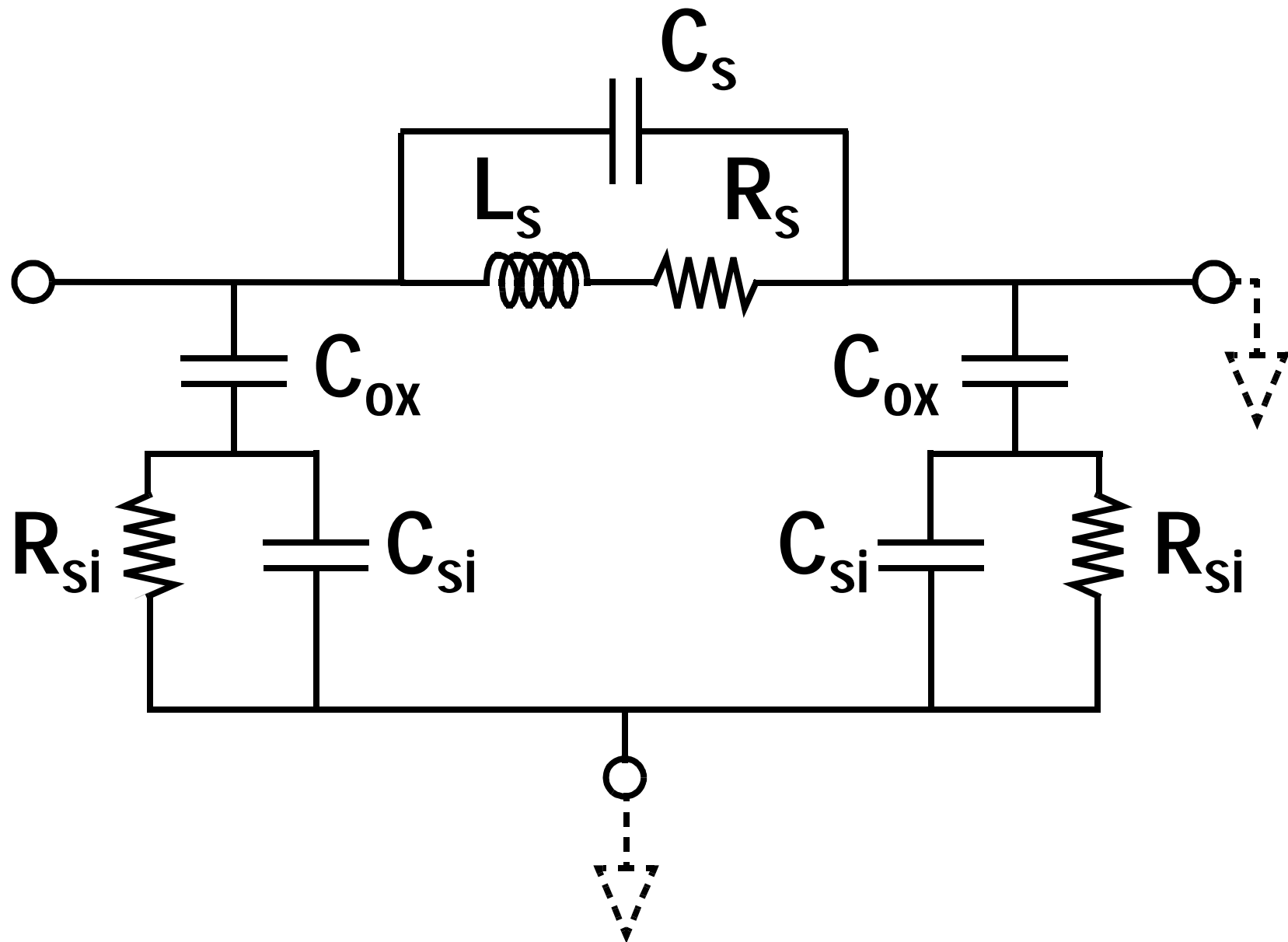
# A Typical Inductor On Silicon



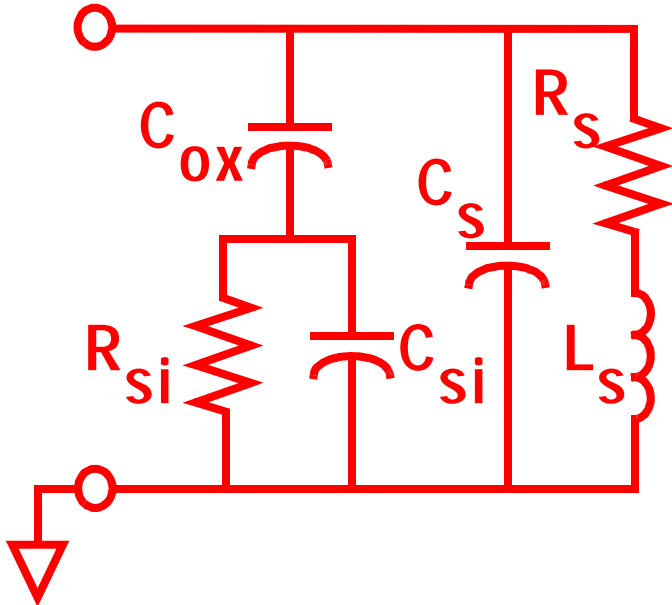
# Model Description



# Model Description

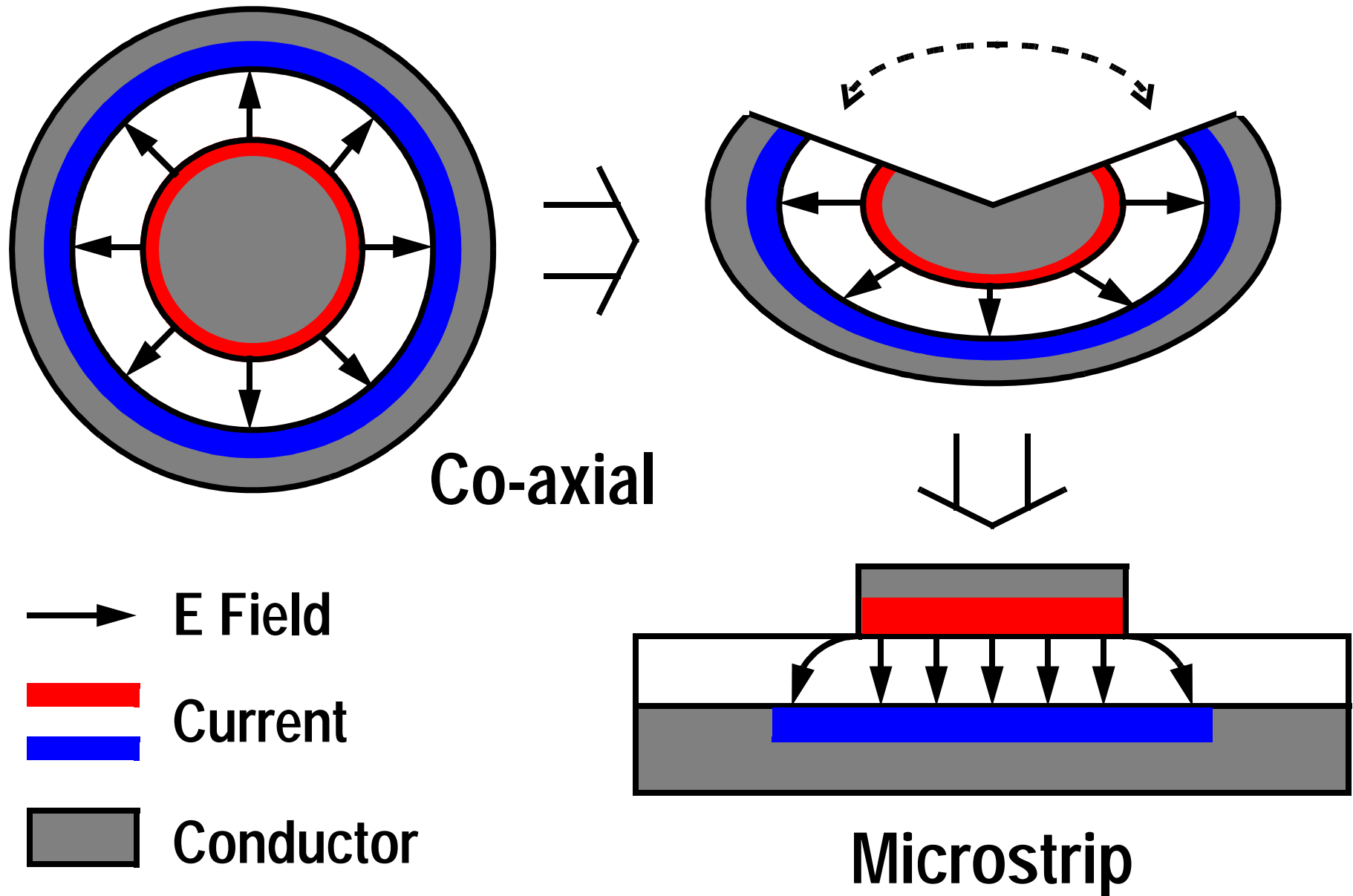


# Model Description

Physical Model of Inductor on Silicon		Effects
	$L_s$ : Greenhouse Method	Mutual Couplings
	$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})}$	Eddy Current
	$C_s = n \cdot w^2 \cdot \frac{\epsilon_{ox}}{t_{ox \text{ M1-M2}}}$	Feed-Through Capacitance
	$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\epsilon_{ox}}{t_{ox}}$	Oxide Capacitance
	$C_{si} = \frac{1}{2} \cdot l \cdot w \cdot C_{Sub}$	Si Substrate Capacitance
	$R_{si} = \frac{2}{l \cdot w \cdot G_{Sub}}$	Si Substrate Ohmic Loss

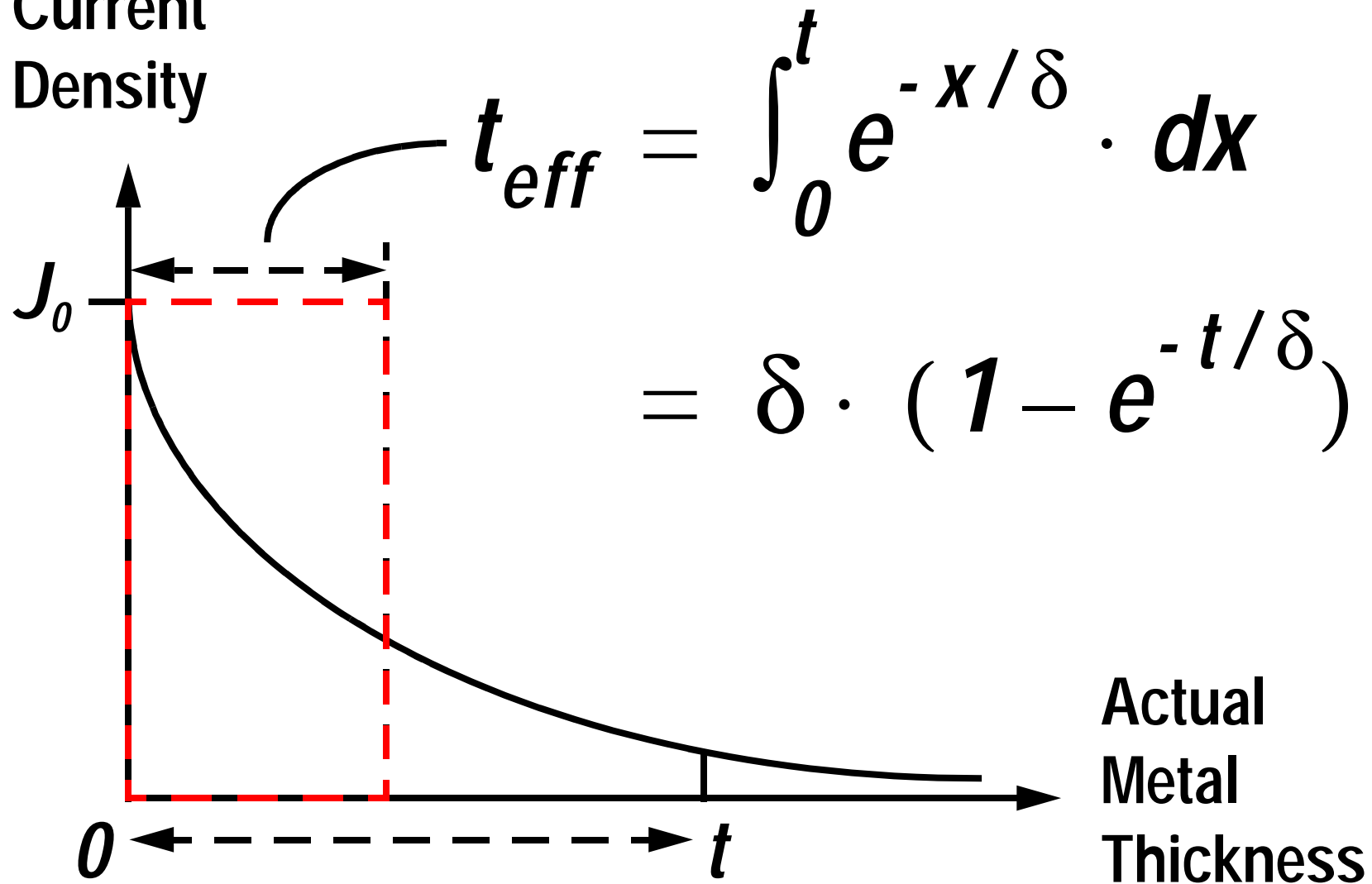


# Skin Effect

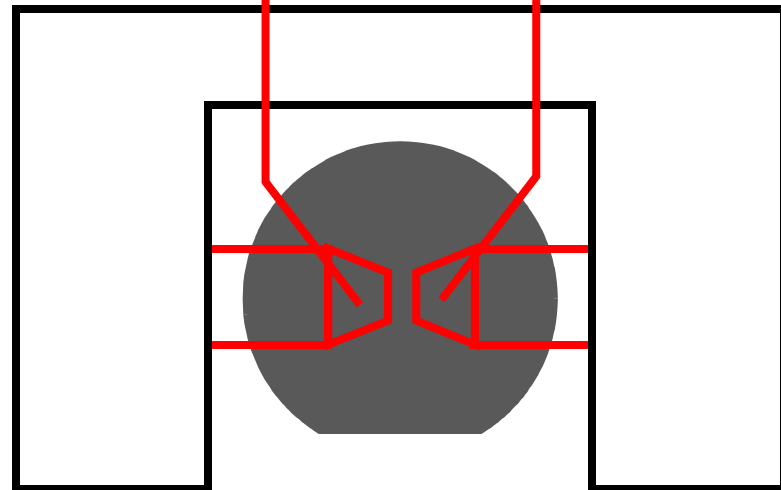
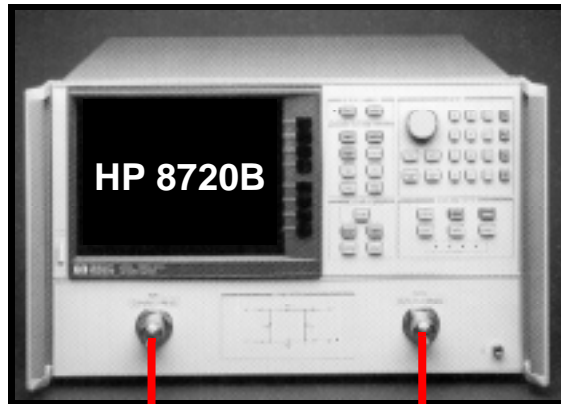


# Effective Metal Thickness

Current  
Density

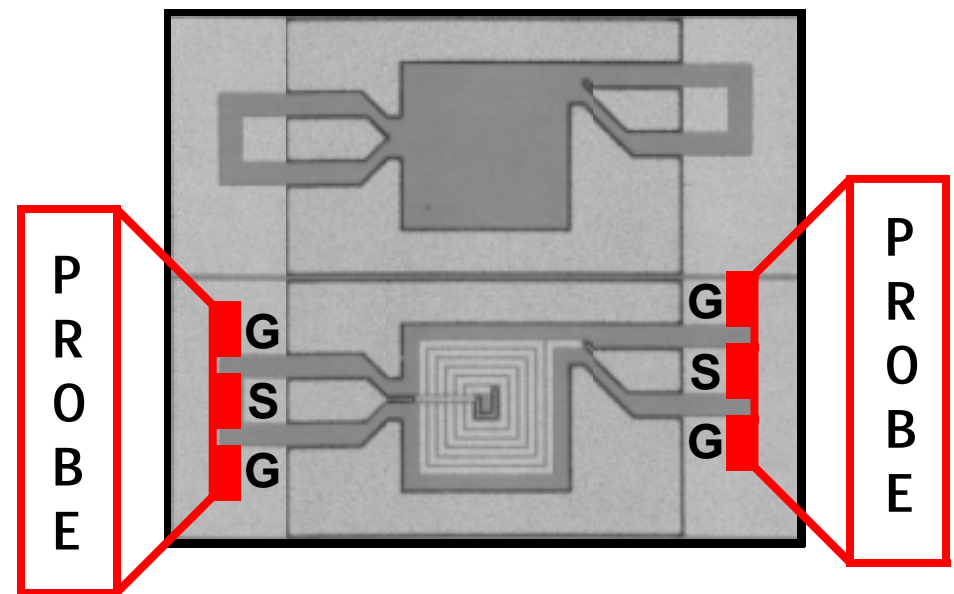


# Measurement Setup



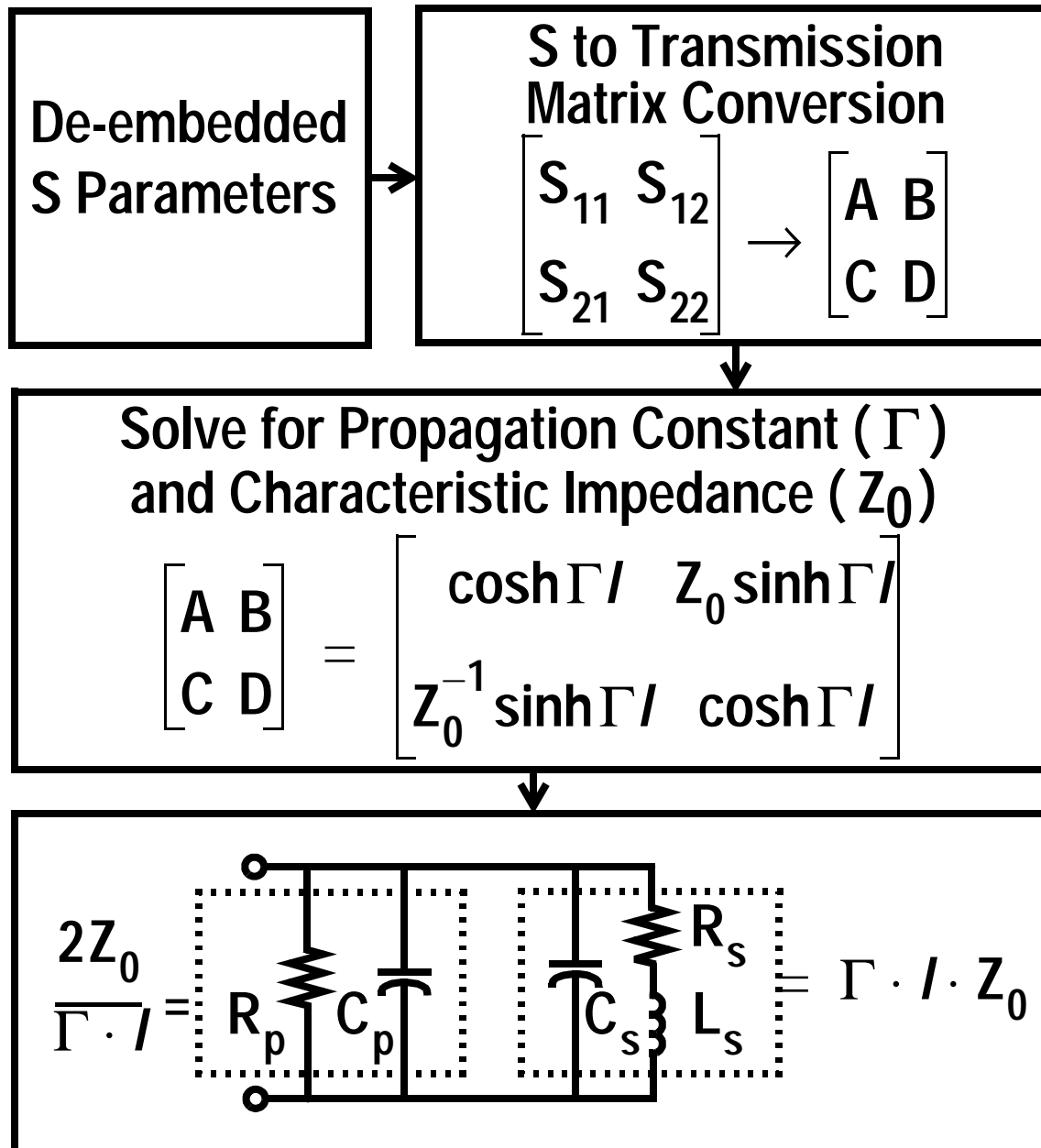
Probe Station

Open Structure

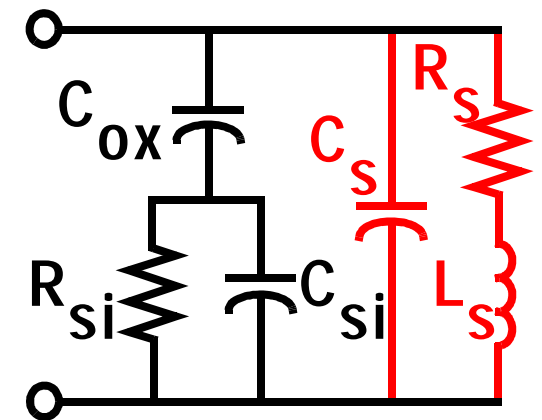
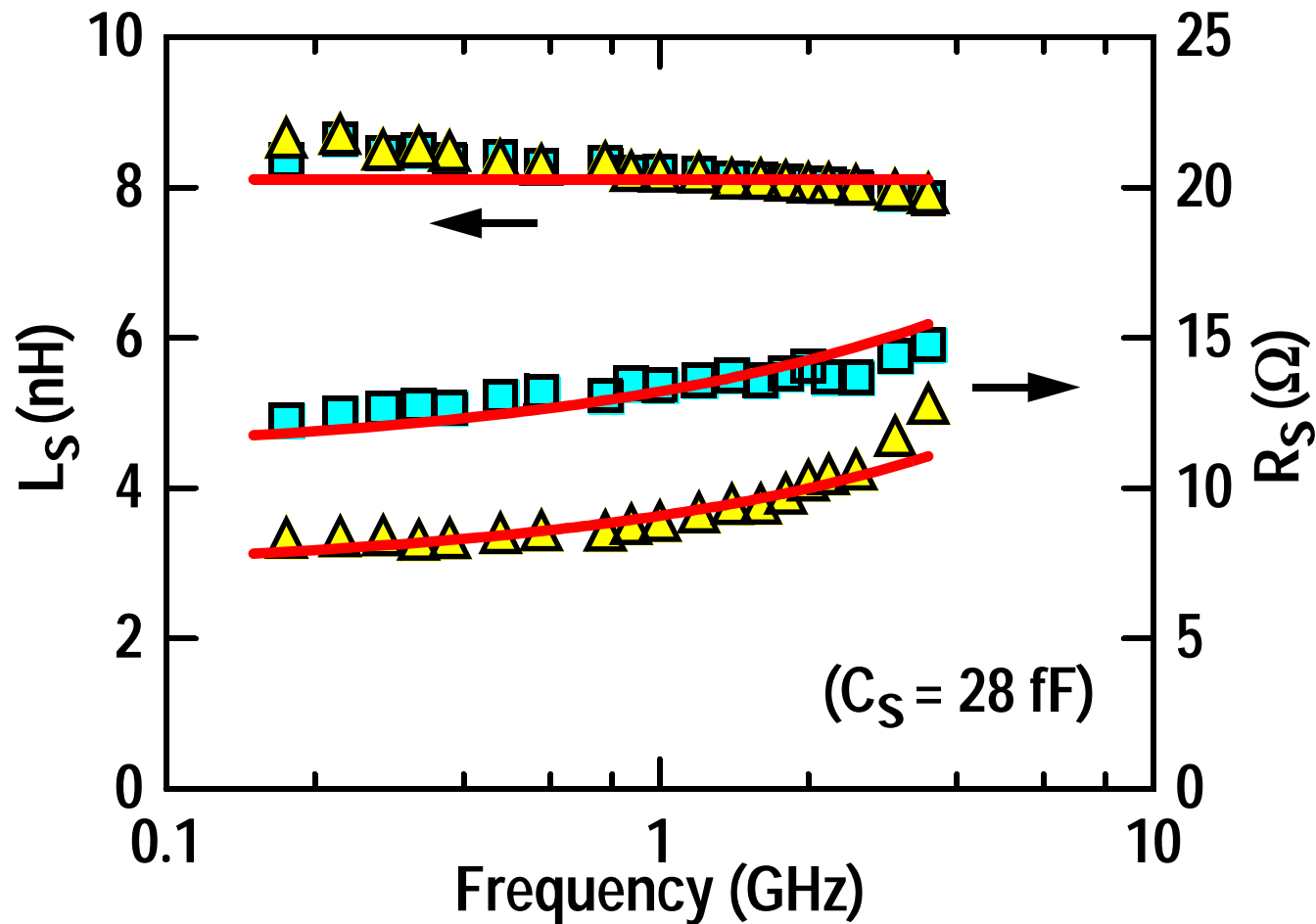


Device Under Test

# Parameter Extraction Procedure

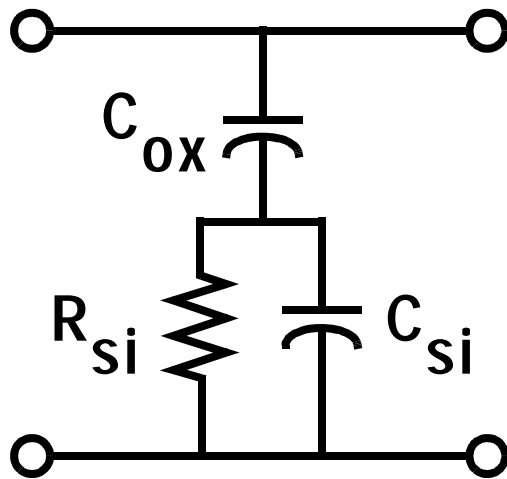


# Measured and Modeled Values of $L_S$ and $R_S$

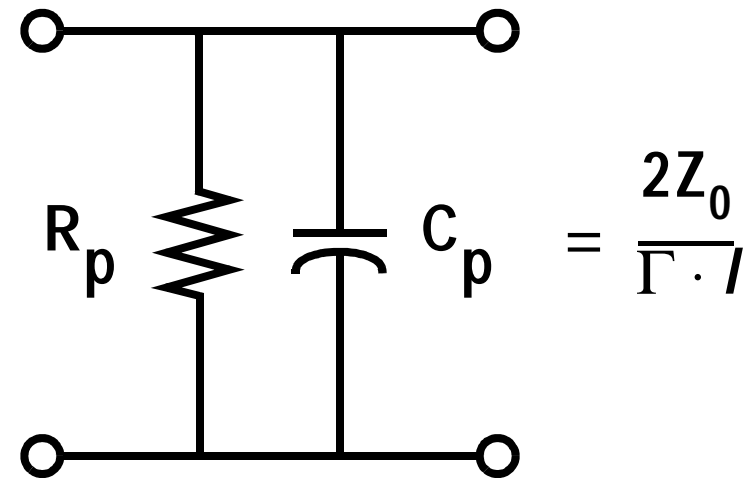


- Yellow Triangle: Copper
- Cyan Square: Aluminum
- Red Line: Model

# Substrate Modeling



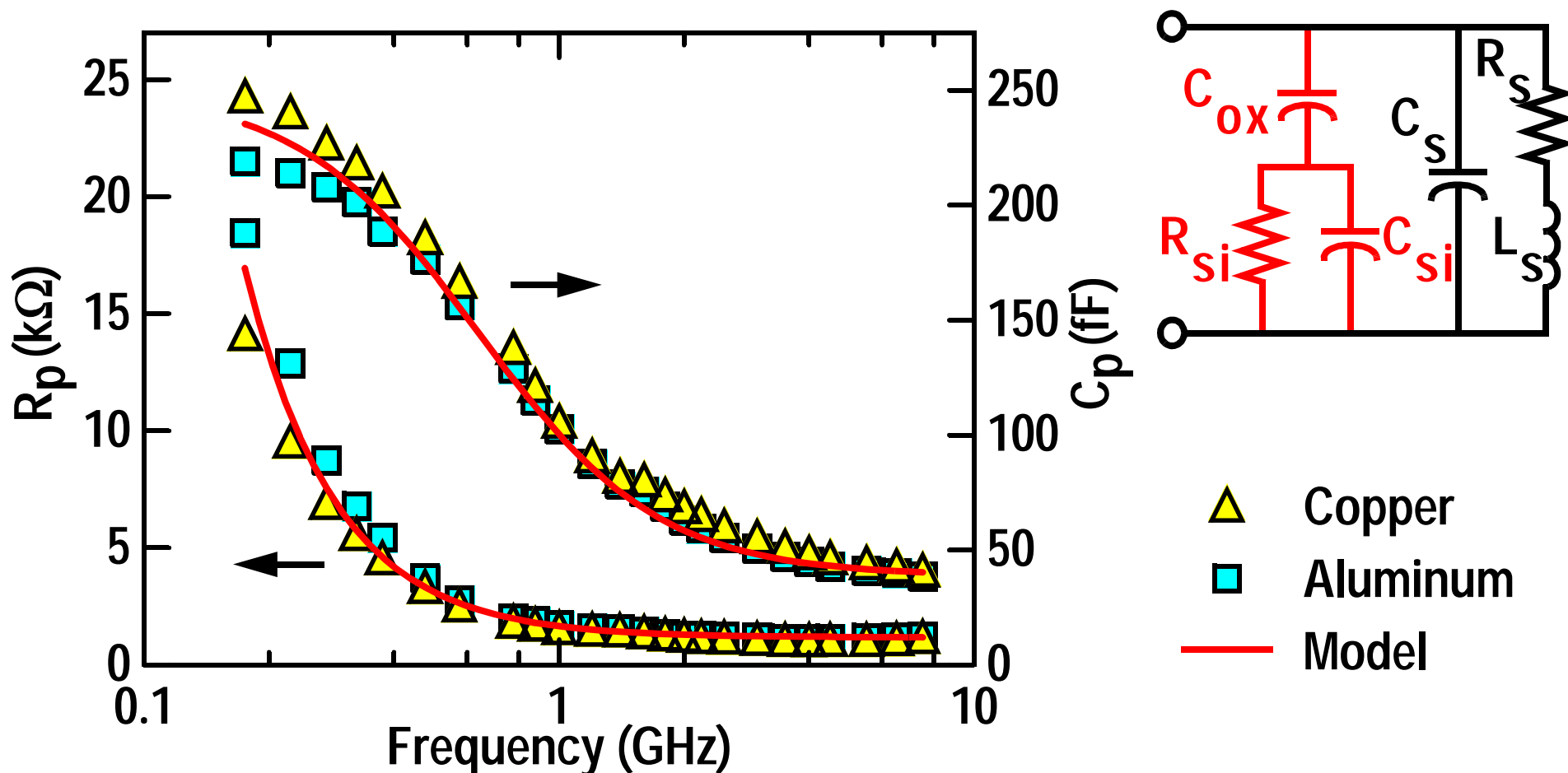
Physical Model



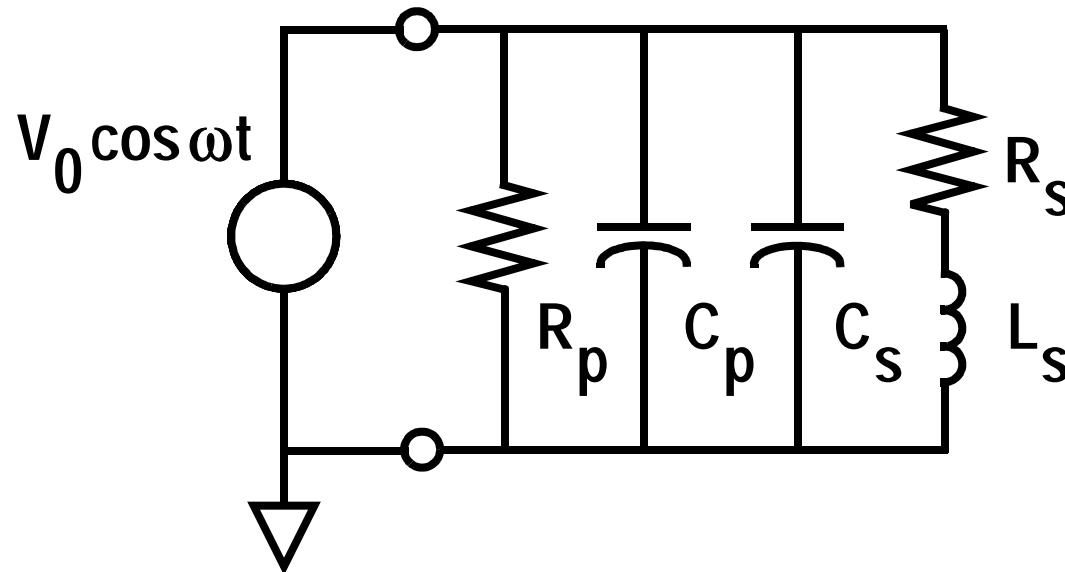
Extracted Capacitance  
and Resistance



# Measured and Modeled Values of $R_p$ and $C_p$



# Definition of Inductor Quality Factor



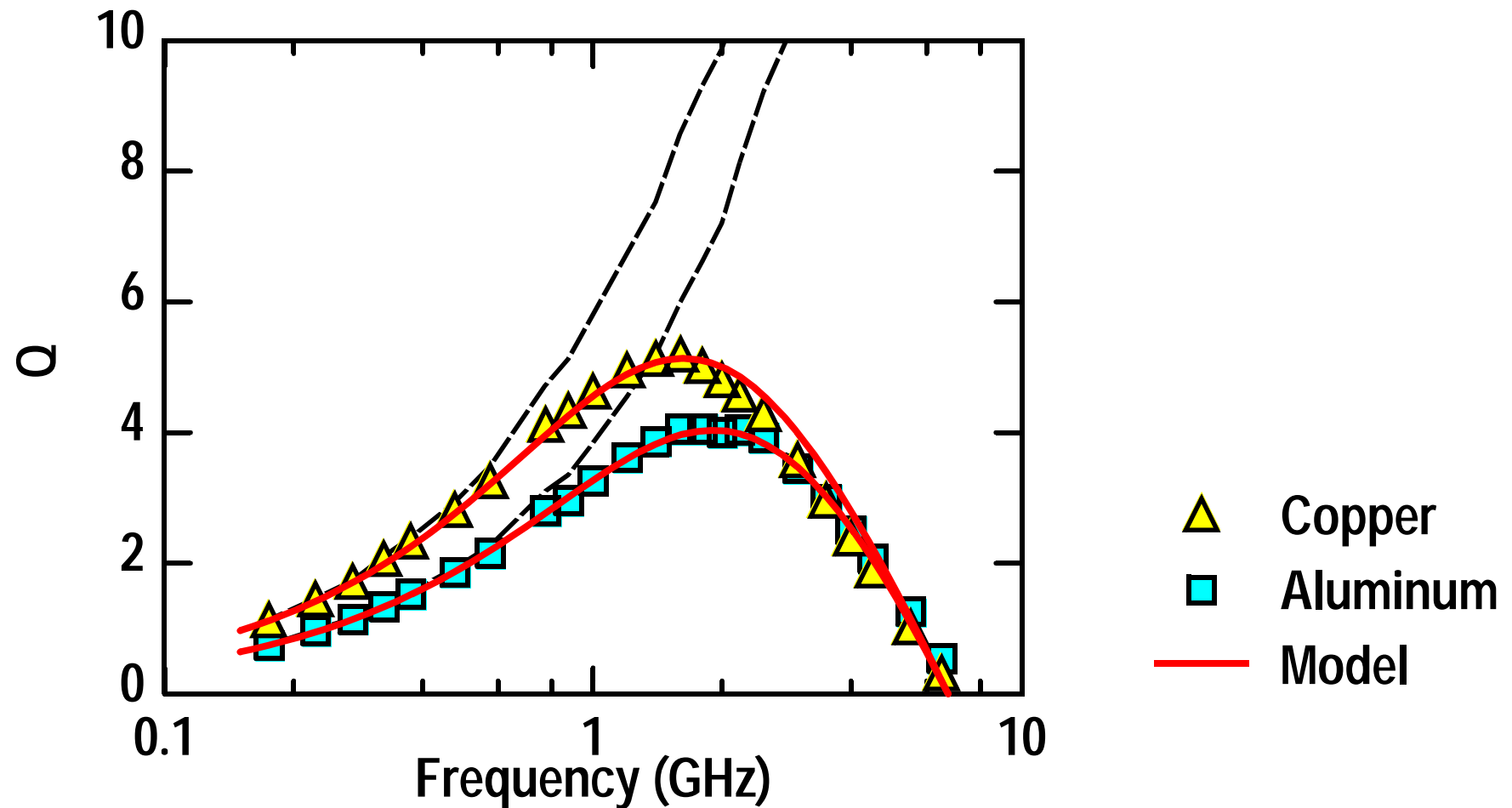
$$Q = 2\pi \frac{|\text{Peak Magnetic Energy} - \text{Peak Electric Energy}|}{\text{Energy Loss in One Oscillation Cycle}}$$

$$\frac{\omega L_s}{R_s} \times \underbrace{\frac{R_p}{R_p + [(\omega L_s / R_s)^2 + 1] \cdot R_s}}_{\text{Substrate Loss Factor}} \times \underbrace{\left( 1 - \frac{R_s^2 (C_p + C_s)}{L_s} - \omega^2 L_s (C_p + C_s) \right)}_{\text{Self-Resonance Factor}}$$

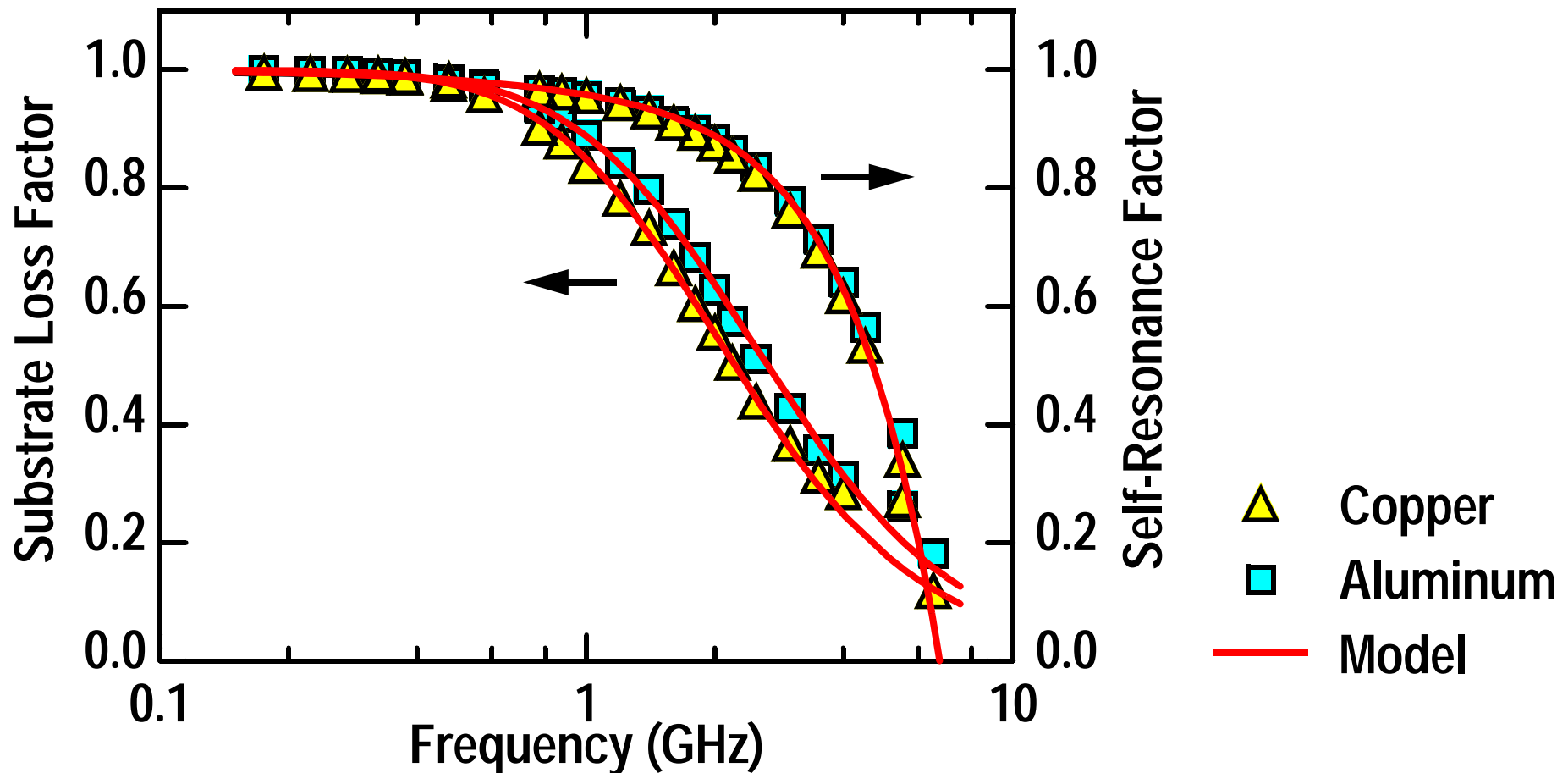
Substrate Loss Factor

Self-Resonance Factor

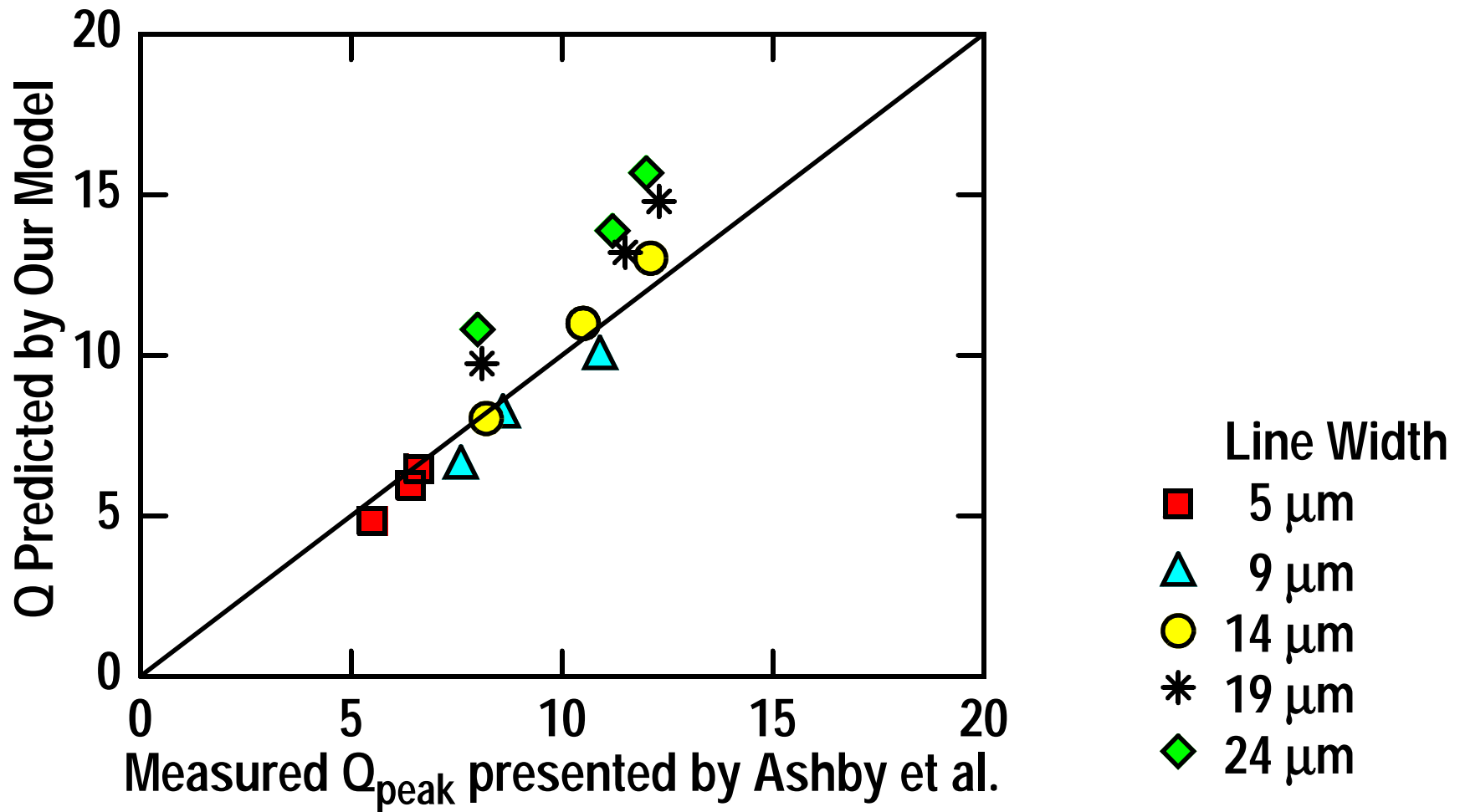
# Measured and Modeled Value of $Q$



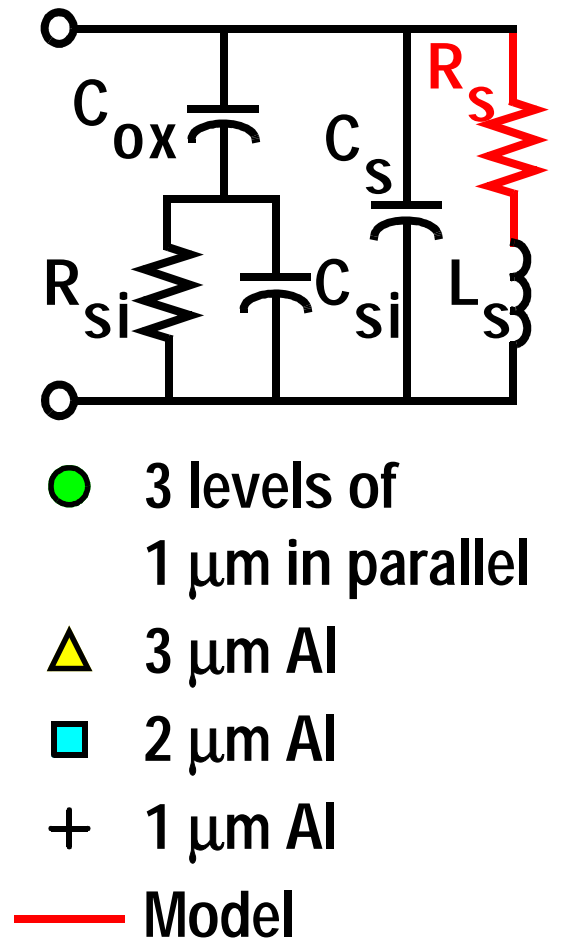
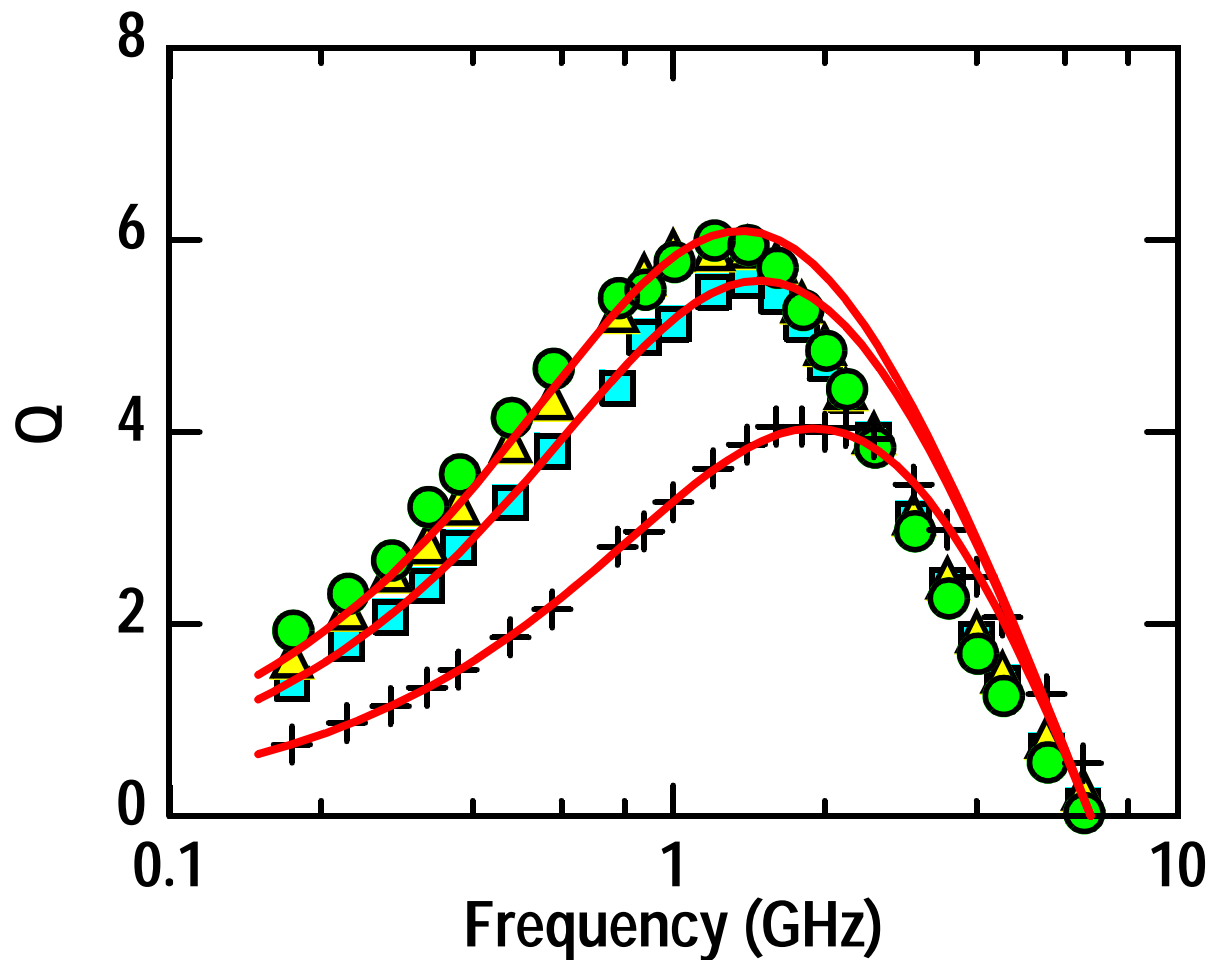
# Measured and Modeled Values of Substrate Factors



# Comparison to Published Results

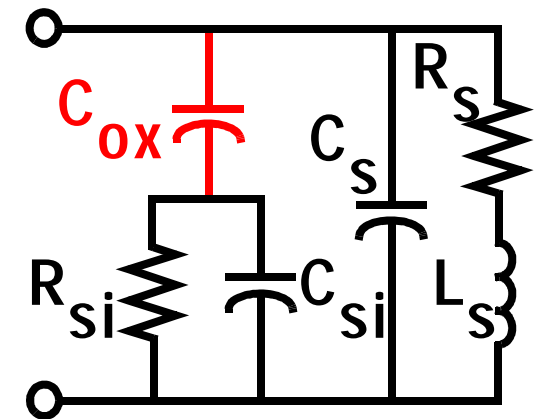
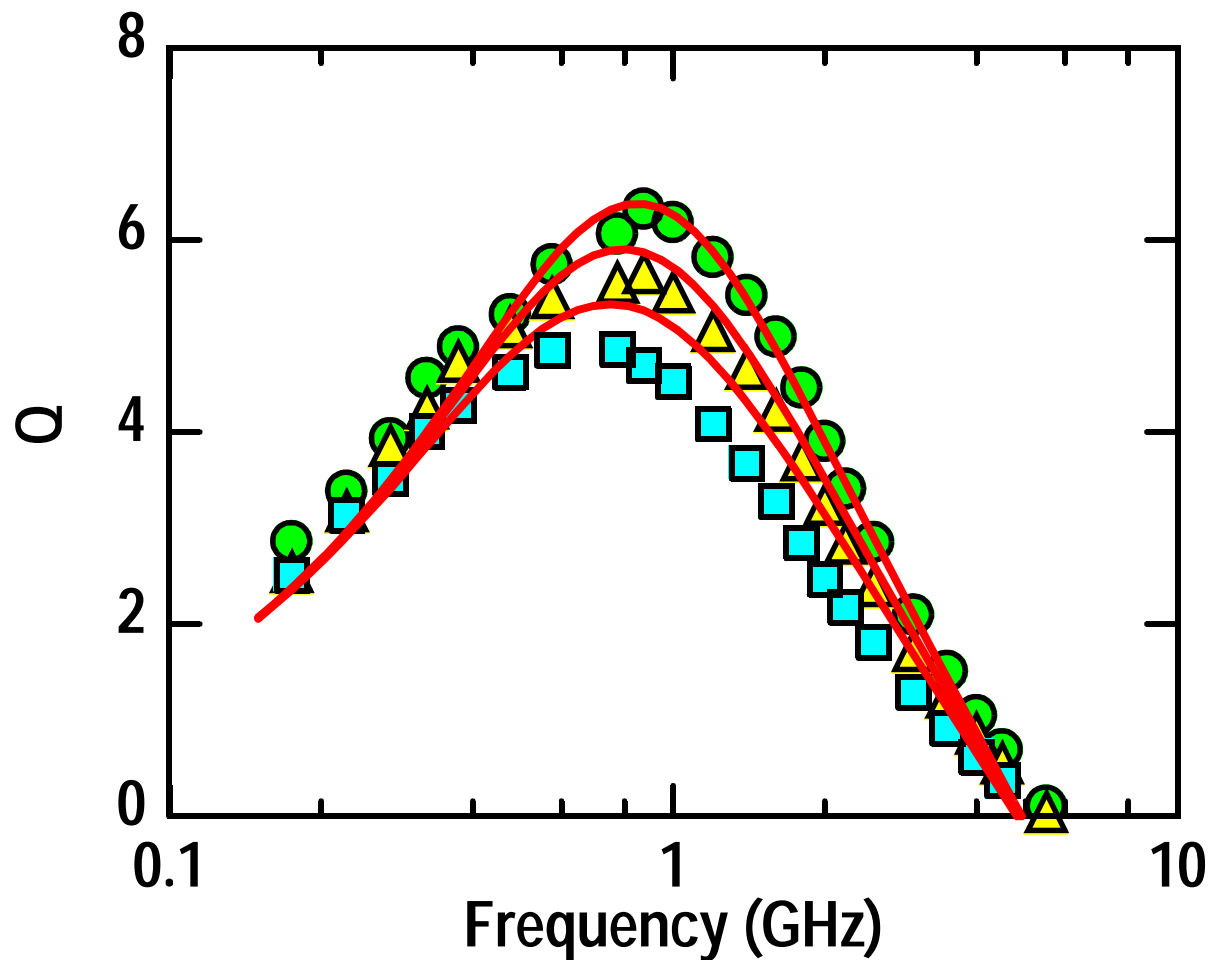


# Effect of Metal Scheme on Q



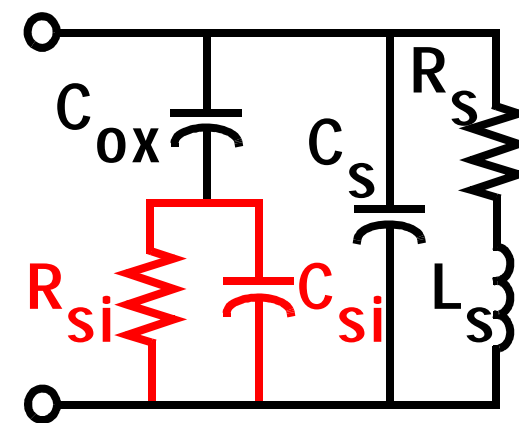
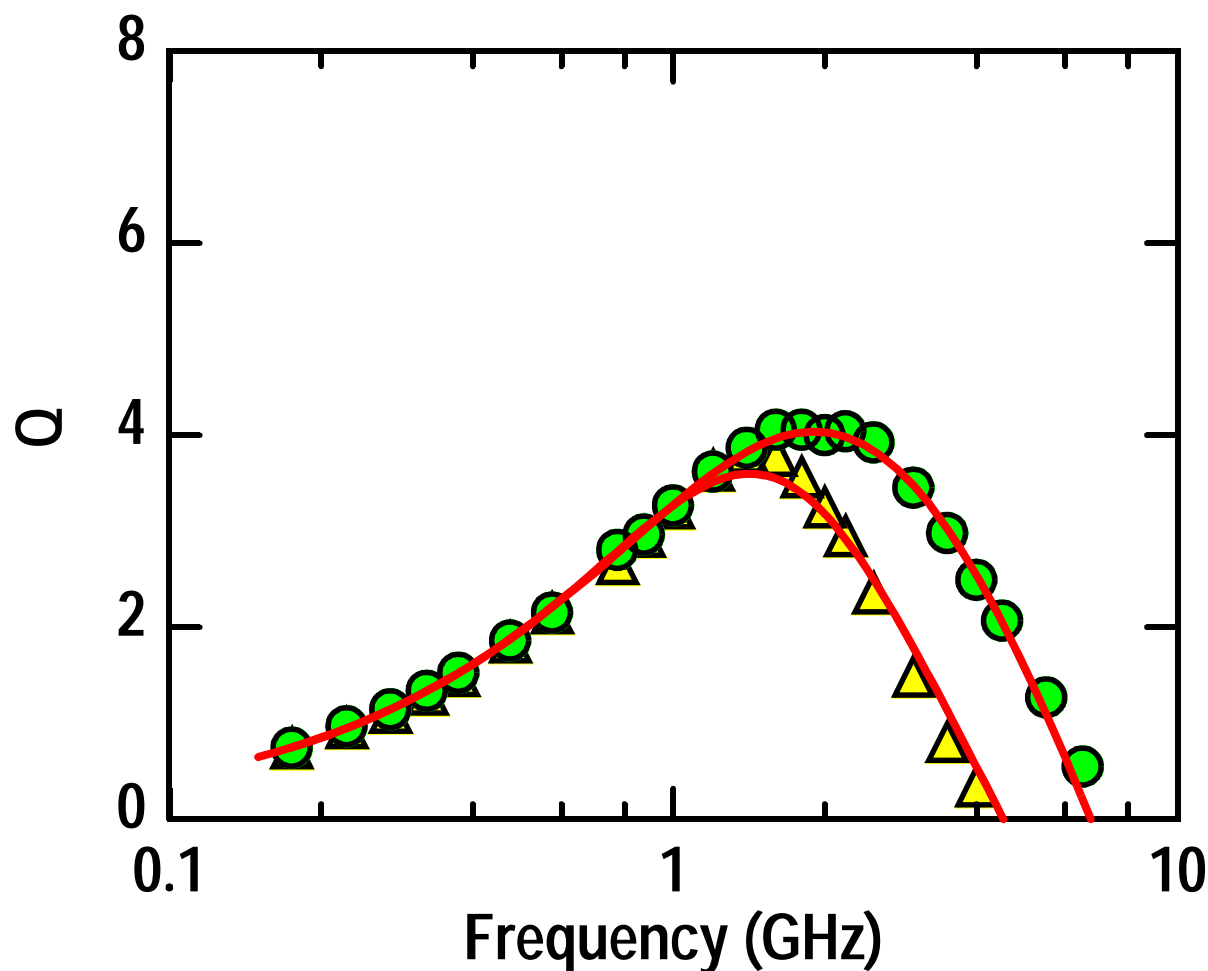


# Effect of Oxide Thickness on Q



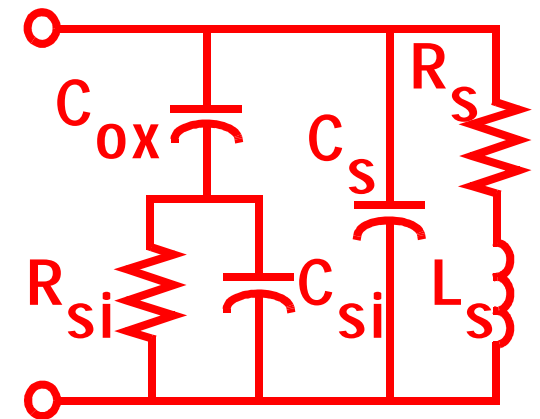
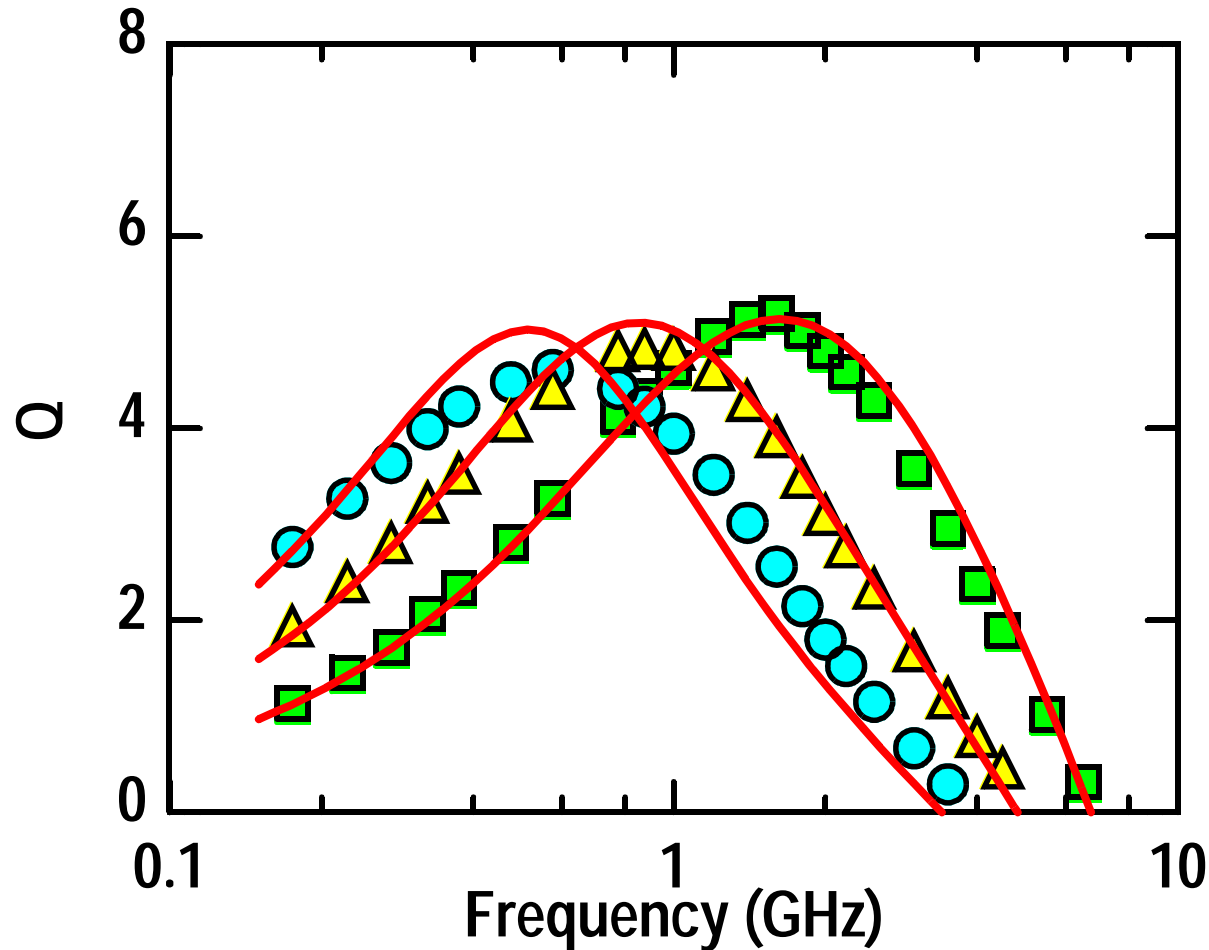
- 6.5  $\mu\text{m}$  Oxide
- ▲ 4.5  $\mu\text{m}$  Oxide
- 2.5  $\mu\text{m}$  Oxide
- Model

# Effect of Substrate Resistivity on Q



- 10 Ω-cm Si:  
 $C_{sub} = 1.6 \times 10^{-3} \text{ fF}/\mu\text{m}^2$   
 $G_{sub} = 4.0 \times 10^{-8} \text{ S}/\mu\text{m}^2$
- ▲ 6 Ω-cm Si:  
 $C_{sub} = 6.0 \times 10^{-3} \text{ fF}/\mu\text{m}^2$   
 $G_{sub} = 1.6 \times 10^{-7} \text{ S}/\mu\text{m}^2$
- Model

# Effect of Layout Area on Q



Outer Dimension  
Line Width

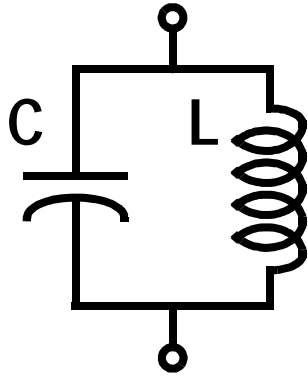
● 550 μm, 41 μm

▲ 400 μm, 24 μm

■ 300 μm, 13 μm

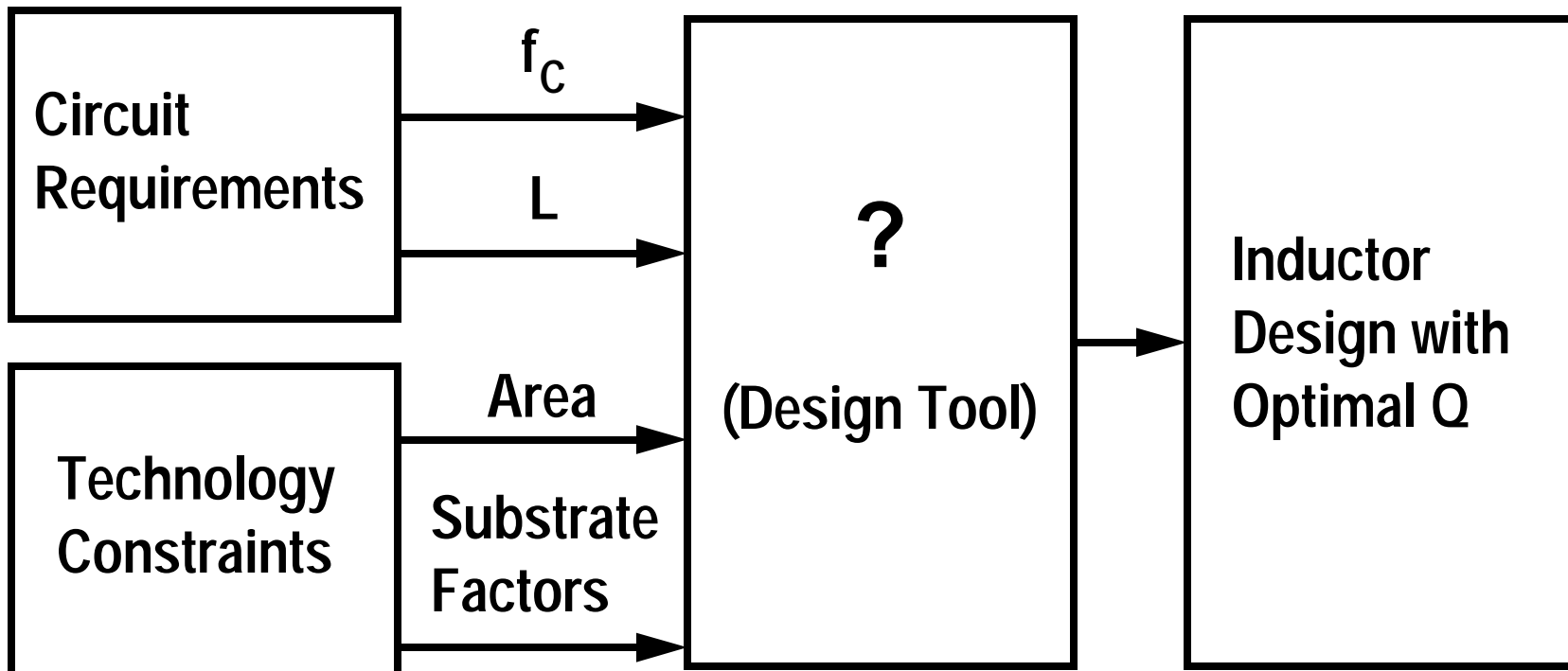
— Model

# Application of Model

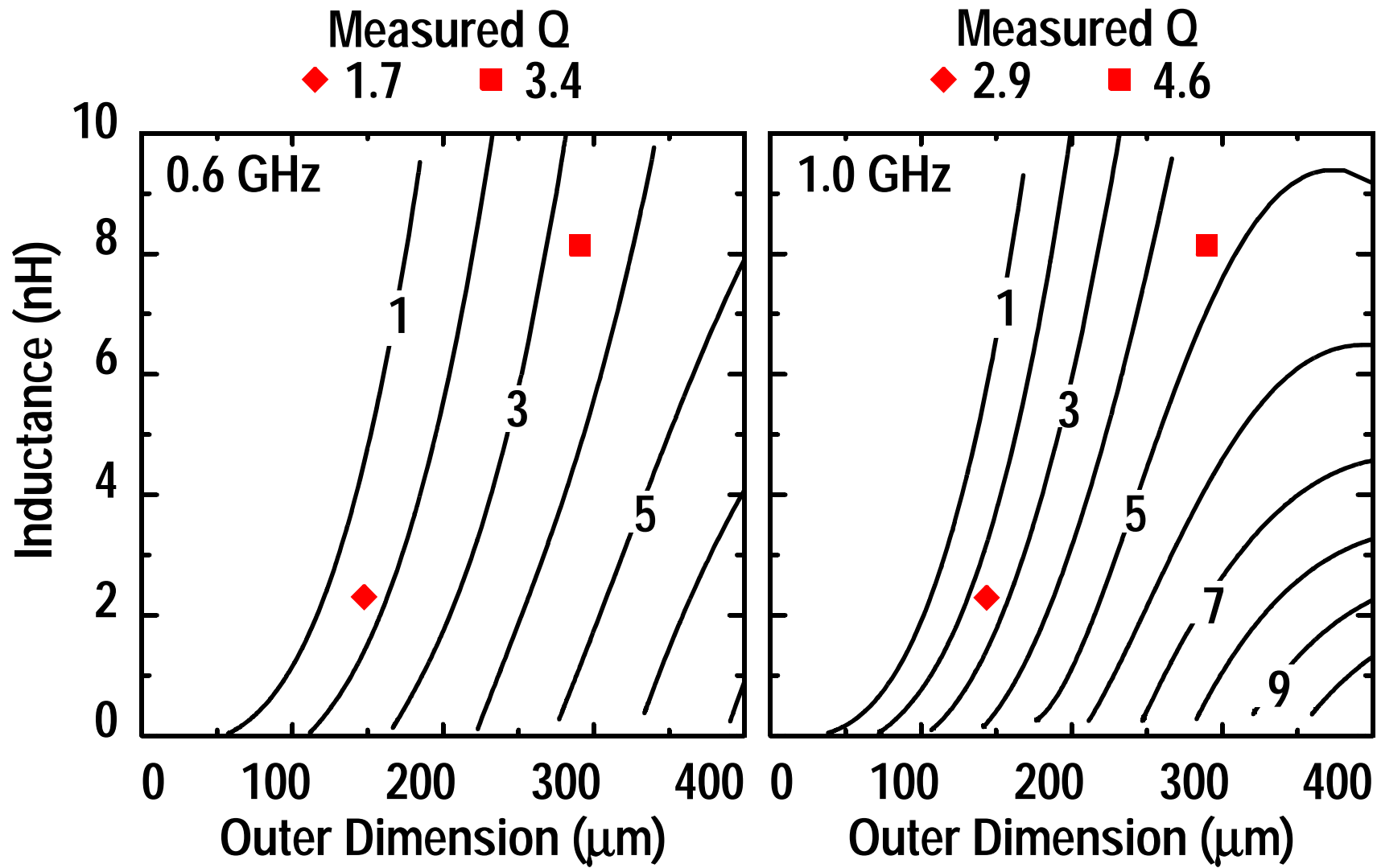


$$f_c = \frac{1}{2\pi\sqrt{L \cdot C}}$$

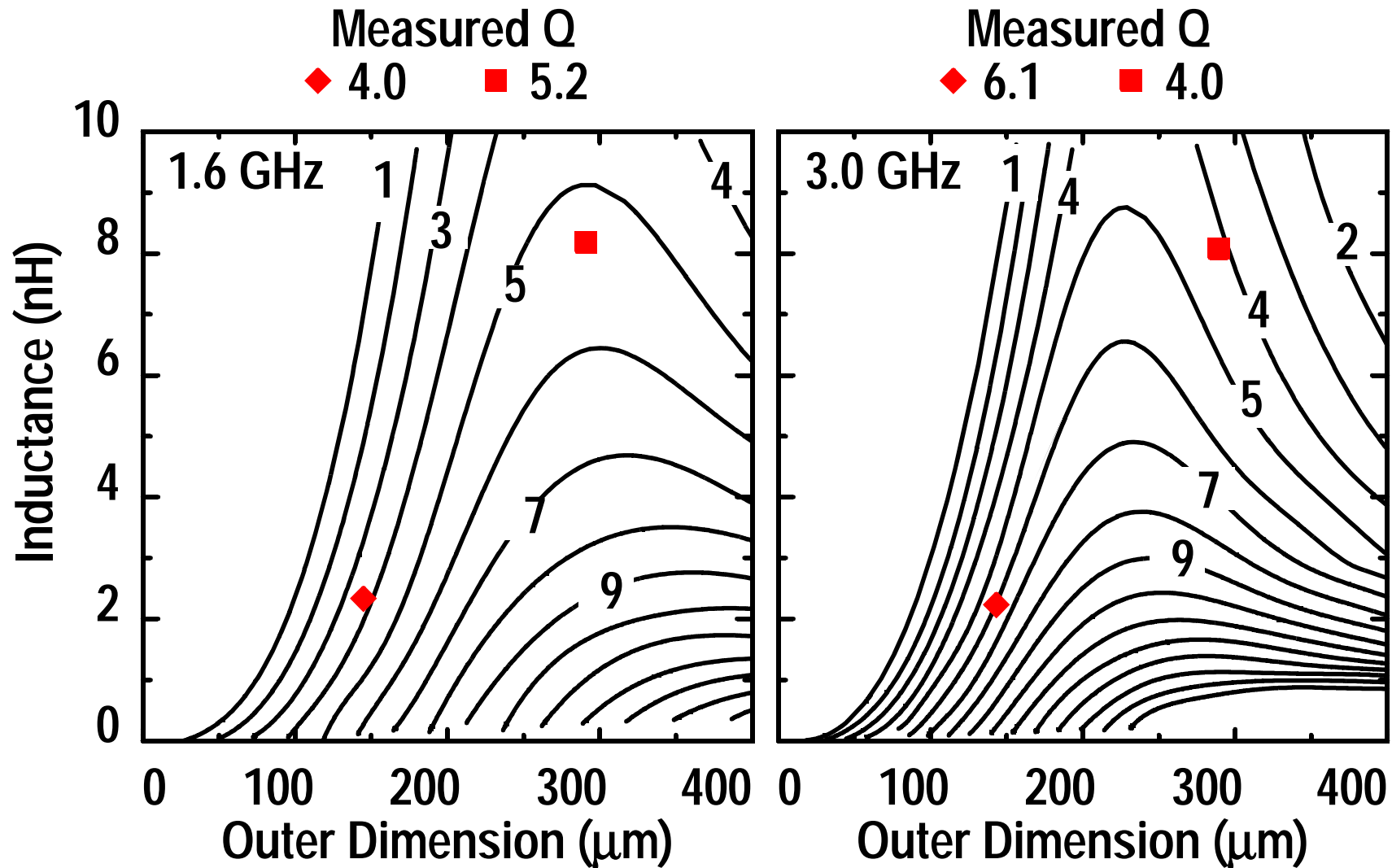
$$f_c = 1.6 \text{ GHz}, C = 1.2 \text{ pF} \rightarrow L = 8 \text{ nH}$$



# Contour Plots of Q



# Contour Plots of Q





# Outline

- Overview
- A physical model for on-chip inductors
- Effects of process and layout parameters
- Design methodology
- Inductors with patterned ground shields
- Substrate noise coupling
- Conclusions

# Overview

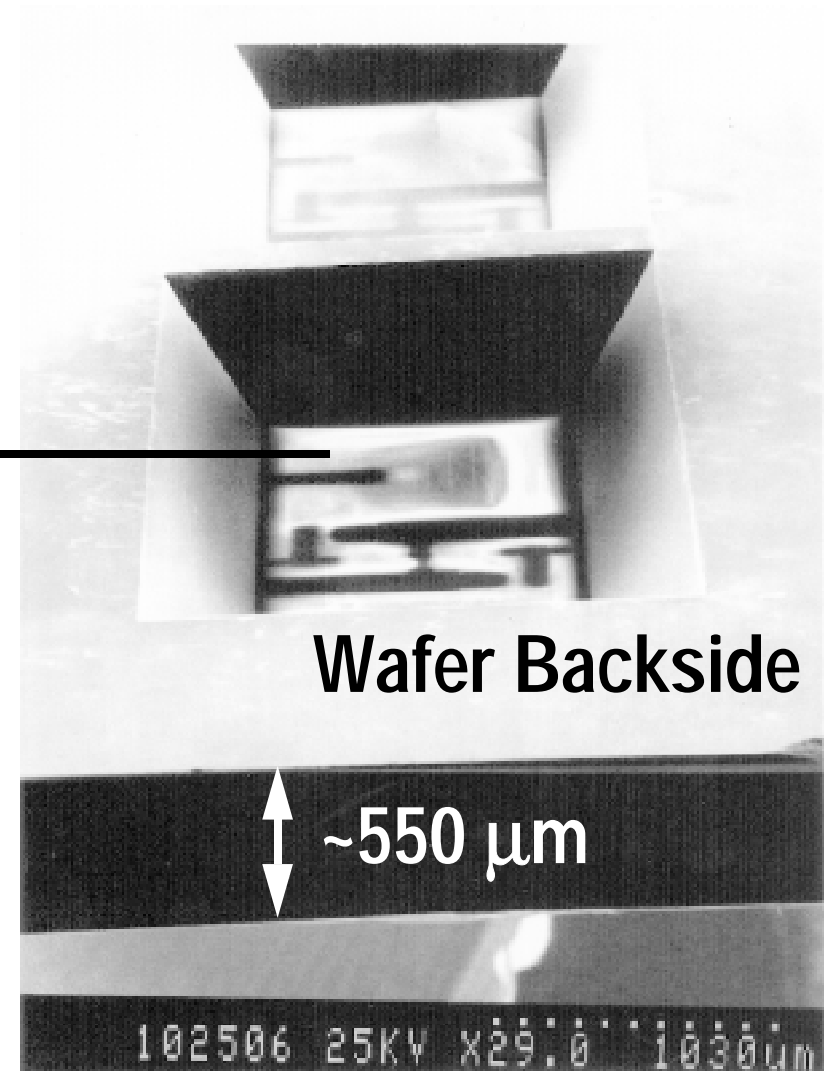
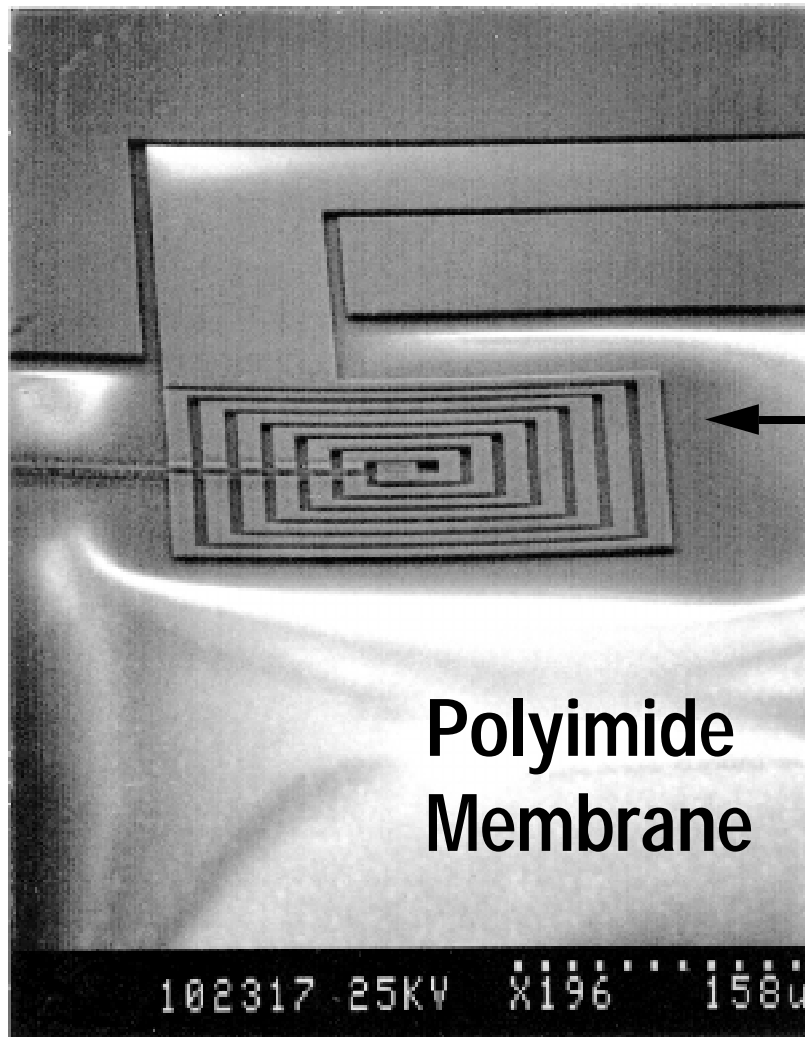
- Challenges

- Q degraded by substrate loss
- Substrate coupling
- Modeling and characterization
- Process constraints

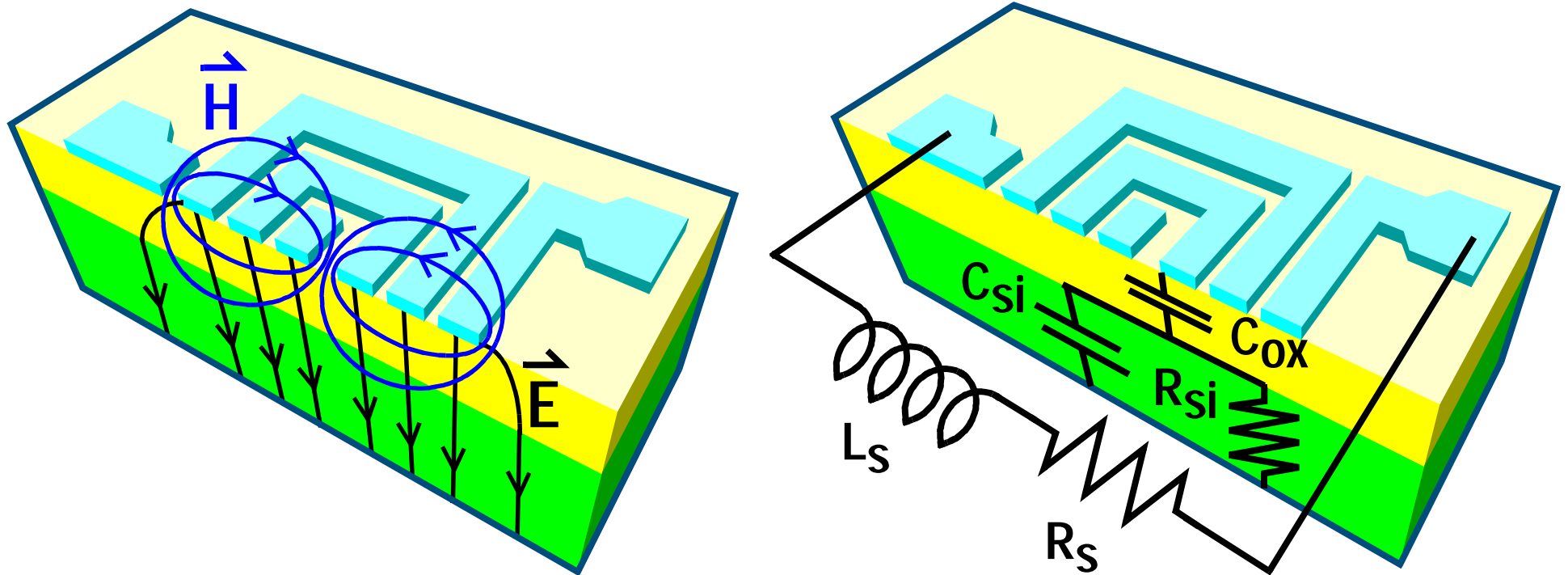
- Approaches

- Etch away Si substrate
- **Patterned Ground Shield**

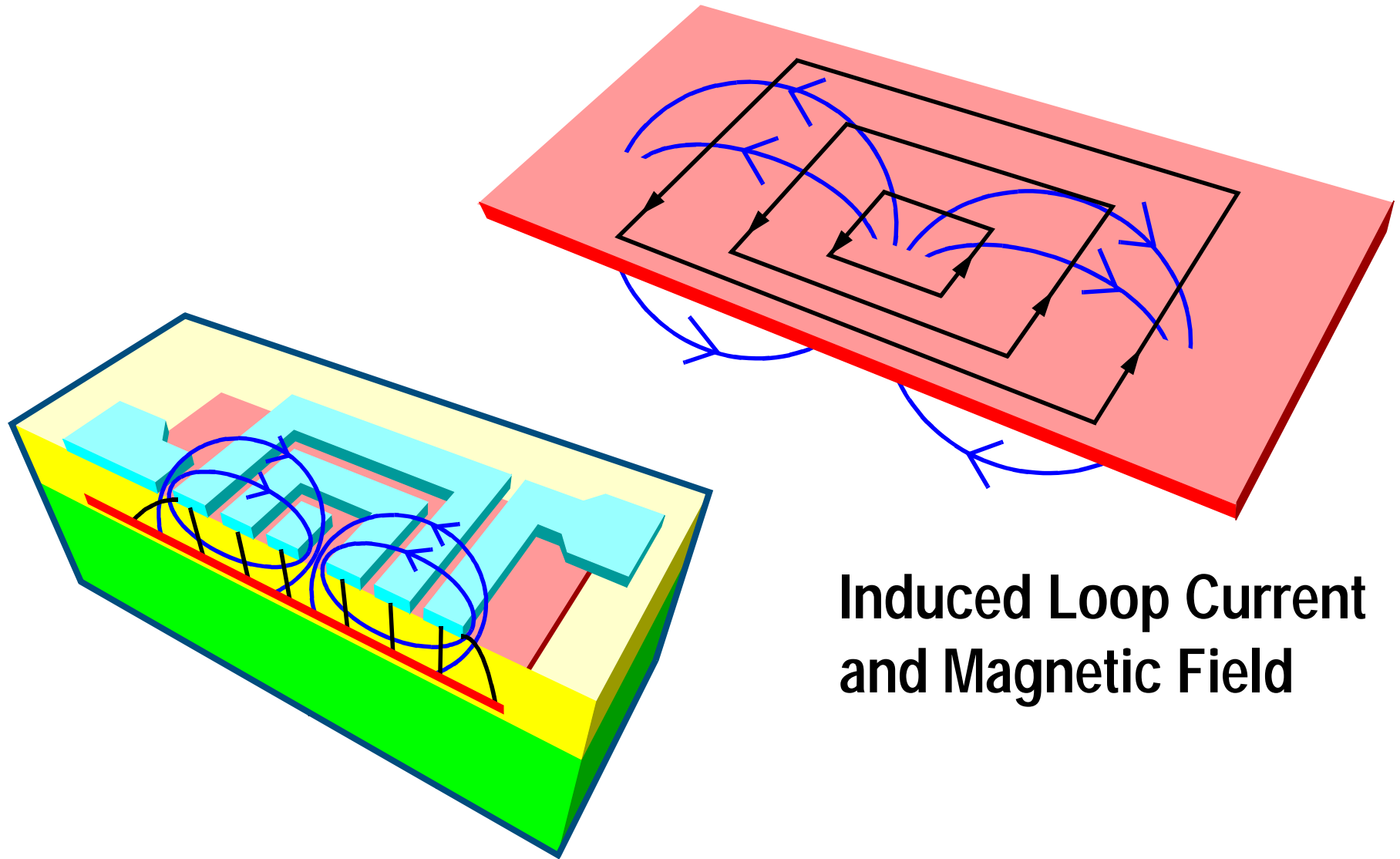
# Suspended Inductors



# Electromagnetic Fields of Conventional On-Chip Inductors

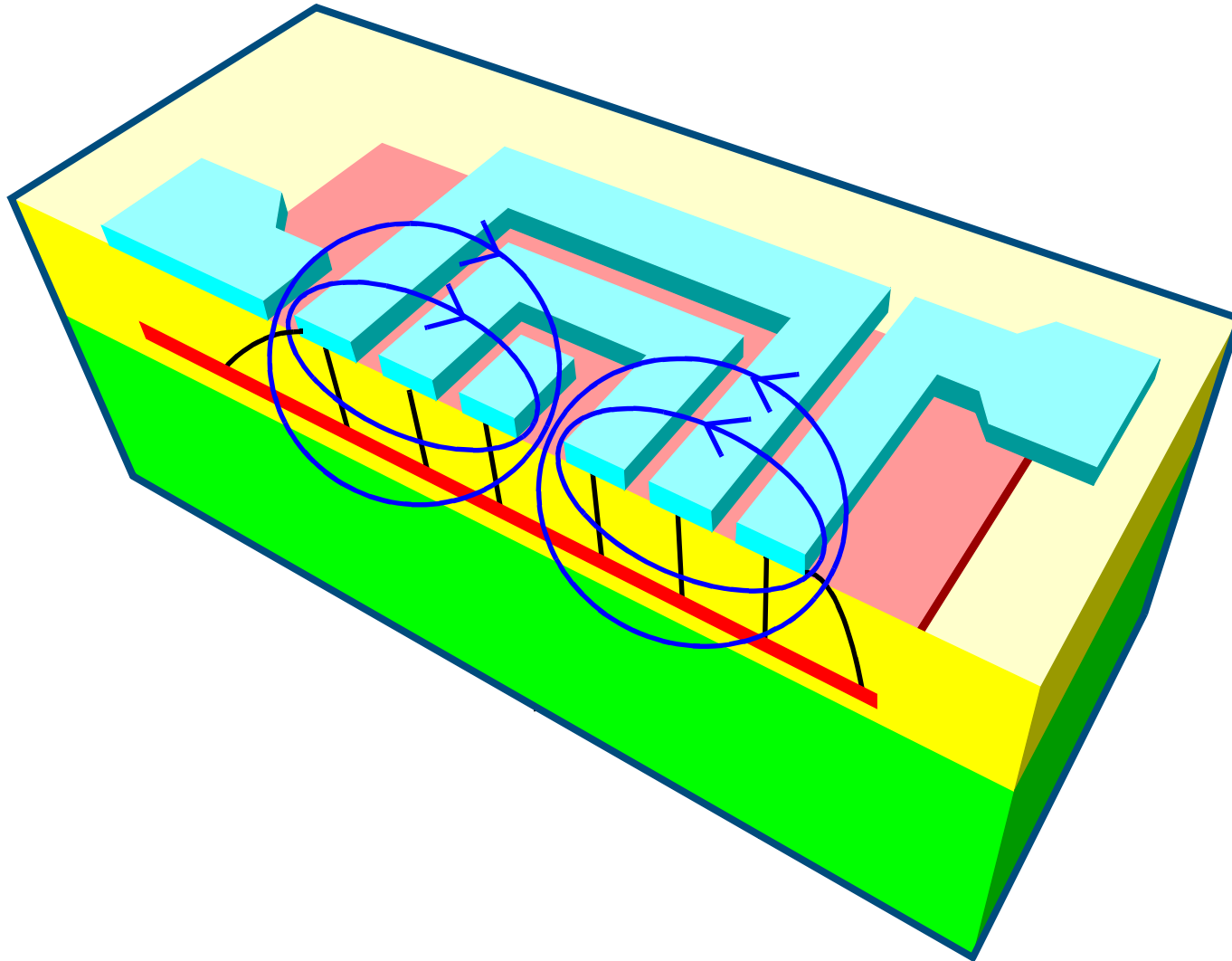


# Problems with Solid Ground Shield



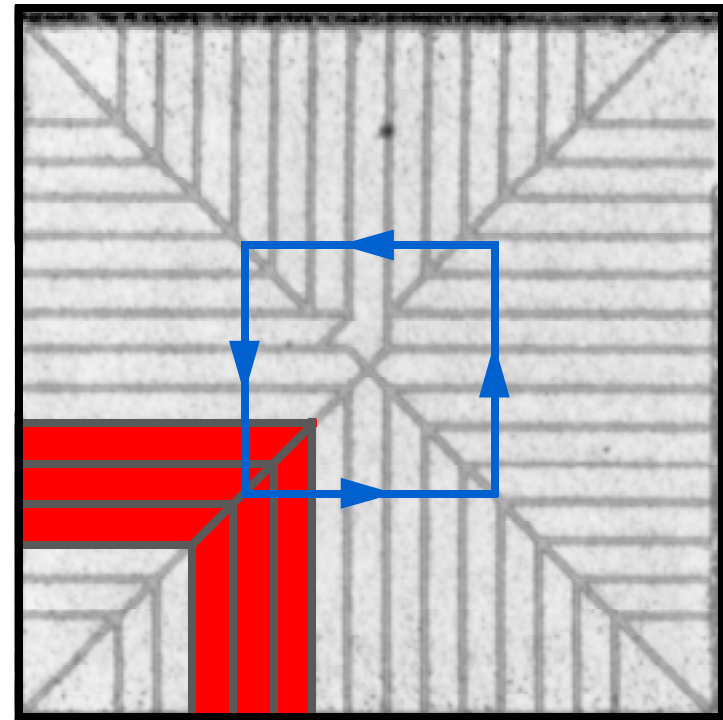
**Induced Loop Current  
and Magnetic Field**

# EM Fields of On-Chip Inductors with Patterned Ground Shield



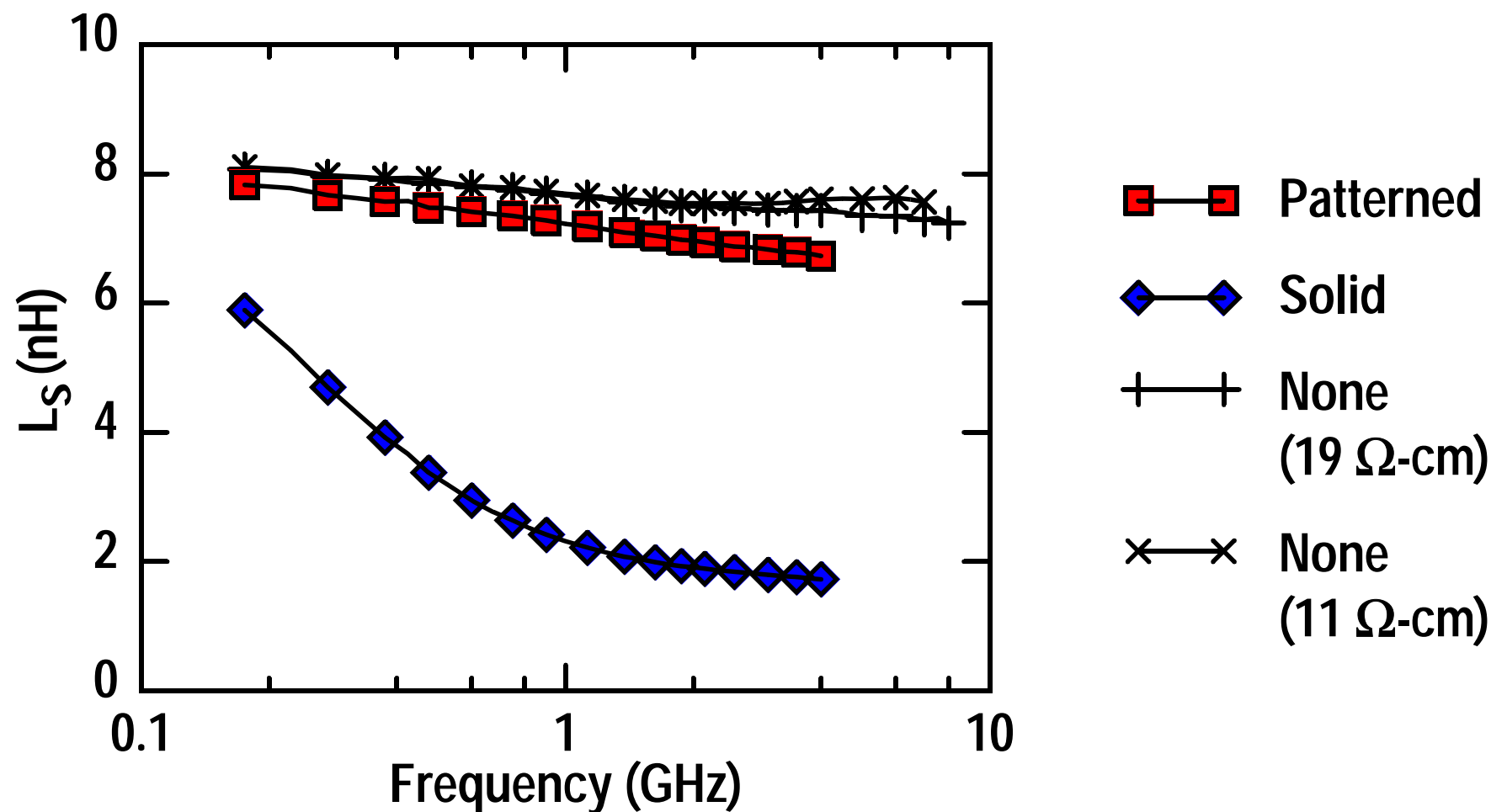
# Patterned Ground Shield Design

- Pattern
  - Orthogonal to spiral  
(induced loop current)
- Resistance
  - Low for termination of  
the electric field
  - Avoid attenuation of  
the magnetic field



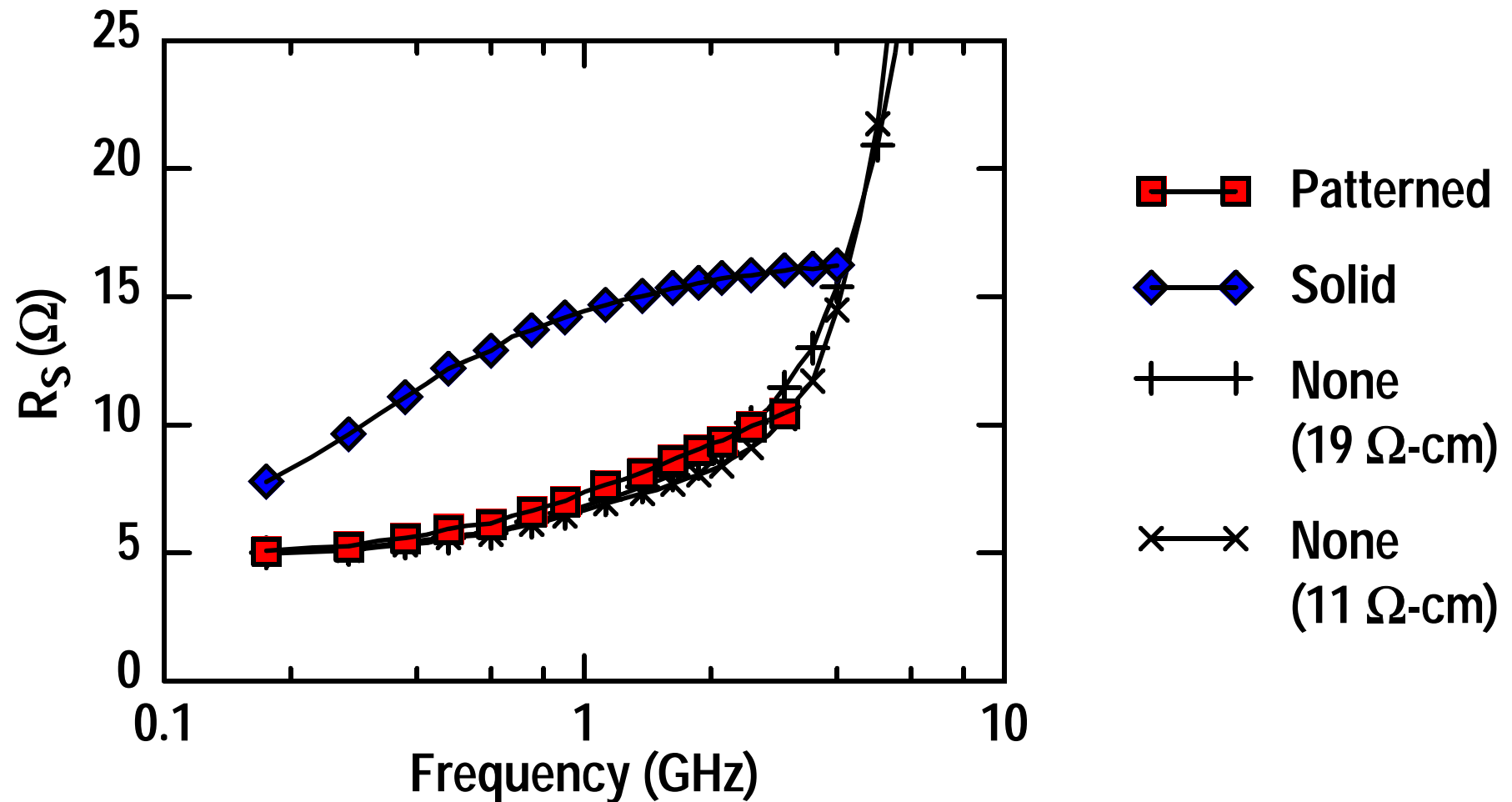
- Ground Strips
- Slot between Strips
- Induced Loop Current

# Effect of Aluminum Ground Shields on L

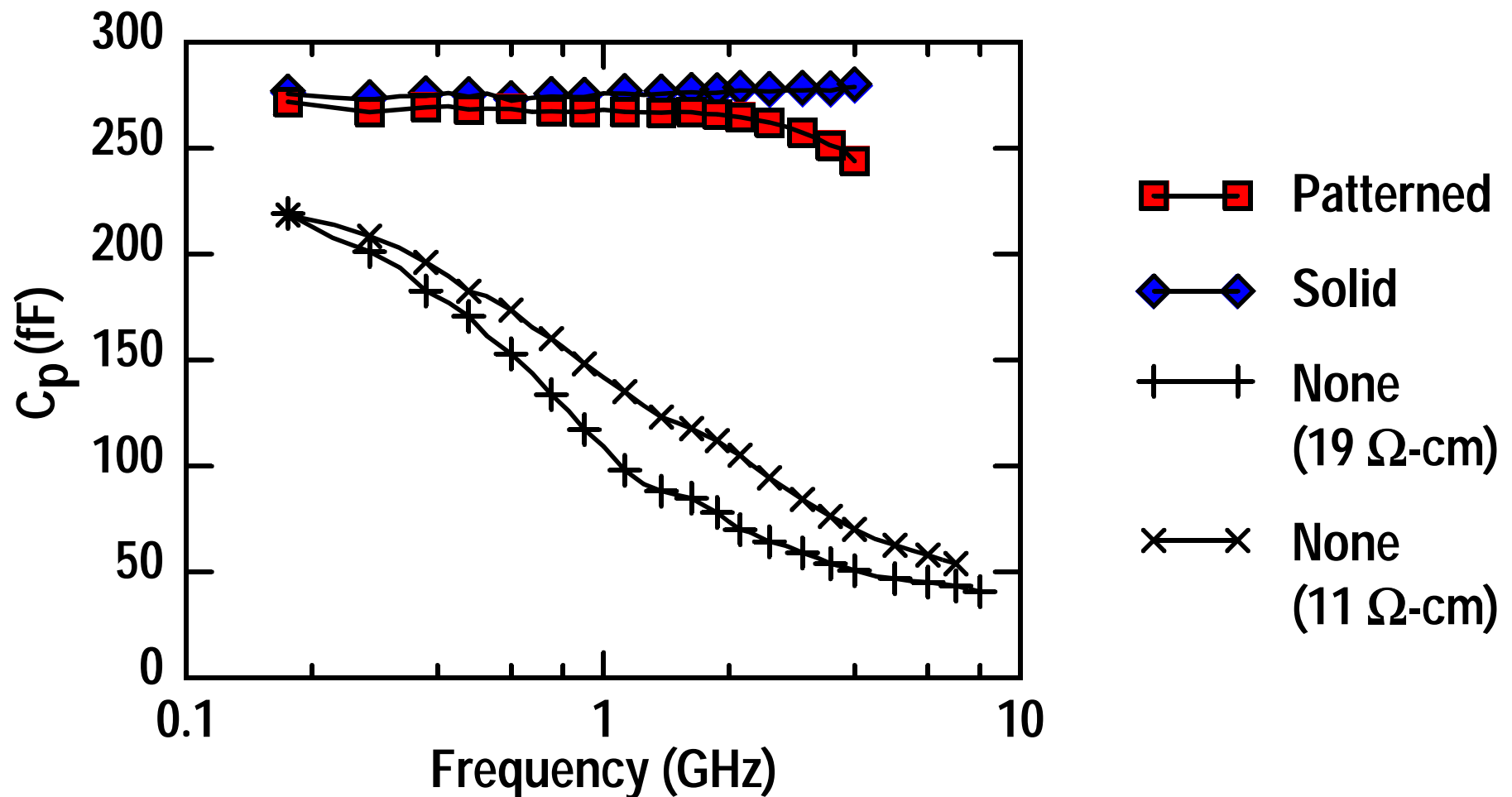




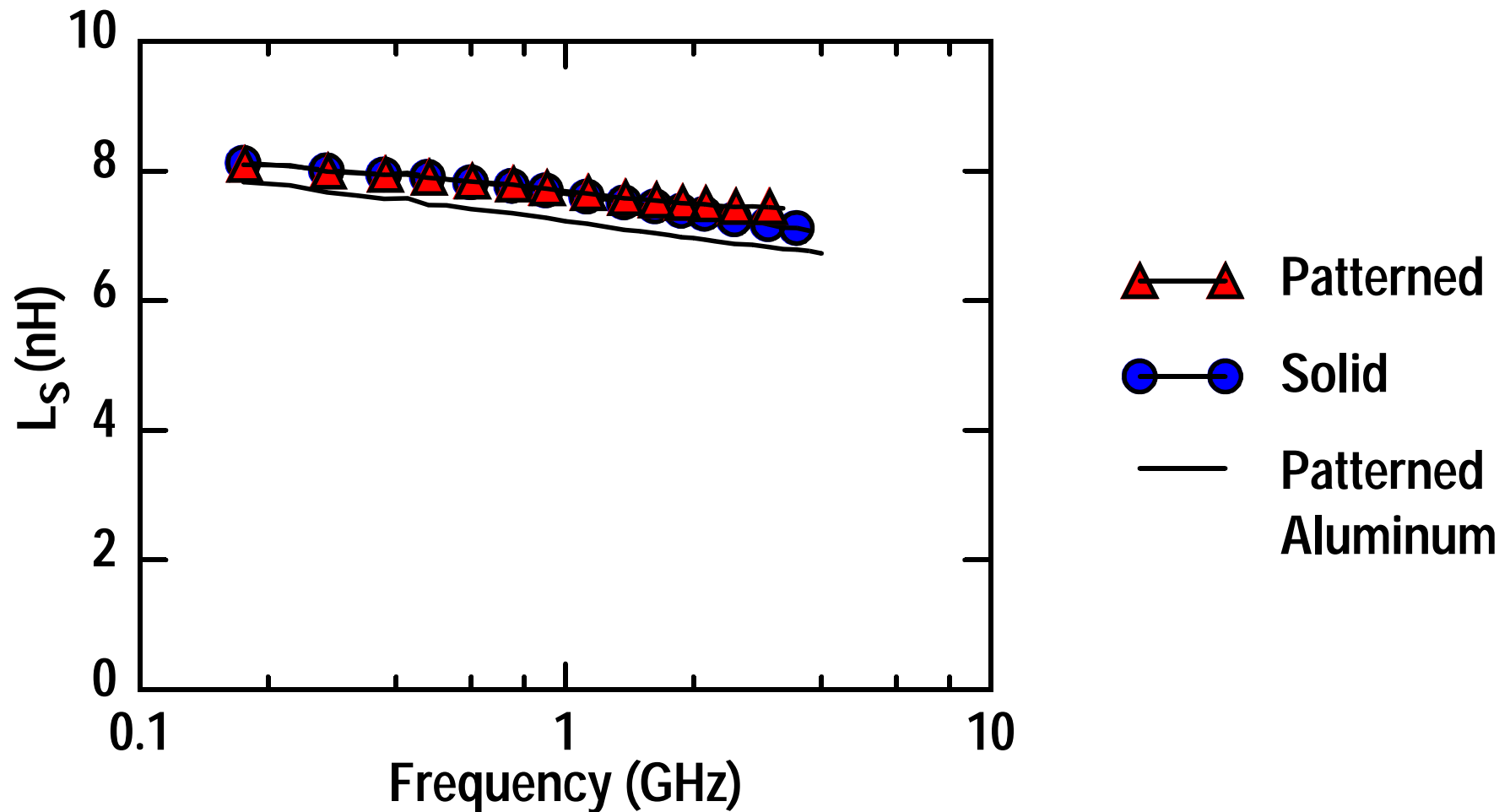
# Effect of Aluminum Ground Shields on R



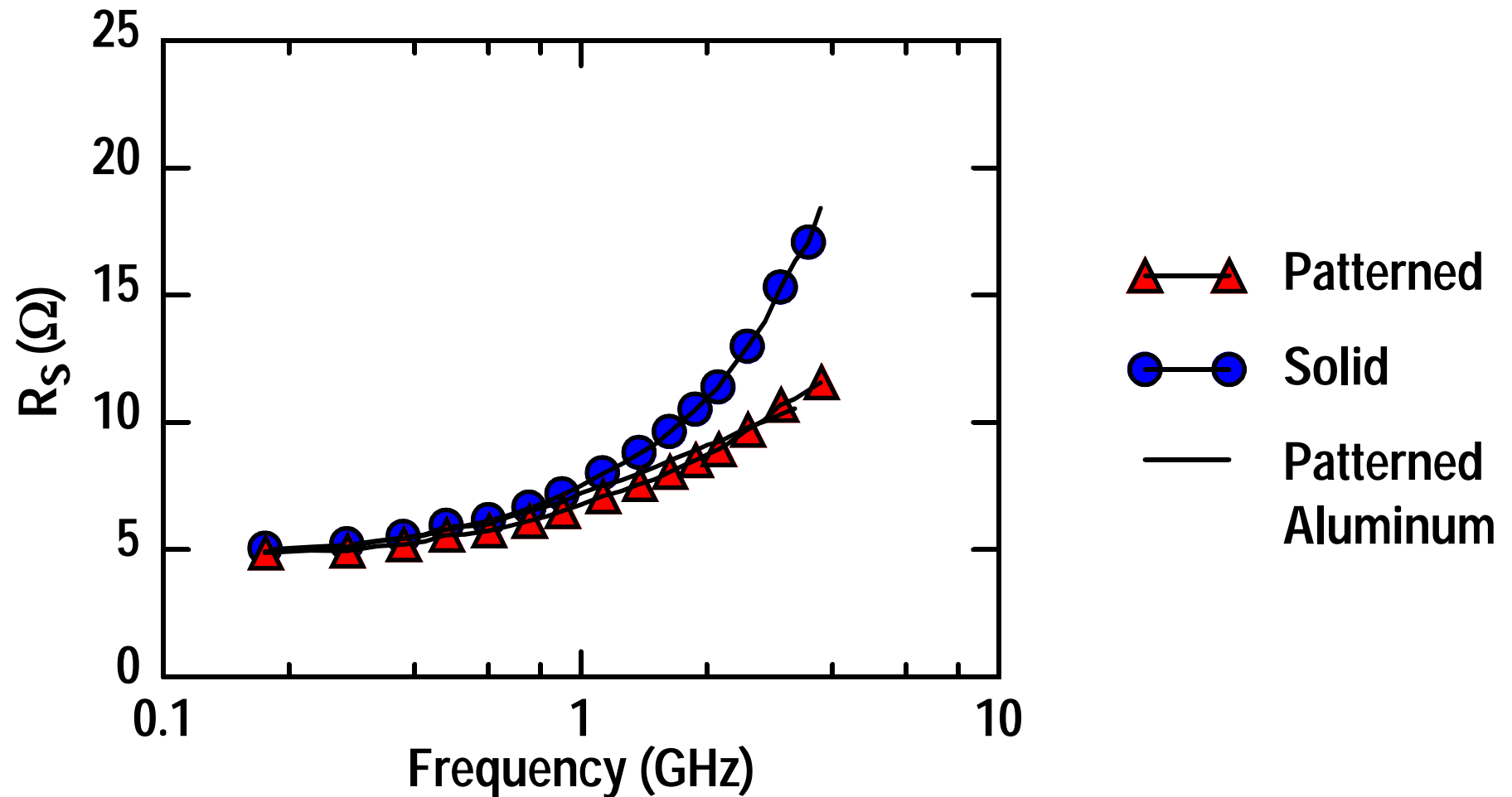
# Effect of Aluminum Ground Shields on C



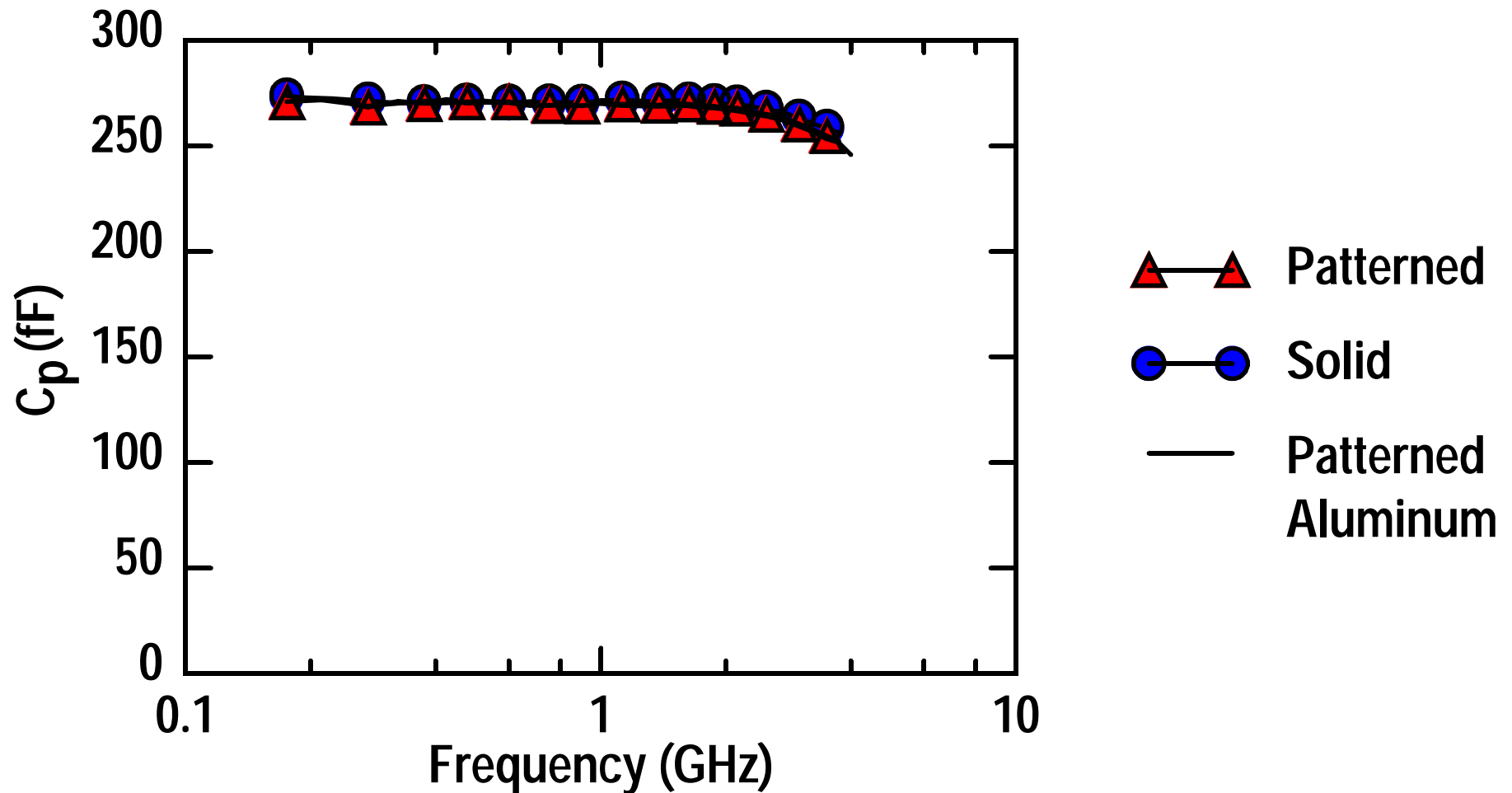
# Effect of Polysilicon Ground Shields on L



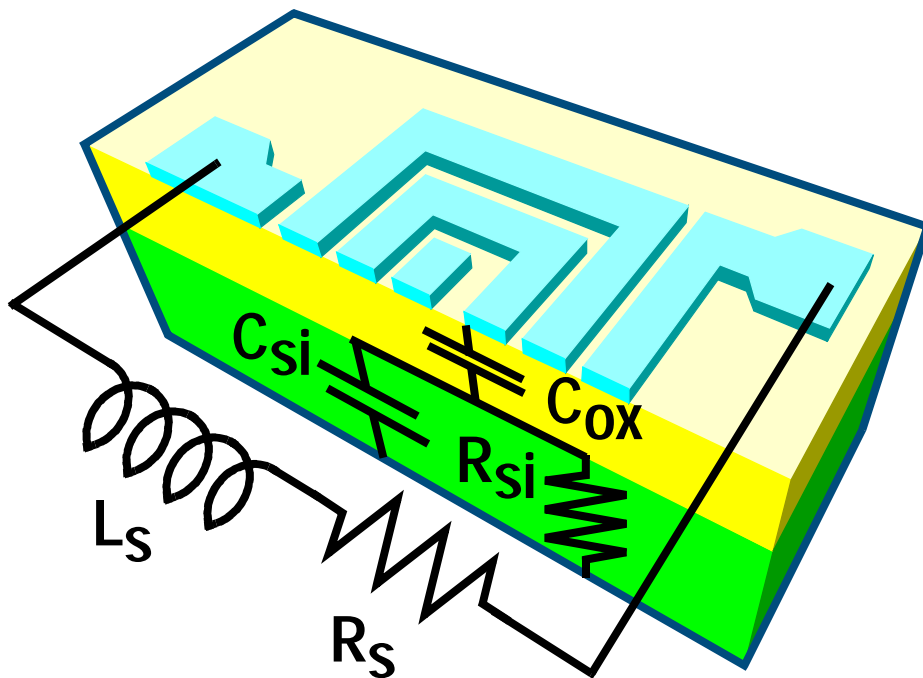
# Effect of Polysilicon Ground Shields on R



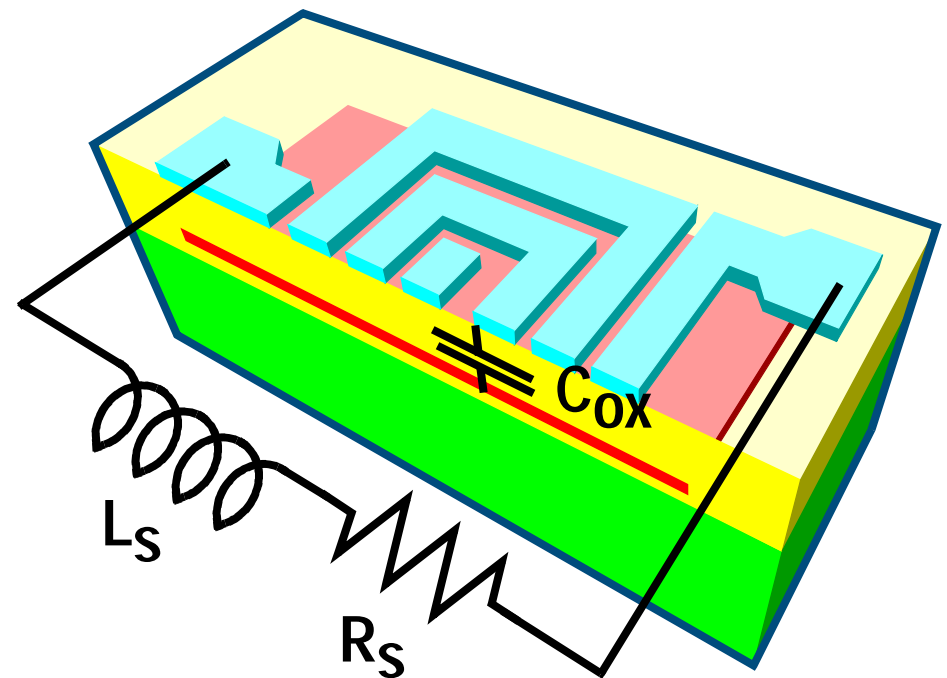
# Effect of Polysilicon Ground Shields on C



# Circuit Models of On-Chip Inductors

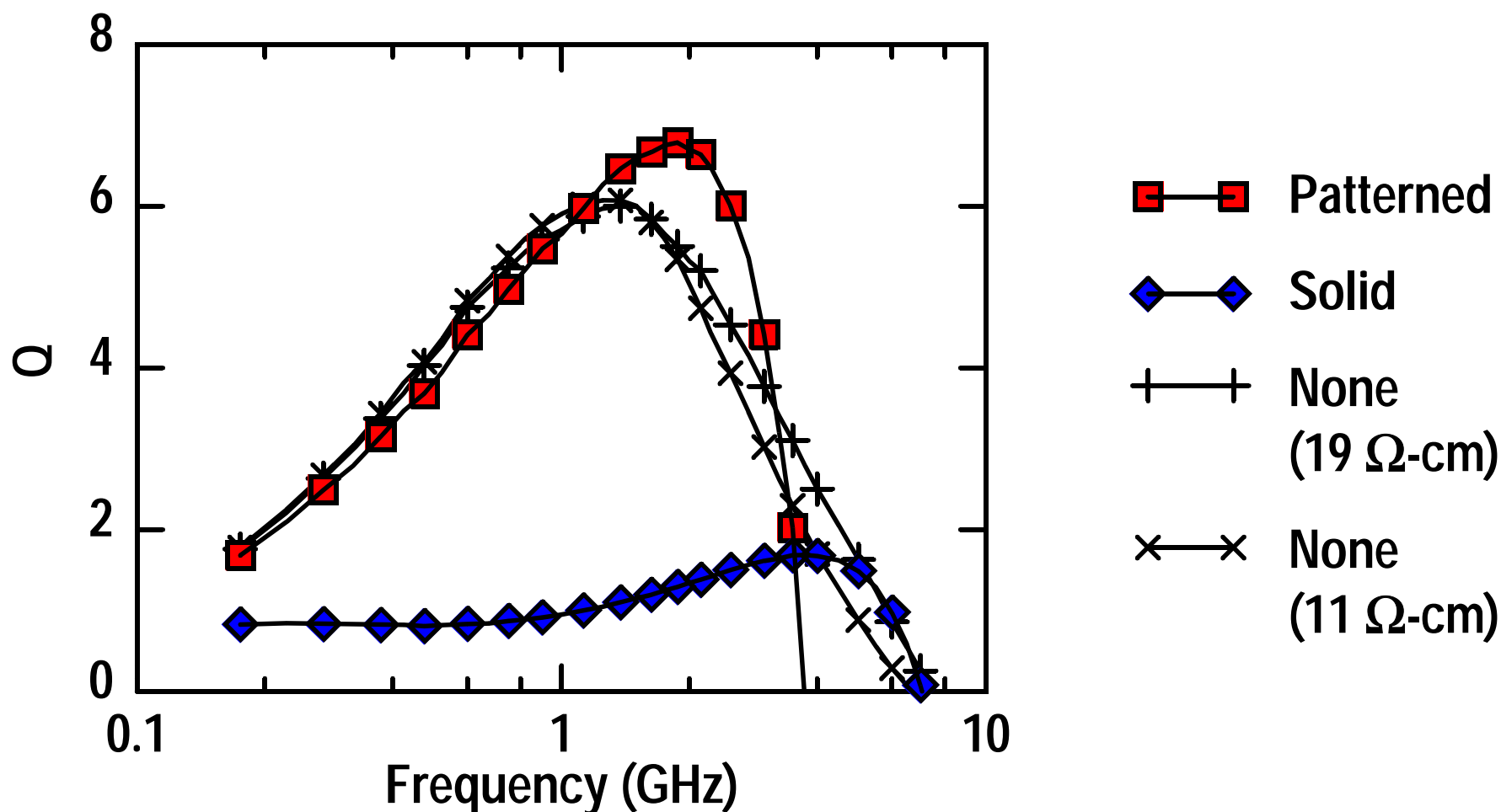


Conventional Design

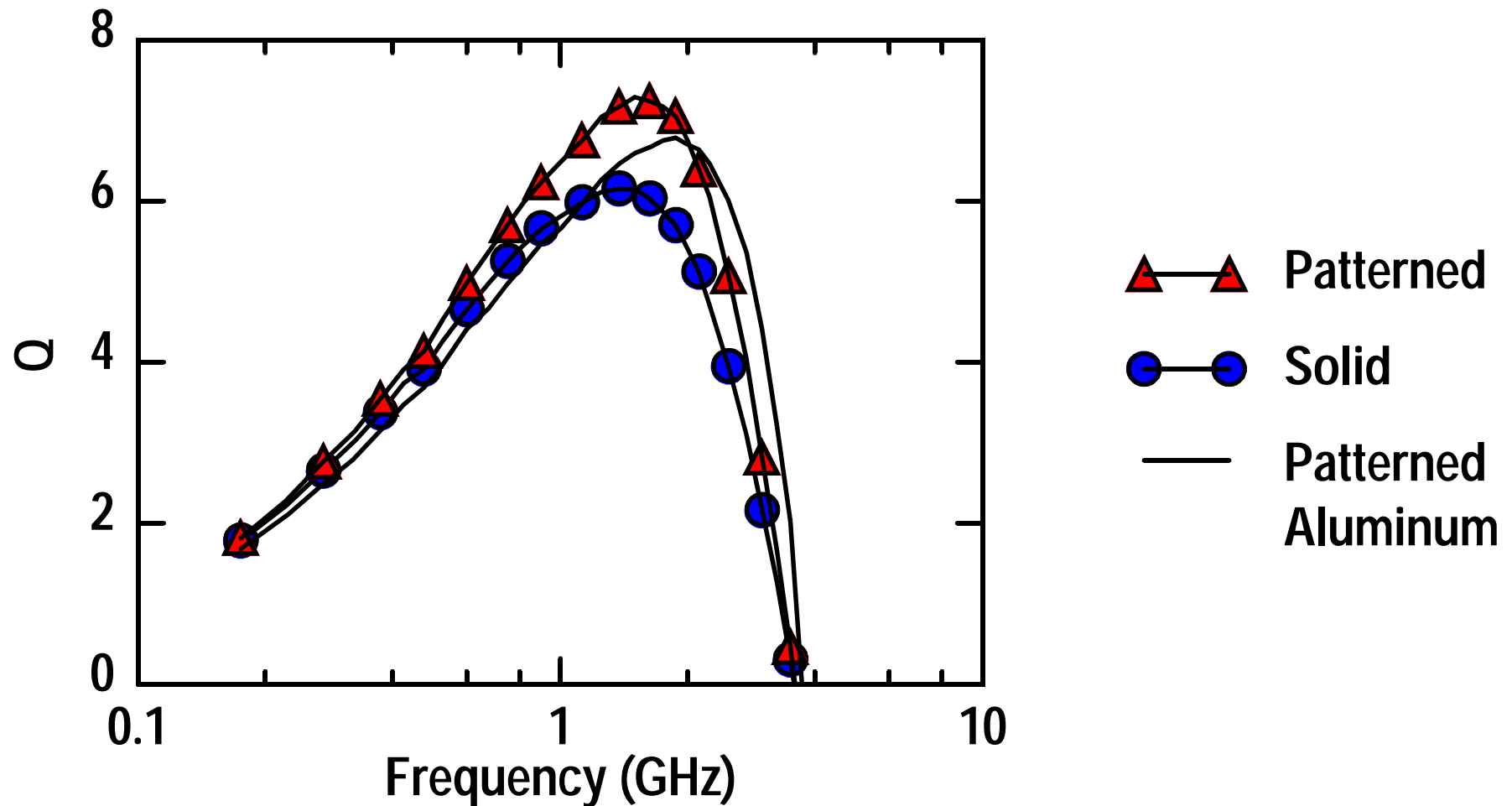


With  
Patterned Ground Shield

# Effect of Aluminum Ground Shields on Q

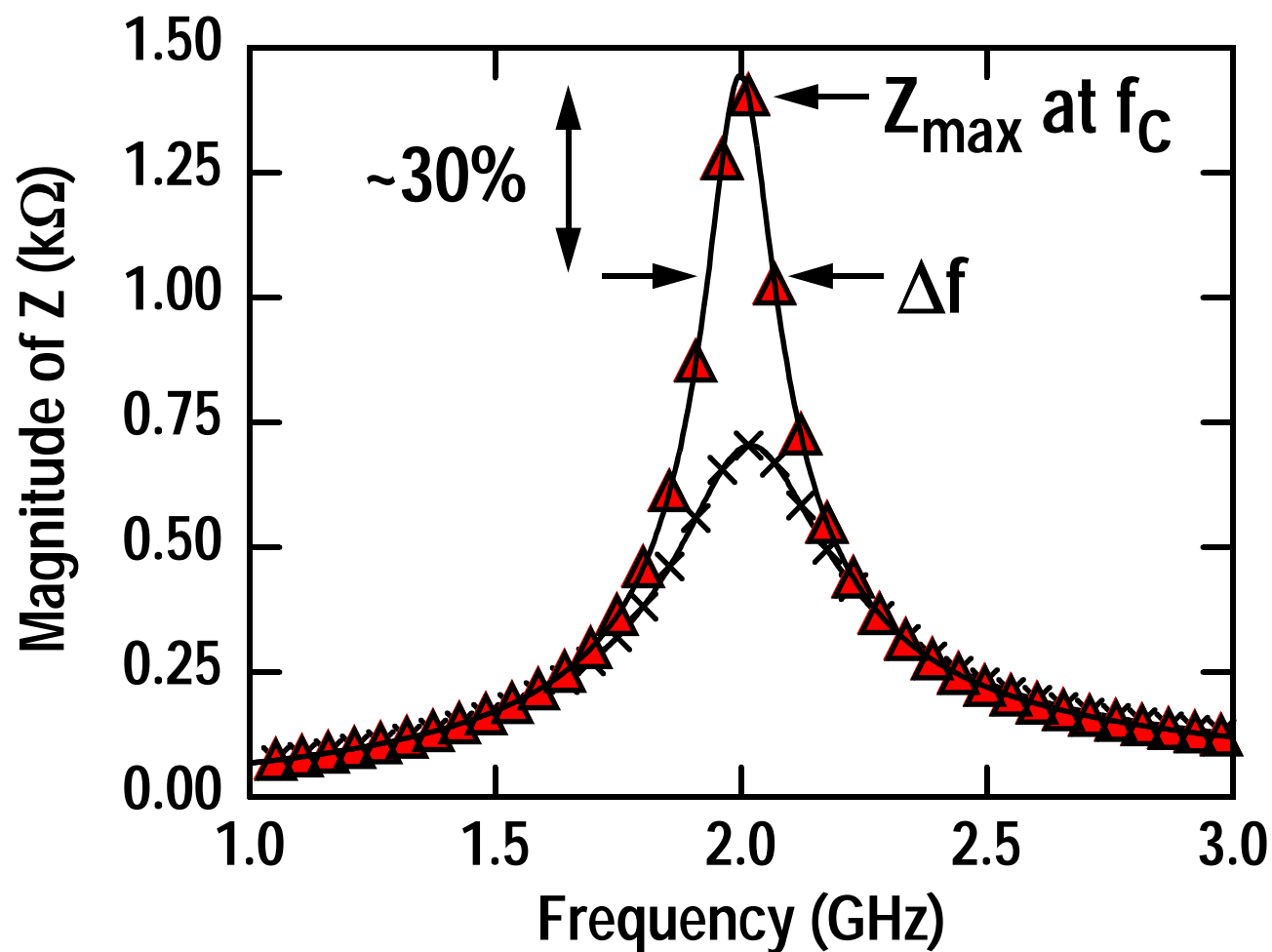


# Effect of Polysilicon Ground Shields on Q

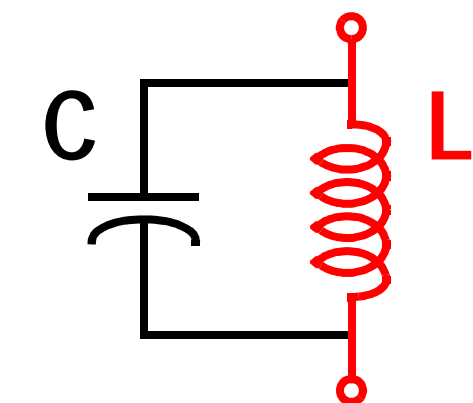




# Parallel LC Resonator at 2 GHz



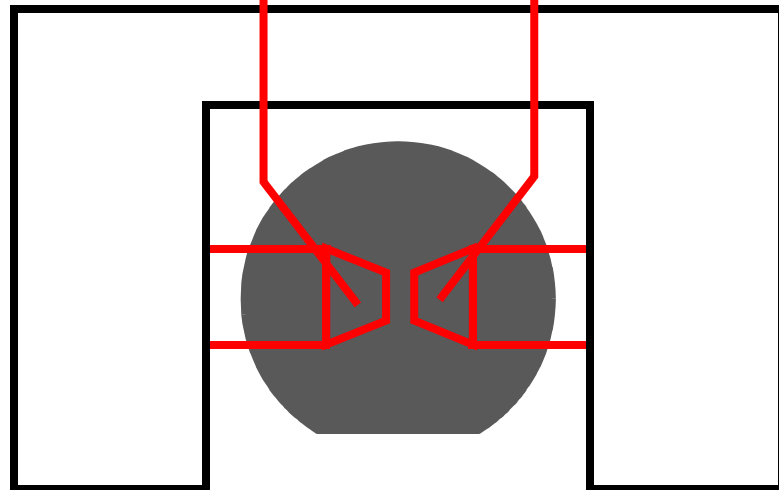
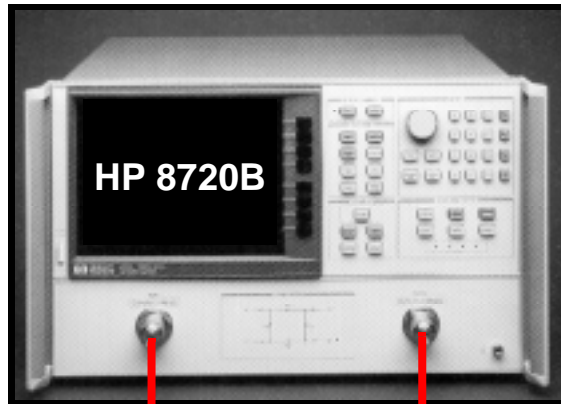
$$Q_{\text{RESONATOR}} = \frac{f_c}{\Delta f}$$



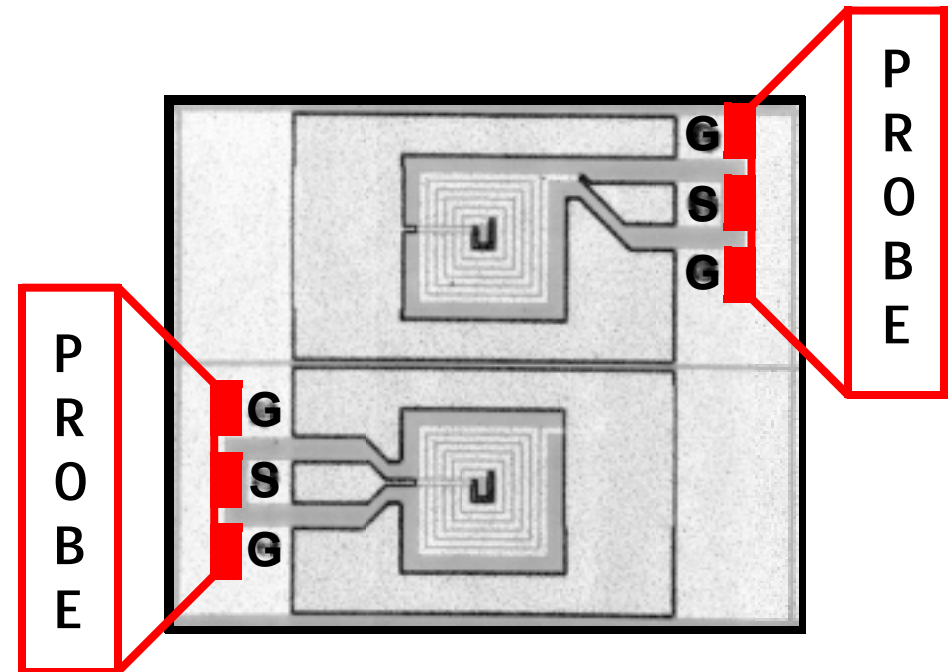
▲ — ▲ Patterned Polysilicon

× — × None (11  $\Omega$ -cm)

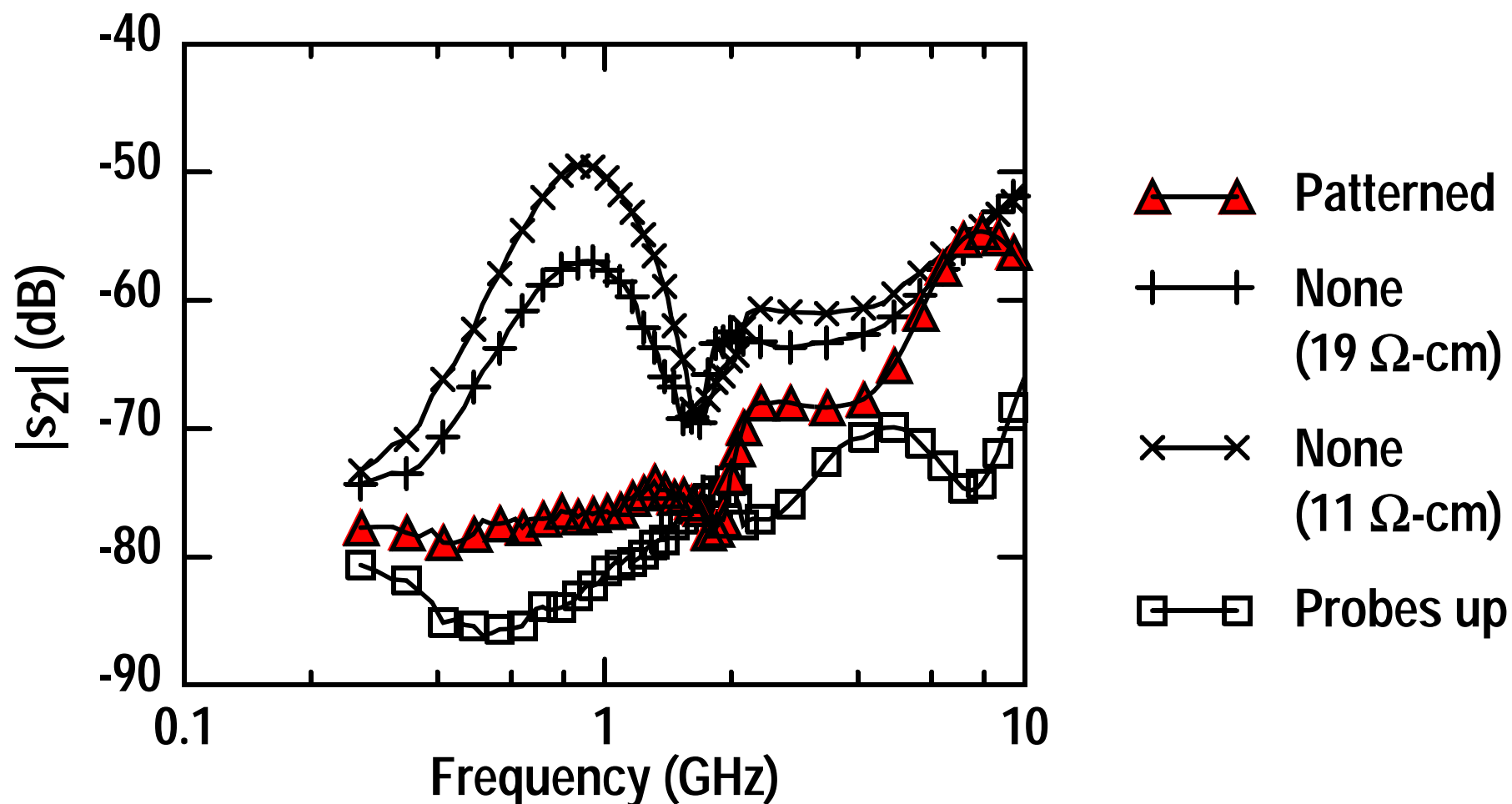
# Noise Coupling Measurement



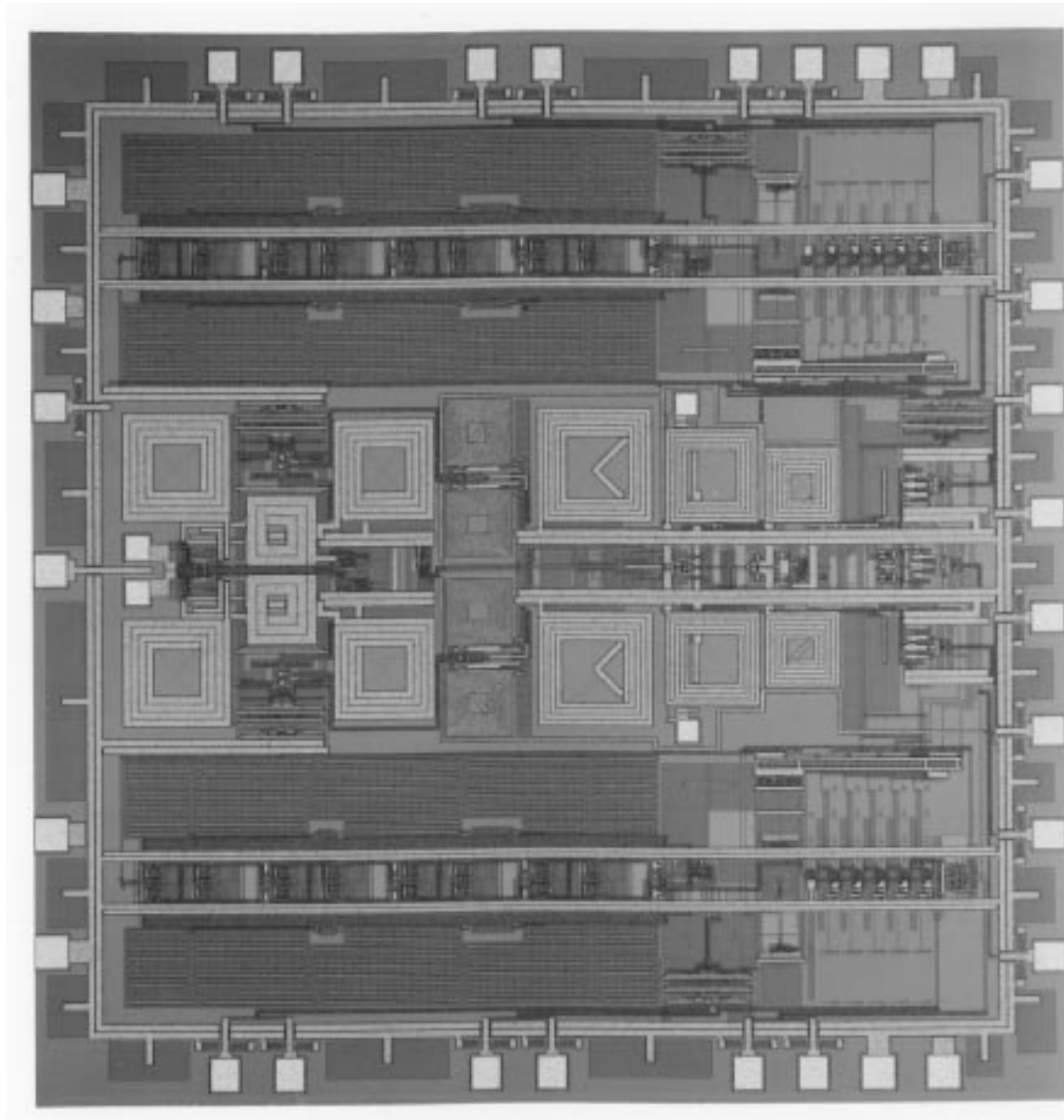
Probe Station



# Effect of Polysilicon GS on Isolation



# A Single-Chip CMOS GPS Receiver



# Conclusions

- A compact model for spiral inductors on silicon has been presented.
- Physical phenomena important to limitation and prediction of  $Q$  were investigated.
- Effects of various structural parameters on  $Q$  have been demonstrated.
- The scalable model can be used as a design tool for optimizing  $Q$ .

# Conclusions on Patterned Ground Shield

- Improves Q by eliminating substrate loss  
(up to 33% at 1-2 GHz)
- Improves isolation by preventing substrate coupling (up to 25 dB at 1 GHz)
- Simplifies modeling
- Eliminates substrate dependency
- Requires no additional process steps

# Acknowledgments

- Center for Integrated Systems Industrial Sponsors
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- National Semiconductor FMA Fellowship (Dr. G. Li)

# Acknowledgments

- Prof. Simon Wong
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- Prof. Tom Lee
- Rosanna Foster and Ann Guerra
- CIS and SNF Staff Members
- Friends
- Family