(Assignment 2/2, 100 Marks, Refer to Greensheet for Due Date, Due During Lecture)

Design of a Single Stage Amplifier

Use schematic composer, Spectre simulator, (optional: Skill coding, Ocean programming) and calculator in the Cadence CAD tool (as well as hand calculation if required) for this assignment. Submit your formal report including graphs, in 2-column IEEE format, in the classroom and put all your hand write-up into an appendix at the end of your report. Informal reports lose 50 marks and late reports lose 10 marks daily.

Specifications:

You are required to optimize a single-stage common-gate amplifier using i) hand calculations based on your first assignment, ii) Cadence simulation to verify the part (i) and iii) automated Ocean programming (optional) in Cadence to achieve the best optimum results. You must include all test benches, graphs, component values and program codes in your report.

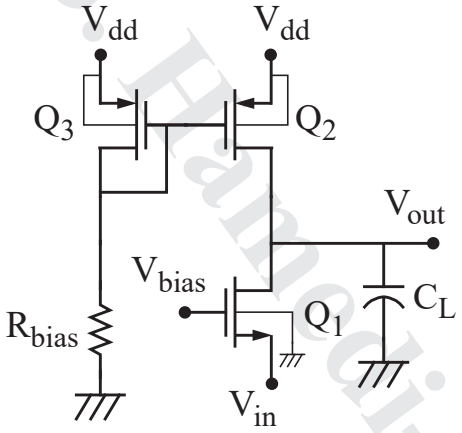

Fig. 1: A Single Stage Common Gate Amplifier

Table 1: Amplifier Characteristics

Technology	sgfet
Supply Voltage	1V
Bandwidth (3dB Frequency)	› 100MHz
Low Frequency Voltage Gain	› 20dB
Voltage Swing	› 0.7V
Load Capacitance	100fF
P_{diss} (rms)	‹ 1mW