San Jose State University
Department of Electrical Engineering
EE178, Fall 2017, Crabill

EE178 Midterm Exam 1

September 28, 2017 P1___
Open book, open notes P2___
Calculators allowed P3___
You have until next class meeting.
Do not open the exam until instructed to do so. S ___

Name: _____

Signature: _____

By signing the above, you agree that you are observing San Jose State University Honor Code.

Write your answers in the spaces provided, on this test booklet. At the end of the exam, hand in this signed test booklet.

- Do not hand in scratch paper.
- Answer on the same page as the question.
- Show your calculations.

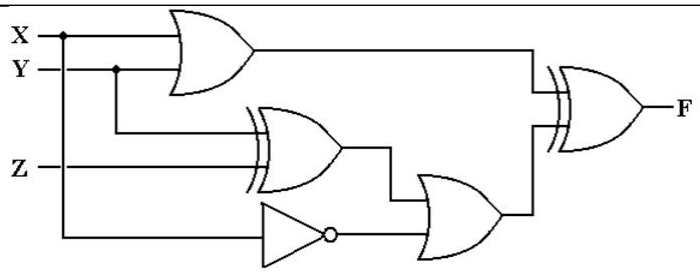
Mental Synthesis (40 points)

Convert between Verilog and a Synthesized Result. When drawing circuits, use common functional building blocks like gates, muxes, decoders, adders, D flip-flops (no other flip-flop types allowed).

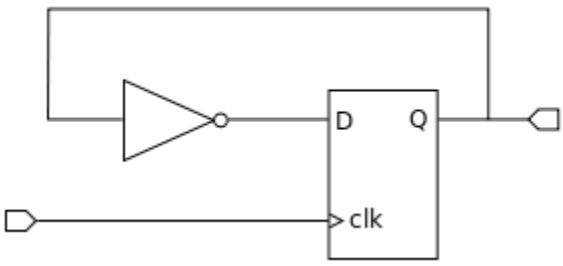
Verilog	Synthesized Result

`wire [15:0] a, b;`
`wire [15:0] alu;`
`wire [1:0] s;`
 	
`assign alu = s[1]?`
`(s[0]?(a | b):(a & b)):`
`(s[0]?(a - b):(a + b));`	

`reg [2:0] rot;`
 	
`always @(posedge clk)`
`begin`
`rot <= {rot[0], rot[2:1]};`
`end`	

`reg q;`
 	
`always @(posedge clk)`
`begin`
`case ({s,r})`
`2'b01: q <= 1'b0;`
`2'b10: q <= 1'b1;`
`default: q <= q;`
`endcase`
`end`	

All About The Benjamins (30 points)

You are managing development of the iToilet and need to select an implementation technology for the swipe gesture detection controller. Your marketing department has forecast you will need 5,000 units over the lifetime of the product.

You have done some shopping around, and found two different solutions that may be reasonable for your project. Each is described below:

Structured Application Specific Integrated Circuit (Structured ASIC)

- Must pay one-time setup fee of $2,000,000 to the fab
- Each controller requires a Structured ASIC chip
- Cost is $1.00 per Structured ASIC chip

Field Programmable Gate Array (FPGA)

- No one-time setup fee as FPGA is a standard product
- Each controller requires an FPGA chip
- Cost is $120.00 per FPGA chip

Which implementation technology would you select based on total project cost, and why? Please show your work.

At what unit volume would it make sense to select the other implementation technology (in other words, where is the crossover point?) Please show your work.

Counter-Based Design (30 points)

Consider the design of a counter-based circuit used to enable a periodic event. You encountered such a circuit in Lab Assignment #2. Even if you did not elect to use this circuit, it was discussed in class.

Assume you have a 4.238010 MHz master clock as an input to your counter, and you need to generate evenly-spaced single-cycle pulses to enable a digital audio circuit at a target rate of 22,050 Hz. How many master clock cycles occur for every output pulse? Show your calculation.

Since the result is fractional, round it to the nearest whole number. Assuming you use a Modulo-N counter to generate the single-cycle pulses, what is the minimum counter size (number of bits) required to count this number of clock cycles?

Using the rounded result, what is the actual (achieved) rate of output pulses per second? Show your calculations.