Design and implementation of 16X8 SRAM in 0.25u SCMOS technology

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***Abstract*- The objective of the project is to design a (16X8)128-bit Static Random Access Memory (SRAM) with fast read and write access, low power consumption, high SNM. The main functional blocks are 6TSRAM cell, row and column decoders, preconditioning circuit, read/write block and sense amplifier. The key design features include precharging the bitline to a lower voltage than VDD and use of equalization transistors, use of clock tree buffers to reduce the fan out on clock signals to less than four, use of dynamic NAND in decoders, reducing sense amp on time during the read cycle to reduce power consumption. The clock tree buffers help to provide a more real estimate of access times. They do not present any area overhead as they are accommodated in the available area. A 20% reduction in read access and 30% in write access times can be observed when an ideal clock signal is provided to the wordline driver. The power consumed by the bitline conditioning circuit is reduced by 15% and the access times are reduced by 16% using the above approach. The sense amp is turned off after a valid read and does not operate for the full read cycle.**

I. INTRODUCTION

A lower power static-type memory device for use as main storage has been realized in CMOS technology. CMOS circuits have inherent advantages of low power and large noise margin. Therefore, there has been a great demand for memories possessing not only lower power and high density, but also high speed comparable to the NMOS and bipolar ECL memories. Designing the 128-bit SRAM provided us with an opportunity to learn and explore various aspects of high speed full-custom VLSI design. This design is unique on the grounds of strategy to minimize power consumption by reducing precharge voltage of bitlines, switching off the sense-amp after a read operation, use of dynamic NAND gates in row and column decoders and use of clock tree buffers to limit the fan out on clock signal to four.

II. DESIGN DESCRIPTION

The main building blocks used in implementing this project are 6T SRAM cell, row and column decoders, bit-line conditioning circuitry, read-write control circuitry, sense amplifier and clock tree buffers.

A. 6T SRAM cell

The SRAM cell incorporates basic 6T design. The sizes used in designing 6T are 1.5:1 (W/L) for PMOS, 2.25:1 for NMOS in cross coupled inverter and 1.5:1 for access transistors. Here L=0.24um. The sizing was done keeping in mind the read and write stability and the static noise margins (SNM). Figures 1-3 show the SNM plots for read, write and hold operations. Fig 4 shows the internal node of the memory cell during the read operation. For read stability this voltage should remain below the threshold of the NMOS transistors. The margin is essential to ensure the design works on silicon.

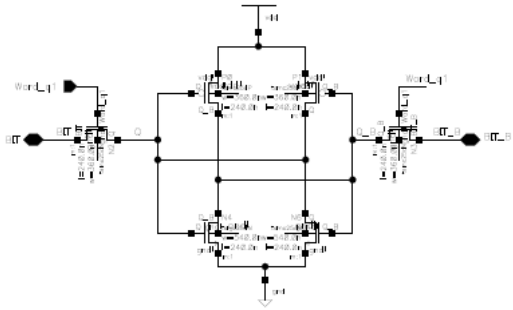

Fig 1. The 6T SRAM cell

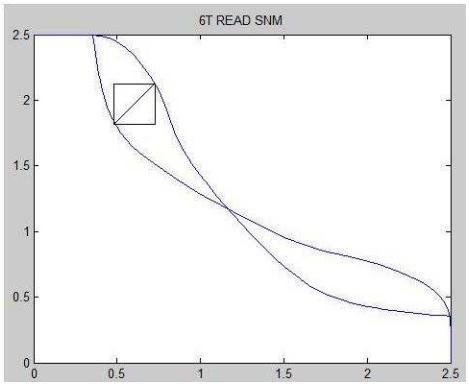

Fig1. Read static noise margin

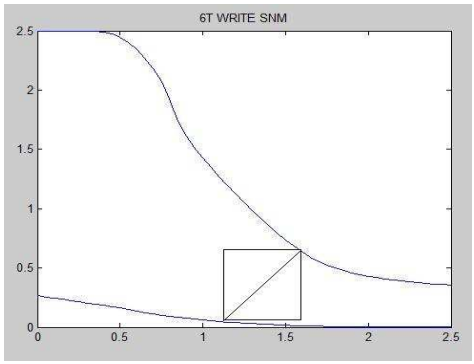

Fig2. Write Static noise margin

B. Bit line conditioning

The bit-line conditioning circuitry uses NMOS transistors to pre-charge the bit lines. An additional NMOS is used to equalize the bitlines (Fig5). In a read or a write cycle one of the bit lines is discharged while the other remains at the

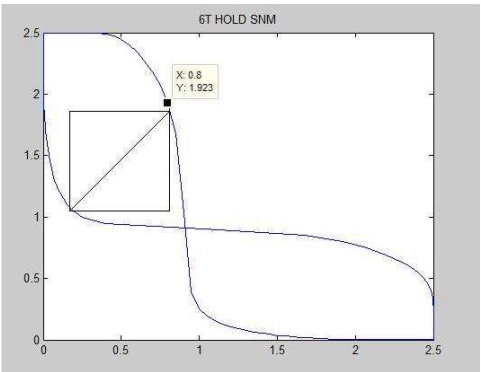

Fig 3. Hold static noise margin

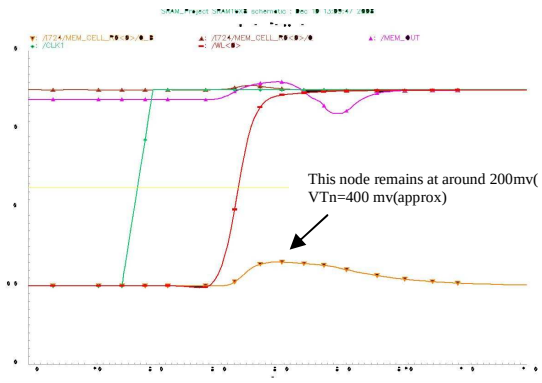

Fig4. Voltage bump of internal state (Q) in the 6T SRAM cell

precharged voltage. The precharged line helps the other bitline to charge along with the pull up transistors. This reduces the precharging time of the circuit. The fact that the bitlines have to be charged to a lesser voltage than VDD also reduces the power consumed by the block.

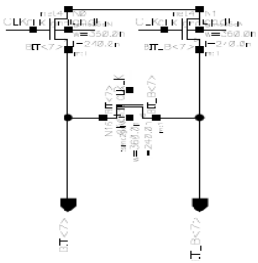
Fig 5. NMOS transistors used for precharge and equalization

C. *Decoders*

The address decoding stage has been divided into two stages: pre-decoder and decoder. This two stage approach greatly reduces the number of gates used in the design. The decoder is implemented using dynamic NAND gates which have less power consumption and faster response. A 4:16 row decoder and 3:8 column decoders are used in the design. The decoder is synchronized with the negative edge of the phase 2 (precharge clock). Thus the access times of the memory are not affected by the decoder delay since the decoding is completed before the phase 1 clock goes high. The load on the clock is reduced by limiting the fan out to four inside the decoder.

D. *Read/write circuitry*

The read/write block consists of the column multiplexer, write driver and data driver. The column multiplexer is implemented using access NMOS transistors. The write and data drivers are also implemented using access NMOS transistors. During the read cycle, write is strobe is low and the write circuit is cut off from the mux output. The mux outputs are now connected to the sense amplifier. Thus a single block performs both the functions for read and write.

E. *Sense amplifier*

The sense amplifier uses two cross coupled inverters and isolation transistors connecting the inverter inputs to the bit lines. The isolation transistors prevent the bit lines from loading the sense amp during the read operation. Also, to reduce power consumption the sense amp enable signal is turned off after the read has been done. Fig6 shows the scheme for turning off the sense-amp enable. The high-time of this signal is determined by simulations.

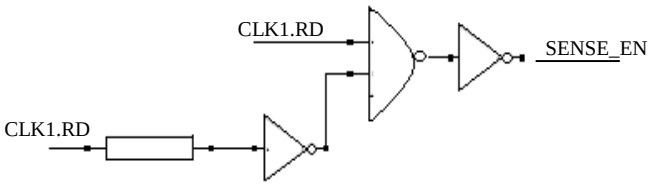

Fig6. Sense-amp enable signal is turned off after the read operation

F. *Clock tree*

For this project the access times are defined as the delay 50% transition time from the phase one clock's rising edge to the 50% transition time when the data is written (for the write access) or the 50% transition time when the read is valid at the output port. The optimal delay will be obtained when the fan out of each stage in the delay path is approximately four [1], [2]. The clock tree is used to ensure that the fan out of each stage in the clock path is slightly less than four. Thus the input clock is now buffered which reduces the load on the input clock signals. Such an approach gives real access times as compared to the access times observed when ideal input clock signals are considered for simulations. Fig7 shows the schematic for this scheme.

III. IMPLEMENTATION

The design is implemented in 250 nm SCMOS technology. The layout is done for the design with the clock tree buffers. Up to metal 4 has been used for routing the signals. The SRAM is sized on the basis of the above discussion on SNM. The word lines are driven by the row decoder which is pitch matched with the core. This minimizes the routing need for

wordline drivers and improves memory performance. The write access time is measured as the 50% time from the

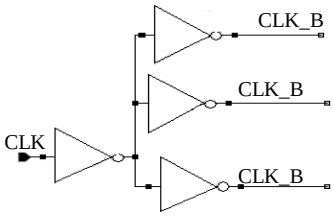

Fig7. Clock tree buffers avoid clock loading and provide close to real values for access times

positive edge of clock1 to the 50% time when the internal node is driven high or low (1 or 0). Similarly, the read access time is measured from the time when the clock to the time when the output is valid at the output port. Fig8 shows the die picture of the complete SRAM design.

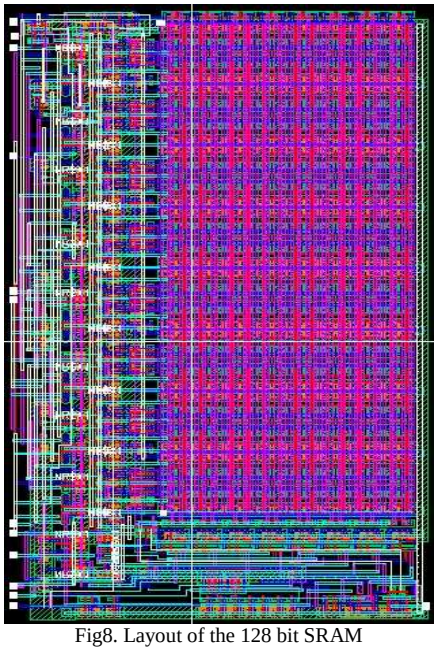

Fig8. Layout of the 128 bit SRAM

IV. RESULTS

The measured parameters for the design are summarized in the following tables.

TABLE I
6T SRAM cell parameters (per SRAM cell)

READ	0.39V
WRITE	0.74V
HOLD	1.06V
Cell area	29.33 um^2
Diffusion capacitance(access transistors)	1.0512fF
Gate capacitance(access transistors)	1.4832fF
Word line capacitance	0.076fF

TABLE II
Measured parameters with clock tree buffers
Pre-layout SPICE simulations (VDD=2.5, T=27C)

Overall SRAM AREA	5528 um^2
MEM CORE AREA	2769.85 um^2
Read Access	596ps(read 0), 440ps(read 1)
Write Access	480ps(write 1), 415ps(write 0)
Power dissipation	0.8 mW
Energy-delay product	2.025E-20 J-s

TABLE III
Measured parameters without clock tree buffers
Pre-layout SPICE simulations (VDD=2.5, T=27C)

Read access	481ps(read 0), 350ps(read 1)
Write access	324ps(write 1), 312ps(write 0)

The read –write SPICE simulation waveforms are presented in figures 9-12.

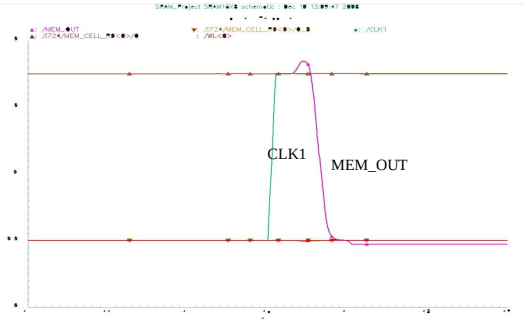

Fig 9. Read zero cycle

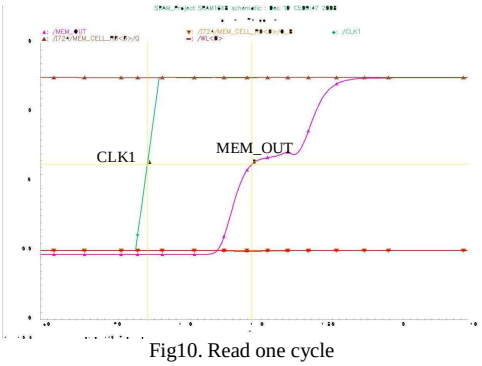

Fig10. Read one cycle

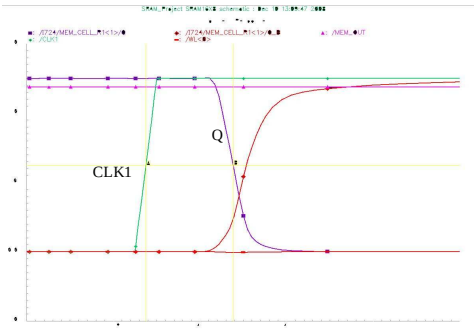

Fig11. Write zero cycle

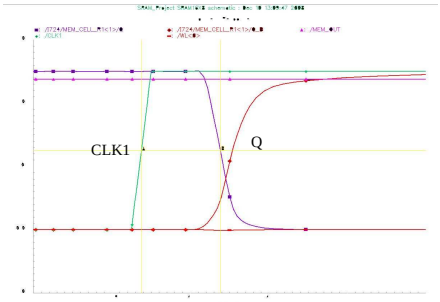

Fig12. Write one cycle

The post layout simulations were also performed to estimate the performance on silicon.

Measured parameters with clock tree buffers
Post-layout SPICE simulations (VDD=2.5, T=27C)

Read Access	1.23 ns(read 0)
Write Access	1.25ns(write 1), 937ps(write 0)
Power dissipation	0.9mW

The post simulations show an increase in the access times which is due to the parasitic capacitances and resistances present in the RC extracted view. The plots for the SPICE simulations (post layout) are shown in figures 13-15.

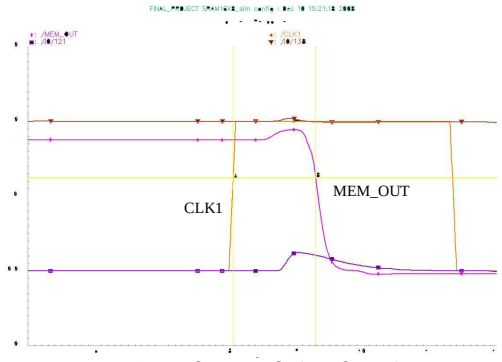

Fig 13. Read zero cycle (post layout)

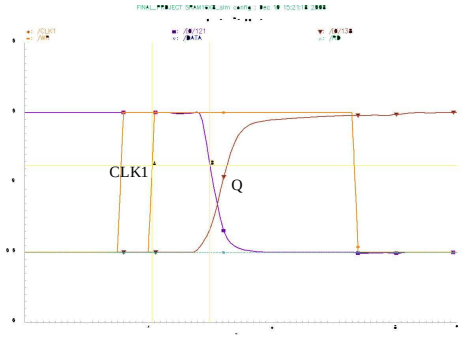

Fig 14. Write one (post layout)

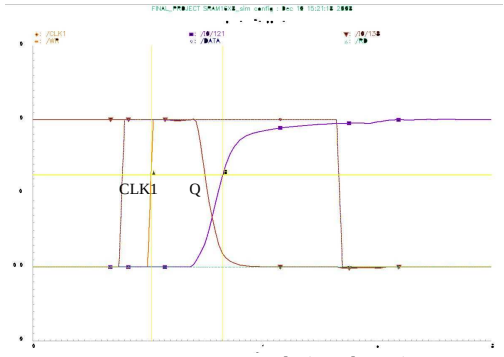

Fig 15. Write zero cycle (post layout)

V. CONCLUSION

A 128 bit (16X8) SRAM was designed and implemented in 0.25 micron technology using MOSIS SCMOS deep sub micron rules. The layout was done for the design containing the clock tree buffers. The pre layout and post layout simulations were performed in SPICE using the Cadence spectre simulator. Up to metal 4 has been used in the layout design. The clock tree buffers give a closer estimate of the delays to the values that would be observed in an integrated system. The delay times increase significantly in the post layout simulations due to the parasitic resistances and capacitances. The results show that the SRAM core occupies a major portion of the total design area. The techniques used for reducing power in bit line conditioning circuit provide significant reduction in power.

ACKNOWLEDGMENT

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REFERENCES

[1] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikkolic, *Digital Integrated Circuits, Second Edition*
[2] Neil H. Weste, David Harris, Ayan Bannerjee, David Harris, *CMOS VLSI Design*