

Introducing Suspendance Analysis

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Abstract—Suspendance analysis is based on determinant expansion and is an effective tool for calculating node admittances. The node admittance is equal to the ratio of the suspendance obtained when the node is open to the suspendance obtained when the node is shorted. Suspendance is expressed in terms of circuit admittances and transadmittances and is calculated by shorting passive circuit components based on minimum expansion algorithm to yield compact and accurate results. Only certain passive components are shorted one at a time and multiplied by the remaining circuit suspendance. Admittances of previously shorted components are set to zero in succeeding calculations. The overall suspendance is calculated by summing contributions of shorted passive components and cross coupled voltage controlled current sources.

Index Terms—Admittance, amplifier, BJT, bridged, determinant, expansion, feedback, inductor, MOSFET, suspendance, symbolic, transadmittance.

I. INTRODUCTION

SYMBOLIC analysis is essential for understanding and design automation of Analog circuits. When circuit transfer functions are expressed parametrically the impact of each component on circuit behavior is better studied. By calculating a few primary transfer functions at each node of a circuit, other transfer functions can be easily extracted. Node admittance is one of these primary transfer functions that can be extracted fast and accurately using a few methods. However, the complexity associated with these techniques has limited their influence on circuit analysis and solving systems of equations derived from fundamental circuit laws [1] is still the main adopted approach to obtain circuit transfer functions. Symbolic analyses are generally performed by topological methods that use signal flow graphs or algebraic methods that use matrices [2]–[3]. These techniques are briefly addressed here.

In tree enumeration methods, the determinant of the admittance transfer function is calculated by directed or undirected methods. In directed approach, the determinant is given by the sum of all tree admittance products in a graph that is constructed from an augmented circuit. Results include some equal terms with opposite signs that need term cancellation and hence are not efficient [4]. In undirected approach, the determinant is given by the product of the common spanning trees between a voltage graph formed by voltage sources and

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a current graph formed by current sources [5]. This method suffers from the complexity of the search algorithm and sign calculation for each product term [6].

In signal flowgraph methods, more comprehensive graphs are formed and analyzed based on a circuit. In some approaches, transfer function is generated by calculating path and loop weights and by enumerating the n-order loops [7]–[8]. These enumerations add to computational complexity and additional conditions must be incorporated to include all types of sources. Independent and controlled voltage sources must never form a loop and independent and controlled current sources must never form cutsets which are sets of edges whose removal would disconnect a graph [9]. In other signal flowgraph approaches, both currents and voltages are treated as variables in generation of graphs [10]. Compared with the circuit, the size of these graphs increases more than twofold because extra rows and columns are appended to accommodate mixed variables.

In hierarchical decomposition methods, network graphs are partitioned and symbolic expressions are generated in a nested form by utilizing several methods such as topological analysis [11], network formulation [12], and determinant decision diagram based analysis [13]. A meaningful decomposition requires an advanced knowledge of the generated graph [14]. This method becomes inefficient in the presence of different composing sub-blocks which are tightly coupled together. It also suffers from accuracy and algorithm complexity.

In topological approximation methods, long symbolic expressions are shortened in a trade-off between simplicity and accuracy. Elements with insignificant contribution to the network are either removed or shorted during or after generation of the symbolic terms [15]–[16]. Simplification after generation requires complete circuit analysis and therefore, resources used to create pruned terms are not fully utilized. Term reduction is achieved by finding the smallest weight spanning trees or term cancellation algorithms that can be applied to the tree enumeration, signal flow graph or matrix determinant methods [17] or by polynomial reduction [18] or interpolation [19] methods. All these suffer from exponential algorithm complexity.

In partial analysis methods, some circuit components and the complex radial frequency are kept as symbols while other components are assigned numerical values. Partial numeric and symbolic analysis are performed in order to extract a transfer function while reducing the length of the symbolic expressions. The interpolation method, applies numerical algorithms to circuit branches that do not have symbolic variables and utilizes tree enumeration or signal flowgraph to solve circuit matrices [20]. The parameter extraction method, uses

combined topological and constitutive equations in solving circuit matrices [21]–[22]. The numeric matrix is solved based on determinant properties of the modified nodal analysis [23] or one of its derivations [24]–[25].

In pathological element methods, circuit structures are mapped to predefined topologies or reference models such as nullators and norators to predict the behavior of active networks. A nullator has zero voltage drop and zero current flow and a norator has an arbitrary voltage drop and current flow [26]–[27]. Existence of known circuit connectivity is required for successful topological guess and extraction of transfer functions in these analyses methods [28]–[31].

In extra element methods, calculation of transfer functions is simplified by breaking up the analysis into three parts. An extra element connected across a node is first removed and a simpler transfer function is calculated. The driving point impedance looking into that node is then calculated. Finally, the null impedance looking into that node is calculated and the original transfer function from these three results is reconstructed [32]–[33]. Lengthy calculations are required to obtain three independent sub transfer functions.

In determinant expansion methods, the principal determinant of the circuit is calculated by summing the products of circuit elements with their corresponding sub-determinants [34]–[35]. For active circuits that include dependent sources, extra rules are required for calculating accurate determinants using expansion algorithm. Utilizing graphs and their associated rules unnecessarily complicates the circuit analysis [36]–[37]. In other approaches, active elements are replaced by nullators and norators and circuits that include a mixture of dependent sources are analyzed through applying six rules [38]. Residual networks are formed to show how a circuit determinant can be expanded by both passive and active circuit components [39]. When there are more than one controlled sources, the residual networks remaining after the expansion of the first source will still contain the other controlled sources. Thus, the expansion takes one controlled source at a time in the same manner as expanding the principal determinant in terms of passive elements. A combination of determinant expansion and extra element methods is also studied in [40]. Replacing dependent sources with nullators and norators adds an additional calculation step and more virtual nodes to circuit and increase the size of residual network matrix. Furthermore, determinant expansion by all types of dependent sources adds additional rules and increase the complexity of calculations.

The suspandance analysis introduced in this paper is based on determinant expansion method. All passive components are expressed with admittances and all dependent sources are converted to voltage controlled current sources. The circuit determinant is expanded by passive components only and the contribution of cross coupled current sources is added later. To generate the circuit determinant with the least number of calculations, minimum expansion algorithm has to be followed. The dual of the suspandance analysis that uses impedance components and current controlled voltage sources can be equally utilized in circuit analysis. However, because transistors are major components in most electronic circuits

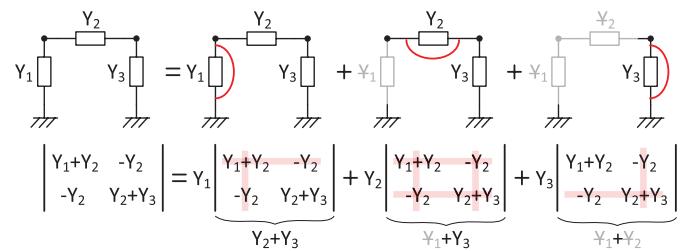


Fig. 1. Concept of determinant expansion for a passive circuit.

and use voltage controlled current sources to model their behavior, the suspandance analysis based on admittances is only considered and explained in this paper.

Section II of this paper explains the concept of determinant expansion and explains its inherent advantages compared to solving determinants extracted from systems of equations. Section III explains the suspandance analysis and shows how to calculate suspandance of a network from primitive open ($S_u = 0$), solo ($S_u = Y$) and short ($S_u = 1$) structures. It also explains the minimum expansion algorithm used in calculating suspandance terms. Section IV extracts node admittances of a few popular circuits using suspandance analysis and compares the results by Spice simulation. This section is then followed by the conclusion.

II. DETERMINANT EXPANSION

The concept of determinant expansion was explained mathematically by [41] and was introduced to passive circuits by [34]–[35]. As shown in Fig. 1, the admittance determinant can be obtained by summation of products of passive circuit elements and their corresponding sub-determinants. For elements that only appear diagonally (Y_1 and Y_3), the sub-determinant is obtained by eliminating the rows and columns that include these element. For other non-diagonal elements (Y_2), the sub-determinant is obtained by first merging and then collapsing the rows and columns that have these element.

Shunt circuit elements appear diagonally in the admittance matrix and sequential circuit elements as well as dependent sources appear elsewhere. In determinant expansion algorithm shown in Fig. 1, the corresponding sub-determinant for each passive circuit component can be directly obtained from the circuit when that element is shorted. Components that were shorted in prior determinant expansion calculation are set to zero (opened or removed from circuit) in all succeeding calculations.

The **first** major advantage of applying determinant expansion to a circuit is the **independence** from systems of equations and signal flowgraphs because the admittance determinant can be directly obtained from the circuit without any translation.

The **second** major advantage of using determinant expansion is inherent **cancellation** of redundant terms in any matrix determinant. Direct calculation of admittance determinant for circuit shown in Fig. 1 results in $(Y_1 + Y_2)(Y_2 + Y_3) - Y_2^2$ which has equal terms with opposing signs (redundant) terms that need to be cancelled. A passive circuit with n nodes has a maximum of n shunt admittances that connect nodes

to ground, $n - 1$ sequential admittances that connect consecutive nodes together and $0.5[n^2 - 3n + 2]$ bridge admittances that connect non-consecutive nodes together. The determinant of an n -node passive circuit includes a maximum of $2[n^n - (n + 1)^{n-1}]$ redundant terms (if all components are populated) that need to be cancelled. Each term has a unit of Ω^{-n} (order of n). As number of nodes increase, the order and the number of redundant terms in a determinant increase exponentially and the simplification of determinant becomes very time consuming. When dependent sources are added to a circuit, the number of redundant terms in the admittance matrix increase even more and determinant expansion remains a better choice for circuit analysis.

The **third** major advantage of using determinant expansion is the **compactness** of results. The term cancellation in direct determinant calculation requires expansion of terms before simplification. Determinant of a circuit with n nodes has $(n + 1)^{n-1}$ terms while each term is a product of n admittances and has a unit of Ω^{-n} . On the other hand, the determinant expansion factors circuit components efficiently and represents the results with much less number of summations and multiplications when compared with those obtained from direct determinant calculations.

The **fourth** major advantage of using determinant expansion is **simplicity** of results and calculations as algorithm progresses. Term cancellations at the end of direct determinant calculation needs lots of resources as explained earlier. To simplify cancellation, alternative methods such as elimination of rows and columns can be utilized to reduce the order of determinant. When order is reduced, the complexity of terms remaining in determinant increases enormously. Therefore, regardless of the algebraic approach, the final steps of calculating determinants directly become very lengthy and tedious to execute. In contrary, as passive components are shorted and later removed from circuit during determinant expansion, results become shorter and extremely easier to extract. Furthermore, the order of remaining terms at one point becomes less than the order of initial terms (Ω^{-n}). At this point, calculation can stop and there will be no need to continue with the expansion algorithm because the contribution of remaining structures to determinant will be zero. This was illustrated in the last step of determinant expansion shown in Fig. 1 where one of the circuit nodes is completely eliminated after removing (Y_1 and Y_2) and circuit order is reduced generating zero contribution to circuit determinant.

The **fifth** major advantage of using determinant expansion is **reusability** of results obtained earlier. The admittance $Y_a(j\omega)$ at node (a) of a circuit is expressed as

$$Y_a(j\omega) = \frac{i_a(j\omega)}{v_a(j\omega)} = \frac{O(j\omega)}{D_a(j\omega)} \quad (1)$$

where $i_a(j\omega)$ and $v_a(j\omega)$ represent the current and the voltage at node (a), respectively, while an external source is connected to node (a). Other independent sources in the circuit are discarded for admittance calculation because they create transadmittance terms across node (a) that must be avoided. The $O(j\omega)$ and $D_a(j\omega)$ represent the admittance determinants at node (a) when it is left open or shorted to ground, respectively.

Based on determinant expansion algorithm, shorting a shunt component connected to node (a) is required to extract admittance determinant. Therefore, calculation of $O(j\omega)$ includes calculating $D_a(j\omega)$ and results can be reused. This will be shown practically in Section IV of this paper.

III. SUSPENDANCE ANALYSIS

Suspendance analysis is based on determinant expansion algorithm explained in previous section. What distinguishes suspendance analysis from other determinant expansion algorithms are **i**) exclusion of graphs, **ii**) exclusion of nullators and norators for modelling active circuit components, **iii**) exclusion of active components in determinant expansion, **iv**) inclusion of contributions by cross coupled sources and **v**) using minimum expansion algorithm in determinant calculation.

The complete outline of the suspendance analysis consist of the followings.

- Su.1. Passive circuit elements are expressed in terms of admittances.
- Su.2. Dependent sources are converted to voltage controlled current sources.
- Su.3. The results of determinant expansions are called suspendance terms which have units of Ω^{-n} where n is the order of circuit and represent number of nodes.
- Su.4. Suspendance terms are calculated by shorting passive circuit components one at a time and multiplying them by the remaining circuit suspendance. Admittances of previously shorted components are set to zero in succeeding calculations.
- Su.5. When elements connected to a node are removed, that node is eliminated and the order of the remaining circuit is reduced making its suspendance contribution zero.
- Su.6. Suspendance of a component shorted to ground from both terminal (short structure) is unity. Suspendance of a component shorted to ground from one terminal (solo structure) is equal to admittance of the component. Suspendance of a component floating from both terminal (open structure) is zero.
- Su.7. Suspendance contribution of voltage controlled current sources are extracted when passive circuit components are shorted converting these sources to an equivalent passive admittance or disabling them by shorting or removing them from circuit.
- Su.8. Cross coupled voltage controlled current sources create an additional suspendance term which is equal to products of their transadmittance gains. The sign is determined by number of dependent current sources and the number of opposing current directions.
- Su.9. Total circuit suspendance is calculated by summing the contributions of passive circuit components and cross coupled voltage controlled current sources.
- Su.10. To extract suspendance terms efficiently, minimum expansion algorithm is used that determines which passive components to short during suspendance analysis.
- Su.11. If cross coupled voltage controlled current sources exist in a circuit, all shunt, sequential and bridged

components must be shorted and all circuit nodes must be eliminated.

- Su.12. If shunt voltage controlled current sources without cross coupled patterns exist in a circuit, all shunt and sequential components must be shorted and one of the circuit nodes must be eliminated.
- Su.13. for any other cases, only shunt components must be shorted in order to calculate circuit suspendance. When shunt components are removed, remaining circuit becomes float and its suspendance contribution becomes zero.

The minimum expansion algorithm explained above (Su.10 to Su.13) is obtained by studying the admittance determinant for circuits that include passive components and voltage controlled current sources. The naming for suspendance analysis is selected based on the fact that floating passive structures contribute nothing to admittance determinant unless they are connected to AC ground (suspended) from at least one node.

The suspendance terms of some popular patterns that often repeat in many electronic circuits are studied here before applying suspendance analysis to larger and more complex circuits in Section IV.

A. Suspendance of Basic Passive Structures

During suspendance analysis, many circuits are simplified to passive networks that include array, series, parallel, trigon and tetragon structures. The suspendance of these structures are extracted here.

1) Array Suspendance: A circuit is simplified to an array structure when all admittances are connected to ground from only one terminal, as shown in Fig. 2.

First, Y_1 is shorted and is multiplied by the suspendance of the remaining Y_2 to Y_n array structure. Y_1 is removed and Y_2 is then shorted and is multiplied by the suspendance of the remaining Y_3 to Y_n array structure. This shorting and removing algorithm continues until Y_n with a known solo suspendance remains in the circuit. Therefore, the suspendance of the array structure is given by

$$Su = Y_1 Y_2 \dots Y_n \quad (2)$$

2) Series Suspendance: A circuit is simplified to a series structure when only one of the admittances is connected to ground and other admittances are connected sequentially, as shown in Fig. 3.

First, Y_n is shorted and is multiplied by the suspendance of the remaining Y_1 to Y_{n-1} series structure. Y_n is removed and Y_{n-1} is then shorted and is multiplied by the suspendance of the remaining Y_1 to Y_{n-2} series structure. This shorting and removing algorithm continues until Y_1 with a known solo suspendance remains in the circuit. Therefore, the suspendance of the series structure is given by

$$Su = Y_1 Y_2 \dots Y_n \quad (3)$$

Analyzing circuits in Fig. 4 which are variants of array and series structures shows that all these circuits have the same

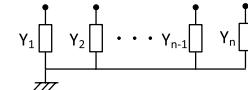


Fig. 2. Array structure.

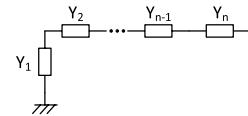


Fig. 3. Series structure.

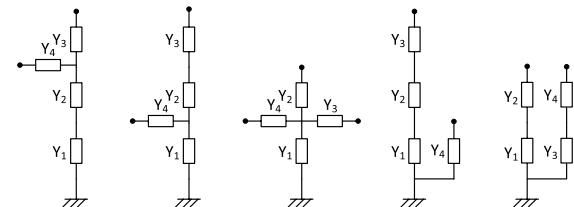


Fig. 4. Variations of tapped series and array structures.

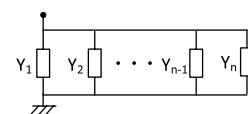


Fig. 5. Parallel structure.

suspendance given by (4)

$$Su = Y_1 Y_2 Y_3 Y_n \quad (4)$$

3) Parallel Suspendance: A circuit is simplified to a parallel structure when all parallel admittances are connected to ground from one terminal, as shown in Fig. 5.

First, Y_1 is shorted. The suspendance will be the shorted admittance Y_1 times the suspendance of the remaining circuit which is a short and has a suspendance of unity. The result becomes Y_1 .

Second, Y_1 is removed and Y_2 is shorted. The suspendance will be the shorted admittance Y_2 times the suspendance of the remaining circuit which is a short and has a suspendance of unity. The result becomes Y_2 .

This shorting and removing algorithm continues until Y_n with a known solo suspendance remains and Y_1 to Y_{n-1} shorted earlier are removed from circuit. Therefore, the suspendance of the parallel structure is obtained by summing all individual suspendances obtained earlier and is given by

$$Su = Y_1 + Y_2 + \dots + Y_n \quad (5)$$

4) Trigon Suspendance: A circuit is simplified to a trigon (3-element) structure when the remaining three admittances are circularly connected together and are connected to ground from only one node as shown in Fig. 6.

First, Y_1 is shorted. The suspendance will be the shorted admittance Y_1 times the suspendance of the remaining circuit which is a parallel structure and has a suspendance of $Y_2 + Y_3$. The result becomes $Y_1(Y_2 + Y_3)$.

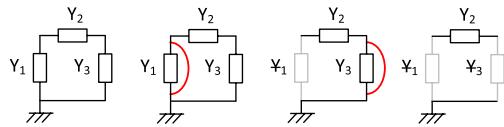


Fig. 6. Trigon structure and shorting steps to calculate its suspendance.

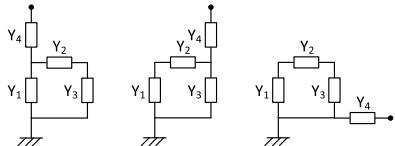


Fig. 7. Variations of tapped trigon structures.

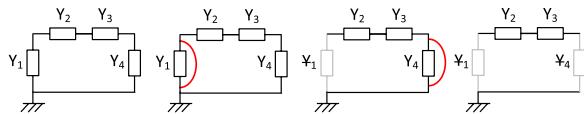


Fig. 8. Tetragon structure and shorting steps to calculate its suspendance.

Second, Y_3 is shorted and Y_1 is removed. The suspendance will be the shorted admittance Y_3 times the suspendance of the remaining circuit which is a solo structure and has a suspendance of Y_2 . Therefore, the result becomes Y_2Y_3 .

After Y_3 is removed, the remaining circuit will be open structure with a suspendance of zero. Therefore, the suspenance of the trigon structure becomes

$$Su = Y_1(Y_2 + Y_3) + Y_2Y_3 \quad (6)$$

Analyzing circuits in Fig. 7 which are variants of trigon structure shows that all these circuits have the same suspendance given by (7)

$$Su = Y_4[Y_1(Y_2 + Y_3) + Y_2Y_3] \quad (7)$$

5) *Tetragon Suspendance:* A circuit is simplified to a tetragon (4-element) structure when the remaining four admittances are circularly connected together and are connected to ground from only one node as shown in Fig. 8.

First, Y_1 is shorted. The suspendance will be the shorted admittance Y_1 times the suspendance of the remaining circuit which is a trigon structure and has a suspendance of $Y_2(Y_3 + Y_4) + Y_3Y_4$. The result becomes $Y_1[Y_2(Y_3 + Y_4) + Y_3Y_4]$.

Second, Y_4 is shorted and Y_1 is removed. The suspendance will be the shorted admittance Y_4 times the suspendance of the remaining circuit which is a series structure and has a suspendance of Y_2Y_3 .

After Y_4 is removed, the remaining circuit will be open structure with a suspendance of zero. Therefore, the suspendance of the tetragon structure becomes

$$Su = Y_1[Y_2(Y_3 + Y_4) + Y_3Y_4] + Y_2Y_3Y_4 \quad (8)$$

B. Suspendance of Basic Active Structures

Dependent sources in a circuit should be converted to voltage controlled current sources using simple source transformation because these type of sources have transadmittance gains that can be easily added to or subtracted from

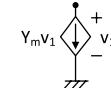


Fig. 9. Passive source structure.

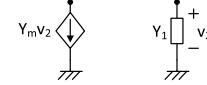


Fig. 10. Open source structure.

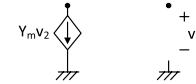


Fig. 11. A variation of the open source structure.

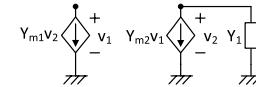


Fig. 12. Cross coupled structure.

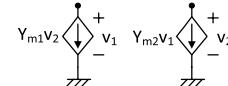


Fig. 13. A variation of the cross coupled structure.

other circuit admittances for generating suspendance terms. Applying suspendance rules by shorting passive circuit components one at a time replaces the voltage controlled current sources with either admittances or removes or shorts these sources. These cases are studied by the following structures.

1) *Passive Source Suspendance:* A passive source structure is shown in Fig. 9. Y_m is the transadmittance gain of the controlled current source. The current of the source depends on the voltage across the source making it behave as Y_m transadmittance. The suspendance becomes $Su = Y_m$.

2) *Open Source Suspendance:* An open source structure is shown in Fig. 10. Shorting Y_1 sets the current of the source to zero making it behave as an open circuit and have no impact on circuit suspendance. The suspendance becomes $Su = Y_1$.

A variation of the open source structure is shown in Fig. 11. Here Y_1 is set to zero and the suspendance becomes $Su = 0$.

3) *Cross Coupled Suspendance:* A cross coupled structure is shown in Fig. 12. The voltage v_2 becomes $\frac{-Y_{m2}v_1}{Y_1}$ making $Y_{m1}v_2$ behave as $\frac{-Y_{m1}Y_{m2}}{Y_1}$ transadmittance. When this transadmittance is shorted during suspendance analysis, v_1 becomes zero and the $Y_{m2}v_1$ current source acts as an open circuit and have no impact on circuit suspendance. The circuit becomes an array structure and its suspendance becomes $Su = -Y_{m1}Y_{m2}$.

A variation of the cross coupled structure is shown in Fig. 13. Here Y_1 is set to zero and the suspendance becomes $Su = -Y_{m1}Y_{m2}$.

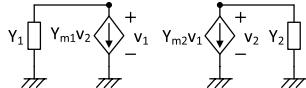


Fig. 14. Another variation of the cross coupled structure.

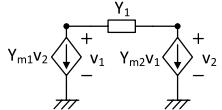


Fig. 15. A different variation of the cross coupled structure.

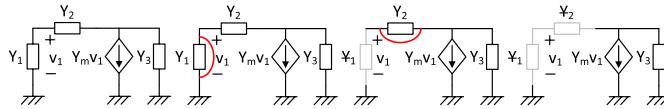


Fig. 16. A circuit with shunt source structure and shorting steps to calculate its suspandance.

Another variation of the cross coupled structure is shown in Fig. 14. The circuit suspandance is $S_u = Y_2(Y_1 - \frac{Y_{m1}Y_{m2}}{Y_2})$.

A different variation of the cross coupled structure is shown in Fig. 15. First Y_1 is shorted and both current sources act as parallel transadmittances. Next, Y_1 which was shorted in the first step is set to zero (removed from circuit) and the circuit becomes the cross coupled structure studied earlier. The circuit suspandance becomes $S_u = Y_1(Y_{m1} + Y_{m2}) - Y_{m1}Y_{m2}$.

4) Shunt Source Suspandance: A circuit with a $Y_{m1}v_1$ shunt source is shown Fig. 16. One node must be eliminated to reduce the circuit order while calculating the suspandance. This can be achieved by shorting and removing either Y_1 and Y_2 or Y_3 and Y_2 .

First, admittance Y_1 is shorted making the controlling voltage v_1 zero and removing the controlled current source. The remaining circuit will be the parallel combination of two admittances Y_2 and Y_3 . The suspandance becomes $Y_1(Y_2 + Y_3)$.

Second, admittance Y_2 is shorted and Y_1 is removed making the controlled current source act as Y_m admittance. The remaining circuit will be the parallel combination of Y_m and Y_3 . The circuit suspandance becomes $Y_2(Y_m + Y_3)$.

Removing Y_1 and Y_2 eliminates one node and reduces the circuit order and there will be no need to continue the suspandance calculation. The overall suspandance of the circuit shown Fig. 16 will be the sum of all individual answers obtained at each step above and is given by $S_u = Y_1(Y_2 + Y_3) + Y_2(Y_m + Y_3)$.

5) Sequential Source Suspandance: A circuit with a $Y_{m1}v_1$ sequential (non-shunt) source is shown Fig. 17. Shorting and removing passive shunt components would be enough to calculate the suspandance.

First, Y_1 is shorted making the controlling voltage V_1 zero and removing the controlled current source. The remaining circuit will be solo with admittance Y_2 . The circuit suspandance becomes Y_1Y_2 .

Second, Y_2 is shorted and Y_1 is removed making the controlled current source act as Y_m admittance. The remaining

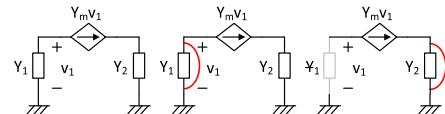


Fig. 17. A circuit with sequential source structure and shorting steps to calculate its suspandance.

circuit will be solo with admittance Y_m . The circuit suspandance becomes Y_2Y_m .

The overall suspandance of the circuit shown in Fig. 17 will be the sum of all individual answers obtained at each step above and is given by $S_u = Y_1Y_2 + Y_2Y_m$.

In the next section, four-node circuits are studied using suspandance analysis to illustrate the effectiveness of this method. The general notation that will be used in extraction of suspandance terms is presented in (9)

$$S_u = \left(\sum_1 Y \right) \left(\left(\sum_{1,1} Y \right) (S_{u1,1}) + \dots + \left(\sum_{1,q} Y \right) (S_{u1,q}) \right) + \dots + \left(\sum_p Y \right) \left(\left(\sum_{p,1} Y \right) (S_{up,1}) + \dots + \left(\sum_{p,q} Y \right) (S_{up,q}) \right) \quad (9)$$

$\sum_p Y$ represents the p^{th} admittance shorted, where p is equal to or less than the total number of passive components in the circuit, $\sum_{p,q} Y$ is the q^{th} admittance shorted in the p^{th} sub-circuit and $S_{up,q}$ is its corresponding suspandance. Comparing the results derived in the next section with (9) helps to better understand and follow the steps used in extracting suspandance terms.

IV. ADMITTANCE CALCULATION

In this section, the practical application of suspandance analysis for calculating node admittances of two four-node circuits are studied. The first circuit is a two-stage BJT amplifier with feedback and the second circuit is an active MOSFET inductor. High frequency models are incorporated for transistors of these circuits. The node admittances of each circuit is simulated with Spice and is compared with the result obtained from suspandance analysis to verify the effectiveness of this method.

A. Two-Stage BJT Amplifier

The circuit of a two-stage BJT amplifier that was primitively studied in [42] without inclusion of parasitic capacitors and without extraction of all node admittances is shown in Fig. 18. M_1 is an npn transistor with common base configuration and M_2 is a pnp transistor with emitter degeneration configuration. The AC signal travels from node (i) towards nodes (x), (y) and (o). There are two bridged paths in the circuit that are formed by G_f and $C_{\mu 2}$.

The AC model of the amplifier is shown in Fig. 19. Transistors are assumed to operate in active region and are replaced by their high frequency small-signal model. DC sources are discarded from the model because of superposition and separating AC and DC analyses.

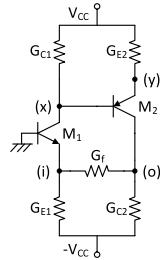


Fig. 18. A two-stage BJT amplifier.

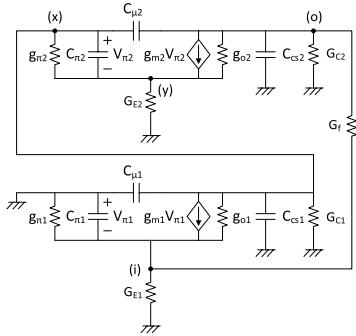
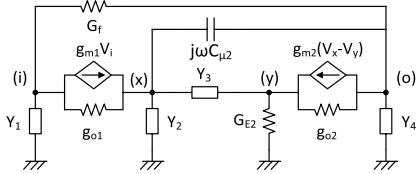


Fig. 19. Small-signal AC model of the two-stage BJT amplifier.

Fig. 20. Π -arrayed small-signal AC model of the two-stage BJT amplifier.

The simplified Π -arrayed AC model of the amplifier is shown in Fig. 20. The following parameters are expressed based on the values in Fig. 19.

$$Y_1 = G_{E1} + g_{\pi 1} + j\omega C_{\pi 1} \quad (10)$$

$$Y_2 = G_{C1} + j\omega(C_{\mu 1} + C_{cs1}) \quad (11)$$

$$Y_3 = g_{\pi 2} + j\omega C_{\pi 2} \quad (12)$$

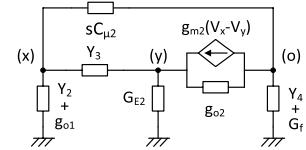
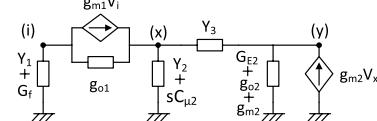
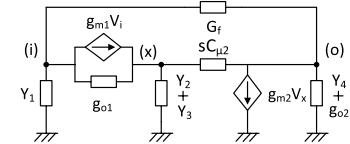
$$Y_4 = G_{C2} + j\omega C_{cs2} \quad (13)$$

where g_m is transconductance gain, g_o is the output conductance, g_π is the input conductance and C_π , C_μ and C_{cs} are parasitic capacitors of transistors.

Admittances at (i), (x), (y) and (o) nodes of the circuit are calculated by suspendance analysis. Suspendance of the whole circuit as well as suspendances when each of these nodes are shorted must be calculated. These nodes can be shorted in any order. First, Y_1 is shorted, as shown in Fig. 21, and the first circuit suspendance $Su1$ is given by (14).

$$\begin{aligned} Su1 = & (G_f + Y_4) \times ((Y_2 + g_{o1} + sC_{u2}) \times (G_{E2} + Y_3 + g_{m2} + g_{o2}) + \\ & (G_{E2} + g_{o2}) \times Y_3) + \\ & (Y_2 + g_{o1}) \times ((G_{E2} + Y_3) \times (g_{o2} + sC_{u2}) + sC_{u2} \times (g_{m2} + g_{o2})) + \\ & G_{E2} \times (g_{o2} \times (Y_3 + sC_{u2}) + Y_3 \times sC_{u2} + sC_{u2} \times g_{m2}) \end{aligned} \quad (14)$$

Second, Y_4 is shorted, as shown in Fig. 22, and the second circuit suspendance $Su2$ is given

Fig. 21. Sub-circuit after shorting Y_1 .Fig. 22. Sub-circuit after shorting Y_4 .Fig. 23. Sub-circuit after shorting G_{E2} .

by (15).

$$\begin{aligned} Su2 = & (G_f + Y_1) \times ((G_{E2} + g_{o2}) \times (Y_2 + Y_3 + g_{o1} + sC_{u2}) + \\ & (Y_2 + g_{o1} + sC_{u2}) \times (Y_3 + g_{m2})) + \\ & (G_{E2} + g_{o2}) \times ((Y_2 + Y_3 + sC_{u2}) \times (g_{m1} + g_{o1})) + \\ & (Y_2 + sC_{u2}) \times ((g_{m1} + g_{o1}) \times (Y_3 + g_{m2})) \end{aligned} \quad (15)$$

Because Y_1 was shorted in previous step, it is set to zero and $\overline{Su2}$ is given by

$$\begin{aligned} \overline{Su2} = & G_f \times ((G_{E2} + g_{o2}) \times (Y_2 + Y_3 + g_{o1} + sC_{u2}) + \\ & (Y_2 + g_{o1} + sC_{u2}) \times (Y_3 + g_{m2})) + \\ & (G_{E2} + g_{o2}) \times ((Y_2 + Y_3 + sC_{u2}) \times (g_{m1} + g_{o1})) + \\ & (Y_2 + sC_{u2}) \times ((g_{m1} + g_{o1}) \times (Y_3 + g_{m2})) \end{aligned} \quad (16)$$

Third, G_{E2} is shorted, as shown in Fig. 23, and the third circuit suspendance $Su3$ is given by (17).

$$\begin{aligned} Su3 = & (Y_4 + g_{o2}) \times ((Y_2 + Y_3 + sC_{u2}) \times (G_f + Y_1 + g_{m1} + g_{o1}) + \\ & (G_f + Y_1) \times g_{o1}) + \\ & (Y_2 + Y_3) \times ((Y_1 + g_{m1} + g_{o1}) \times (G_f + sC_{u2}) + sC_{u2} \times G_f) + \\ & Y_1 \times (G_f \times (g_{o1} + sC_{u2}) + g_{o1} \times sC_{u2} + sC_{u2} \times g_{m2}) + \\ & g_{o1} \times ((G_f + sC_{u2}) \times g_{m2}) + \\ & G_f \times (sC_{u2} \times g_{m2} + g_{m1} \times g_{m2}) + \\ & sC_{u2} \times g_{m2} \times g_{m1} \end{aligned} \quad (17)$$

Because Y_1 and Y_4 were shorted in previous steps, they are set to zero and $\overline{Su3}$ is given by

$$\begin{aligned} \overline{Su3} = & g_{o2} \times ((Y_2 + Y_3 + sC_{u2}) \times (G_f + g_{m1} + g_{o1}) + G_f \times g_{o1}) + \\ & (Y_2 + Y_3) \times ((g_{m1} + g_{o1}) \times (G_f + sC_{u2}) + sC_{u2} \times G_f) + \\ & g_{o1} \times ((G_f + sC_{u2}) \times g_{m2}) + \\ & G_f \times (sC_{u2} \times g_{m2} + g_{m1} \times g_{m2}) + \\ & sC_{u2} \times g_{m2} \times g_{m1} \end{aligned} \quad (18)$$

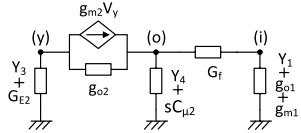
Fig. 24. Sub-circuit after shorting Y_2 .

TABLE I

TRANSISTOR PARAMETERS OF THE TWO-STAGE BJT AMPLIFIER

	β	g_m [Ω^{-1}]	g_o [Ω^{-1}]	g_π [Ω^{-1}]	C_π [F]	C_μ [F]	C_{cs} [F]
M ₁	50	10^{-2}	10^{-4}	$10^{-3}/5$	10^{-13}	10^{-14}	10^{-13}
M ₂	30	10^{-2}	10^{-4}	$10^{-3}/3$	10^{-13}	10^{-14}	10^{-13}

Fourth, Y_2 is shorted, as shown in Fig. 24, and the third circuit suspandance Su4 is given by (19)

$$\begin{aligned} \text{Su4} = & (Y_1 + g_{m1} + g_{o1}) \times ((G_f + Y_4 + sC_{u2}) \times (G_{E2} + Y_3 + g_{m2} + g_{o2}) + \\ & (G_{E2} + Y_3) \times g_{o2}) + \\ & (Y_4 + sC_{u2}) \times ((G_{E2} + Y_3 + g_{m2} + g_{o2}) \times G_f) + \\ & (G_{E2} + Y_3) \times g_{o2} \times G_f \end{aligned} \quad (19)$$

Because Y_1 , Y_4 and G_{E2} were shorted in previous steps, they are set to zero and $\overline{\text{Su4}}$ is given by

$$\begin{aligned} \overline{\text{Su4}} = & Y_2 \times ((g_{m1} + g_{o1}) \times ((G_f + sC_{u2}) \times (Y_3 + g_{m2} + g_{o2}) + Y_3 \times g_{o2}) + \\ & sC_{u2} \times ((Y_3 + g_{m2} + g_{o2}) \times G_f) + \\ & Y_3 \times g_{o2} \times G_f \end{aligned} \quad (20)$$

Based on Su.13 explained in Section III, since voltage controlled current sources do not form cross coupled patterns and because these sources are not in shunt format, there will be no need to short passive sequential and bridge components. Shorting passive shunt components would be enough to give the total suspandance. Therefore, the overall suspandance of the two-stage BJT amplifier is given by

$$O(j\omega) = Y_1 \text{Su1} + Y_4 \overline{\text{Su2}} + G_{E2} \overline{\text{Su3}} + Y_2 \overline{\text{Su4}} \quad (21)$$

Direct determinant calculation of the circuit produces 291 terms while each term is the product of 4 elements. Determinant has redundancy and after tedious term cancellations, 121 terms while each term is the product of 4 elements remain. Results derived from suspandance analysis has only 104 elements which are efficiently factored and are easy to simplify if element values are given. Calculating circuit determinant using suspandance analysis achieves $\frac{104}{4 \times 121} = 21.5\%$ term reduction (more than four times storage efficiency) when compared with direct determinant calculation. To verify the accuracy of the suspandance analysis, numerical values are substituted and the calculated node admittances are compared with results obtained from Spice simulation. It is assumed $G_{E1} = 10^{-2} \Omega^{-1}$, $G_{C1} = 10^{-3} \Omega^{-1}$, $G_{E2} = 10^{-2} \Omega^{-1}$, $G_{C2} = 10^{-3} \Omega^{-1}$ and $G_f = 10^{-2} \Omega^{-1}$. Transistor parameters are listed in Table I.

Admittance Y_i at node (i) of the circuit is equal to the ratio of the whole circuit suspandance $O(j\omega)$ to the suspandance $D_i(j\omega)$ when node (i) is shorted. $D_i(j\omega)$ is equal to $\text{Su}i$ calculated earlier. Therefore, Y_i is given by (22), shown at the bottom of the next page.

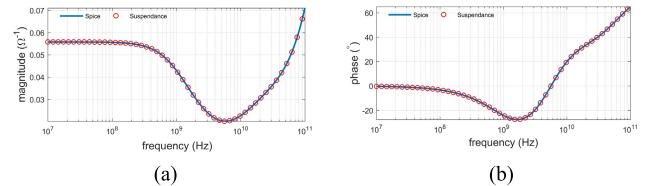


Fig. 25. Plot of node (i) Admittance, (a) Magnitude and (b) Phase.

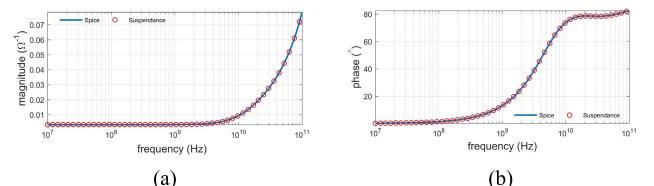


Fig. 26. Plot of node (x) Admittance, (a) Magnitude and (b) Phase.

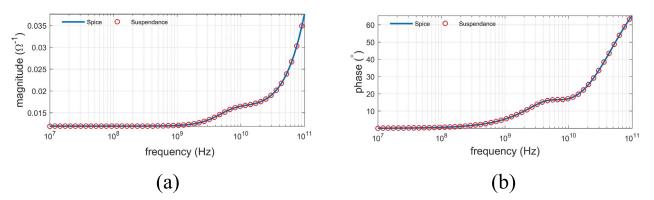


Fig. 27. Plot of node (y) Admittance, (a) Magnitude and (b) Phase.

$D_i(j\omega)$ when node (i) is shorted. $D_i(j\omega)$ is equal to $\text{Su}i$ calculated earlier. Therefore, Y_i is given by (22), shown at the bottom of the next page.

The admittance Y_i of the two-stage BJT amplifier is simulated in Spice and is compared with the result obtained from suspandance analysis. Both plots are identical as shown in Fig. 25.

Admittance Y_x at node (x) of the circuit is equal to the ratio of the whole circuit suspandance $O(j\omega)$ to the suspandance $D_x(j\omega)$ when node (x) is shorted. $D_x(j\omega)$ is equal to $\text{Su}4$ calculated earlier. Therefore, Y_x is given by (23), shown at the bottom of the next page.

The admittance Y_x of the two-stage BJT amplifier is simulated in Spice and is compared with the result obtained from suspandance analysis. Both plots are identical as shown in Fig. 26.

Admittance Y_y at node (y) of the circuit is equal to the ratio of the whole circuit suspandance $O(j\omega)$ to the suspandance $D_y(j\omega)$ when node (y) is shorted. $D_y(j\omega)$ is equal to $\text{Su}3$ calculated earlier. Therefore, Y_y is given by (24), shown at the bottom of the next page.

The admittance Y_y of the two-stage BJT amplifier is simulated in Spice and is compared with the result obtained from suspandance analysis. Both plots are identical as shown in Fig. 27.

Admittance Y_o at node (o) of the circuit is equal to the ratio of the whole circuit suspandance $O(j\omega)$ to the suspandance $D_o(j\omega)$ when node (o) is shorted. $D_o(j\omega)$ is equal to $\text{Su}2$ calculated earlier. Therefore, Y_o is given by (25), shown at the bottom of the next page.

The admittance Y_o of the two-stage BJT amplifier is simulated in Spice and is compared with the result obtained

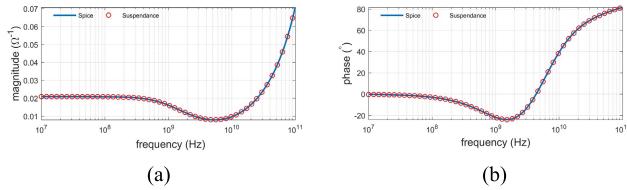


Fig. 28. Plot of node (o) Admittance, (a) Magnitude and (b) Phase.

from suspendance analysis. Both plots are identical as shown in Fig. 28.

As demonstrated above, the suspendance analysis accurately solves the two-stage BJT amplifier regardless of the existence of feedback mechanism formed by G_f and M_2 . Using 8 equations, (14) to (21), 4 node admittances were calculated without writing any KVL and KCL and without the requirement to solve systems of equations. This means the admittance transfer function for each node is only obtained by driving two suspendance terms demonstrating an excellent efficiency for suspendance analysis.

B. Active Inductor

The circuit of an active inductor realized by MOSFETs that was studied in [43] without extraction of accurate node admittances is shown in Fig. 29. Transistors M_1 , M_6 and M_7 are used for biasing, M_2 , M_3 and M_5 are in common source configuration and M_4 and M_5 are used for feedback. The AC signal travels from node (i) towards nodes (x), (y) and (z).

The AC model of the active inductor is shown in Fig. 30. Transistors are assumed to operate in saturation region and are replaced by their high frequency small-signal model. It is also assumed that M_4 body effect can be neglected. DC sources are discarded from the model because of superposition and separating AC and DC analyses.

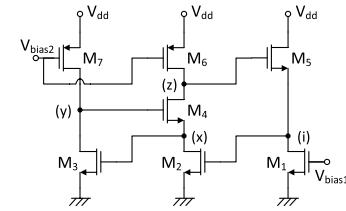


Fig. 29. An active MOSFET inductor.

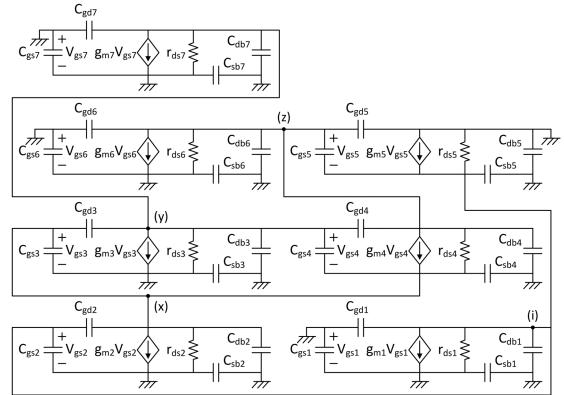


Fig. 30. Small-signal AC model of the active MOSFET inductor.

The simplified Π -arrayed AC model of the inductor is shown in Fig. 31. The following parameters are expressed based on the values in Fig. 30

$$Y_1 = g_{ds1} + g_{ds5} + g_{m5} + j\omega(C_{gd1} + C_{db1} + C_{gs2} + C_{sb5}) \quad (26)$$

$$Y_2 = g_{ds6} + j\omega(C_{db4} + C_{gd5} + C_{gd6} + C_{db6}) \quad (27)$$

$$Y_3 = g_{ds3} + g_{ds7} + j\omega(C_{db3} + C_{gd7} + C_{db7}) \quad (28)$$

$$Y_4 = g_{ds2} + j\omega(C_{db2} + C_{gs3} + C_{sb4}) \quad (29)$$

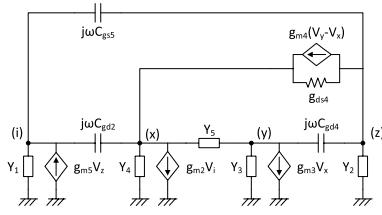
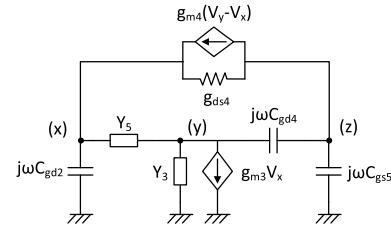
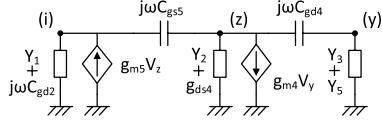
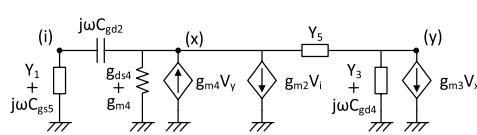
$$Y_5 = j\omega(C_{gd3} + C_{gs4}) \quad (30)$$

$$Y_i = \frac{i_i(j\omega)}{v_i(j\omega)} = \frac{O(j\omega)}{D_i(j\omega)} = \frac{1.217 \times 10^{31} + 7.33 \times 10^{20}(j\omega) + 1.443 \times 10^{10}(j\omega)^2 + 0.0703 \times (j\omega)^3 + 1 \times 10^{-13}(j\omega)^4}{2.181 \times 10^{32} + 3.311 \times 10^{22}(j\omega) + 4 \times 10^{11}(j\omega)^2 + 1 \times (j\omega)^3} \quad (22)$$

$$Y_x = \frac{i_x(j\omega)}{v_x(j\omega)} = \frac{O(j\omega)}{D_x(j\omega)} = \frac{1.449 \times 10^{31} + 8.729 \times 10^{20}(j\omega) + 1.718 \times 10^{10}(j\omega)^2 + 0.0837 \times (j\omega)^3 + 1.191 \times 10^{-13}(j\omega)^4}{4.362 \times 10^{33} + 1.039 \times 10^{23}(j\omega) + 6.082 \times 10^{11}(j\omega)^2 + 1 \times (j\omega)^3} \quad (23)$$

$$Y_y = \frac{i_y(j\omega)}{v_y(j\omega)} = \frac{O(j\omega)}{D_y(j\omega)} = \frac{6.615 \times 10^{30} + 3.984 \times 10^{20}(j\omega) + 7.841 \times 10^9(j\omega)^2 + 0.03821 \times (j\omega)^3 + 5.436 \times 10^{-14}(j\omega)^4}{5.55 \times 10^{32} + 2.5 \times 10^{22}(j\omega) + 4.15 \times 10^{11}(j\omega)^2 + 1 \times (j\omega)^3} \quad (24)$$

$$Y_o = \frac{i_o(j\omega)}{v_o(j\omega)} = \frac{O(j\omega)}{D_o(j\omega)} = \frac{1.329 \times 10^{31} + 8.002 \times 10^{20}(j\omega) + 1.575 \times 10^{10}(j\omega)^2 + 0.0767 \times (j\omega)^3 + 1.092 \times 10^{-13}(j\omega)^4}{6.353 \times 10^{32} + 9.226 \times 10^{22}(j\omega) + 6.007 \times 10^{11}(j\omega)^2 + 1 \times (j\omega)^3} \quad (25)$$

Fig. 31. Π -arrayed small-signal AC model of the active MOSFET inductor.Fig. 34. Sub-circuit after shorting Y_1 .Fig. 32. Sub-circuit after shorting Y_4 .Fig. 33. Sub-circuit after shorting Y_2 .

where g_m is transconductance gain, g_{ds} is the output conductance and C_{gs} , C_{gd} , C_{db} and C_{sb} are parasitic capacitors of transistors.

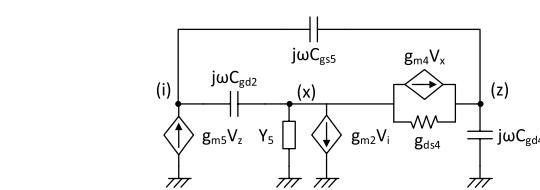
There are four shunt admittances (Y_1 , Y_2 , Y_3 and Y_4) in the circuit that must be shorted first for calculating the overall suspenance. Node (x) has dominant inductive characteristic and calculating admittance at node (x) will be derived here. Therefore, Y_4 is first shorted, as shown in Fig. 32. The suspenance term has only 29 elements and is given by (31)

$$\begin{aligned} Su1 = & (Y_2 + g_{ds4}) \times ((Y_1 + j\omega C_{gd2} + j\omega C_{gs5}) \times (Y_3 + Y_5 + j\omega C_{gd4})) + \\ & (Y_1 + j\omega C_{gd2}) \times ((Y_3 + Y_5) \times (j\omega C_{gd4} + j\omega C_{gs5}) + j\omega C_{gs5} \times j\omega C_{gd4} + \\ & j\omega C_{gd4} \times g_{m4}) + \\ & (Y_3 + Y_5) \times (j\omega C_{gd4} \times j\omega C_{gs5} + j\omega C_{gs5} \times -g_{m5}) + \\ & j\omega C_{gs5} \times (-g_{m5} \times j\omega C_{gd4} + j\omega C_{gd4} \times g_{m4}) \end{aligned} \quad (31)$$

Second, Y_2 is shorted and Y_4 which was shorted in previous step is set to zero or is removed from circuit, as shown in Fig. 33. The corresponding suspenance term includes 35 elements and is given by (32)

$$\begin{aligned} Su2 = & g_{ds4} \times ((Y_1 + j\omega C_{gd2} + j\omega C_{gs5}) \times (Y_3 + Y_5 + j\omega C_{gd4})) + \\ & (Y_1 + j\omega C_{gs5}) \times ((Y_3 + j\omega C_{gd4}) \times (Y_5 + g_{m4} + j\omega C_{gd2}) + \\ & j\omega C_{gd2} \times Y_5 + Y_5 \times g_{m3} + g_{m3} \times g_{m4}) + \\ & (Y_3 + j\omega C_{gd4}) \times ((Y_5 + g_{m4}) \times j\omega C_{gd2} + j\omega C_{gd2} \times g_{m2}) + \\ & Y_5 \times (g_{m3} \times j\omega C_{gd2} + j\omega C_{gd2} \times g_{m2}) + \\ & j\omega C_{gd2} \times g_{m3} \times g_{m4} \end{aligned} \quad (32)$$

Third, Y_1 is shorted and Y_4 and Y_2 which were shorted in previous steps are set to zero or are removed

Fig. 35. Sub-circuit after shorting Y_3 .

from circuit, as shown in Fig. 34. The corresponding suspenance term includes 40 elements and is given by (33)

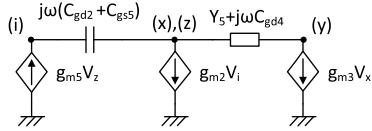
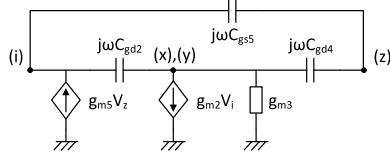
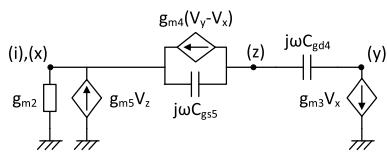
$$\begin{aligned} \overline{Su3} = & j\omega C_{gd2} \times ((g_{ds4} + j\omega C_{gs5}) \times (Y_3 + Y_5 + j\omega C_{gd4}) + \\ & (Y_3 + Y_5) \times j\omega C_{gd4} + j\omega C_{gd4} \times g_{m4}) + \\ & j\omega C_{gs5} \times ((Y_3 + j\omega C_{gd4}) \times (Y_5 + g_{ds4} + g_{m4}) + g_{ds4} \times Y_5 + \\ & Y_5 \times g_{m3} + g_{m3} \times g_{m4}) + \\ & Y_3 \times (Y_5 \times (g_{ds4} + j\omega C_{gd4}) + j\omega C_{gd4} \times (g_{ds4} + g_{m4})) + \\ & g_{ds4} \times ((Y_5 + j\omega C_{gd4}) \times g_{m3}) + \\ & Y_5 \times g_{m3} \times j\omega C_{gd4} + \\ & j\omega C_{gd4} \times g_{m4} \times g_{m3} \end{aligned} \quad (33)$$

Fourth, Y_3 is shorted and Y_4 , Y_2 and Y_1 which were shorted in previous steps are set to zero or are removed from circuit, as shown in Fig. 35. The corresponding suspenance term includes 40 terms and is given by (34)

$$\begin{aligned} \overline{Su4} = & Y_5 \times ((g_{ds4} + j\omega C_{gd4}) \times (j\omega C_{gd2} + j\omega C_{gs5}) + j\omega C_{gd2} \times j\omega C_{gs5} + \\ & j\omega C_{gs5} \times -g_{m5}) + \\ & j\omega C_{gd4} \times ((g_{ds4} + g_{m4}) \times (j\omega C_{gd2} + j\omega C_{gs5}) + j\omega C_{gs5} \times j\omega C_{gd2} + \\ & j\omega C_{gd2} \times g_{m2}) + \\ & g_{ds4} \times ((j\omega C_{gd2} + j\omega C_{gs5}) \times (g_{m2} - g_{m5}) + g_{m2} \times g_{m5}) + \\ & j\omega C_{gd2} \times (g_{m2} \times j\omega C_{gs5} + j\omega C_{gs5} \times -g_{m5} - g_{m4} \times g_{m5}) + \\ & j\omega C_{gs5} \times (-g_{m5} \times g_{m4} + g_{m2} \times g_{m4}) + \\ & g_{m2} \times g_{m4} \times g_{m5} \end{aligned} \quad (34)$$

Because the circuit has cross coupled voltage controlled current sources, all sequential and bridged components must be shorted besides previously shorted shunt components and the contribution of cross coupled voltage sources must be added in order to obtain the overall circuit suspenance.

Fifth, g_{ds4} is shorted and Y_4 , Y_2 , Y_1 and Y_3 which were shorted in previous steps are set to zero or are removed from

Fig. 36. Sub-circuit after shorting g_{ds4} .Fig. 37. Sub-circuit after shorting Y_5 .Fig. 38. Sub-circuit after shorting $j\omega C_{gd2}$.

circuit, as shown in Fig. 36. The corresponding suspendance term includes 14 elements and is given by (35)

$$\overline{Su5} = (j\omega C_{gd2} + j\omega C_{gs5}) \times ((g_{m2} - g_{m5}) \times (Y_5 + j\omega C_{gd4}) + (Y_5 + j\omega C_{gd4}) \times g_{m3}) + (Y_5 + j\omega C_{gd4}) \times g_{m2} \times g_{m5} \quad (35)$$

Sixth, Y_5 is shorted and Y_4 , Y_2 , Y_1 , Y_3 and g_{ds4} which were shorted in previous steps are set to zero or are removed from circuit, as shown in Fig. 37. The corresponding suspendance term includes 20 elements and is given by (36)

$$\begin{aligned} \overline{Su6} = & g_{m3} \times (j\omega C_{gd4} \times (j\omega C_{gd2} + j\omega C_{gs5}) + j\omega C_{gd2} \times j\omega C_{gs5} + j\omega C_{gs5} \times -g_{m5}) + \\ & j\omega C_{gd4} \times ((j\omega C_{gd2} + j\omega C_{gs5}) \times (g_{m2} - g_{m5}) + g_{m2} \times g_{m5}) + \\ & j\omega C_{gd2} \times (g_{m2} \times j\omega C_{gs5} + j\omega C_{gs5} \times -g_{m5}) \end{aligned} \quad (36)$$

Seventh, $j\omega C_{gd2}$ is shorted and Y_1 , Y_4 , Y_3 , Y_2 , g_{ds4} and Y_5 which were shorted in previous steps are set to zero or are removed from circuit, as shown Fig. 38. The corresponding suspendance term includes 19 elements and is given by (37)

$$\begin{aligned} \overline{Su7} = & g_{m2} \times (j\omega C_{gs5} \times j\omega C_{gd4} + j\omega C_{gd4} \times g_{m4}) + \\ & j\omega C_{gs5} \times (-g_{m5} \times j\omega C_{gd4} + j\omega C_{gd4} \times g_{m3}) + \\ & j\omega C_{gd4} \times (g_{m4} \times (g_{m3} - g_{m5}) + g_{m3} \times g_{m5}) + \\ & -g_{m3} \times g_{m4} \times g_{m5} \end{aligned} \quad (37)$$

Eight, $j\omega C_{gs5}$ is shorted and Y_1 , Y_4 , Y_3 , Y_2 , g_{ds4} , Y_5 and $j\omega C_{gd2}$ which were shorted in previous steps are set to zero or are removed from circuit, as shown in Fig. 39.

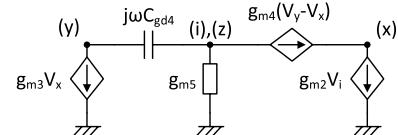
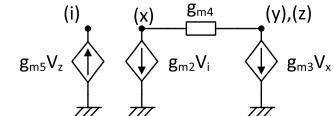
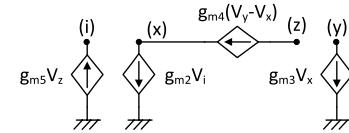
Fig. 39. Sub-circuit after shorting $j\omega C_{gs5}$.Fig. 40. Sub-circuit after shorting $j\omega C_{gd4}$.

Fig. 41. Sub-circuit after opening all passive elements.

The corresponding suspendance term includes 14 elements and is given by (38)

$$\begin{aligned} \overline{Su8} = & -g_{m5} \times (j\omega C_{gd4} \times g_{m4} + g_{m3} \times g_{m4}) + \\ & j\omega C_{gd4} \times (g_{m4} \times (g_{m2} + g_{m3}) + -g_{m2} \times g_{m3}) + \\ & g_{m2} \times g_{m3} \times g_{m4} \end{aligned} \quad (38)$$

Ninth, $j\omega C_{gd4}$ is shorted and Y_1 , Y_4 , Y_3 , Y_2 , g_{ds4} , Y_5 , $j\omega C_{gd2}$ and $j\omega C_{gs5}$ which were shorted in previous steps are set to zero or are removed from circuit, as shown in Fig. 40. The corresponding suspendance term includes 6 elements and is given by (39)

$$\overline{Su9} = g_{m4} \times g_{m2} \times g_{m5} + -g_{m2} \times g_{m3} \times g_{m5} \quad (39)$$

Last, all circuit elements that were shorted in previous steps are set to zero or are removed from circuit, as shown in Fig. 41. The contribution of the remaining nested cross coupled current sources is given by (40).

$$\overline{Su10} = g_{m2} \times g_{m3} \times g_{m4} \times g_{m5} \quad (40)$$

The principal determinant of the active inductor is given by

$$\begin{aligned} O(j\omega) = & Y_4 \overline{Su1} + Y_2 \overline{Su2} + Y_1 \overline{Su3} + Y_3 \overline{Su4} + g_{ds4} \overline{Su5} \\ & + Y_5 \overline{Su6} + j\omega C_{gd2} \overline{Su7} + j\omega C_{gs5} \overline{Su8} + j\omega C_{gd4} \overline{Su9} + \overline{Su10} \end{aligned} \quad (41)$$

Direct determinant calculation of the circuit produces 239 terms while each term is the product of 4 elements. Determinant has redundancy and after tedious term cancellations, 163 terms while each term is the product of 4 elements remain. Results derived from suspendance analysis has only 218 elements which are efficiently factored and are easy to simplify if element values are given. Calculating circuit determinant using suspendance analysis achieves $\frac{218}{4 \times 163} = 33.4\%$ term reduction (more than three times storage efficiency) when compared

TABLE II
TRANSISTOR PARAMETERS OF THE FOUR-NODE ACTIVE INDUCTOR

	$g_m [\Omega^{-1}]$	$g_{ds} [\Omega^{-1}]$	$C_{gs} [F]$	$C_{gd} [F]$	$C_{db} [F]$	$C_{sb} [F]$
M_1, M_6 and M_7	1m	1 μ	10f	5f	1f	2f
M_2	6m	6 μ	60f	30f	6f	12f
M_3	2m	2 μ	20f	10f	2f	4f
M_4	15m	15 μ	150f	75f	15f	30f
M_5	5m	5 μ	50f	25f	5f	10f

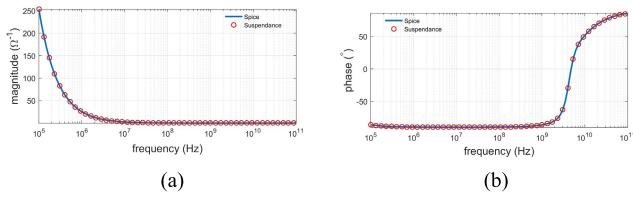


Fig. 42. Plot of node (x) Admittance, (a) Magnitude and (b) Phase.

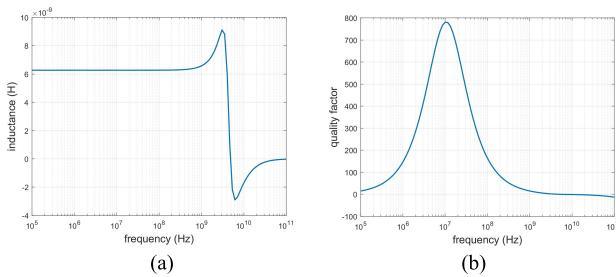


Fig. 43. (a) Inductance and (b) Quality factor at node (x).

with direct determinant calculation. To verify the accuracy of the determinant expansion, numerical values are substituted and the calculated node admittance is compared with results obtained from Spice simulation. Transistor parameters are listed in Table II.

As explained earlier, only node (x) which has a dominant inductive characteristic is considered for verification to illustrate the functionality of the active inductor. Admittance Y_x at node (x) of the circuit is equal to the ratio of the whole circuit suspandance $O(j\omega)$, given by (41), to the suspandance $D_x(j\omega)$, given by (31) as (42), shown at the bottom of this page.

The admittance Y_x of the active inductor is simulated in Spice and is compared with the result obtained from determinant expansion analysis. Both plots are identical as shown in Fig. 42.

The circuit has a constant inductance of 6.25nH from low frequencies up to 1 GHz, as shown in Fig. 43(a). The quality factor is shown in Fig. 43(b). It achieves a peak of 780 at 10 MHz. The self-resonance frequency is 4.8 GHz.

$$Y_x = \frac{i_x(j\omega)}{v_x(j\omega)} = \frac{O(j\omega)}{D_x(j\omega)} = \frac{1.804 \times 10^{29} + 1.116 \times 10^{19} (j\omega) + 4.855 \times 10^8 (j\omega)^2 + 0.01153 \times (j\omega)^3 + 1.085 \times 10^{-13} (j\omega)^4}{4.808 \times 10^{25} + 1.131 \times 10^{21} (j\omega) + 5.909 \times 10^{10} (j\omega)^2 + 1 \times (j\omega)^3} \quad (42)$$

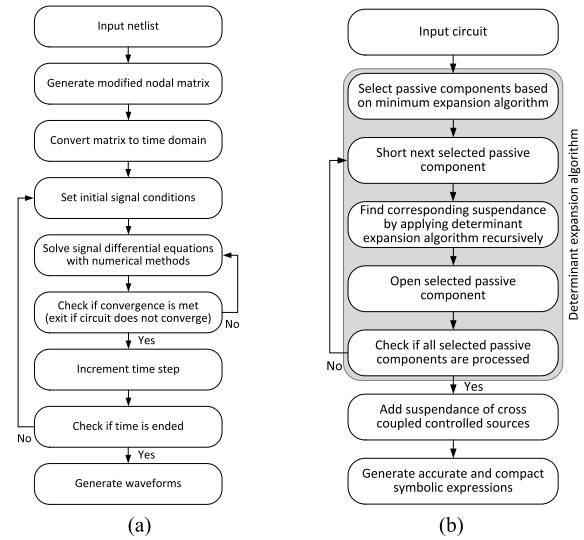


Fig. 44. Flowchart of (a) Spice and (b) Suspandance analyses.

The inductor can be utilized in a low-jitter oscillator operating at 10 MHz or can be utilized in an ideal waveform shaping filter that accommodates several hundreds of harmonics of the 10 MHz fundamental tone. As demonstrated above, the suspandance analysis accurately solves the node admittance of an active inductor regardless of the existence of feedback mechanism formed by M_4 and M_5 .

The Spice simulator used here as a reference is based on numerical analysis and solving circuit determinants derived from modified nodal matrices. Determinants consist of numeric values with only frequency variable and hence are very efficient to calculate and store in memory. It is also possible to convert each determinant from frequency domain to time domain and solve partial or ordinary differential equations while nonlinear elements are incorporated in the circuit, as shown in Fig. 44(a). However, there are two drawbacks of using numerical simulators for Analog circuits. First, outputs are waveforms and impacts of circuit components on transfer functions are obscured. Second, to understand the impact of circuit elements on circuit responses, parametric sweep must be performed which drastically increases the simulation time and the results might not be as predictable as expressions obtained from symbolic analysis.

The flowchart of Suspandance analysis is shown in Fig. 44(b). There is no arithmetic involved and determinant is expanded by a very simple algorithm. Results are efficiently factored and the compact expressions are very easy to simplify and to interpret.

The flowchart of the direct determinant calculation used in many algebraic symbolic analyses [44]–[45] is shown in

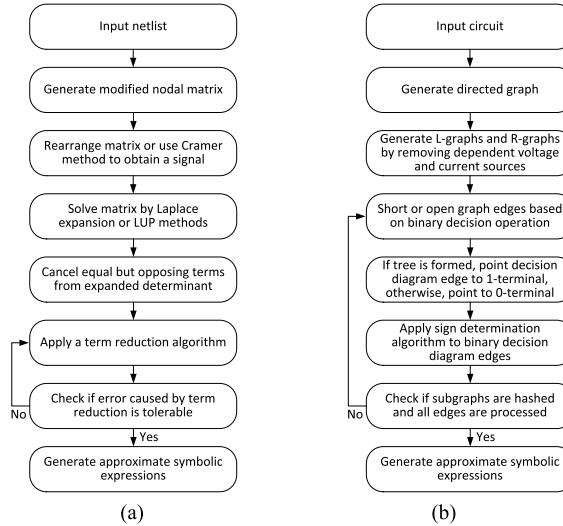


Fig. 45. Flowchart of (a) Algebraic and (b) Graph analyses.

TABLE III

PERFORMANCE COMPARISON OF FOUR CIRCUIT ANALYSIS METHODS

Analysis	Type	Speed	Parameter Sweep	Storage Efficiency	Accuracy	Output Format
Spice	numeric	Fast	Slow	High	High	Waveform
Suspendance	symbolic	Average	Fast	Average	Exact	Expression
Algebraic		Average	Fast	Low	Relative	and Waveform
Graph		Slow	Fast	Low	Relative	

Fig. 45(a). Most analyses use the same processing core but apply different reduction algorithm. Determinant is calculated using fast methods such as Laplace expansion [41] or LUP decomposition [46]. However, results need term cancellation that reduce the overall performance of the analysis.

The flowchart of the Graph analysis based on topological circuit analysis [47] is shown in Fig. 45(b). The generation of graphs, the allocation of signs and the implementation of decision diagrams needed for results generation and simplification make the speed of Graph analysis slower than other symbolic analyses.

The performance of the four analyses explained by flowcharts is compared and listed in Table III. Both algebraic and graph methods create redundant terms that must be simplified making their storage efficiency low. The accuracy of the expressions generated by these two methods also depends on their utilization of term reduction algorithm.

V. CONCLUSIONS

Suspendance analysis is an effective tool for accurate node admittance extraction of any circuit. Error free and cancellation free results are generated which are compactly factored and are very easy to simplify. Suspendance analysis does not use signal flow graphs and is performed directly on the original circuit. Furthermore, it does not require solving a matrix generated from the system of equations. The algorithm used for suspendance calculation is very easy to follow.

The node admittance of a circuit is obtained by the ratio of the circuit suspendance when the node is left open to the

circuit suspendance when the node is shorted to the reference ground. The suspendance of a circuit is expressed in terms of its admittances and transadmittances. All dependent sources in a circuit are converted to voltage controlled current sources because these sources have transadmittance gains that can be added to or subtracted from other circuit admittances for generating suspendance terms. To obtain the suspendance of a circuit, passive circuit components based on minimum expansion algorithm are shorted one at a time and their admittances are multiplied by the remaining circuit suspendances. Circuit components can be shorted in any order. When the suspendance of the remaining circuit in each step becomes a function of components shorted earlier, admittances of these shorted components are set to zero and they are removed from circuit in all succeeding calculations. Removing these components from the circuit considerably simplifies the suspendance analysis as it progresses. Whenever the order of suspendance terms drops, the suspendance analysis can be stopped which further reduces the number of iterations required to analyze a circuit. The overall suspendance is calculated by summing all individual results obtained from each step and the contribution of cross coupled voltage controlled current sources.

Two complex four-node circuits were analyzed in this paper and their node admittances were extracted using suspendance analysis. Node admittances were easily extracted using 2-3 suspendance calculations per node admittance. Existence of bridges and feedback components did not add to the complexity of the suspendance analysis. The compact and concise results obtained from suspendance analysis fully matched with the numerical results obtained from Spice simulations.

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