EE223 Analog Integrated Circuits
Fall 2018

Project Description

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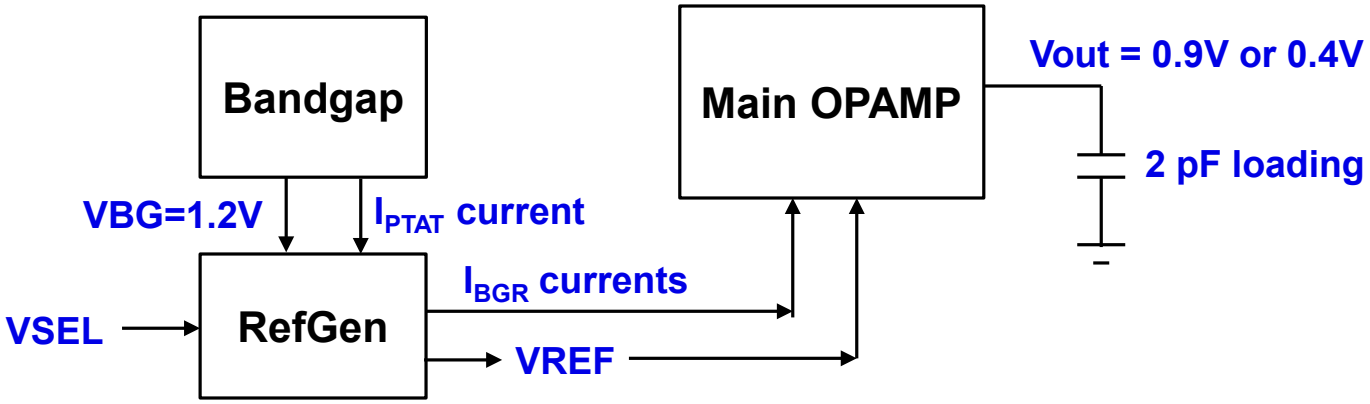
Project Logistics

1. A group of 3 students
2. Less number of students per group is fine
3. One Project Report per group
4. Report should be in IEEE conference paper format
5. Project Report due : 5 PM, Dec 10

Project Description

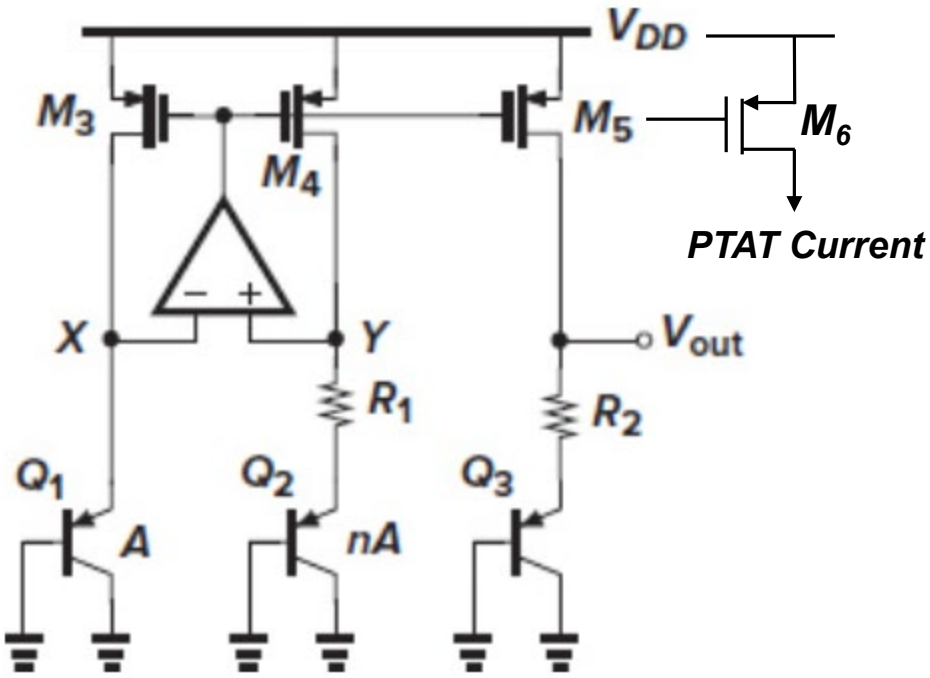


VSEL pulse is used to create either VREF = 0.9V or 0.4V.
See page 6 for the circuit diagram to implement this.

Main Circuit – High Gain OPAMP
Auxiliary Circuits – Bandgap, RefGen

- VDD=1.8V
- Device types available for the design
  → nmos2v, pmos2v, nmos2v_nat, vpnp5, resnsppoly, Ideal cap
- Results should meet the requirement over the following PVT corners
  - TT, 1.8V, 27C
  - SS, FF
  - 1.7V, 1.9V
  - -40C, 125C

Bandgap



Use PMOS diff pair input
for the Folded-cascode amplifier

Key Spec

Vout should be 1.2V.
Vout variation less than ±1% over PVT
PTAT current is nominally 25uA

Design Procedure

Q1=1, Q2=8, Q3=3
Choose R1 to get the current around I=4~5uA
Then choose R2 to get around Vout=1.2V

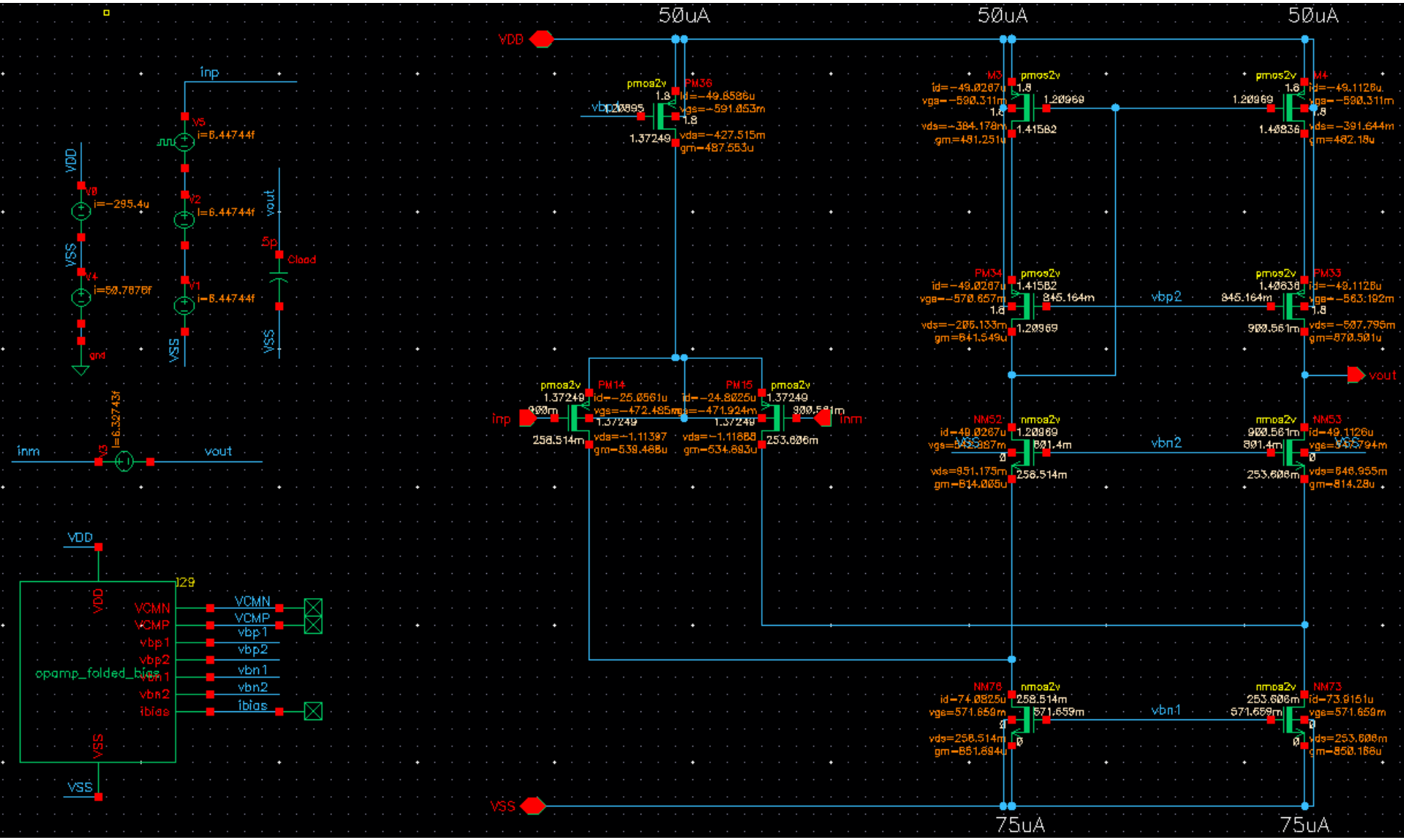
The OPAMP will force the node X and Y to be the same for the matching between M3 and M4.

M3, M4, M5 are generally sized to be the same to carry the same current.

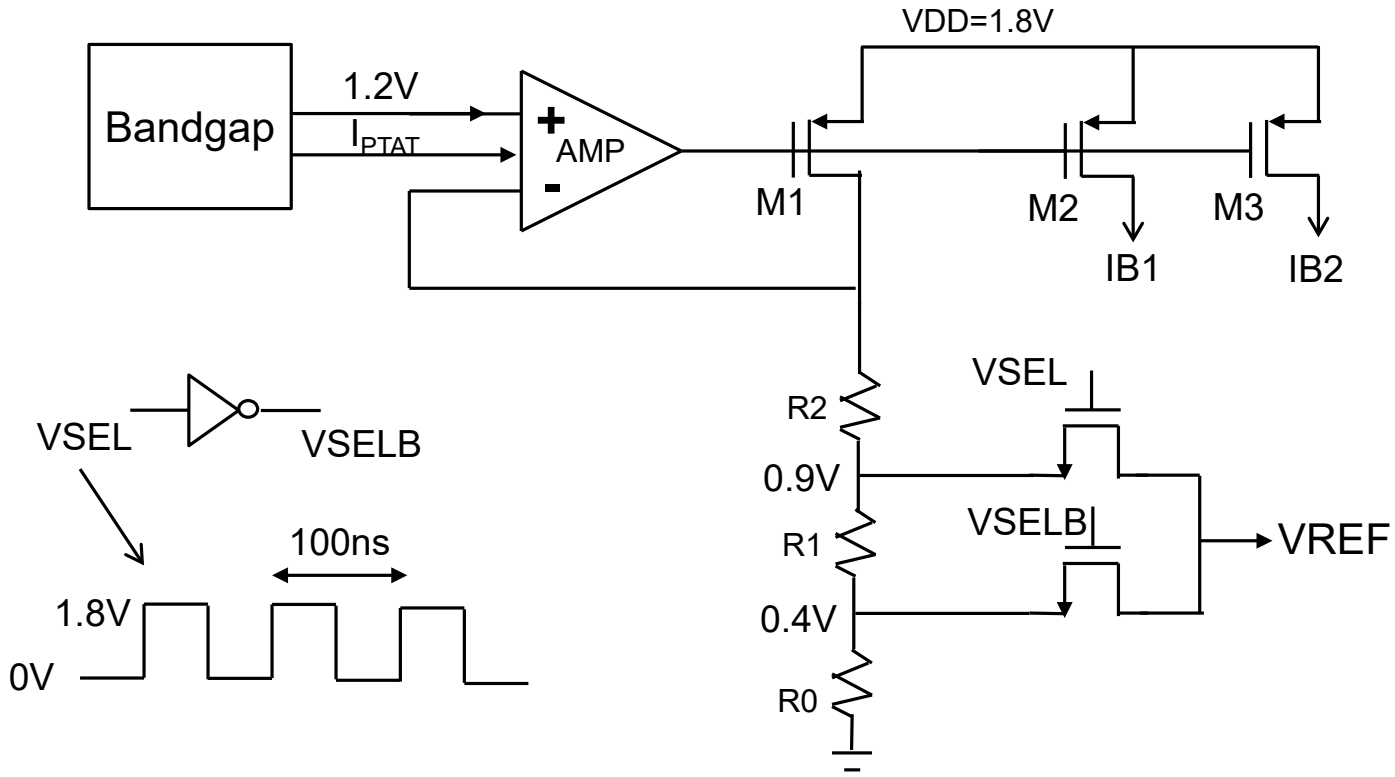
Final Vout, the bandgap voltage output, should be around 1.2V.

Choose R2 to compensate temperature variation of the bandgap voltage.

Example Folded-Cascode Amplifier Circuit



Reference Generator



Design Points

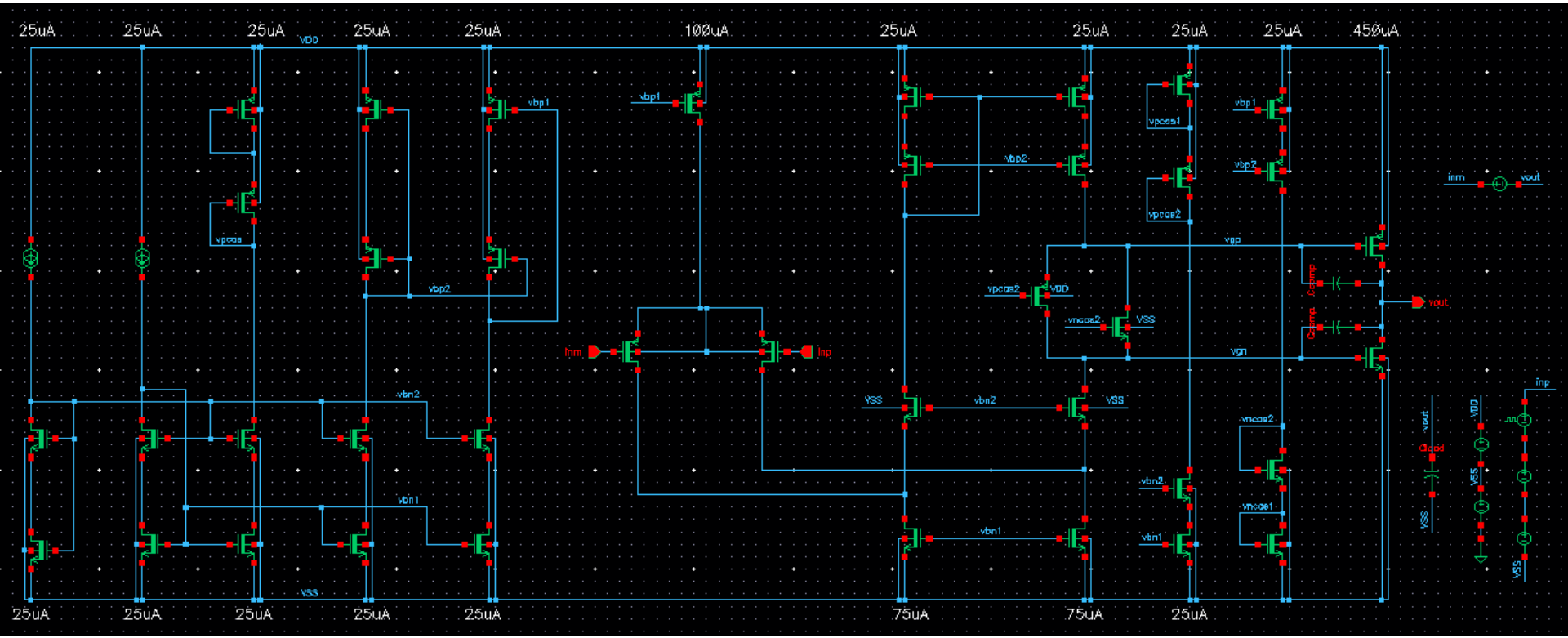
1. AMP and M1 will constitute a 2-stage RC compensated OPAMP.
2. AMP needs to be stable in unity gain configuration.
3. VREF is the input voltage to the main OPAMP.
4. VSEL is the input pulse you have to apply to measure the output of the main OPAMP.
5. IB1 and IB2 will supply the currents required in the Main Amplifier.

Main OPAMP Spec

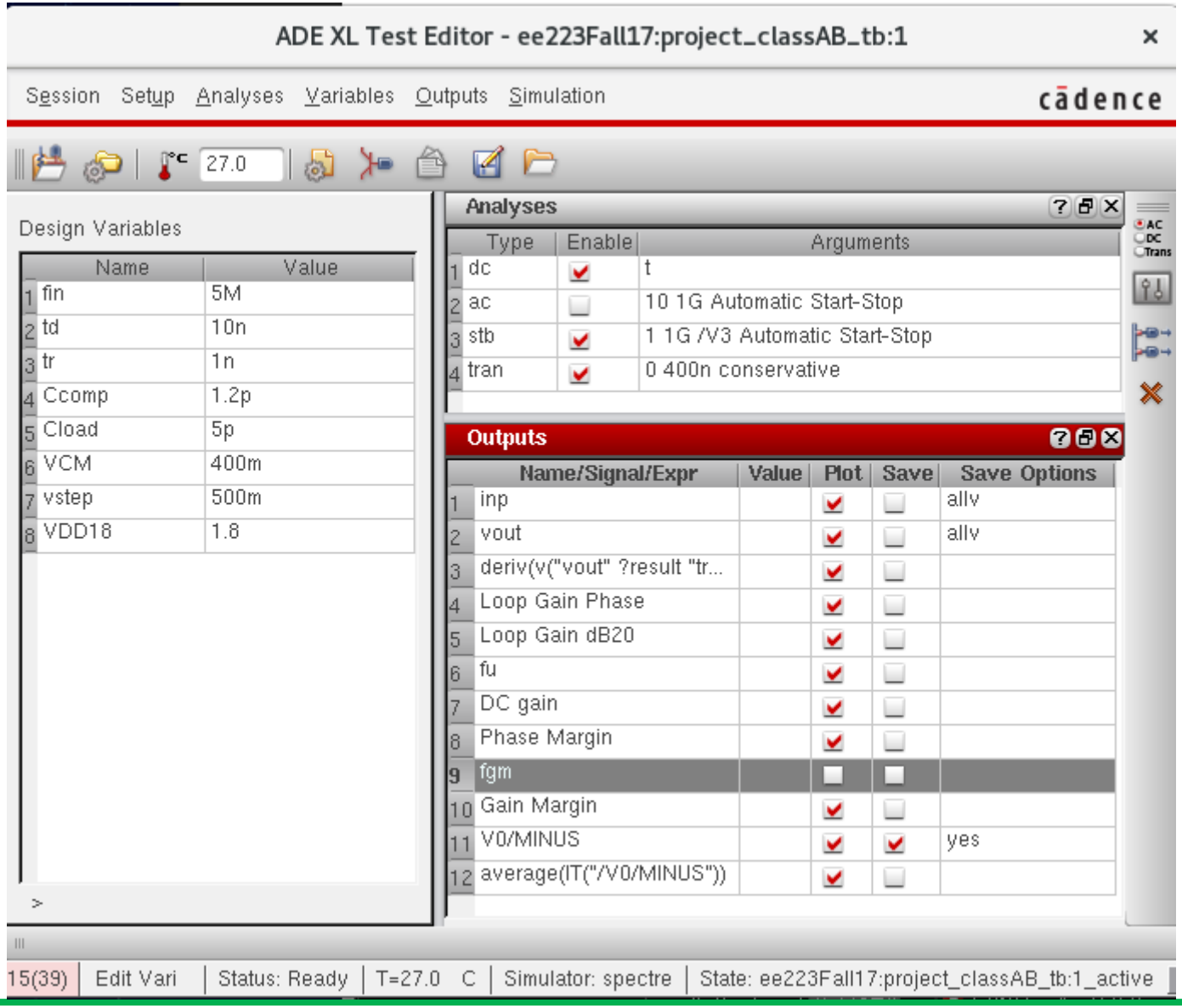
Parameter	Typical Result	PVT Result
DC Gain	80 dB	> 70 dB
Unity Gain Frequency	30 MHz	> 25 MHz
Phase Margin	60 Degree	> 55 Degree
Gain Margin	12 dB	> 9 dB
Slew Rate	15 V/us	> 10 V/us
Power	1.5 mW	< 2 mW

- Loading cap = 2 pF
- For Transient simulation, apply 10MHz input pulse at VSEL and run for 400 ns.

Example Main OPAMP



ADE Test Editor for Main OPAMP



ADE output parameters of previous slide

- fu
  - To get the unity gain frequency expression in ADE
  - Run stb analysis and plot the Loop Gain and Phase
  - In the plot window, choose Loop Gain dB20 and send it to Calculator → See next page Figure (a)
  - In Calculator, take “cross” of the Loop Gain dB20 → See next page Figure (b)
  - Send buffer expression to ADE → See next page Figure (c)

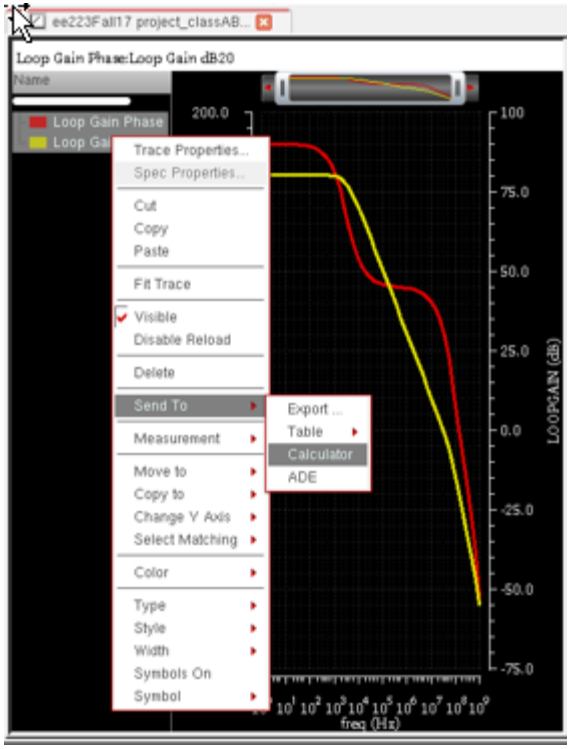
- DC gain
  - To get the DC gain in ADE
  - Send Loop Gain dB20 to Calculator
  - In Calculator, take “value” at 10 Hz of the Loop Gain 20dB → See Figure on page 12
  - Send buffer expression to ADE

- Phase Margin
  - To get Phase Margin in ADE,
  - Send Loop Gain Phase to Calculator
  - In Calculator, take “value” at fu of the Loop Gain Phase
  - Send buffer expression to ADE

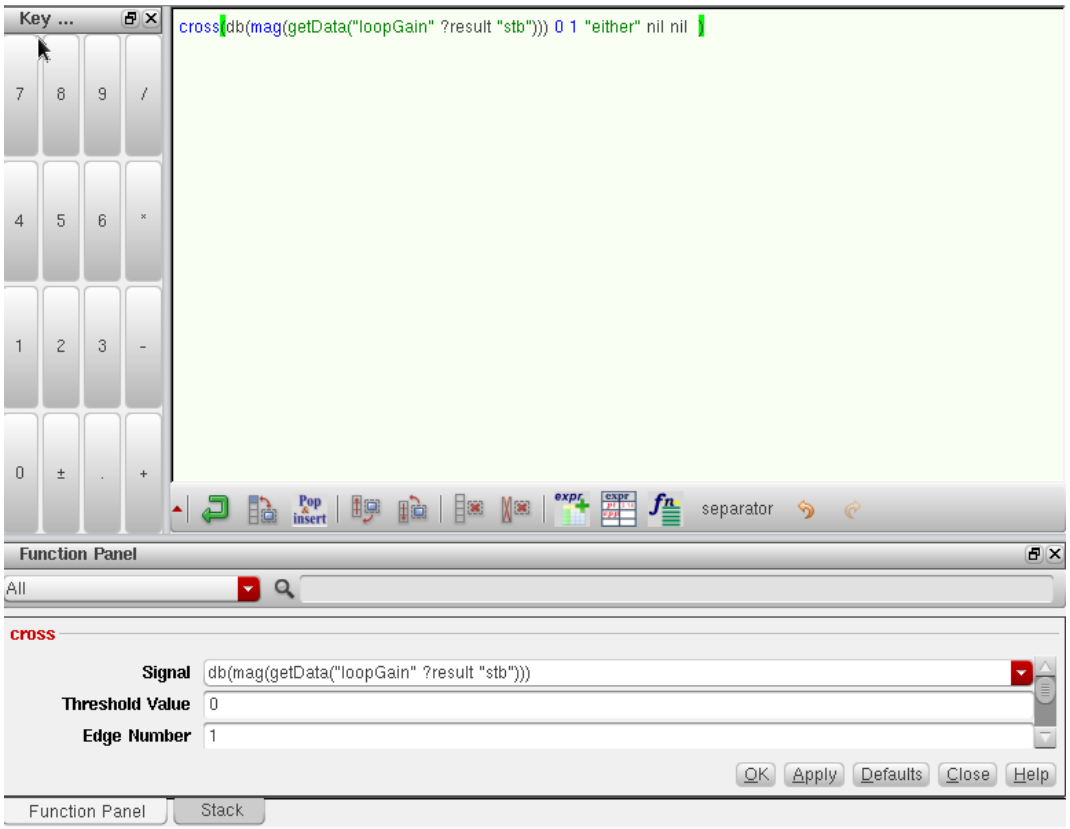
- Gain Margin
  - To get Gain Margin in ADE,
  - Send Loop Gain Phase to Calculator
  - In Calculator, take “cross” of the Loop Gain Phase
  - Send buffer expression to ADE and name it as fgm
  - Then, send Loop Gain dB20 to Calculator
  - In Calculator, take “value” at fgm of the Loop Gain 20dB
  - Send buffer expression to ADE

ADE output parameter for fu

(a)

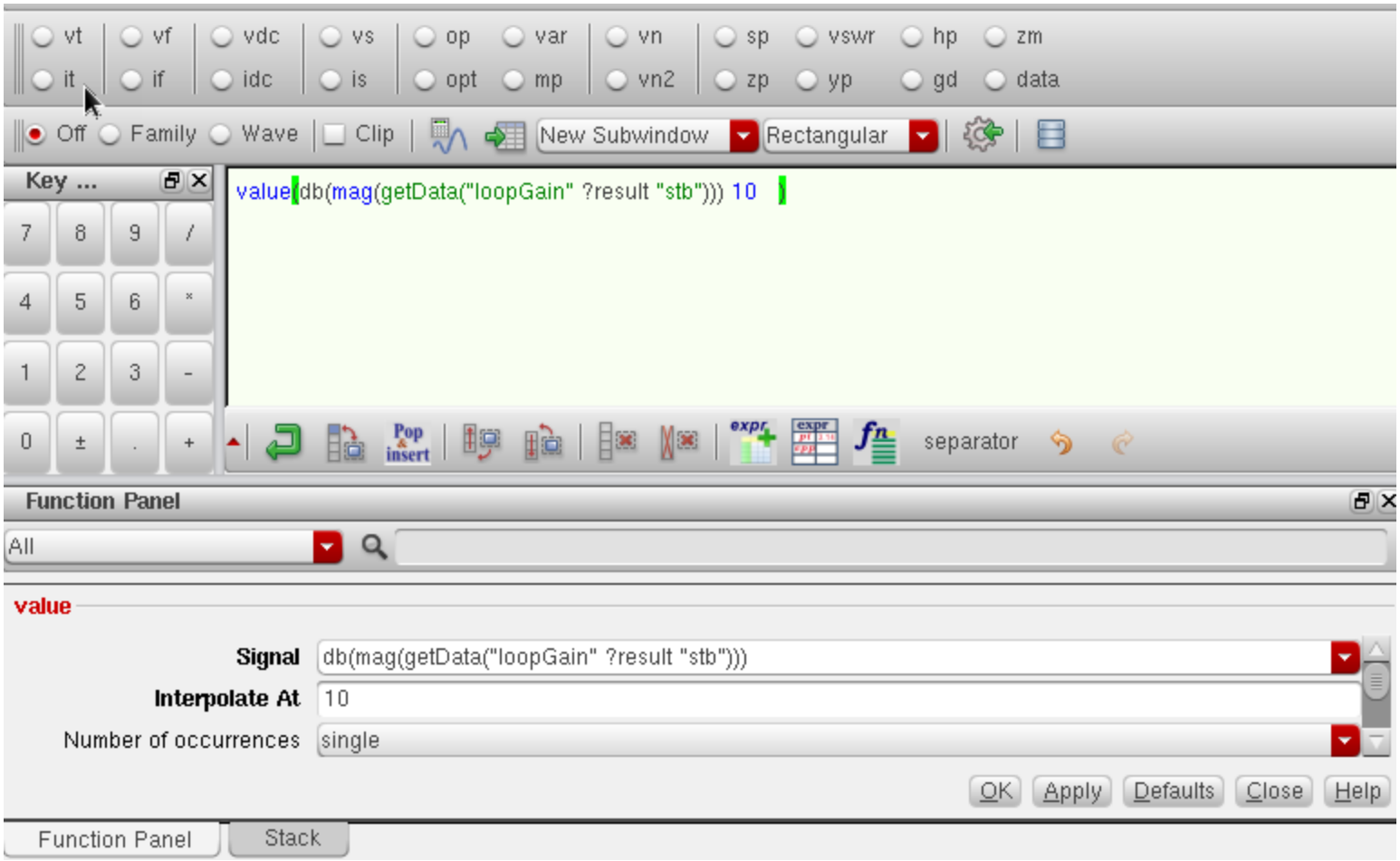


(b)



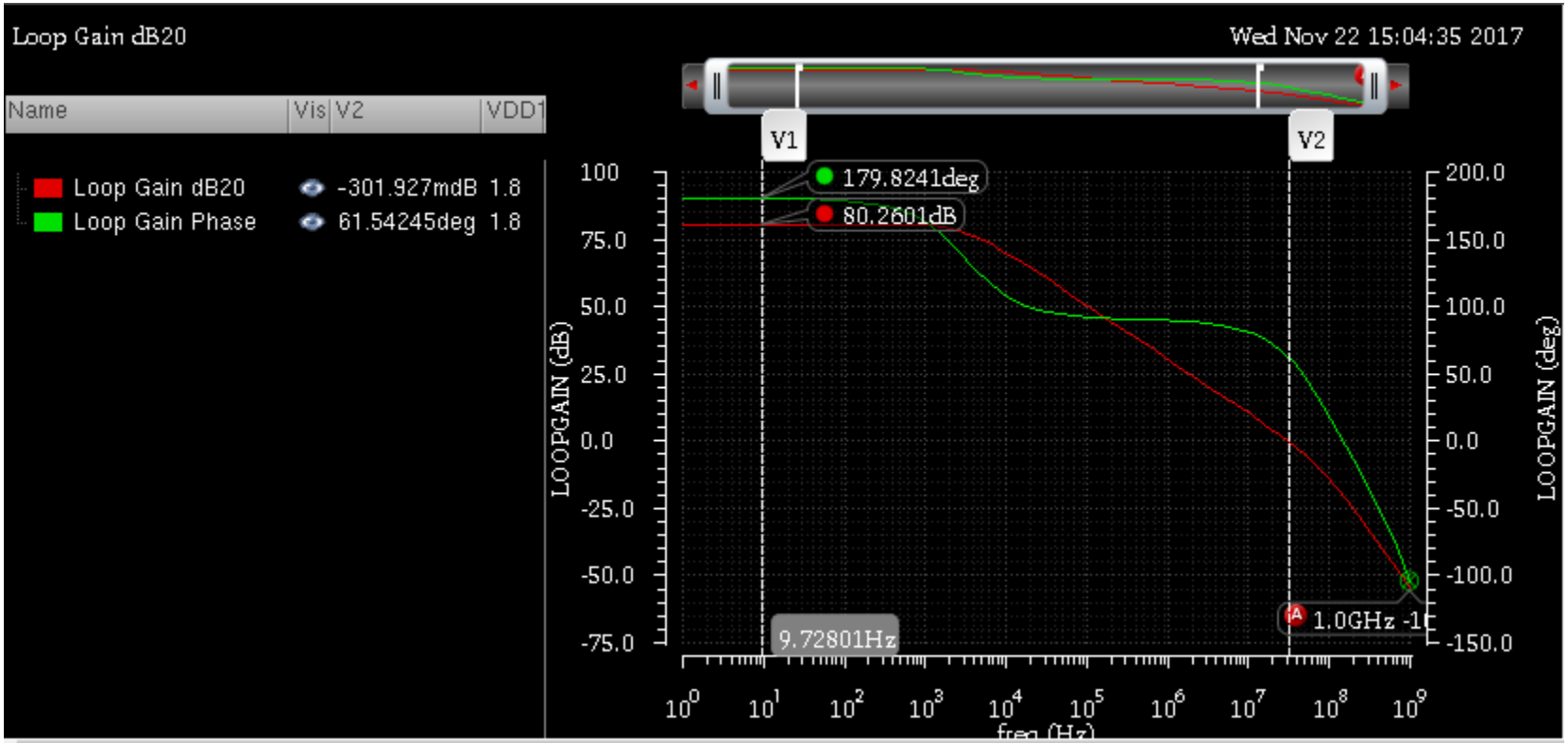
(c)

ADE output parameter for DC Gain



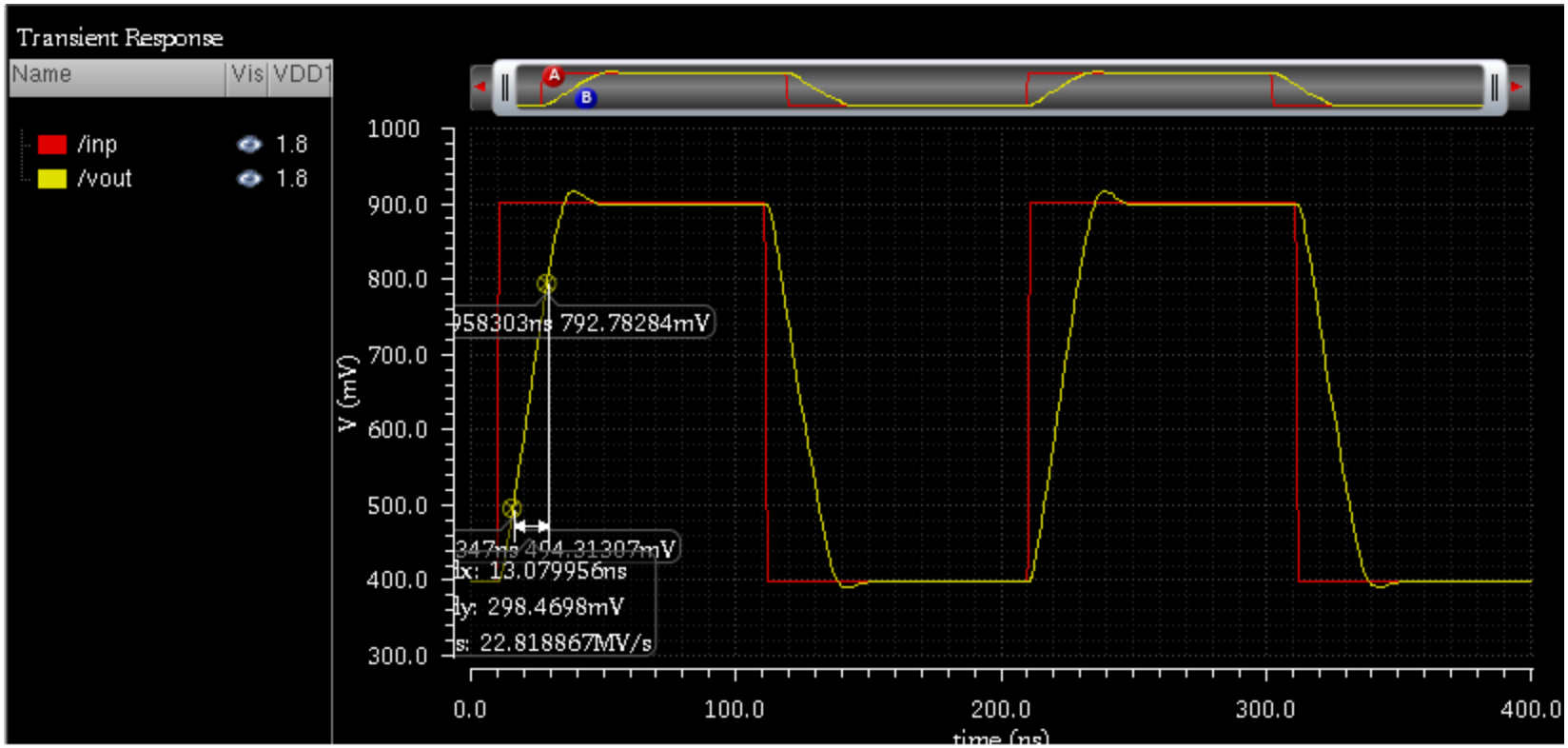
Typical Result for Main OPAMP

stb analysis



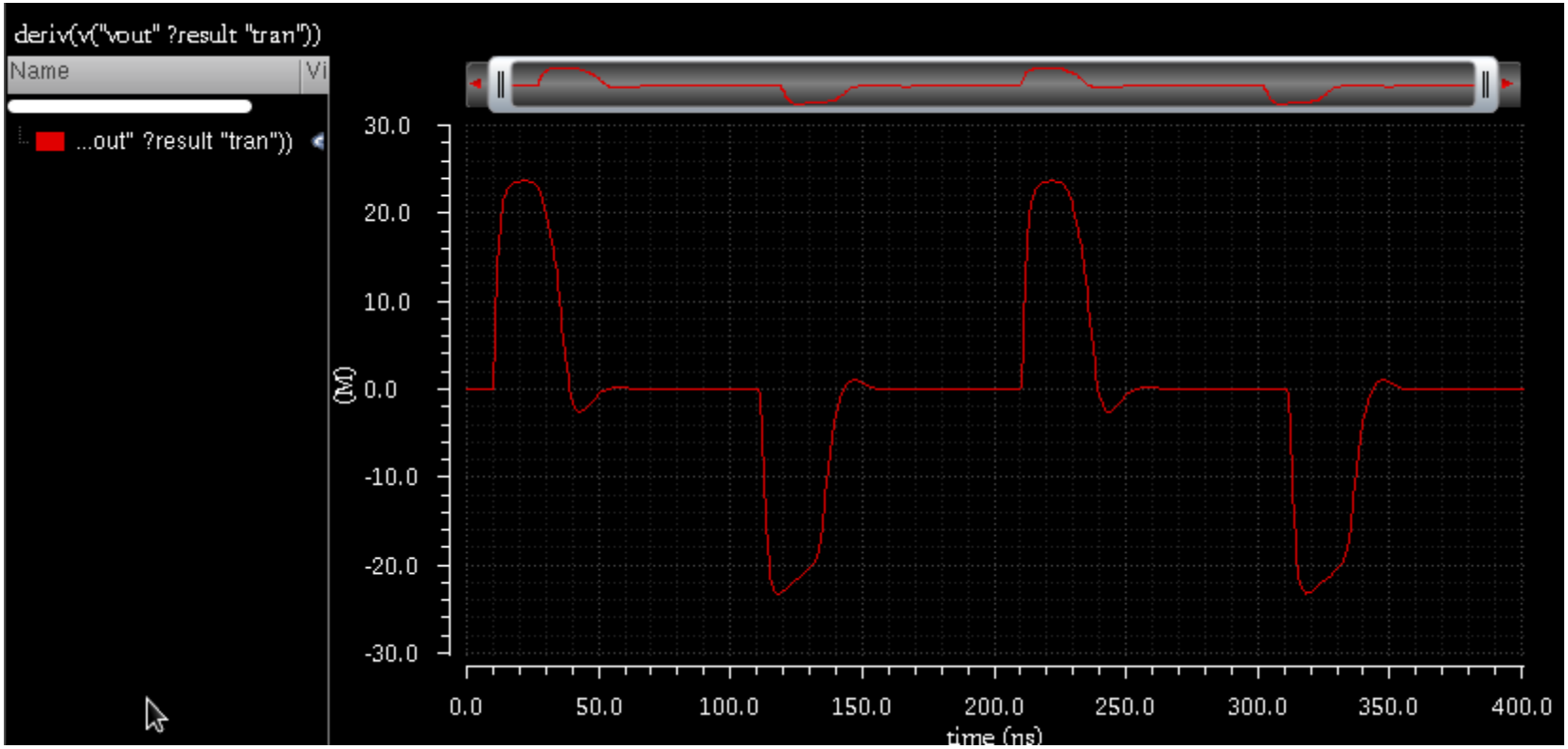
Typical Result for Main OPAMP

Transient analysis- Input waveform will be different this time.
You will have to apply a 1.8V pulse at VSEL node. – See the description on page 6.

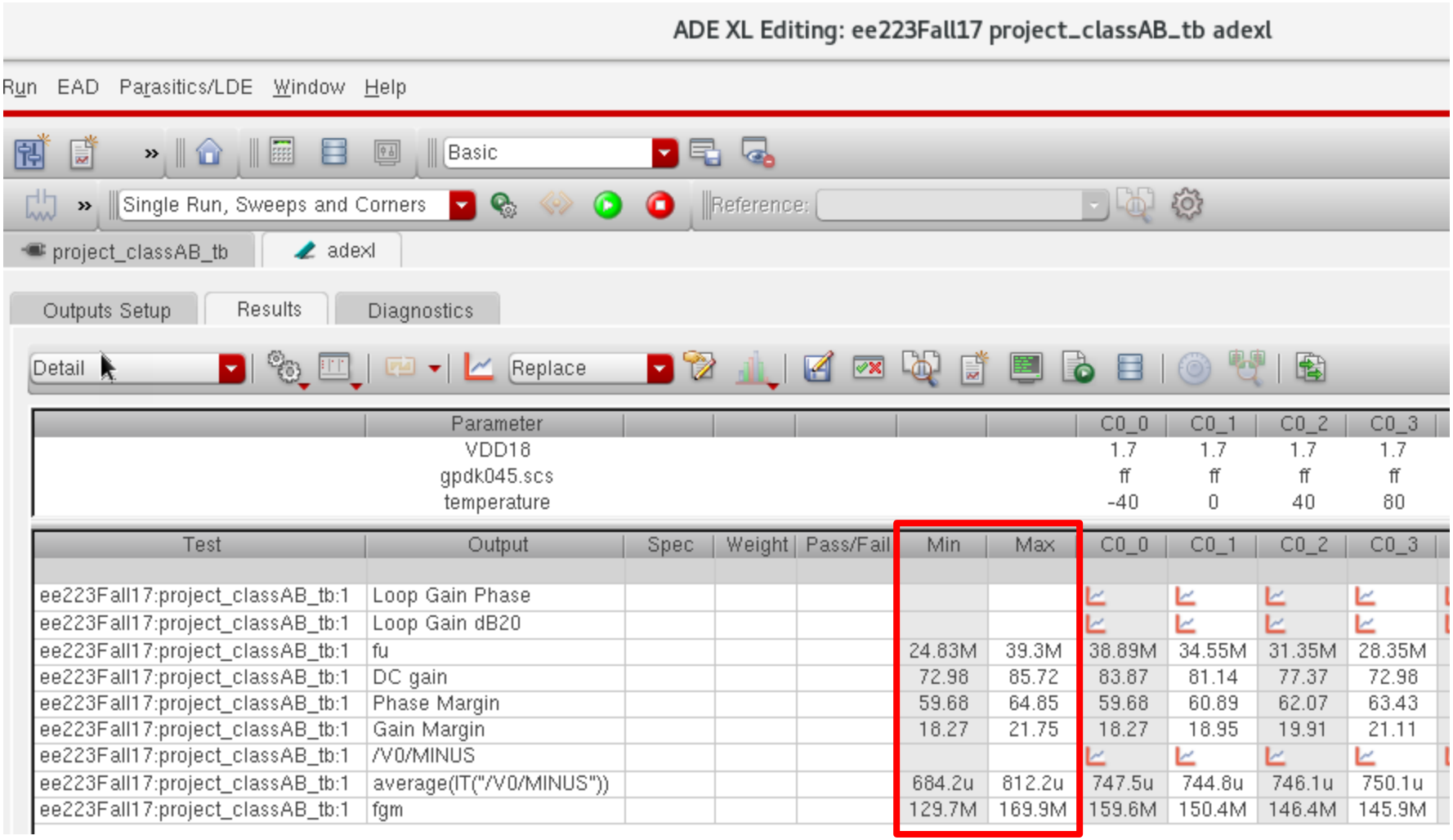


Typical Result for Main OPAMP

Slew rate by taking “deriv” of the output signal in Cadence Calculator



PVT Simulation Result for Main OPAMP using ADE-XL



Parameter						C0_0	C0_1	C0_2	C0_3
VDD18						1.7	1.7	1.7	1.7
gpdk045.scs						ff	ff	ff	ff
temperature						-40	0	40	80

Test	Output	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2	C0_3
ee223Fall17:project_classAB_tb:1	Loop Gain Phase									
ee223Fall17:project_classAB_tb:1	Loop Gain dB20									
ee223Fall17:project_classAB_tb:1	fu				24.83M	39.3M	38.89M	34.55M	31.35M	28.35M
ee223Fall17:project_classAB_tb:1	DC gain				72.98	85.72	83.87	81.14	77.37	72.98
ee223Fall17:project_classAB_tb:1	Phase Margin				59.68	64.85	59.68	60.89	62.07	63.43
ee223Fall17:project_classAB_tb:1	Gain Margin				18.27	21.75	18.27	18.95	19.91	21.11
ee223Fall17:project_classAB_tb:1	/V0/MINUS									
ee223Fall17:project_classAB_tb:1	average(IT("/V0/MINUS"))				684.2u	812.2u	747.5u	744.8u	746.1u	750.1u
ee223Fall17:project_classAB_tb:1	fgm				129.7M	169.9M	159.6M	150.4M	146.4M	145.9M

PVT conditions : TT, SS, FF, 1.7V, 1.8V, 1.9V, -40C, 0C, 40C, 80C – Total 36 corners

References

- Bandgap
  - Chapter 11 of the Textbook
  - H. Banba, et al. “A CMOS Bandgap Reference Circuit with Sub-1-V Operation,” *IEEE Journal of Solid-State Circuits*, Vol. 34, no. 5, pp. 670–674, May 1999

- RefGen
  - Ian Wheeler, *MS Thesis, California State University, Sacramento*, A fast settling reference generator with signal-dependent charge cancellation for an 8-bit 1.5 bit/stage pipeline ADC, 2013

- OPAMP
  - K. Langen and J. Huijsing, “Compact low-voltage power-efficient operational amplifier cells for VLSI,” *IEEE Journal of Solid-State Circuits*, Vol. 33, no. 10, pp. 1482–1496, Oct 1998