SRAM Cell, Noise Margin, and Noise

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Courtesy of MAH and BAW

Overview

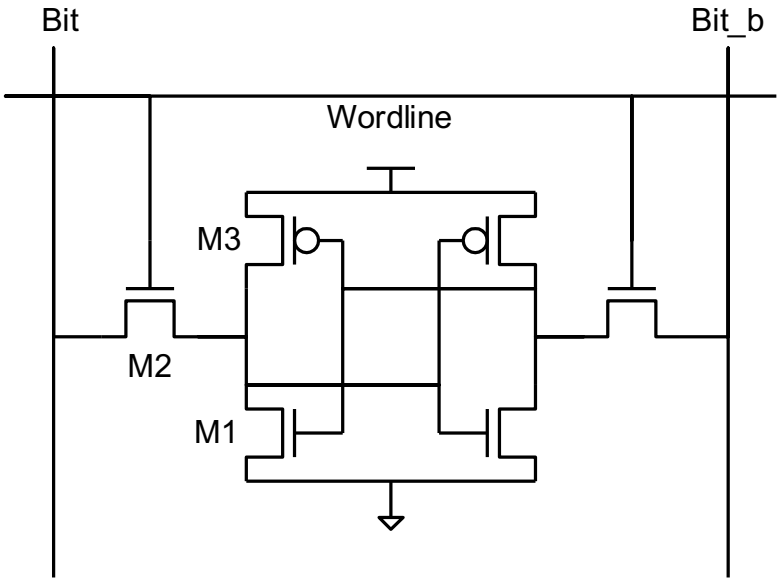
- **Reading**
  - Rabaey 5.3
  - W&H 2.5
- **Background**
  - Reading a memory cell can disturb its value. In addition, if small bitline swings are used, great care must be taken to ensure that the sense amplifier detects the correct value. To understand why the cell can loose its value, or a sense amplifier can detect the wrong value, we need to take a closer look at what we mean when we talk about digital gates – what assumptions do we make about these gates. To do this, we need to examine the voltage transfer functions of our gates, and check to make sure they obey the 'right' properties. They need to have a high gain region and low gain regions to 'restore' the digital signal.
  - Next we will look at sources of noise and how these noise sources affect our digital gates. A gates immunity to noise is called its noise margin, and we will look at this in more detail in the following lecture.

SRAM Cell

- We need to be able to read and write a memory cell
- Read
  - Transfer the value of the cell onto the bit lines
  - Do this without changing the value of the cell
- Write
  - Change the value of the bit cell
- Since there is only one control signal, how does this work?
  - It is all done with the bitline levels

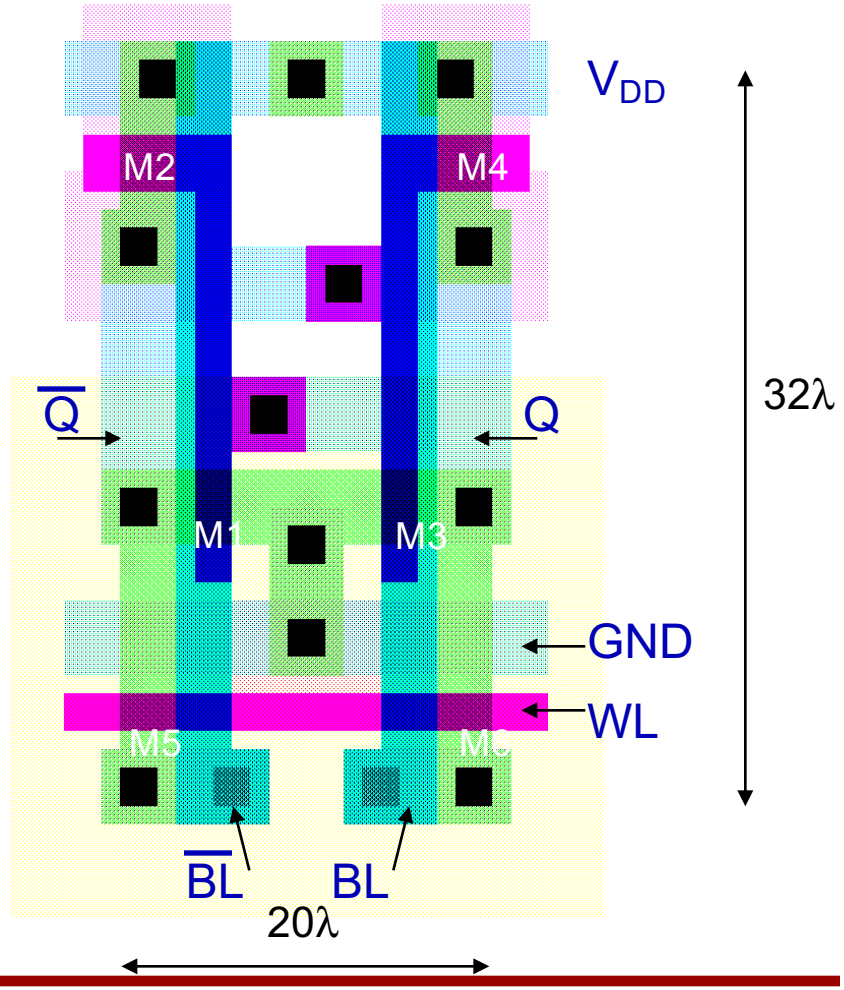
6T SRAM Cell

- Only one control terminal
- Read
  - Both bit lines start at Vdd
  - Cell pulls one down
- Write
  - One bit line is pulled low
  - Low bit line value overpowers cell
- This is a ratio circuit
  - M2 must overpower M3, but not M1
  - Interesting design problem (later)



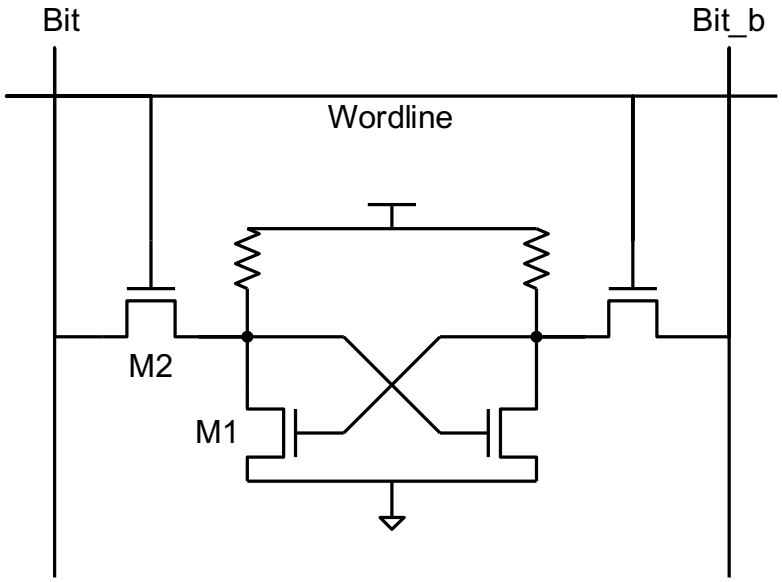
6T-SRAM Layout

- Capacitances on the storage nodes are small
  - Susceptible to noise coupling and soft errors.
- Notes
  - M2 is vertical
  - WL is in poly
    - Can strap in metal (M1 or M3) with additional contact.
  - Q and Q' will couple to BL and BL'
    - But it couples to both so differential noise is partially compensated.
  - Q node has large diffusion area.
- Dedicated SRAM processes can make cells half the area.



Memory Cell Stability

- If a cell is not sized correctly, it can lose its value during a read
  - Was a serious problem with poly load 4T cells
    - Removed pMOS devices, use very high value resistors
      - Power problem otherwise.
    - R = 10Gohms
    - See this later in this lecture
- Why did the cell lose its value?
  - How to size the cell?
  - Is there some science?



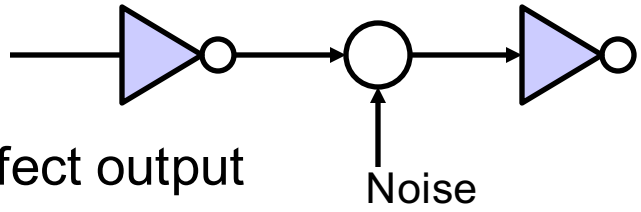
- Think of this as Noise/Noise Margin issue.

Noise Margins and VTC

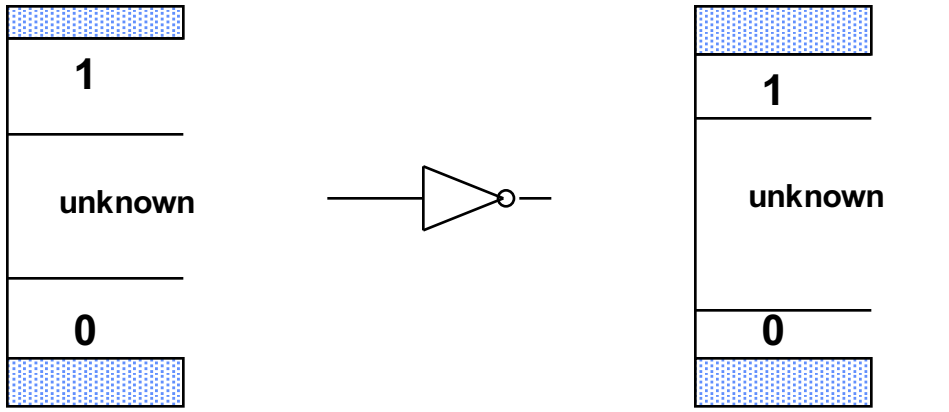
Noise and The Digital Abstraction

- Signals are represented by voltages
  - Voltages are not fundamentally quantized
  - Signals will have noise

All this means is that the signals are not all going to have the same values



- In digital systems, noise should not affect output
- Divide voltage range into regions: 0, X, 1



Input range

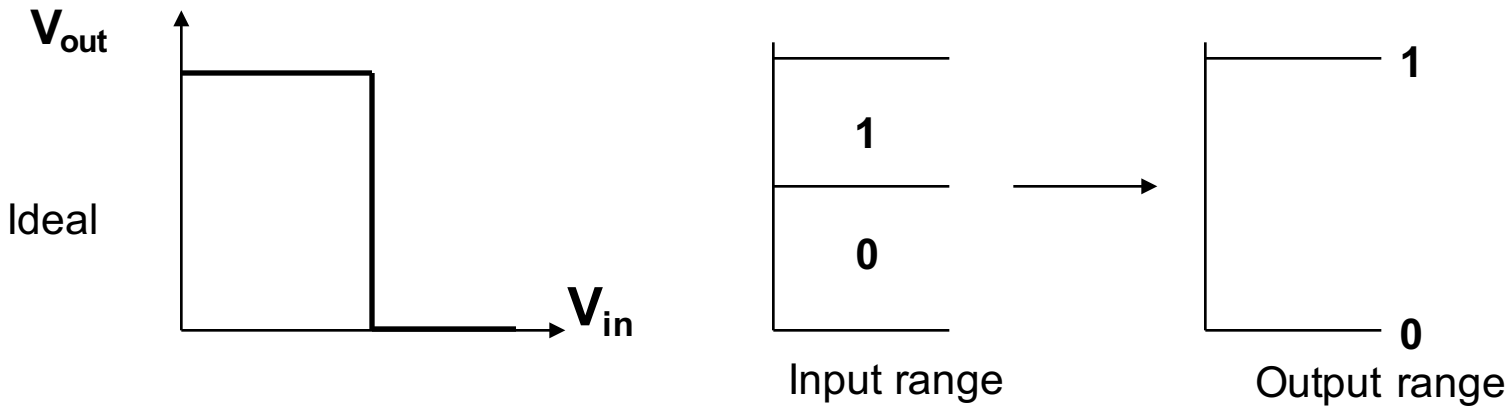
Output range

Digital Gates

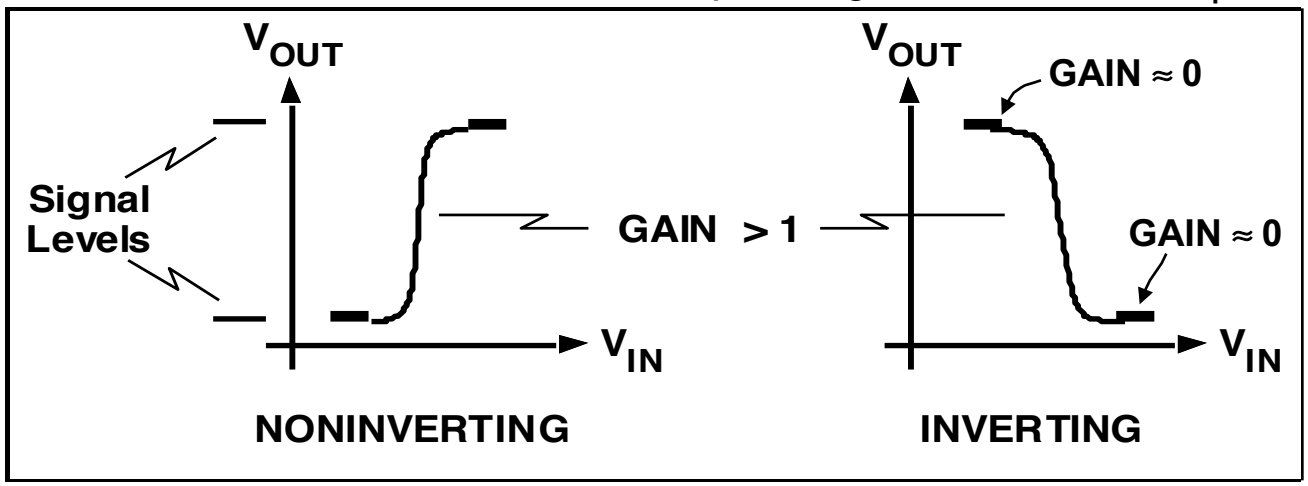
- All digital gates need to map input voltages to an output voltage
  - V_{IH}, V_{IL} for input, and V_{OH}, V_{OL} for output
    - Often VDD or Gnd.
    - Generally the range allows you to cascade gates
  - In prior lectures, we haven't been too concerned about the voltage
    - Concern was mostly about the amount of current available to drive the load capacitance, and how to size this current
- What happens to voltages between Vdd and Gnd?
  - Want to attenuate any noise
  - $V_{IL} < V_{IN} < V_{IH}$ still results in V_{OH} or V_{OL} at the output.

Voltage Transfer Characteristics

- DC plot of V_{out} vs. V_{in}

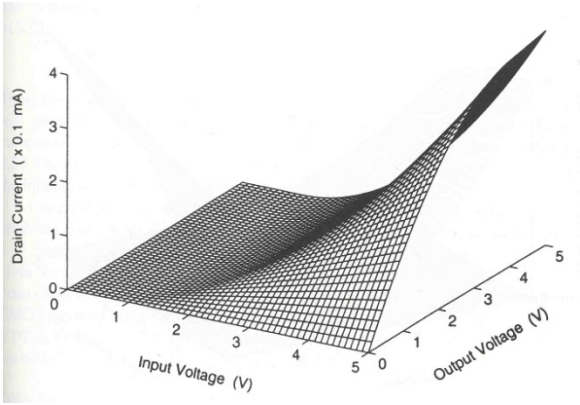


Actual

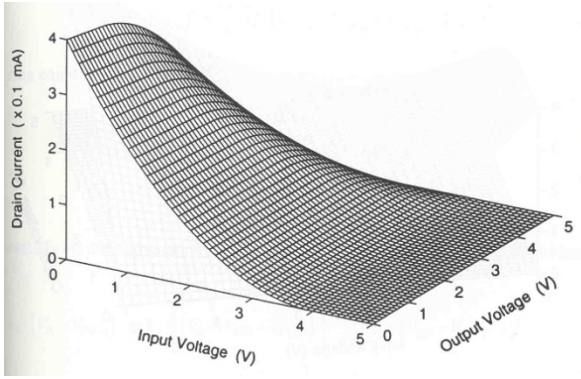


For gain to be small at the ends, it must be greater than 1 in the middle of the transfer function

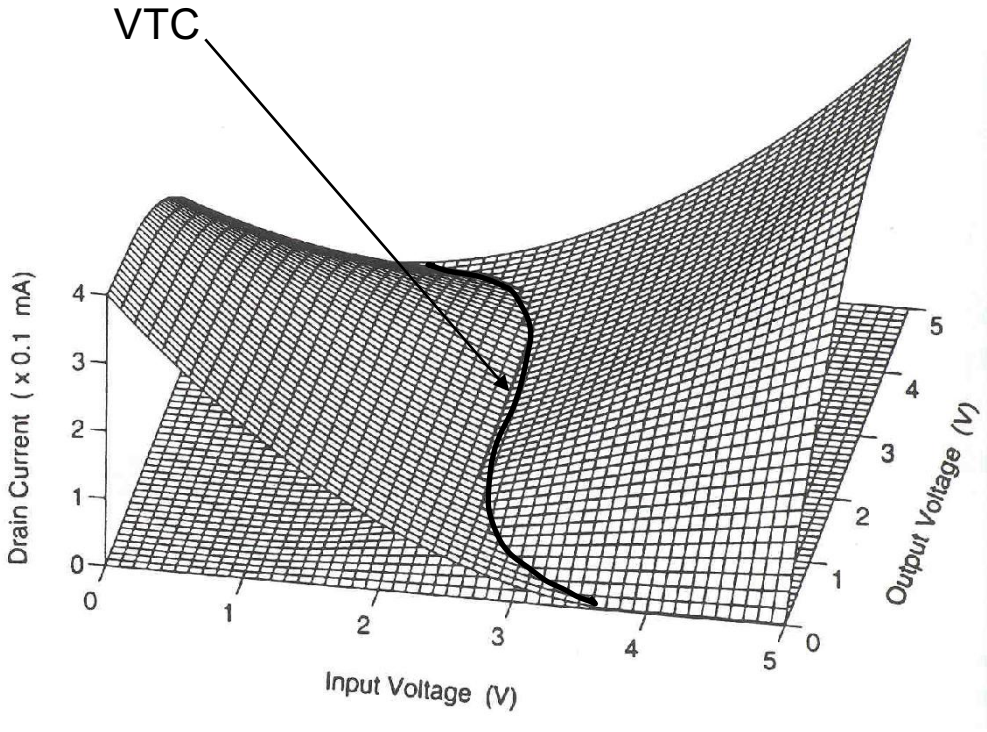
CMOS I-V Surface Plots



NMOS IV surface



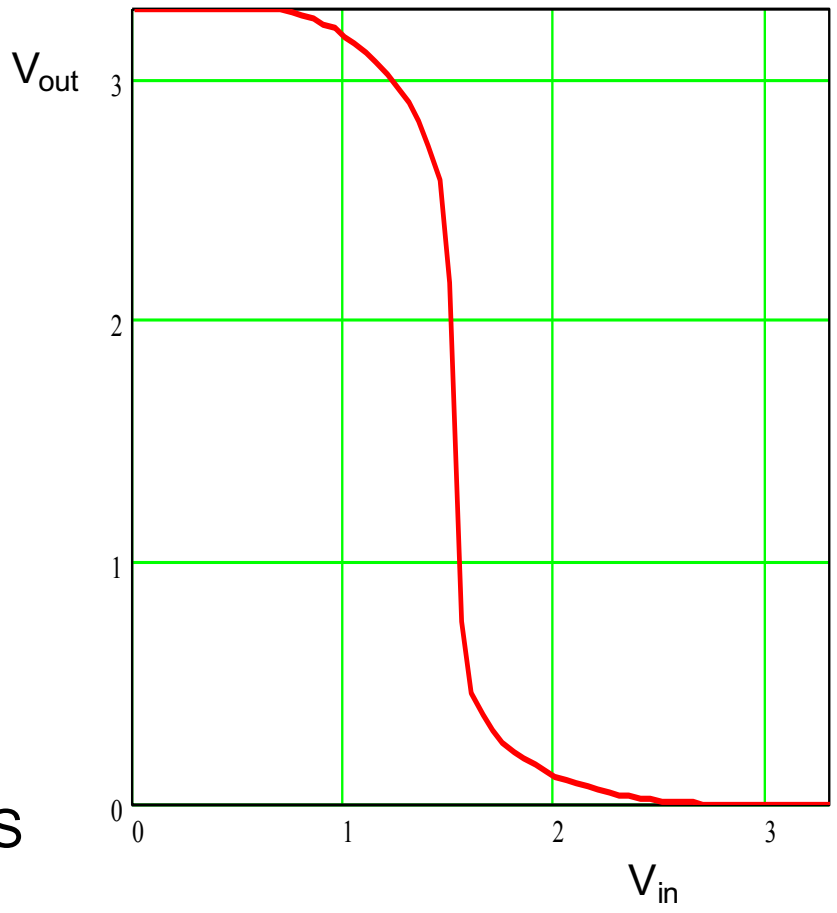
PMOS IV surface



Intersection of IV surfaces of NMOS + PMOS devices

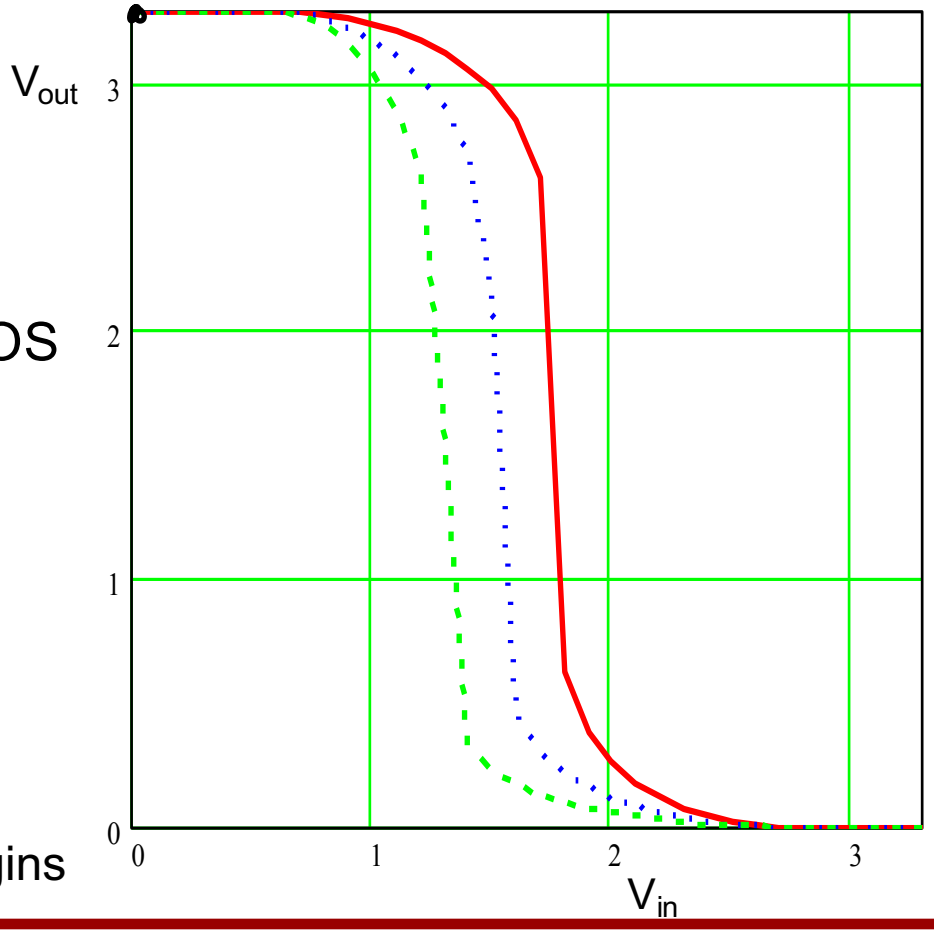
CMOS Inverter's Transfer Function

- Looks pretty ideal
  - Flat near Vdd, Gnd
    - Either pMOS, or nMOS off
  - High gain in middle
    - Both transistors saturated
    - Not vertical because of output resistance of transistors
  - Rounded on top and bottom
    - One transistor linear, the other is saturated in this region
- Switching point depends on nMOS to pMOS size ratio
  - This is for a 2-1 pMOS to nMOS
- Derivation is appended at the end.



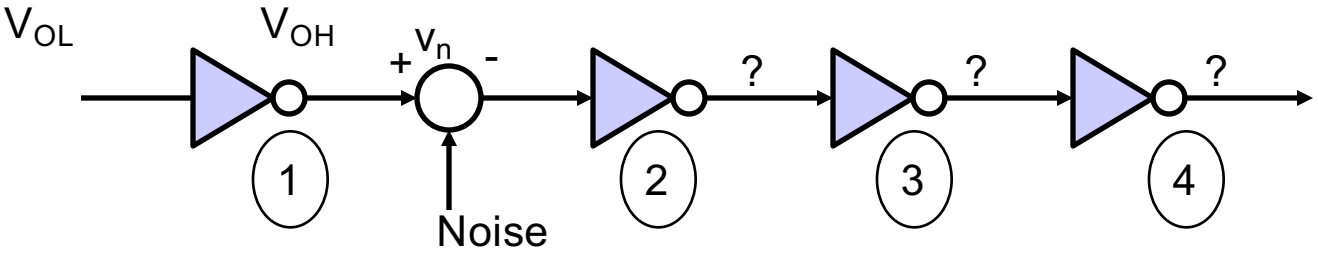
Transfer Function

- Plot shows three curves
  - pMOS 4x, 2x 1x
  - Red solid 4x
  - Green dash 1x
- High gain region
  - V_{in} where nMOS and pMOS current balance
- Main point:
  - Large flat regions
  - Tolerate lots of noise
  - Symmetric curve
    - Good high and low margins



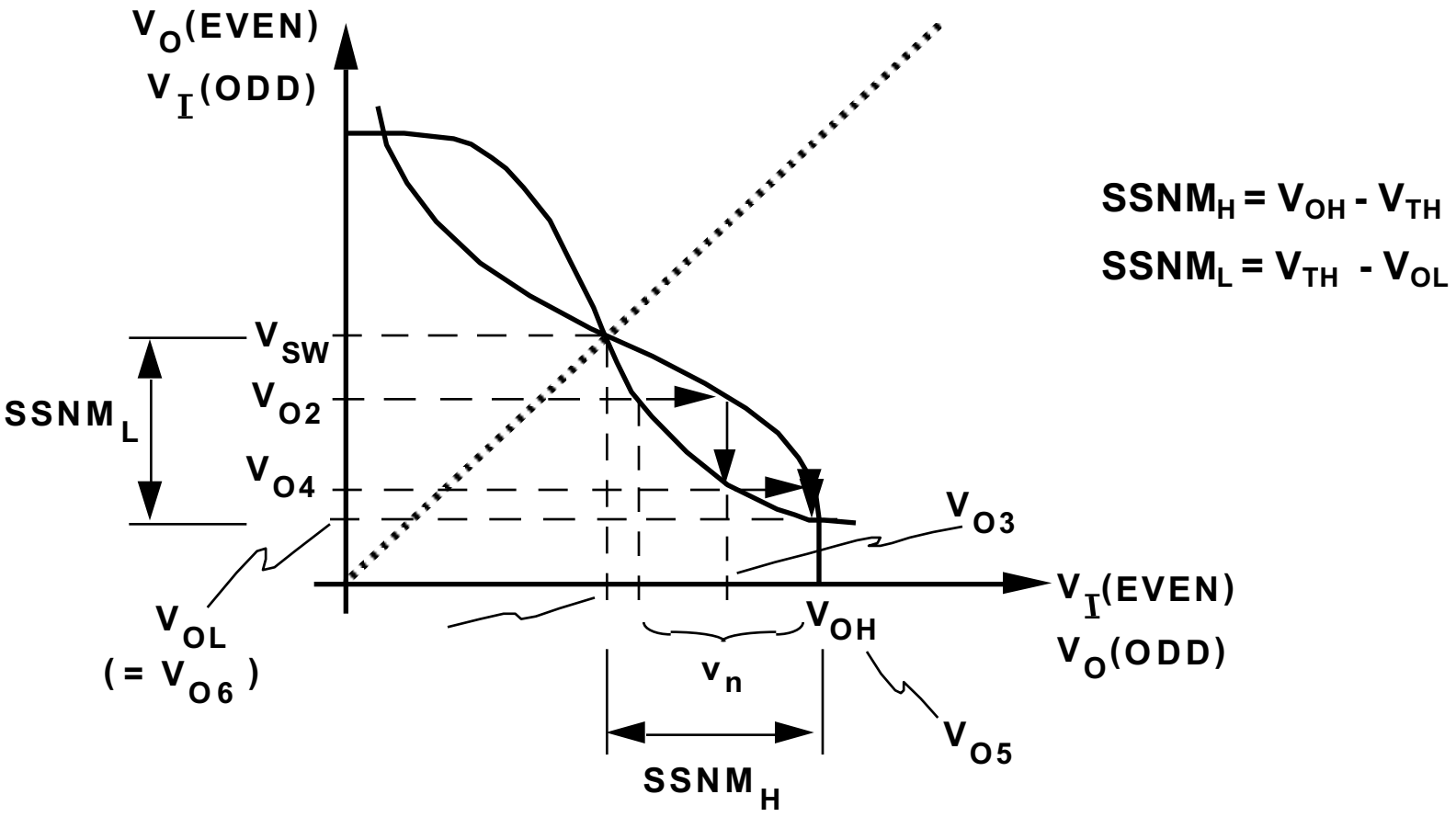
Single Stage Noise Margins

- Simplest type of noise margin is the single-stage noise margin
- Defined as maximum noise, v_n, in a single stage that still allows subsequent stages to recover to the right value (regenerative property)

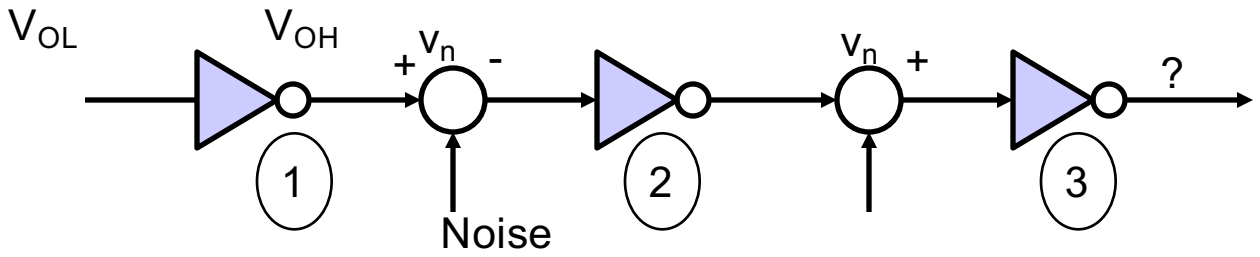


- In the above circuit $V_{i2} = V_{o1} - v_n = V_{OH} - v_n$
- For noise added to a high level input, the correct levels will be maintained if $V_{OH} - v_n > V_{sw}$ (point where $V_{in} = V_o$)
- For noise added to a low level input, correct levels will be maintained if $V_{OL} + v_n < V_{sw}$

Single Stage Noise Margins



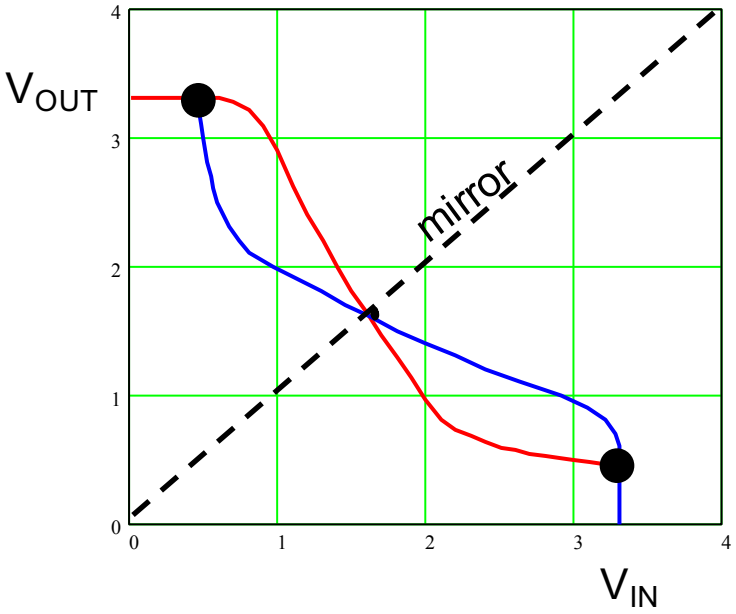
Multiple Noise Sources

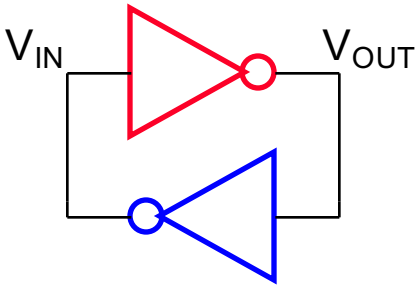


- What happens if there are more then one noise source?
  - Many ways to look at this problem
  - Most conservative method finds max noise possible at EVERY gate and still have the system work

Alternate View of Multi-stage Noise

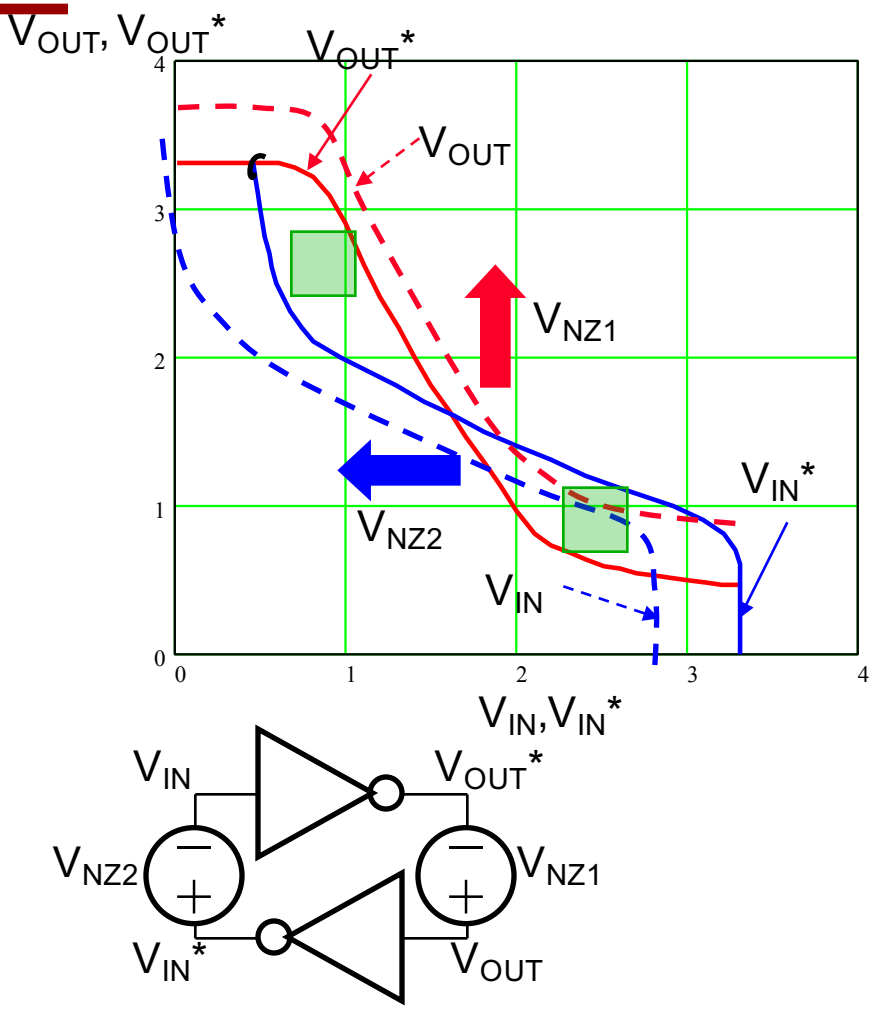
- The chain is the same as two cross connected inverters!
  - Draw the VTC on the same plot.
    - Mirror along the unity axis.
  - 2 stable points
    - Stable logic values of 0 and 1 as a signal propagates down the chain.
- How to find the tolerable noise?
  - Ideally, it is the maximum shift in VTC that still maintains stable binary values.
  - Classical analytical approach is the unity-gain noise margin
    - Unity-gain point on the curves
    - Conceptually, these points are when noise has gain > 1 and is no longer suppressed.





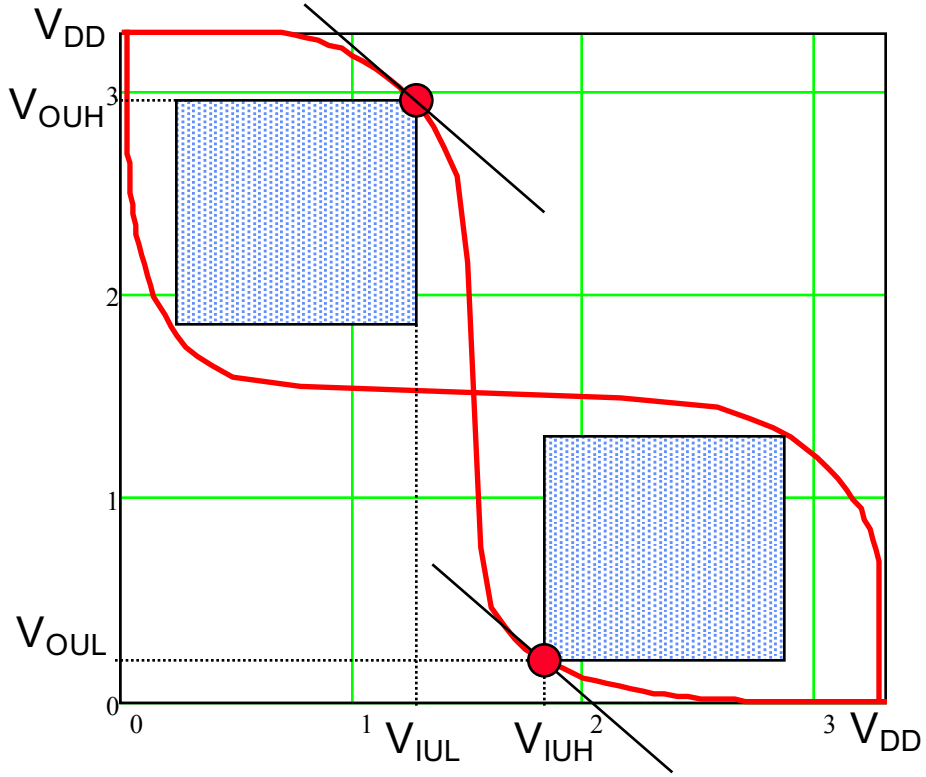
Multi-Stage Noise Margin

- A.K.A. Static Noise Margin
- Noise is essentially a shift in the voltage.
  - A shift of all even stages (V_{IN} +ve shift right).
  - And a shift of all odd stages (V_{OUT} –ve shift).
- Maximum tolerable magnitude of noise
  - Largest shift (in both directions) that still results in intersecting VTC.
  - Essentially, it's the largest SQUARE we can fit inside the VTC.



Unity Gain Noise Margins

- An estimate of the size of the largest box.
  - Works well for symmetric VTCs.
  - Good for static CMOS logic.



$UGM_H = V_{OUH} - V_{IUH}$

$UGM_L = V_{IUL} - V_{OUL}$

Note:

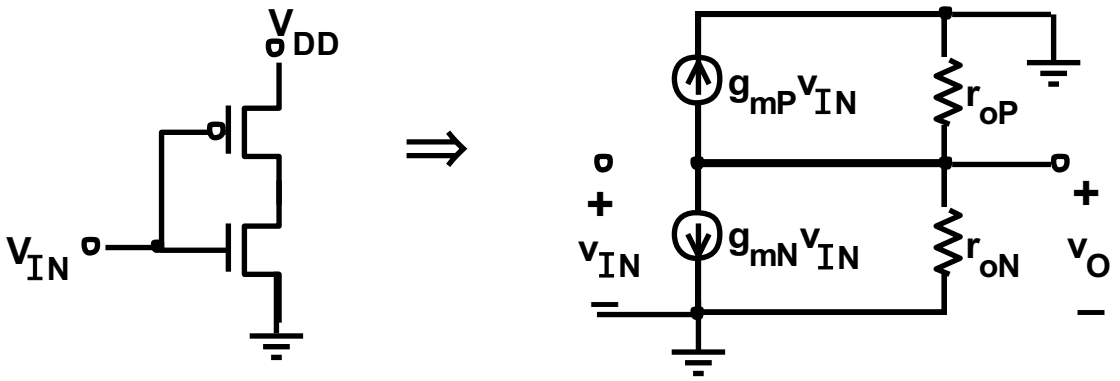
V_{IUL} **is the same as** V_{IL}

V_{IUH} **is the same as** V_{IH}

Gain Calculations

- Like voltage transfer functions unity gain points are complex to calculate
  - Have methods of calculation in the notes, but not critical
- Key point is to use small-signal methods

Gain Calculation



where $g_{mN} = \frac{\partial I_{DN}}{\partial V_{GS}}$

$g_{mP} = \frac{\partial I_{DP}}{\partial V_{GS}}$

$\frac{1}{r_{oN}} = \frac{\partial I_{DN}}{\partial V_{DS}}$

$\frac{1}{r_{oP}} = \frac{\partial I_{DP}}{\partial V_{DS}}$

Then $A_v = \frac{V_o}{V_{in}} = -(g_{mN} + g_{mP})\, r_{oP} || r_{oN} = -(g_{mN} + g_{mP})/(g_{ON} + g_{OP})$

Derivation of Noise Equations

So which equations should we use for the derivation?

Our equations incorporating velocity saturation are:

(for $V_{ds} < V_{dsat}$: linear)

$$I_{Dlin} = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1+\frac{V_{ds}}{E_c L}\right)} \left(V_{gs} - V_{TN} - \frac{\mathbf{V_{ds}}}{\mathbf{2}}\right)V_{ds}$$

(for $V_{ds} > V_{dsat}$: saturation)

$$I_{Dsat} = W_N \nu_{sat} C_{ox} \frac{(V_{gs} - V_{TN})^2}{(V_{gs} - V_{TN}) + E_c L_N}$$

The use of these equations directly may be too complicated when computing the partial derivatives, but we still want accurate results!

One approach: since V_{ds} is small in the first equation, we could replace the term $(1+V_{ds}/E_cL)$ with a constant to represent the degradation factor. Then, we could replace the second equation with the alpha-power law model.

$$I_{Dlin} = F_1 \left(V_{gs} - V_{TN} - \frac{\mathbf{V_{ds}}}{\mathbf{2}}\right)V_{ds}$$

$$I_{Dsat} = F_2 (V_{gs} - V_T)^{\alpha}$$

$F_1 = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1+\frac{V_{ds}}{E_c L}\right)}$ With V_{ds} set to a small value

Unity Gain Points for CMOS Inverter

Unity gain points are the two points where $A_v = -1$

Case 1: $V_{in} = V_{IL}$, $V_o = V_{OUH}$ (n-channel saturated, p-channel linear)

$g_{mN} = \alpha F_{2N} (V_{GS} - V_{TN})$ $\qquad 1/r_{oN} = 0$

$g_{mP} = F_{1P}(V_{DD} - V_o)$ $\qquad 1/r_{oP} = F_{1P} (V_o - V_{in} + V_{TP})$

At $V_{IN} = V_{IL}$,

$$A_v = - \frac{\alpha F_{2N} (V_{IL} - V_{TN}) + F_{1P}(V_{DD} - V_{OUH})}{F_{1P}(V_{OUH} - V_{IL} + V_{TP})} = -1$$

Cannot solve this unless we have one other constraint: I_{DN} (sat) = I_{DP} (lin)

$$F_{2N} (V_{gs} - V_{TN})^{\alpha} = F_{1P} (V_{gs} - V_{TN} - \frac{V_{ds}}{2})V_{ds}$$

$V_{gs} \rightarrow V_{IL}$, $V_{gs} \rightarrow V_{DD} - V_{IL}$, $V_{ds} \rightarrow V_{DD} - V_{OUH}$

Use this relationship and the gain equation above to solve for V_{IL} and V_{OUH}

Unity Gain Calculation (cont'd)

Case 2: $V_{in} = V_{IH}$, $V_o = V_{OUL}$ (n-channel linear, p-channel saturated)

$g_{mP} = \alpha F_{2P} (V_{DD} - V_{in} + V_{TP})$ $\quad 1/r_{oP} = 0$

$g_{mN} = F_{1N} V_o$ $\quad 1/r_{oN} = F_{1N} (V_{in} - V_{TN} - V_o)$

At $V_{IN} = V_{IH}$,

$$A_v = - \frac{F_{1N} V_{OUL} + \alpha F_{2P}(V_{DD} - V_{IH} + V_{TP})}{F_{1N}(V_{in} - V_{TN} - V_o)} = -1$$

Cannot solve this unless we have one other constraint: I_{DN} (lin) = I_{DP} (sat)

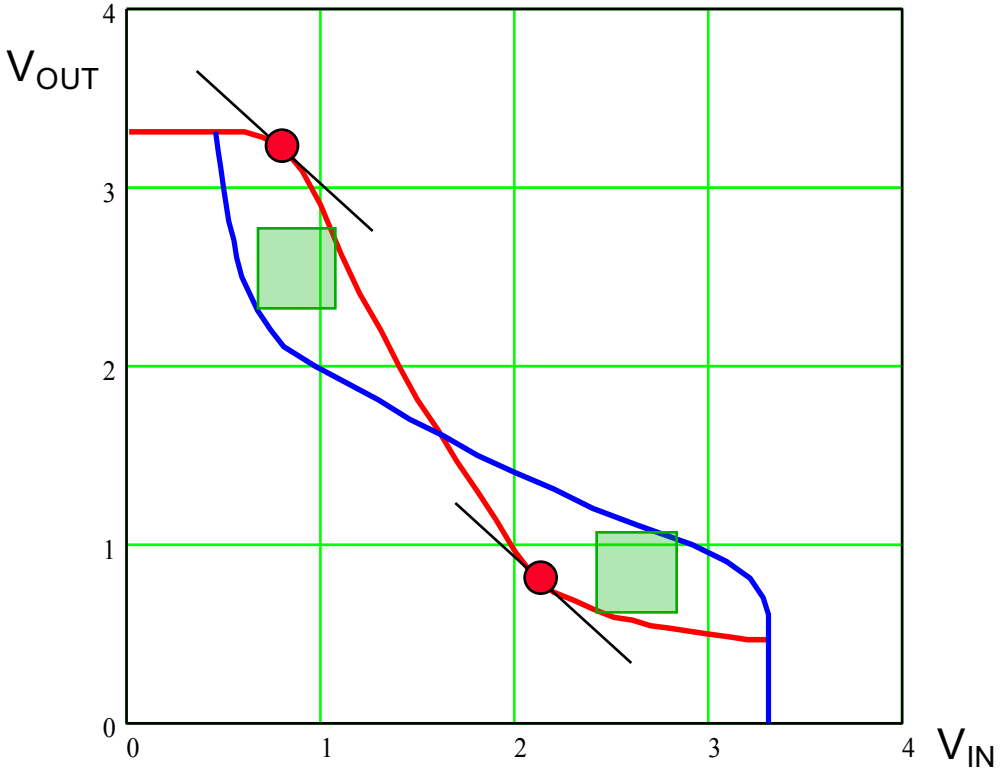
$$F_{1N} \left(V_{gs} - V_{TN} - \frac{V_{ds}}{2}\right) V_{ds} = F_{2P}(V_{gs} - V_{TN})^{\alpha}$$

$V_{gs} \rightarrow V_{IH}$, $V_{ds} \rightarrow V_{OUL}$, $V_{gs} \rightarrow V_{DD} - V_{IH}$

Use this relationship and the gain equation above to solve for V_{IH} and V_{OUL}

UGM Inaccuracy

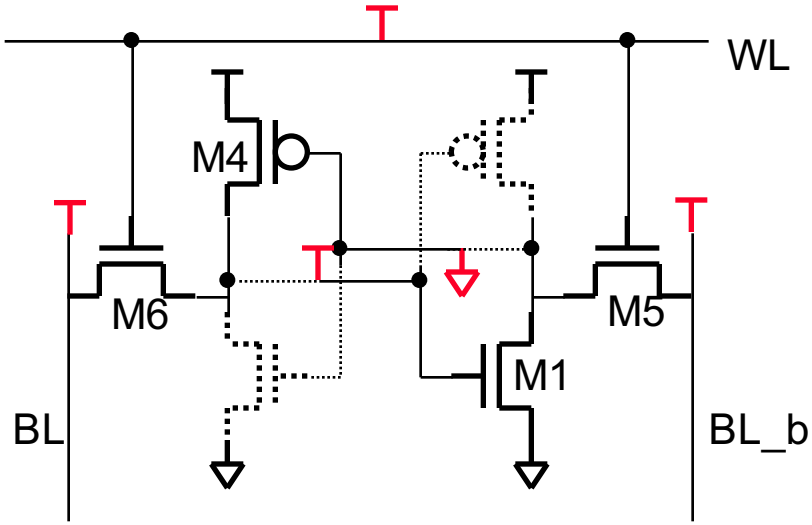
- For asymmetric VTCs, unity-gain margin is incorrect for the NM.
- The best way is to graphically fit a maximum square.



Memory Cell Analysis

Semi-static CMOS SRAM Analysis (Read)

- Analysis to illustrate the sizing issue.
  - Semistatic
    - BL doesn't move
      - O.K. assumption
    - Internal voltages don't move.
      - Overestimate
  - Ideal square law models – actually solvable!
  - But, only gives us an idea (not entirely realistic).
- Both BL and BL_b are precharged to Vdd.
  - M4 and M6 are both pulling HIGH so no sizing constraint.
  - M1 fights against M5.
    - M1 in Triode, M5 in Sat
    - M1 must win to avoid flipping the cell.



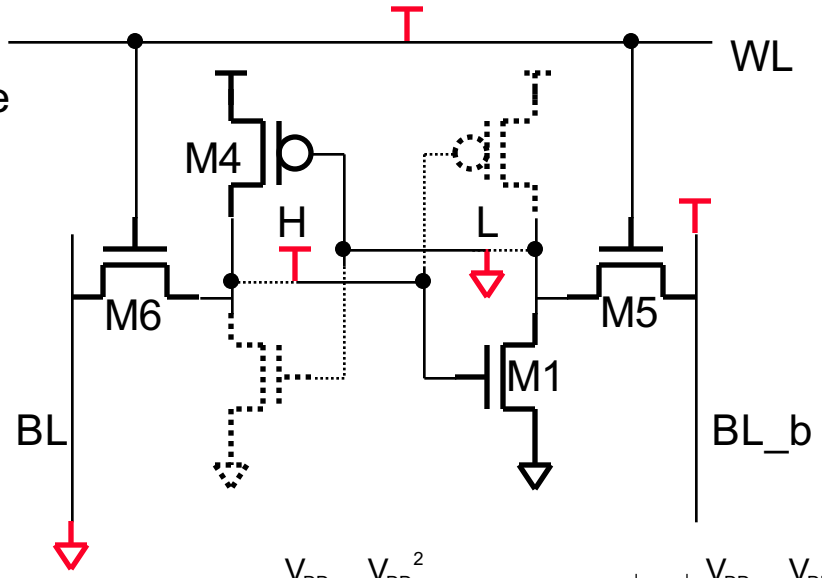
$$k_{N\_M1}((V_{DD}-V_{TN})\frac{V_{DD}}{2}-\frac{V_{DD}^{2}}{8})>\frac{k_{N\_M5}}{2}(\frac{V_{DD}}{2}-V_{TN^*})^{2};$$

$$V_{TN}=\frac{V_{DD}}{4};V_{TN^*}=\frac{V_{DD}}{3}$$

$$(W/L)_{N\_M5}<18(W/L)_{N\_M1}$$

Semi-static CMOS SRAM Analysis (Write)

- 2 possible constraints
  - Only 1 needs to be satisfied for write to occur.
  - Writing a LOW
    - M6,M4 are both in Triode
    - M6 must overwrite M4.
  - Writing a HIGH
    - M1 in Triode, M5 in Sat
    - M5 should overwrite M1.
    - This condition is superceded by READ.



$$k_{N\_M6}((V_{DD}-V_{TN})\frac{V_{DD}}{2}-\frac{V_{DD}^{\ 2}}{8})>k_{P\_M4}((V_{DD}-|V_{TP}|)\frac{V_{DD}}{2}-\frac{V_{DD}^{\ 2}}{8});$$

$$V_{DS}=\frac{V_{DD}}{2}$$

$$\mu_N(W/L)_{N\_M6}>\mu_P(W/L)_{P\_M4}$$

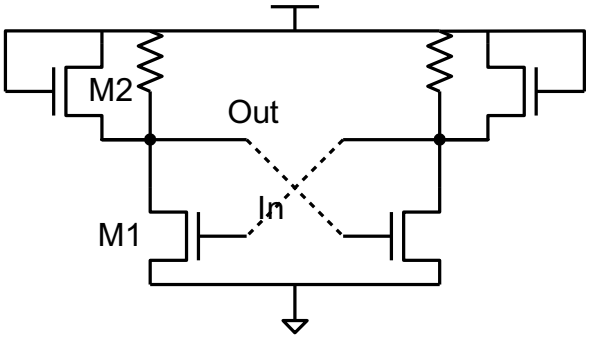
$$k_{N\_M1}((V_{DD}-V_{TN})\frac{V_{DD}}{2}-\frac{V_{DD}^{\ 2}}{8})<\frac{k_{N\_M5}}{2}(\frac{V_{DD}}{2}-V_{TN^*})^2;$$

$$V_{TN}=\frac{V_{DD}}{4};V_{TN^*}=\frac{V_{DD}}{3}$$

$$(W/L)_{N\_M5}>18(W/L)_{N\_M1}$$

Memory Cell Margins

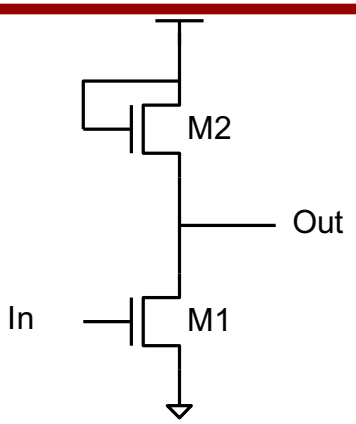
- Read operation is more sensitive to noise.
- It is better to look at the memory cell's margin during a READ operation to finalize the sizing.
  - Assume bit lines are at Vdd
  - Access device becomes a load
  - If we break the cross coupling
    - These are the dotted lines
    - Results in a funny inverter

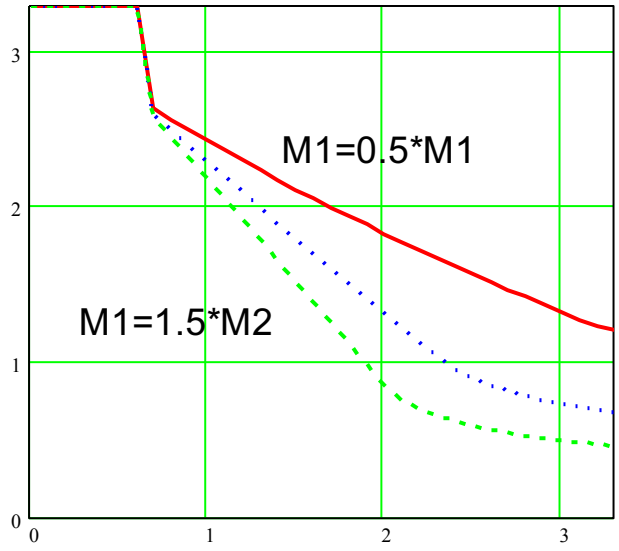


- This inverter needs to be a good digital gate
  - Needs to have noise margins
  - If the resistor current is very small this inverter is easy to analyze – both M1 and M2 are saturated for much of the swing

Cell Inverter Transfer Function

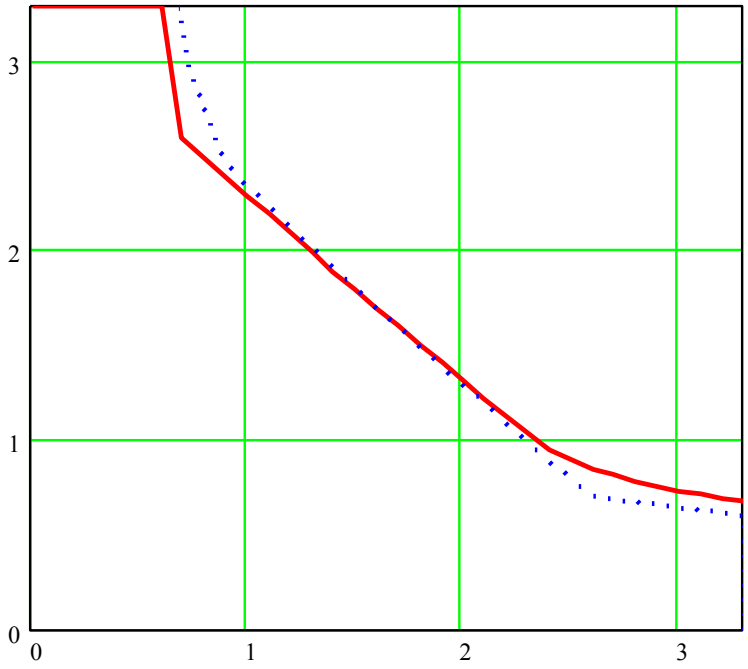
- If M1 and M2 are the same size
  - If both are saturated
  - V_{gs} of both transistors needs to be rougly the same
- Implies
  - $V_{out} = Vdd - V_{in}$ for $V_{th} < V_{in} < V_x$
  - V_x is the input voltage where M1 leaves saturation
    - Since V_{dsat} is around 1.5V, should be around Vdd – 1.5V
    - Remember until M1 becomes linear, V_{gs} of transistors match
- This implies gain of this gate is only 1
  - This is the middle curve





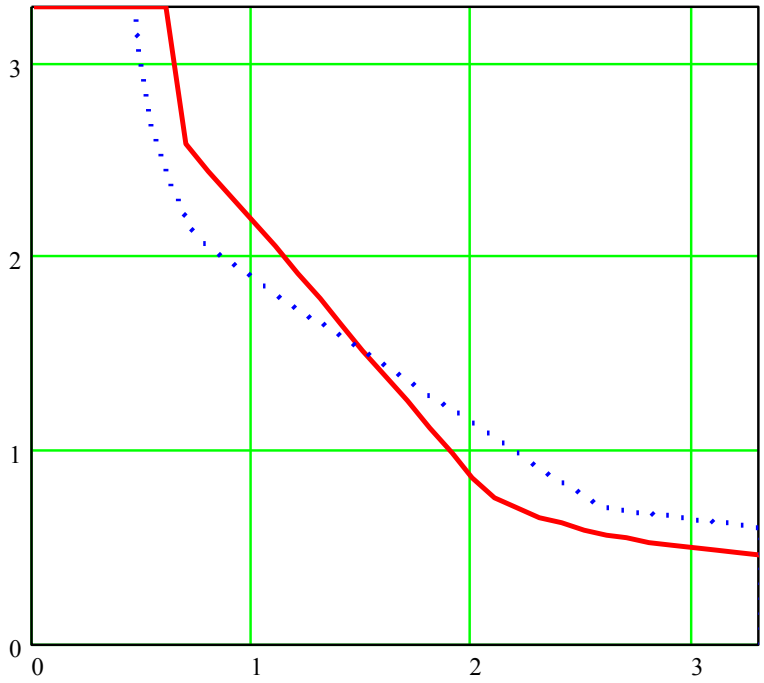
Cell Stability

- What happens when you cross couple two of these inverters.
- Draw the transfer curve of both inverters in one plot
  - V_{out} of one inverter is V_{in} of the the other, and vice versa
  - For M1 equal M2
  - Only one place curves cr
  - Vdd/2
- Cell will forget value
  - Not enough gain in cell
  - Increase gain
    - Make M1 larger

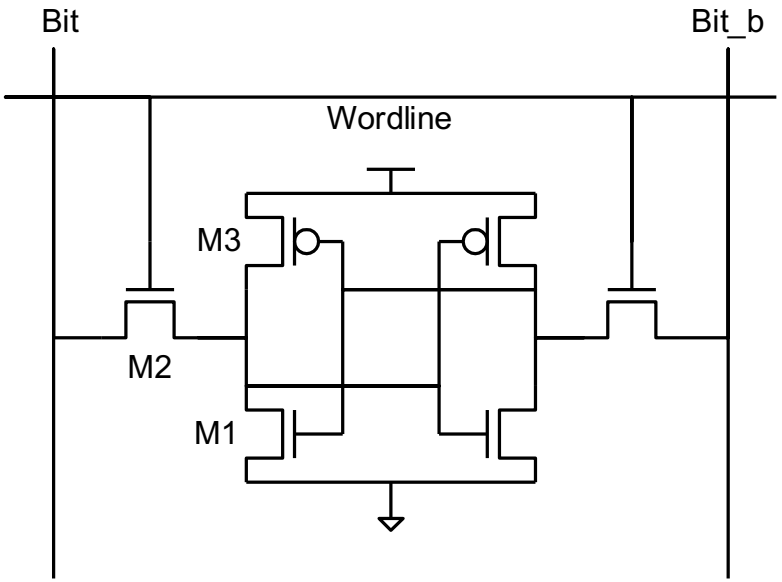


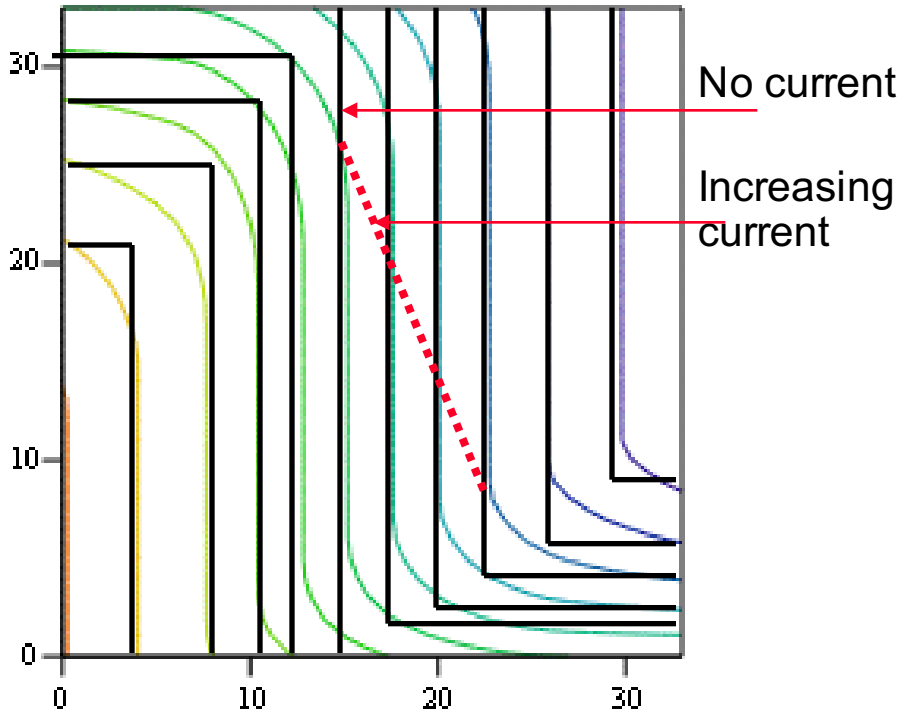
Cell Stability

- This plot shows what happens when M1 = 1.5 M2
  - Cell is stable in theory
    - Three crossing points
  - What about noise?
    - Noise shifts curve
  - ~100mV of noise will flip the cell



6-Transistor SRAM

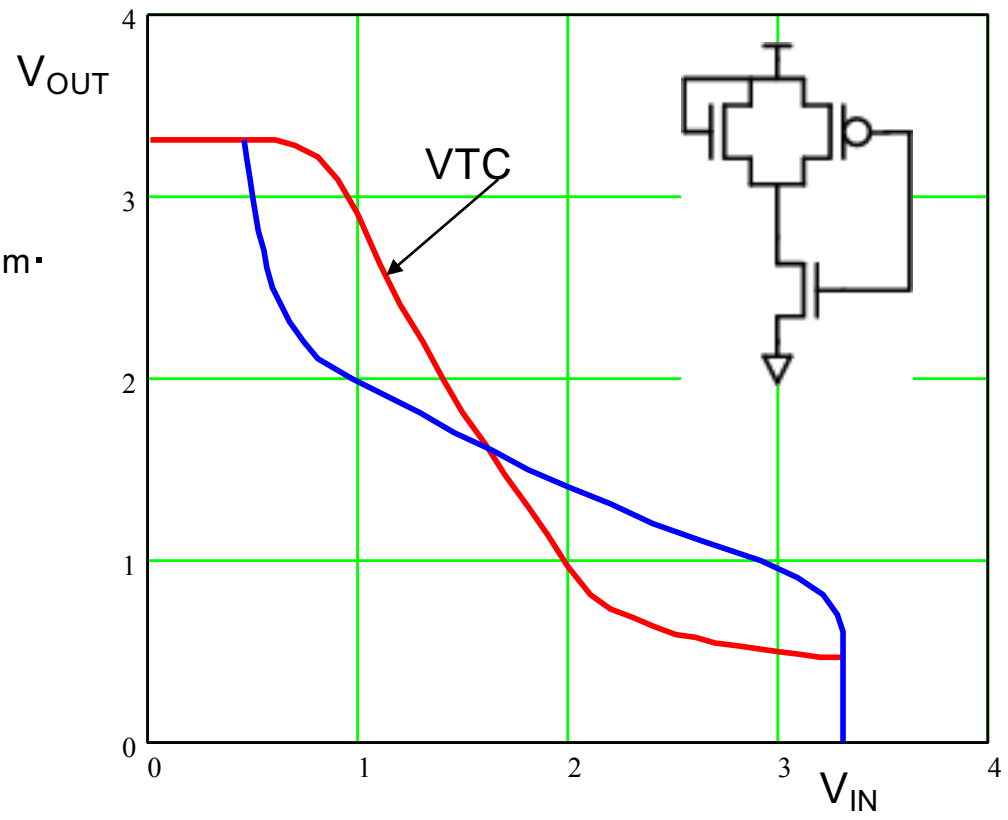




- Can be thought of as injecting a current with M2 which shifts the curve.
  - Not quite because current changes with the voltage.
  - But it reduces the margin.

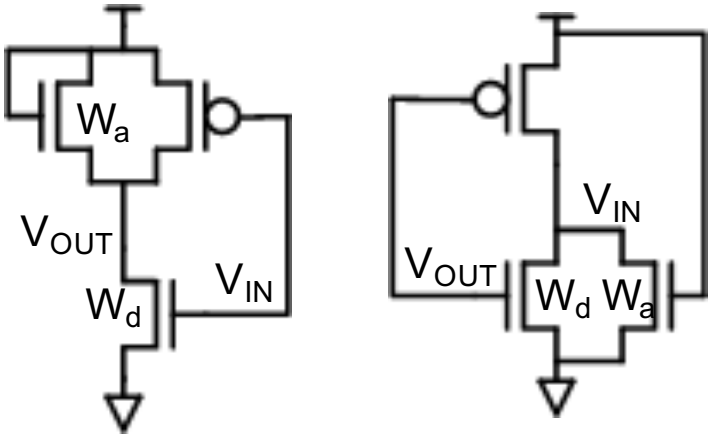
Read Margin for 6-T SRAM

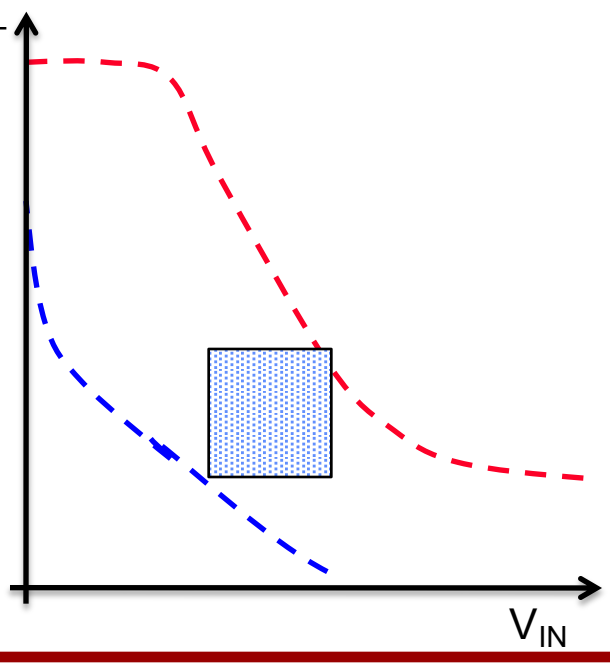
- pMOS devices help margin a lot
- But gain is still small
  - Around 2
  - PMOS helps the g_m.
- Margins are much better.
  - Several hundred millivolts



Write Noise Margin

- During a write, the cell is imbalanced intentionally
  - One BL is driven to Vdd (Same VTC as a READ)
  - The other BL is driven to Gnd.
- The smallest square that touches both lines is the margin.
  - Shift cannot cause a crossing.

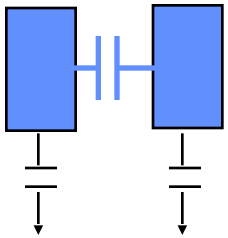




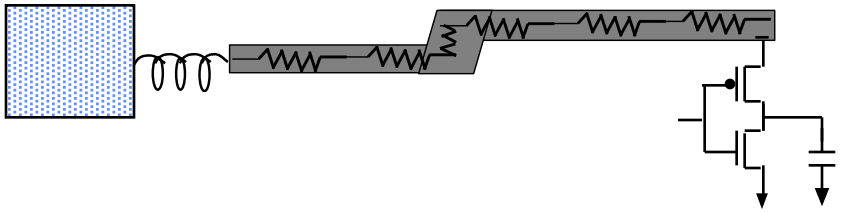
Noise Sources

Sources of Noise and Static Offsets

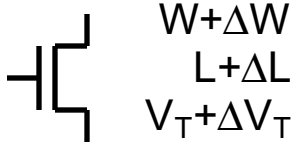
1. Capacitive and inductive coupling between lines:



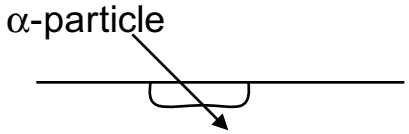
2. Power and ground variations:



3. Transistor mismatches:

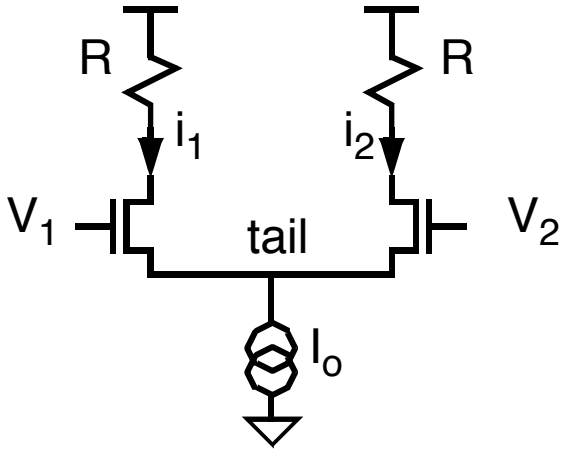


4. High-energy particles:



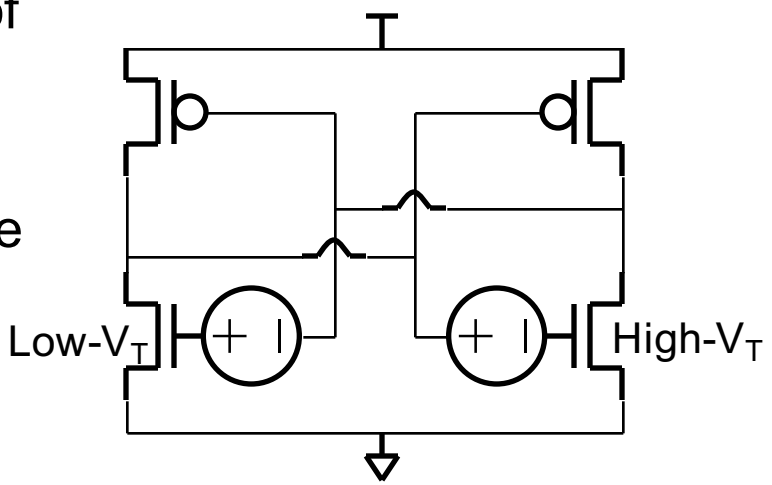
(Pseudo-)Differential Signals

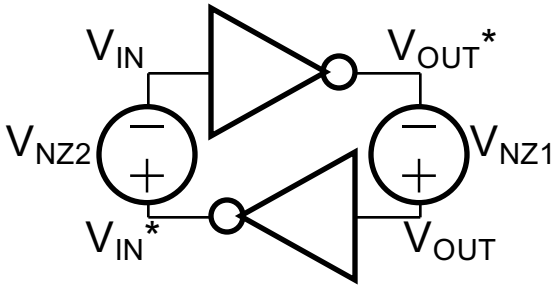
- Can build circuits that have differential outputs
  - Voltage mode (differential domino)
  - Current mode (mostly)
- Current Switch Circuits
  - ECL like circuits -- SCFL (source-coupled fet logic)
  - Analog like functions
- Have low common-mode noise sensitivity
  - Look at voltage difference between wires
    - If noise coupling is to both nodes you don't see it
- Pseudo-differential is when the other node is a DC reference voltage.
  - Maintain the same coupling.



Transistor Matching

- Transistor matching is a function of the area.
  - $\sigma_{VT} = k_{VT}(\text{Area})^{-0.5}$
  - The larger area, the smaller the mismatch.
  - k_{VT}~20mV-μm
- Threshold mismatch is dominant
  - Value is Gaussian distributed.
  - Simply modeled by adding a voltage source to the gate.

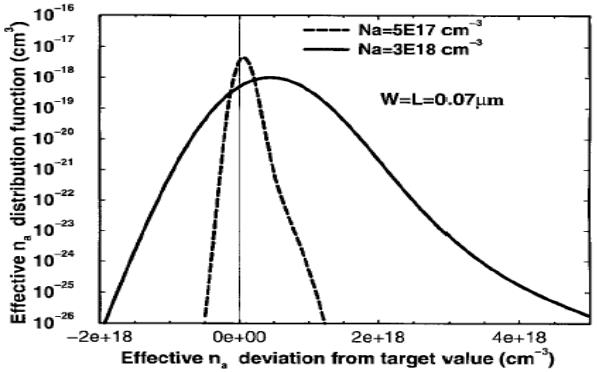




Threshold Voltage Matching Scaling Trend

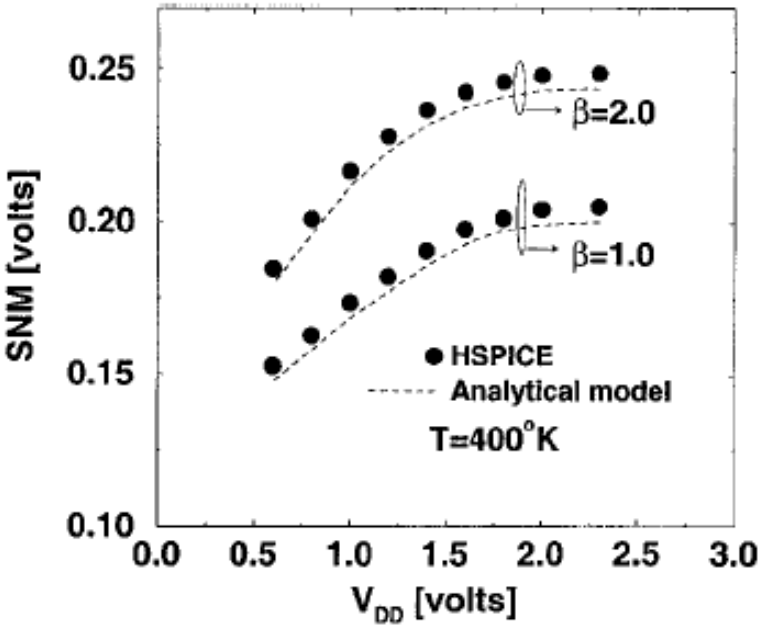
- Threshold variation has been increasing with the increased variation of doping concentrations

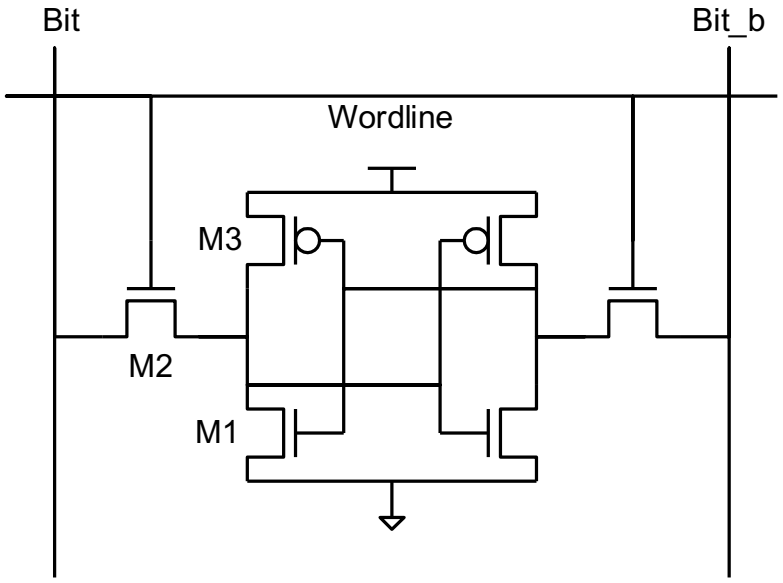
year	1997	1999	2001	2003	2006	2009	2012
L (nm)	250	180	150	130	100	70	50
T_{ox} (nm)	4.5	3.5	2.8	2.3	1.7	1.2	0.8
V_{dd} (V)	2.2	1.8	1.5	1.2	1.0	0.8	0.5
V_{th} (V)	0.45	0.40	0.35	0.33	0.30	0.28	0.2
N_a (cm^{-3})	5.95e17	8.0e17	9.5e17	1.22e18	1.8e18	2.9e18	4.85e18
σVth (mV)	21	23	25	27	28	30	32



Impact of Cell Sizing and Supply on Noise Margin

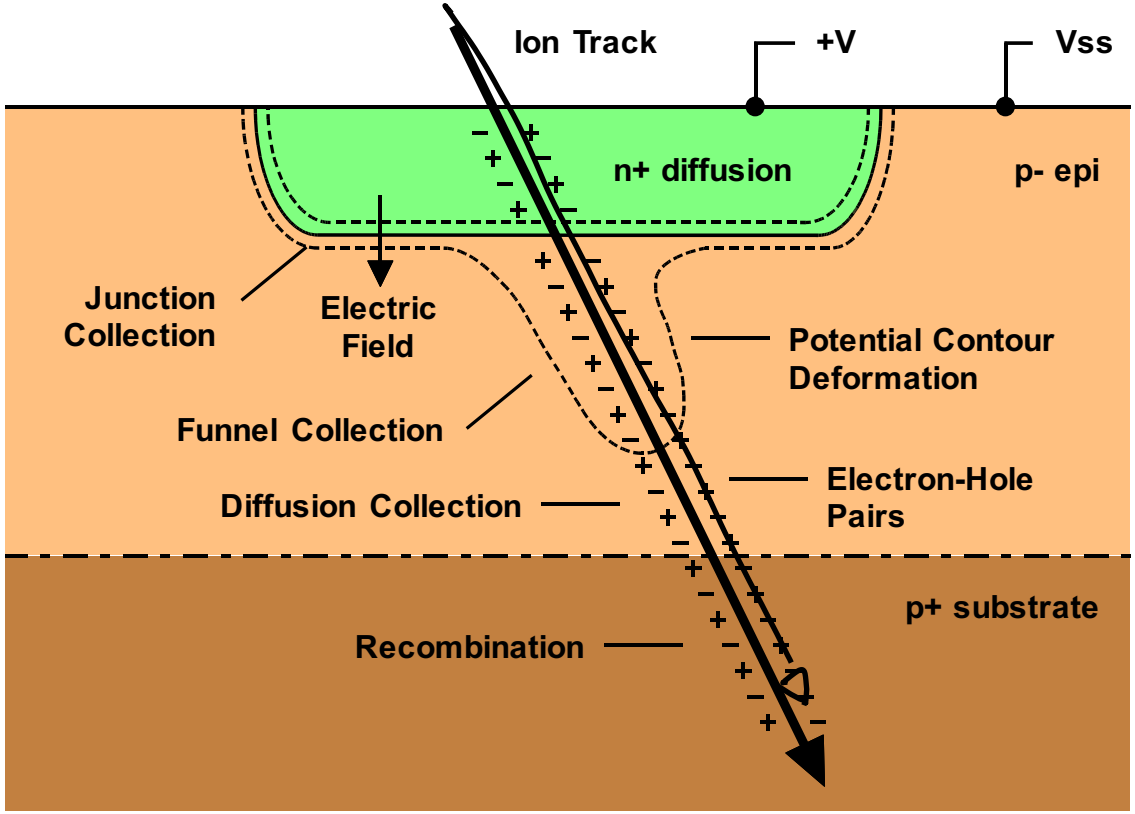
- The read margin depends on the sizing ratio of (pull-down:access)
  - Ratio, $\beta = W/L_{M1} : W/L_{M2}$
  - Higher ratio is better for read.
- Read margin is very sensitive to the supply voltage.



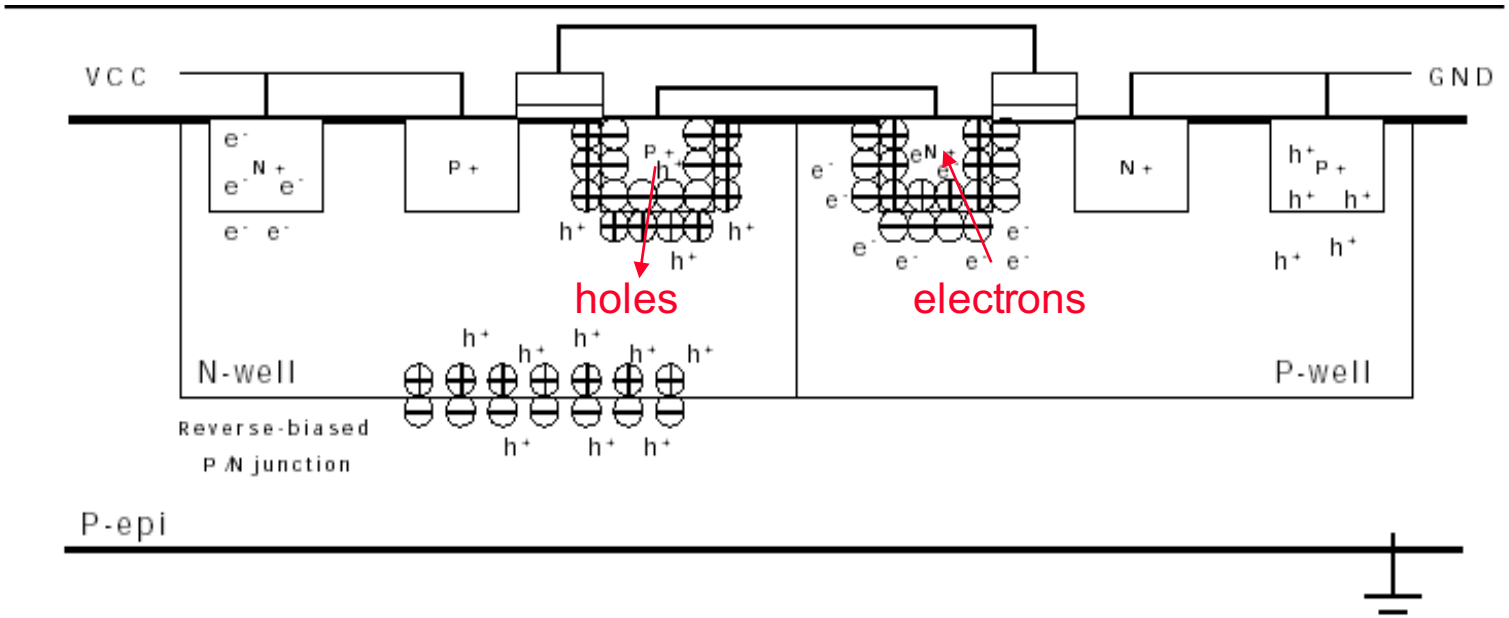


High-Energy Particles and Soft Errors

- Neutron or a-particle (He ion) creates electron-hole pairs upon impact.
  - Atmospheric or lead in packages
  - Perturbs the potential of the junction momentarily.

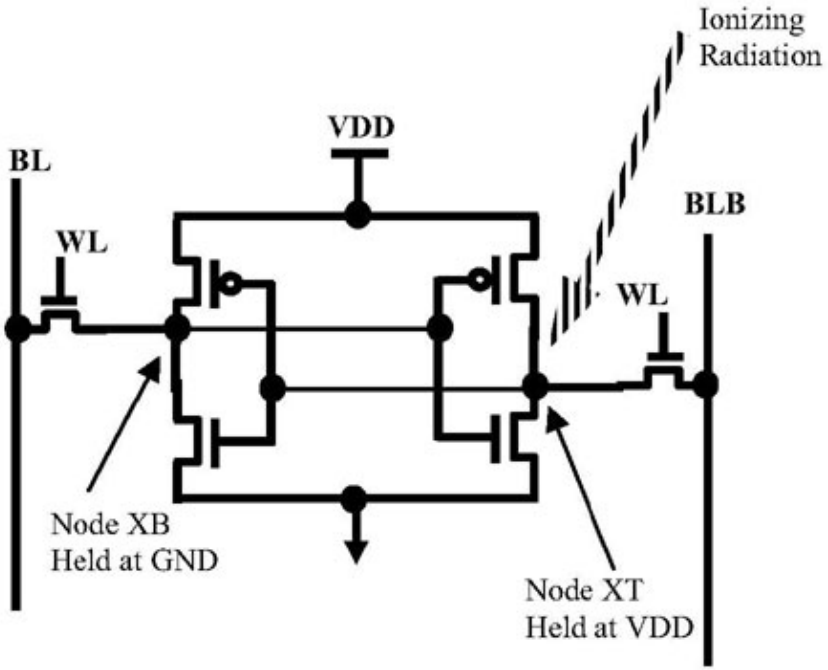


Impact of a Collision

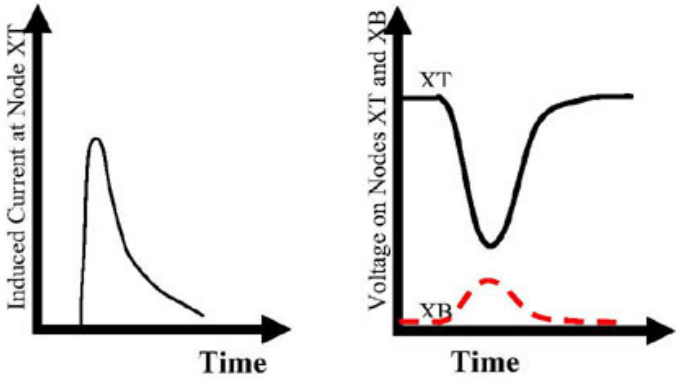


- Electrons collect in n-type diffusion
  - Lowers voltage.
  - Has an impact if stored value was a 1.
- Holes collect in p-type diffusion.
  - Raises voltage.
  - Has an impact if stored value was a 0.

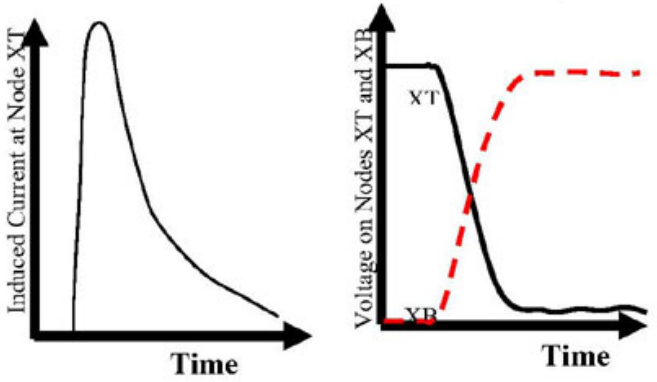
Impact on SRAM Cell



Low Charge Collection and Fast Recovery Time
=> no soft error occurs and the cell recovers



Large Charge Collection and Slow Recovery Time
=>soft error occurs and the cell flips

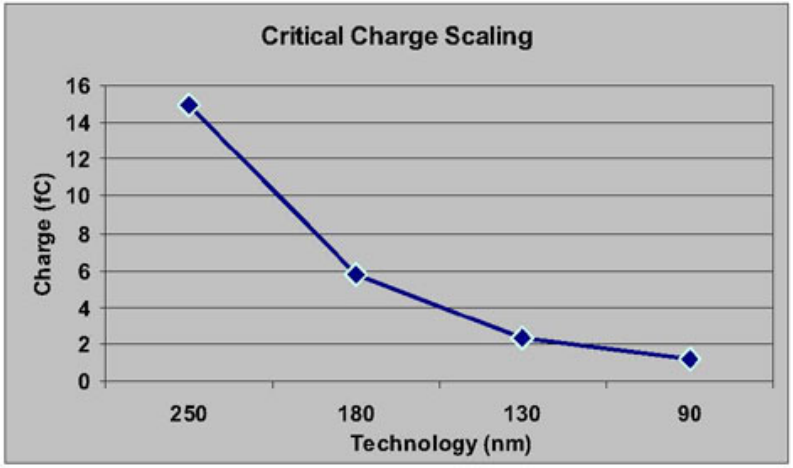


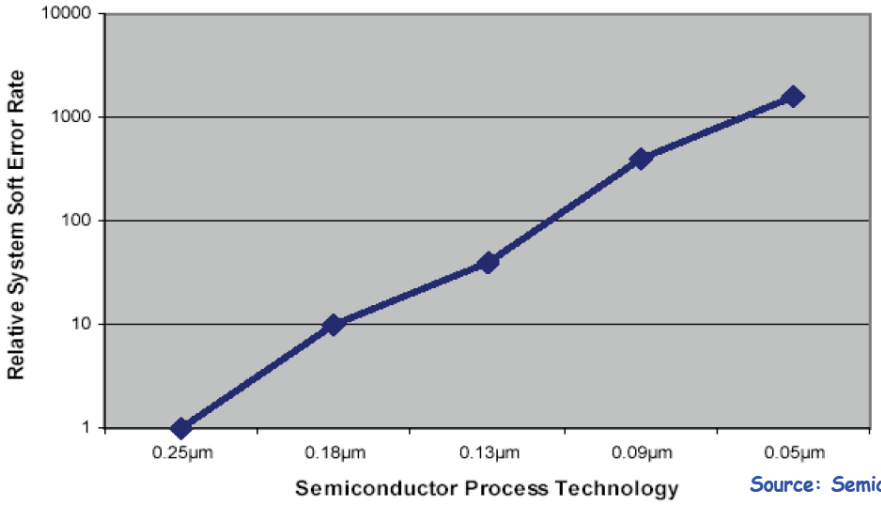
What Does Soft Error Rate Depend On

- Number of particles
  - Type of packaging (lead free)
  - Shielding of cosmic rays (more sensitive for space applications)
- Volume (Area * depth) of the collecting diffusion.
  - Larger the area the more charge induced from the particle.
- Error rate depends on $Q_{induced}$.
  - $Q_{induced} > Q_{critical} = Q_{store}$ + constant
    - Constant proportional to I_{dsat}
  - Increasing the storage capacitance helps minimize error.
  - Increasing the voltage reduces the impact of the particle charge.
- Metric: Failure-In-Time (FIT) per megabit value, 1 FIT = 1 Failure in 10^9 hours
  - Example:
    - Assume SER for a SRAM = 4000 FIT/Mb
    - SRAM contains = 16Mb
    - 64,000 errors in 10^9 hours or 1 failure every 1.8years (acceptable?)

Why is SER Important

- SER induces high failure rates for SRAMs.
  - Getting worse for flip-flops
- Impact on system is not predicted and hence undetected errors can impact computational accuracy.
- Problem worsens with scaling
  - Lower voltage
  - Higher density.

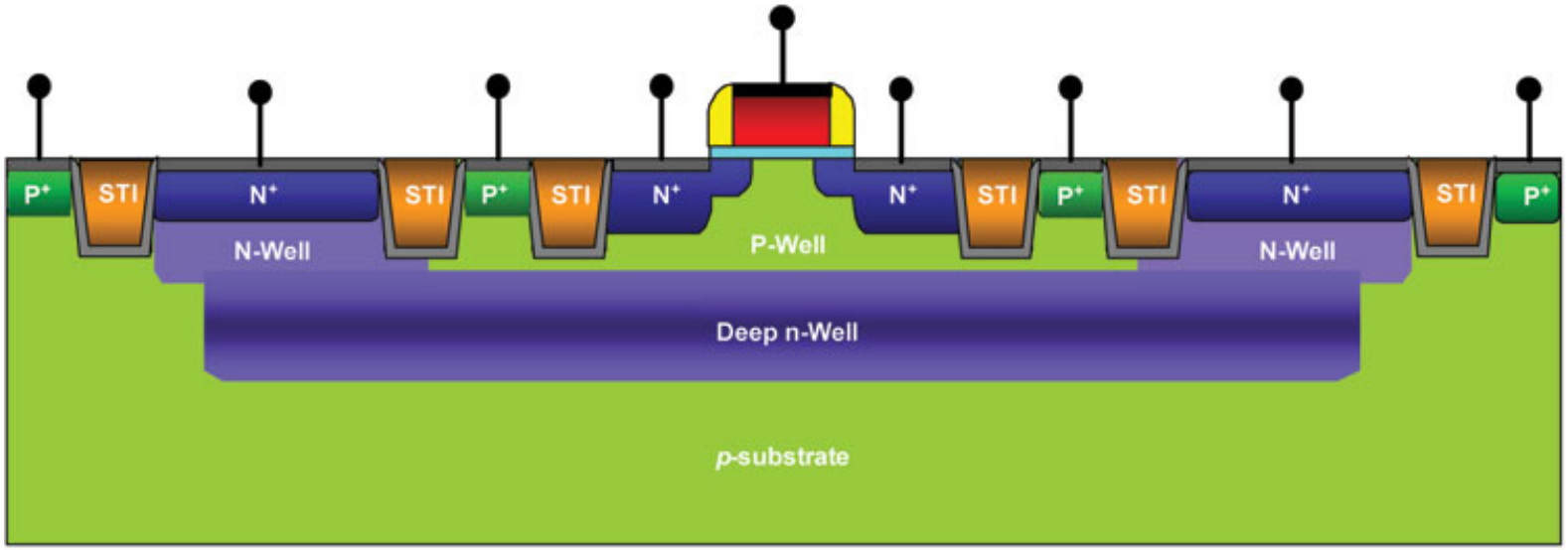




Source: Semico Research, www.actel.com

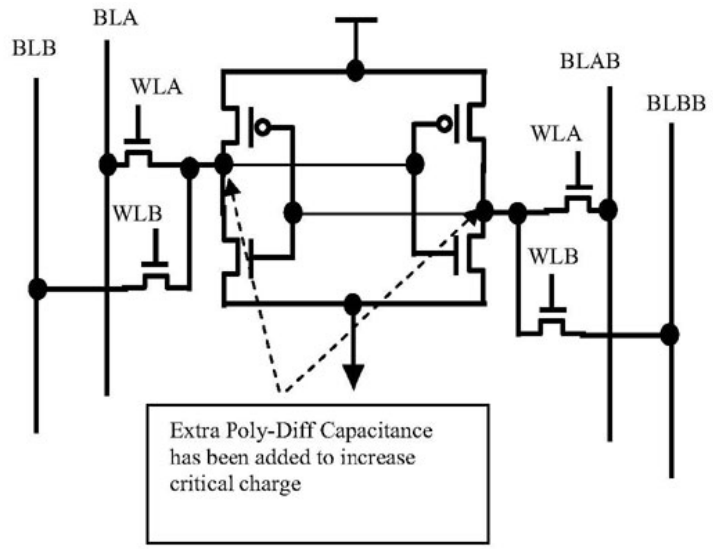
Addressing SER: Technology

- Deep N-Well technology
  - Reduce depth of P-Well
  - Provide a second place for charge to go.
- Reduce SER 1.5x-2.5x for α-particles

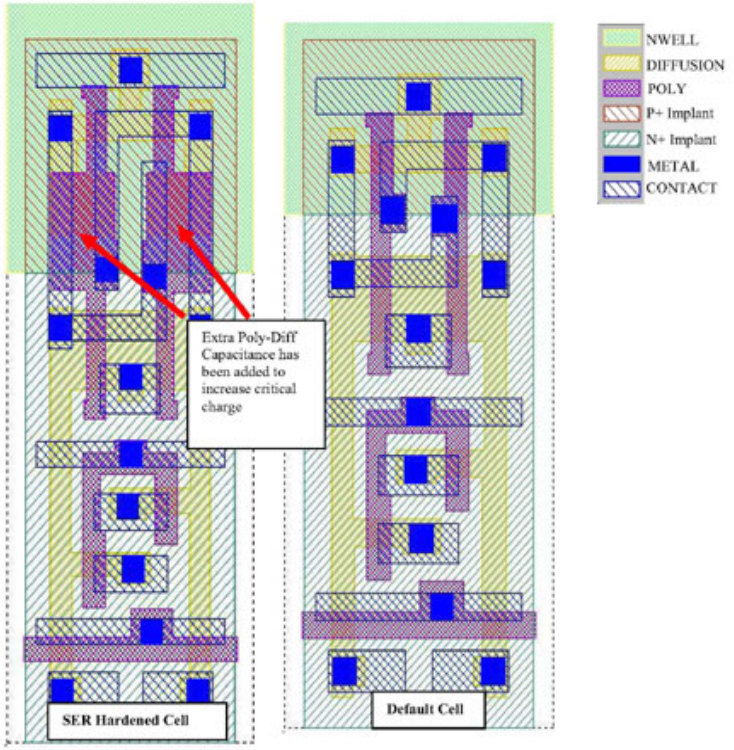


Addressing SER: Layout

- Hardening the bit cells
  - Add capacitance to increase Q_{crit}
- Penalizes circuits
  - 6-8% speed, 13-15% area
  - 23x SER improvement



[MTDT04 N.Derhacobian]



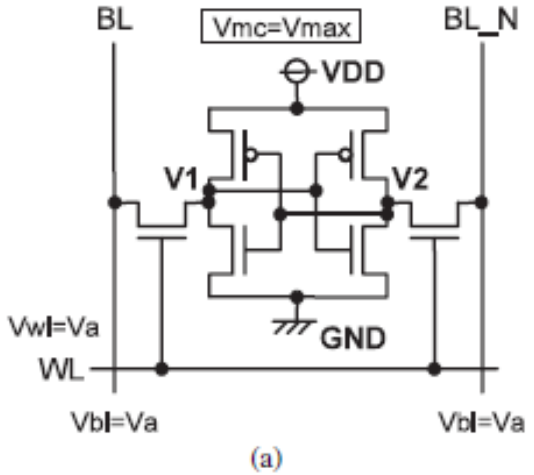
Addressing SER: Architecture

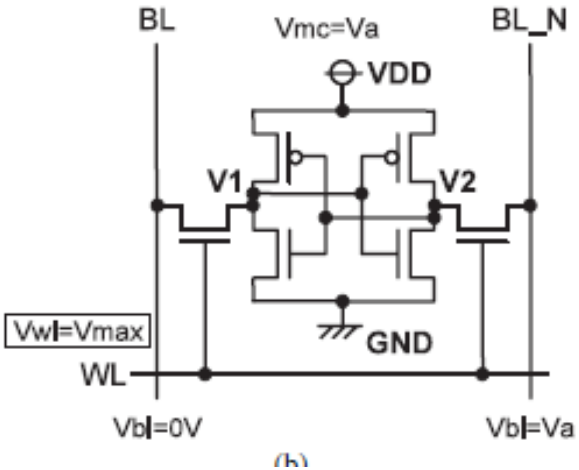
- Error-Correction-Code (ECC)
  - Simple
    - Parity bit check – a big XOR to detect an error
    - One extra bit per byte to perform check
  - Complex:
    - Detect and correct errors (single-bit, multi-bit)
- Area and performance overhead
  - Area overhead is inversely proportional to word width.
  - ~20% for 32bits, ~10% for 64bits
- >10x SER improvement

SRAM Cell Design Trends

Dual V_{dd} Design

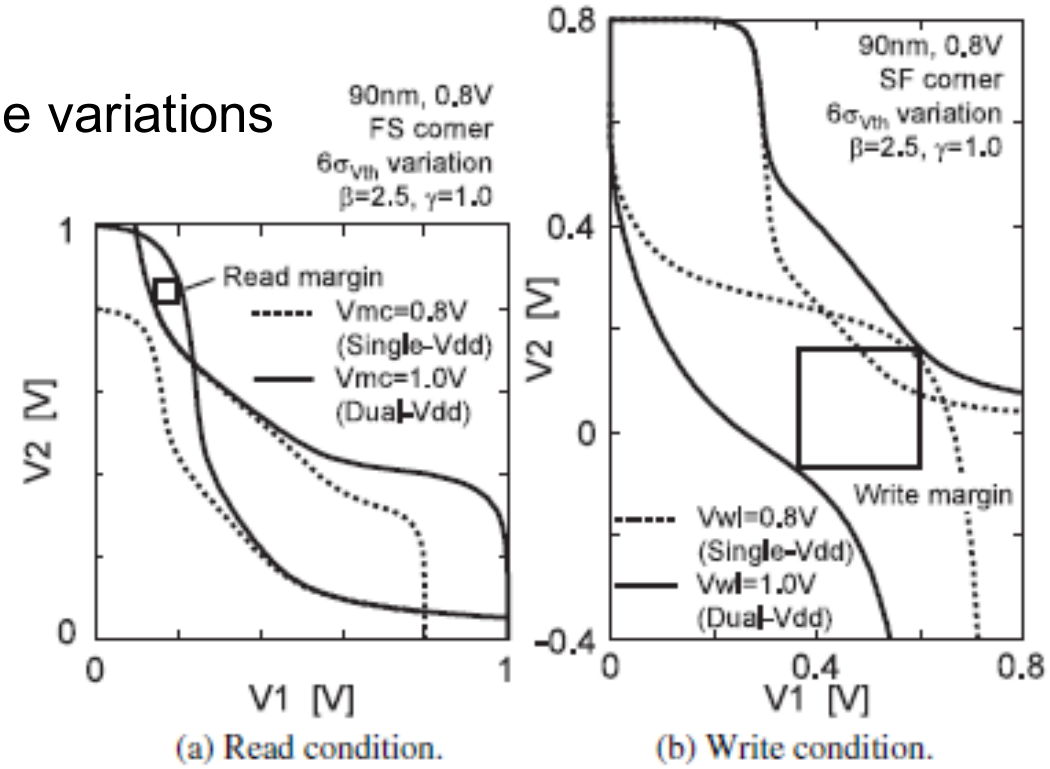
- Increase READ margin without sacrificin WRITE margin
  - Dynamically vary the V_{dd}.
- When READ
  - Use max V_{dd} for the cell
  - Lower pre-charge voltage (V_a) for bit-lines
- When WRITE
  - Use lower voltage for cell (V_a)
  - Use max voltage for WL
- When not accessing
  - Use lower cell voltage (<V_a)
  - Minimize leakage





Dual V_{dd} Margin

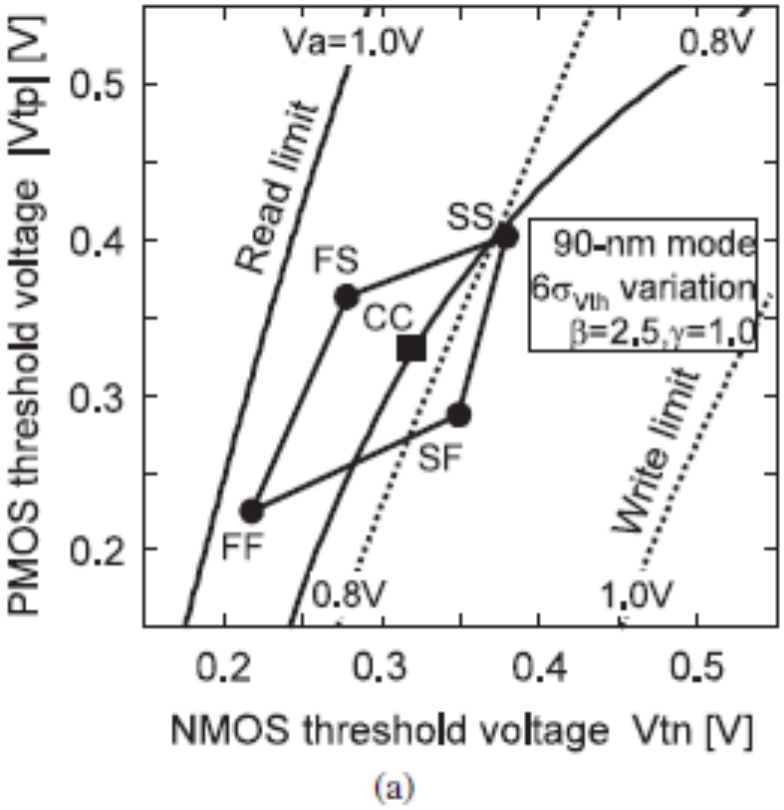
- Dual V_{dd} can dramatically increase the margins.
  - Write margin is the VTC when the bit-lines are split.
  - Account for worst case variations



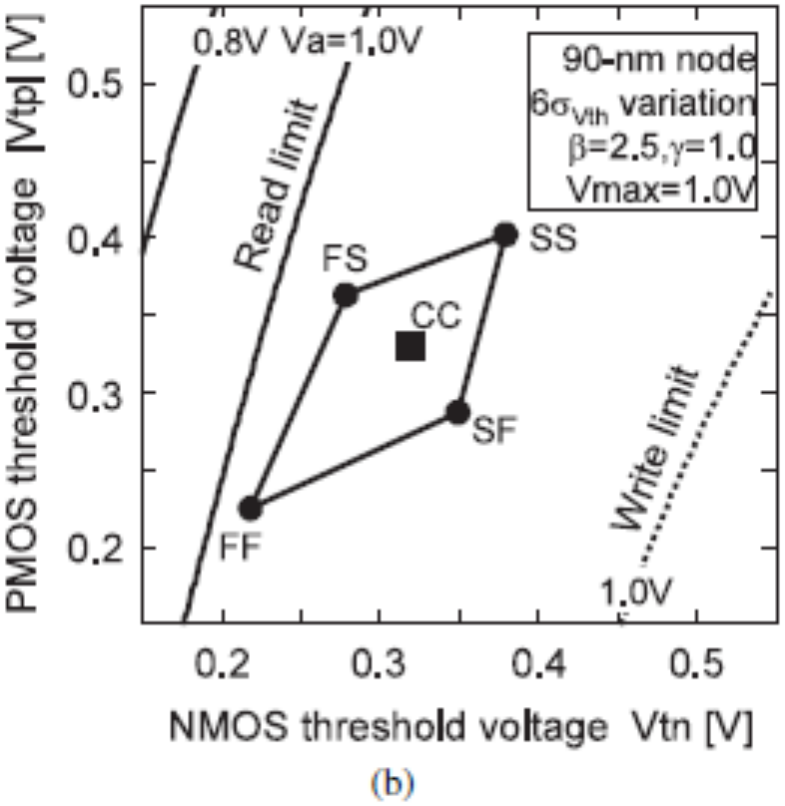
(a) Read condition. (b) Write condition.

Dual Vdd Corner Simulations

- Single V_{dd}
- Dual V_{dd}



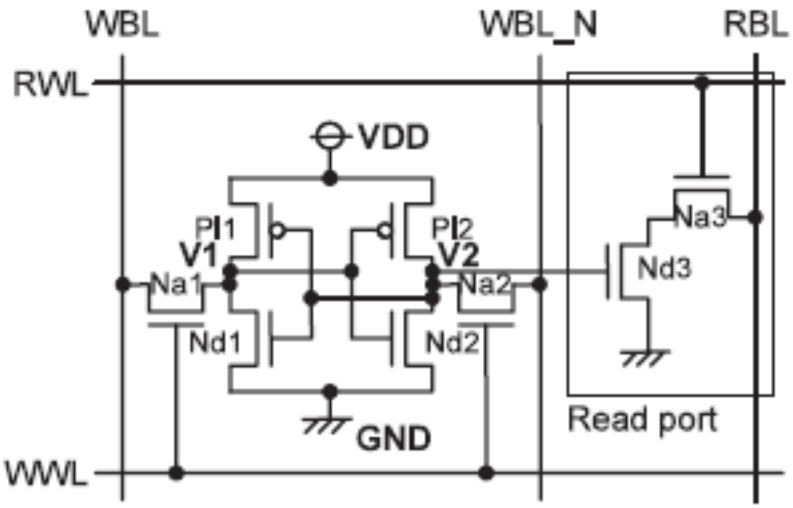
(a)

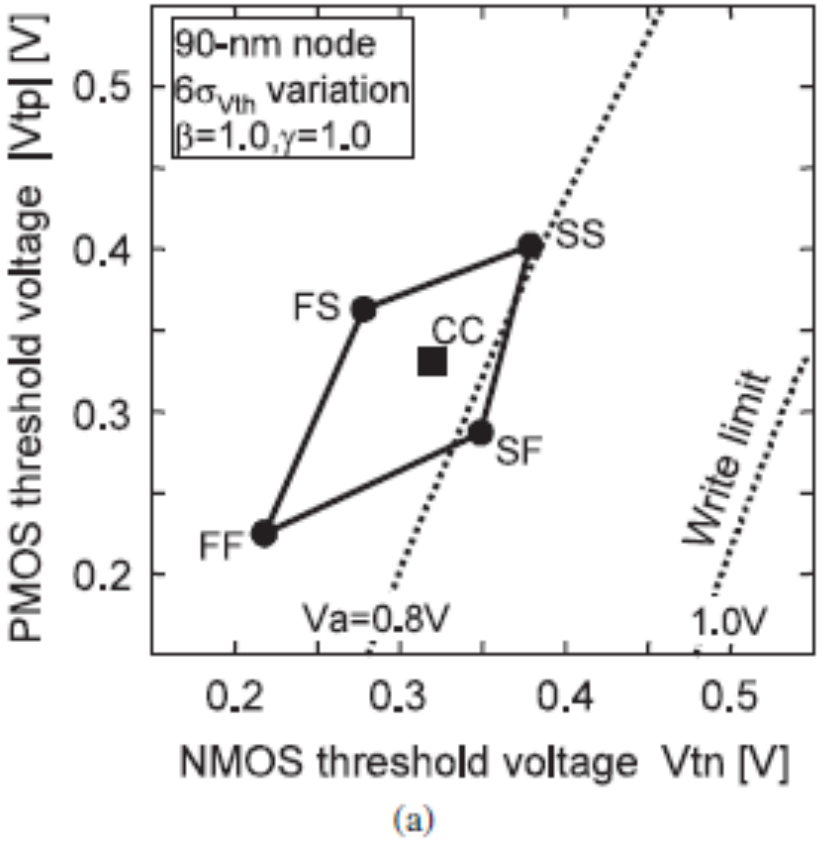


(b)

8T Cell

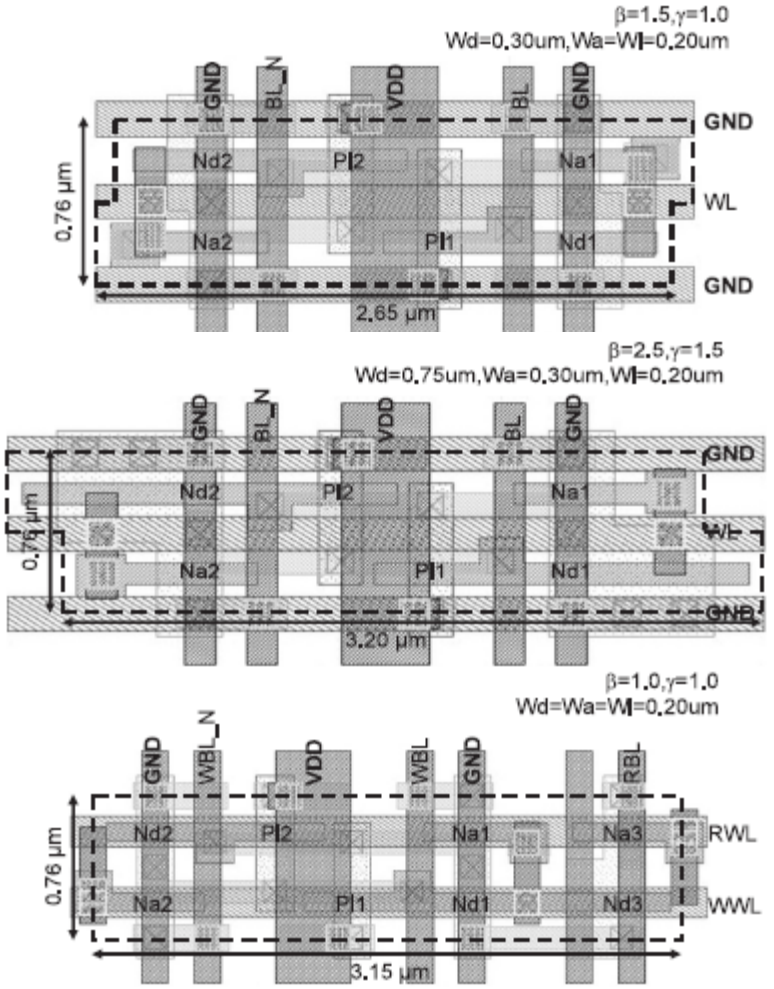
- Use more transistors per cell
  - Many possible designs
- Use separate RBL
  - No read/write conflict
  - Slightly improve SER





Area Comparison

- 6T cell layout
  - Depends on sizing of access transistors
- 8T cell can use minimum devices throughout
  - Devices are NMOS (in series)
    - Little overhead for additional transistors.
  - Added RBL is over active devices.
  - Almost same area (10% penalty for min 6T design)



Summary

- SRAM cells are a good way to understand noise margins.
  - Single stage noise margin is not realistic enough for the worst case scenario.
  - SRAM feedback is similar to generalized noise margin (multiple noise sources).
- Gain in the logic gate is critical in providing noise margin.
  - READ access leads to low noise margins because of the reduced gain.
- Noise margins are critical to recover from noise injection.
  - SER is a serious issue for deeply scaled devices due to the low Q_{crit}.
- Modern designs for memories are favoring larger capacitances, more complex cells, and accessing of the cells to improve margin.

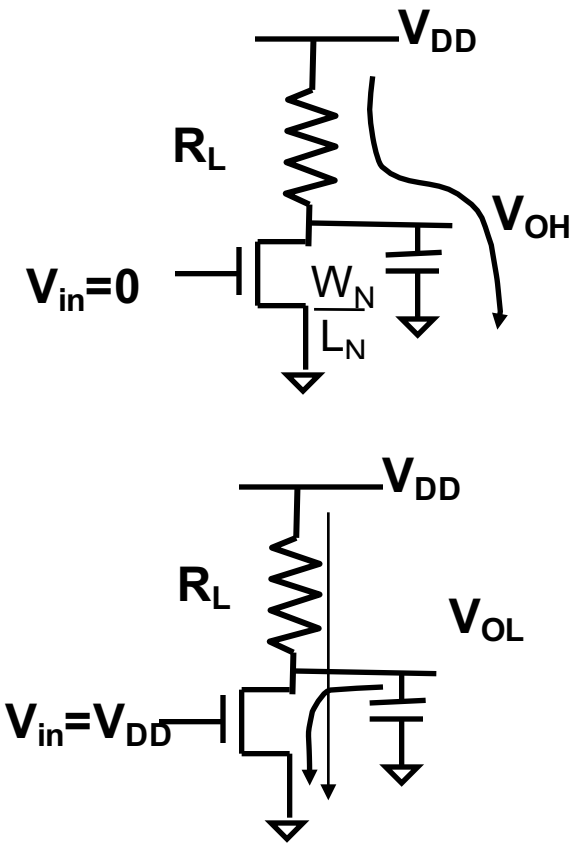
Review of Voltage Transfer Characteristics

Courtesy of BAW

Voltage Transfer Functions

- Many classes spend a lot of time deriving VTC
  - I don't think it is very useful, so we won't do it
- The next pages of lecture notes outline the derivation
  - With a 'real' MOS model they become complex
    - Unless you have a computer
- Important points to remember
  - The switching point V_{sw} is set by ratio of up / down currents
  - Transfer functions found by finding region of operation
    - nMOS linear, pMOS sat, etc
  - Estimating shape is easy
  - Need flat regions and high gain regions

Simple Resistive Load



When V_{in}=0 V, the MOS transistor turns off and the output capacitance is charged up to V_{DD} through the resistance R. Therefore,

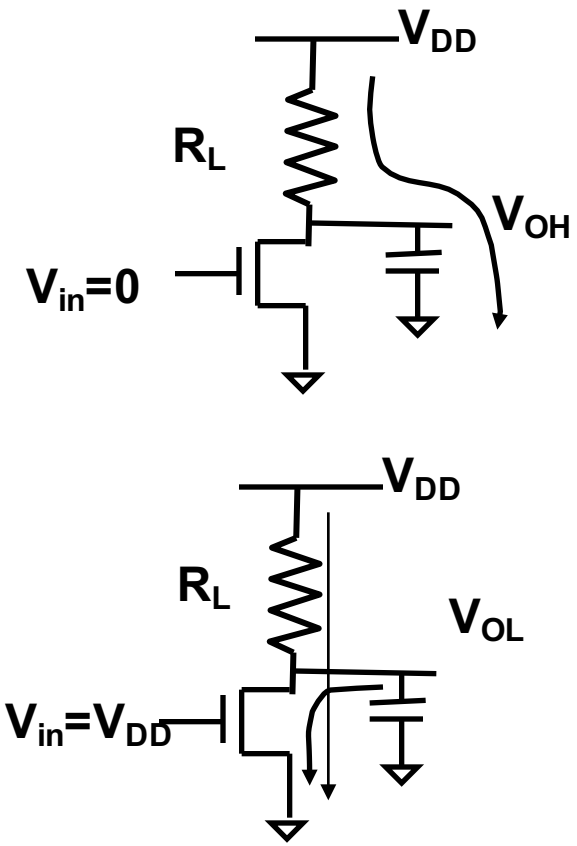
$$V_o = V_{DD} = V_{OH}$$

When $V_{in}=V_{DD}$, the MOS transistor turns on and discharges the output capacitance to a low value, V_{OL}, that depends on the ratio of R to the on-resistance of the transistor. Therefore,

$$\frac{V_{DD} - V_{OL}}{R_L} = k' \frac{W}{L} (V_{DD} - V_{TN} - \frac{V_{OL}}{2}) V_{OL}$$

$$V_{OL} \approx \frac{V_{DD}}{R_L k' (W/L) (V_{DD} - V_{TN})}$$

Using Advanced Model



What happens if we use velocity saturation model?

$$V_o = V_{DD} = V_{OH} \qquad \text{(no change)}$$

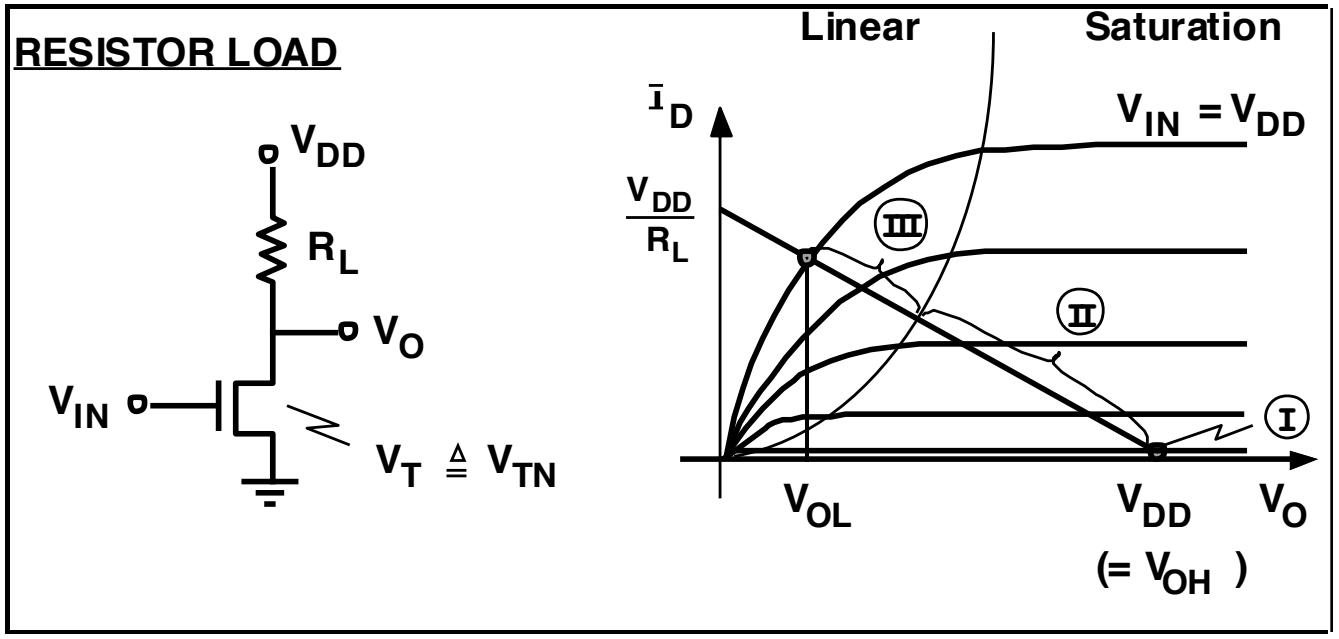
$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{\mu_e C_{ox}}{(1 + V_{OL}/E_c L)} \frac{W}{L} (V_{DD} - V_{TN} - \frac{V_{OL}}{2}) V_{OL}$$

$$V_{OL} \approx \frac{V_{DD}}{R_L \; k' (W/L) \; (V_{DD} - V_{TN})} \qquad \text{(roughly the same)}$$

Load Line for Resistive Load Inverter

What happens between the two extreme points?

=> look at load-line characteristics of the two devices



VTC Calculation

(I) **INVERTER OFF** $(V_{IN} < V_{TN})$

$$\boxed{V_O = V_{OH} = V_{DD}}$$

(II) **INVERTER SATURATED**

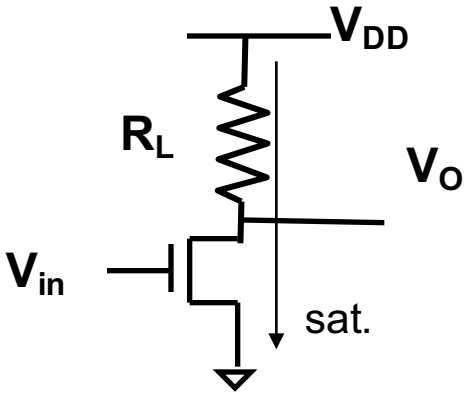
$$\boxed{I_D = \frac{k_I}{2}(V_{IN} - V_{TN})^2 \quad \text{where} \quad k_I \triangleq \mu_n C_{ox}\left(\frac{W}{L}\right)_I}$$

and

$$I_D = \frac{V_{DD} - V_O}{R_L}$$

$$\therefore \quad \frac{k_I}{2}(V_{IN} - V_{TN})^2 = \frac{V_{DD} - V_O}{R_L}$$

$$V_O = V_{DD} - \frac{R_L k_I}{2}(V_{IN} - V_{TN})^2$$



VTC Calculation (cont'd)

III INVERTER LINEAR

$$I_D = k_I\left(V_{IN} - V_{TN} - \frac{V_O}{2}\right)V_O = \frac{V_{DD} - V_O}{R_L}$$

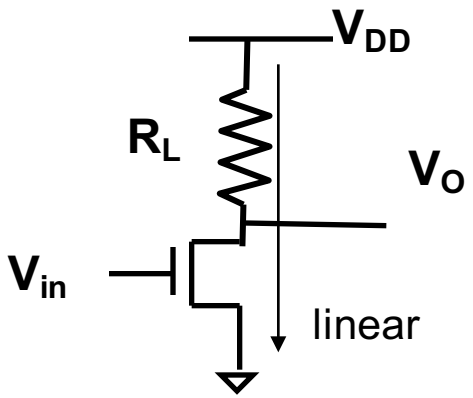
$$V_O\left[1 + R_L k_I\left(V_{IN} - V_{TN} - \frac{V_O}{2}\right)\right] = V_{DD}$$

II – III TRANSITION

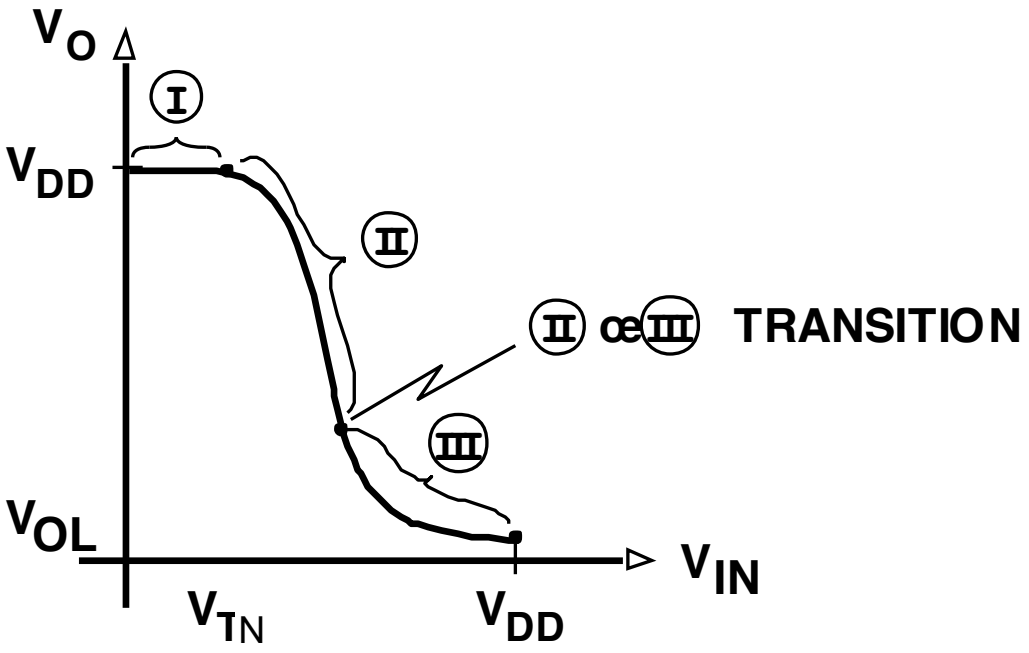
$$V_{IN} - V_{TN} = V_O$$

$$\therefore \quad V_O\left(1 + \frac{R_L k_I}{2} V_O\right) = V_{DD}$$

$$V_O = \frac{1}{R_L k_I}\left[\sqrt{1 + 2V_{DD} R_L k_I} - 1\right]$$



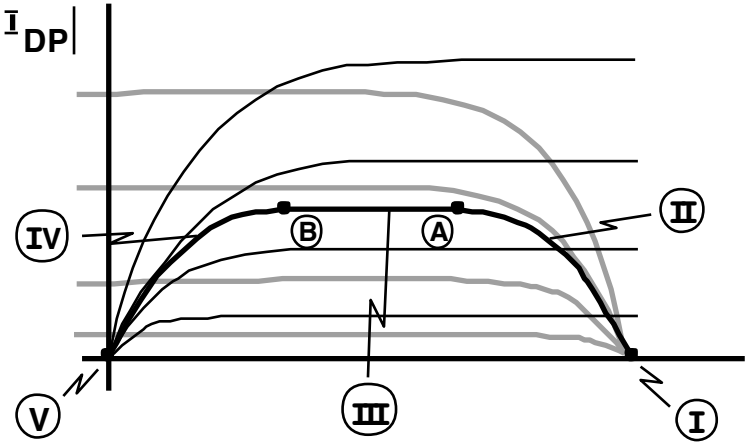
Summary of VTC for Resistive Load Case



Typically large resistors are needed to achieve desired V_{OL}

$\therefore$ not practical way to implement an inverter in MOS design.

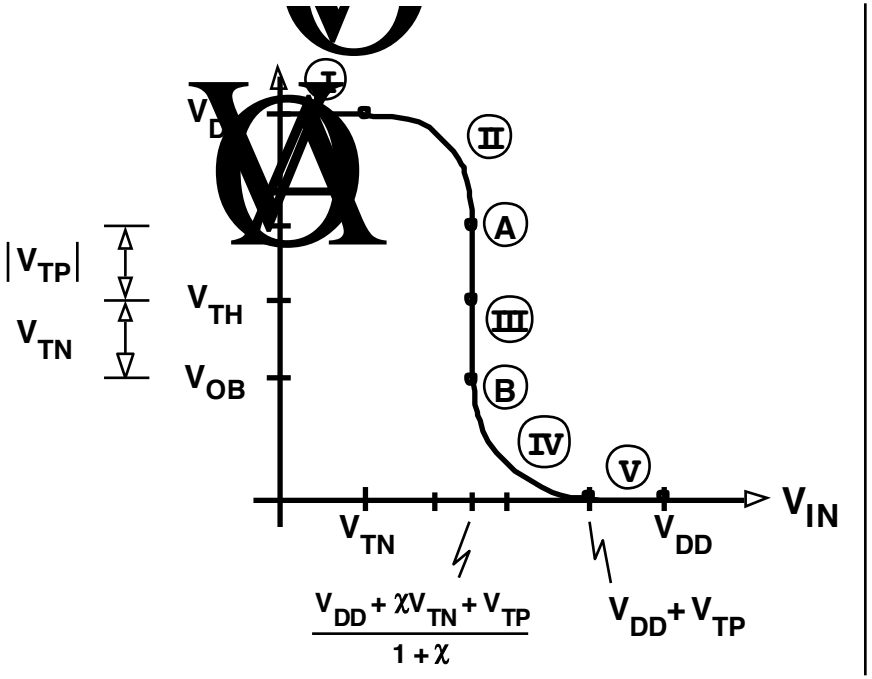
CMOS Inverter Load Line Characteristics



$$V_O = V_{DSN}$$
$$= V_{DD} + V_{DSP}$$
$$= V_{DD} - |V_{DSP}|$$

	I	N-CHANNEL OFF
A	II	N-CHANNEL SATURATED, P-CHANNEL LINEAR
A	III	N-CHANNEL SATURATED, P-CHANNEL SATURATED
B		(III EXISTS IF $V_A > V_B$)
B	IV	N-CHANNEL LINEAR, P-CHANNEL SATURATED
	V	P-CHANNEL OFF

CMOS Inverter VTC



Equations for CMOS VTC

I. N-channel device off: $V_{in} \leq V_{TN} \;\; \therefore V_o = V_{DD}$

II. N-channel saturated, P-channel linear

$$I_{DP} = \frac{W_P}{L_P} \frac{\mu_e C_{ox}}{\left(1+\frac{V_{ds}}{E_c L}\right)} \left(V_{gs} - V_{TP} - \frac{V_{ds}}{2}\right) V_{ds}$$

Where $V_{gs} = V_{DD} - V_{in}$, $V_{ds} = V_{DD} - V_o$

$$I_{DN} = W_N \nu_{sat} C_{ox} \frac{(V_{gs} - V_{TN})^2}{(V_{gs} - V_{TN}) + E_c L_N}$$

Where $V_{gs} = V_{in}$, $V_{ds} = V_o$

Set $I_{DP} = I_{DN}$

III. N-channel saturated, P-channel saturated

$$I_{DN} = W_N \nu_{sat} C_{ox} \frac{(V_{gs} - V_{TN})^2}{(V_{gs} - V_{TN}) + E_c L_N} = W_P \nu_{sat} C_{ox} \frac{(V_{gs} - V_{TP})^2}{(V_{gs} - V_{TP}) + E_c L_P} = I_{DP}$$

Equations for CMOS VTC (cont'd)

IV. N-channel linear, P-channel saturated

$$I_{DN} = \frac{W}{L}\,\frac{\mu_e C_{ox}}{\left(1+\frac{V_{ds}}{E_c L}\right)}\,(V_{gs} - V_{TN} - \frac{V_{ds}}{2})V_{ds}$$ Where $V_{gs} = V_{in}$, $V_{ds} = V_o$

$$I_{DP} = W\nu_{sat}C_{ox}\,\frac{(V_{gs} - V_{TP})^2}{(V_{gs} - V_{TP}) + E_c L_P}$$ Where $V_{gs} = V_{DD} - V_{in}$, $V_{ds} = V_{DD} - V_o$

Set $I_{DP} = I_{DN}$

V. P-channel device off, $V_{in} = V_{DD}$, $V_o = 0$