EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 19: Pipelined ADC 1

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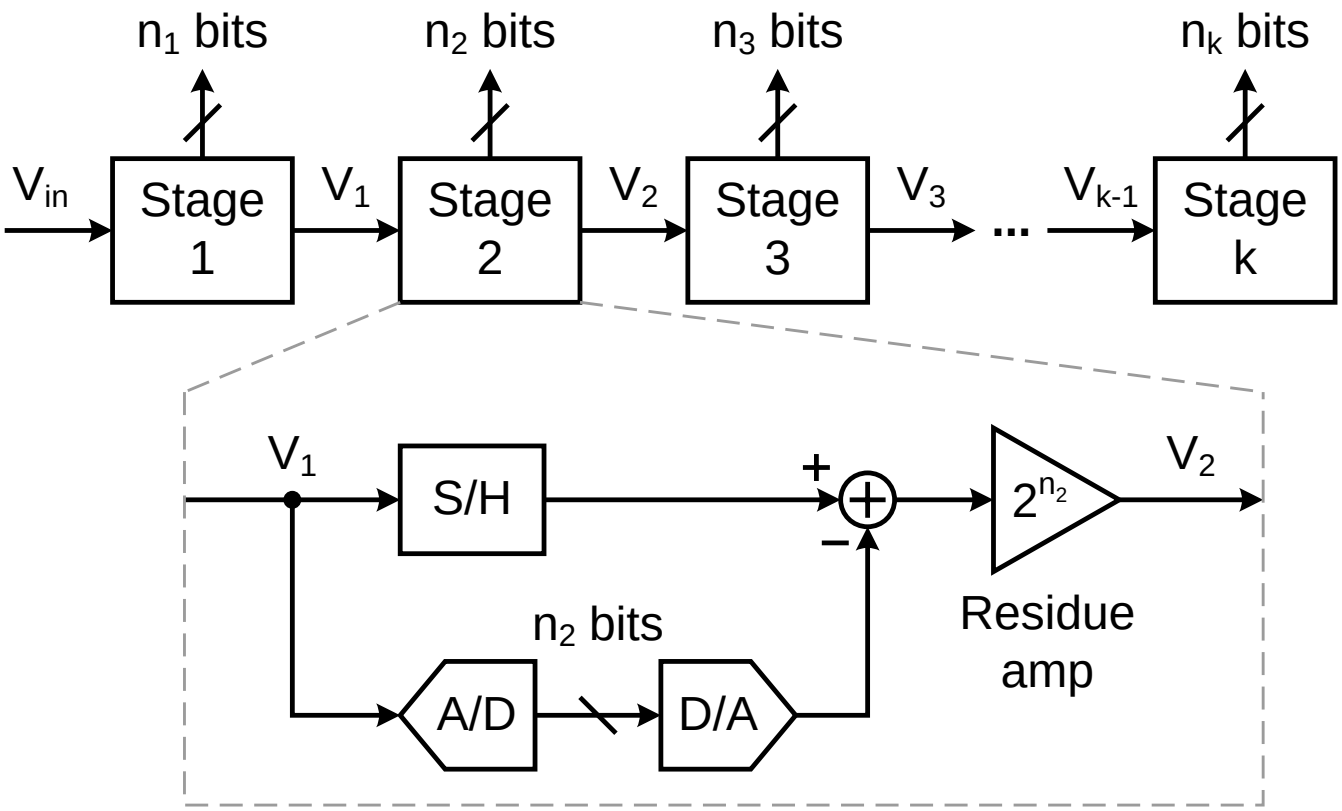
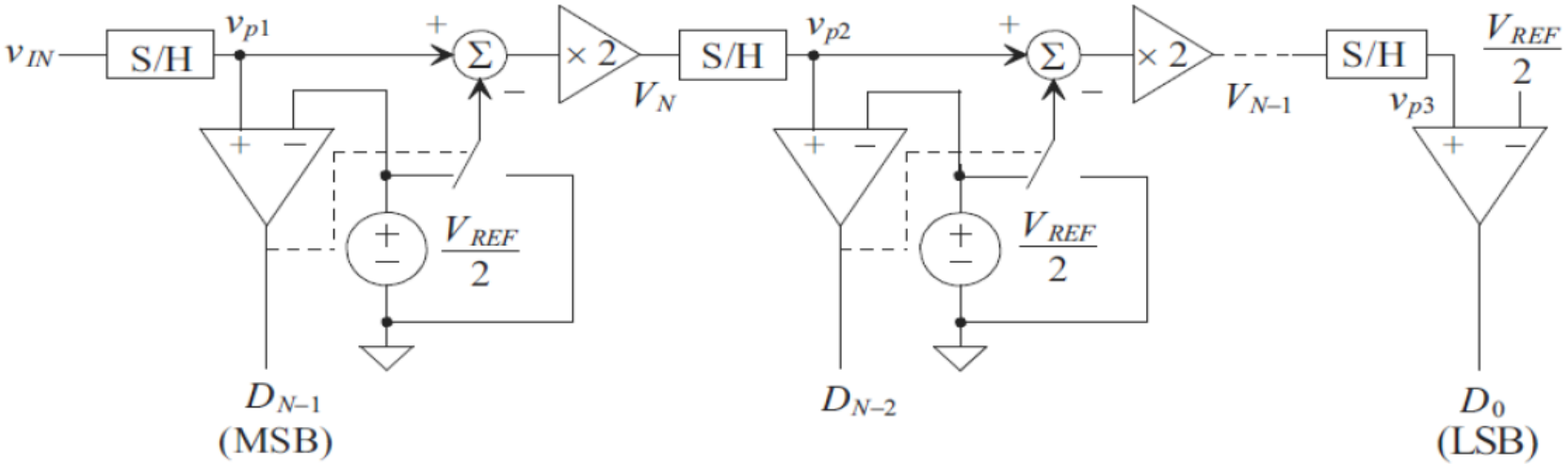
Pipelined ADC Architecture

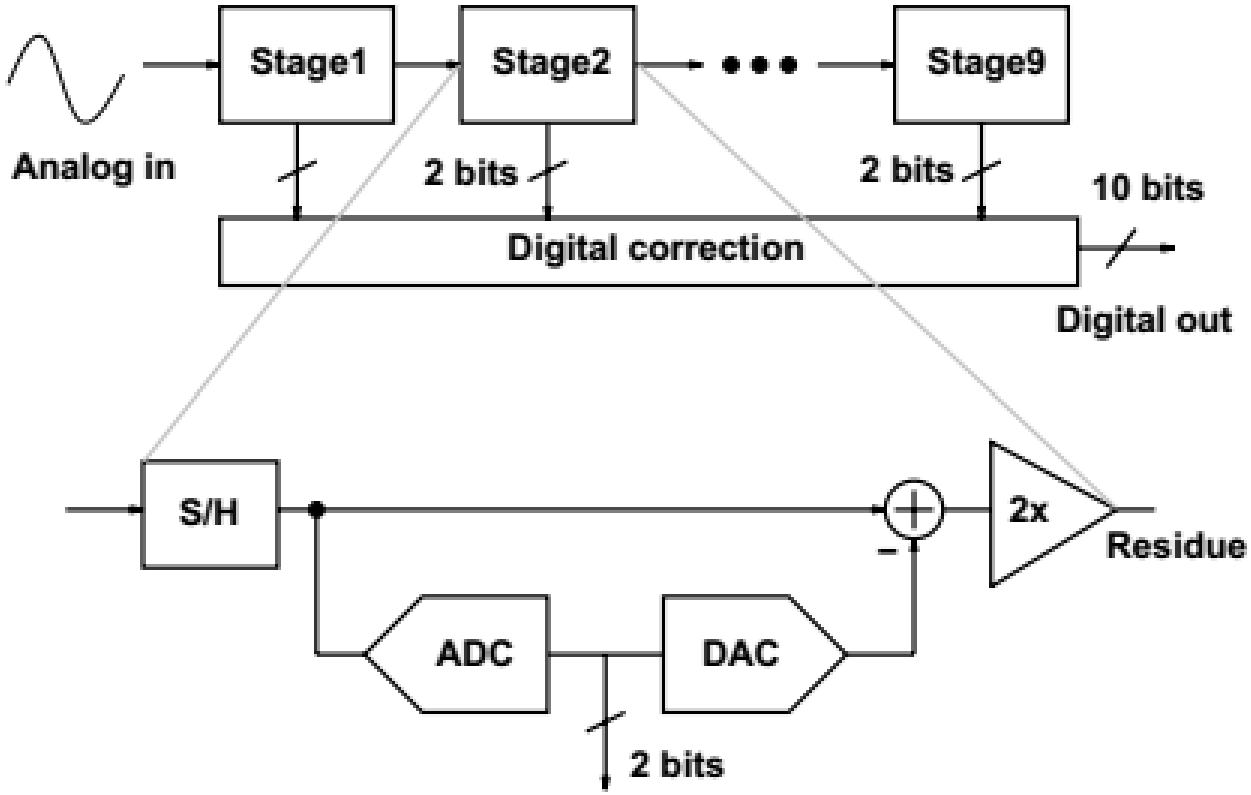


S. Lewis et. al., “A 10-b 20-Msample / s Analog-to-Digital Converter,” *IEEE Journal of Solid-State Circuits*, vol. 27, pp. 351-358, March, 1992.

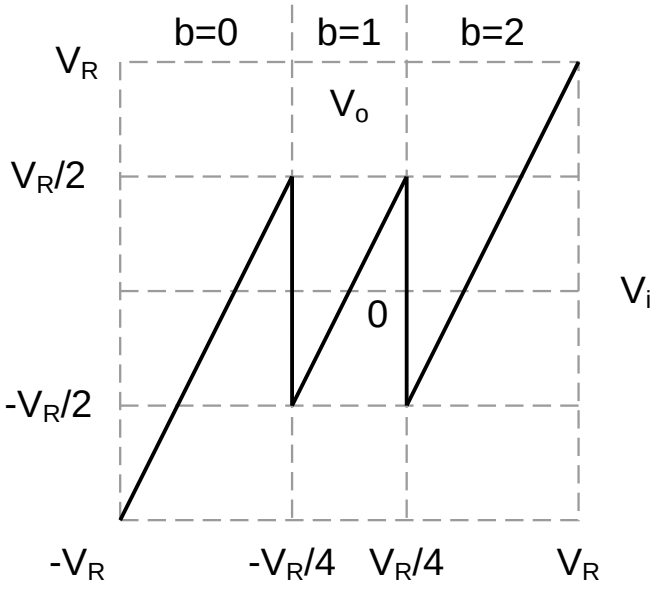
1-bit/stage Pipelined ADC

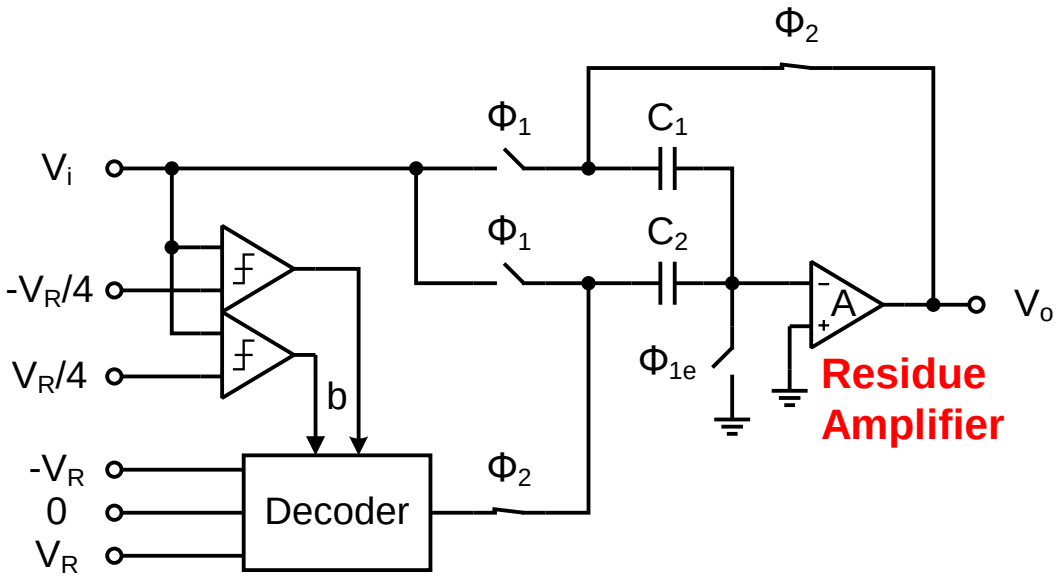


10-Bit Pipelined ADC (1.5-Bit/Stage) Architecture



1.5-Bit Per Stage

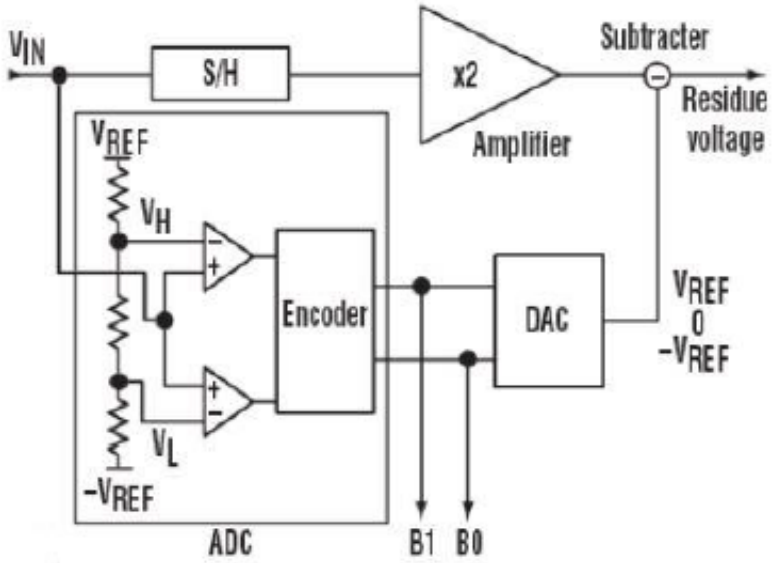


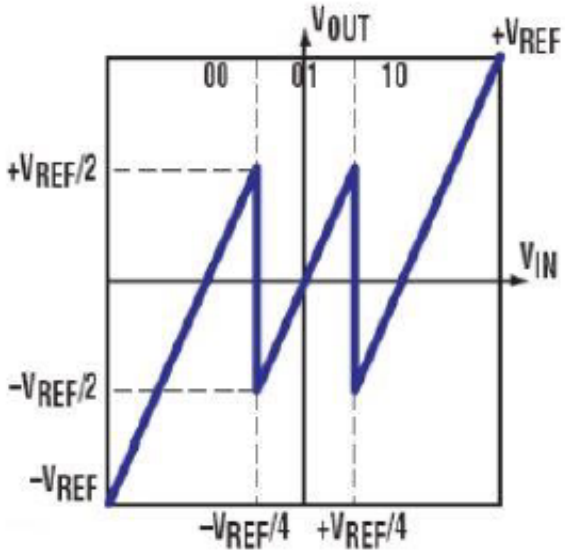


$$V_o = \begin{cases} 2V_i - V_{ref} & \text{if } V_i > V_{ref}/4 & d = 2\,(10)_2 \\ 2V_i & \text{if } -V_{ref}/4 \le V_i \le +V_{ref}/4 & d = 1\,(01)_2 \\ 2V_i + V_{ref} & \text{if } V_i < -V_{ref}/4 & d = 0\,(00)_2 \end{cases}$$

- 2X gain + 3-level DAC + subtraction all integrated
- Digital redundancy relaxes the tolerance on Comparator offsets

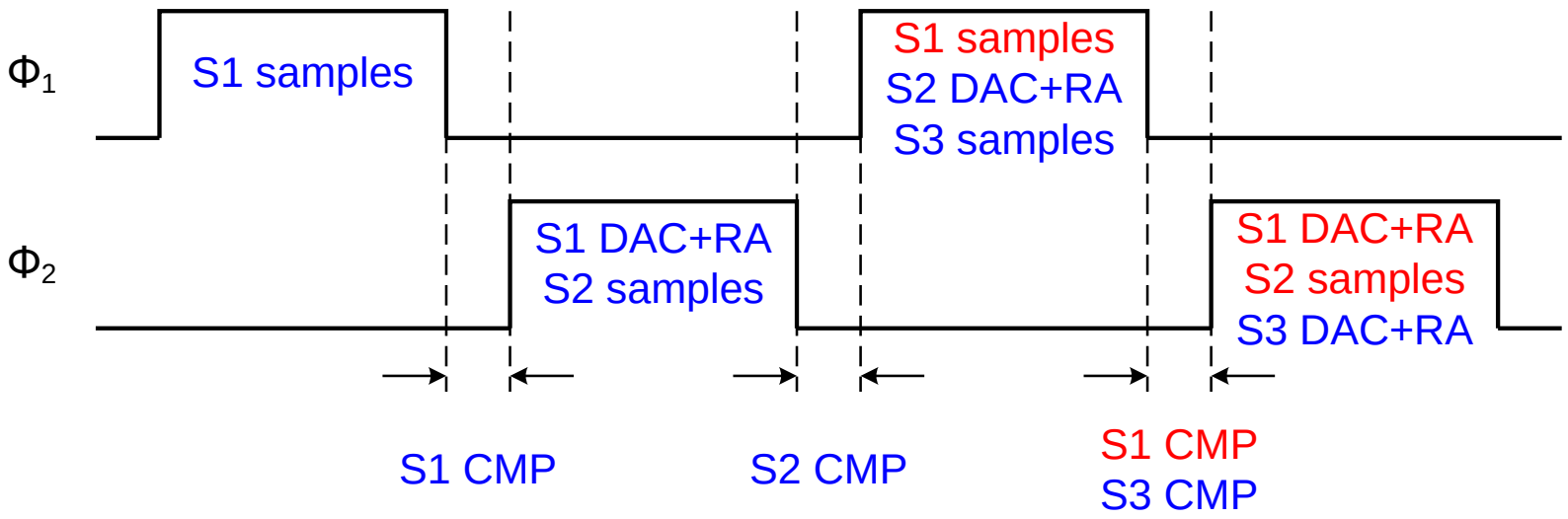
1.5-Bit Stage Architecture





V_{IN}	Range	B1	B0	DAC O/P	Residue
$V_{IN} > V_H$	H	1	0	$+V_{REF}$	$2V_{IN} - V_{REF}$
$V_L < V_{IN} < V_H$	M	0	1	0	$2V_{IN}$
$V_H < V_L$	L	0	0	$-V_{REF}$	$2V_{IN} + V_{REF}$

Timing Diagram of Pipelining



- Two-phase nonoverlapping clock is typically used, with the coarse ADCs operating within the nonoverlapping times
- All pipelined stages operate simultaneously, increasing throughput at the cost of latency