University of California
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WeFr 2-3:30pm

We, February 18, 2:00-3:30pm

EECS 141: SPRING 09—MIDTERM 1

NAME	Last First

SID	

Problem 1 (10):

Problem 2 (15):

Problem 3 (5):

Total (30)	

PROBLEM 1 DC Analysis (10 points)

A world-renowned researcher in Berkeley has recently invented a three-terminal device. She named it "volristor" — it is basically a resistor whose resistance is controlled by a voltage applied to its third terminal. Schematic symbol and R-V characteristic are shown in Fig. 1. Please note the polarity of the voltage defined in Fig. 1 ($V_{AB} = V_A - V_B$).

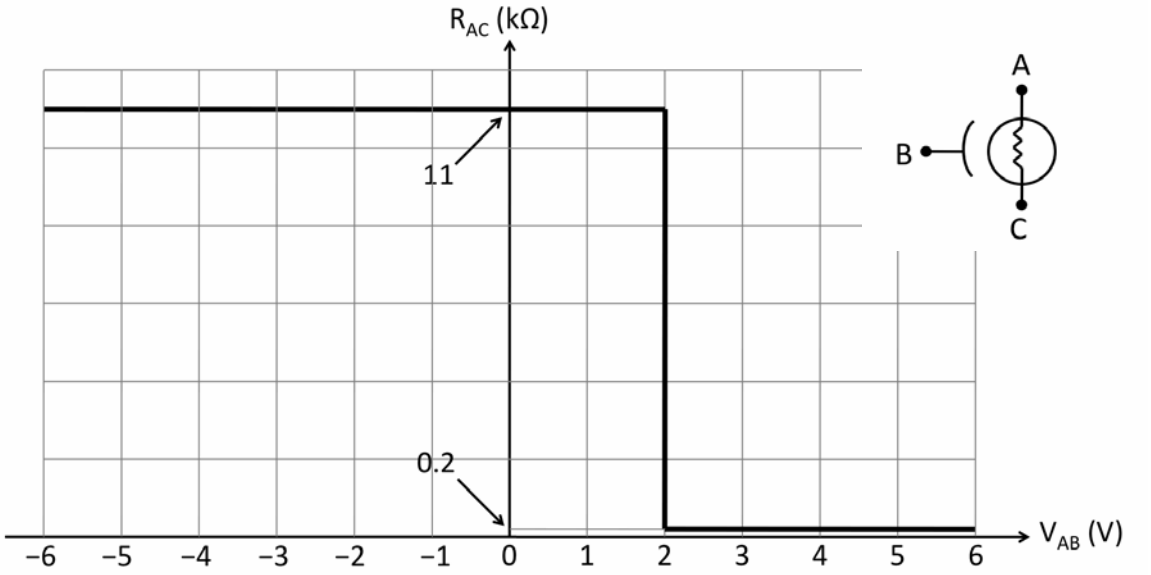


Figure 1 Schematic Symbol and R-V Characteristic of the New Device.

(1) One of last year's EE141 students played with the device and constructed a logic inverter as shown in Fig. 2. Sketch the voltage transfer characteristic (VTC) of this inverter in the space provided in Fig. 3. *(4 pts)*

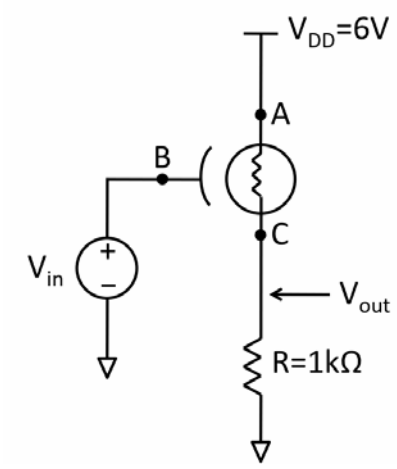


Figure 2 An Inverter that Employs the New Device.

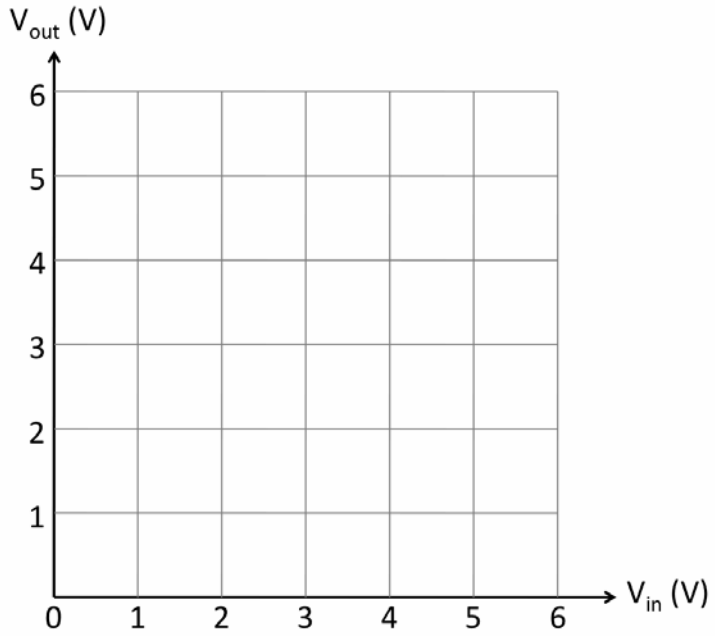


Figure 3 VTC of the Inverter in Fig. 2.

(2) Compute the noise margins (NM_H and NM_L) of the inverter in Fig. 2. *(3 pts)*

NM_H =
NM_L =

(3) You may have noted from the VTC plot that the inverter's threshold voltage V_M is away from $V_{DD}/2$. This is often undesirable for digital operations. To improve that, the EE141 student designed another inverter that incorporates a current source. Schematic of the new inverter is shown in Fig. 4. Amplitude of the current source I_S is 0.4mA. Design the value of the resistor R_X so that $V_M = V_{DD}/2$. *(3 pts)*

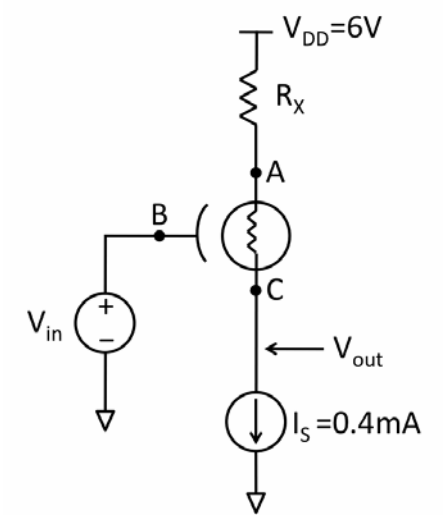


Figure 4 New Inverter Designed to Improve V_M.

R_X =

PROBLEM 2 – Logical Effort (15 Points)

Given the complex gate below:

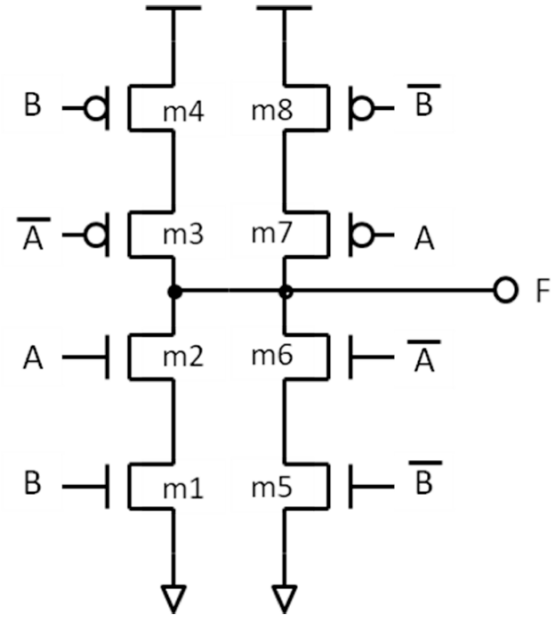


Figure 1 Complex gate.

(1) Draw the truth table and determine the logic function of the complex gate shown in Fig. 1. *(1 pt)*

F =

(2) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What is logical effort of this gate for each input (A, $\overline{A}$, B, $\overline{B}$)? *(3 pts)*

m1=m2= m5=m6=

m3=m4= m7=m8=

LE_A=

LE_B=

$LE_{\overline{A}}$=

$LE_{\overline{B}}$=

(3) Suppose we are only interested in the delay of the falling output transition **when both input A and input B are pulled high**. Size the transistor m1 and m2 to make the logical effort of this gate for the input A the same as a unit inverter. For transistors m3-m8, use the sizes you found in (2). (Use m3=m4…=m8=2 if you do not know the answer to part (2)) *(1 pt)*

m1=m2=

(4) Suppose we are only interested in the delay of the falling output transition **when both input A and input B are pulled high**. Assume we can arbitrarily choose the size of any transistor in this gate and the **only sizing constraint is m1=m2**. What are the maximum and minimum logical efforts we can achieve for the input A? *(2 pts)*

Max LE_A=

Min LE_A=

The designer finally settles on the relative transistor sizing shown in Fig. 2a (that is, all transistors are equal). This gate is used in the complex logic network shown in Fig. 2b (Really complex…☺). Assume the initial input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) equals (L, H, H, L), where L means logical low and H means logical high.

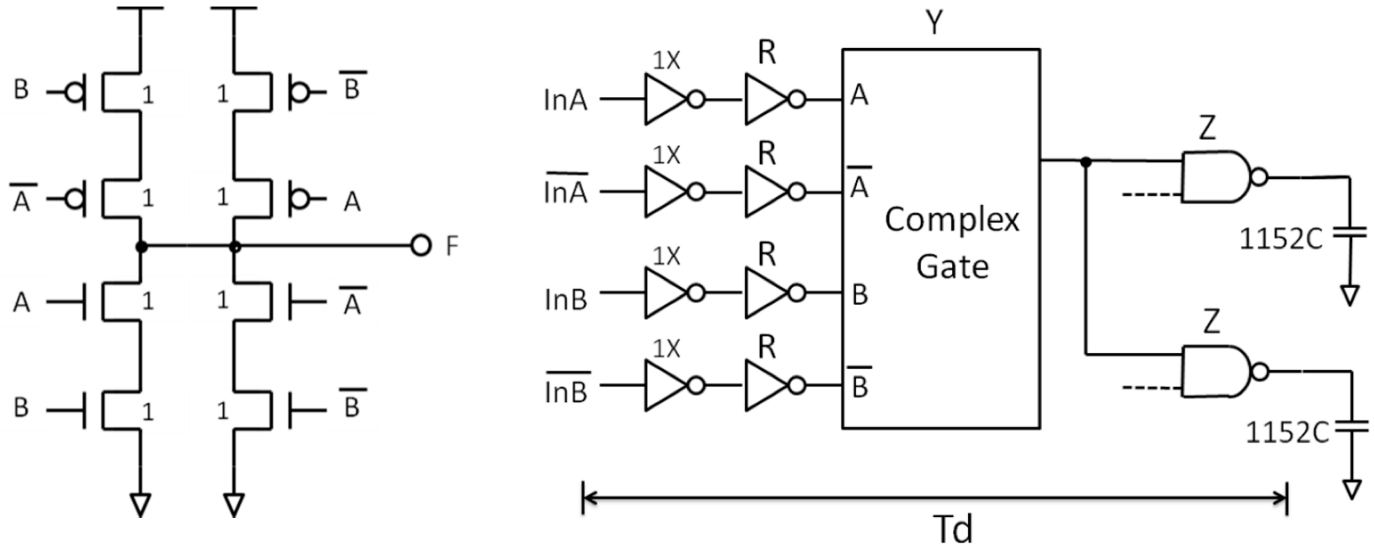


Figure 2: (a) Finalized transistor sizing; (b) Complex logic network.

(5) Size the inverter R, the complex gate Y, and the NAND Z to minimize the propagation delay Td_{11} from input to output when the input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) switches from (L, H, H, L) to (H, L, H, L). *(5 pts)*

R=

Y=

Z=

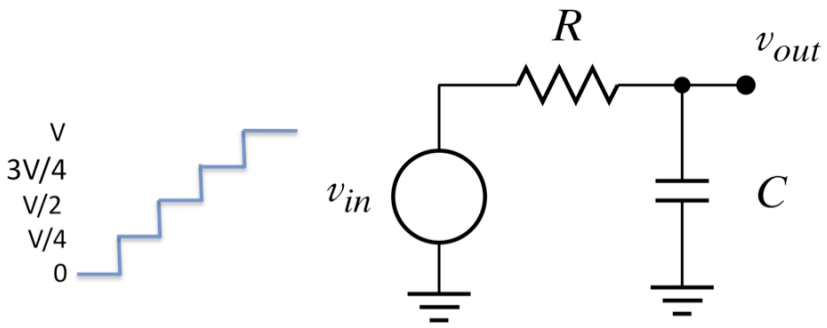
(6) Using the transistor sizes you found in (5), calculate the delay Td_{11}, and the propagation delay Td_{01} from input to output when the input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) switches from (H, L, H, L) back to (L, H, H, L). Assume $\gamma = 1$. *(3 pts)*

$Td_{11} =$ t_{p0}

$Td_{01} =$ t_{p0}

PROBLEM 3: Energy (5 pts)

A capacitor is charged using the input waveform shown in the Figure below.



a. Compute the total energy taken from the supply during the charging. Compare this to the case where the input would be raised from 0 to V in one step (3 Pts). NOTE: You may assume that the output voltage reaches steady state after every step.

E(small steps) =

E(one step) =

b. Estimate what the total energy consumption would be if the consecutive steps were made infinitesimally small. Explain. (2 Pts)

E(very small steps) =