UNIVERSITY OF CALIFORNIA, BERKELEY
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Due Friday, February 26 , 5pm, box in 240 Cory

[PROBLEM 1] Capacitive Coupling

Fig.1 shows a circuit that has two interconnect lines with a large coupling capacitance between them. (35 pts)

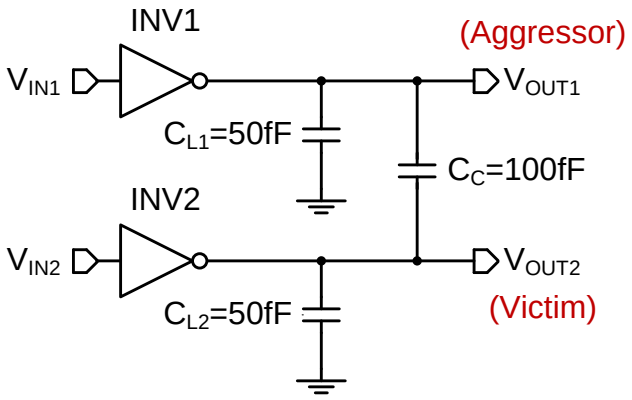


Fig.1.

(a) Estimate the peak value of noise on the victim line when the aggressor line switches by 1.2V with zero rising time? The aggressor is V_{OUT1}, and the victim is V_{OUT2}. Assume that V_{OUT2}=0, i.e. V_{IN2}=1.2V initially. Ron of nMOS, $R_{ON,n}$, and pMOS, $R_{ON,p}$, in INV2 is 1MΩ. (5 pts)

If the aggressor switches by,

$$\Delta V_A = 1.2V$$

then the peak value of noise on the victim line will be,

$$\Delta V_V = \frac{C_C \Delta V_A}{(C_{L2} + C_C)} = \frac{(100fF)(1.2V)}{(50fF + 100fF)} = 0.8V$$

(b) What is the delay from V_{IN1} rising to V_{OUT1} falling with step input of V_{IN1} when V_{IN2}=V_{DD}(no transition)? How much energy is **drawn from supply** in this case? Assume that Ron of nMOS, $R_{ON,n}$, and pMOS, $R_{ON,p}$, in each inverter is equal to 1kΩ. (10pts)

Delay = ln(2) * R_{ON} * (C_{L1} + C_C) = ln(2)*1k*150fF = 103.97pS

Either i) or ii) will be given full credit if the process and the answer is right.

i) Energy drawn from supply:

E_{SUPPLY} = None

ii) Energy dissipated in the circuit

$E_{DISS} = ½ * (C_{L1} + C_C) * V_{DD}^2 = ½ * 150fF * 1.2^2 = 108fJ$

(c) What is the delay from V_{IN1} rising to V_{OUT1} falling when V_{IN2} transits from 0 to V_{DD} at the same time as VIN1? How much energy is **drawn from supply** in this case? Assume that Ron of nMOS, $R_{ON,n}$, and pMOS, $R_{ON,p}$, in each inverter is equal to 1kΩ. (10pts)

$Delay = ln(2) * R_{ON} * C_{L1} = ln(2)*1k*50fF = 34.66pS$

Either i) or ii) will be given full credit if the process and the answer is right.

i) Energy drawn from supply:

E_{SUPPLY} = None

ii) Energy dissipated in the circuit: two inverters dissipate energy.

$E_{SUPPLY} = ½ * C_{L1} * V_{DD}^2 *2 = ½ * 50fF * 1.2^2 *2 = 72fJ$

(d) What is the worst case delay, or maximum delay, from V_{IN1} to V_{OUT1}? What is energy **drawn from supply** in this case? Assume that Ron of nMOS, $R_{ON,n}$, and pMOS, $R_{ON,p}$, in each inverter is equal to 1kΩ. (10pts)

$Delay = ln(2) * R_{ON} * (C_{L1} + 2*C_C) = ln(2)*1k*250fF = 173.28pS$

Either i) or ii) will be given full credit if the process and the answer is right.

i) Energy drawn from supply:

$E_{SUPPLY} = (C_{L1} + 2*C_C) * V_{DD}^2 = 250fF * 1.2^2 = 360fJ$

ii) Energy dissipated in the circuit: two inverters dissipate energy.

$E_{SUPPLY} = ½ * (C_{L1} + 2*C_C) * V_{DD}^2 *2 = ½ * 250fF * 1.2^2 *2 = 3600fJ$

[PROBLEM 2] Inverter and Wiring Delay

Fig.2. shows a pair of symmetrically sized inverters, Ron_nmos=Ron_pmos, driving a large capacitive load, CL=10pF, with input buffer having an output resistance of 1kΩ. The first inverter, INV1, is made of thin-oxide transistors and has an intrinsic delay of 20pS, tinv_thin. The second inverter, INV2, is made with thick-oxide transistors and has an intrinsic delay of 50pS, tinv_thick. Assume that a symmetrical, unit sized (size=1) inverter has input capacitance C_{ginv}=3fF and γ=1 (C_G=C_D) for both thin and thick oxide devices. (45pts)

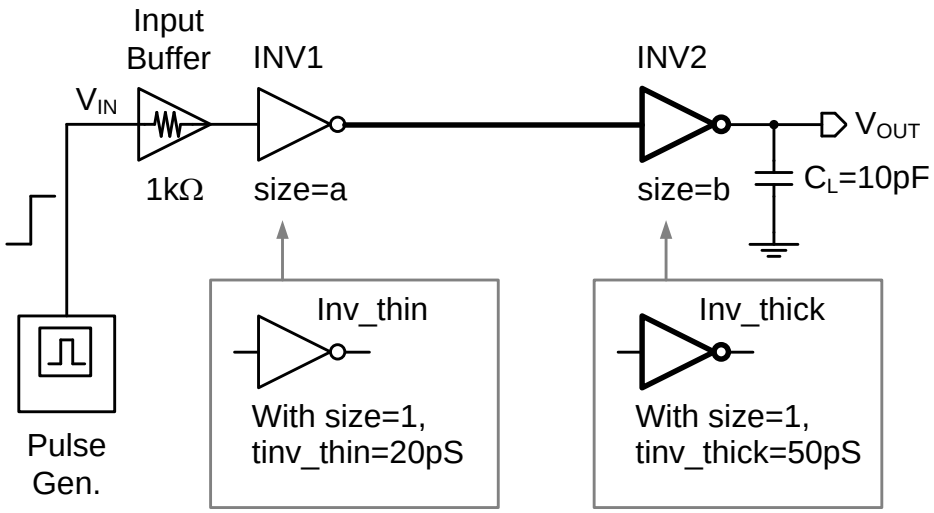


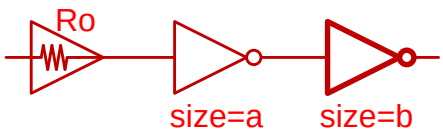
Fig.2.

(a) Find Cint, intrinsic or diffusion capacitance of a transistor, and Req, equivalent resistance of a transistor, for a unit size inverter (size=1) made of thin-transistors and for a unit size inverter (size=1) made of thick-oxide transistor. (i.e. Fine Cint_thin, Req_thin, Cint_thick, and Req_thick)

Cint_thin = γ * $C_{Gg,inv}$ = 3fF
tp_thin = 20pS = ln(2) * Req_thin * Cint_thin
∴ Cint_thin = 3fF, and Req_thin = 9.62kΩ

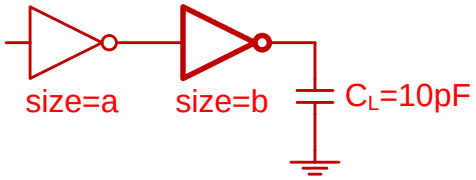
Cint_thick = γ * $C_{g,inv}$ = 3fF
tp_thick = 50pS = ln(2) * Req_thick * Cint_thick
∴ Cint_thick = 3fF, and Req_thick = 24.04kΩ

(b) Assume the size of INV2 is given as ‘b’. Find the size of INV1, a, in terms of b in order to minimize the overall delay from V_{IN} to V_{OUT}.



For minimum delay, each stage should have the same delay.
Ro * a * C_{ginv}_thin = (Req_thin / a) * (b * C_{ginv}_thick)
a^2 = (Req_thin / Ro) * (C_{ginv}_thick / C_{ginv}_thin) * b
a = sqrt[(9.62k/1k) * b] = 3.1 * sqrt(b)

(c) Assume the size of INV1 is given as ‘a’. Find the size of INV2, b, in terms of b in order to minimize the overall delay from V_{IN} to V_{OUT}.

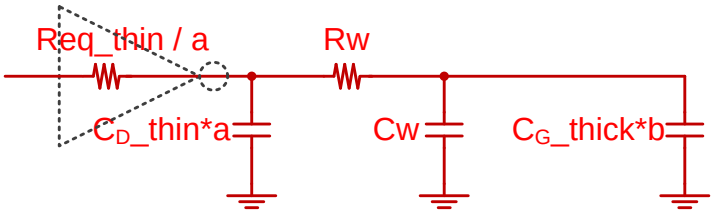


(Req_thin / a) * (b * C_{ginv}_thick) = (Req_thick / b) * C_L
b^2 = (Req_thick / Req_thin) * (C_L / C_{ginv}_thick) * a
b = sqrt[(24.04k/9.62k) * (10p / 3f) * a] = 91.27 * sqrt(a)

(d) From your answer (b) and (c), calculate ‘a’ and ‘b’.

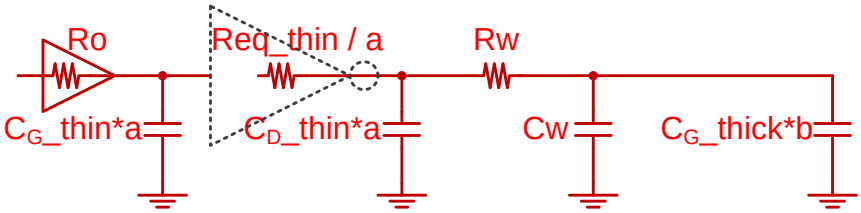
From (b), a = 3.1 * sqrt(b) → a^2 = 9.61b
From (c), b = 91.27 * sqrt(a) → b^2 = 8330a
b^4 = 8330^2 * 9.61 * b → b ≅ 874, a = sqrt (9.61*874) ≅ 92

(e) Due to the two inverters' position in the chip, the INV1 and INV2 are connected with metal-1 wire, 1mm long and 1um wide. Assume the wire is over field oxide with no other wire nearby. The sheet resistance of aluminum in metal-1 is 100mΩ/□, one side fringing capacitance from metal-1 to substrate is 40aF/um, and bottom plate capacitance is 30aF/um2.
Find the equivalent lumped element resistance and capacitance for this wire.
Sketch a schematic for a lumped RC model of the connection between the two inverters, including relevant capacitances and resistances from the inverters themselves.



□ of metal-1 wire = 1mm/1um = 1000
Rw = 1000 * 100mΩ/□ = 100Ω
Cpp = 1mm * 1um * 30aF/um2 = 30fF
Cfringe = 2 * 1mm * 40aF/um = 80fF
Cw = Cpp + Cfringe = 110fF

(f) Assume the size of the INV2 is given as 'b'. Find the size of the INV1, a, in terms of b that minimize the overall delay with wiring parasitic present.



t_{DELAY} = $\ln(2)*[R_O*a*C_{ginv}\_thin + Req\_thin/a*C_D\_thin*a + (Req\_thin/a + R_W)*(C_W + C_{ginv}\_thick)]$

$\partial t_{DELAY} / \partial a = \ln(2) * [Ro*C_{ginv}\_thin - Req\_thin*(C_W+C_{ginv}\_think*b)/a^2] = 0$

$a^2 = Req\_thin*(C_W+C_{ginv}\_think*b) / (Ro*C_{ginv}\_thin)$

$a^2 = 9.62k * (110f + 3f * b) / (1k * 3f)$ → $a = 1.79 * sqrt(110+3*b)$

[PROBLEM 3] MOS MODEL

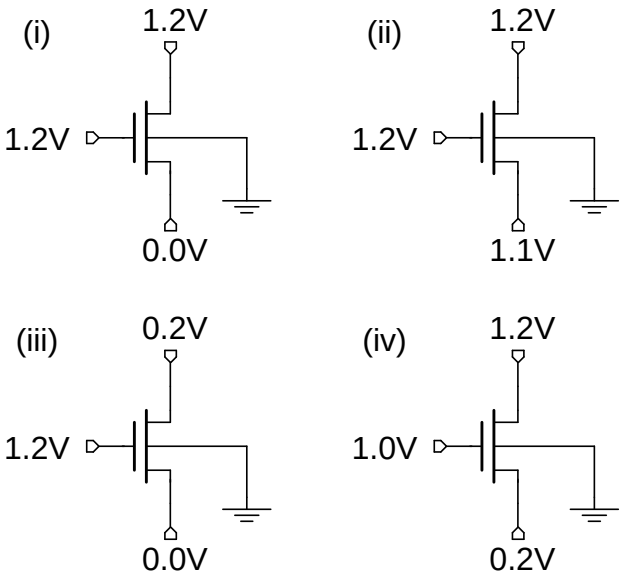


Fig.3.

(a) Find the region of operation for each transistor in Fig.3. Assume V_{TO}=0.4V.

i) Velocity Saturation

$V_{GT} = V_{GS} – V_{TO} = 1.2V-0.4V = 0.8V > 0$

$V_{DS} = 1.2$ V

$V_{D,VSAT} = Ec * L = 6$ V/um * 100nm = 0.6V (Unified Model)

(or $V_{D,VSAT}=1/(1+V_{GT}/Ec*L)*V_{GT}=1/(1+0.8/0.6)*0.8=0.43V$ (Velocity Saturation Model))

$V_{DS,eff} = \min(V_{GT},V_{DS},V_{D,VSAT}) = V_{D,VSAT}$

ii) Cutoff

$V_T = V_{TO}+\gamma*[\text{sqrt}(2*\phi_F+V_{SB})- \text{sqrt}(2*\phi_F)]$

$= 0.4+0.2*[\text{sqrt}(0.88+1.1)-\text{sqrt}(0.88)] = 0.494V$

$V_{GT} = V_{GS} – V_T = 0.1 – 0.494 < 0$

iii) Linear

$V_{GT} = V_{GS} – V_{TO} = 1.2V-0.4V = 0.8V > 0$

$V_{DS} = 0.2$ V

$V_{D,VSAT} = Ec * L = 6$ V/um * 100nm = 0.6V (Unified Model)

(or $V_{D,VSAT}=1/(1+V_{GT}/Ec*L)*V_{GT}=1/(1+0.8/0.6)*0.8=0.43V$ (Velocity Saturation Model))

$V_{DS,eff} = \min(V_{GT},V_{DS},V_{D,VSAT}) = V_{DS}$

iv) Saturation

$V_T = V_{TO}+\gamma*[\sqrt{(2*\phi_F+V_{SB})}- \sqrt{(2*\phi_F)}]$

$= 0.4+0.2*[\sqrt{(0.88+0.2)}-\sqrt{(0.88)}] = 0.42V$

$V_{GT} = V_{GS} – V_T = 0.8V-0.42V = 0.38V > 0$

$V_{DS} = 1.0$ V

$V_{D,VSAT} = Ec * L = 6$ V/um * 100nm = 0.6V (Unified Model)

(or $V_{D,VSAT}=1/(1+V_{GT}/Ec*L)*V_{GT}=1/(1+0.8/0.6)*0.8=0.43V$ (Velocity Saturation Model))

$V_{DS,eff} = \min(V_{GT},V_{DS},V_{D,VSAT}) = V_{GT}$

(b) Calculate the nMOS transistor current in each of the cases in Fig.3..

Use the following parameters if needed: V_{TO}=0.4V, E_C=6V/μm, L=100nm, W=400nm, v_{sat}=8X10^{6}cm/sec, C_{OX}=1.6X10^{-6}F/cm^2, un=270cm^2/V-sec, γ=0.2(V$^{1/2}$), 2|ϕ_F|=0.88V, λ=0.7V^{-1}.

i) Transistor is in the velocity saturation region.

I_{DS} = un*Cox*(W/L)*(V_{GT} – V_{DS_eff}/2)*V_{DS_eff}*(1+ λ*V_{DS})

= 270*1.6e-6*(400/100)*(0.8-0.6/2)*0.6*(1+0.7*1.2)

≅ 954uA (Unified Model)

Or I_{DS} = un*Cox*(W/L)/(1+$V_{D,VSAT}$/Ec*L)*(V_{GT} – $V_{D,VSAT}$/2)*$V_{D,VSAT}$*(1+ λ*V_{DS})

= 270*1.6e-6*(400/100)/(1+0.43/0.6)*(0.8-0.43/2)*0.43*(1+0.7*1.2)

≅ 466uA (Velocity Saturation Model)

ii) Transistor is in cutoff.

I_{DS} = I_{sub} or I_{DS} = 0 (if we ignore sub-threshold current).

iii) Transistor is in the linear region.

I_{DS} = un*Cox*(W/L)*(V_{GT} – V_{DS_eff}/2)*V_{DS_eff}*(1+ λ*V_{DS})

= 270*1.6e-6*(400/100)*(0.8-0.2/2)*0.2*(1+0.7*0.2)

≅ 276uA (Unified Model)

iv) Transistor is in the saturation region.

I_{DS} = un*Cox*(W/L)*(V_{GT} – V_{DS_eff}/2)*V_{DS_eff}*(1+ λ*V_{DS})

= 270*1.6e-6*(400/100)*(0.38-0.38/2)*0.38*(1+0.7*1.0)

≅ 212uA (Unified Model)