(Assignment 1/2, 100 Marks, Refer to Greensheet for Due Date, Due During Lecture)

Characteristics of the MOS Transistors

Use schematic composer, Spectre simulator and calculator in the Cadence CAD tool (as well as hand calculation if required) for this assignment. Submit your formal report including graphs, in 2-column IEEE format, in the classroom and put all your hand write-up into an appendix at the end of your report. Informal reports lose 50 marks and late reports lose 10 marks daily.

- using "tar xvzf nwsoi2nm.tgz" command, untar the model library into your Linux account at SJSU. Using the provided model library outside EE network is absolutely prohibited. Study the contents of the library and read the included documentation carefully.
- Run Cadence by "virtuoso" command. Open the "library manager" from the "tools" menu of the "virtuoso" window. You should be able to see some standard predefined libraries in Cadence including "analogLib", "sgfet" and "ee223" in the "library manager". Select the "ee223" library and then create a new composer schematic "cell view" called "tb_nmos_IV". A new blank schematic window will appear. The objective is to create the following test bench, shown in Fig. 1, to measure the IV transfer characteristics of the nmos transistors.

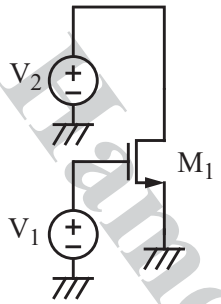
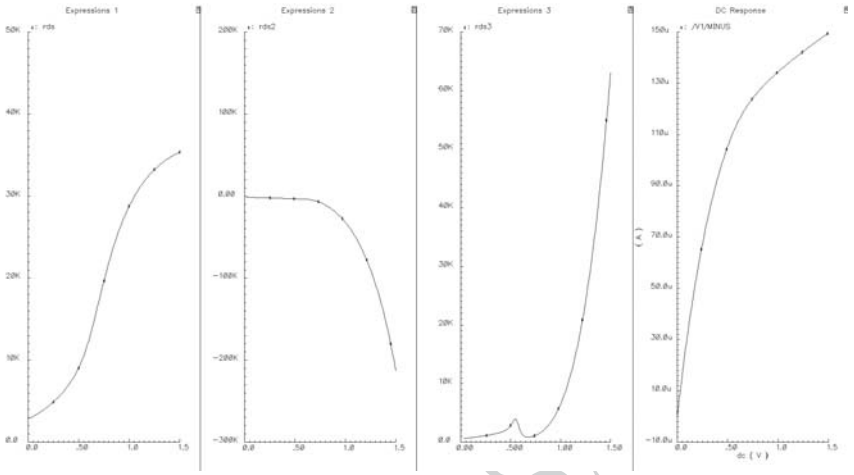


Fig. 1: Test Bench To Characterize IV Curves of an NMOS Transistor

- Use transistors from "sgfet" library and "vdc" and "gnd" symbols from "analogLib" library to create the test bench. You can insert instances to the "tb_nmos_IV" schematic cell view, place wires between different nodes, name wires, move, copy and change the properties of instances by using the "Add" and "Edit" menus of the Schematic Composer. After the test bench is created, save your circuit from the "Design" menu of the Schematic Composer and if there is no error, run "Analog Design Environment" from the "Tools" menu of the Schematic Composer to start the simulation.
- When the "Analog Design Environment" window appears, select "spectre" simulator from "Setup" menu. Add "./models/spectre/sgfet.inc to the "Model Libraries" under "Setup" menu. Choose "dc" simulation from "Analyses" menu. Sweep the DC voltage of the V_2 source from 0 to 1V by 10mV linear increments. Edit the DC voltage of the V_1 to be the variable "a". Copy the variable "a" from Schematic Composer to Analog Design Environment using the "Variables" menu. Edit the variable "a" to be equal to 0.5V using "Variables" menu. Use "Parametric Analysis" from "Tools" menu and edit "a" to vary from 0 to 1V by 100mV linear increments. Select the drain current (click on drain node or click on the negative terminal of the voltage source connected to the drain) and gate-source

voltage (click on the gate wire) to be "saved" and "plotted" using the "Outputs" menu. Finally, select "netlist and run" from the "simulation" menu to get the output IV curves in the "Waveform" window.

- To plot the resistance r_{ds} from the output transfer characteristics (I_{DS} versus V_{DS}) of the nmos transistor use "Calculator" from "Tools" menu and press the "idc" button and then select the drain node of the transistor. Select the "deriv" from the "Special Functions" and then press the "1/x" button to obtain $r_{ds} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1}$. Open a new "Subwindows" from the "Window" menu of the "Waveform" screen, select the new window by clicking on it and then press the "plot" button of the "Calculator". Using calculator obtain the second and the third order inverse derivatives of the output IV curves.
- An example of simulation results from a different technology without parametric sweep is shown in Fig. 2 as a reference.



Note:

These and other following graphs are only samples and not from gpdk technology.

Fig. 2: I_{ds}, r_{ds} and its two derivatives Functions of V_{ds} for an NMOS Transistor

- Repeat above steps by sweeping the V_1 in "dc" analysis and stepping V_2 in "Parametric Analysis" to get the input IV curves.
- To plot transconductance g_m from the input transfer characteristics (I_{DS} versus V_{GS}) of the nmos transistor use "Calculator" from "Tools" menu and press the "idc" button and then select the drain node of the transistor. Select the "deriv" from the "Special Functions" to obtain $g_m = \frac{\partial I_D}{\partial V_{GS}}$. Open a new "Subwindows" from the "Window" menu of the "Waveform" screen, select the new window by clicking on it and then press the "plot" button of the "Calculator". Using calculator obtain the second and the third order derivatives of the input IV curves.
- Repeat above steps using a suitable test bench for a pmos transistor.
- What are the V_1 values which yield the maximum g_m for nmos and pmos transistors? Why g_m reaches to a maximum and then decreases?

- Finally, “Save State” in “cellview” from the “Session” menu of the “Analog Design Environment”. This will help you to jump start your new simulations by choosing the “Load State” or double clicking on the created cellview without repeating the steps required by “Analog Design Environment” to run the same simulation.
- You can import functions generated by the calculator into “Analog Design Environment” by selecting the “Setup” under the “Outputs” menu and by pressing the “Get Expression” button.