# IC RESISTORS

Lecture 1

Advanced Digital IC Design **Khosrow Ghadiri** 



- IC passive components modeling and fabrication
  - IC resistors
  - IC inductors
  - IC capacitors





 Discrete resistors: are made from wires wounded around a cylinder of carbon film layers.



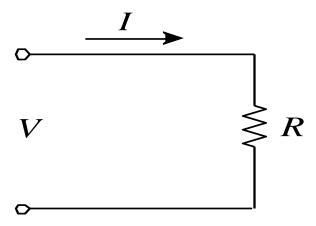
■ Integrated-circuit resistors: are made from doped semiconductors, polysilicon film and connected to each other or other part of IC circuit with metallization using good conductors like aluminum.





Resistors follow Ohm's law that states the resistance in ohm  $\Omega$  of resistors is directly proportional to voltage applied V in volts across the resistor and indirectly proportional to current, I in ampere flows through the resistor.

$$R = \frac{V}{I}$$



Resistance of a resistor is defined as a ratio of voltage across it over current through it.





• The Resistance is also directly related to resistivity  $\rho$  in  $\Omega-cm$  of the material of which the resistor is made of and its length L in Cm and indirectly proportional to its cross sectional area  $A=x_iW$  in .

$$R = \rho \frac{L}{x_j W}$$



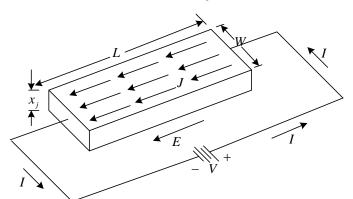


The resistivity is also inversely proportional to the conductivity.

$$\rho = \frac{1}{\sigma}$$

The electric field:

$$E = \frac{V}{L}$$



The drift current density

$$J = J_n \left( drift \right) + J_p \left( drift \right) = qn\mu_n E + qp\mu_p E = q \left( n\mu_n + p\mu_p \right) \frac{V}{L}$$

The drift current

$$I = J.A = q(n\mu_n + p\mu_p)\frac{V}{L}(Wx_j) = q(n\mu_n + p\mu_p)\frac{Wx_j}{L}V$$

The resistance can be rewritten in terms of sheet resistance as

$$R = \frac{V}{I} = \frac{1}{q(n\mu_n + p\mu_p)x_j} \frac{L}{W} = R_S \frac{L}{W} = R_S N_S$$





The resistivity is also inversely proportional to the conductivity.

$$\rho = \frac{1}{\sigma}$$

• The sheet resistance is defined as a ratio of resistivity over junction depth  $X_i$  in integrated circuit,

$$R_{S} = \frac{\rho}{x_{i}} = \frac{1}{\sigma x_{i}}$$

- and expressed in  $\Omega/\Box$  .
- Resistance can be rewritten in terms of sheet resistance as

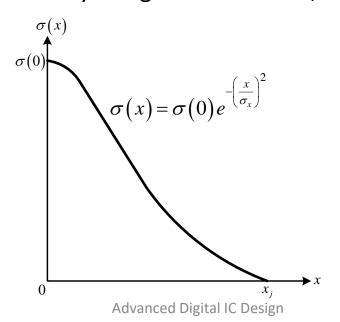
$$R = R_S \frac{L}{W} = R_S N_S$$

• Where  $N_S = L/W$  is the length-to-width ratio and is called the number of squares and is unit-less





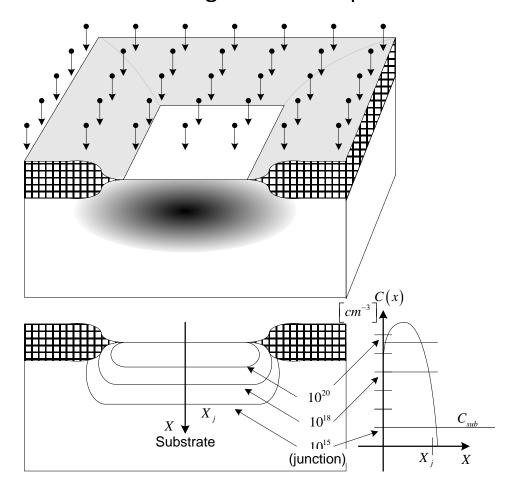
- Distribution models
  - Gaussian
  - Dual Pearson IV
  - Monte Carlo
- Resistivity  $\rho(x)$  is not uniform in integrated circuit. Resistivity is smallest at surface, increasing inside the material due to diffusion, or stating in another way, conductivity is highest at surface, reducing inside material.







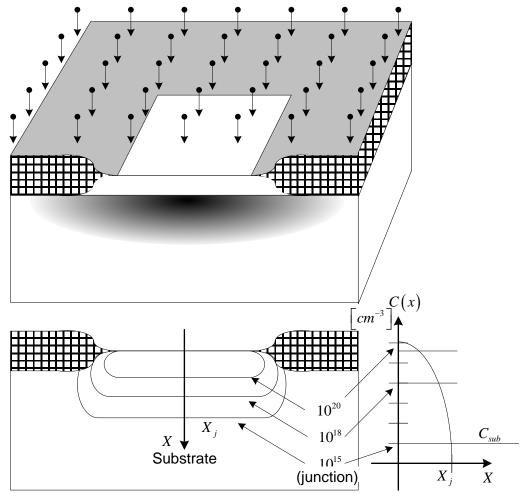
Gaussian distribution resulting from ion implantation







Gaussian distribution resulting from annealing

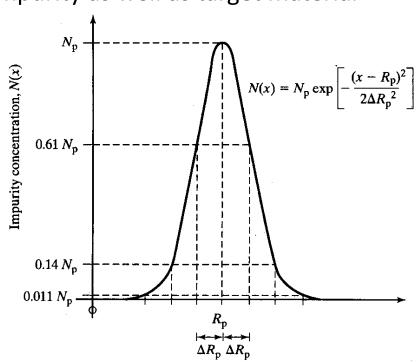






- Impurity Concentration profile
- Gaussian distribution resulting from ion implantation. The impurity is shown implanted completely below the wafer surface x = 0
- The projected range, or expected vale which is function of the ion energy plus mass and atomic number of impurity as well as target material

$$R_p$$
 = Projected range  $\Delta R_p$  = Straggle = standard deviation  $N_p$  = The peak concentration @  $x = R_p$   $Q = dose = \int_0^\infty N(x) \, dx = \sqrt{2\pi} N_p \Delta R_p$   $N(x) = N_p e^{-\frac{(x-R_p)^2}{2\Delta R_p^2}}$   $N_p = \sqrt{2\pi} N_p \Delta R_p$ 







 The conductivity profile is a normalized Gaussian distribution resulting from ion implantation.

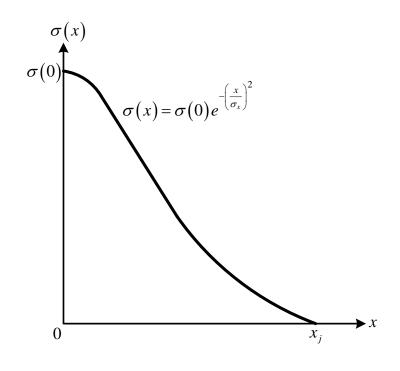
$$\sigma(x) = \sigma(0)e^{-\left(\frac{x}{\sigma_x}\right)^2}$$

- The expected value is zero
- The standard deviation is

$$\sigma_{\rm x}$$
 = standard deviation

The peak-value is

$$\sigma(x)$$
 = the peak conductivity @ x =0





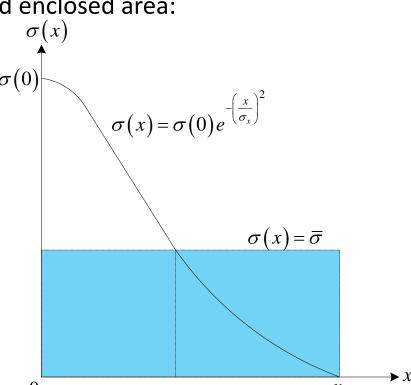


- The average conductivity is a single value for the conductivity that will provide the most suitable uniform conductivity approximation of the real conductivity dependence.
- The average conductivity  $\overline{\sigma}$  is shown in dashed line, can be found by equating the rectangular area  $\overline{\sigma}x$  and enclosed area:

$$\int_{0}^{x_{j}} \sigma(x) dx \simeq \int_{0}^{\infty} \sigma(x) dx$$

$$\bar{\sigma} \simeq \frac{1}{x_{j}} \int_{0}^{\infty} \sigma(x) dx$$

$$R_{S} = R_{\square} = 1/\bar{\sigma}x_{j}$$







- A single Pearson distribution P(x) is characterized by four parameters position of the peak  $R_P$ , the straggle  $\Delta R_P$ , the skewness which is indicating the tilting of the profile  $\delta$ , and kurtosis  $\beta$  which indicates the flatness at the top of the profile.
- The concentration

$$n(x) = n(0) \exp[P(x)]$$

The Pearson type IV

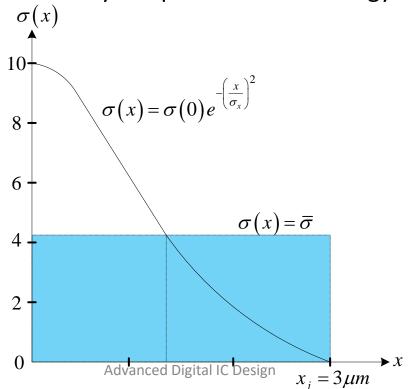
$$P(x) = \frac{1}{2b_2} \ln(b_2 x^2 + b_1 x + b_0) - \frac{\frac{b_1}{b_2} + 2a_0}{\sqrt{4b_2 b_0 - b_1^2}} \arctan \frac{2b_2 x + b_1}{\sqrt{4b_2 b_0 - b_1^2}}$$





### Problem:

- A) Find the average conductivity for the layer shown in figure, given the standard deviation is  $\sqrt{2}$
- $\blacksquare$  B) Design a  $100k\Omega$  resistor using this layer, given the minimum dimension achievable by the particular technology is  $~^{1}\mu m$  .







### Solution:

A) The average conductivity:

$$\bar{\sigma} = \frac{10(\Omega - cm)^{-1}}{3\mu m} \int_0^\infty e^{-\frac{x^2}{2}} dx$$

The so called Laplace integral is:

$$\int_0^\infty e^{-\frac{x^2}{2}} dx = \sqrt{\frac{\pi}{2}} \mu m$$

Then the average conductivity is:

$$\bar{\sigma} = \frac{10(\Omega - cm)^{-1}}{3\mu m} \left(\sqrt{\frac{\pi}{2}}\mu m\right) = 4.18(\Omega - cm)^{-1}$$

B) The sheet resistance:

$$R_s = R_{\Box} = \frac{1}{\overline{\sigma}x_j} = \frac{1}{4.18(\Omega - cm)^{-1} \times 3 \times 10^{-4} cm} = 797.4\Omega/\Box$$

$$\frac{L}{W} = \frac{R}{R_s} = \frac{100,000}{797.4} = 125 \implies L = 125W = 125\mu m$$



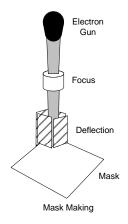


- The fundamental unit of IC manufacturing: Silicon wafer.
- The typical wafer diameter: 20 cm in 1990's, \$50.00, 150 chips.
- The maximum wafer diameter: 30 cm in 2014.
- Development of 45 cm wafer is in horizon.
- A lot: A group of around 24 wafers undergoes the same sequence of fabrication process.
- DRAM: 200 steps
- A typical complex IC chip area: 1.5cmX1.5cm
- A typical IC: Several millions electronic devices
- A typical cost of wafer: \$2000.00.
- The yield of mature process: how many of the chip work: %90
- A typical IC package: In plastic Dual-in-line (DIP)/ Wire bonds
- A typical IC for cellular phone/laptop package: encapsulated in low-profile surface mount package or mount directly mounted on the circuit board using a flip-chip technique/ Electroplated solder bumps.



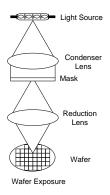


- Photolithography can be divided into three steps:
  - Design using CAD system
    - Layout
    - Simulation
    - Design Rule Verification
  - Mask making





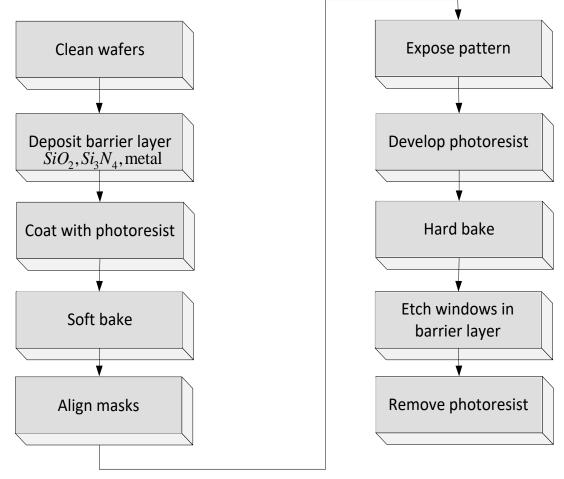
- Wafer exposure
  - The patterns transfer form mask to photo resist
  - Chemical or plasma etching to transfer the
  - pattern from the photo resist to burrier material
  - on the surface of wafer.







The various steps of basic photolithographic process





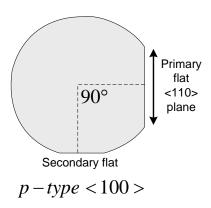


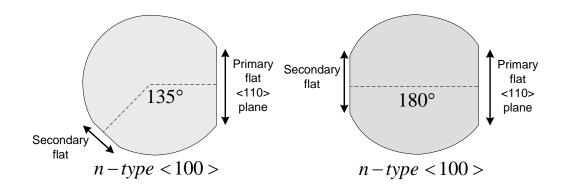
- n or p-type silicon wafer are available with a specified resistively
- Typically the growing crystal is doped with boron, phosphorous or arsenic. Arsenic and antimony is used for low resistively (high concentration) n-type crystal.
- The thickness  $250 \mu m \le t \le 500 \mu m$
- The diameter  $200mm(8 \text{ inch}) \le d \le 300mm(12 \text{ inch})$  (wafers with diameter of 1,1.5,2,3,4,5 and 6 inches have been used at various stages in history of solid state devices).
- The diameter of wafer is chosen in order to withstand the mechanical and thermal strain during the process steps. (for example a 6 to 8 inch diameter semiconductor wafer needs to be about  $500 \mu m$  thick.

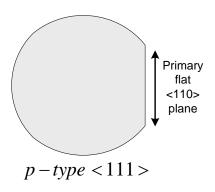


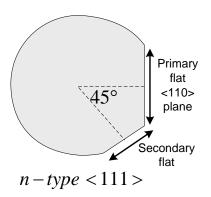


Schematic of a simple lithographic exposure system





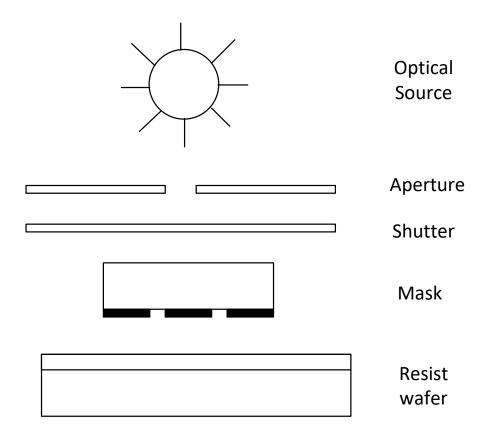








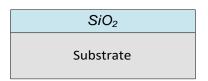
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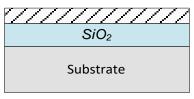




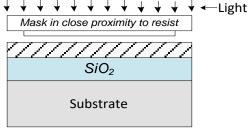
Schematic of a simple lithographic exposure system



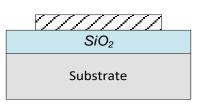
1) Silicon dioxide barrier layer growth



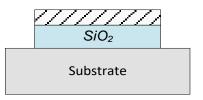
2) Application of photoresist



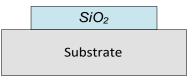
3) Close proximity printing



4) Substrate following resist exposure



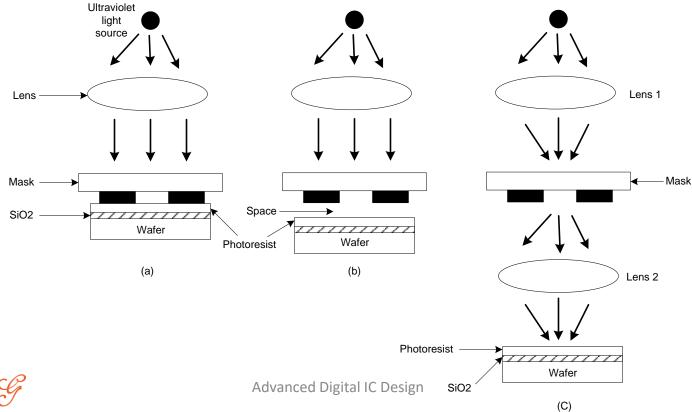
5) Substrate following etching SiO2



6) Substrate following resist removal



- (a) Contact printing, in which wafer is in intimate contact with mask,
- (b) proximity printing, in which wafer and mask are in close proximity
- (c) projection printing, in which light source is scanned across the mask and focused on the wafer.







The resistivity is also inversely proportional to the conductivity.

$$\rho = \frac{1}{\sigma}$$

The sheet resistance is defined as a ratio of resistivity P over junction depth  $X_i$  in integrated circuit,

$$R_S = \frac{\rho}{x_j} = \frac{1}{\sigma x_j}$$

- and expressed in  $\Omega/cm$
- Resistance can be rewritten in terms of sheet resistance as

$$R = R_S \frac{L}{W} = R_S N_S$$

• Where  $N_{\rm S}=L/W$  is the length-to-width ratio and is called the number of squares





The Sheet resistance for frequently used materials in IC.

MATERIAL	THICKNESS $(x_j)$	SHEET RESISTANCE
n <sup>+</sup> -Polysilicon	500 nm	$R_{\rm S}=20\Omega/cm$
Aluminum	1000 nm	$R_S = 0.07 \Omega/cm$
Silicided polysilicon		$R_{S} = 5 \Omega/cm$
Silisided source/drain diffusion		$R_S = 3\Omega/cm$





- The Change from run-to-run, chip-to-chip is largely due to ion-implanter.
- The doping concentration  $N_D$  can be expressed as:

$$N_D = \overline{N}_D \left( 1 \pm \varepsilon_{N_D} \right)$$

- Where  $\overline{N}_D$  is the average doping and is the normalized uncertainty.
- For example:

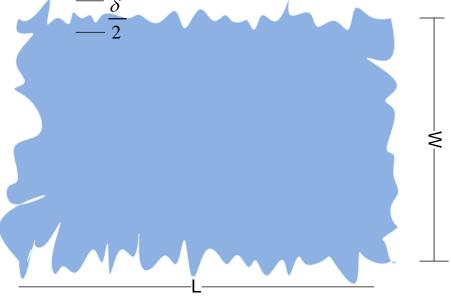
Doping concentration defined by an average of  $\bar{N}_{D}=10^{17}\,cm^{-3}$  and normalized uncertainty of  $\varepsilon_{ND}=0.025$  means that

$$Nd = (10^{17} cm^{-3})(1 \pm 0.025) = 10^{17} \pm 2.5 \times 10^{15} cm^{-3}$$





- Mobility Variation are due to random local variation in Crystal defects
- Ignoring Coupling between doping concentration and mobility variation
- The resistor thickness  $x_j$  variation is due to time and local wafer temperature variation during the furnace annealing process
- The lateral dimensions of the resistor are affected by random linewidth variations from the pattern transfer processes.
- The uncertainty on one edge is defined as  $\delta/2$







Sheet Resistance

$$W = \overline{W} \pm \delta/2 \pm \delta/2 = \overline{W} \pm \delta$$
$$L = \overline{L} \pm \delta/2 \pm \delta/2 = \overline{W} \pm \delta$$

Uncertainty from each edge:

$$W = \overline{W} \left( 1 \pm \delta / \overline{W} \right) = \overline{W} \left( 1 \pm \varepsilon_W \right)$$
 $L = \overline{L} \left( 1 \pm \delta / \overline{L} \right) = \overline{L} \left( 1 \pm \varepsilon_L \right)$ 
 $E_W = \delta / \overline{W}$ 
 $E_L = \delta / \overline{L}$ 

$$\overline{R} = \frac{1}{q\overline{N}_{D}\left(1 + \varepsilon_{N_{D}}\right)\overline{\mu}_{n}\left(1 + \varepsilon_{\mu_{n}}\right)\overline{\chi}_{j}\left(1 + \varepsilon_{x_{j}}\right)} \left[\frac{\overline{L}\left(1 + \varepsilon_{L}\right)}{\overline{W}\left(1 + \varepsilon_{W}\right)}\right]$$





- Sheet Resistance
- The average resistance

$$\overline{R} = \frac{1}{qN\overline{d}\,\overline{\mu}_n\overline{\chi}\,j} \left(\frac{\overline{L}}{\overline{W}}\right)$$

Substitution for each term that is subject to manufacturing is

$$\overline{R} = \frac{1}{q\overline{N}_{D}\left(1 + \varepsilon_{N_{D}}\right)\overline{\mu}_{n}\left(1 + \varepsilon_{\mu_{n}}\right)\overline{\chi}_{j}\left(1 + \varepsilon_{x_{j}}\right)} \left[\frac{\overline{L}\left(1 + \varepsilon_{L}\right)}{\overline{W}\left(1 + \varepsilon_{W}\right)}\right]$$

The average resistance

$$\varepsilon_{R} = \sqrt{\varepsilon_{N_{D}}^{2} + \varepsilon_{\mu_{n}}^{2} + \varepsilon_{x_{j}}^{2} + \varepsilon_{L}^{2} + \varepsilon_{W}^{2}}$$

Uncertainty up to 0.1

