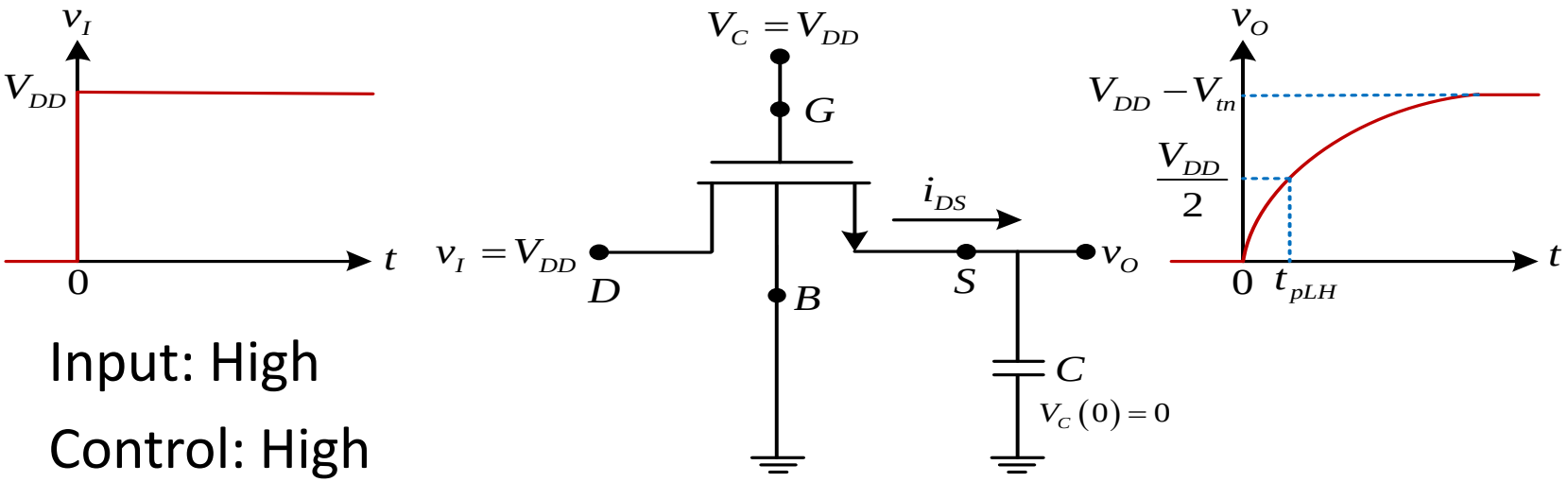
Transmission Gate

Lecture 9

- nMOSFET pass
- nMOS: Switch
- V_C : control voltage
- C: Total capacitance between output node and ground

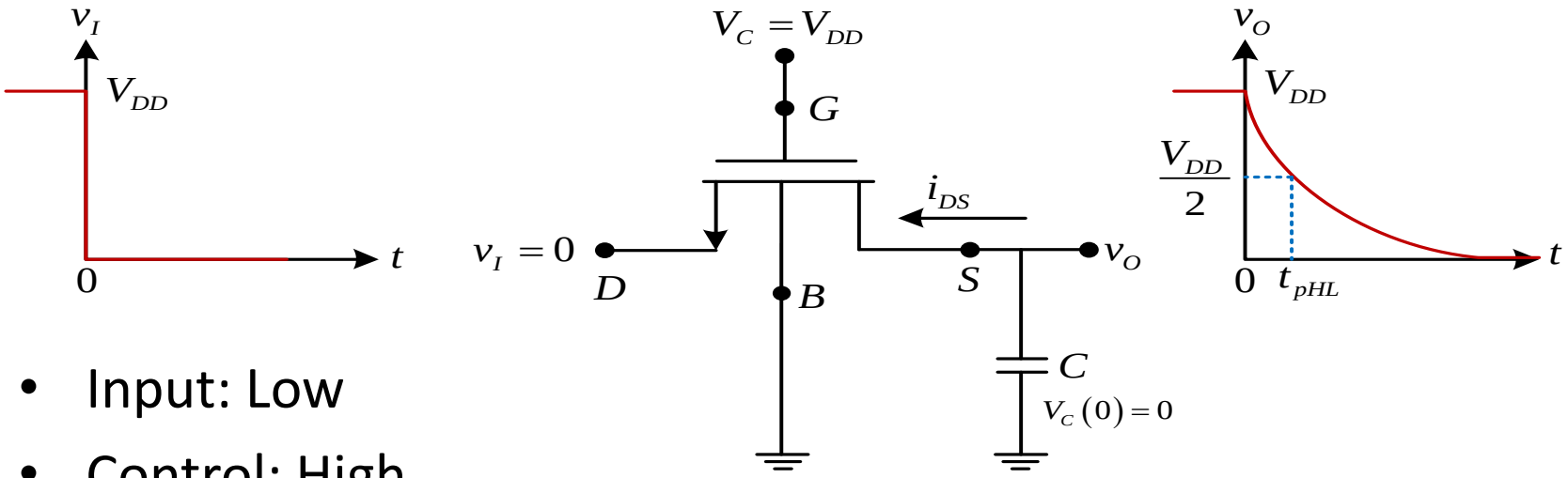


- Input: High
- Control: High
- Capacitor: Charging
- Output: $V_{DD} - V_{tn}$

$$i_{DS} = \frac{1}{2} k_n \left(V_{DD} - v_O - V_{tn} \right)^2$$

$$V_{tn} = V_{tn0} + \gamma \left(\sqrt{v_O + 2V_F} - \sqrt{2V_F} \right)$$

- pMOSFET pass
- pMOS: Switch
- VC: Control voltage
- C: Total capacitance between output node and ground



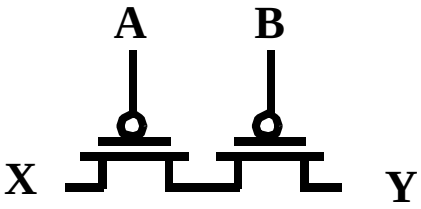
- Input: Low
- Control: High
- Capacitor: Discharging
- Output: 0

$$i_{DS} = \frac{1}{2} k_p \left(V_{DD} - V_{tp} \right)^2$$

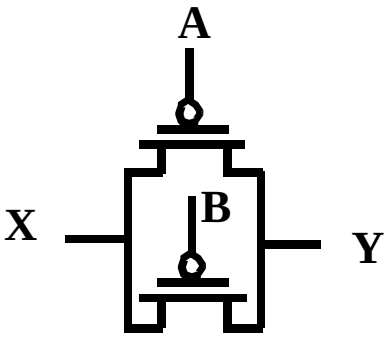
$$V_{tp} = V_{tp0}$$

- pMOSFET series and parallel connection

PMOS switch closes when switch control input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$

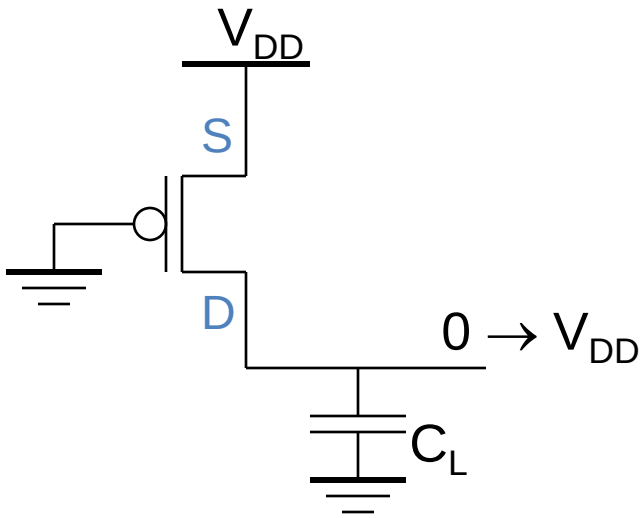


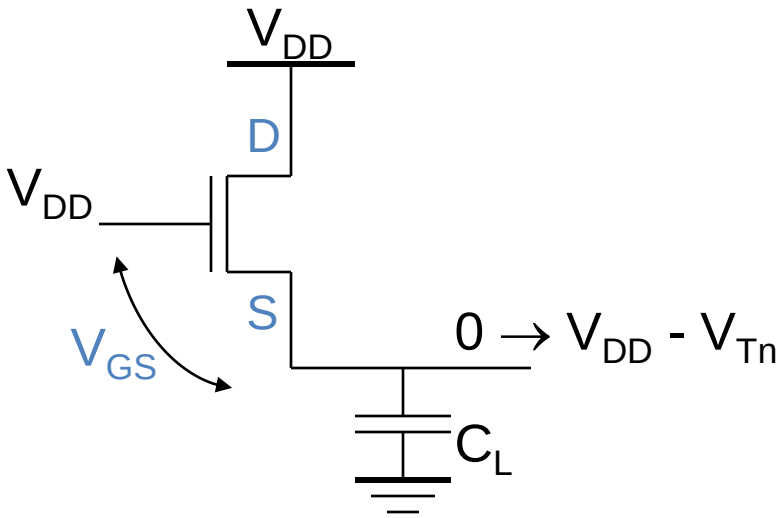
$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

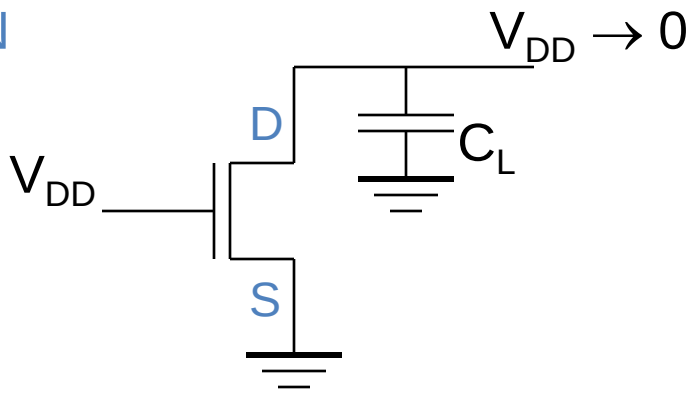
- Threshold drops:

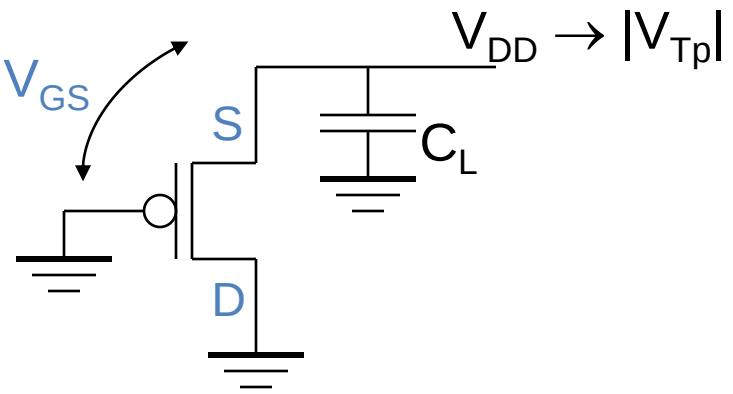
PUN





PDN



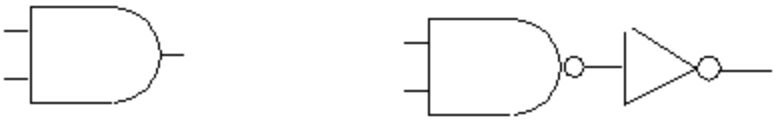


- Complementary CMOS logic Style
  - **PUP is the DUAL of PDN**
    (can be shown using DeMorgan's Theorem's)

$$\overline{A+B} = \bar{A}\bar{B}$$

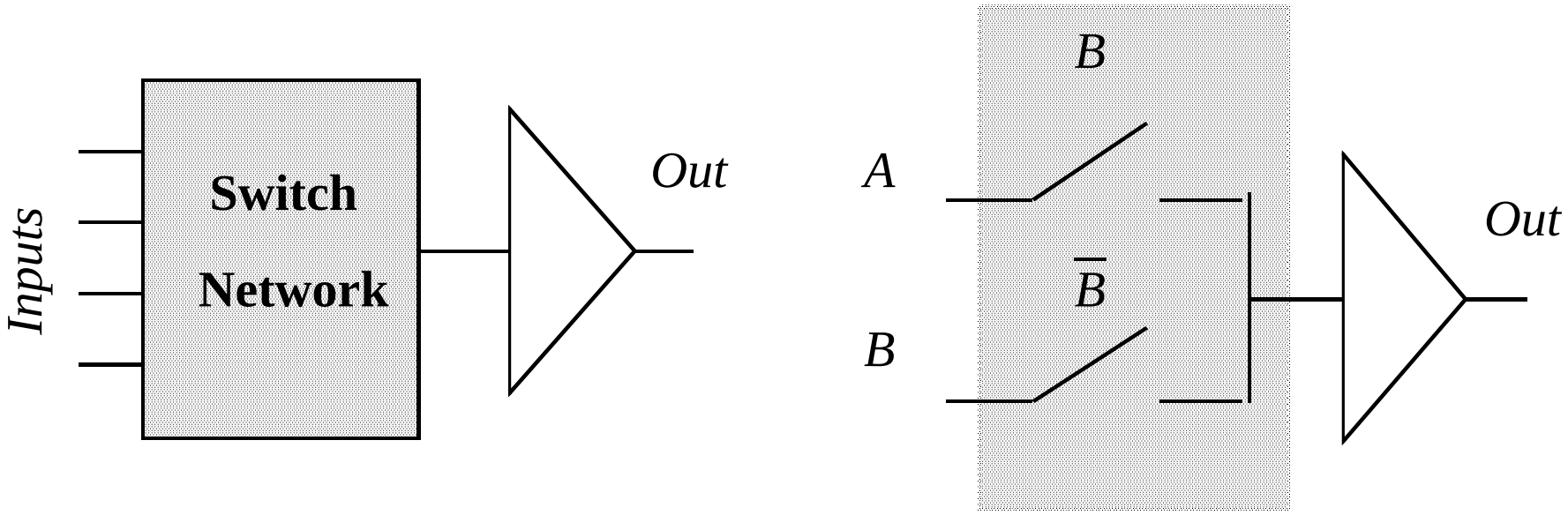
$$\overline{AB} = \bar{A}+\bar{B}$$

  - **The complementary gate is inverting**



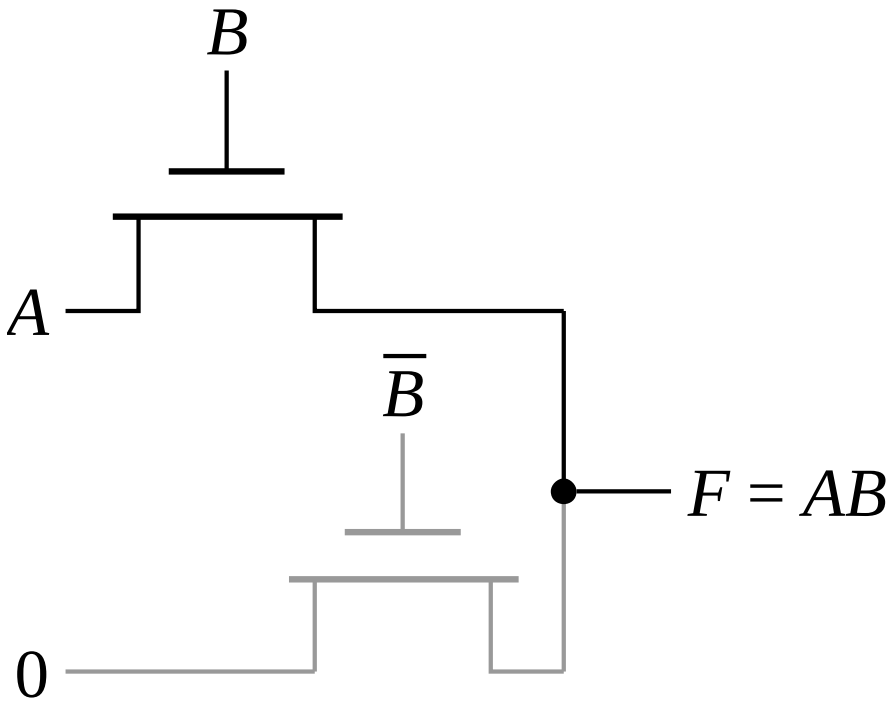
AND = NAND + INV

- Pass-transistor logic

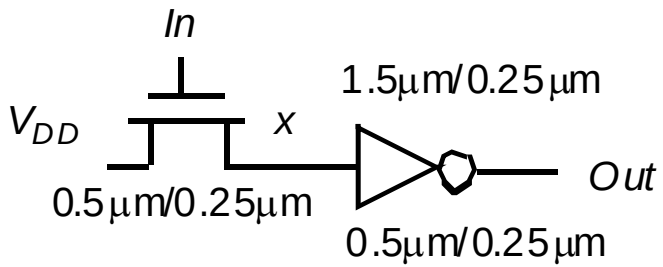


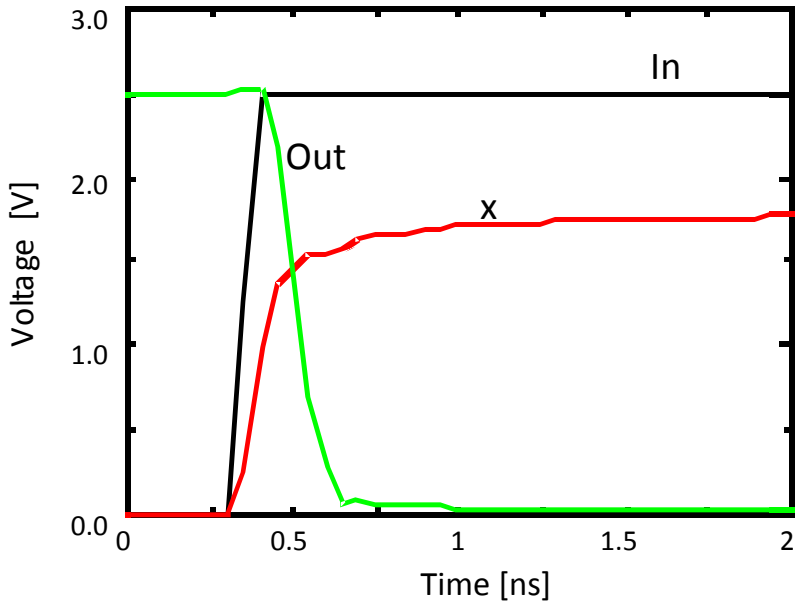
- **N transistors**
- **No static consumption**

- AND gate

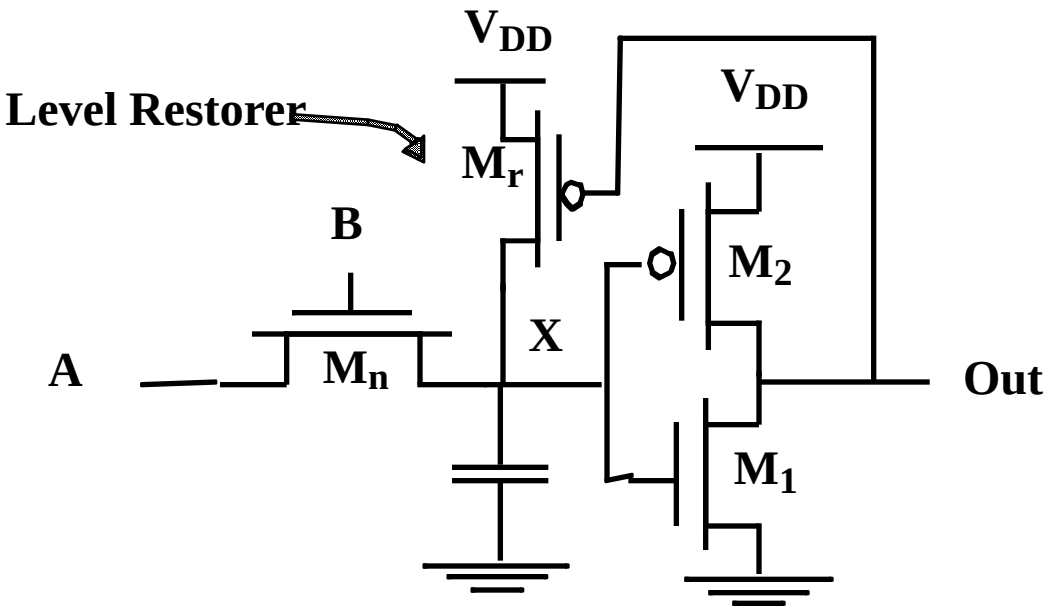


- nMOS-only logic



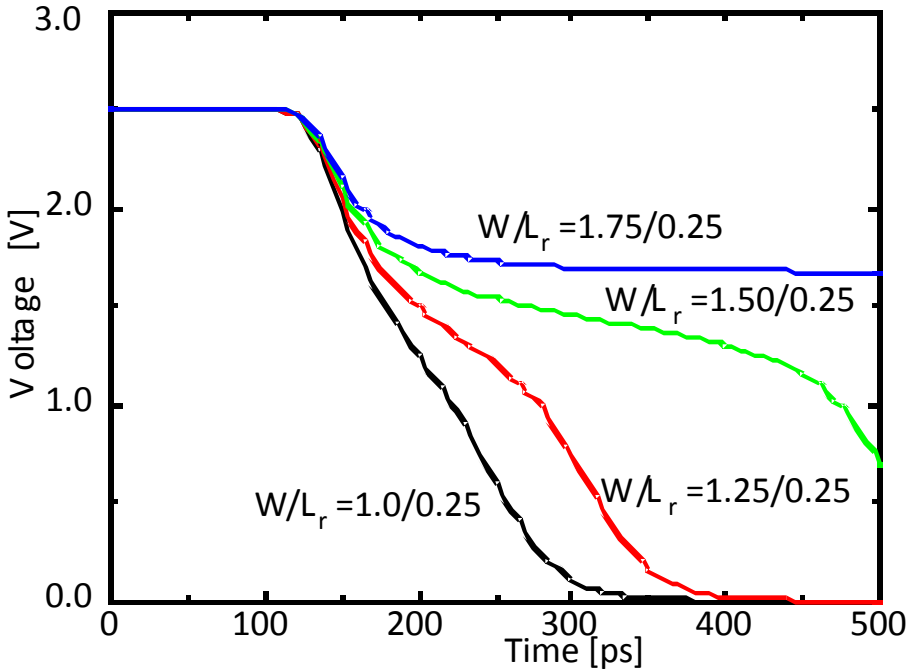


- nMOS-only logic level restoring transistor



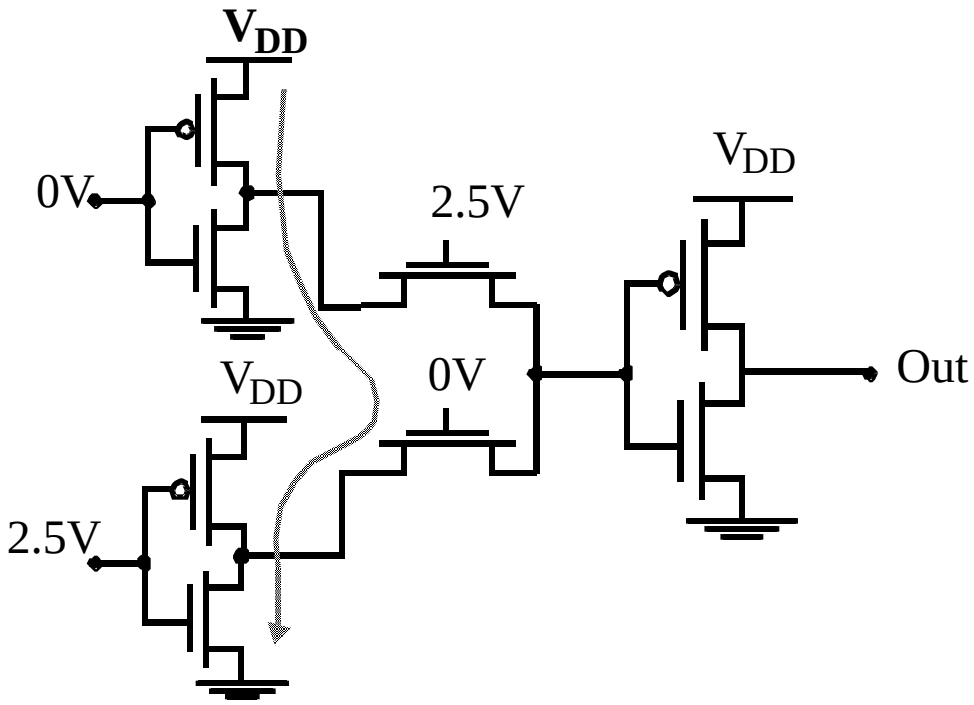
- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

- nMOS-only logic level restorer sizing



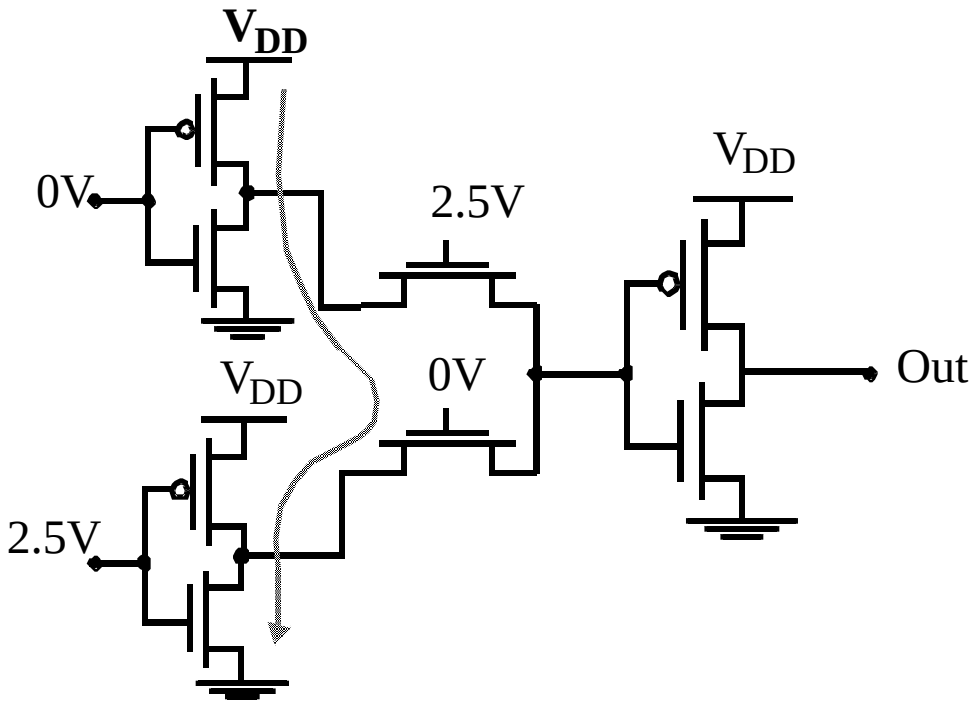
- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

- Single transistor pass gate with $V_T = 0$



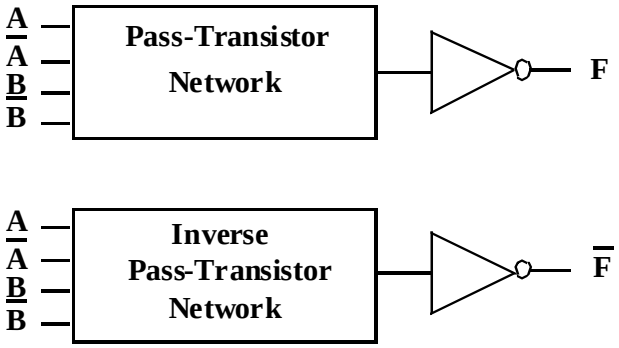
WATCH OUT FOR LEAKAGE CURRENTS

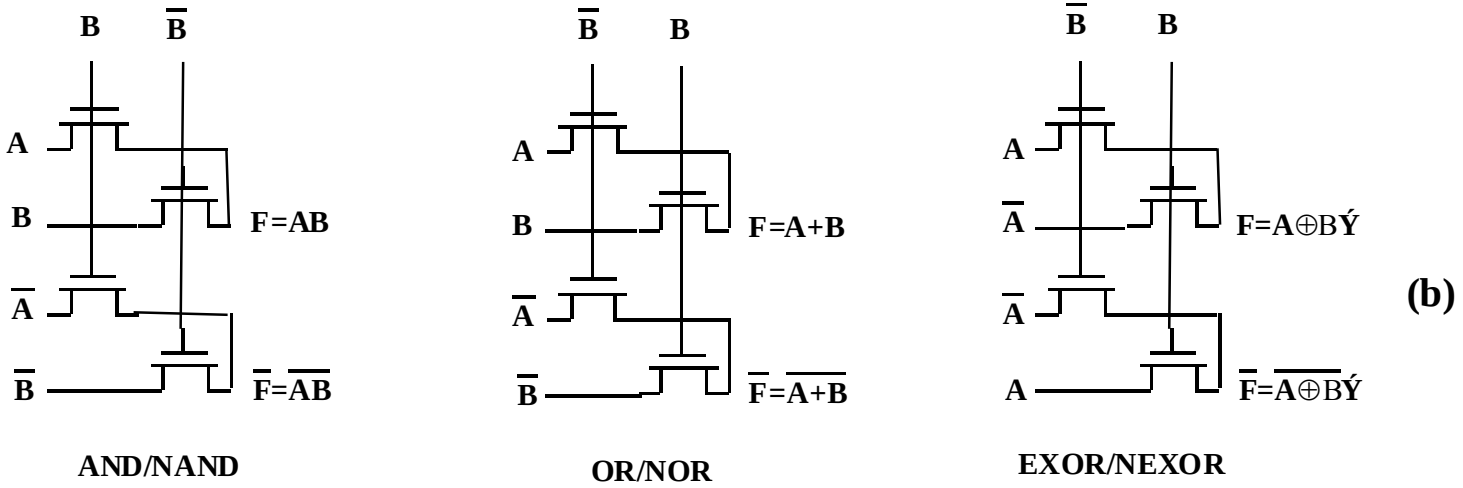
- Single transistor pass gate with $V_T = 0$



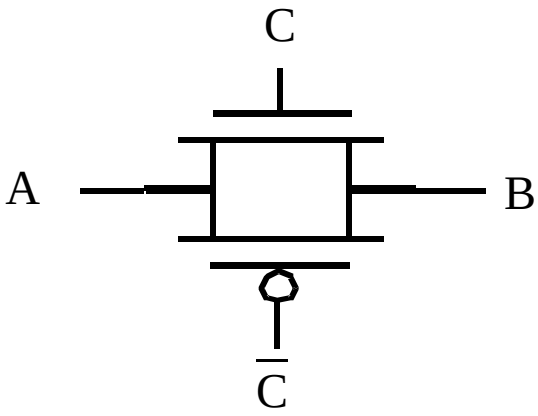
WATCH OUT FOR LEAKAGE CURRENTS

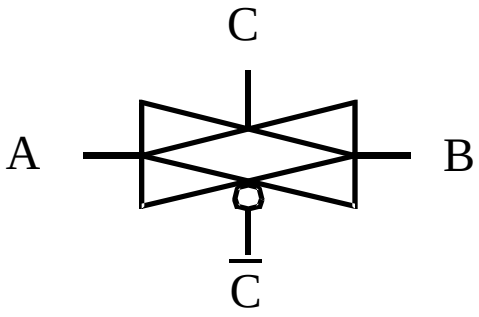
- Complementary pass transistor

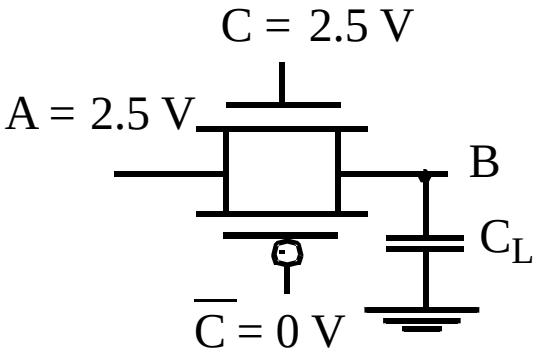




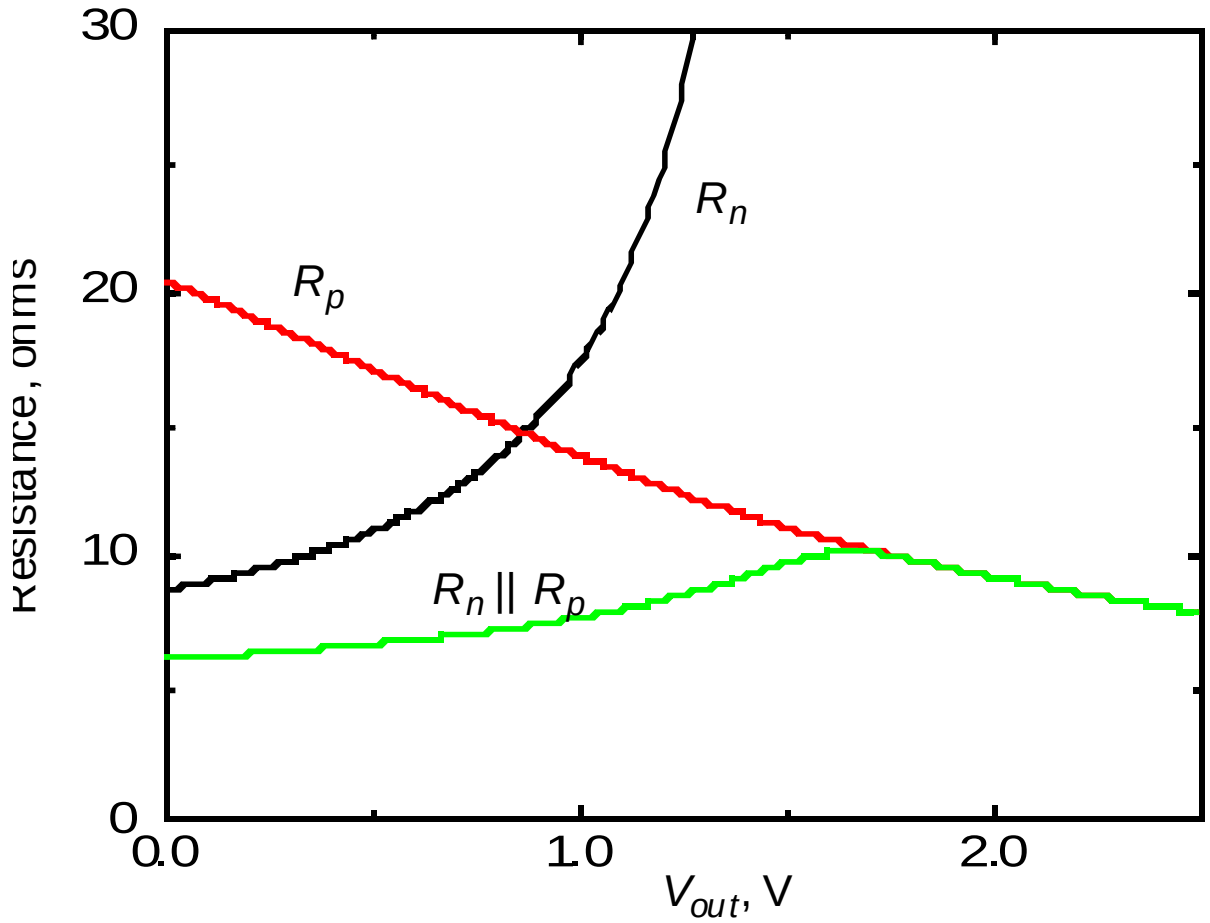
- Transmission gate

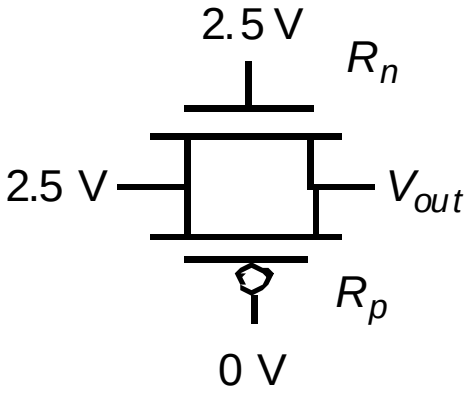




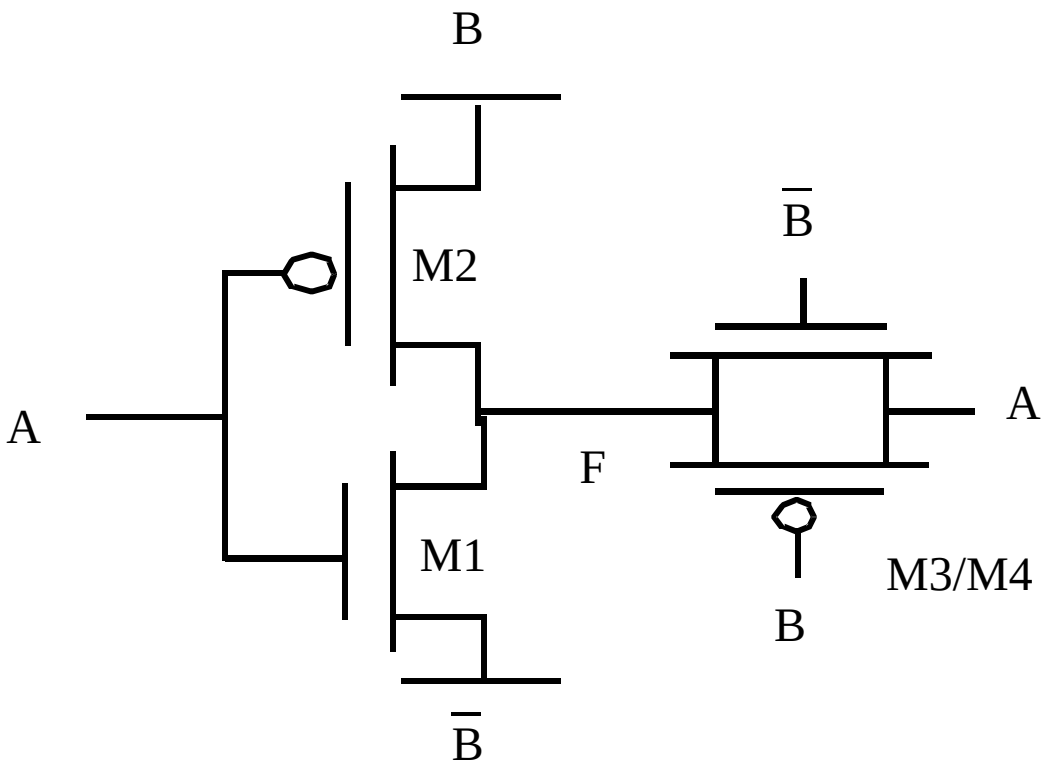


- Resistance of transmission gate

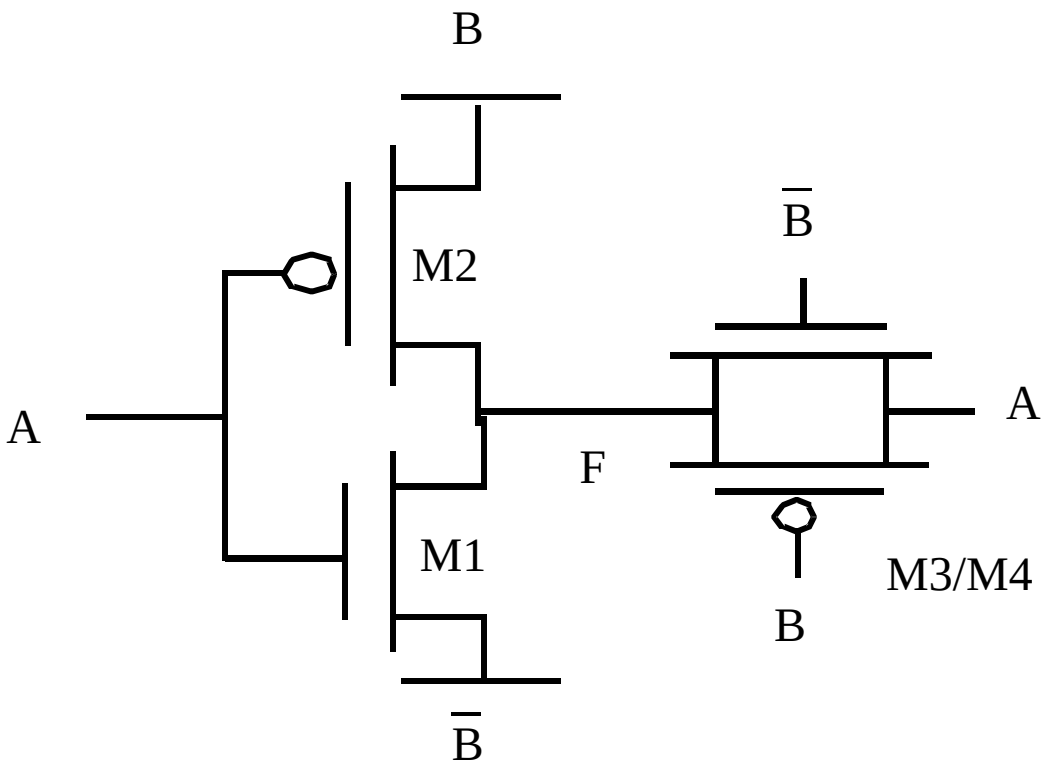




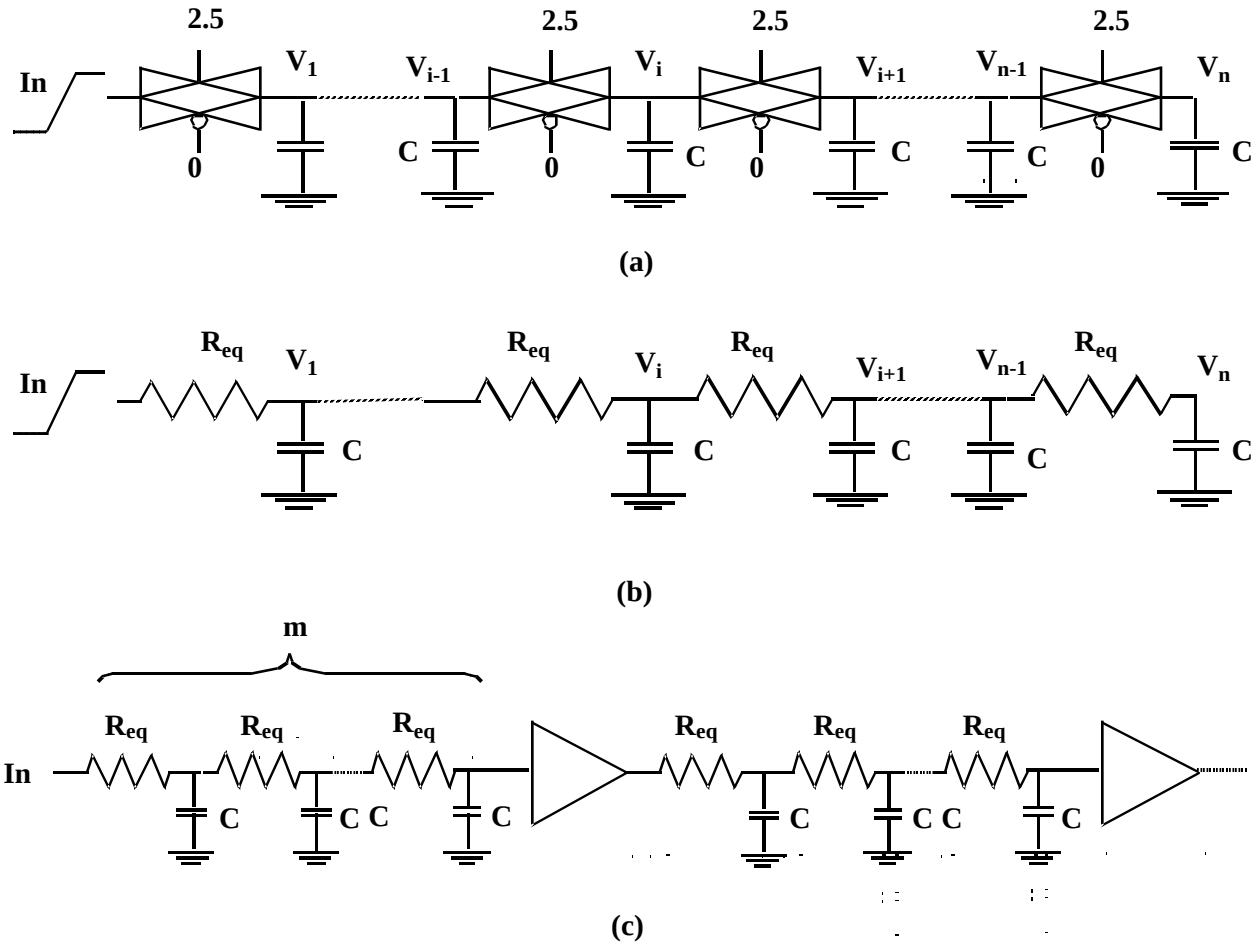
- Transmission gate XOR



- Transmission gate XOR



- Delay in transmission gate network



- Delay optimization
  - **Delay of RC chain**

$$t_p = 0.69 \sum_{k=0}^{n} CR_{eq} k = 0.69 CR_{eq} \frac{n(n+1)}{2}$$

  - **Delay of Buffered Chain**

$$t_p = 0.69 \left\lfloor \frac{n}{m} CR_{eq} \frac{m(m+1)}{2} \right\rfloor + \left(\frac{n}{m} - 1 \right) t_{buf}$$

$$= 0.69 \left[CR_{eq} \frac{n(m+1)}{2} \right] + \left(\frac{n}{m} - 1 \right) t_{buf}$$

$$m_{opt} = 1.7 \sqrt{\frac{t_{pbuf}}{CR_{eq}}}$$