Spice Modeling of Silicon Nanowire Field-Effect Transistors for High-Speed Analog Integrated Circuits

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***Abstract*—Vertical nanowire surrounding gate field-effect transistors (SGFETs) provide full gate control over the channel to eliminate short-channel effects and to achieve ultralow OFF current. This paper presents the fully depleted BSIMSOI modeling of low-power NMOS and PMOS SGFETs with 10 nm channel length and 2 nm channel radius, extraction of distributed device parasitics, and measuring the capabilities of these transistors for high-speed analog and RF applications. When biased with $V_{\rm ds} = 0.5$ V and $V_{\rm gs} = 0.5$ V at the active operating region, NMOS and PMOS SGFETs have 2 μA and 0.7 μA drain currents, 14 μA/V and 8 μA/V transconductances, 400 kΩ and 1.1 MΩ output resistances, 36 THz and 25 THz unity-current-gain cutoff frequencies, and 120 THz and 100 THz maximum frequency of oscillations, respectively. A single-stage CMOS SGFET amplifier dissipates 1.64 μW power and provides 500 GHz bandwidth with -6.5 gain and -24 dBm third-order intermodulation distortion tones for a two-tone input signal with 10 mV amplitude and 10 GHz frequency spacing. The large-signal operation of the amplifier with 1 V output swing exhibits 2.2 ps delay, 5.4 ps rise time, and 4.7 ps fall time while oscillating at 30 GHz. All these parameters indicate that vertical nanowire surrounding gate transistors are promising candidates for the next-generation very-large-scale integration (VLSI) technology.**

***Index Terms*—Field-effect transistor, high frequency, modeling, nanowire, silicon.**

I. Introduction

THE SPEED of silicon integrated circuits are reaching beyond 100 GHz to enable integration of the patch antenna on the substrate and to realize ultracompact designs [1]. The small feature size of the planar bulk MOSFETs helps to increase the speed and functionality of the wireless communication systems while reducing the fabrication cost [2]. Even though the current very-large-scale integration (VLSI) technology has approached to its scaling limits necessitating a replacement technology, silicon-based devices are still favored to realize large-scale circuits and systems because all aspects of the technology, such as producing practically defect-free wafers to complex circuit fabrication steps, have been well established.

Recent device developments in both molecular and quantum levels will eventually replace the traditional silicon-based transistors. Single electron transistors offer promising results in terms of functionality and organic molecules have been shown to operate as switches [3], [4]. Various research groups have demonstrated the operation of fundamental logic blocks including a memory, an arithmetic logic unit (ALU), and a state machine using molecular transistors on fabric-like architectures [5]. Spintronics is another emerging field to replace the state-of-the-art VLSI, and a recent study has successfully implemented a fully functional CPU in liquid nitrogen temperature [6], [7]. However, all aforementioned technologies are still in the exploratory stage and far from being fully implemented for commercial use. Therefore, finding other silicon-compatible solutions that can produce high-performance and low-power devices to accommodate large system on chip (SoC) designs is vital.

Double-gated silicon-on-insulator (SOI) technology offers a unique solution in reducing leakage current as compared to bulk transistors; however, placing ultrathin transistor bodies between two metal gates to produce a realistic threshold voltage is highly questionable to fabricate [8]. The triple-gated SOI transistor or FINFET is another choice that presents close-to-ideal subthreshold slope and small drain-induced barrier lowering (DIBL), both of which are core factors to reduce the OFF current [9], [10]. Other 3-D structures such as carbon nanotube and nanowire transistors have been shown to operate at very-high frequencies and participate the race toward establishing the next-generation VLSI technology [11]–[14].

We conducted a 3-D device design study on undoped surrounding gate silicon nanowire transistors with the objective to design CMOS circuits with minimal power dissipation [15]–[17]. We explored that the strengths of this technology was superior as compared to both dual-gated SOI and FINFET technologies in terms of static and dynamic power dissipations, suppression of short-channel effects, breakdown voltage, and the ease of manufacturability. We also pointed out the weaknesses of silicon nanowire transistors such as increased layout area due to surrounding gate metal thickness, large source resistance caused by source contact extension, and limited ON current caused by fixed transistor geometry. In our earlier studies, we used these transistors in basic digital logic gates and found out that the worst case delays and power dissipations were in sub-10 ps and sub-100 nW ranges [18], [19].

We also investigated the performance, power dissipation, and layout area of more complex circuits such as neuron and SRAM using the software process improvement and capability determination (SPICE) level-6 model in circuit simulations [20], [21]. While using this model helped in simulating digital circuits, more accurate intrinsic device modeling and parasitic RC

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extraction are required for simulating high-speed analog and RF integrated circuits. This need prompted us to explore more appropriate higher level SPICE models such as fully depleted BSIMSOI [22]. Even though various analytical physical models were proposed by different research groups for surrounding gate transistors, these results are only satisfactory for long-channel devices and large discrepancies arise between the simulated and modeled I–V characteristics when the transistor channel length approaches 10 nm range [23]–[26]. The inaccuracies are especially intolerable in active region for analog and RF applications where impact ionization and DIBL are dominant factors in determining the transistor linearity.

The main focus of this paper is to develop an accurate fully depleted BSIMSOI model for all operating regions of the surrounding gate field-effect transistors (SGFETs) and compare the results against numerical device simulations in measuring small-signal and large-signal device characteristics. The 3-D device structure and the physical model of the nanowire SGFET are presented and compared with a planar bulk transistor with same dimensions in Section II. Section III presents the BSIMSOI model parameters and the comparison between input and output I–V characteristics of the intrinsic device obtained from BSIMSOI model and device simulation. Calculation of voltage dependent intrinsic gate-oxide capacitance and device parasitic resistors and capacitors including the effective high-frequency gate resistance are also presented in Section III. Extrinsic transistor input and output I–V characteristics, transconductance, and output resistance at various biasing conditions for 2 nm radius and 10 nm channel length NMOS and PMOS transistors are provided in Section IV. This section also contains extraction of S-parameters, power gains, $f_{\max}$, and f_τ of NMOS and PMOS transistors. Section V characterizes the large-signal and small-signal operations of a single stage CMOS amplifier using the developed models.

II. SGFET Device

The device structure of the vertical SGFET is shown in Fig. 1. The transistor is built on top of an n-well (p-well), which has a depth of 30 nm and a diameter of 40 nm. The intrinsic transistor has a channel length of 10 nm, a radius of 2 nm, a gate oxide of 1.5 and 12 nm source and drain junctions extended from both ends of the channel. NMOS and PMOS transistors are constructed as enhanced-type with undoped silicon bodies, while source and drain junctions have Gaussian profiles with a peak doping concentration of 10^{20} cm^{-3}. Silvaco Atlas simulator is used to characterize the intrinsic transistors. The impacts of quantum confinement and carrier transportation are included by a self-consistent Schrodinger–Poisson solver combined with nonequilibrium Green's function. The Fermi statistics, low- and high-electric field mobility, concentration-dependent Shockley–Read–Hall recombination, Arora's lattice temperature, and Serberherr's impact ionization models are included in the simulations [15]–[21].

The extrinsic transistor uses 4 nm $\times$ 4 nm contacts with 4 nm spacing. The minimum spacing between metal1 interconnects is 5 nm and the minimum width and height of the metal1 interconnects are 14 and 10 nm, respectively, yielding an aspect ratio of 1.4. The metal gate has a thickness of 10 nm. A small contact geometry results in smaller device area due to closer spacings; however, it increases the resistance of each contact. Gate and source terminals have critical contact resistances due to their large distance from metal1 layer. Therefore, two parallel contacts are used for each source and gate terminals, and the n-well (p-well) is also surrounded by a concentric metal ring to reduce the overall resistance of the source terminal. The drain, gate, and source contacts have thicknesses of 6, 18, and 34 nm, respectively. The concentric source contact has 6 nm thickness, 6 nm width, 13 nm inner radius, and 19 nm outer radius. The n-well or p-well overlap with the concentric source contact is 1 nm. The minimum side overlap of metal1 and contact is 1 nm. The distance between metal1 and metal2 (not shown in the layout) is 36 nm. The metal2 and via12, which connects metal1 and metal2 layers, have the same design rules as metal1 and contact. The area of the vertical SGFET is 1600 nm^2 (40 nm $\times$ 40 nm). SGFETs have negligible gate–drain overlap and drain–source parasitic capacitances as compared with planar MOSFETs.

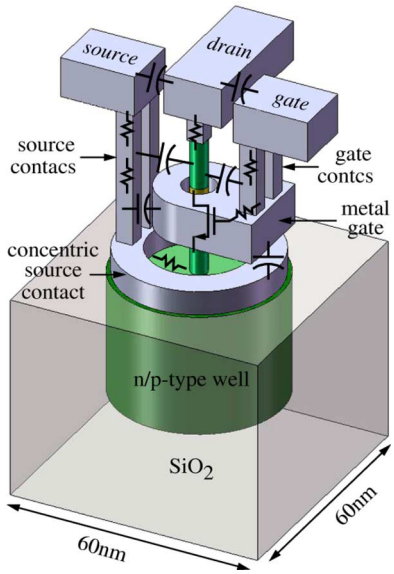

Fig. 1. 3-D view of the vertical nanowire SGFET.

The top views of the vertical SGFET and the planar MOSFET layouts are shown in Fig. 2(a) and (b). The layout of the planar MOSFET has the same active device and contact areas as well as metal and contact spacings. Considering 4 nm extension of the polysilicon gate from each side of the channel width to prevent channel salicidation during fabrication that is used to reduce the gate sheet resistance, the area of the planar MOSFET is also 1600 nm^2 (76 nm $\times$ 21 nm) with body contact and 1130 nm^2 (54 nm $\times$ 21 nm) without body contact. The area of the large channel width planar transistors with body contact reaches to 62% of the total SGFET area with the same channel width.

Downscaling of bulk MOSFETs has introduced various quantum mechanical effects in nanoscale devices and has increased the complexity of device modeling required for accurate circuit simulation [27]. The channel length scaling of the bulk

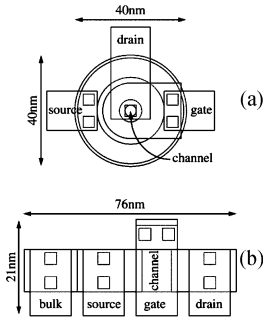

Fig. 2. Layout views. (a) Vertical nanowire SGFET. (b) Planar bulk MOSFET.

MOSFETs increases the device speed while introducing strong electric fields in channel causing early drain–source voltage breakdown. Therefore, reducing drain–source voltage and using lightly doped drain (LDD) are necessary to ensure proper device operation. To prevent strong vertical electric field in the channel and high gate leakage current caused by carriers tunneling into the thin gate oxide, the gate voltage of the transistor must also be reduced [28]. Continuous scaling of voltage levels and device dimensions in planar MOSFETs weaken the gate control over channel and enhance short-channel issues such as high-channel OFF current, punch-through, gate bias dependent mobility, threshold voltage variation, and gate leakage current increasing the overall static power dissipation [29].

Another major issue of the nanoscale bulk MOSFETs is the latchup caused by substrate bipolar parasitics. Extra spacing between NMOS and PMOS transistors and addition of low-resistive substrate contacts are required to minimize latchup, which increase the layout area of planar transistors [30]. When bulk MOSFETs operate at high frequencies, the strong signal coupling through resistive silicon substrate increase the interaction among different circuit blocks and deteriorate the overall quality of the SoC devices [31]. To minimize substrate coupling, guard rings, and shallow trench isolations must be used that increase the layout area and cost significantly [32].

Intrinsic undoped single-gate, double-gate, triple-gate, or gate-all-around SOI MOSFETs have minimal substrate coupling and latchup compared with bulk MOSFETs, and hence, they are better choice for mixed signal VLSI applications. The advantage of the vertical nanowire SGFETs is the full gate control over the channel, reduced short-channel effects and low standby current due to low subthreshold slope and DIBL. The circuit modeling and the parasitic extraction of the SGFETs are presented in the next section.

III. Intrinsic Modeling and Parasitic Extraction

SPICE models of NMOS and PMOS SGFETs are created by fully depleted BSIMSOI parameters. Important SGFET model parameters are listed in Table I. These parameters are optimized to ensure input and output I–V characteristics of 10 nm channel length and 2 nm radius SGFETs closely match to those obtained from numerical device simulations. Intrinsic input I–V characteristics of NMOS and PMOS SGFETs are shown in Fig. 3(a) and (b), respectively, in the subthreshold regime. The intrinsic

TABLE I
List of BSIMSOI Model Parameters of SGFETs

Parameters	Values
Channel Length (L)	10 nm
Channel Radius (R)	2 nm
Gate Oxide Thickness (t_{ox})	1.5 nm
Channel Doping Concentration (n_{ch})	1.5e+019 cm^{-3}
Substrate Doping Concentration (n_{sub})	1.0e+011 cm^{-3}
Threshold Voltage (V_{th0})	0.26 V (nmos) −0.28 V (pmos)
Mobility (U_0)	1000 cm^2/V.s (nmos) 300 cm^2/V.s (pmos)
Parasitic Resistance Per Unit Area (R_{dsw})	130 Ω.μm (nmos) 360 Ω.μm (nmos)
Saturation Velocity (V_{sat})	≈ 2e+06 cm/s
Subthreshold Region Offset Voltage (V_{off})	0.06 V
Channel Length Modulation (P_{clm})	25
Primary Output Resistance DIBL Effect (P_{diblc1})	1.02e−006
Secondary Output Resistance DIBL Effect (P_{diblc2})	1
Primary Short Channel Effect on V_{th} (D_{vt0})	3.8
Secondary Short Channel Effect on V_{th} (D_{vt1})	2.75
Short Channel Body Bias Effect on V_{th} (D_{vt2})	0 V^{-1}
Primary Narrow Width Effect on V_{th} (D_{vt0w})	0
Secondary Narrow Width Effect on V_{th} (D_{vt1w})	7.25e+007
Narrow Width Body Bias Effect on V_{th} (D_{vt2w})	0.34 V^{-1}
Subthreshold Region DIBL Coefficient (Eta_0)	0.008
Subthreshold Body Bias DIBL Effect (Eta_b)	0.174 V^{-1}
DIBL Coefficient Exponent (D_{sub})	1
Drain/Source to Channel Coupling Capacitance (C_{dsc})	1.373e−010 F/cm^2

output I–V characteristics of the NMOS and PMOS SGFETs are also shown in Fig. 4 (a) and (b), respectively. A close match between SPICE models and numerical simulators are observed for all values of $V_{\rm gs}$, especially at high voltage levels in active operating region.

The intrinsic coupling capacitance $C_{\rm dsi}$ between drain and source terminals of the fully depleted channel is obtained by

$$C_{\rm dsi} = \varepsilon_{\rm si}\varepsilon_0 \frac{\pi R^2}{L} \tag{1}$$

where $\varepsilon_{\rm si} = 11.7$ is the relative permittivity of the silicon, $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm is the permittivity of vacuum, $R = 2$ nm is the channel radius, and $L = 10$ nm is the channel length. The intrinsic drain and source coupling capacitance is therefore equal to 0.13 aF. The gate oxide capacitance of the transistor is obtained by

$$C_{\rm gsi} = \varepsilon_{\rm ox}\varepsilon_0 \frac{2\pi RL}{t_{\rm ox}} \tag{2}$$

and is equal to 2.9 aF, where $\varepsilon_{\rm ox} = 3.9$ is the relative permittivity of the silicon oxide and $t_{\rm ox} = 1.5$ nm is the oxide thickness. The intrinsic gate–source capacitance $C_{\rm gsi}$ of the NMOS and PMOS SGFETs are shown in Fig. 5(a) and (b), respectively. These capacitors are obtained from transient simulations using

$$C_{\rm gsi} = \frac{I(t)}{dV(t)/dI(t)} \tag{3}$$

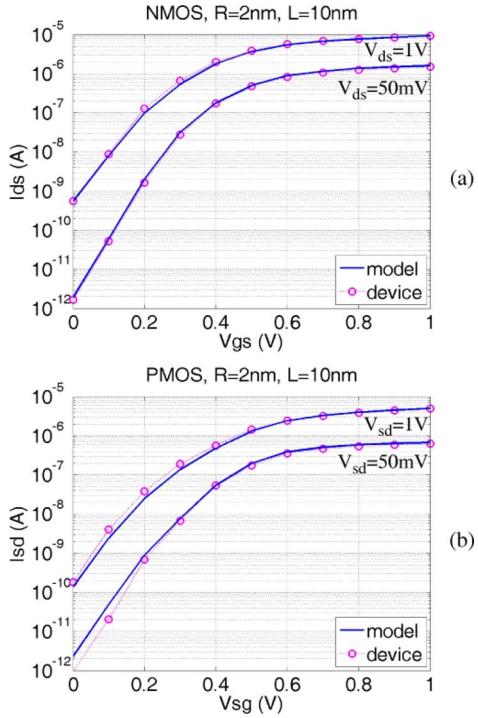

Fig. 3. Subthreshold input I–V characteristics of intrinsic. (a) NMOS. (b) PMOS SGFETs.

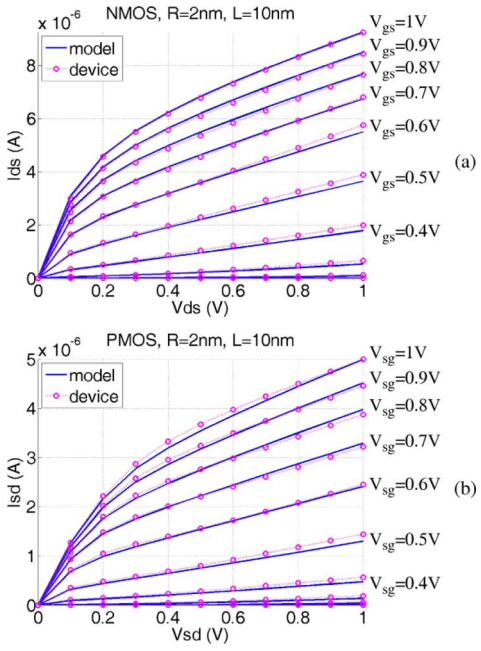

Fig. 4. Output I–V characteristics of intrinsic. (a) NMOS. (b) PMOS SGFETs.

where $I(t)$ represents the feed current through the gate–source terminal and $dV(t)/dt$ represents the rate of change of the charging voltage across the gate and source terminals. When NMOS and PMOS SGFETs are OFF, the intrinsic gate–source capacitance is negligible due to the fully depleted channel and becomes

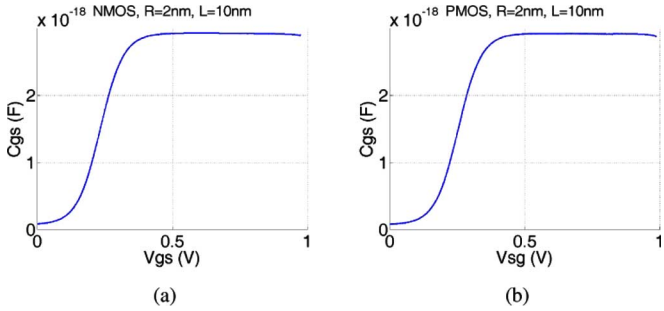

Fig. 5. Intrinsic gate oxide capacitance. (a) NMOS. (b) PMOS SGFETs.

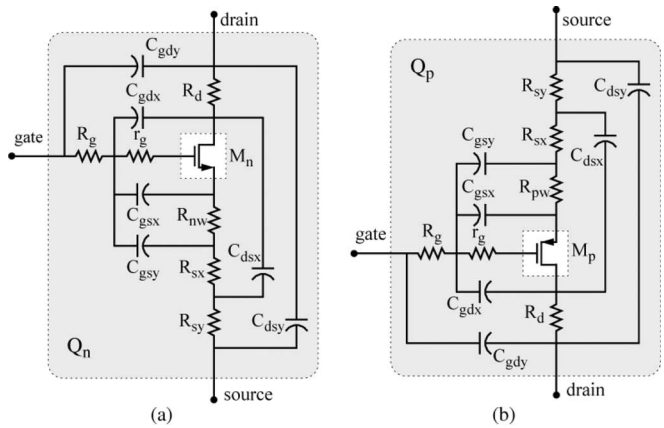

Fig. 6. Distributed parasitic components across. (a) Intrinsic NMOS, M_n. (b) Intrinsic PMOS, M_p, SGFETs.

equal to

$$C_{\rm gsi} = \frac{C_{\rm ox}\, C_{\rm dsi}}{C_{\rm ox} + C_{\rm dsi}}. \tag{4}$$

When NMOS and PMOS SGFETs become ON, their channel invert and the intrinsic gate–source capacitance reaches C_{ox}.

At very small dimensions, the extrinsic parasitic resistance and capacitance of the transistor interconnects become dominant due to small metal thickness and close metal spacing. Therefore, parasitics need to be accurately calculated for high-speed modeling of analog and RF circuits. The distributed parasitic RC components across the intrinsic SGFET transistor, shown in Fig. 1, are modeled for NMOS and PMOS transistors, as shown in Fig. 6(a) and (b), respectively.

$C_{\rm gsx}$ is the parasitic capacitance between metal gate and the concentric source and $C_{\rm gsy}$ is the parasitic capacitance between metal gate and the source contact. The resistor r_g accounts for the effective gate resistance at high frequencies caused by the distributed gate-oxide channel. The resistance R_g accounts for two parallel gate contacts. $C_{\rm dsx}$ is the parasitic capacitance between intrinsic drain and source contacts and $C_{\rm dsy}$ is the parasitic capacitance between drain and source interconnects. Resistors $R_{\rm sx}$ and $R_{\rm sy}$ represent source contacts and resistors $R_{\rm nw}$ and $R_{\rm pw}$ represent overall concentric n-well and p-well resistances from intrinsic source to extrinsic source contacts of NMOS and PMOS SGFETs, respectively. $C_{\rm gdx}$ is the parasitic

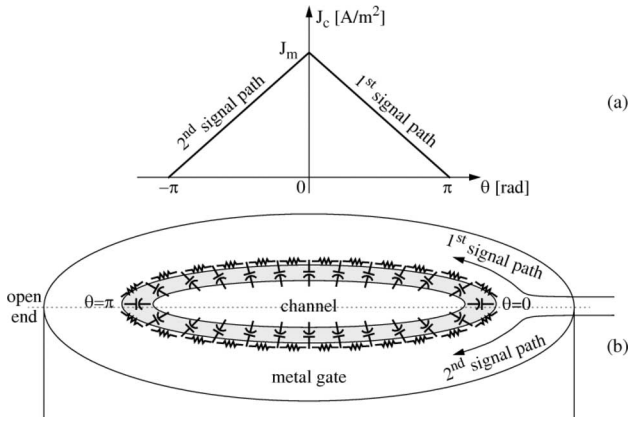

Fig. 7. Gate and channel. (a) High-frequency current distribution. (b) Parasitics.

capacitance between gate contact and the intrinsic drain and C_{gdy} is the parasitic capacitance between gate and drain interconnects. The resistor R_d represents the drain contact of the transistor.

All parasitic coupling and fringe capacitors are calculated by using 3-D ADS momentum field simulator. Besides effective resistance r_g, all other parasitic resistors are calculated by $\rho l/S$ at low frequencies, where $\rho = 180\ \Omega$·nm is the resistivity of the sub-10 nm copper wire [18], l is the length of the resistive path, and S is the cross-section area of the resistive path. The resistance r_g affects the impedance and noise matching of the transistor at RF and is obtained by considering the high-frequency gate current density distribution resulted from the distributed RC network of the gate-oxide and channel, as shown in Fig. 7(a) and (b). When a high-frequency signal is applied to one end of the metal gate ($\theta = 0$, where θ represents the angle of the surrounding metal gate), the signal travels through two parallel signal paths (first and second), as shown in Fig. 7(b), until it reaches the other end of the metal gate ($\theta = \pm\pi$). While the high-frequency current signal travels through metal gate, it leaks through distributed gate-oxide capacitors, and the current density of the signal decreases from the maximum value of J_m and reaches 0, as shown in Fig. 7(a).

The effective distributed high-frequency gate resistance is, therefore, given by [33]

$$r_g = \frac{1}{2}\frac{1/\pi \int_0^{\pi} V(\theta)d\theta}{1/\pi \int_0^{\pi} I(\theta)d\theta} = \frac{1}{2}\frac{\int_0^{\pi} (R_s\, R\theta/L)\,(J_c\, S)d\theta}{\int_0^{\pi} (J_c\, S)d\theta} \tag{5}$$

where R_s is sheet resistance of the metal gate, L is the channel length, S is the cross-section area of the metal gate, R is the radius of the nanowire transistor, and J_c is the current density distribution given by $J_{\mathrm{m}}(\pi - \theta)/\pi$, where J_m is the maximum current density in the metal gate and θ is the surrounding gate angle. The effective resistor r_g is, therefore, given by

$$r_g = \frac{1}{12}\left(R_s \frac{2\pi R}{L}\right) \tag{6}$$

which is equal to the effective gate resistance of the planar transistors with signals applied to both ends of the gate. However, due to the excess polysilicon resistance of planar MOSFETs and the wide metal gate structure of nanowire SGFETs, it is expected that the overall effective gate resistance of nanowire SGFETs is smaller than planar transistors. A small r_g significantly enhances the operation speed and impedance-matching capabilities of the transistor.

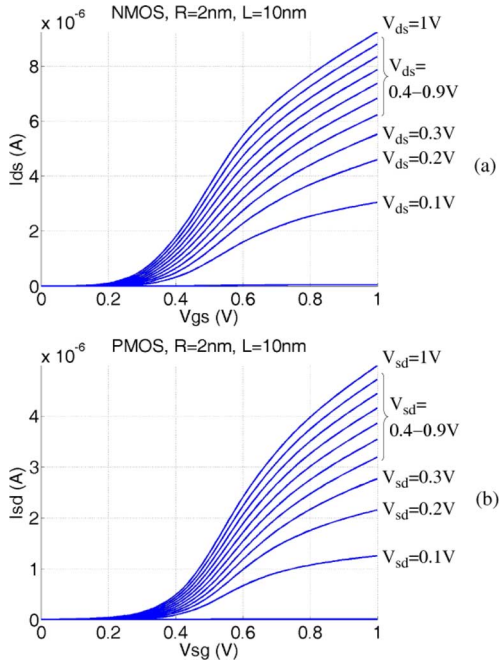

Fig. 8. Input I–V characteristics of extrinsic. (a) NMOS. (b) PMOS SGFETs.

The distributed SGFET parasitic components are listed in Table II(a) and (b) for resistors and capacitors, respectively. A comparison between the layouts of the vertical nanowire SGFETs and planar bulk MOSFETs reveals that SGFETs suffer from larger source resistance and gate–source capacitance, while MOSFETs suffer from larger source/drain junctions, gate–drain, and gate-source capacitances.

IV. Extrinsic SGFET Characteristics

The input I–V characteristics of the extrinsic NMOS and PMOS SGFETs including all parasitic resistances are shown in Fig. 8(a) and (b), respectively, in 0.1 V V_{ds} increments. The extrinsic saturation currents of NMOS and PMOS transistors are 9 and 5 μA, respectively. The extrinsic transconductances of NMOS and PMOS SGFETs, calculated from the slopes of the input I–V characteristics, reach a maximum value of 20 and 11.5 μA/V at $V_{\mathrm{gs}} = 500$ mV and $V_{\mathrm{sg}} = 550$ mV, as shown in Fig. 9(a) and (b), respectively.

The output I–V characteristics of the extrinsic NMOS and PMOS SGFETs including all parasitic resistances are shown in Fig. 10(a) and (b), respectively, in $V_{\mathrm{gs}} = 0.1$ V increments. Extrinsic output resistances, calculated from inverse slopes of output I–V characteristics, are shown in Fig. 11(a) and (b) for NMOS and PMOS SGFETs, respectively. At similar biasing conditions (i.e., $V_{\mathrm{gs}} = 0.5$ V and $V_{\mathrm{ds}} = 0.5$ V), the NMOS and PMOS transistors have 400 kΩ and 1.1 MΩ output resistances, respectively.

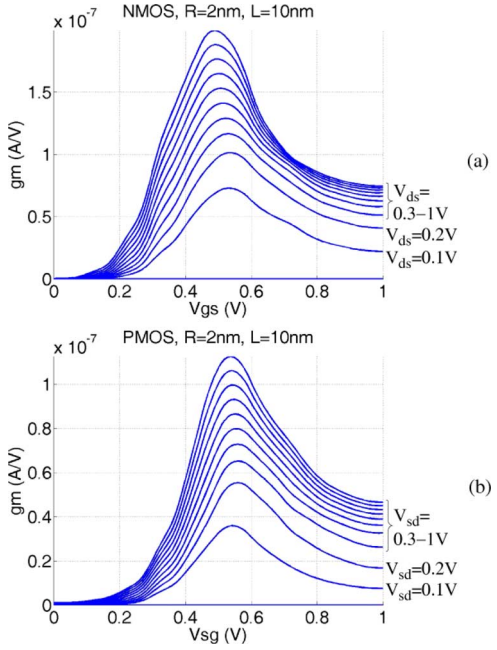

Fig. 9. Transconductance of extrinsic. (a) NMOS. (b) PMOS SGFETs.

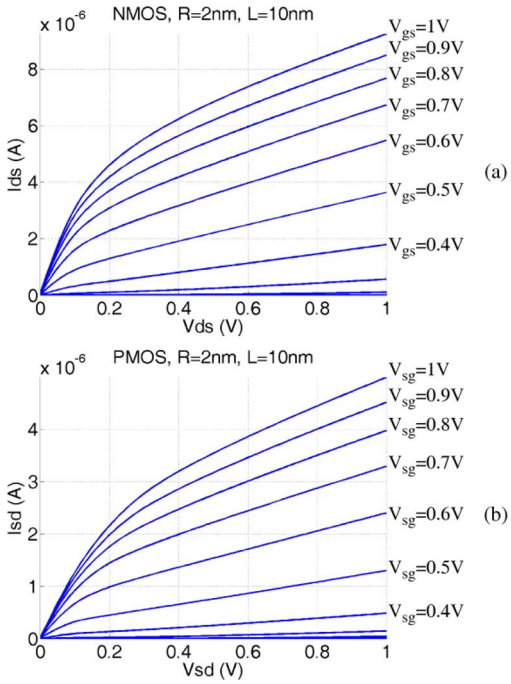

Fig. 10. Output I–V characteristics of extrinsic. (a) NMOS. (b) PMOS SGFETs.

The S-parameters of NMOS and PMOS SGFETs are shown in Fig. 12(a) and (b), respectively. These parameters are obtained by sweeping the frequency from 1 MHz to 10^3 THz and using ports with $Z_0 = 1$ kΩ internal resistances to ensure stability. Compared with nanowire transistors, the inductors and capacitors of the input and output bias-T circuits are selected to behave as open and short connections, respectively, at the sweeping frequency. The transistors are biased with $V_{\rm ds} = 1$ V

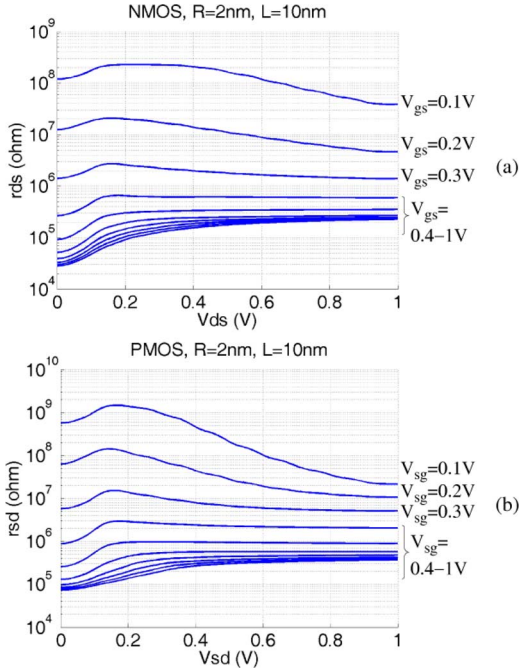

Fig. 11. Output resistance of extrinsic. (a) NMOS. (b) PMOS SGFETs.

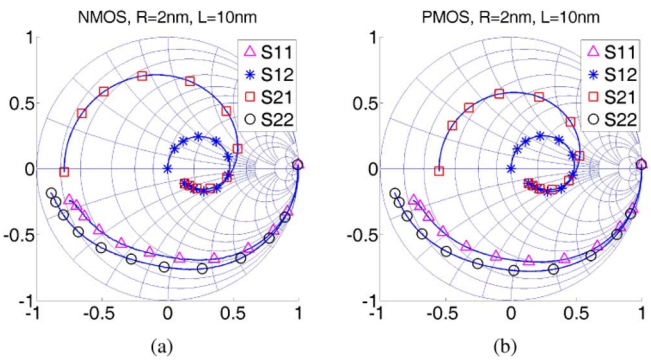

Fig. 12. S-parameters of extrinsic. (a) NMOS. (b) PMOS SGFETs.

and $V_{\rm gs} = 0.5$ V to yield the maximum transconductance and to ensure a high power gain. The S_{22} (output return loss) is a measure of the transistor output resistance and S_{21} (forward gain) is a measure of the transistor voltage gain. Due to similar dimensions, NMOS and PMOS SGFETs have very similar parasitic components, while the g_m and $r_{\rm out}$ of NMOS and PMOS transistors differ from each other. Therefore, it is expected that S_{22} and S_{21} of the NMOS and PMOS transistors deviate from each other, while S_{11} (input return loss) and S_{12} (reverse gain) of transistors match more closely, as shown in Fig. 12(a) and (b).

The two important figure of merits for RF transistors are the maximum frequency of oscillation ($f_{\rm max}$) and the unity-current-gain cutoff frequency (f_τ). The $f_{\rm max}$ is obtained when the magnitude of the maximum available power gain ($G_{\rm max}$) of the transistor becomes unity and f_τ is obtained when the magnitude of the current gain (H_{21}) of the transistor becomes unity. The $G_{\rm max}$ and H_{21} of the transistor, under simultaneous conjugate impedance-matching conditions at input and output

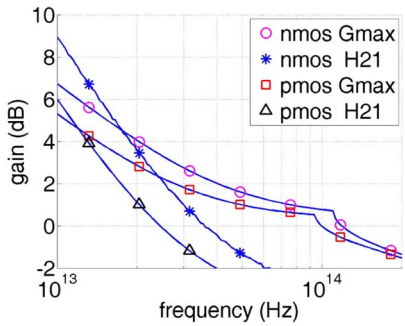

Fig. 13. High-frequency power and current gains of extrinsic NMOS and PMOS SGFETs.

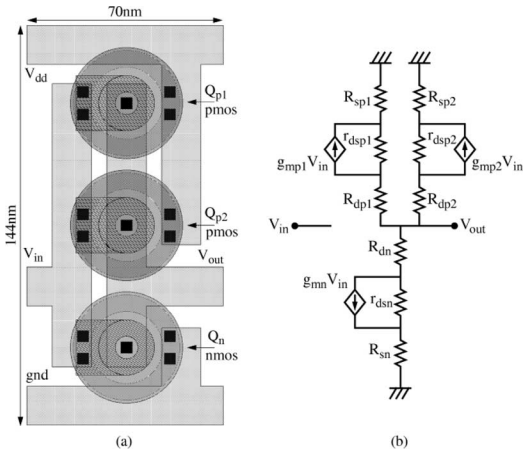

Fig. 14. SGFET CMOS amplifier. (a) Layout. (b) Low-frequency small-signal model.

ports, are expressed in terms of S-parameters using

$$G_{\max} = \frac{S_{21}^2}{(1 - S_{11}^2)(1 - S_{22}^2)} \tag{7}$$

and

$$H_{21} = \frac{S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \tag{8}$$

The magnitudes of $G_{\max}$ and H_{21} of NMOS and PMOS SGFETs are shown in Fig. 13. The $f_{\max}$ and f_τ of NMOS and PMOS SGFETs are 120 THz, 36 THz and 100 THz, 25 THz, respectively.

V. SGFET CMOS Amplifier

The layout of an SGFET CMOS amplifier that can be used as both large-signal inverter or small-signal amplifier is shown in Fig. 14(a). The biasing point of the transistors are mainly decided by the voltage level of the input signal. For 1 V supply voltage, both transistors operate in active region when the input voltage changes from 0.4 to 0.6 V. Two PMOS transistors (Q_{p1} and Q_{p2}) are used in parallel to ensure their overall ON current is almost equal to that of the single NMOS transistor (Q_n). The area of the SGFET amplifier is 70 nm $\times$ 144 nm. The low-frequency small-signal model of the amplifier, when both transistors operate in active region, is shown in Fig. 14(b). For each transistor, R_d represents the drain resistance and R_s the overall source resistance given by $R_{\rm sn} = R_{\rm sx} + R_{\rm sy} + R_{\rm nw}$ for NMOS and $R_{\rm sp} = R_{\rm sx} + R_{\rm sy} + R_{\rm pw}$ for PMOS, respectively, as listed in Table II. The low-frequency small-signal gain of the CMOS amplifier is given by

$$A_{v0} = -\left[\frac{g_{\rm mn} r_{\rm dsn}}{R_n} + \frac{g_{\rm mp1} r_{\rm dsp1}}{R_{p1}} + \frac{g_{\rm mp2} r_{\rm dsp2}}{R_{p2}}\right] \times (R_n \,\|R_{p1}\|\, R_{p2}) \tag{9}$$

where

$$R_n = r_{\rm dsn} + R_{\rm sn} + R_{\rm dn} \approx r_{\rm dsn} \tag{10}$$

and

$$R_{p1} = r_{\rm dsp1} + R_{\rm sp1} + R_{\rm dp1} \approx r_{\rm dsp1} \tag{11}$$

and

$$R_{p2} = r_{\rm dsp2} + R_{\rm sp2} + R_{\rm dp2} \approx r_{\rm dsp2}. \tag{12}$$

Therefore, (9) can be rewritten as

$$A_{v0} \approx -[g_{\rm mn} + g_{\rm mp1} + g_{\rm mp2}](r_{\rm dsn} \,\|r_{\rm dsp1}\|\, r_{\rm dsp2}) \tag{13}$$

and is approximately equal to -6.9, considering that at $V_{\rm ds} = 0.5$ V and $V_{\rm gs} = 0.5$ V, the transconductance g_m of NMOS and PMOS transistors are 14 and 8 μA/V, and the output resistance $r_{\rm ds}$ of NMOS and PMOS transistors are 400 kΩ and 1.1 MΩ, respectively. The simplified low-frequency voltage-gain expression of the SGFET amplifier becomes similar to the MOSFET amplifier gain when $R_s \ll 1/g_m \ll r_{\rm ds}$ is satisfied.

The frequency bandwidth and linearity are other important figure of merits of an amplifier. When biased at $V_{\rm gs} = 0.5$ V, the gain of the amplifier is 20 $\times$ log(6.5) = 17 dB and the phase is 180°, as shown in Fig. 15. The unity-voltage-gain cutoff frequency of the amplifier is 20 THz with a phase angle of 60°. The 3 dB frequency bandwidth of the amplifier is about 500 GHz and the power dissipation is about 1.64 μW. The output spectrum of the amplifier in response to a two-tone test with 10 GHz spacing is shown in Fig. 16. The second and third harmonic distortions (HD2 and HD3 tones) of the amplifier are 10 and 20 dB below the fundamental tones, respectively. The third order intermodulation distortions (IM3 tones) are 24 dB below the fundamentals for 10 mV input signal levels.

TABLE II
List of SGFET Parasitic (a) Resistors and (b) Capacitors

(a) Resistors	Values
r_g	10 Ω
R_g	110 Ω
R_{nw} (R_{pw})	2.3 (3.4) kΩ
R_{sx}	100 Ω
R_{sy}	100 Ω
R_d	70 Ω

(b) Capacitors	Values
C_{gsx}	3 aF
C_{gsy}	1 aF
C_{gdx}	0.5 aF
C_{gdy}	0.8 aF
C_{dsx}	0.5 aF
C_{dsy}	0.8 aF

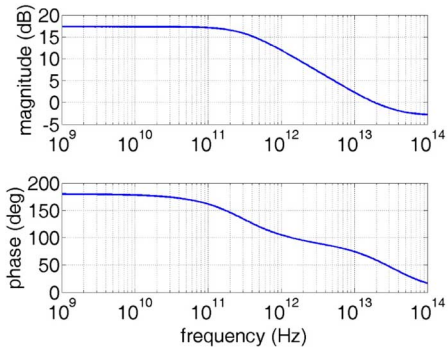

Fig. 15. Amplifier small-signal frequency response.

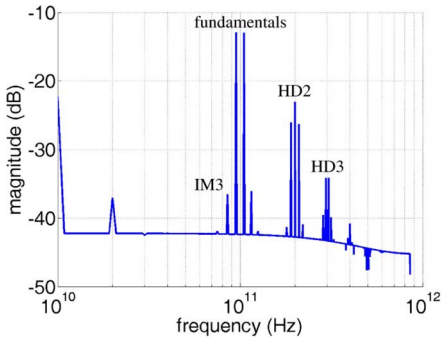

Fig. 16. Amplifier two-tone output spectrum.

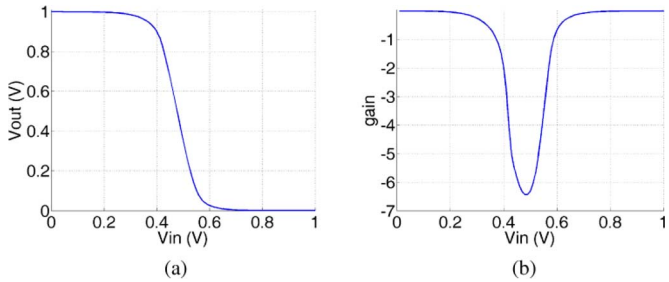

Fig. 17. Amplifier large-signal (a) transfer characteristic and (b) dc gain.

The transfer characteristic of the SGFET CMOS amplifier including all parasitic resistors and its slope representing the dc voltage gain are shown in Fig. 17(a) and (b), respectively. When the input voltage applied to the amplifier reaches 500 mV, the gain of the circuit reaches -6.5. The large-signal transient response of the SGFET amplifier, acting as an inverter, is shown in Fig. 18. Seven inverters are cascaded with a closed-loop feedback, and the initial condition of the circuit is chosen to ensure self-oscillation. The gate delay of each SGFET inverter is 2.2 ps and the rise and fall times are 5.4 and 4.7 ps, respectively, while the oscillation frequency is 30 GHz. These values are obtained by considering all parasitic values of the layout.

The summary of the SGFET characteristics are listed in Table III. These parameters indicate that vertical SGFET technology is a promising candidate for the next-generation low-power and high-speed VLSI circuits when the mainstream planar MOSFET technology reaches its scaling limit.

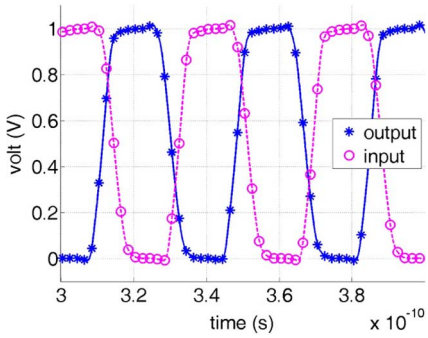

Fig. 18. Amplifier large-signal transient response.

TABLE III
CHARACTERISTICS OF SGFETS WITH BSIMSOI MODELING

parameters	nmos	pmos
I_{off} (V_{GS}=0V and V_{DS}=1V)	540 pA	80 pA
I_{ds} (V_{GS}=0.5V and V_{DS}=0.5V)	2 μA	0.7 μA
g_m (V_{GS}=0.5V and V_{DS}=0.5V)	14 μA/V	8 μA/V
r_{ds} (V_{GS}=0.5V and V_{DS}=0.5V)	400 kΩ	1.1 MΩ
f_τ	36 THz	25 THz
f_{max}	120 THz	100 THz
CMOS Amplifier Area	70nm×144nm	
Amplifier Power Dissipations	1.64μW	
3dB Bandwidth	500GHz	
3rd Order Intermodulation Distortions	−24dBm for f_2–f_1=10GHz	
Small-Signal DC Gain	−6.5	
Large-Signal Delay	2.2ps	
Large-Signal Rise Time	5.4ps	
Large-Signal Fall Time	4.7ps	
Rail-to-Rail Swing	1V	

VI. CONCLUSION

The vertical silicon nanowire transistors produce less short-channel effects and static power dissipation compared with nanoscale planar bulk MOSFETs, and therefore, they are considered as possible candidates for next-generation low-power and high-speed VLSI technologies. SGFETs are also easy to fabricate and provide full gate control over the channel that are important factors to achieve close-to-ideal subthreshold slope and low DIBL. To characterize the merits of nanoscale SGFETs for analog and RF applications, there is a need to generate accurate SPICE models for transistors with channel lengths approaching 10 nm range.

This paper presented an accurate SPICE modeling of NMOS and PMOS SGFETs with 10 nm channel length and 2 nm channel radius. The fully depleted BSIMSOI parameters were extracted from input and output I–V characteristics obtained from 3-D Silvaco Atlas device simulations. The distributed RC parasitics of the NMOS and PMOS transistors were calculated and added to the SPICE models as subcircuits. The low-frequency,

high-frequency, small-signal, and large-signal characteristics of the NMOS and PMOS SGFETs were measured to demonstrate the capabilities and merits of these transistors for high-speed analog and RF applications.

When biased at $V_{\rm ds} = 0.5$ V and $V_{\rm gs} = 0.5$ V, the NMOS and PMOS SGFETs exhibited 2 and 0.7 μA drain currents, 14 and 8 μA/V transconductances, 400 kΩ and 1.1 MΩ output resistances, 36 and 25 THz unity-current-gain cutoff frequencies, and 120 and 100 THz maximum frequency of oscillations, respectively. A simple single stage CMOS SGFET amplifier dissipated 1.64 μW power and showed 500 GHz bandwidth with -6.5 gain and -24 dBm third-order intermodulation distortion tones for a two-tone input signal with 10 mV amplitude and 10 GHz frequency spacing. The large-signal operation of the amplifier with 1 V output swing exhibited 2.2 ps delay, 5.4 ps rise time, and 4.7 ps fall time, while oscillating at 30 GHz. All these results indicated the potential use of vertical nanowire SGFETs in high-speed and low-power next-generation VLSI technologies.

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