UNIVERSITY OF CALIFORNIA, BERKELEY

College of Engineering

Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey **Homework #6** **EECS 141 (SP10)**

Due Friday, March 19 , 5pm, box in 240 Cory

[PROBLEM 1] Pass Transistor Logic

Consider the pass transistor logic implemented in a CMOS process as shown in Fig.1. Assume that $V_{TN}=|V_{TP}|=0.3V$. Ignore body effect, but **don't ignore V_T drop** in pass transistor logic. V_{DD} =1.2V (45 pts)

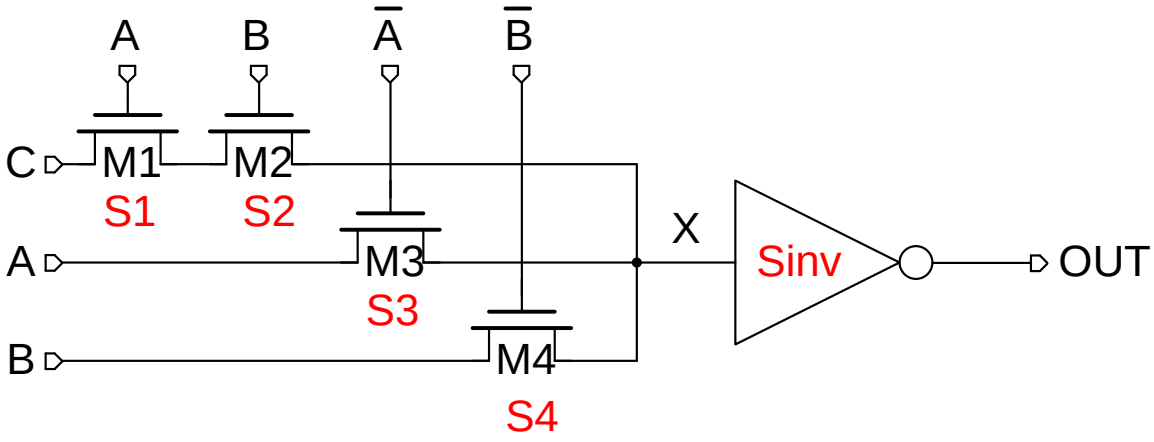
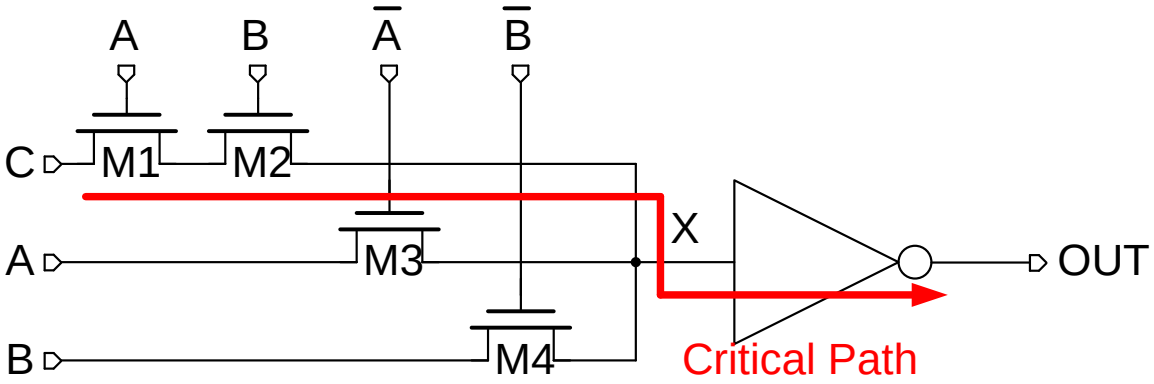


Fig.1.

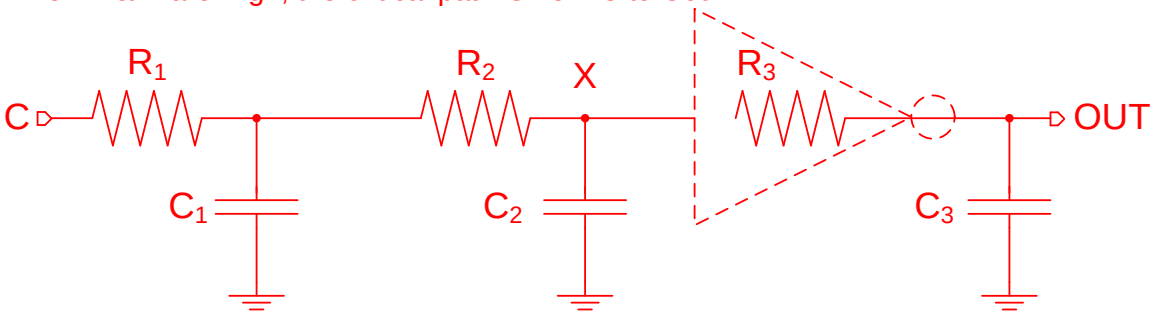
(a) What is the logic function performed by this circuit? (5 pts)
OUT = $\overline{(A \cdot B \cdot C)}$ = $\overline{A}$ + $\overline{B}$ + $\overline{C}$

(b) What is the purpose of having the two branches controlled by $\overline{A}$ and $\overline{B}$? (5 pts)
Without two branches, X node is floated (or open) when A or B is Low.

(c) If OUT drives a large C_L, derive an approximate expression for the worst-case propagation delay of the whole circuit. Assume the following parameters for the minimum-size NMOS and PMOS transistors, S=1: R_{eqn}=10kΩ, R_{eqp}=20kΩ, $C_{gs}=C_{gd}$=1fF; $C_{db}=C_{sb}$=1fF. The inverter is symmetrical sized, i.e. PMOS:NMOS=2:1. Ignore the miller effect at input and output of the inverter. Ignore overlap capacitances and feed-through from the gates of the switching transistors to the circuit nodes. (10 pts) (**Hint:** you may model the circuit as RC networks. Provide the delay expression in terms of R_{eq} and parasitic Cgs and Cgd of a transistor, i.e. use simple pass transistor model in prob.1(b) of HW#5.)



When A & B are High, the critical path is from C to Out.



,where R1 = $R_{ON,N}$/S1=10k/S1,

C1 = S1*(Cgd1+Cdb1)+S2*(Cgs2+Csb2)=2f*(S1+S2),
R2 = $R_{ON,N}$/S2=10k/S2,
C2 = S2*(Cgd2+Cdb2) + S3*(Cdb3) + S4*(Cdb4) + 3*Sinv*(Cgd,inv+Cgs,inv)
= 2f*S2 + 1f*S3 + 1f*S4 + 6f*Sinv
R3 = Rinv = 10k/Sinv
C3 = Cint = 3f*Sinv

Delay = ln(2) * [R1*C1 + (R1+R2)*C2 + R3*C3]

(d) Explain qualitatively how you would like to size the pass transistors, S1 and S2. Derive relationship transistors' size. (5pts)

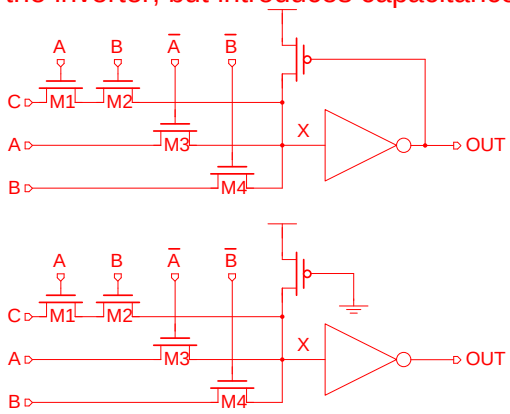
R1 < R2 (S1>S2) because R1 appears in both C1 and C2.
S2 is chosen to be minimum size in order to reduce capacitance.
Sinv is also chosen to be minimum size in order to reduce capacitance because this inverter does not drive other loading capacitor.

(e) Discuss the sources of static power dissipation in the circuit. (5pts)

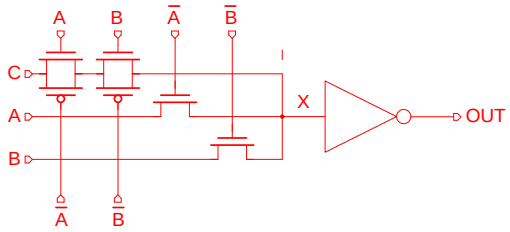
Because Vx = VDD – VT, there is short circuit current in the output inverter.

(f) Propose two circuit modifications to improve the performance and power dissipation of the circuit, and discuss the pros and cons of each of them. (5pts)

i) Keeper: the size should be minimized in order not to impact performance too much. It improves power consumption by removing short circuit current of the inverter, but introduces capacitance in node X.



ii) Transmission gate: TG improves the power due to eliminating the short circuit current. Although the C1 & C2 increases, the R1 & R2 reduces as well.



(g) What are the impacts on the performance and power consumption of this circuit if the threshold voltage of M1, M2, M3, and M4 is lowered? Assume that inverter has the same threshold voltage for nMOS and pMOS. (5pts)

If Vth is lowered, Vx is increased by that amount. So short circuit current is reduced.
Moreover, the reduced Vth decreases Ron of pass transistors, so delay will be reduced.

(h) What is minimum supply voltage for which this circuit is still operational? Show your line of thought. Assume that the inverter switches only when input is $V_{DD}/2$.(5pts)

The maximum Vx = VDD - VT
Therefore, VDD-VT > VDD/2, so VDD > 2VT.

[PROBLEM 2] Pass transistor gate with level restorer

Consider the circuit in Fig.2. Let Cx = 50fF. M1 has W/L=0.5/0.25, and M2 has W/L = 0.5/0.5. Assume the output inverter doesn't switch until its input equals $V_{DD}/2$ (V_{DD} =2.5V). Use unified model. (30pts)

NMOS:
VTn = 0.5, *k'n* = 100 μA/V2, $V_{D,VSAT}$ = 0.6V, λ=0V, γ=0.4$V^{1/2}$, $2\Phi_F$ = −0.6V
PMOS:
VTp = −0.5V, *k'p* = −40 μA/V2, $V_{D,VSAT}$ = −1V, λ = 0, γ = -0.4$V^{1/2}$, $2\Phi_F$ = 0.6V

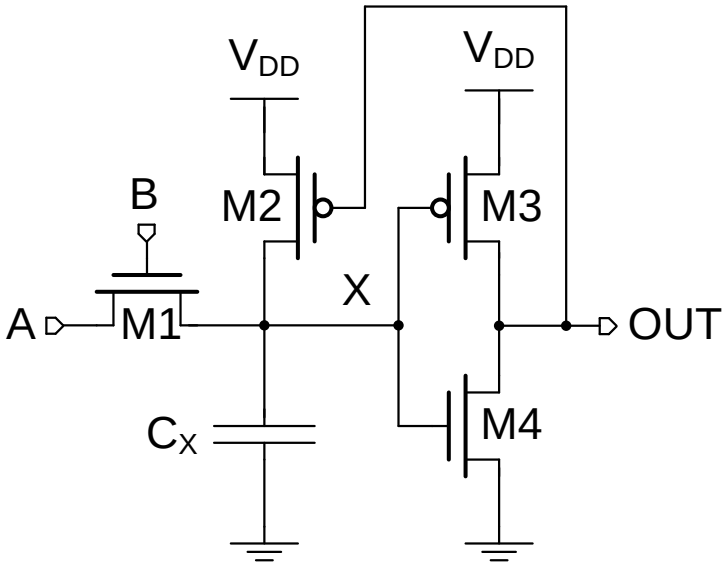


Fig.2.

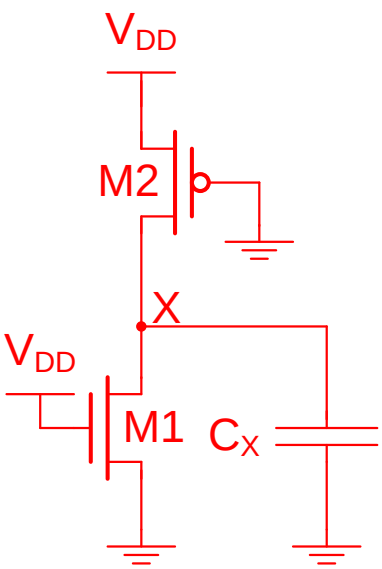
(a) What is the function of M2? (5pts)

Level restorer avoids static power consumption.

(b) Describe qualitatively how this circuit operates for H→L and L→H input transitions.B is at 2.5V (5pts)

When V_A goes from H→L, Vx is slowly discharged due to the stronger Mn, and then Vout is charged to towards VDD, which turns off Mr. Finally Vx is discharged to 0.
When V_A goes from L→H, Vx is charged toward VDD-Vt and Vout goes to 0, which turns on M2 and helps charging Vx to VDD.

(c) How long will it take M1 to pull node x down from 2.5V to 1.25V if 2.5V to 0V step input is applied to A, and B is at 2.5V? (5pts)



Find V_{OL} ; @ V_{OL}, M2 is velocity Saturation, and M1 is in linear region.
$Kp'*(W/L)_2*(VDD-Vtp-Vdsatp/2)*Vdsatp=Kn'*(W/L)_1*(VDD-Vtn-V_{OL}/2)* V_{OL}$
$40u*(0.5/0.5)*(2.5-0.5-1/2)*1=100*(0.5/0.25)*(2.5-0.5- V_{OL}/2)* V_{OL}$
$\therefore V_{OL}=0.015\ V\approx 0V$

For M2,
@Vx=VDD: Id,begin=0 (Vds=0, linear region)
@Vx=VDD/2: Id,final=Idsat,p=60(uA)

For M1,
@Vx=VDD: Id,begin=204(uA)
@Vx=VDD/2: Id,final=204(uA) (because $\lambda=0$)

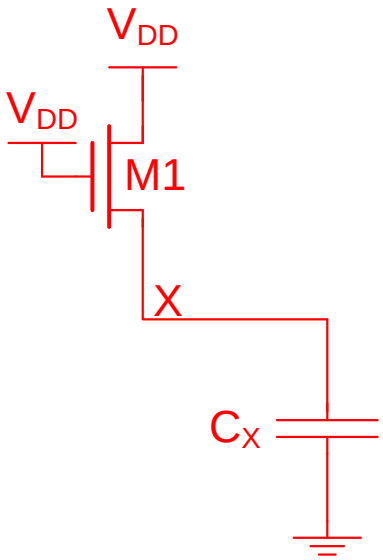
Req,begin = Vdd/204uA ≈ 12.3 kΩ
Req,final = VDD/2 / (204.4uA - 60uA) = 8.7 kΩ
Req = (12.3k+8.7k)/2 = 10.5 kΩ

τ = Req*Cx = 10.5k * 50f = 525pS

$VDD/2 = VOL + (VDD-VOL)\exp(-tpHL/\tau) \approx 2.5*\exp(-tpHL/525p)$

$\therefore$ tpHL = ln(2)*525pS = 364 pS

(d) How long will it take M1 to pull node x up from 0 to 1.25V if 0V to 2.5V step input is applied to A, and B is at 2.5V? (5pts)



For M1,
Req,begin = Vdd/204uA ≈ 12.3 kΩ (velocity saturation)
Req,final = VDD/2 / 26.63uA = 46.9 kΩ
(saturation because min(V_{GT},V_{DVSAT},V_{DS})=V_{GT})
where V_T@VDD/2 = 0.5+0.4(sqrt(1.25+0.6)-sqrt(0.6))=0.734V

Req = (12.3k+46.9k) / 2 ≈ 29.6 kΩ

τ = Req*Cx = 29.6k * 50f = 1480 pS
∴tpLH = ln(2) * 1480pS = 1026 pS

(e) What is the minimum value of V_B(Voltage of B input) necessary to pull Vx down to 1.25V when V_A=0V? (5pts)

To pull down Vx, Id of M1 has to be greater than Id of M2 when Vx = VDD/2
Id of M2 = 60 uA (from Part c)
Id of M1 = Kn'(W/L)(VB-Vtn-Vdsatn/2)Vdsatn ≥ 60uA
VB ≥ 1.3 V

(f) If node B is at 2.5V, what is the maximum size of M2 such that the circuit still operates as intended? (5pts)

Id,M1 > Id,M2
Id,M1 = 204 uA (from part c)
Id, M2 = Kp'(W/L)(VDD-Vtp-Vdsatp/2)Vdsatp ≤ 204 uA
(W/L) <= 3.4

[PROBLEM 3] Dynamic Logic

Consider the domino circuit in Fig.3. Assuming that all inputs of the circuit shown in Fig.3 are initially Low (0V) during the pre-charge phase and that all internal nodes are at 0V. Ignore all other parasitic capacitance except C_1, C_2, and C_3. It is given that V_{DD}=2.5V, V_{tn0}=0.5V, $2\varphi_F$=0.6V and γ=0.4V$^{0.5}$. (25pts)

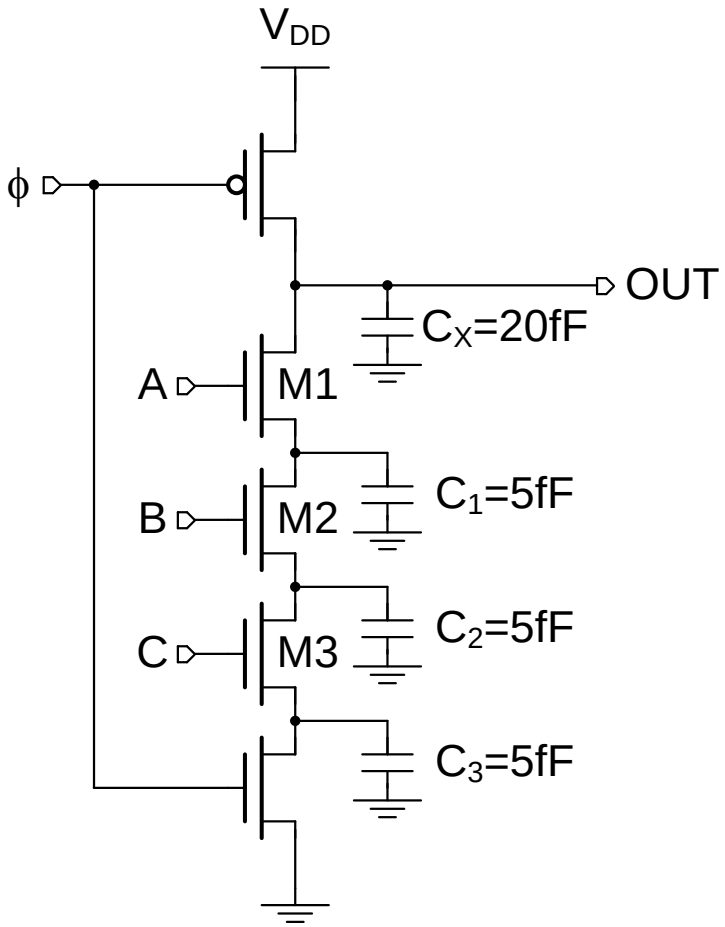


Fig.3.

(a) Calculate the voltage drop on V_{out} (OUT node voltage) if A changes to High (2.5V) during the evaluation phase. (10pts) (**Hint:** Don't forget the body effect.)

Assuming that ΔVout < Vtn, the capacitor C1 is charged to a voltage Vs (=VDD-Vtn), which is the maximum voltage for which M1 conducts. The Vs is calculated by using the equation that is valid at the edge of conduction and cut-off:

$$V_{GS} = V_{tn}$$

$$\Rightarrow V_{GS} = V_{tn0} + \gamma\left(\sqrt{|2\varphi_F + V_{SB}|} - \sqrt{|2\varphi_F|}\right)$$

Since the bulk of the NMOS transistors is connected to ground, the previous equation can be rewritten as:

$$V_G - V_S = V_{tn0} + \gamma\left(\sqrt{|2\varphi_F + V_S|} - \sqrt{|2\varphi_F|}\right)$$
$$\Rightarrow V_G - V_S - V_{tn0} + \gamma\sqrt{|2\varphi_F|} = \gamma\left(\sqrt{|2\varphi_F + V_S|}\right)$$
$$\Rightarrow \left(V_G - V_S - V_{tn0} + \gamma\sqrt{|2\varphi_F|}\right)^2 = \gamma^2(2\varphi_F + V_S)$$
$$\Rightarrow V_S^2 - 4.78V_S + 5.234 = 0$$
$$\Rightarrow V_S = \frac{4.78V - 1.38V}{2} = 1.7V$$

(We accept only the lower solution of the quadratic equation, since after reaching this voltage the transistor doesn't conduct and can't thus reach the higher value).

Hence, charge conservation yields:

$$C_X V_{DD} = C_X V_o + C_1 V_S$$
$$\Rightarrow C_X \Delta V_o = C_1 V_S$$
$$\Rightarrow \Delta V_o = C_1 V_S / C_X = 0.43V$$

Since $V_{GS} = V_{tn} = 0.8V$, our assumption about $\Delta V_o < V_{tn} = 0.8V$ was correct.

(b) Calculate the voltage drop on V_{OUT} (OUT node voltage) if both A and B change to High (V_{DD}=2.5V) (5pts).

Similarly to (a), capacitors C_1 and C_2 will be charged to a final voltage of $1.7V$. Hence, charge conservation gives:

$$C_X \Delta V_o = C_1 V_S + C_2 V_S \Rightarrow \Delta V_o = 0.851V > V_{tn}$$

Hence, our assumption that $\Delta V_{out} < V_{tn}$ doesn't hold anymore and ΔV_o is calculated as follows:

$\Delta V_o = V_{DD} \dfrac{C_s}{C_s + C_X}$, where $C_s = C_1 + C_2$.

Hence,

$$\Delta V_o = 2.5V \frac{10}{10 + 20} = 0.83V$$

(c) What is the maximum number of transistors that can be connected in series to M1 and M2 (including M1 and M2, excluding M3) if the output should not fall below 0.9V during the evaluation phase? Assume that each one of the new transistors has the same intrinsic capacitance (to ground) as M1 and M2 (C=5fF). (10pts)

The final value of Vo=0.9V corresponds to ΔVo=1.6V > Vtn. Hence, the following equation is valid:

$$\Delta V_o = V_{DD} \frac{C_s}{C_s + C_X}$$

where C_s the total intrinsic capacitance to be charged.

The worst case is when all of the connected transistors conduct and thus Cs=N*C (where *N* the number of the transistors). In this case (1) gives:

$$\Delta V_o (NC + C_X) = V_{DD} NC$$
$$\Rightarrow NC(V_{DD} - \Delta V_o) = \Delta V_o C_X$$
$$\Rightarrow N = \frac{1.6V \times 20\,fF}{0.9V \times 5\,fF} = 7.1$$

, hence *N* = 7.