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TuTh9:30-11am

EECS 141: SPRING 03—MIDTERM 1

NAME	Last First

SID	

Problem 1 (on 12):

Problem 2 (on 9):

Problem 3 (on 9):

Total (on 30)	

PROBLEM 1: Power (12 pts)

Consider the circuit of Fig. 1. The signal waveforms of each signal within one period are shown in Fig. 2. You may assume that these signals are repeated with a frequency of 1 MHz (or T = 1 μs). Use the following device parameters: V_T = 0.5 V; γ = 0; R_{on} = 10 kΩ; R_{off} = ∞.You may ignore the parasitic capacitances of the transistors.

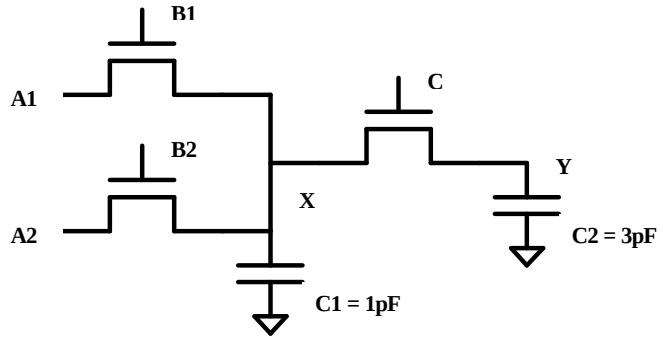


Fig. 1

a. Draw the waveform of the signals on nodes *X* and *Y*, assuming that all input signals are switching between 0 and 2.0 V**.** (4 pts)

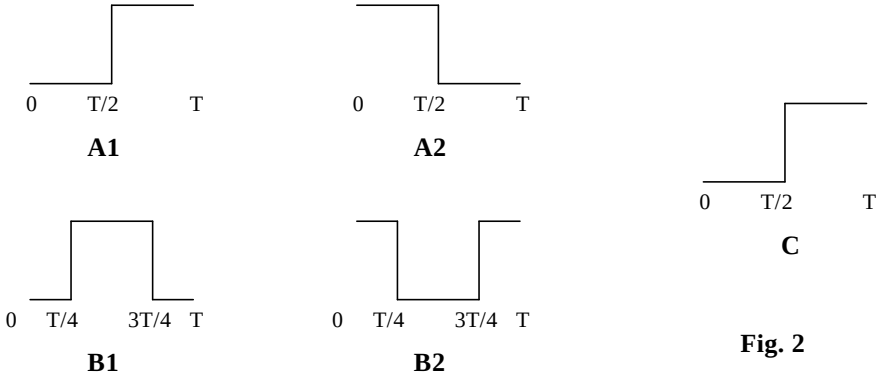
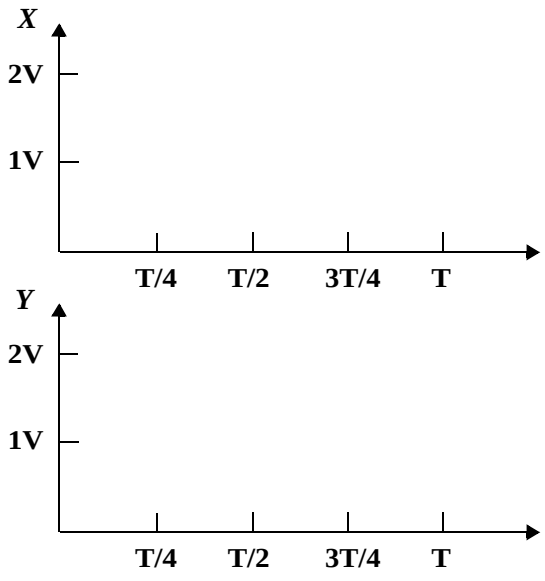


Fig. 2



b. Calculate the dynamic power dissipation of this circuit. (2 pts)

P_{dyn}=

c. The power consumption of the CMOS inverter can be minimized through circuit optimizations. Determine how each circuit parameter mentioned in the table should be changed to reduce the different inverter power consumption components (6 pts)

For each parameter, fill in one of the following choices in the blanks:
A – Increase **B** – Decrease **C** – Doesn't affect this type of power consumption

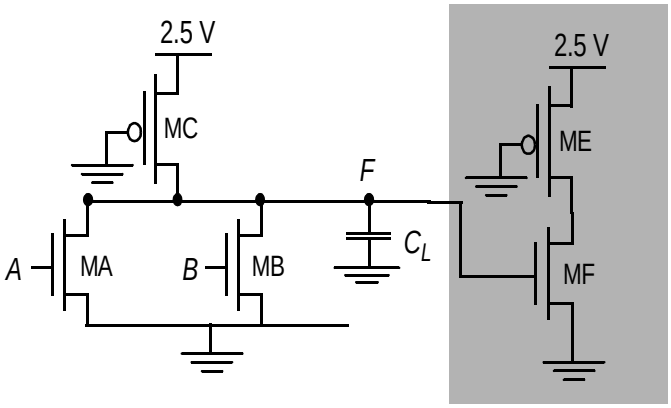
Goal	Circuit Parameter Optimization	A, B or C
Minimize the dynamic power consumption due to C_L charging and discharging	Vdd C_L Transistor $\|V_{th}\|$ Transistor widths (first order)	
Minimize the direct-path power consumption (assume a fixed rise and fall time at the input)	Vdd C_L Transistor $\|V_{th}\|$ Transistor widths	
Minimize the static power dissipation	Vdd C_L Transistor $\|V_{th}\|$ Transistor widths	

PROBLEM 2: VTC and propagation delay (9 pts)

Consider the digital circuit shown below. It pictures an alternative 2-input NOR gate followed by a single fanout inverter. To make the analysis of this circuit easy, we are using simplified transistor models. First, of all we assume that the transistor can be represented by a linear resistor, this is

NMOS (for W/L = 1): RN_{on} = 10 kΩ; RN_{off} = ∞; V_{TN} = 0.75V.

PMOS (for W/L = 1): RP_{on} = 20 kΩ; RP_{off} = ∞; V_{TP} = -0.75V.



a. Assume that the PMOS is of minimum size (this is, W/L = 1). Determine the sizes of the two NMOS transistors MA and MB so that the V_{OL} of the NOR gate is **at most** 0.5 V. Also describe under what conditions this happens. (2pts).

$(W/L)_{MA}$=
$(W/L)_{MB}$=

b. The parasitic capacitances of a unit size NMOS and PMOS transistor are given in the table below. You may assume that **all capacitances are constant and linear over the operation range**. Determine the equivalent load capacitance C_L at the output of the NOR gate (i) for A switching from 0→1, and B = 0; (ii) for A and B switching simultaneously from 0 → 1. You should use the sizes derived in a. for both the NOR gate and the fanout inverter. (4 pts)

Hint: In case you are not sure about your answer in a, use $(W/L)_{NMOS}$ = 3.

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Table 1: Transistor capacitances (for W/L = 1)

Cap in fF	C_{gs}	C_{gd}	C_{gb}	C_{sb}	C_{db}
NMOS	0.1	0.15	0.2	0.25	0.3
PMOS	0.12	0.17	0.22	0.27	0.32

$\mathbf{CL}_{(\text{A: } 0\rightarrow 1;\ \text{B=0})}$ =

$\mathbf{CL}_{(\text{A,B: } 0\rightarrow 1)}$ =

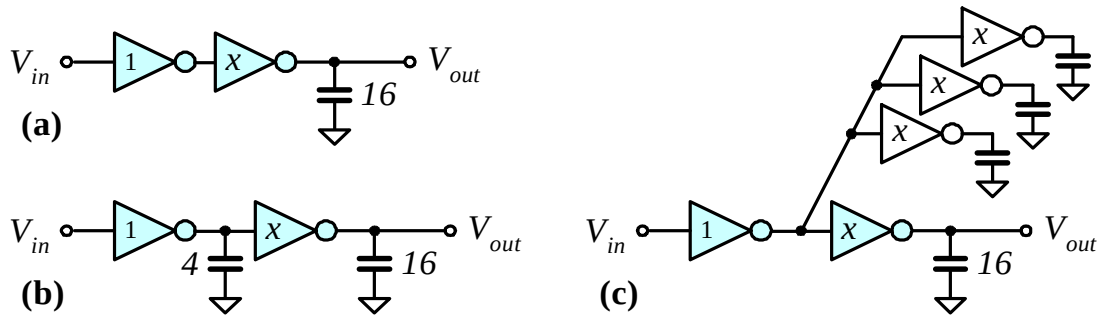
c. Determine the propagation delay of the NOR gate for *A* switching from 0→1 and 1→0, while *B*=0. For C_L, use the answer you got in b. If not sure, use C_L = 8 fF. You may assume that the VM of the gate is approximately at VDD/2. (3 pts)

$\mathbf{tp}_{0\rightarrow 1}$=

$\mathbf{tp}_{1\rightarrow 0}$ =

PROBLEM 3: Sizing (9 pts)

The circuits shown in the figure below illustrate the impact of small topological changes on the delay and energy, when driving a fixed load at the output. You may assume that $\gamma = 1$ (or $C_{intrinsic} = C_{gate}$). For each of the circuits in the Figure, calculate following:



a. Size ***x*** of the second inverter in the chain to minimize propagation delay from input V_{in} to output $V_{out.}$ (6 pts)
Hint: do not blindly use the equations given in the book.

x (a) =
x (b) =
x (c) =

b. Energy consumed by the shaded path in all three cases (3 pts). You may assume that V_{DD} = 1 V, and that the capacitances are given in fF. (3pts).

E (a) =
E (b) =
E (c) =