Quantification of figures of merit of 7T and 8T SRAM cells in subthreshold region and their comparison with the conventional 6T SRAM cell

Pulkit Sharma, R. Anusha, K. Bharath, Jasmine K. Gulati, Preet K. Walia, Sumit J. Darak
ECE Department, Indraprastha Institute of Information Technology Delhi, India (IIIT-Delhi)

***Abstract*—The need for low-power SRAM results in many design challenges in deep submicron technology. In this paper, 6T, 7T and 8T SRAM cells designed in 65nm bulk CMOS technology in the subthreshold region have been compared on the basis of various Figures of Merit (FoMs). The 7T and 8T SRAM cells are able to work at 200mV with 8T exhibiting highest Read Static Noise Margin (RSNM), Hold Static Noise Margin (HSNM) and Write Noise Margin (WNM). All cells result in low leakage in the subthreshold region. Statistical Analysis has been carried out to examine the effect on RSNM due to on-die parametric fluctuations.**

Index terms: RSNM, Subthreshold, SRAM, Statistical Analysis.

I. INTRODUCTION

Subthreshold SRAM design has appeared as a finer solution for low-power applications. However, this imposes challenges in the design of memory cell, which include small margins, poor cell stability, writeability and bit-line voltage swing. Further, it results in exponentially increased variations in performance and power.This paper presents 6T, 7T and 8T SRAM cells in section II. Section III presents simulation results comparing 6T cell with 7T and 8T cells in the subthreshold region on the basis of various FOMs. Statistical analysis of the three SRAM cell configurations is done to analyze the effect of fluctuation of threshold voltage (V_t) due to manufacturing anomalies and Random Dopant Fluctuations (RDF) in the channel region of transistors. Finally the paper is concluded in section IV.

II. DIFFERENT SRAM CELLS

This section presents the conventional 6T SRAM cell [1] and 7T [2], 8T [3] cells designed for low power applications. Fig. 1 depicts the circuit of all the three cells and table I tabulates their transistor sizes.

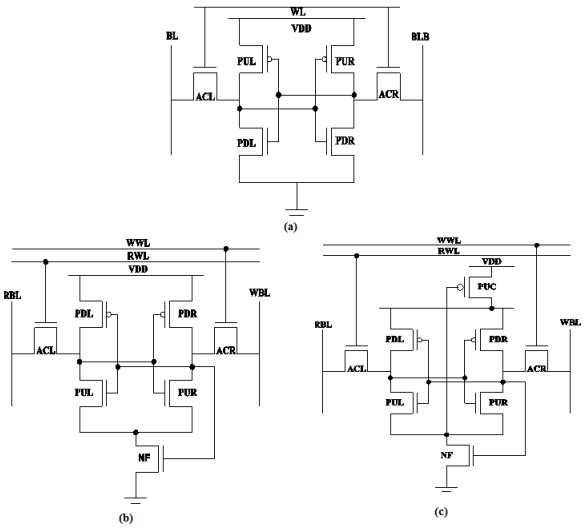

Fig. 1: (a) 6T SRAM cell (b) 7T SRAM cell (c) 8T SRAM cell

TABLE I: Widths of transistors of different SRAM configurations

Devices	Width (nm)		
	6T	7T	8T
PDL	200	200	200
PDR	200	180	180
ACL, ACR	150	150	150
PUL	135	135	135
PUR	135	120	120
NF	X	200	200
PUC	X	X	135

III. SIMULATION RESULTS

A. Results for different F0Ms

Fig. 2 depicts the WNM, RSNM, HSNM and leakage power for the three cells for different supply voltages (V). The 8T cell exhibits the highest RSNM, 1.3X than that of 6T cell and 1.16X higher than the 7T cell. In subthreshold regions, 6T cell and 7T cell behave almost similar in terms of RSNM. 8T cell has highest HSNM, around 1.16X of HSNM of 6T cell in the subthreshold region, whereas HSNM of 6T cell and 7T cell are almost same for all V. WNM of 8T is found to be 1.67X better than that of 6T and 7T has 1.6X better write margin as compared to 6T cell. Table II, III and IV tabulate the results for Read time, Read current and Write time respectively. Read currents for all the three cells are almost same. 8T cell results in no excess leakage power in and out of subthreshold regions because of stacking effect, whereas 7T cell exhibits 1.12X more leakage in the subthreshold region compared to 6T cell. Simulations are done using Cadence Virtuoso.

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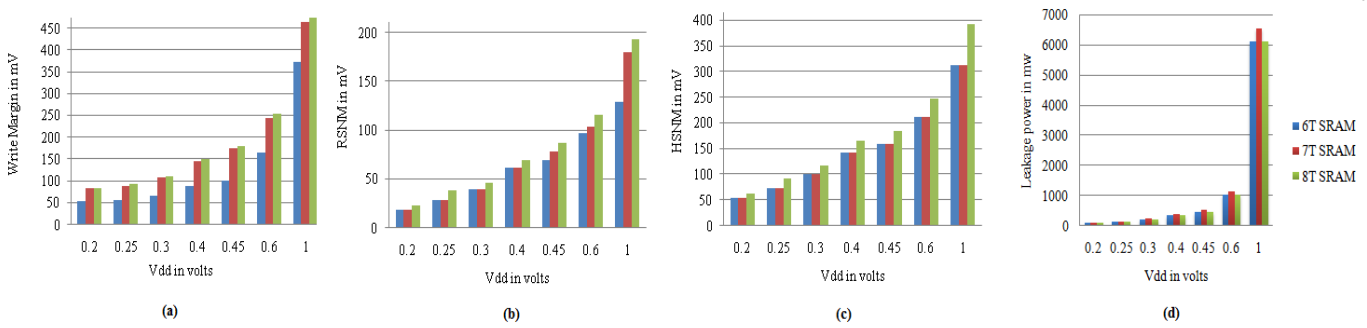

Fig. 2: FoMs of three SRAM cells (a) Write Margin (b) RSNM (c) HSNM (d) Leakage Power

TABLE II: Read time of 8T, 7T SRAM cells versus standard 6T SRAM cell

V	6T Read Time (ns)	7T Read Time (ns)	8T Read Time (ns)
0.2	1108	1287	1000
0.25	393	460.46	450
0.3	146	172.417	150
0.4	29	38.73	30
0.45	15	16.99	15
0.6	6	7,163	5.5
1	3	4.83	3.4

TABLE III: Read currents of 8T, 7T SRAM cells versus standard 6T SRAM cell

V	6T Read Current (mA)	7T Read Current (mA)	8T Read Current (mA)
0.2	0.034	0.029	0.035
0.25	0.123	0.118	0.122
0.3	0.386	0.377	0.396
0.4	2.77	2.72	2.7
0.45	5.72	5.79	5.8
0.6	22.77	21.6	20
1	85.62	82.5	80

B. Statistical Analysis

Using Monte Carlo simulations, random fluctuations in (V_t) are induced and correspondingly RSNM (R) values are sampled. Assuming R to be a Gaussian random variable. Let p_r be the probability of RSNM deviating below 50mV due to the fluctuations in V_t.

Then, $p_r = P(R < t) = \int_{-\infty}^{t} f_R(r)dr$ where $t = 50mV$ and $f_R(r)$ is the probability density function (PDF) of R. Table V depicts the mean and standard deviation of R. Fig. 3 depicts the PDF of R and p_r for all the three cells. It can be seen that p_r for 8T is about $1.433 * 10^{-3}$ and that for 7T and 6T is $1.977 * 10^{-3}$ and $1.460 * 10^{-2}$ respectively.

TABLE IV: Write time of 8T, 7T SRAM cells versus standard 6T SRAM cell

V	6T Write (ns)	7T Write '0' (ns)	7T Write '1' (ns)	8T Write '0' (ns)	8T Write '1' (ns)
0.2	21.73	40.28	19.65	37.5	30
0.25	7.15	15.25	6.8	13	11.5
0.3	2.5	7	2.3	5	3.5
0.4	0.49	2.42	0.6	1.12	0.72
0.45	0.27	1.52	0.43	0.6	0.4
0.6	0.12	0.89	0.16	0.29	0.16
1	0.06	0.75	0.09	0.14	0.09

TABLE V: Mean (μ) and standard deviation (σ) of R

Cell	μ (mV)	σ (mV)
6T	108.6	24.9
7T	124.7	24.5
8T	143.1	29.8

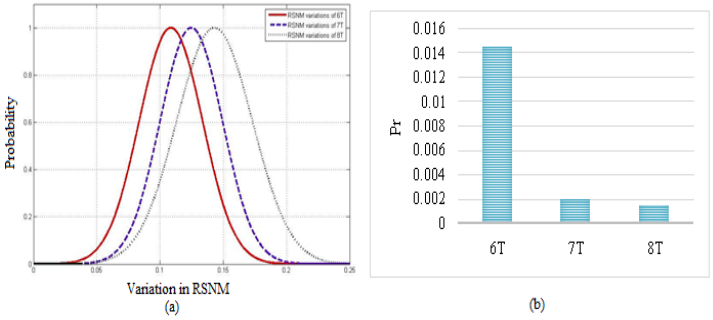

Fig. 3: (a) PDF of R (b) Trend showing P_r for the three SRAM cells

IV. Conclusion

This paper compares 6T, 7T and 8T SRAM cells in and out of subthreshold regions on the basis of various FoMs. It can be concluded that 8T cell performs the best in terms of noise margins without compromising in leakage power and read time but with a penalty of write time as compared to 6T SRAM cell. 7T cell shows better WNM and RSNM but at the cost of more leakage power, read time and write time. Statistical analysis suggests that 8T and 7T cells are more resilient to on-chip parametric variations-induced RSNM fluctuations as compared to standard 6T cell.

References

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