EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 17: DAC 3

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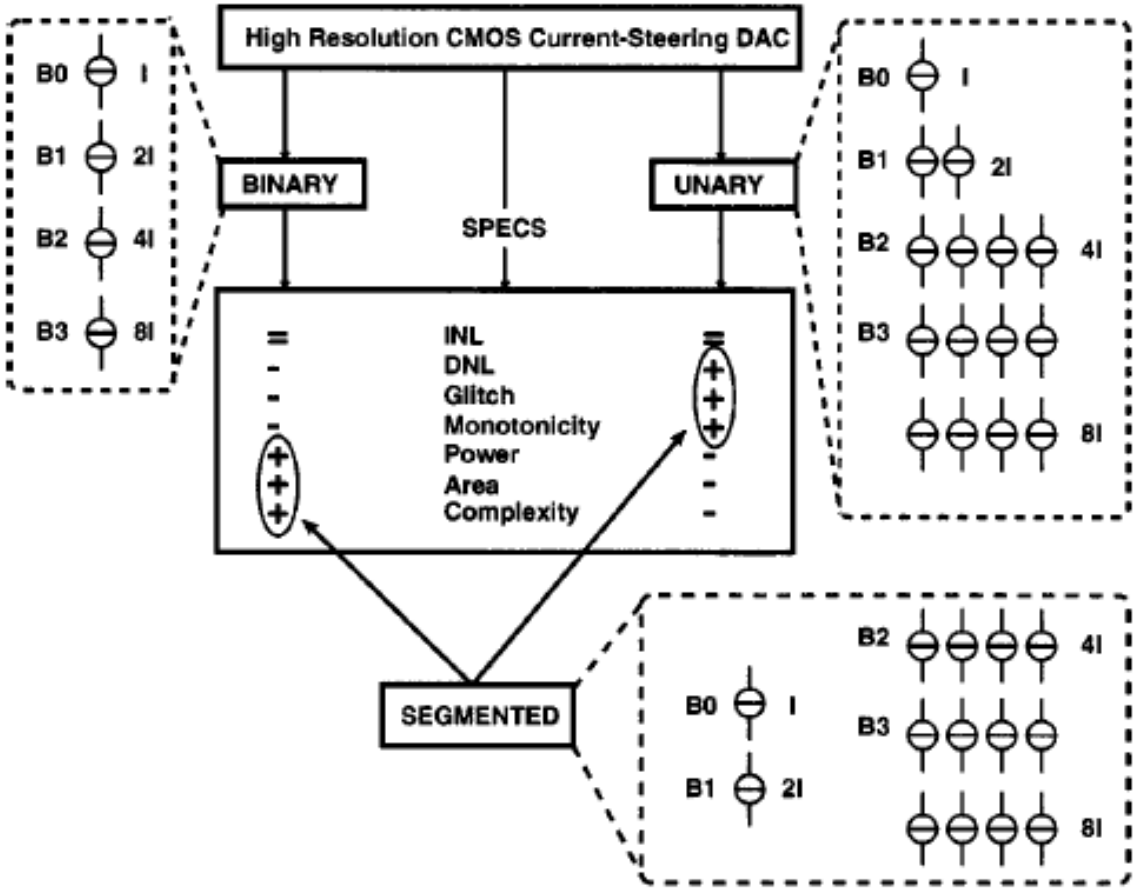
Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	~~Finish Flash ADC~~
28-Feb	~~DAC Architectures - Resistor, R-2R~~
5-Mar	~~DAC Architectures - Current steering, Segmented~~
7-Mar	~~DAC Architectures - Capacitor-based~~
12-Mar	~~SAR ADC with bottom plate sampling~~
14-Mar	~~SAR ADC with top plate sampling~~
19-Mar	~~Midterm Review~~
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	~~Pipelined ADC stage - comparator, MDAC, x2 gain~~
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

DAC 3

DAC Architectures Comparison

4bit Example



Binary Weighted vs Unit Element

Binary-weighted DAC

- Pros
  - Min. # of switched elements
  - Simple and fast
  - Compact and efficient
- Cons
  - Large DNL and glitches
  - Monotonicity not guaranteed
- INL/DNL
  - INL(max) ≈ $(\sqrt{N}/2)\sigma$
  - DNL(max) ≈ 2*INL

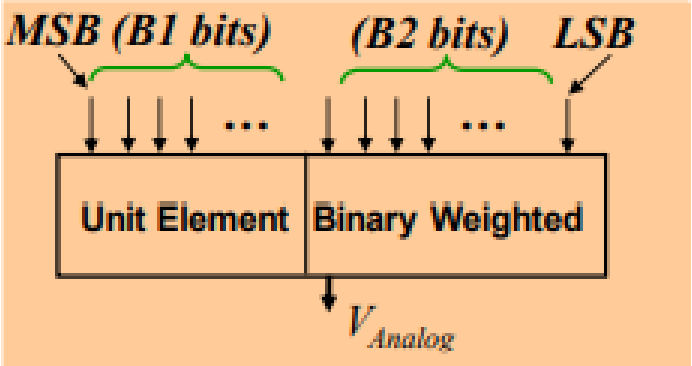
Unit-element DAC

- Pros
  - Good DNL, small glitches
  - Linear glitch energy
  - Guaranteed monotonic
- Cons
  - Needs B2T decoder
  - complex for N ≥ 8
- INL/DNL
  - INL(max) ≈ $(\sqrt{N}/2)\sigma$
  - DNL(max) ≈ σ

Combine BW and UE architectures → Segmentation

Segmented DAC

- Objective:
  Compromise between unit-element and binary-weighted DAC



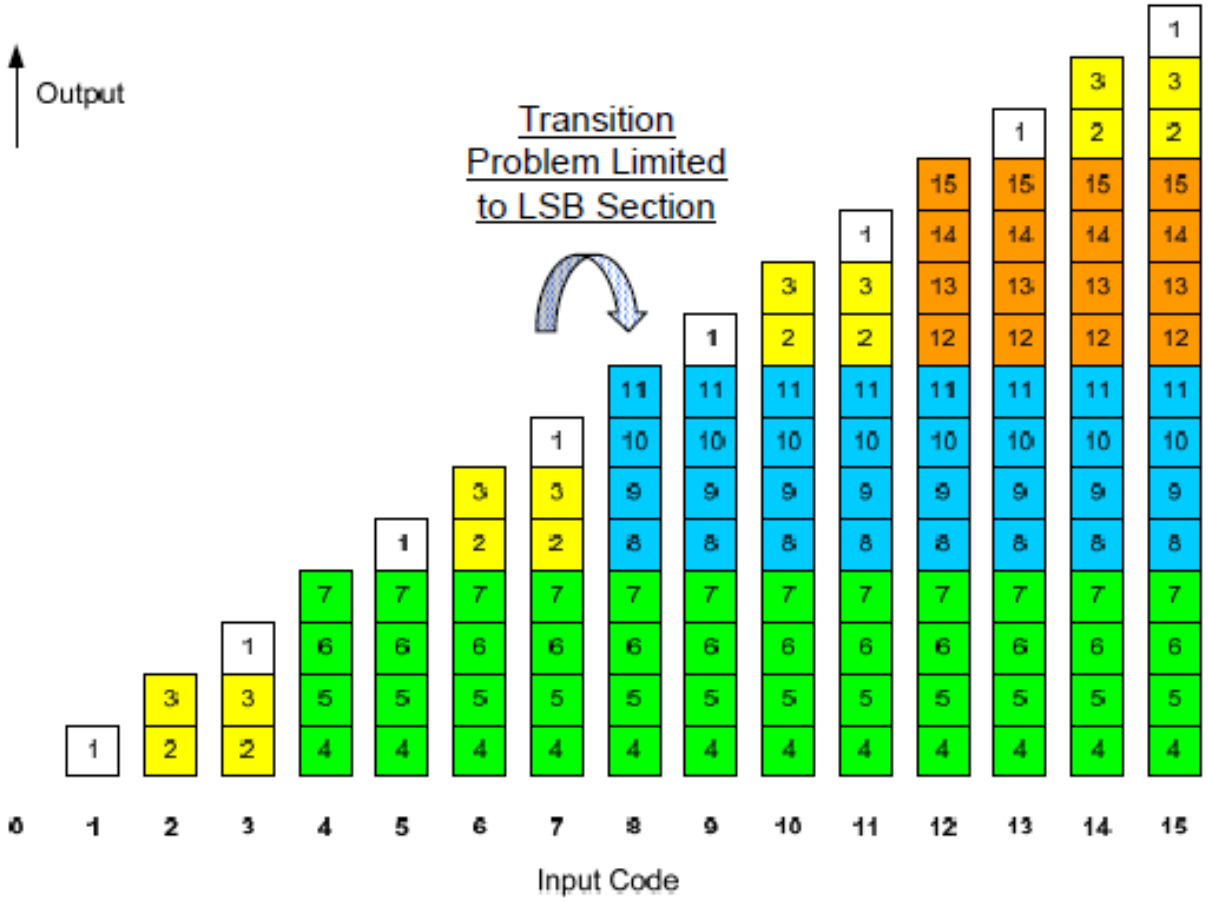
- Approach:
  B_1 MSB bits → unit elements
  B_2 LSB bits → binary weighted

$B_{Total} = B_1 + B_2$

- INL: unaffected same as either architecture
- DNL: Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on → Same as binary weighted DAC with (B_2+1) # of bits
- Number of switched elements: $(2^{B1}-1) + B_2$

Segmented DAC Principle

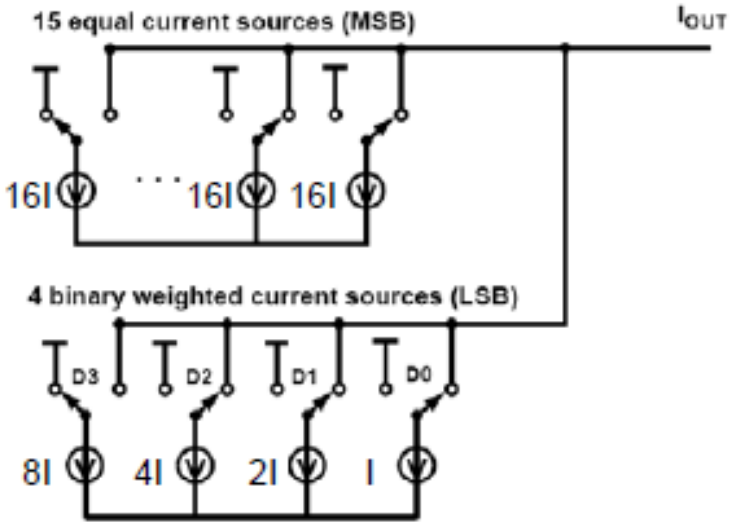
4bit Example (2+2)



DNL/INL of Segmented DAC

- INL
  - Same as in thermometer DAC
- DNL
  - Worst case occurs when LSB DAC turns off and one more MSB DAC element turns on
  - Essentially same DNL as a binary weighted DAC with B_b+1 bits

Example: $B=B_b+B_t=4+4=8$



INL/DNL Comparison Table

	Thermometer	Segmented	Binary Weighted
σ_{INL} (worst case)	$\cong \frac{1}{2}\sigma_u\sqrt{2^B}$		
σ_{DNL} (worst case)	$\cong \sigma_u$	$\cong \sigma_u\sqrt{2^{B_b+1}-1}$	$\cong \sigma_u\sqrt{2^B-1}$
Number of Switched Elements	2^B-1	$B_b+2^{B_t}-1$	B

- INL is same for all architectures
- DNL of Binary-weighted DAC is 2 times the DNL

Example INL/DNL Comparison

($B=12$, $\sigma_u=1\%$)

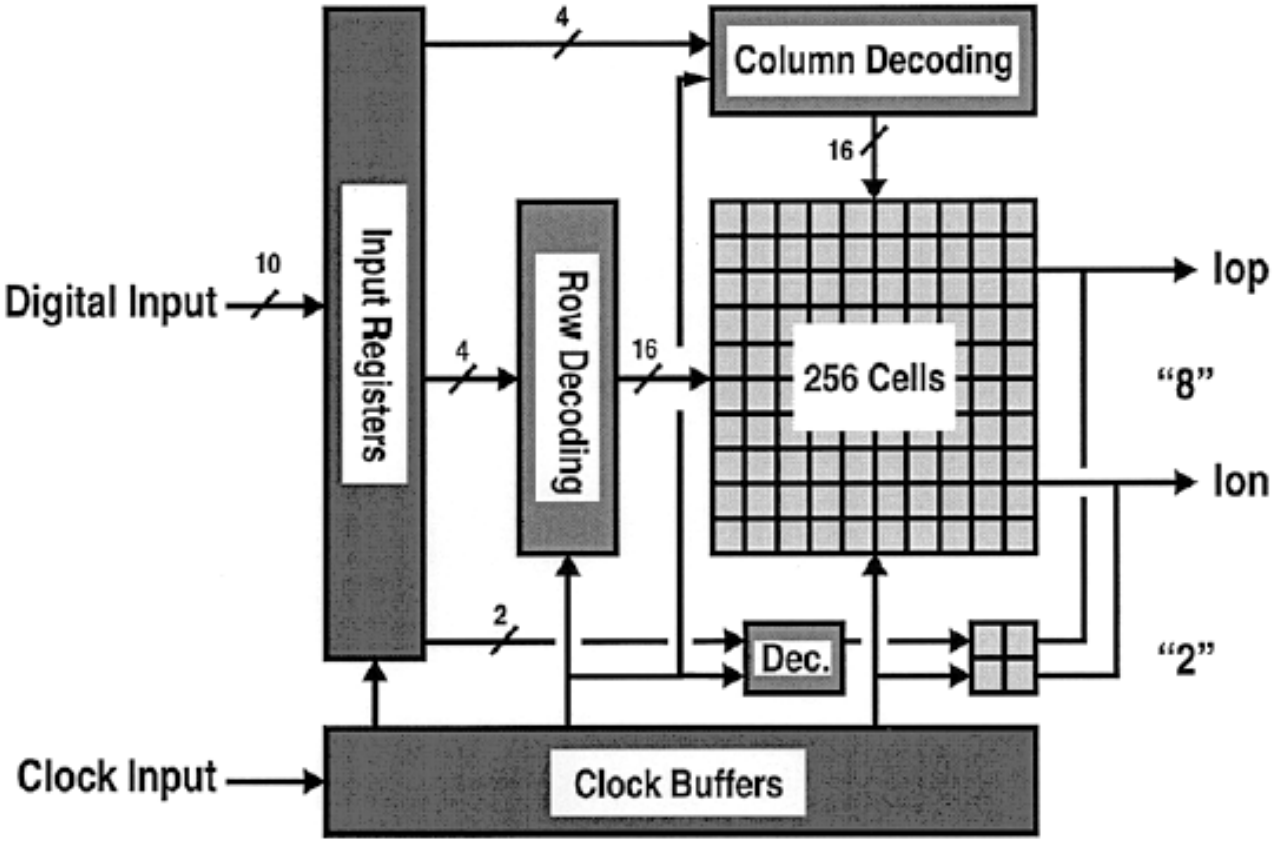
DAC Architecture	σ_{INL} (worst)	σ_{DNL} (worst)	Number of Switched Elements
Thermometer	0.32	0.01	4095
Binary Weighted	0.32	0.64	12
Segmented ($B_b=7$, $B_t=5$)	0.32	0.16	38

DAC INL/DNL Summary

- DAC choice of architecture has significant impact on DNL
- INL is independent of DAC architecture and requires element matching commensurate with overall DAC precision
- Results assume uncorrelated random element variations
- Systematic errors and correlations are usually also important and may affect final DAC performance

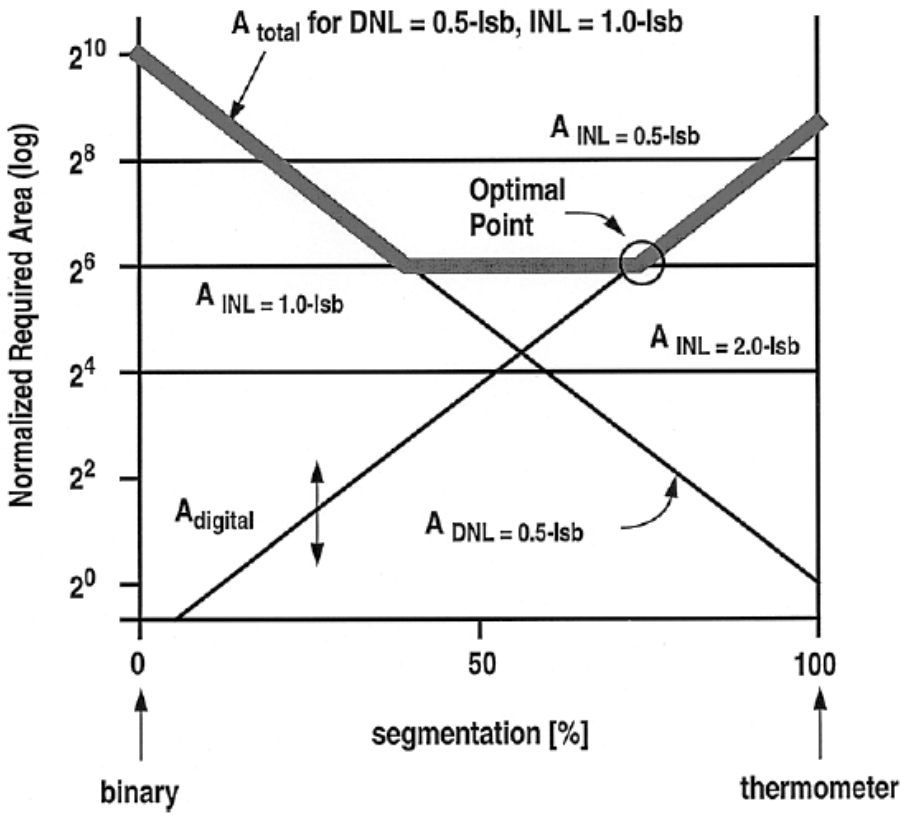
Ref: Kuboki, S.; Kato, K.; Miyakawa, N.; Matsubara, K. Nonlinearity analysis of resistor string A/D converters. IEEE Transactions on Circuits and Systems, vol.CAS-29, (no.6), June 1982. p.383-9.

10-bit Segmented DAC Example (8+2)



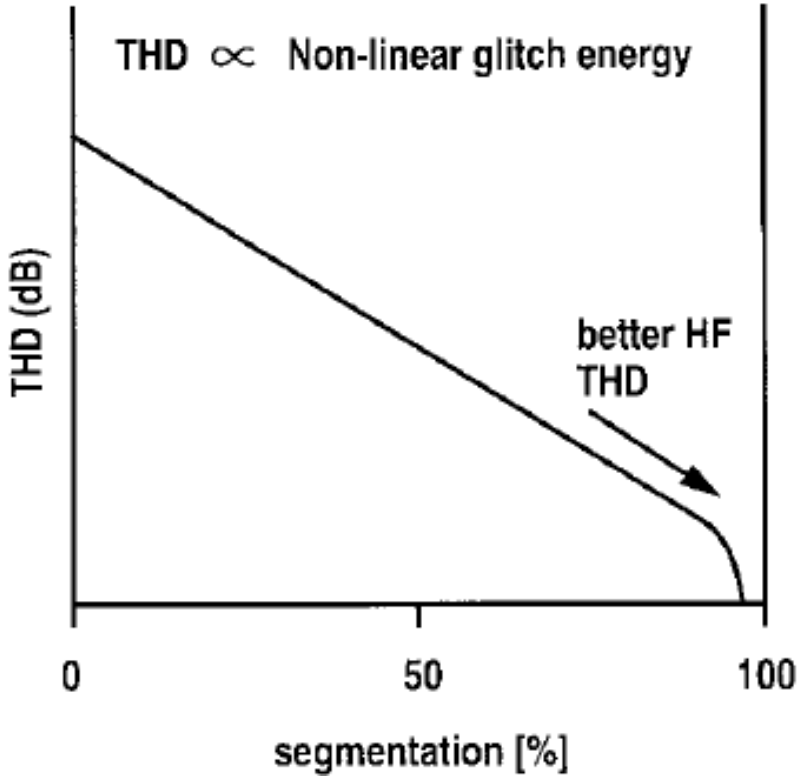
Ref: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

Area vs. Segmentation



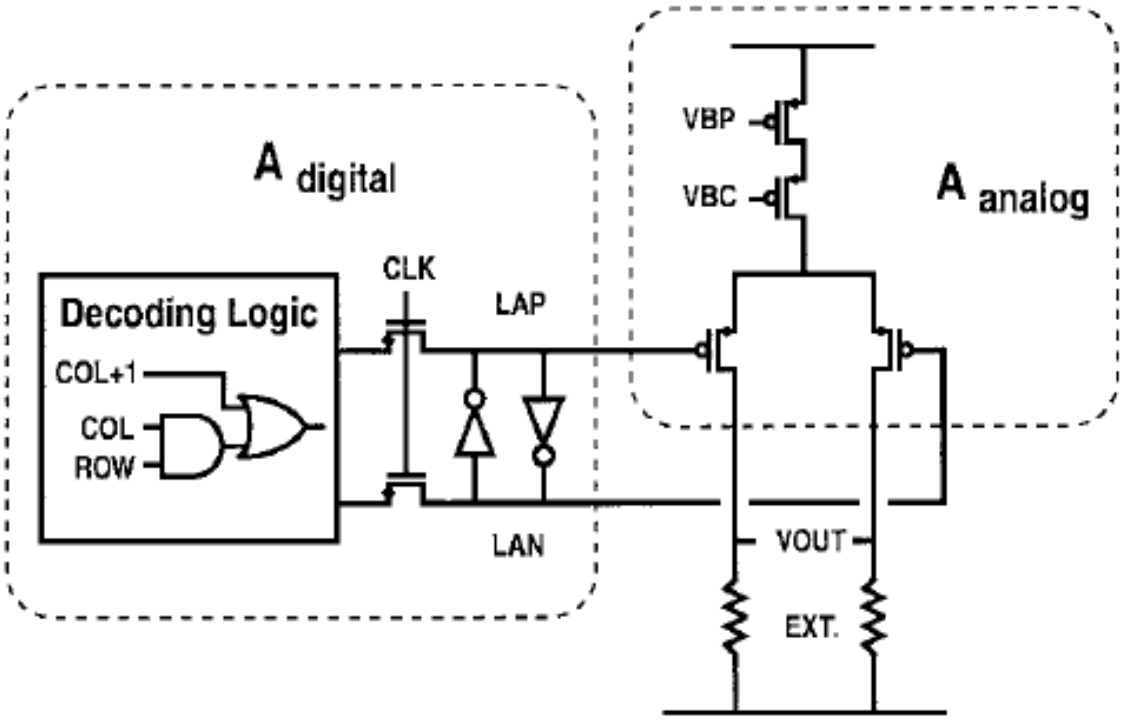
Ref: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

THD vs. Segmentation



Ref: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

Current Cell



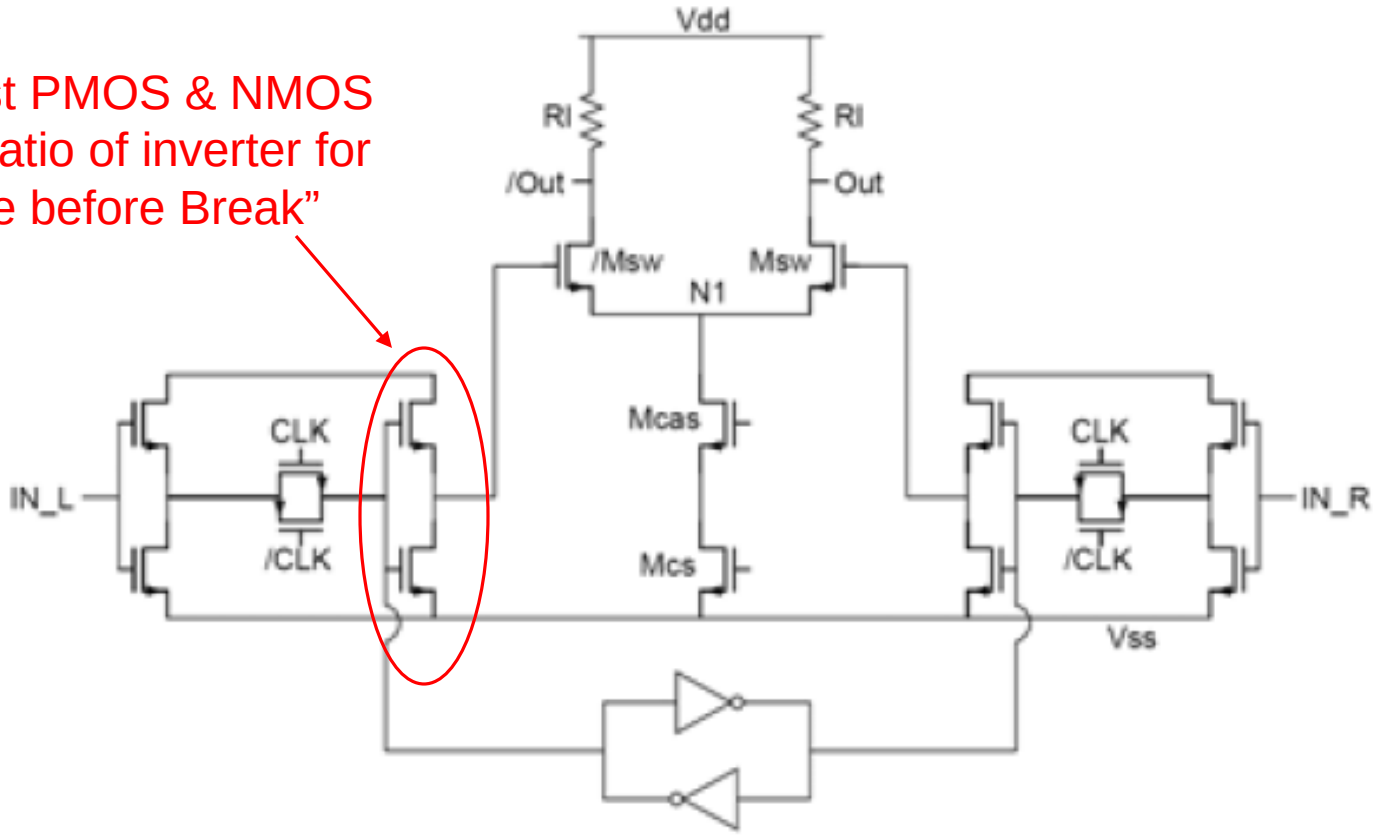
C.-H. Lin and K. Bult, “A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2,” *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

Commonly Used Techniques

- Retiming
  - Latches in (or close to) each current cell
  - Latch controlled by global clock to ensure that current cells switch simultaneously (independent of decoder delays)
- Make before break
  - Ensure uninterrupted current flow, so that tail current source remains active
- Low swing driver
  - Drive differential pair with low swing to minimize coupling from control signals to output
- Cascoded tail current source for high output impedance
  - Ensures that overall impedance at output nodes is code independent (necessary for good INL)

Switch Driver

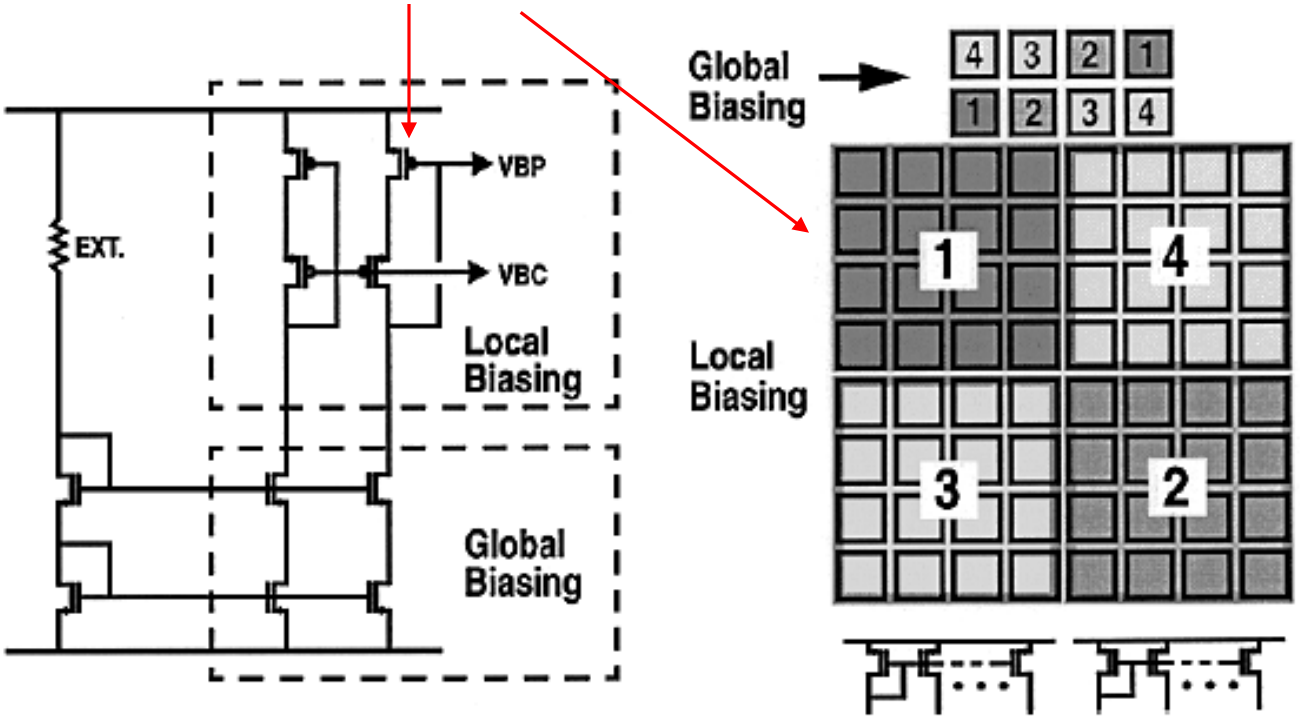
Adjust PMOS & NMOS size ratio of inverter for "Make before Break"



P. Palmers, Xu Wu, and M. Steyaert, "A 130 nm CMOS 6-bit full Nyquist 3GS/s DAC," IEEE Asian Solid-State Circuits Conference, ASSCC '07, pp.348-351, 12-14 Nov. 2007

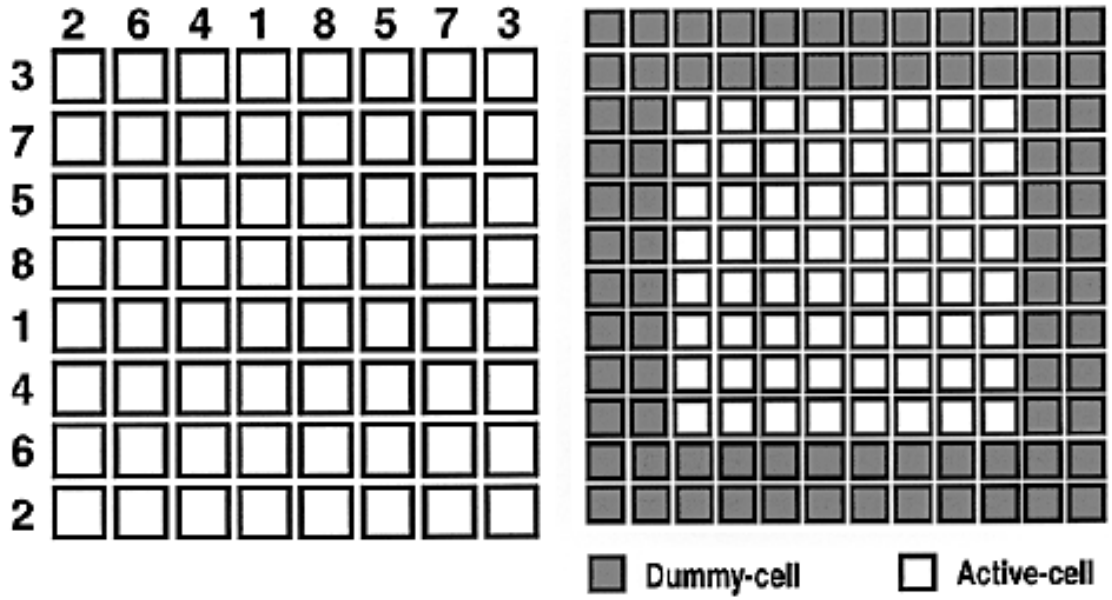
Biasing Scheme

M=4 for Main current source transistors
to place one transistor in each quadrant



Ref: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

Randomization and Dummies



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Homework #5

Designing 4-bit Binary Weighted and Segmented DACs