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[PROBLEM 1] Inverter Delay and Energy (30pts)

Assume the inverters are implemented in standard CMOS with symmetrical VTC. Furthermore, assume $C_{intrinsic} = C_{gate}(\gamma = 1)$. Equivalent resistance and input capacitance of unit-sized inverter are R and C, respectively. The intrinsic delay of unit-sized inverter is t_{inv}. Sizing factor $S \geq 1$.
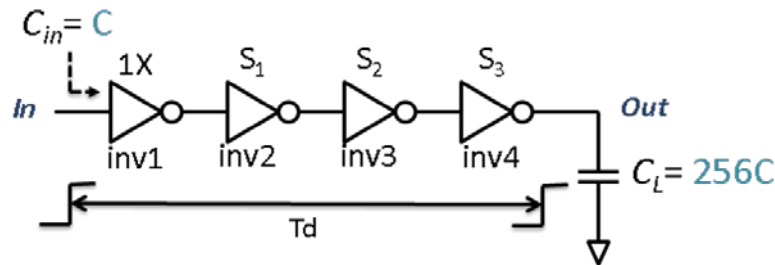

Fig. 1(a) Inverter Chain

(a) For inverters in Fig. 1(a), pick the best sizing factors, S_1, S_2 and S_3 to minimize propagation delay, T_d. What is the minimum delay (in units of t_{inv})? (5 pts)

Solution:

Overall effective fan-out: $F = \dfrac{C_L}{C_{in}} = 256$, (1pts)

$f = \sqrt[N]{F} = \sqrt[4]{256} = 4 ; \quad S_1 = f = 4, S_2 = f^2 = 16, S_3 = f^3 = 64$ (2 pts)

The minimum delay: $T_d = N t_{inv}(1 + \dfrac{\sqrt[N]{F}}{\gamma}) = 4 \times t_{inv} \times (1 + 4) = 20 t_{inv}$ (2 pts)

(b) Assume all inverters share the same supply V_{DD}. What is the total energy drawn from the supply when the input switches from 0 to V_{DD}? What is the total energy dissipated as heat by the circuit? (Answer in symbolic terms: C, V_{DD}) (5 pts)

Solution:

The total switched capacitance during $0 \rightarrow V_{DD}$ at the input is:

$$C_{sw} = C_{int\,rinsic,inv2} + C_{gate,inv3} + C_{int\,rinsic,inv4} + C_L = 4C + 16C + 64C + 256C = 340C$$

The total energy drawn from the supply is: $E_{VDD} = 340CV_{DD}^2$; (2 pts)

The total energy dissipated as heat is:

$$E_{heat} = 0.5(C_{total}) \cdot V_{DD}^2$$
$$\Rightarrow E_{heat} = 0.5(C + 4C + 4C + 16C + 16C + 64C + 64C + 256C) \cdot V_{DD}^2 = 212.5CV_{DD}^2$$
(3 pts)

(c) For inverters in Fig. 1(a), pick the best sizing S_1, S_2 and S_3 to minimize energy consumption. What is the total energy consumed for a full cycle (0→ V_{DD}, V_{DD}→ 0)? (10 pts)

Solution:

To minimize the energy: $S_{min} = 1, S_1 = S_2 = S_3 = 1$ (5 pts)

The total capacitance charged during a full cycle (0→ V_{DD}, V_{DD}→ 0) is:
$$S_{min} = 1, S_1 = S_2 = S_3 = 1,$$
$$C_{total} = C + C + C + C + C + C + C + 256C = 263C \text{ (5 pts)}$$
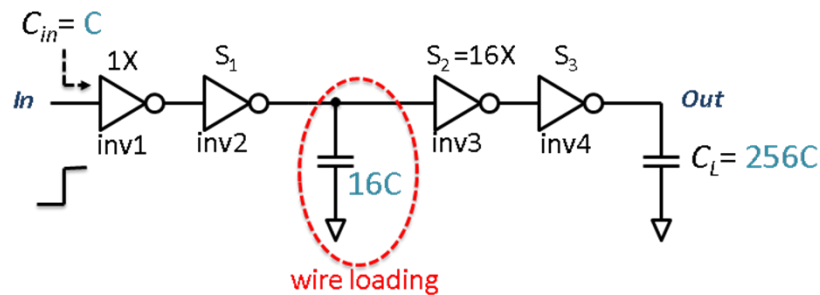$$E_{total} = 263CV_{DD}^2$$

Fig. 1(b) Inverter Chain with Wire Loading

(d) In Fig. 1(b), we take the capacitive loading of the metal wire between inv2 and inv3 into consideration. This wire loading is modeled as a capacitor which is equal to 16C as shown in Fig. 1(b). Assume the sizing factor S_2 is 16X and you can only choose the sizing factor S_1 and S_3. What are the optimal values of S_1 and S_3 for minimum delay? What is the delay (in units of t_{inv})? (10 pts)

Solution:

To find the optimal sizing factors for minimum delay, we start from the delay expression.

$$T_d = t_{inv}\left[(1+S_1)+(1+32/S_1)+(1+S_3/16)+(1+256/S_3)\right]$$ (5 pts)

Taking partial derivative with respect to S₁ and S₃, we get:

$$1-\frac{32}{S_1^2}=0 \quad \Rightarrow S_1 = 4\sqrt{2}$$

$$\frac{1}{16}-\frac{256}{S_3^2}=0 \quad \Rightarrow S_3 = 64$$

Finally, the delay is:

$$T_d = t_{inv}\left[(1+S_1)+(1+32/S_1)+(1+S_3/16)+(1+256/S_3)\right]=(12+8\sqrt{2})t_{inv}=23.31\cdot t_{inv}$$
(5 pts)

[PROBLEM 2] Logical Effort (30 pts)
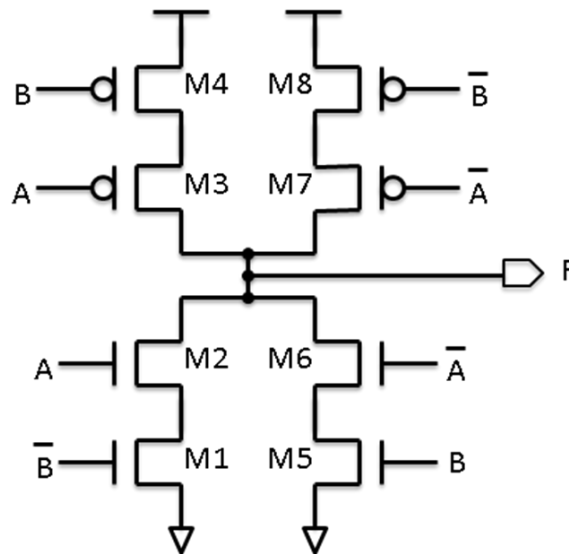
Given the complex gate below:

Fig. 2 Complex Gate

(a) Draw the truth table and determine the logic function of the complex gate shown in Fig. 2. (10 pts)
Solution:

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

This is an XNOR gate. (10 pts)

(b) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio is 2/1). What is logical effort of this gate for each input ($A, \overline{A}, B, \overline{B}$)? (10 pts)

Solution:
M1=M2=M5=M6=2 (1 pts)

M3=M4=M7=M8=4 (1 pts)

$LE_A = (2+4)/3 = 2$ (2 pts)

$LE_B = (2+4)/3 = 2$ (2 pts)

$LE_{\overline{A}} = (2+4)/3 = 2$ (2 pts)

$LE_{\overline{B}} = (2+4)/3 = 2$ (2 pts)

(c) Suppose we are only interested in the delay of the falling output transition when input A is pulled high and input B is pulled low. Size the transistor M1 and M2 to make the logical effort of this gate for the input A the same as a unit inverter. For transistors M3-M8, use the sizes you found in (b). (10 pts)

Solution:

$$LE_A = \left(\frac{\left(\frac{2}{M2} \right) \times (4+M2)}{1 \times 3} \right) = 1 \quad \text{(5 pts)}$$

$\Rightarrow M2 = 8$ (3 pts)

$M2 = M1 = 8$ (2 pts)

[PROBLEM 3] Logical Effort and Sizing (40 pts)

Considering the logic network of Fig. 3, this represents the critical path of a complex logic block. Assume that C_G = 2fF/μm and C_D/C_G = γ = 0.5. All the transistors are long channel for the purpose of calculating logical effort.
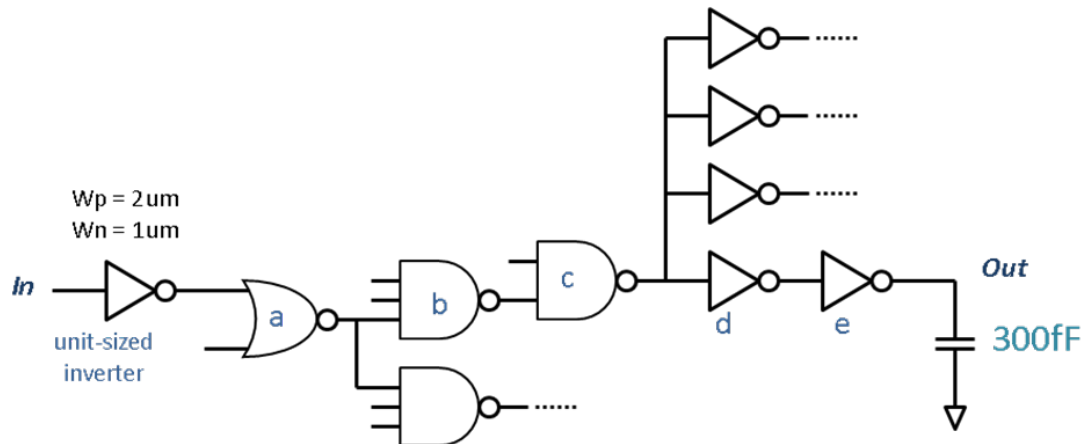

Fig. 3 Critical Path of Combinational Logic

(a) What is the total path effort from **In** to **Out**? (10 pts)

Solution:

$$\prod LE = 1 \times (\frac{5}{3}) \times (\frac{5}{3}) \times (\frac{4}{3}) \times 1 \times 1 = \frac{100}{27}$$

$$B = \prod b_i = 1 \times 2 \times 1 \times 4 \times 1 \times 1 = 8 \qquad \text{(2 pts for each equation)}$$

$$F = \frac{C_L}{C_{in}} = \frac{300\,fF}{(\frac{2\,fF}{um})(2um + 1um)} = 50$$

Path Effort: $PE = (\prod LE)(B)F = \frac{100}{27} \times 8 \times 50 = \frac{40000}{27} = 1481.48$ (4 pts)

(b) To minimize the delay, what should the effective fan-out per stage for this chain of gates be? (10 pts)

Solution:

Effective Fan-out: $EF = \sqrt[N]{PE} = \sqrt[6]{1481.48} = 3.38$ (10 pts)

(c) Size the gates in this chain to minimize the delay from **In** to **Out**. (Only calculate the input capacitance of the gates; don't bother to provide the actual transistor sizes.) (10 pts)

Since $EF = (f_x)(b_x)(LE_x) = 3.38$ for each stage and $f_x = \dfrac{C_{out,x}}{C_{in,x}}$

We can calculate the input capacitance of each stage as follows:

$$C_{in,e} = C_{out,e}\frac{(b_e)(LE_e)}{EF} = 300\frac{1\times 1}{3.38} = 88.76$$

$$C_{in,d} = C_{out,d}\frac{(b_d)(LE_d)}{EF} = 88.76\frac{1\times 1}{3.38} = 26.26$$

$$C_{in,c} = C_{out,c}\frac{(b_c)(LE_c)}{EF} = 26.26\frac{4\times\dfrac{4}{3}}{3.38} = 41.44$$

(2 pts for each stage)

$$C_{in,b} = C_{out,b}\frac{(b_b)(LE_b)}{EF} = 41.44\frac{1\times\dfrac{5}{3}}{3.38} = 20.43$$

$$C_{in,a} = C_{out,a}\frac{(b_a)(LE_a)}{EF} = 20.43\frac{2\times\dfrac{5}{3}}{3.38} = 20.15$$

(d) Using this sizing, what is the delay (in units of t_{inv}) of your chain from **In** rising to **Out** rising? You can assume that the critical input of the complex gates is always at the "top" of the transistor stacks (i.e., the critical input is always closest to the output node). (10 pts)

We set the EF of each stage as 3.38 for minimizing the delay, so the delay

$$D = t_{inv}(\sum_{i=1}^{N}(P_i + LE_i f_i b_i)) = t_{inv}\left((\sum_{i=1}^{N}P_i) + N\times EF\right)$$
$$= t_{inv}\left(\gamma(1+2+3+2+1+1) + 6\times 3.38\right) = 25.28\cdot t_{inv} \quad \text{(10 pts)}$$