Texas A&M University
Electrical Engineering Department

ECEN 665

Laboratory #7: PLL Based Frequency Synthesizer

Objectives: To learn the fundamental operation of a frequency synthesizer based on a charge-pump PLL. To design a charge-pump PLL at the system level and observe its functioning using a SystemView model.

1. Charge Pump PLL design

Figure 1 depicts a block diagram of the PLL to be designed.

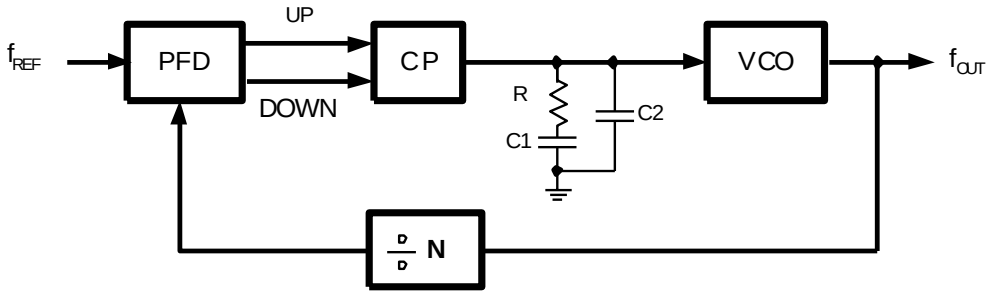


Figure 1. Block diagram of a charge-pump based PLL

The main specifications are derived from the ZigBee standard and are summarized in Table 1.

Table 1. Summary of PLL Specifications

Frequency Band	2400 MHz – 2483.5 MHz
Channels	16
Channel Spacing	5 MHz
Channel frequencies	2405MHz + 5n , n = [0, 15]
Settling time	< 192us
Settling Accuracy	± 40 ppm (96 KHz)

a. Assume a VCO with a free running frequency of 2.4GHz. The control voltage of the VCO varies between 0.5V – 1V. Pick a VCO gain (Hz / V) to cover the required channels (with a margin for process variations!). Discuss the affects of VCO gain in the loop dynamics and the impacts of your choice of VCO gain.

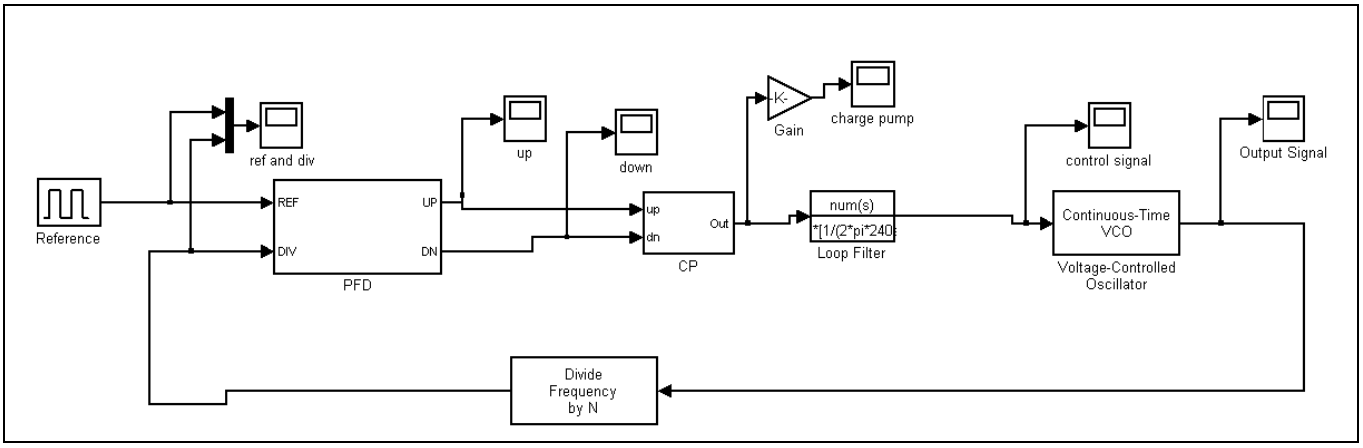
b. Choose an appropriate reference frequency and determine the set of division ratios to generate the required channel frequencies.

c. Find the loop parameters (bandwidth, damping ratio, natural frequency, settling time, location of poles and zero) to comply with the PLL specifications. You can use the procedure given in class notes or follow other procedures from PLL literature, a detailed approach is given in [2] or in summary in [3]. Discuss the impact of these loop parameters on PLL performance. Plot the open loop transfer function and the phase step response.

d. Calculate the values for the components of the loop filter and the charge pump current. What is the impact of charge pump current on the PLL performance? Discuss the size of loop filter components you calculated, considering layout and integration concerns.

e. Implement the PLL you designed in Simulink as shown below. Note that you need to implement the Charge Pump and PFD yourself since they are not available in Simulink. The frequency divider model will be provided to you by the TA.

You can use the subsystem feature of Simulink to make your schematic organized as below. Show your overall diagram as well as the internal scheme of any subsystem you use. Also show the waveforms and discuss the control line of the VCO and the lock behavior. What is the value control voltage settles to for the 16th channel?



Hint: You can implement the PFD as a sequential implementation based on edge triggered D-flip flops. To emulate a realistic approach you can also use the "transport delay" block in Simulink to emulate the delay line before the reset of the flip-flops.

Notes

The due date for this report is the beginning of next week's lab session.

References

[1] IEEE 802.15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/reading/ieee/std/lanman/restricted/802.15.4-2003.pdf

[2] Keliu Shu, Edgar Sanchez-Sinencio, " CMOS PLL Synthesizers, Analysis and Design", Springer, 2005

[3] Sung T. Moon, Ari Y. Valero-Lopez, Edgar Sanchez-Sinencio, "Fully integrated frequency synthesizers: A tutorial", International Journal of High Speed Electronics and System, Vol. 15, No. 2, 2005.