

EE141-Spring 2010 Digital Integrated Circuits

Instructor: Jan Rabaey

WeFr 2:00-3:30pm
127 Dwinelle

What is this class all about?

- ❑ **Introduction to digital integrated circuit design engineering**
 - Key concepts needed to be a good digital IC designer
 - Design creativity
- ❑ **Models that allow reasoning about circuit behavior**
 - Allow analysis and optimization of the circuit's performance, power, cost, etc.
 - Understanding circuit behavior is key to making sure it will actually work
- ❑ **Teach you how to make sure your circuit works**
 - Do you want your transistor to be the one that screws up a 1 billion transistor chip?

What will you learn?

- ❑ Understanding, designing, and optimizing digital circuits for various quality metrics:
 - Performance (speed)
 - Power dissipation
 - Cost
 - Reliability

Detailed Topics

- ❑ CMOS devices and manufacturing technology
- ❑ CMOS gates
- ❑ Combinational and sequential circuits
- ❑ Arithmetic building blocks
- ❑ Interconnect
- ❑ Memories
- ❑ Propagation delay, noise margins, power
- ❑ Timing and clocking
- ❑ Design methodologies

Practical Information

Instructor

- Prof. Jan Rabaey



563 Cory Hall, 643-3986, jan@eecs
Office hours: We 4:00pm-5:30pm

TAs:

- Stanley (Yuan-Shih) Chen, yschen@eecs (OH: Th. 12-1pm)
- Nam-Seog Kim, namseog@eecs (OH: Th. 5-6pm)

Reader:

- TBD

Web page:

http://bwrc.eecs.berkeley.edu/Classes/IcDesign/ee141_s10/

Discussions and Labs

Discussion sessions

- *Th 11am-noon, Stanley* (TBD) (proposed change)
- Th 4-5pm, Namseog (521 Cory)
- Same material in both sessions!

Labs (353 Cory)

- Mo 1-4pm (Stanley)
- Tu 2-5pm (Namseog)
- We 11am-2pm (Stanley/Namseog)

Please choose one lab session and stick with it!

Your EECS141 Week

| | 9 | 10 | 11 | 12 | 1 | 2 | 3 | 4 | 5 | 6 |
|----|---|----|--|---------------|---|------------------------------|---|--------------------|---------------|---|
| Mo | | | | | | Lab 1 (353 Cory) Stanley | | | | |
| Tu | | | | | | Lab 2 (353 Cory) Nam-Seog | | | TA mtng | |
| We | | | Lab 3 (353 Cory) Stanley & Nam-Seog | | | Lecture 127 Dwinelle | | OH Prof. Rabaey | | |
| Th | | | DIS2 Stanley | OH Stanley | | | | DIS1 NamSeog | OH NamSeog | |
| Fr | | | | | | Lecture 127 Dwinelle | | | | |

Assignment due

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Class Organization

- ❑ 9-10 assignments
 - ❑ One design project (with multiple phases)
 - ❑ Labs: 5 software
 - ❑ 2 midterms, 1 final
 - Midterm 1: Fr Febr 19 (**TBD**)
 - Midterm 2: We April 7 (**TBD**)
 - Final: Tu May 11, 11:39am-2:30pm (**TBD**)

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Some Important Announcements

- ❑ Please use the newsgroup for asking questions
(<news://news.csua.berkeley.edu/ucb.class.ee141>)
- ❑ Can work together on homework
 - But you must turn in your own solution
- ❑ Lab reports due 1 week after the lab session
- ❑ Project is done in pairs
- ❑ No late assignments
 - Solutions available shortly after due date/time
- ❑ Don't even think about cheating!

Grading Policy

- ❑ Homeworks: 10%
- ❑ Labs: 10%
- ❑ Projects: 20%
- ❑ Midterms: 30%
- ❑ Final: 30%

Class Material

- ❑ Textbook: “Digital Integrated Circuits – A Design Perspective”, 2nd ed, by J. Rabaey, A. Chandrakasan, B. Nikolic
- ❑ Class notes: Web page
- ❑ Lab Reader: Web page
- ❑ Check web page for the availability of tools

The Web Site

- ❑ The sole source of information

http://bwrc.eecs.berkeley.edu/icdesign/eecs141_s10

(Also via department web-site)

- Class and lecture notes
- Assignments and solutions
- Lab and project information
- Exams
- Many other goodies ...



Print only what you need: Save a tree!

Course Webcast



- ❑ All lectures streamed live
- ❑ Also available in archive
- ❑ Check: <http://webcast.berkeley.edu/courses.php>
- ❑ However: Live experience has advantages



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Software

- ❑ Cadence
 - Widely used in industry
 - Online tutorials and documentation
- ❑ HSPICE and Spectre for simulation

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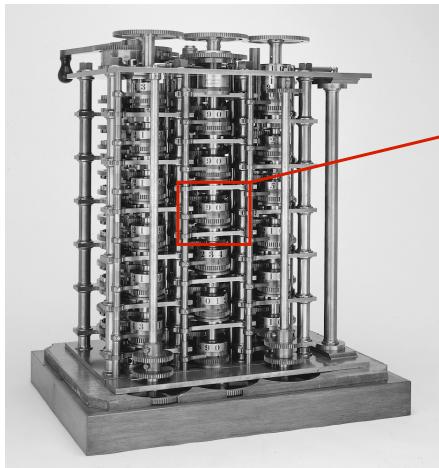
Getting Started

- ❑ Assignment 1: Getting SPICE to work – see web-page
- ❑ Due next Friday, January 29, 5pm
- ❑ NO discussion sessions or labs this week.
- ❑ First discussion sessions in Week 2
- ❑ First software lab in Week 3

Introduction

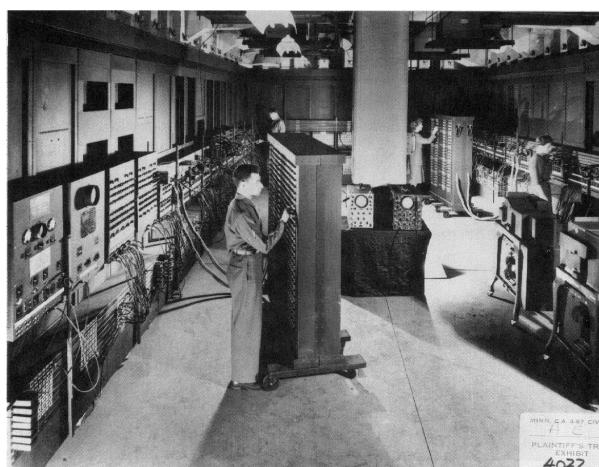
- ❑ Digital Integrated Circuit Design: The Past, The Present and The Future
 - What made Digital IC design what it is today
 - Why is designing digital ICs different today than it was before?
 - Will it change in the future?

The First Computer

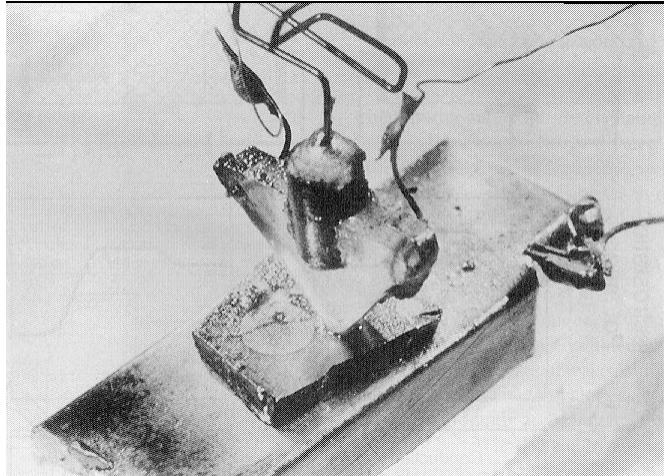


- The Babbage Difference Engine
 - 25,000 parts
 - cost: £17,470

ENIAC - The First Electronic Computer (1946)



The Transistor Revolution



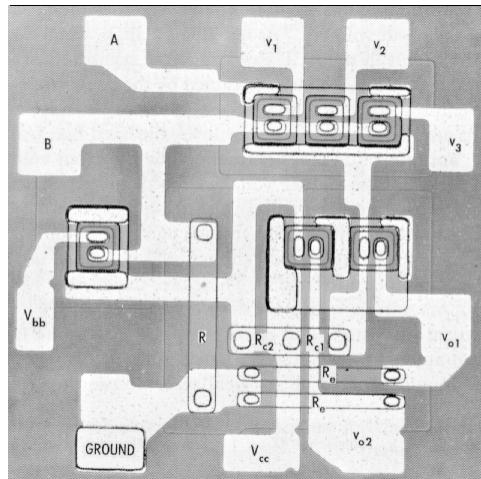
First transistor
Bell Labs, 1948

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The First Integrated Circuits



Bipolar logic
1960's

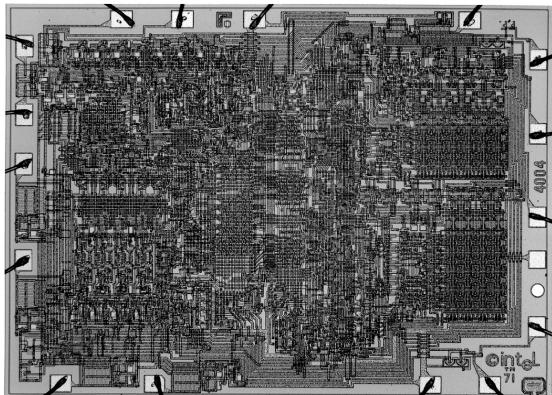
ECL 3-input Gate
Motorola 1966

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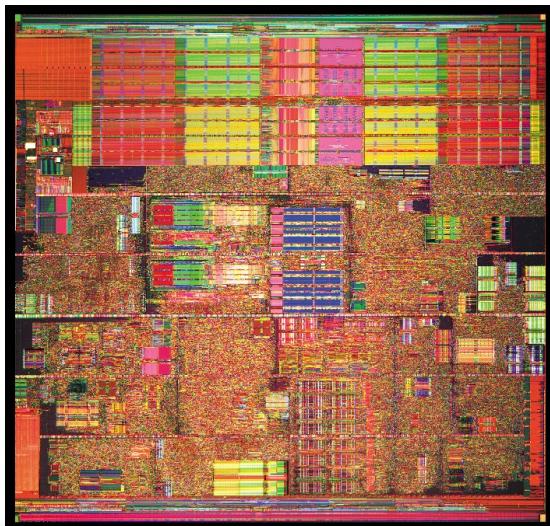
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Intel 4004 Microprocessor



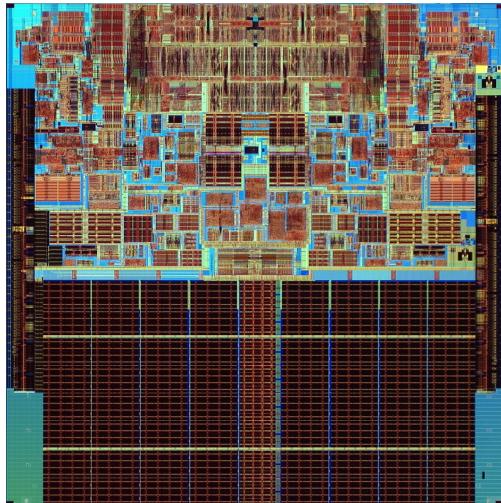
Intel, 1971.
2,300 transistors (12mm^2)
740 KHz operation
($10\mu\text{m}$ PMOS technology)

Intel Pentium 4 Microprocessor



Intel, 2005.
125,000,000 transistors
(112mm^2)
3.8 GHz operation
(90nm CMOS technology)

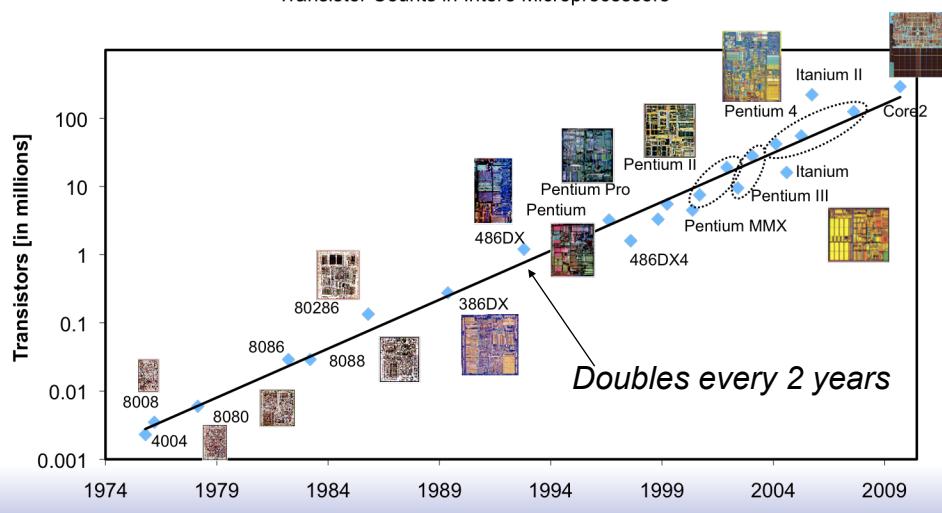
Intel Core 2 Microprocessor



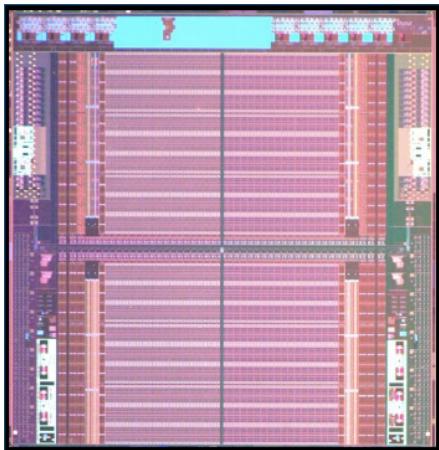
Intel, 2006.
291,000,000 transistors
(143mm²)
3 GHz operation
(65nm CMOS technology)

Transistor Counts

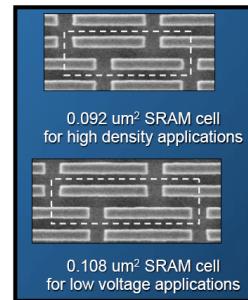
Transistor Counts in Intel's Microprocessors



Intel SRAM Prototype Chip (2009)



- ❑ 22 nm
- ❑ 364 Mbyte SRAM
- ❑ > 2.9 Billion Transistors
- ❑ 3rd generation high-k + metal gate



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Moore's Law

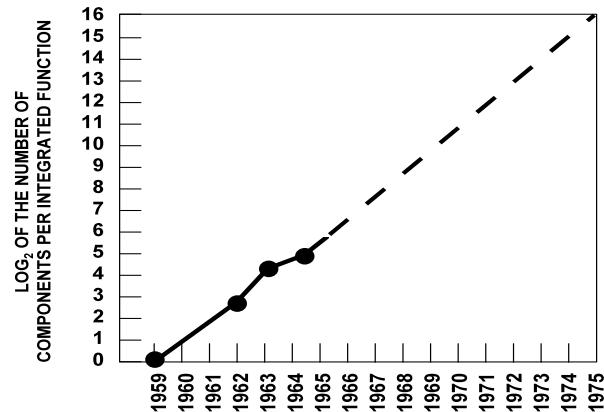
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

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Moore's Law



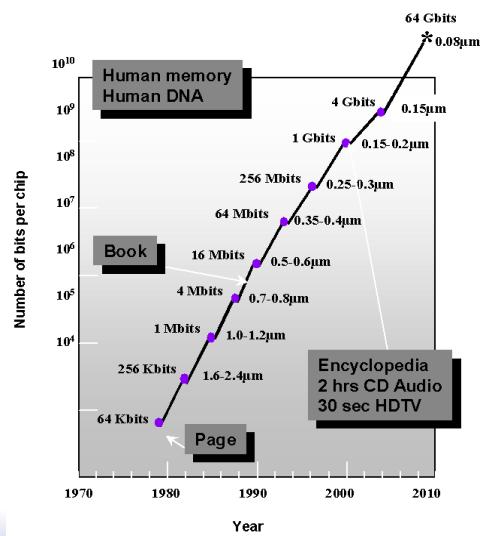
Electronics, April 19, 1965.

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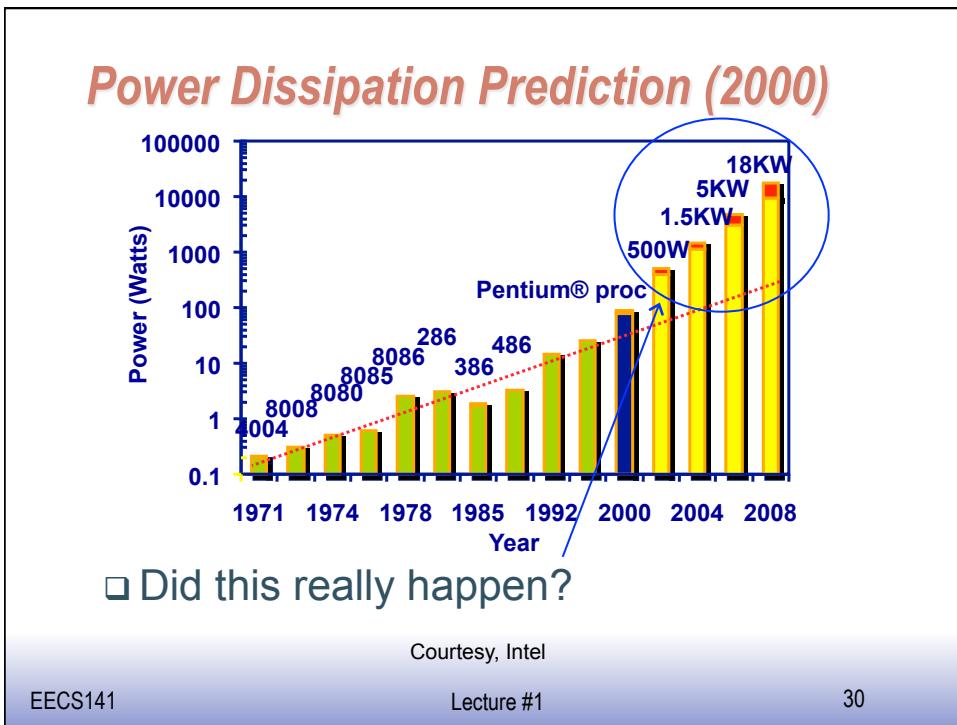
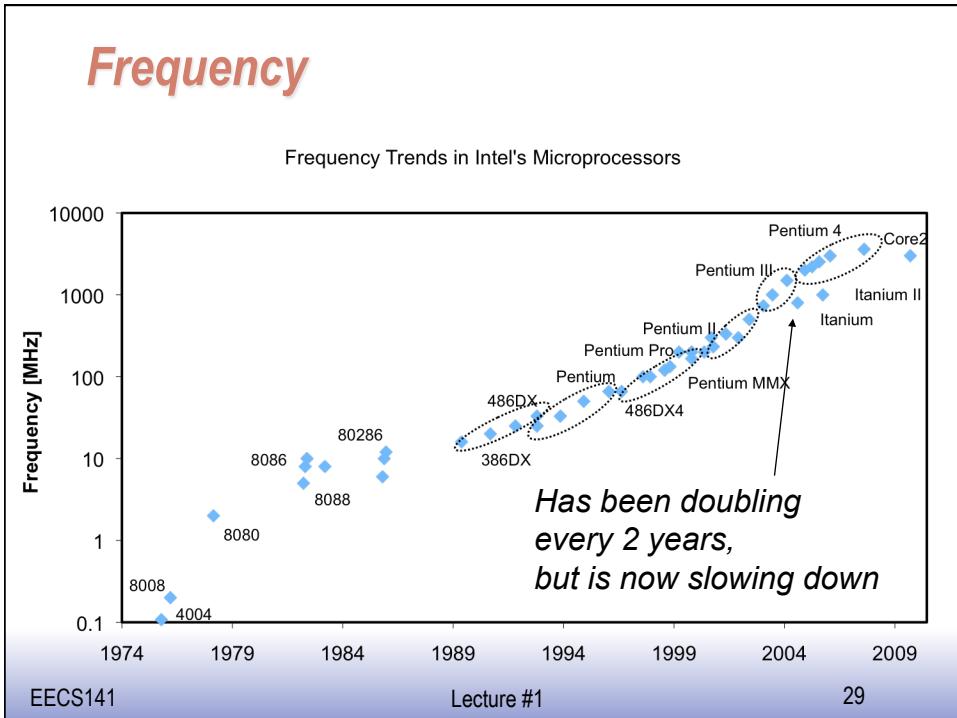
Evolution in Complexity

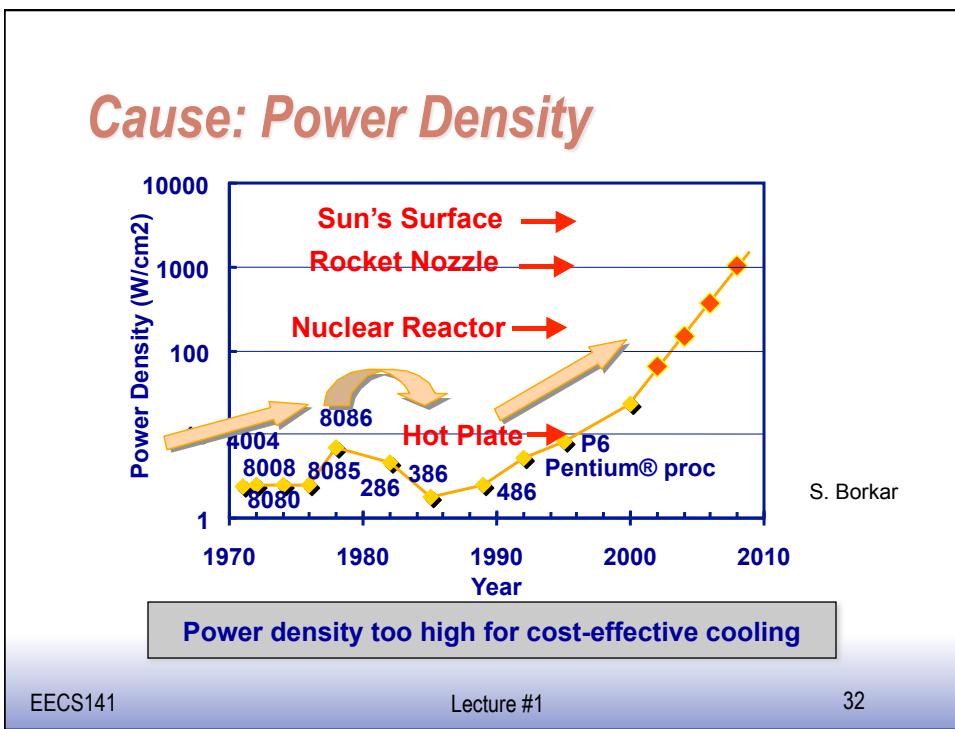
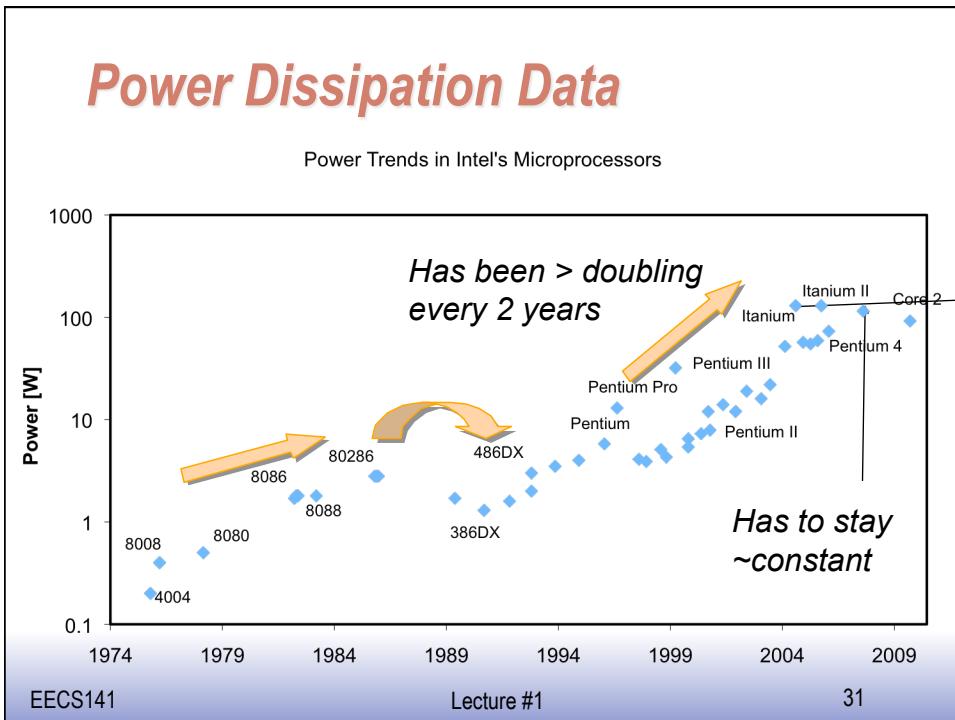


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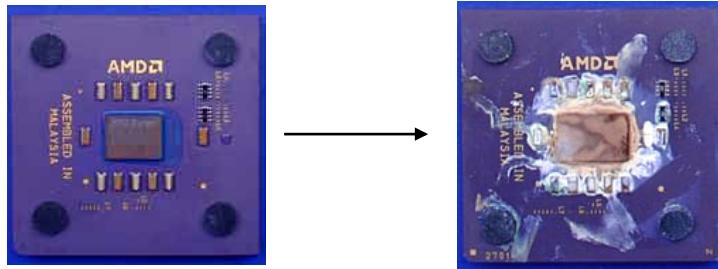
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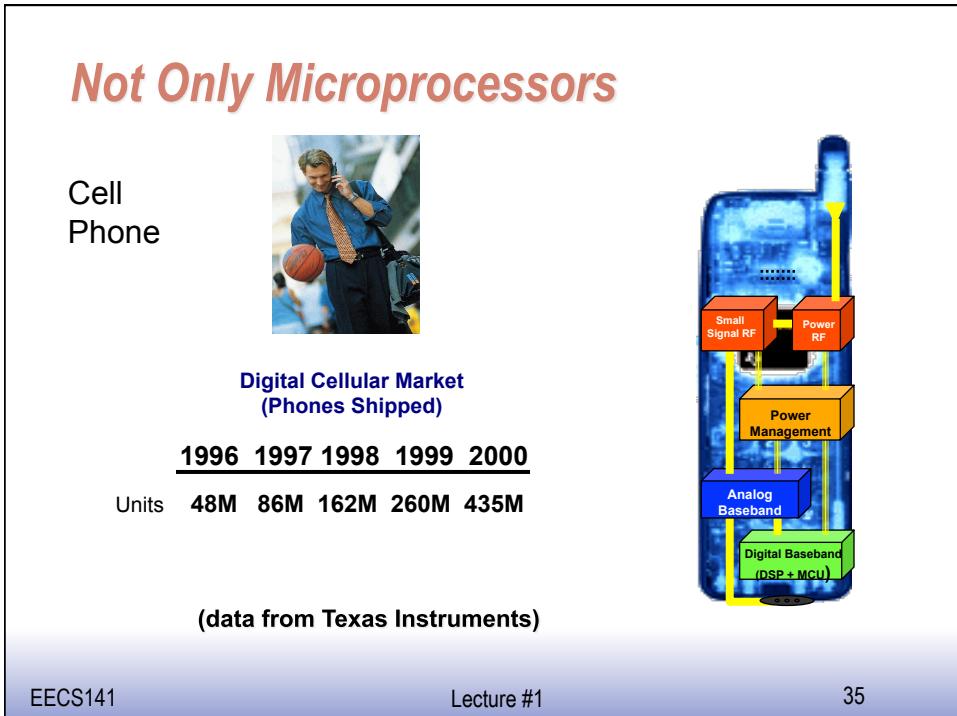
Not enough cooling...



*Pictures from http://www.tomshardware.com/2001/09/17/hot_spot/

Why Scaling?

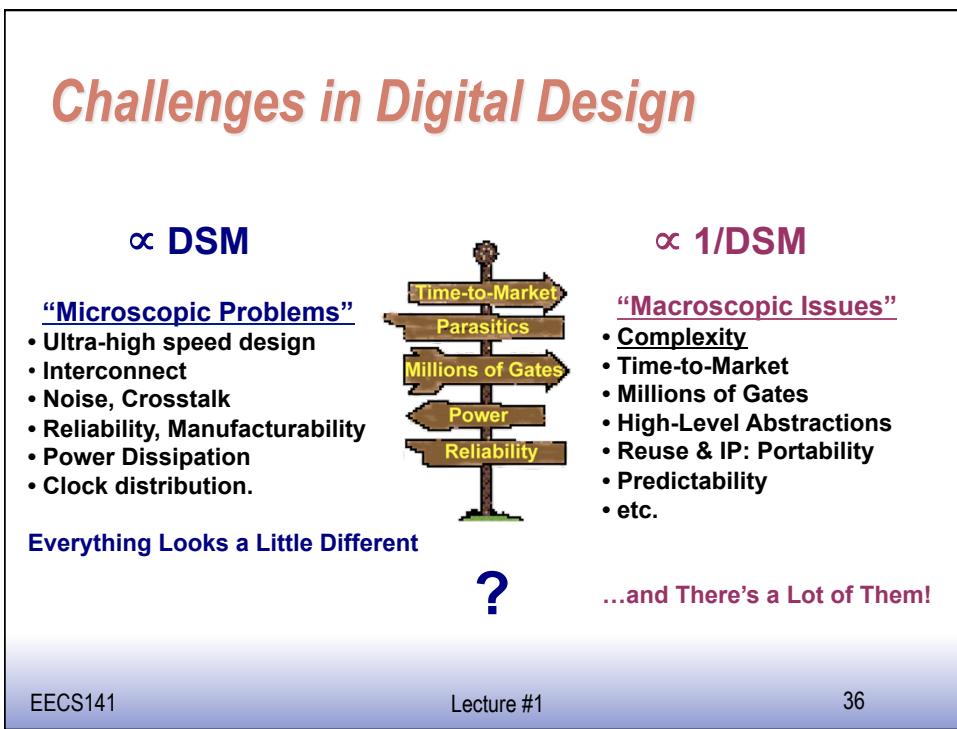
- ❑ Technology shrinks by 0.7/generation
- ❑ With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- ❑ Cost of a function decreases by 2x
- ❑ But ...
 - How to design chips with more and more functions?
 - Design engineering population does not double every two years...
- ❑ Hence, a need for more efficient design methods
 - Exploit different levels of abstraction



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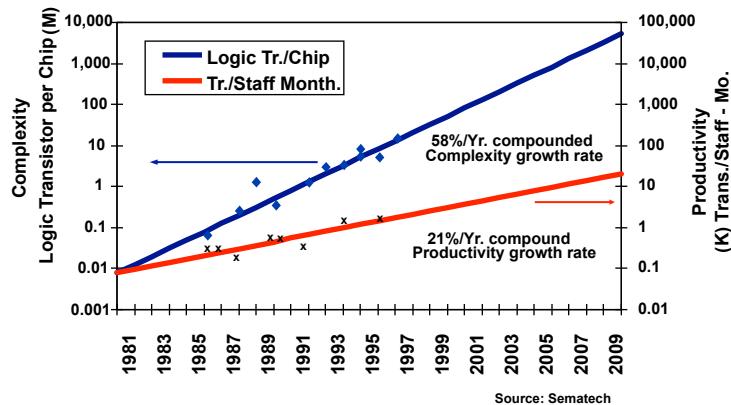


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Productivity Trends



Complexity outpaces design productivity

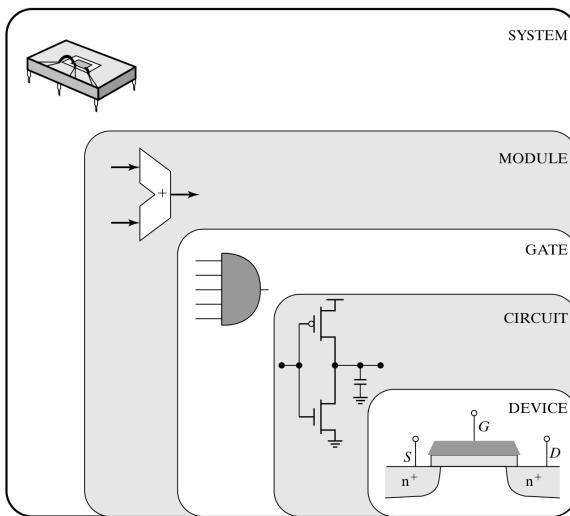
Courtesy, ITRS Roadmap

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Design Abstraction Levels



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Next Lecture

- ❑ Introduce basic metrics for design of integrated circuits – how to measure cost, delay, power, etc.