EE230-02 RFIC II
Fall 2018

Lecture 23: Final Review

Prof. Sang-Soo Lee
sang-soo.lee@sjsu.edu
ENG-259

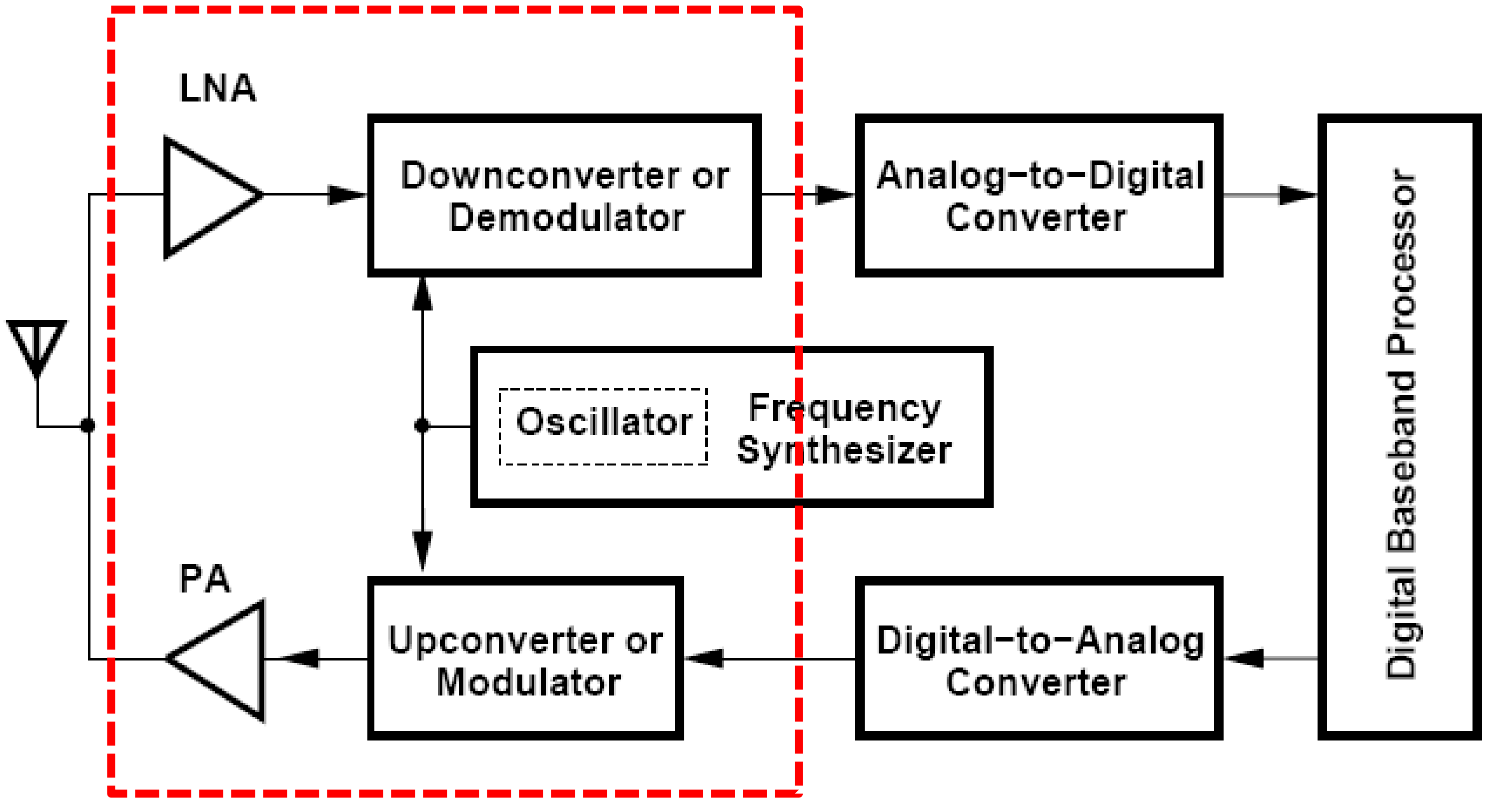
Final Exam

- Dec. 14, Friday 2:45 PM – 4:45 PM
- One-page Aid sheet on Front side only allowed
- Bring a Calculator

Exam Topics

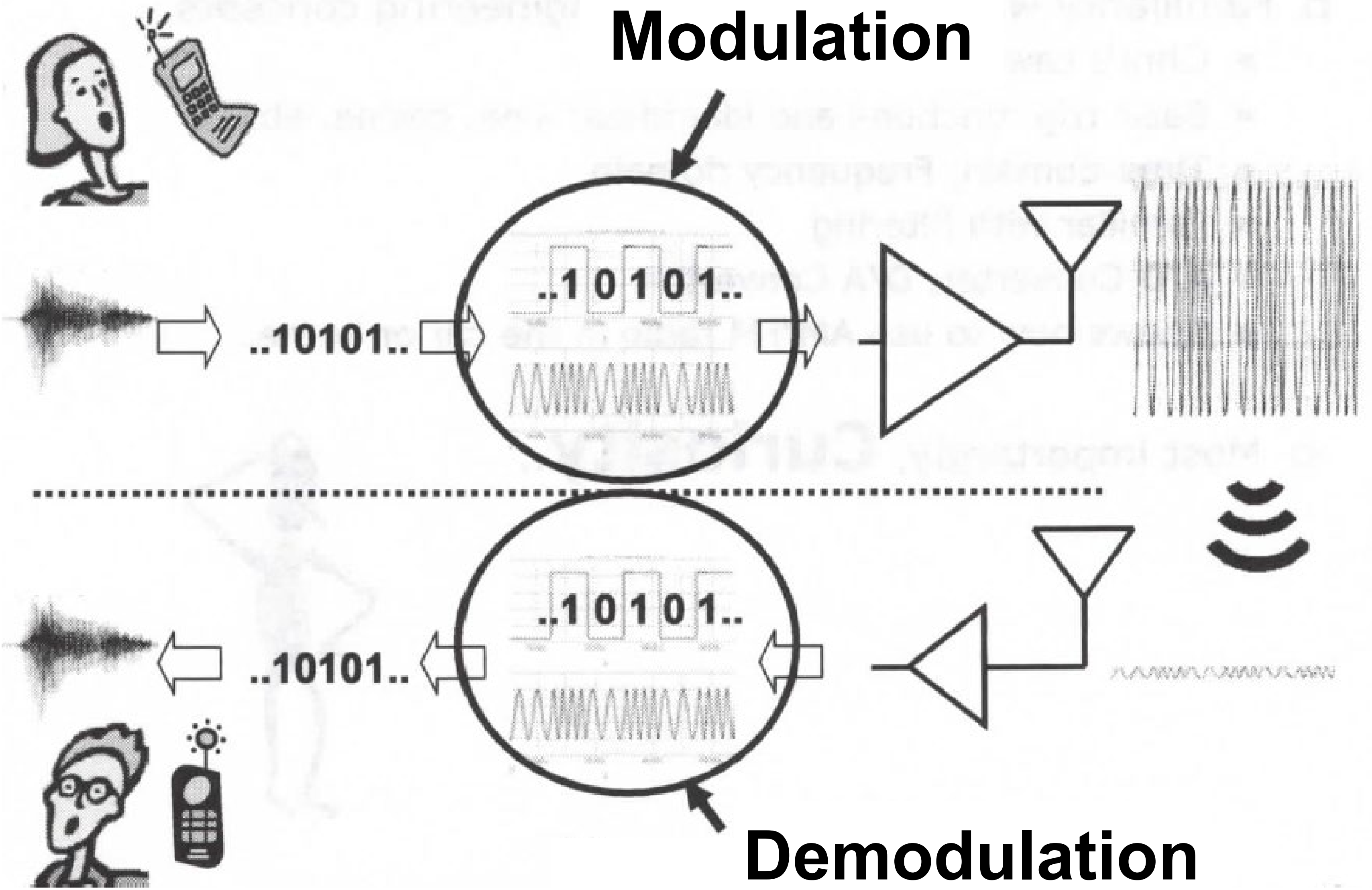
1. RF Basics
2. Matching Network
3. LNA & Noise Factor of the circuit
4. VCO
5. PLL
6. Misc. Questions

Blocks Covered in the Class



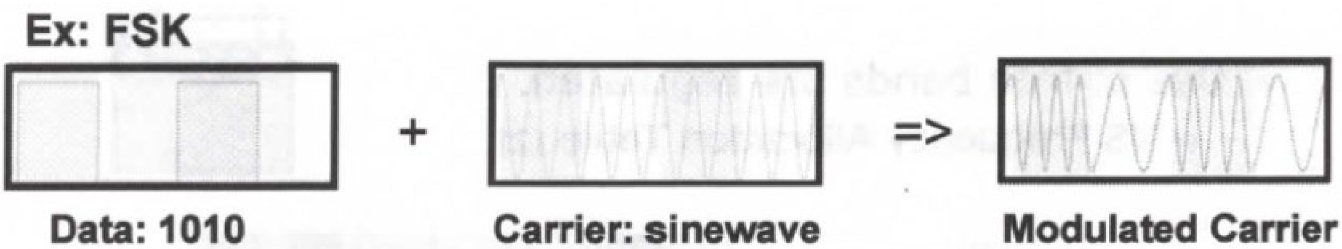
- **Signals are upconverted/downconverted at TX/RX, by an oscillator controlled by a Frequency Synthesizer**

How to send data without wire?

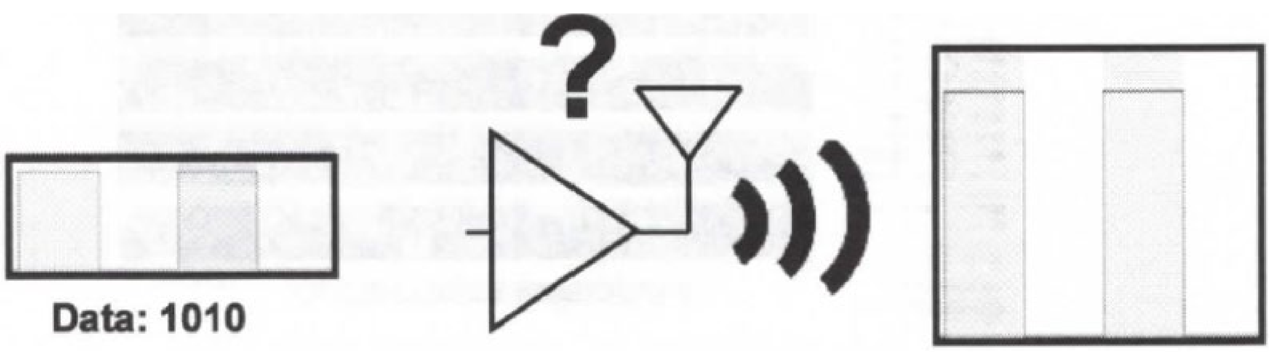


Modulation

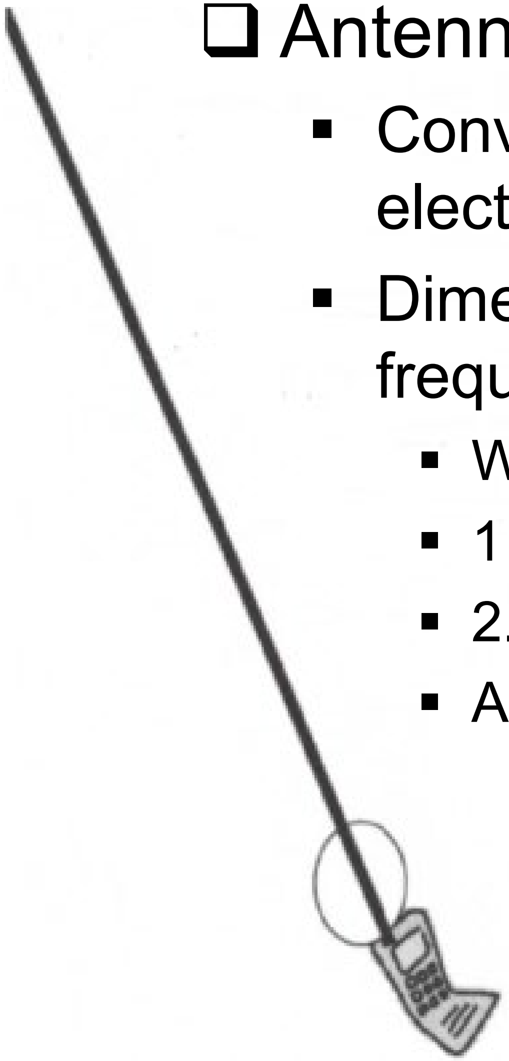
- Process of adding information (or signal) to a carrier signal, typically a sinewave.



- Why do we need to modulate? Why not just send the data as is?



Why Modulation?



- Antenna
  - Converts an electrical signal into an electromagnetic wave radiated in free space
  - Dimension is proportional to wavelength of carrier frequency
    - Wavelength = 300 meter / Freq (in MHz)
    - 1 MHz → 300 meter
    - 2.4 GHz → 12.5 cm
    - Antenna usually ½ or ¼ wavelength long

OR

Signal Power

- Signal power on resistor R
  - Voltage swing is sinusoidal with amplitude A (0-pk).
  - Power (Watt) = $A^2/(2R) = A_{rms}^2/R$ where $A_{rms} = A/\mathrm{sqrt}(2)$
- dBm
  - Power ratio in dB w/ respect to 1 mW.
  - 10mW => 10 log(10mW/1mW) = 10dBm

Watt	dBm	A_{rms}(in V) R=50ohm	Comment
1000	60	223	Typ. Microwave Oven
1	30	7.1	Cell Phone Transmit Power
1m	0	0.225	Bluetooth Transmit Power
50p	-73	50u	Bluetooth Receive Sensitivity
4e-21	-174	4.4e-10	Thermal Noise Floor in 1Hz at room temp

dBm

Calculate the peak-to-peak voltage swing for 0 dBm signal in 50-ohm system.

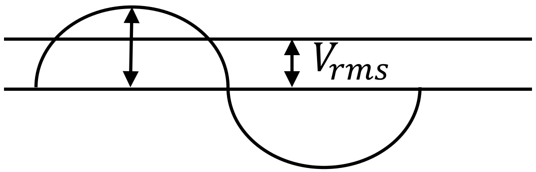
$$0\ dBm \leftrightarrow 1mW$$

$$Power = \frac{{V_{rms}}^2}{R} = \frac{{V_{rms}}^2}{50} = 0.001$$

$$V_{rms} = \sqrt{0.05} = 0.224$$

$$V_{pk-pk} = 2(0.224\ \cdot \sqrt{2}) = 0.632V$$

$$V_{pk} = V_{rms} \cdot \sqrt{2}$$



Voltage Gain and Power Gain

Voltage Gain $$A_V|_{\mathrm{dB}} = 20\log\frac{V_{out}}{V_{in}}$$

Power Gain $$A_P|_{\mathrm{dB}} = 10\log\frac{P_{out}}{P_{in}}$$

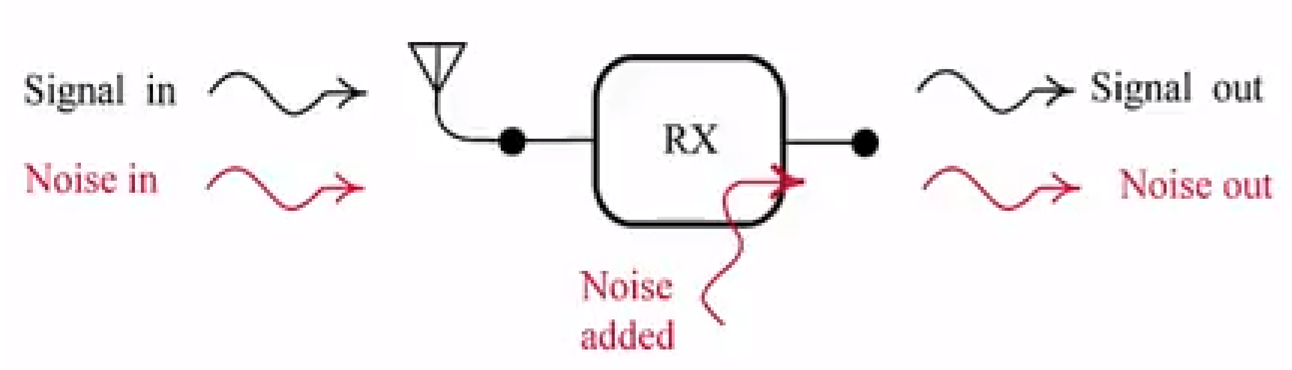
If an amplifier having an input resistance of Ri and driving a load resistance of Ro,

$$A_{P|dB} = 10log\frac{\frac{V_{out}^2}{R_o}}{\frac{V_{in}^2}{R_i}} = 10log\frac{V_{out}^2}{V_{in}^2} + 10log\frac{R_i}{R_o}$$

$$= 20log\frac{V_{out}}{V_{in}} + 10log\frac{R_i}{R_o} = A_{V|dB} + 10log\frac{R_i}{R_o}$$

Voltage Gain ≠ Power Gain if Rin ≠ Rout.

Noise Factor and Noise Figure (dB)



Signal Out = G x Signal In

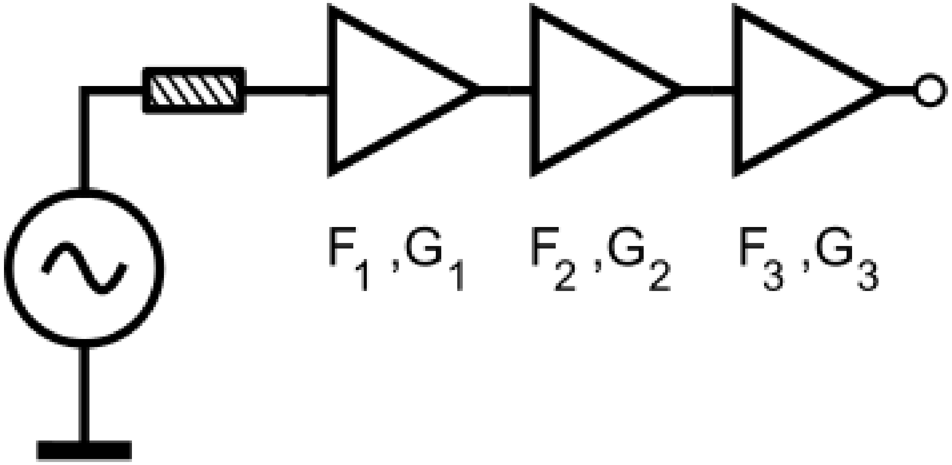
Noise Out = G x Noise In + Noise added

$$NF = \frac{(SNR)_{in}}{(SNR)_{out}} \geq 1$$ A receiver degrades the SNR!

Friis Formula

Friis's formula is used to calculate the total noise factor of a cascade of stages, each with its own noise factor and gain where F_i and G_i are the noise factor and available power gain.

Note that both magnitudes are expressed as ratios, not in decibels.

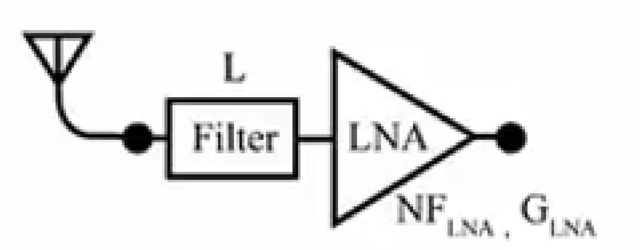


$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}$$

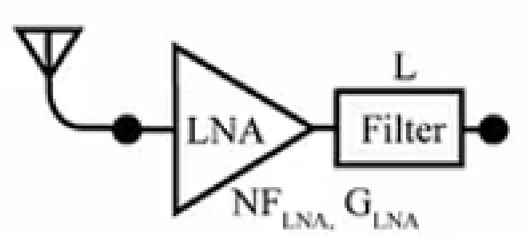
Noise Figure of Cascaded Stages

Example:
L = 1 dB = 1.25
G_{LNA} = 10 dB = 10
NF_{LNA} = 3 dB = 2

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1}$$



$$\begin{aligned} NF_{tot} &= L + (NF_{LNA} - 1) \cdot L \\ &= 1.25 + 1\text{x}1.25 = 2.5 = 4\text{dB} \end{aligned}$$

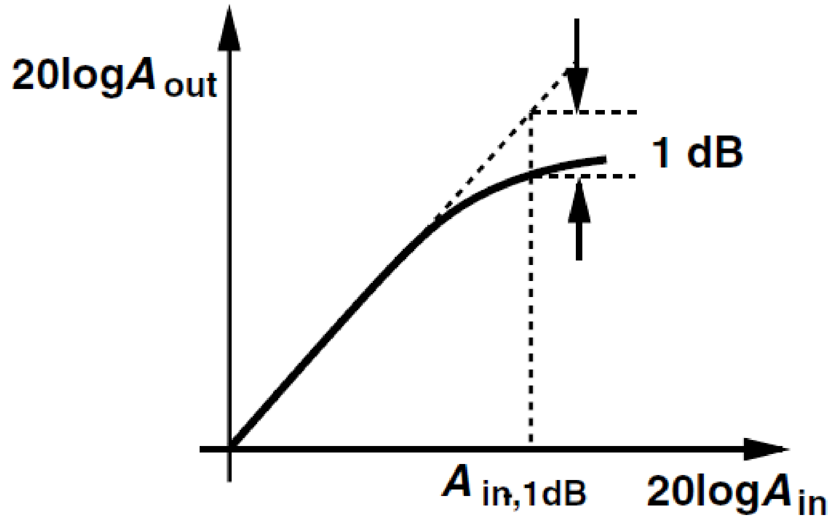


$$\begin{aligned} NF_{tot} &= NF_{LNA} + (L - 1) / G_{LNA} \\ &= 2 + 0.25/10 = 2.025 = 3dB \end{aligned}$$

1. Place those components with lowest NF and highest gain at earlier stages
2. Avoid lossy components at the input

Gain Compression

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos\omega t + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t$$



$$20\log\left|\alpha_1 + \frac{3}{4}\alpha_3 A_{in,1dB}^2\right| = 20\log|\alpha_1| - 1\text{ dB}$$

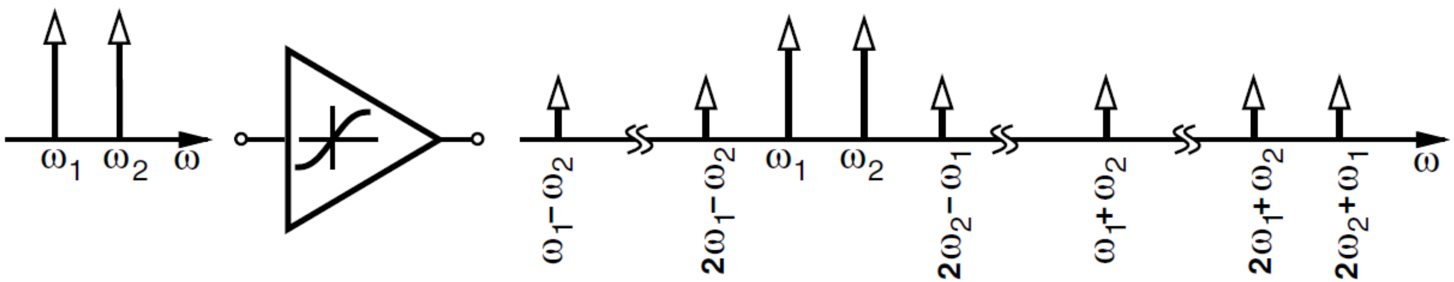
$$A_{in,1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$$

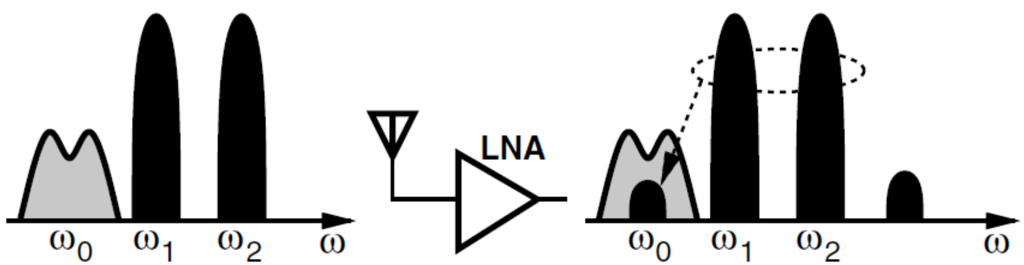
Intermodulation

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$$

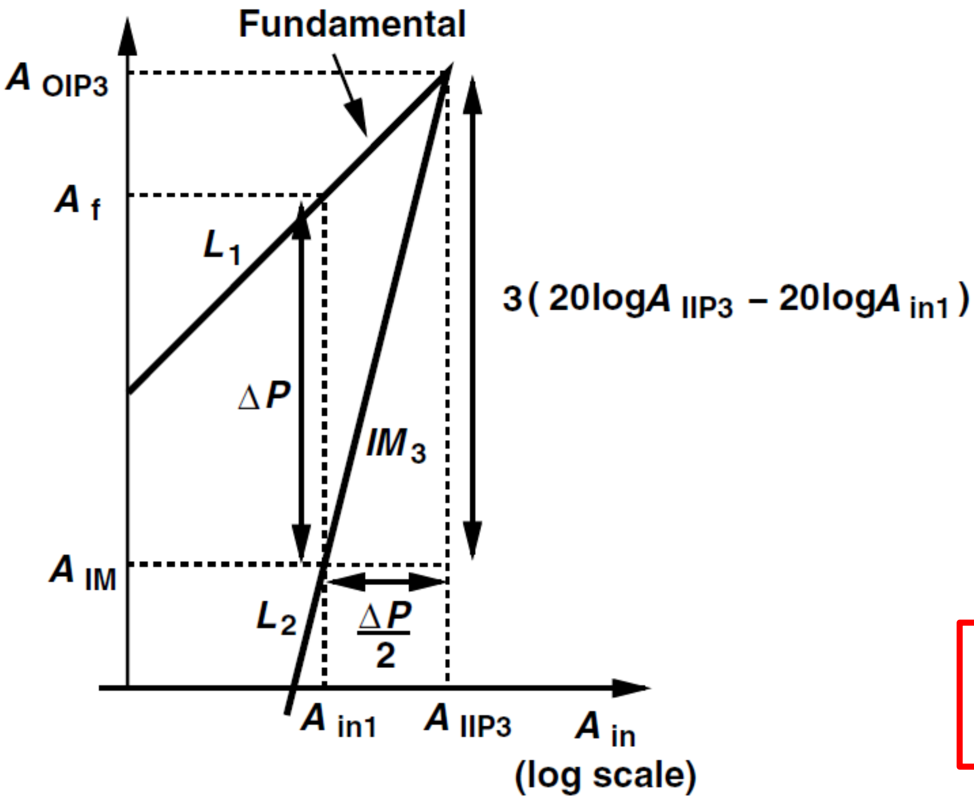
$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t$$

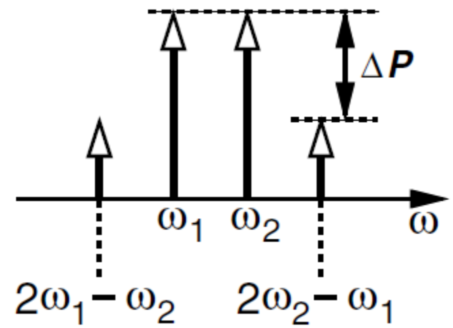
$$y(t) = \alpha_1(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t) + \alpha_2(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^2 + \alpha_3(A_1 \cos\omega_1 t + A_2 \cos\omega_2 t)^3.$$





IP3

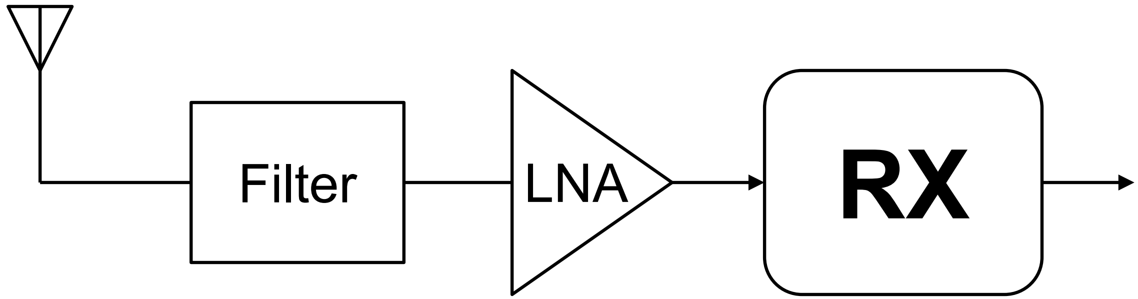




$$IIP_3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm}$$

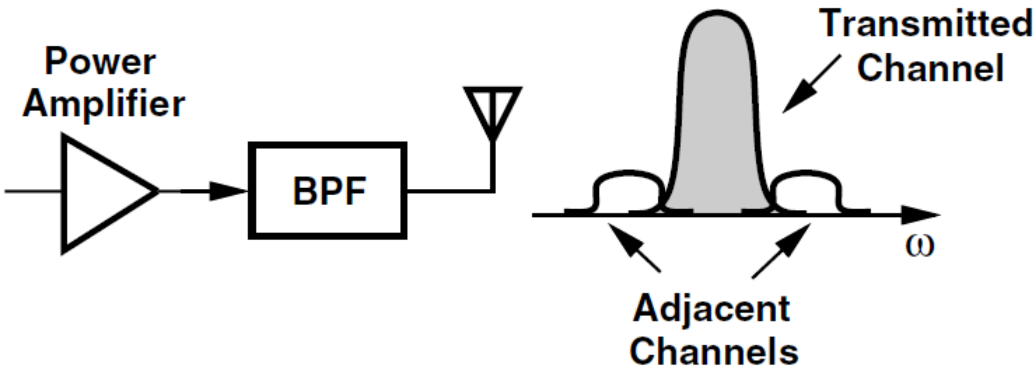
For a given input level (well below *P*1*dB*), the IIP3 can be calculated by halving the difference between the output fundamental and IM levels and adding the result to the input level,
where all values are expressed as logarithmic quantities.

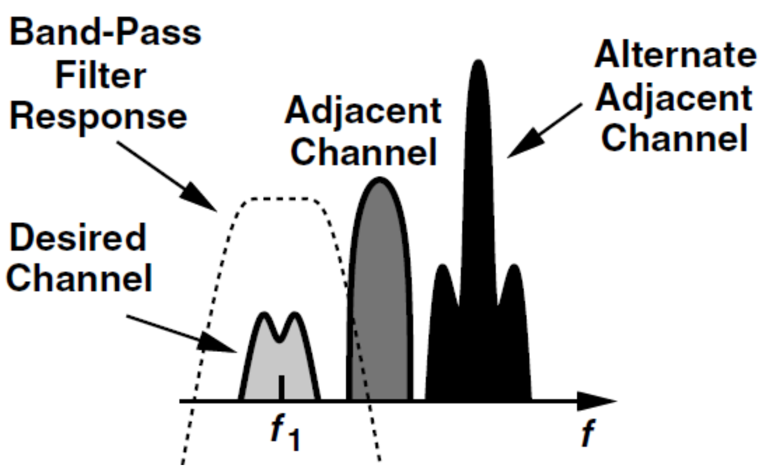
Receiver Architecture Types

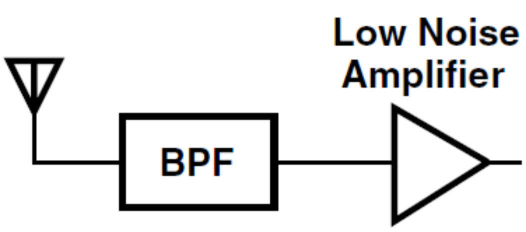


- Heterodyne
- Super-Heterodyne
- Homodyne (Direct conversion or Zero IF)

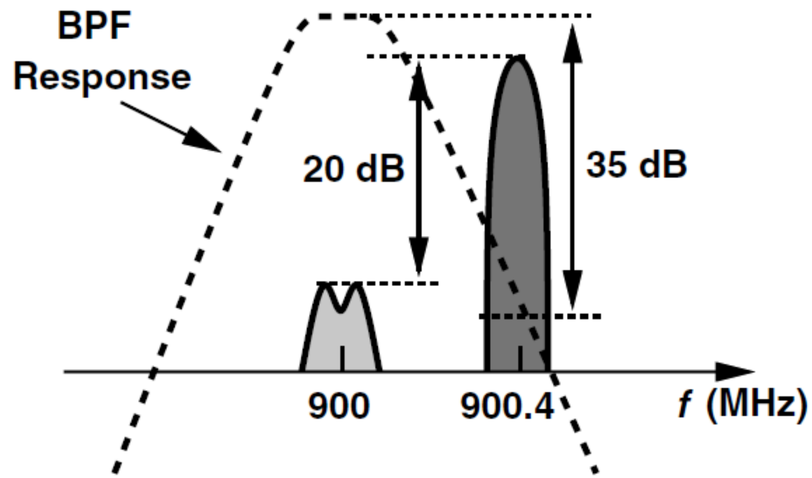
Transceiver Front-End





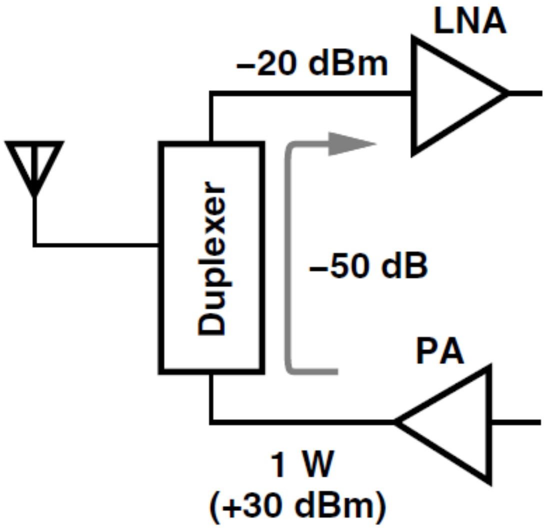


Band Pass Filter



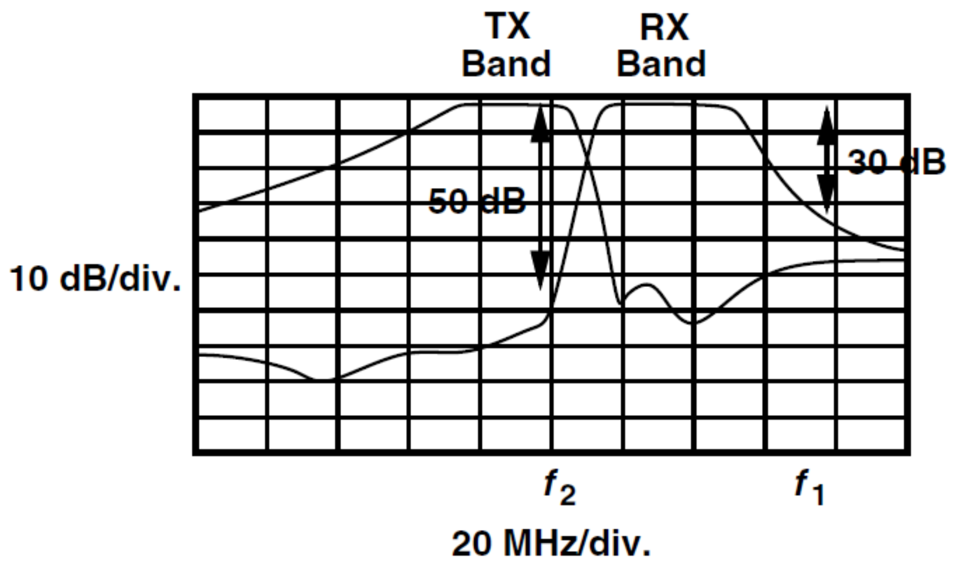
- First, the filter must provide a very high *Q*
- Second, the filter would need a variable, yet precise center frequency

TX–RX Feedthrough



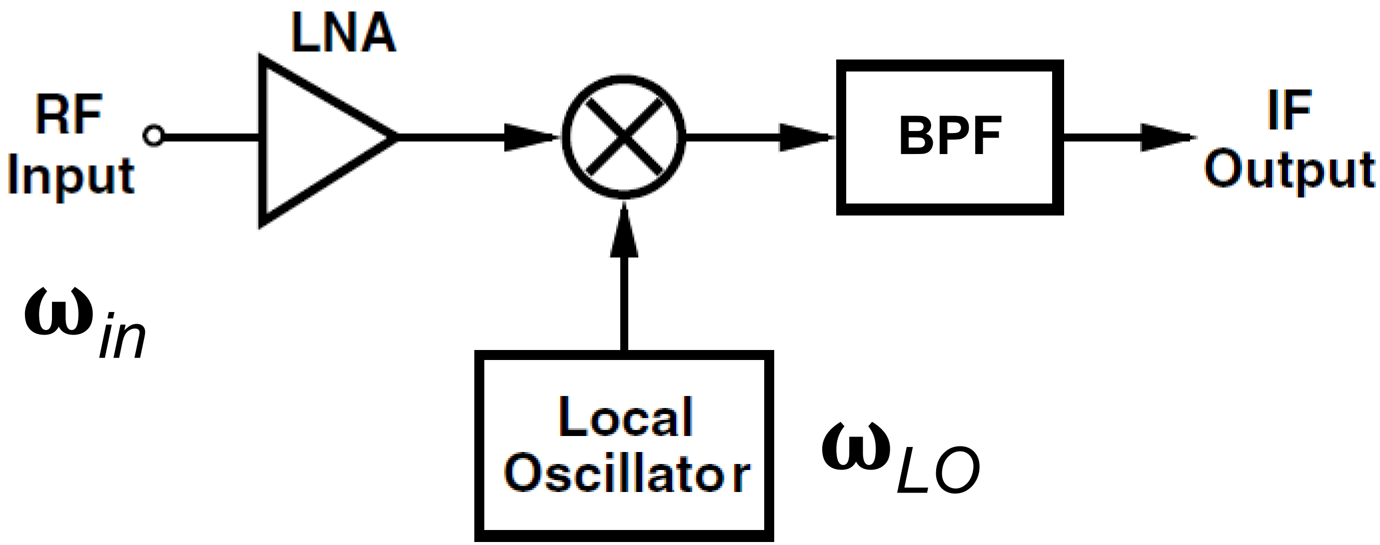
- In full-duplex standards, the TX and the RX operate concurrently.
- With a 1-W TX power, the leakage sensed by LNA can reach -20dBm, dictating a substantially higher RX compression point.

Duplexer Characteristics



- The front-end band-select filter suffers from a trade-off between its selectivity and its in-band loss because the edges of the band-pass frequency response can be sharpened only by increasing the order of the filter.
- Front-end loss directly raises the *NF* of the entire receiver

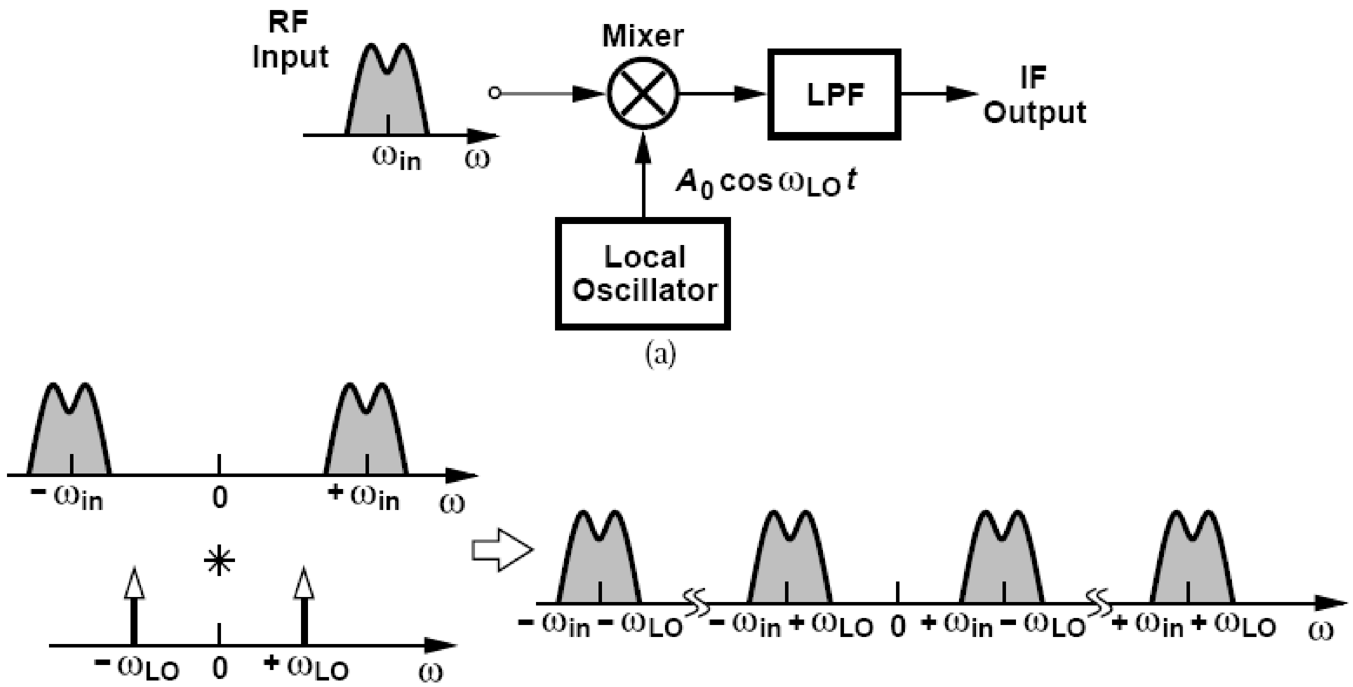
Heterodyne Receiver



$$\omega_{in} \neq \omega_{LO}$$

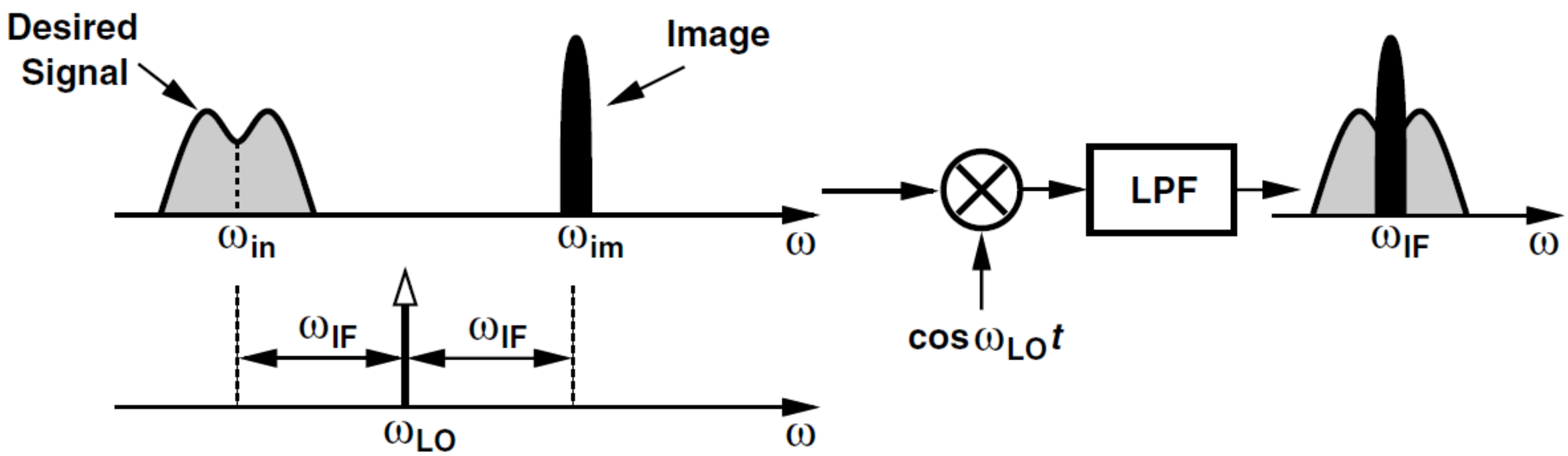
$$\omega_{in} - \omega_{LO} = \omega_{IF}$$

Basic Heterodyne Receiver



- "Heterodyne" receivers employ an LO frequency unequal to ω_{in} and hence a nonzero IF
- A Mixer performs downconversion.
- Due to its high noise, the downconversion mixer is preceded by a low-noise amplifier

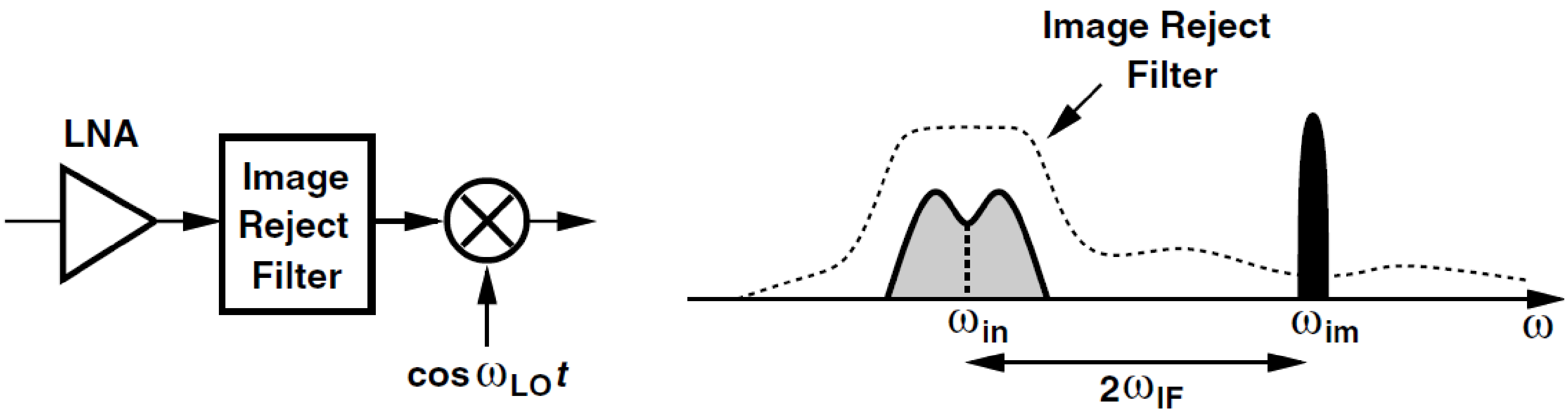
Problem of Image



$$A\cos\omega_{IF}t = A\cos(\omega_{im}-\omega_{LO})t$$
$$= A\cos(\omega_{LO}-\omega_{in})t$$

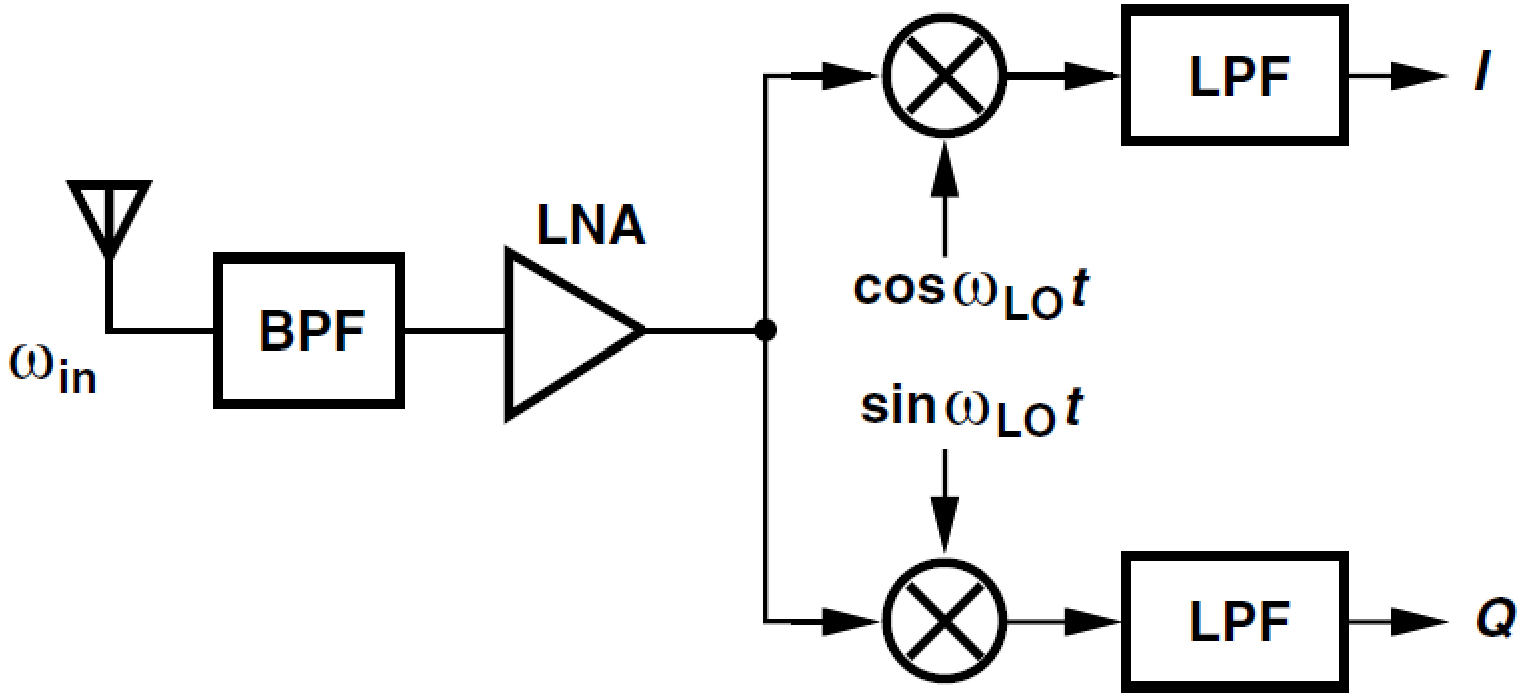
- Two spectra located symmetrically around ω_{LO} are downconverted to the IF

Image Reject Filter



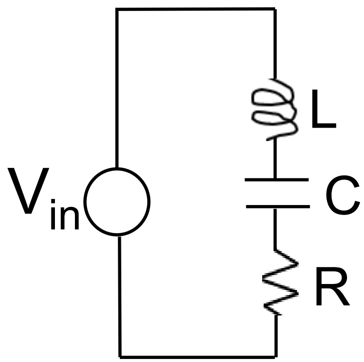
- **The most common approach is to precede the mixer with an "image-reject filter"**
- **A filter with high image rejection typically appears between the LNA and the mixer so that the gain of the LNA lowers the filter's contribution to the receiver noise figure**
- **The linearity and selectivity required of the image-reject filter have dictated passive, off-chip implementations.**

Direct Conversion Receiver



- ➢ **Absence of an image greatly simplifies the design process**
- ➢ **Channel selection is performed by on-chip low-pass filter**
- ➢ **Mixing spurs are considerably reduced in number**

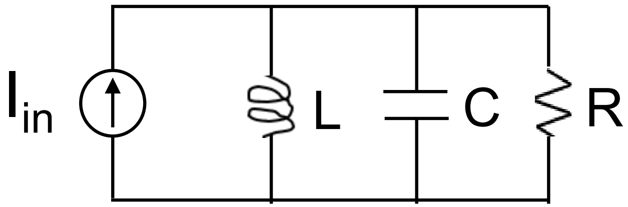
Series & Parallel Resonance



$$Z(\omega_0) = R$$

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 C R}$$

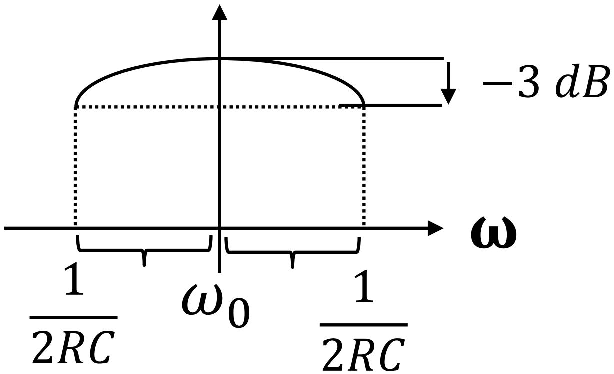
$$|V_L| = |V_C| = Q \cdot |V_{in}|$$



$$Q = \frac{R}{\omega_0 L} = \omega_0 R C$$

$$|I_L| = |I_C| = Q \cdot |I_{in}|$$

BW & Q relationship



$$Total\ BW = \frac{1}{RC}$$

$$\frac{\omega_0}{BW} = \frac{RC}{\sqrt{LC}} = \frac{R}{\sqrt{L/C}} = Q$$

Series-Parallel Transformation

R_p is always larger than R_s

$$R_p = R_s(1 + Q^2) \qquad \Longrightarrow \qquad Q = \sqrt{\frac{R_p}{R_s} - 1}$$

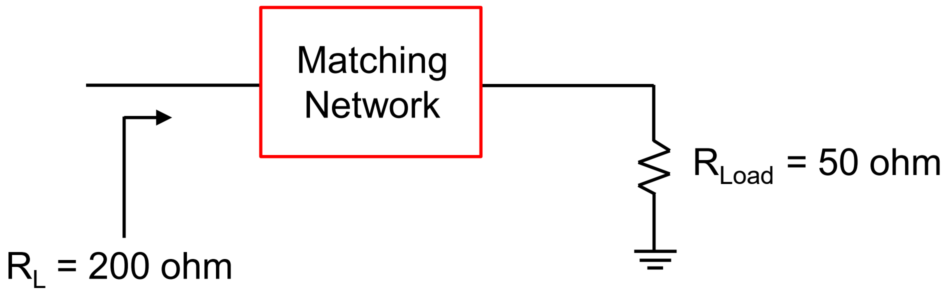
$$X_p = X_s \frac{1+Q^2}{Q^2} \approx X_s$$

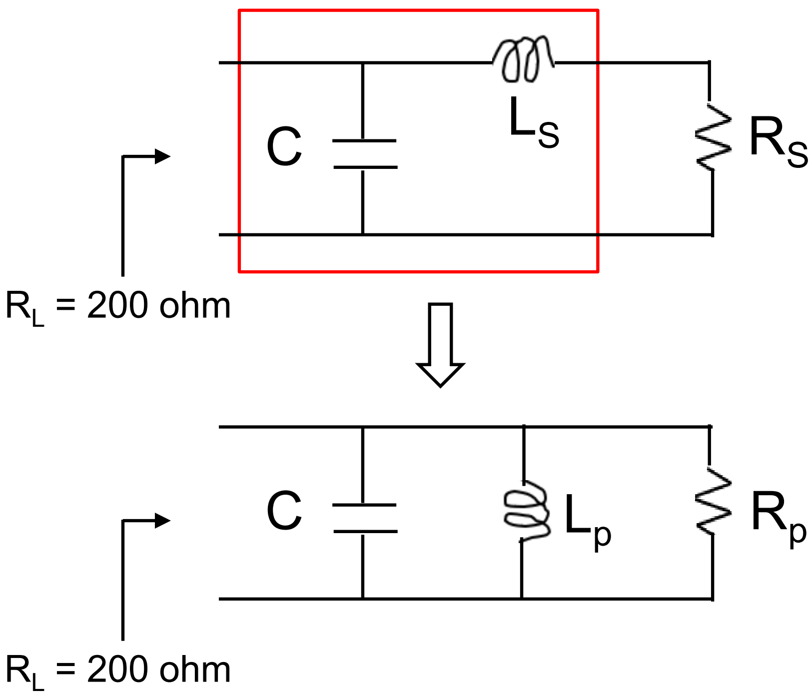
$$L_p = L_s \frac{1+Q^2}{Q^2} \approx L_s$$

$$C_p = C_s \frac{Q^2}{1+Q^2} \approx C_s$$

L-Match: Upward Impedance Transform

Low-pass L-match



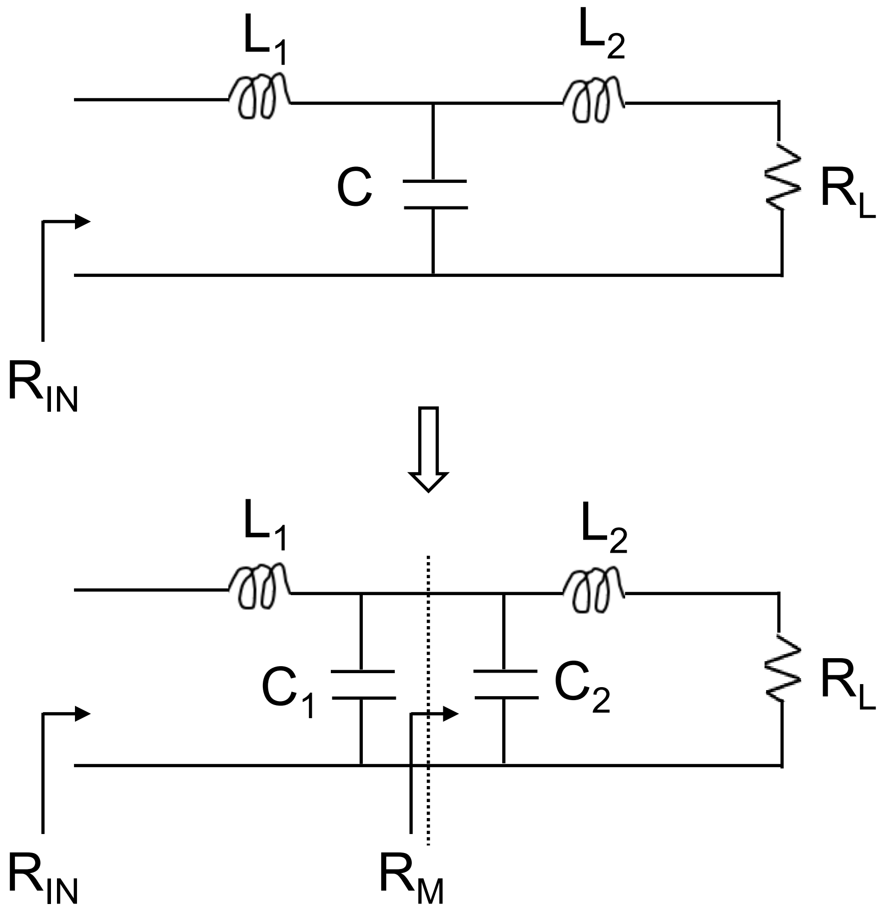


$$R_p = R_s(1 + Q^2)$$

$$L_p = L_s \frac{1 + Q^2}{Q^2}$$

T-Match

To design for a different Q, i.e. different Bandwidth for a given ω_0
We need another degree of freedom



$$Q = Q_L + Q_R$$

$$= \sqrt{\frac{R_M}{R_{IN}} - 1} + \sqrt{\frac{R_M}{R_L} - 1}$$

$R_M > R_L$

$R_M > R_{IN}$

Exercises

We would like to use the matching network shown in Fig. 1 to transform $R_L = 50\Omega$ up to $R_{in} = 100\Omega$. The matching network should be designed for operation at a frequency of 1 GHz, and should have an overall quality factor of $Q = 100$. **In all series-parallel transformation, you may use the high Q approximation ($Q^2 >> 1$).**

Choose appropriate values for C_1, L_1, and L_2.

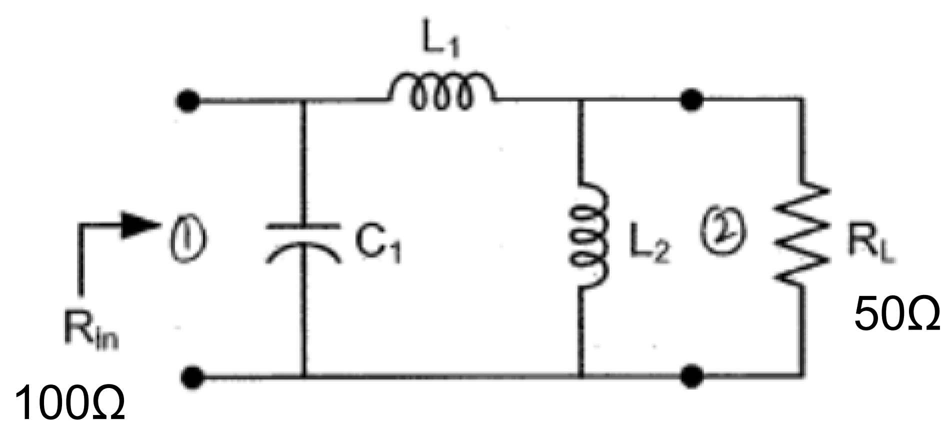
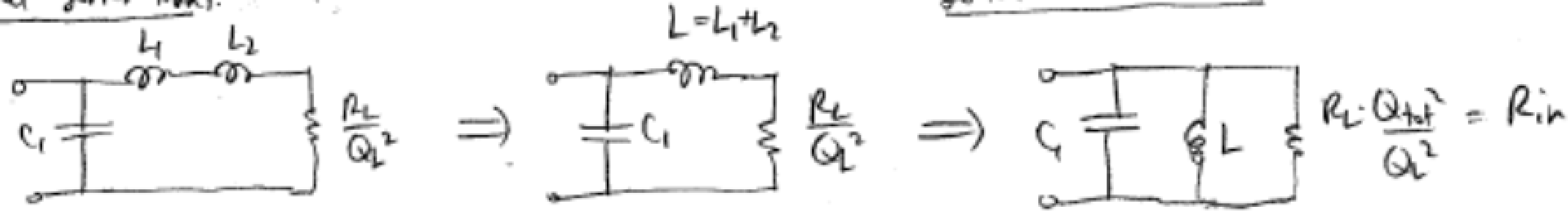


Fig. 1

Parallel - Series trans. Series - Parallel trans.



Now, $R_{in} = R_L \cdot \frac{Q_{tot}^2}{Q_L^2} \Rightarrow Q_R^2 = \frac{R_L}{R_{in}} Q_{tot}^2 = \frac{50}{100}(100)^2 \Rightarrow \boxed{Q_R \approx 71.}$

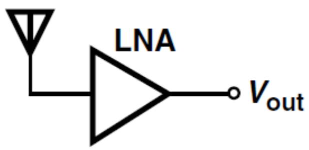
Also, $Q_{tot} = \frac{R_{in}}{\omega_0 L} \Rightarrow L = \frac{R_{in}}{Q_{tot} \cdot \omega_0} = \frac{100}{100 \cdot 2\pi \cdot 1E9} = 1.59E{-10} = L = L_1 + L_2$

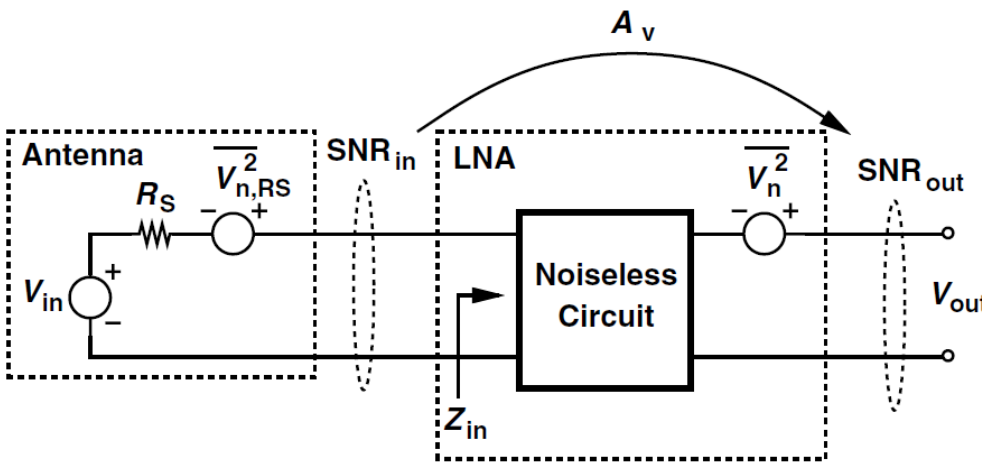
To find L_1 & L_2, use Q_R: $Q_R = \frac{R_L}{\omega_0 L_2} \Rightarrow L_2 = \frac{R_L}{Q_R \cdot \omega_0} = \frac{50}{71 \cdot 2\pi \cdot 1E9} = \boxed{1.13E{-10} = L_2}$

$L_1 = L - L_2 = 1.59E{-10} - 1.13E{-10} = \boxed{4.6E{-11} = L_1}$

Use ω_0 to find C_1: $\omega_0 = \frac{1}{\sqrt{LC_1}} \Rightarrow C_1 = \frac{1}{\omega_0^2 L} = \frac{1}{(2\pi \cdot 1E9)^2 \cdot 1.59E10} = \boxed{1.59E{-10} = C_1}$

Noise Figure





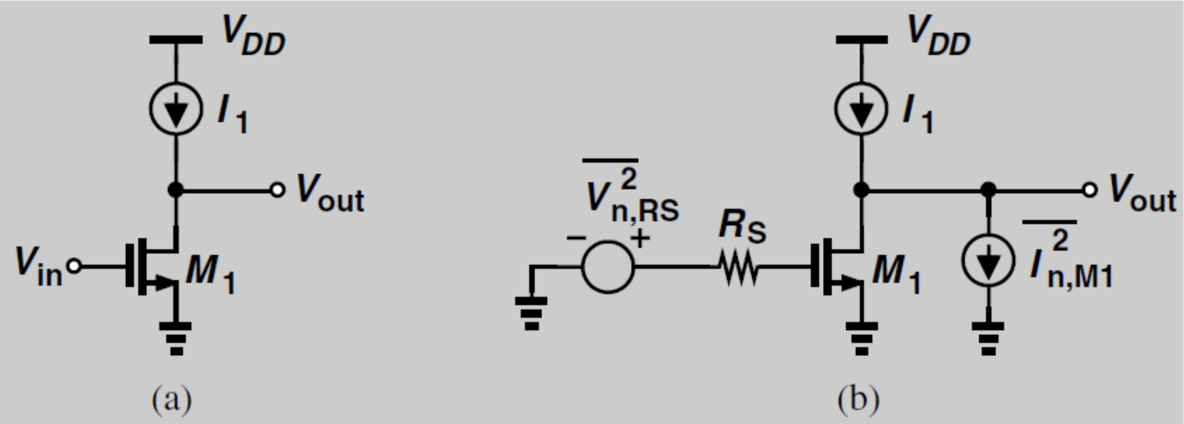
$$\mathrm{NF} = \frac{SNR_{in}}{SNR_{out}} \qquad SNR_{in} = \frac{|\alpha|^2 V_{in}^2}{|\alpha|^2 \overline{V_{RS}^2}} \qquad SNR_{out} = \frac{V_{in}^2 |\alpha|^2 A_v^2}{\overline{V_{RS}^2}|\alpha|^2 A_v^2 + \overline{V_n^2}}$$

$$\mathrm{NF} = \frac{V_{in}^2}{4kTR_S} \cdot \frac{\overline{V_{RS}^2}|\alpha|^2 A_v^2 + \overline{V_n^2}}{V_{in}^2 |\alpha|^2 A_v^2} = \frac{1}{4kTR_S} \cdot \frac{\overline{V_{n,out}^2}}{A_0^2} = \frac{\textit{Total Output Noise}}{\textit{Output Noise due to Source}}$$

$$= \frac{\textit{Noise due to Source} + \textit{Noise due to Circuit}}{\textit{Noise due to Source}} = 1 + \frac{\textit{Noise due to Circuit}}{\textit{Noise due to Source}}$$

Noise Figure Calculation Example

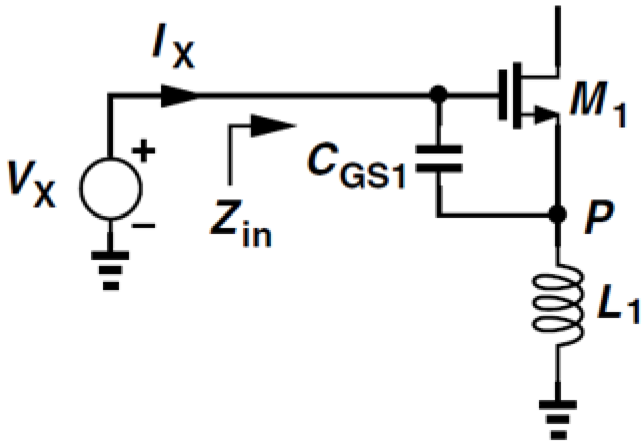
Determine the noise figure of the common-source stage shown below with a source impedance R_S. Neglect the capacitances and flicker noise of M1 and assume I_1 is ideal.



$$NF = \frac{Total\ Output\ Noise}{Output\ Noise\ due\ to\ Source}$$

$$= \frac{(4kT\gamma g_m)r_o^2 + 4kTR_s(g_m r_o)^2}{4kTR_s(g_m r_o)^2} \quad = 1 + \frac{\gamma}{g_m R_s}$$

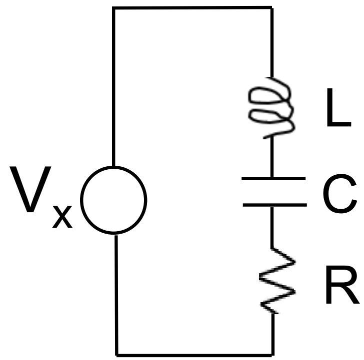
Series Resonance in LNA



$$\frac{V_X}{I_X} = \boxed{\frac{1}{C_{GS1}s} + L_1 s} + \boxed{\frac{g_m L_1}{C_{GS1}}}$$

Resonate

$50\ \Omega$

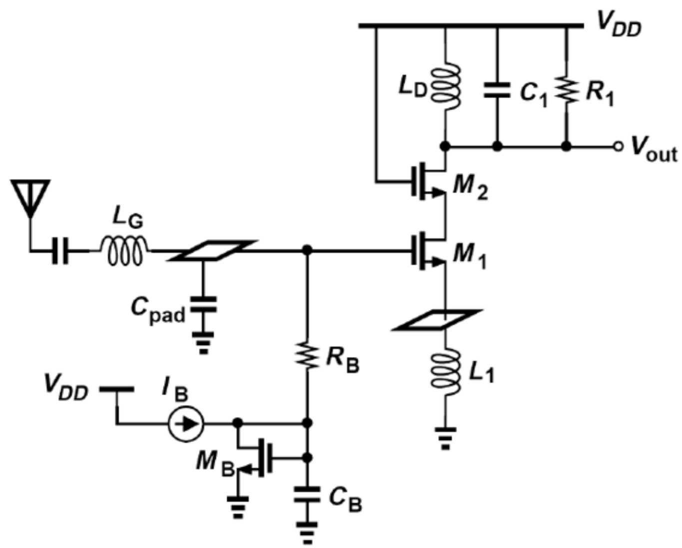


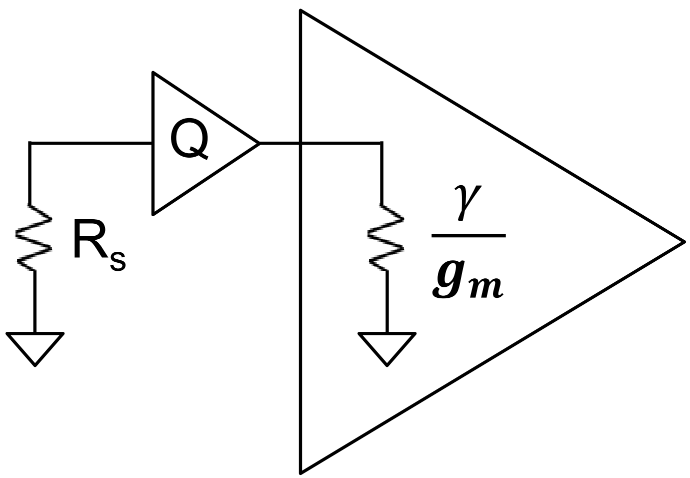
$$Z(\omega_0) = R$$

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR}$$

$$|V_L| = |V_C| = Q \cdot |V_x|$$

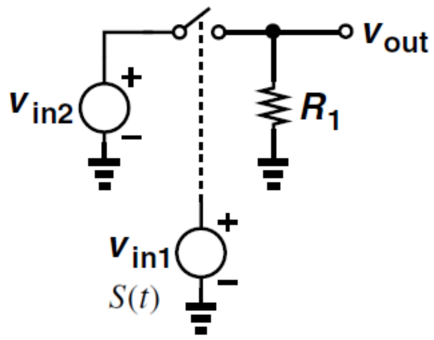
Noise Figure of CS LNA with Inductive Degeneration



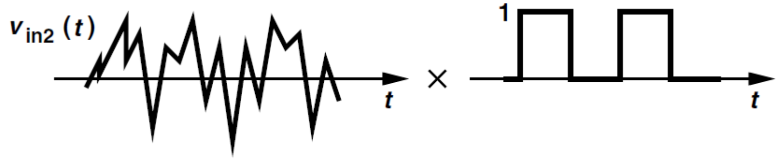


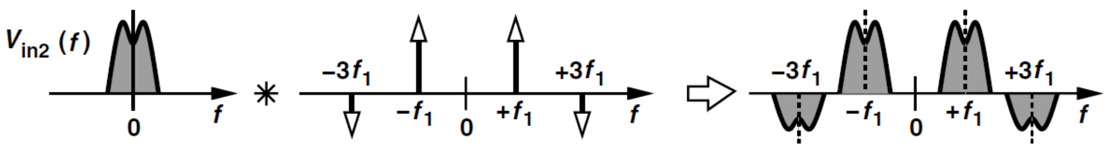
$$NF = 1 + \frac{\gamma}{Q^2 g_m R_S}$$

RF Mixer



$$v_{out}(t) = v_{in2}(t) \cdot S(t)$$





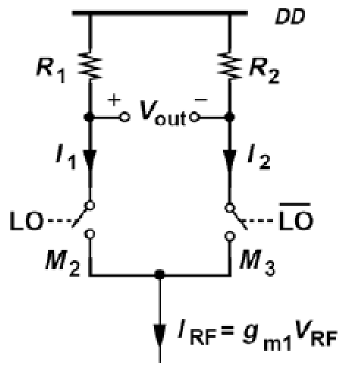
$$T_1 = 2\pi/\omega_1$$

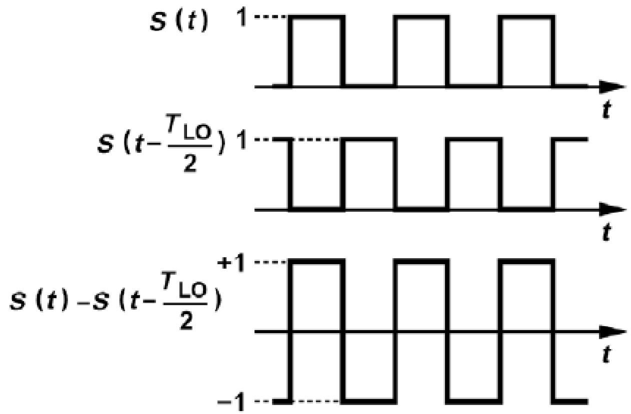
$$V_{out}(f) = V_{in2}(f) * \sum_{n=-\infty}^{+\infty} \frac{\sin(n\pi/2)}{n\pi} \delta\left(f - \frac{n}{T_1}\right) = \sum_{n=-\infty}^{+\infty} \frac{\sin(n\pi/2)}{n\pi} V_{in2}\left(f - \frac{n}{T_1}\right)$$

What is the amplitude when n=1? $\Rightarrow$ $\frac{1}{\pi}$

Conversion Gain

With abrupt LO switching, the circuit reduces to that shown in figure below (left).





$$I_1 = I_{RF} \cdot S(t)$$
$$I_2 = I_{RF} \cdot S\left(t - \frac{T_{LO}}{2}\right)$$

We have for $R_1 = R_2 = R_D$ $V_{out}(t) = I_{RF} R_D \left[S\left(t - \frac{T_{LO}}{2}\right) - S(t) \right]$

The waveform exhibits a fundamental amplitude equal to $4/\pi$, yielding an output given by

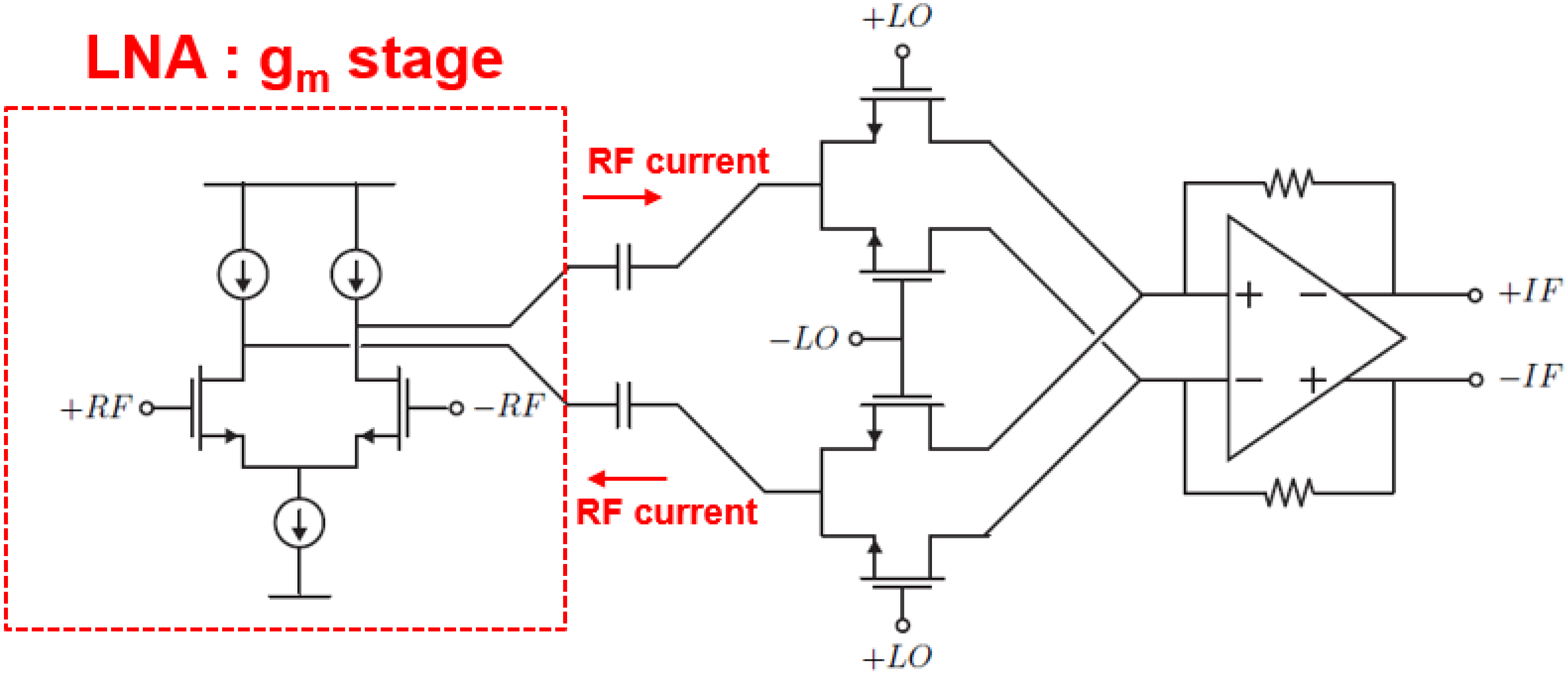
$$V_{out}(t) = I_{RF}(t) R_D \cdot \frac{4}{\pi} \cos \omega_{LO} t + \cdots$$

If $I_{RF}(t) = g_{m1} \cdot V_{RF} \cdot \cos(\omega_{RF} t)$, then

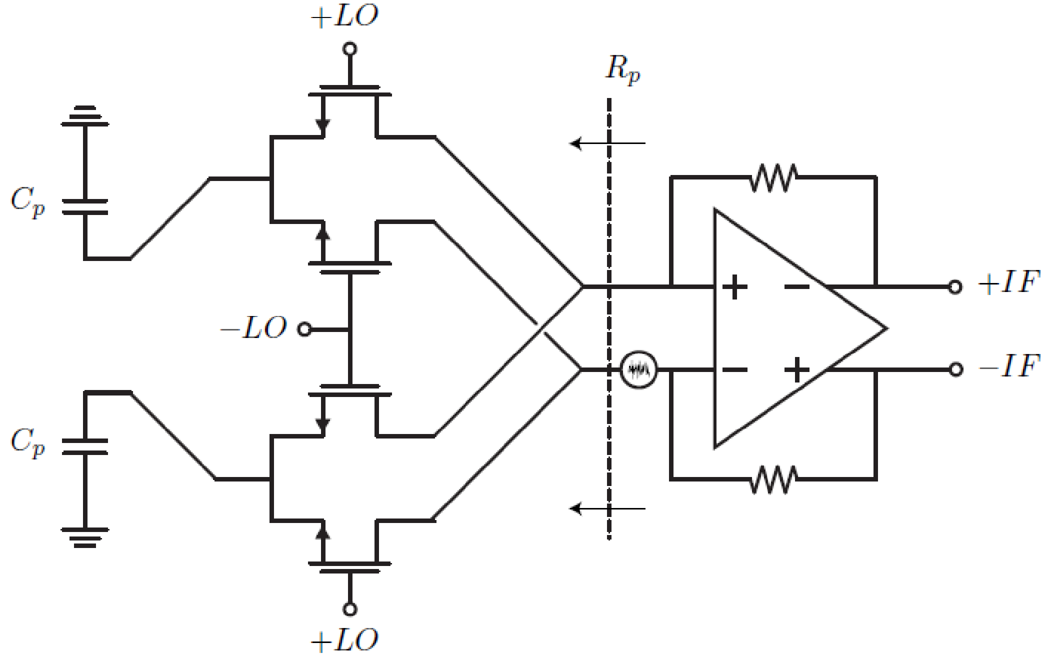
$$V_{IF}(t) = \frac{2}{\pi} g_{m1} R_D V_{RF} \cos(\omega_{RF} - \omega_{LO})t$$

$$\boxed{\frac{V_{IF,p}}{V_{RF,p}} = \frac{2}{\pi} g_{m1} R_D}$$

LNA + Passive Mixer

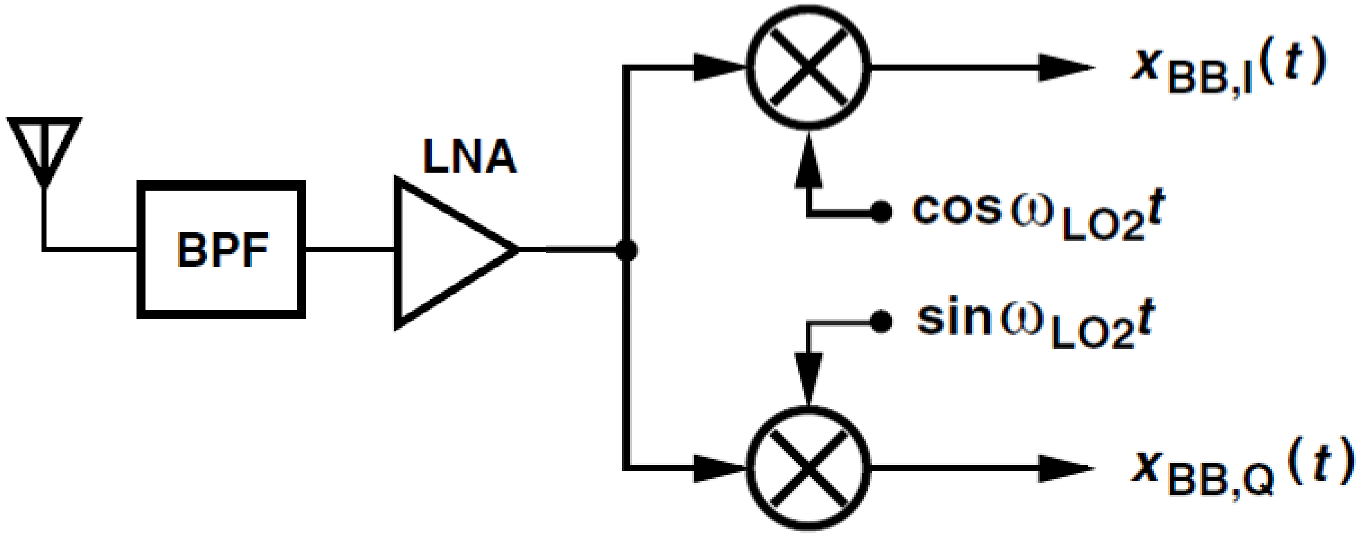


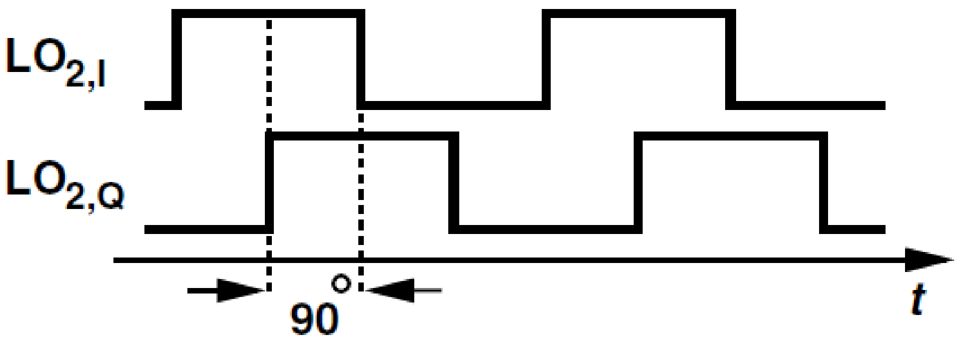
OPAMP Noise



- The op-amp input referred noise is amplified to IF. The resistance seen at the op-amp input terminals is actually a switched capacitor resistor!
- The parasitic capacitance at the output of the transconductance stage is charged and discharged at the rate of the LO.

Quadrature Mixing



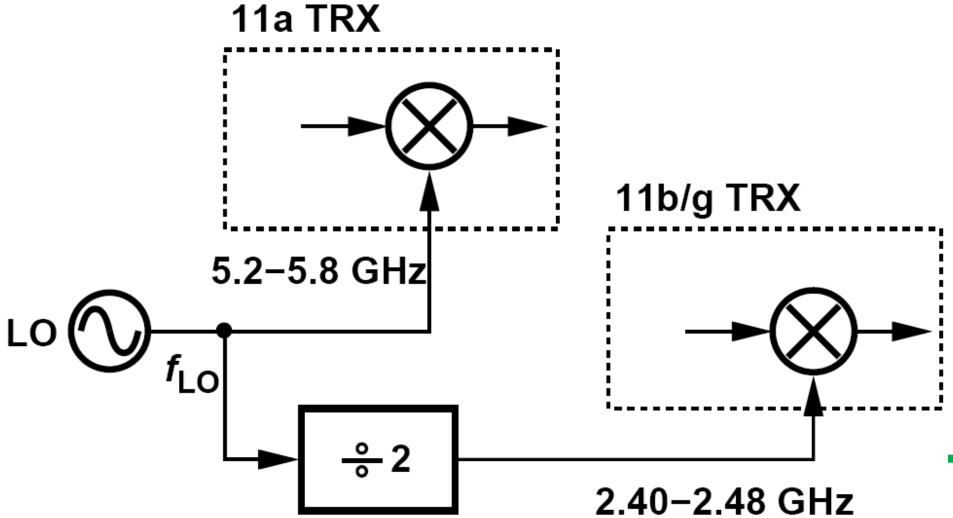


Oscillator Frequency Range

- An RF oscillator Tuning Range based on two components:
  (1) The system specification;
  (2) Margin to cover PVT variations and errors due to modeling inaccuracies.

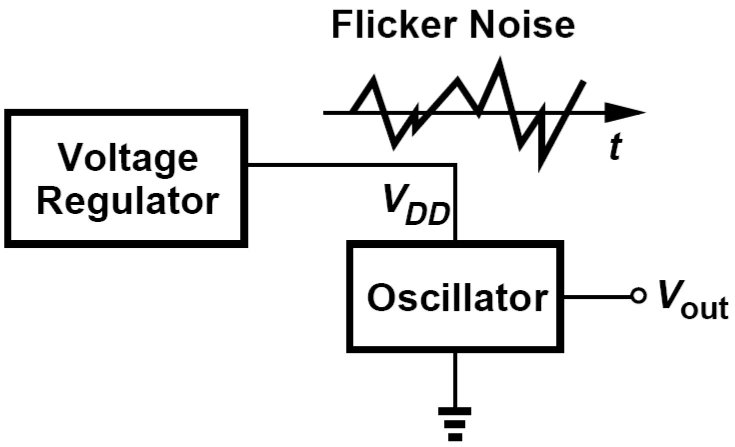
For a direct-conversion transceiver with 2.4-GHz and 5-GHz wireless bands, what is the minimum acceptable tuning range if a single LO must cover both?

For the lower band, 4.8 GHz ≤ f_{LO} ≤ 4.96 GHz.
Thus, a total tuning range of 4.8 GHz to 5.8 GHz, about 20%.
Such a wide tuning range is relatively difficult to achieve in LC oscillators.



Performance Parameters: Supply Sensitivity & Power Dissipation

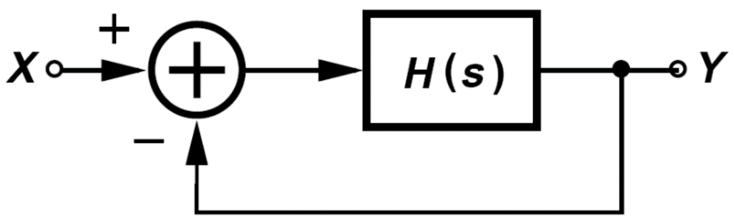
- The frequency of an oscillator may vary with the supply voltage, an undesirable effect because it translates supply noise to frequency (and phase) noise.



- The power drained by the LO and its buffer(s) proves critical in some applications as it trades with the phase noise and tuning range.

Feedback View of Oscillators

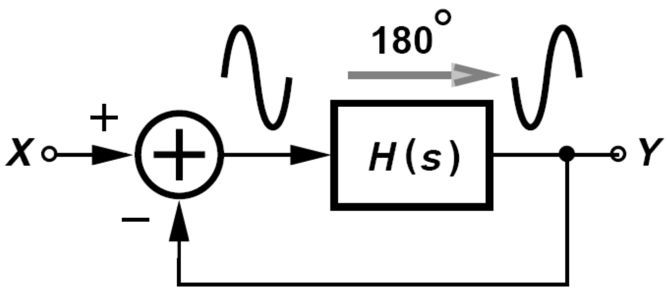
- An oscillator may be viewed as a “badly-designed” negative-feedback amplifier—so badly designed that it has a zero or negative phase margin.

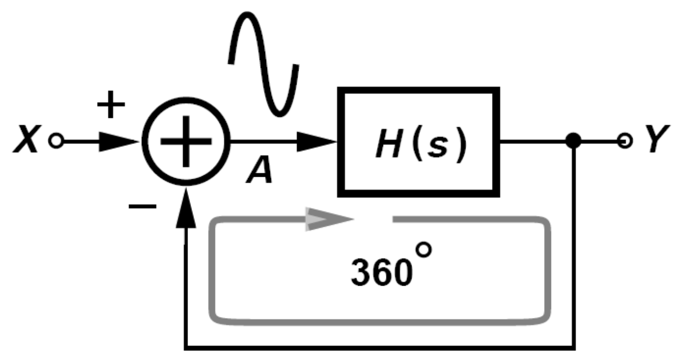


$$\frac{Y}{X}(s) = \frac{H(s)}{1 + H(s)}$$

Barkhausen's Criteria

$$|H(s = j\omega_1)| = 1$$
$$\angle H(s = j\omega_1) = 180^\circ$$

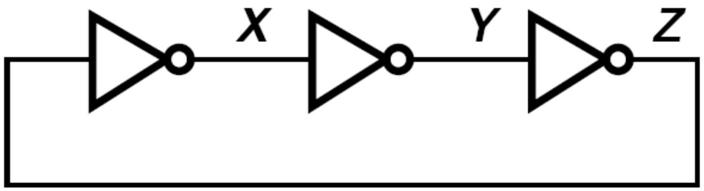


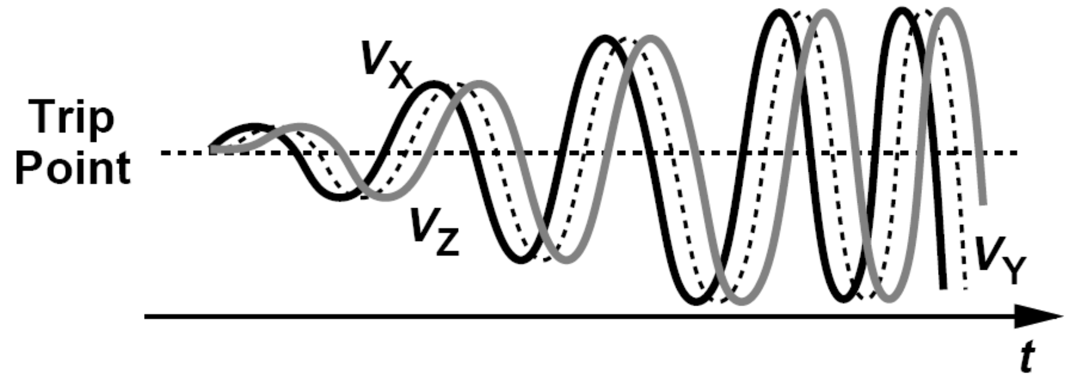


- For an Oscillation, the signal returning to A must exactly coincide with the signal that started at A.
- Requires 180° Phase Shift through H(s).
- This additional phase shift of 180° along with the original negative feedback turns into a positive feedback at ω_1, at this frequency.

Ring Oscillator

- Other oscillators oscillate at a frequency at which the loop gain is higher than unity, thereby experiencing an exponential growth in their output amplitude.
- The growth eventually stops due to the saturating behavior of the amplifier(s) in the loop.





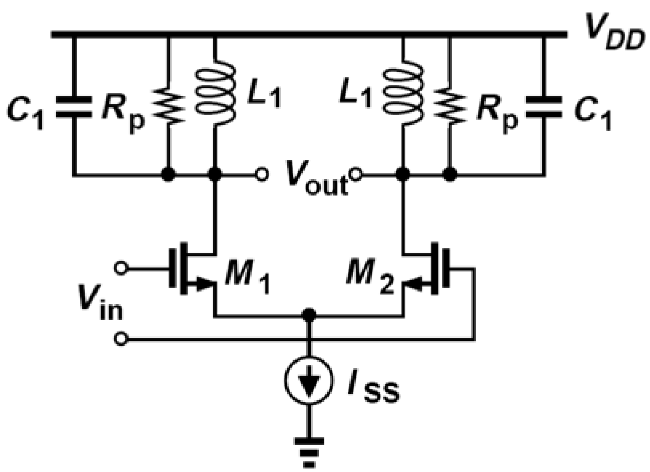
- Each stage operates as an amplifier, leading to an oscillation frequency at which each inverter contributes a frequency-dependent phase shift of 60° .

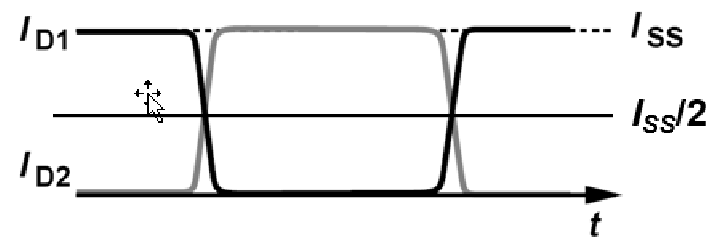
Example of Voltage Swings (I)

The inductively-loaded differential pair driven by a large input sinusoid at

$$\omega_0 = 1/\sqrt{L_1 C_1}$$

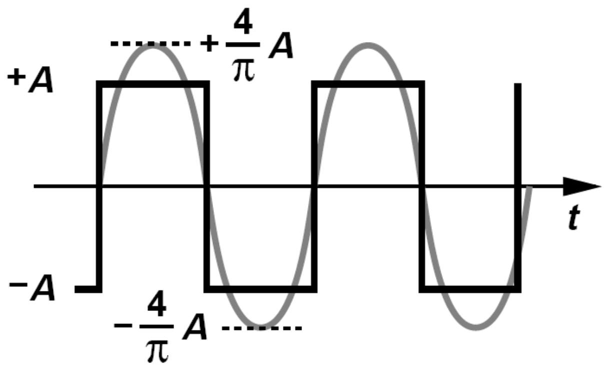
Plot the output current waveforms and determine the output Current swing.

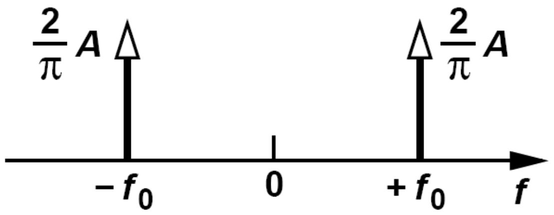




- **With large swings, M_1 and M_2 experience complete switching injecting nearly square current waveforms into the tanks.**
- **The first harmonic of the current is multiplied by R_p**
- **Higher harmonics are attenuated by the tank selectivity.**

Example of Voltage Swings (Ⅱ)

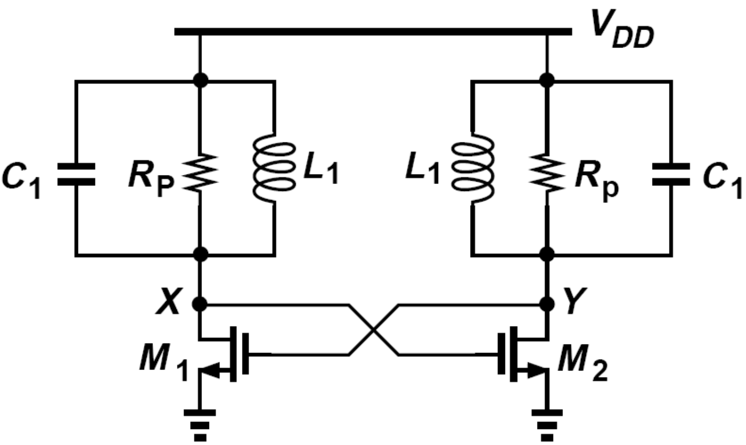


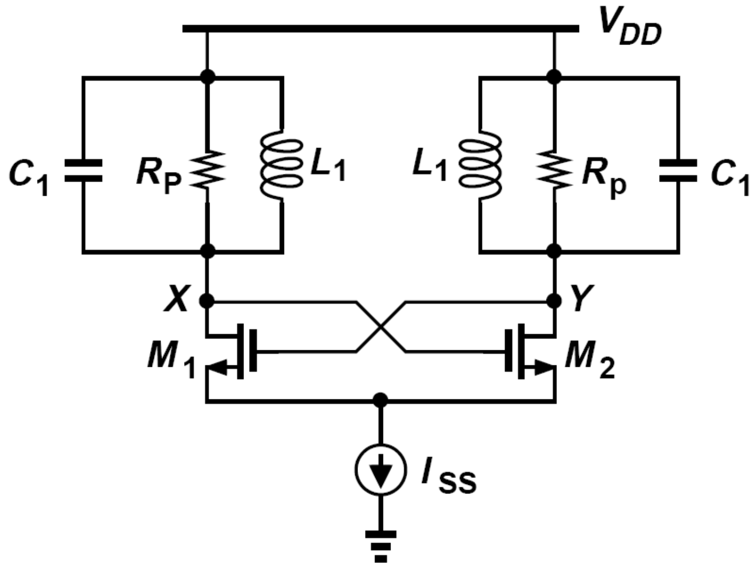


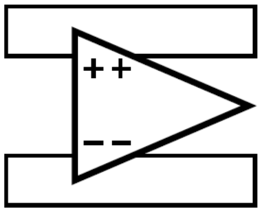
- **Fourier expansion of a square wave of peak amplitude A (with 50% duty cycle) that the first harmonic exhibits a peak amplitude of (4/*π*)*A* (slightly greater than A).**
- **The peak single-ended output swing therefore yields a peak differential output swing of**

$$\boxed{V_{out} = \frac{4}{\pi} I_{SS} R_p}$$

Cross-Coupled Oscillator





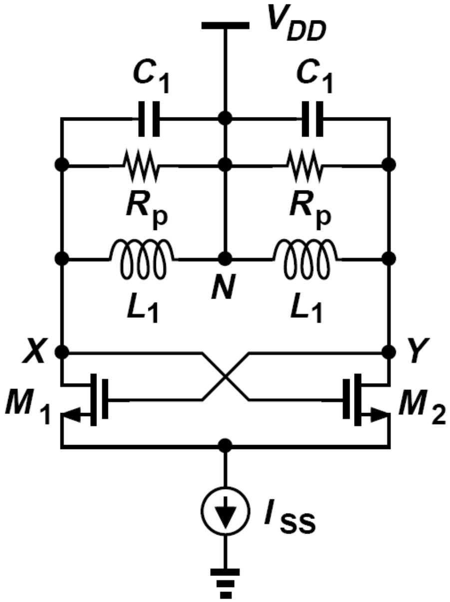


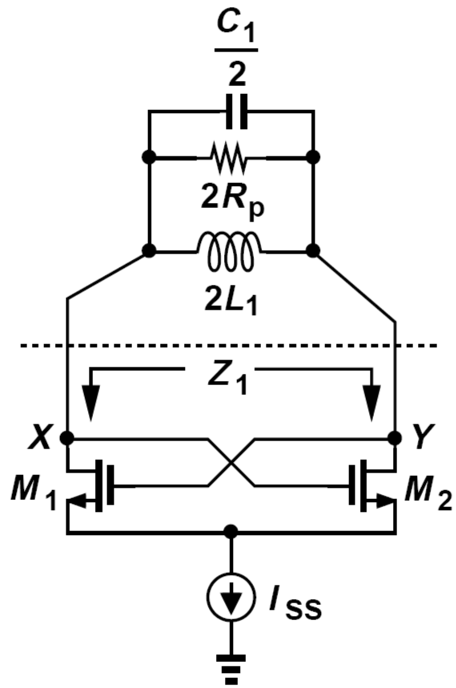
$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_{GS2} + C_{DB1} + 4C_{GD} + C_1)}}$$

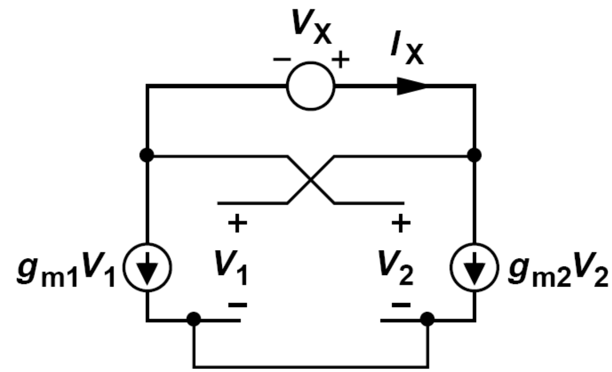
Left circuit suffers from poorly-defined bias currents.
Middle circuit is more robust and can be viewed as an inductively-loaded differential pair with positive feedback.

$$V_{XY} \approx \frac{4}{\pi} I_{SS} R_p$$

One-Port View of Cross-Coupled Oscillator







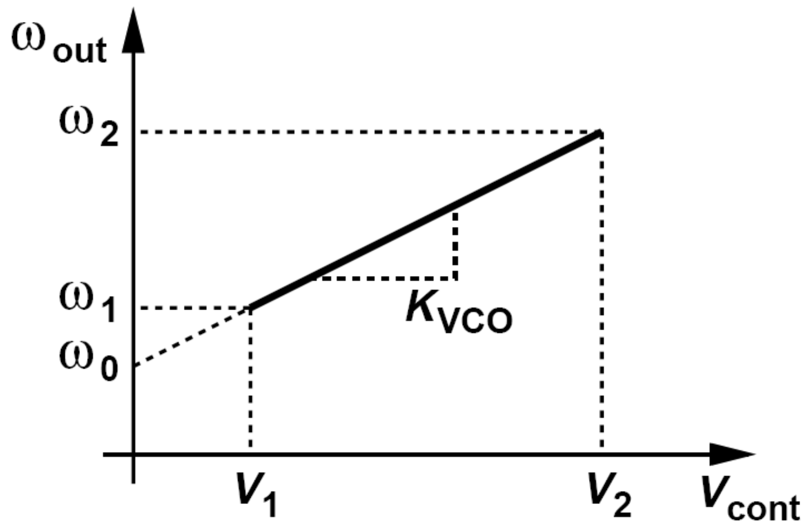
$$I_X = -g_{m1}V_1 = g_{m2}V_2 \quad \Rightarrow \quad \frac{V_X}{I_X} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right)$$

For $g_{m1} = g_{m2} = g_m$ $\quad \frac{V_X}{I_X} = -\frac{2}{g_m}$

For oscillation to occur,
the negative resistance must cancel the loss of the tank:

$$\frac{2}{g_m} \le 2R_p \quad \Rightarrow \quad g_m R_p \ge 1$$

Voltage-Controlled Oscillators: Characteristic

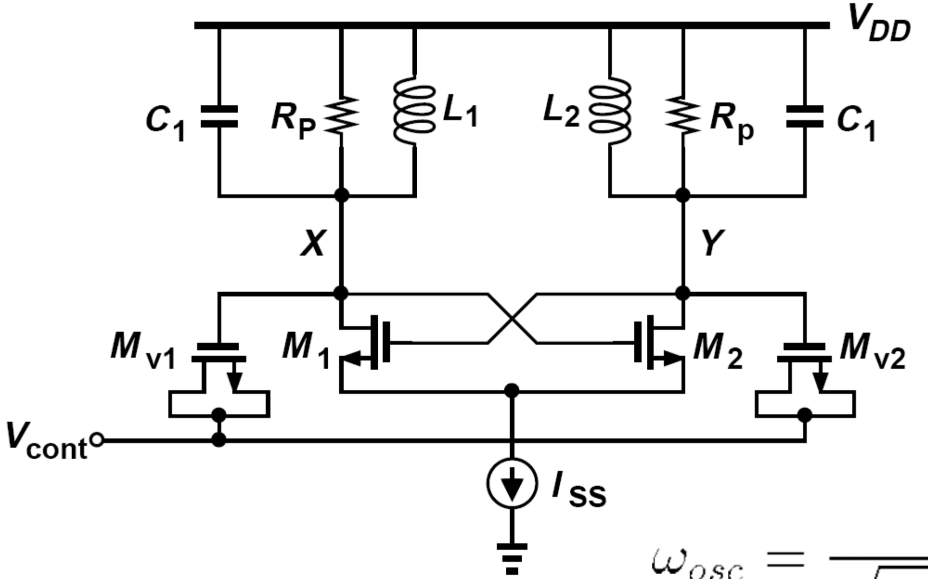


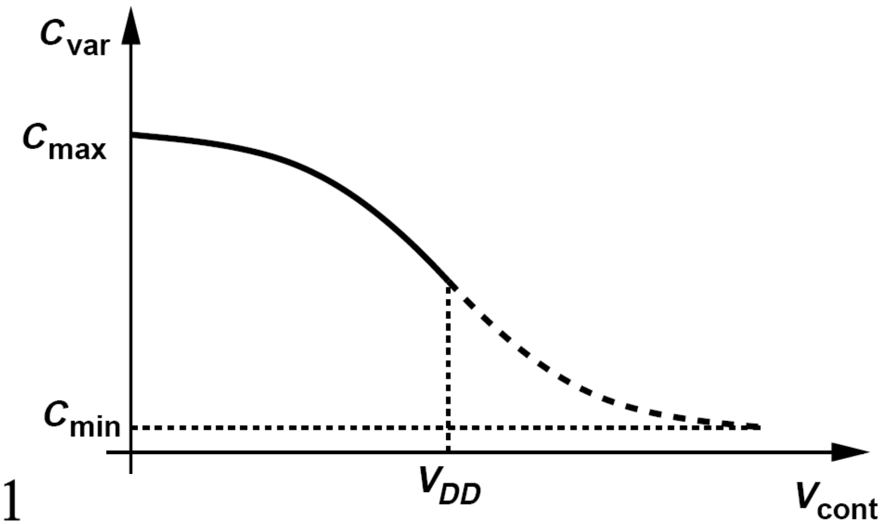
$$\omega_{out} = K_{VCO} V_{cont} + \omega_0$$

- The frequency varies from ω_1 to ω_2 (the required tuning range) as the control voltage, V_{cont}, goes from V_1 to V_2
- The slope, K_{VCO}, is called the "gain" or "sensitivity" of the VCO and expressed in rad/s/V.

VCO Using MOS Varactors

- Since it is difficult to vary the inductance electronically, we vary the capacitance by means of a varactor.
- MOS varactors are more commonly used than *pn* junctions, especially in low-voltage design.





$$\omega_{osc} = \frac{1}{\sqrt{L_1(C_1 + C_{var})}}$$

- First, the varactors are stressed for part of the period if V_{cont} is near ground and V_X (or V_Y) rises significantly above V_{DD}.
- Second, only about half of C_{max} - C_{min} is utilized in the tuning.

Varactors

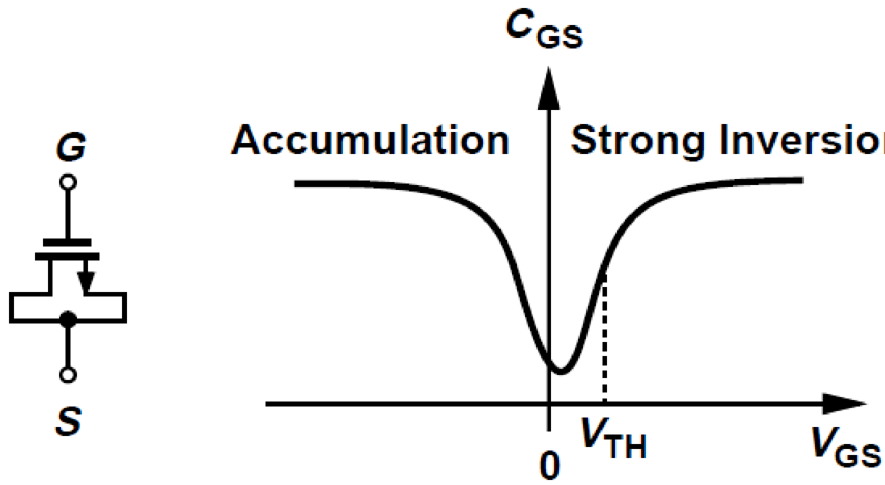
Varactor is a voltage-dependent capacitor.

Two important attributes of varactor design become critical in oscillator design

- **The capacitance range i.e. ratio of maximum to minimum capacitance that varactor can provide.**
- **The quality factor of the varactor.**

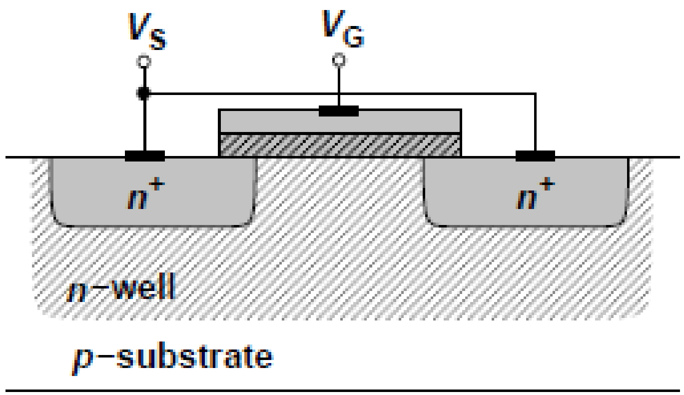
MOS Varactors

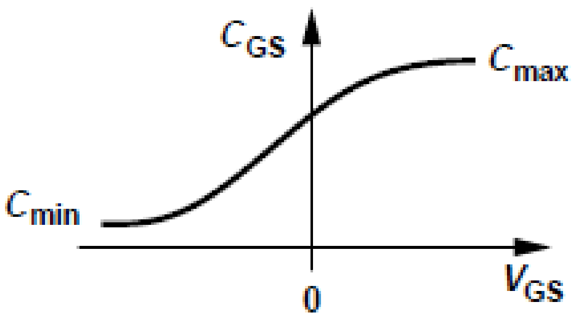
Regular MOS device:



Variation of gate capacitance with Vgs

Accumulation Mode MOS Varactor



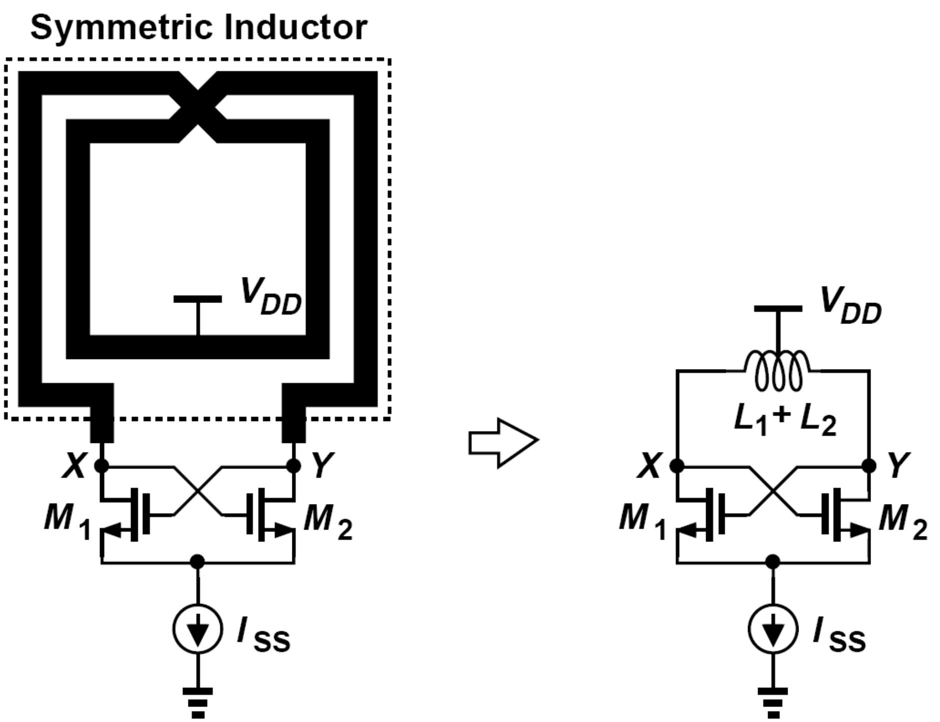


C/V characteristics of varactor

- Accumulation-mode MOS varactor is obtained by placing an NMOS inside an nwell .
- The variation of capacitance with Vgs is monotonic.
- The C/V characteristics scale well with scaling in technology.
- Unlike PN junction varactor this structure can operate with positive and negative bias so as to provide maximum tuning range.

Oscillator Using Symmetric Inductor

- **Symmetric spiral inductors excited by differential waveforms exhibit a higher *Q* than their single-ended counterparts.**



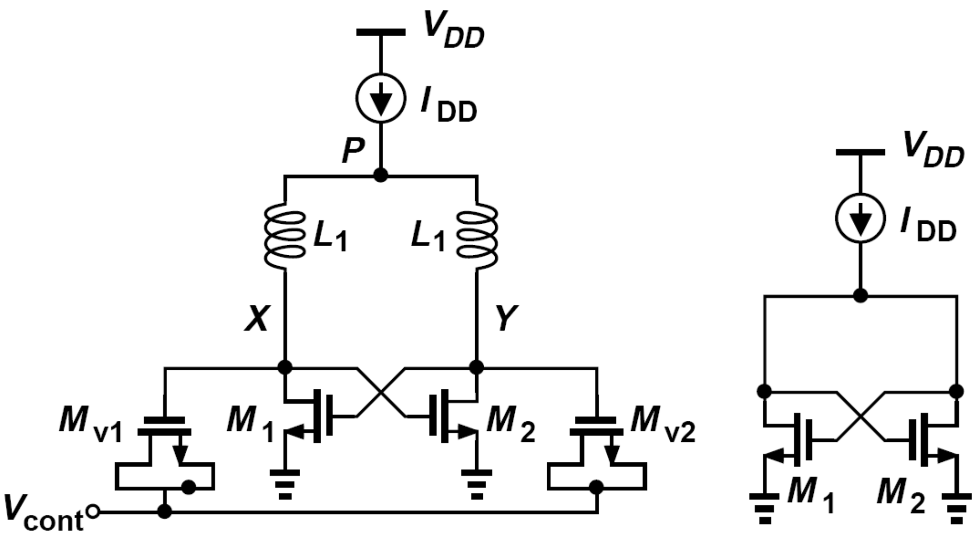
$L_1 = L_2 = 1$ nH
Q = 10 at 10 GHz

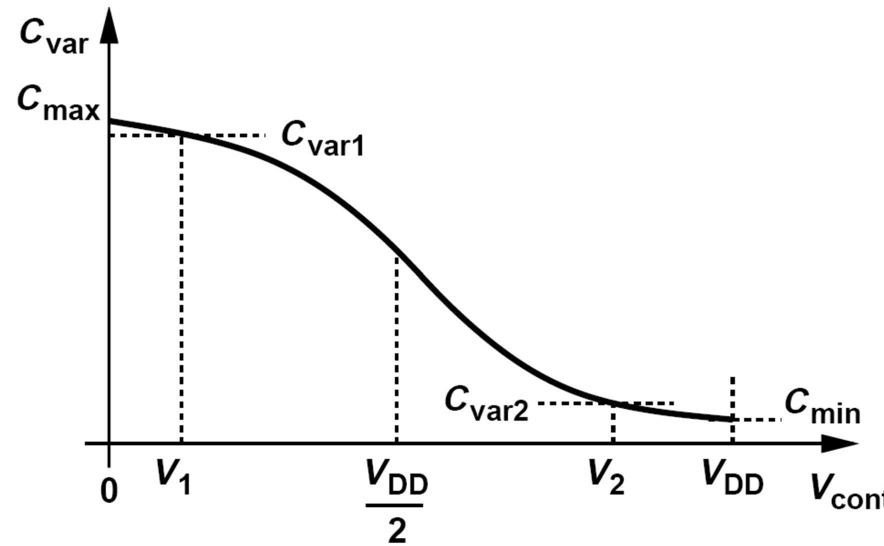
What is the minimum required transconductance of M_1 and M_2 to guarantee start-up?

$$g_{m1,2} \geq (630\ \Omega)^{-1}$$

LC VCOs with Wide Tuning Range: VCOs with Continuous Tuning

- We seek oscillator topologies that allow both positive and negative (average) voltages across the varactors, utilizing almost the entire range from C_{min} to C_{max}.





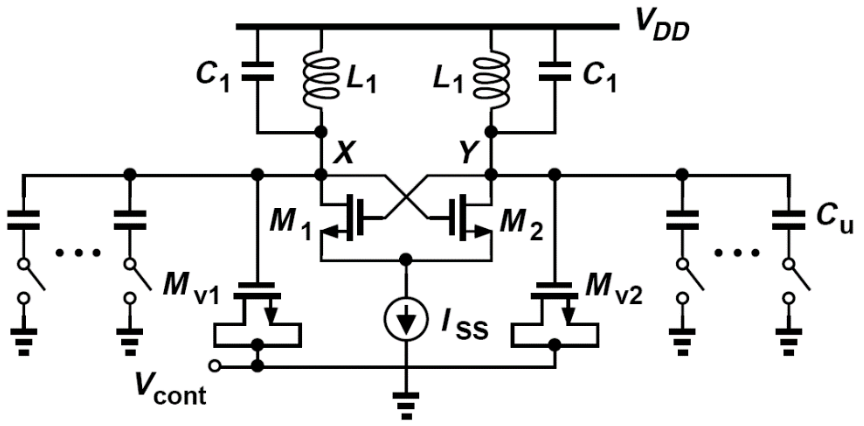
The CM level at X & Y:

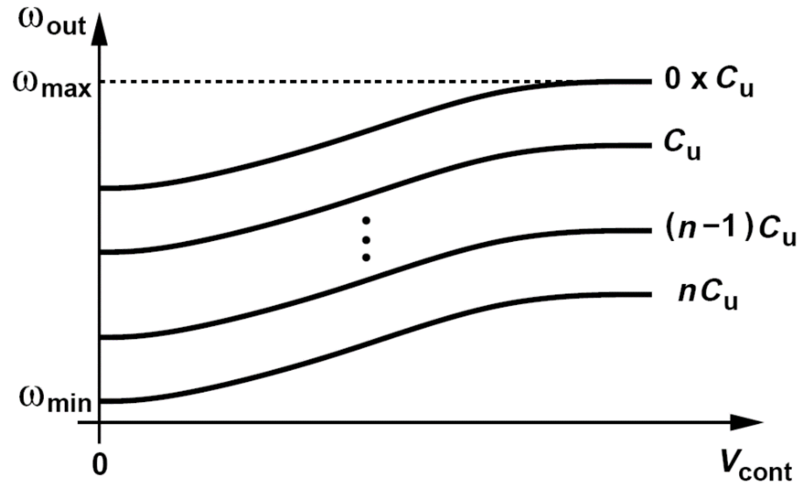
$$V_{GS1,2} = \sqrt{\frac{I_{DD}}{\mu_n C_{ox}(W/L)}} + V_{TH}$$

Select the transistor dimensions such that the CM level is approximately equal to $V_{DD}/2$.
As V_{cont} varies from 0 to V_{DD},
the gate-source voltage of the varactors, $V_{GS,var}$, goes from $+V_{DD}/2$ to $-V_{DD}/2$,

Discrete Tuning

- In applications where a substantially wider tuning range is necessary, "discrete tuning" may be added to the VCO so as to achieve a capacitance range well beyond C_{max}/C_{min} of varactors.

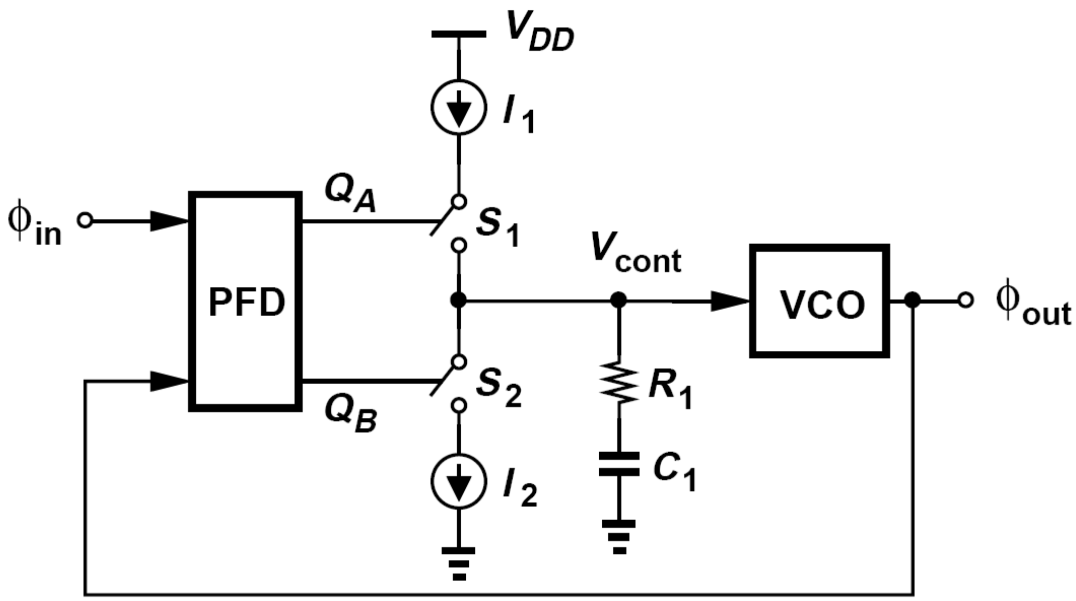




$$\omega_{min} = \frac{1}{\sqrt{L_1(C_1 + C_{max} + nC_u)}}$$

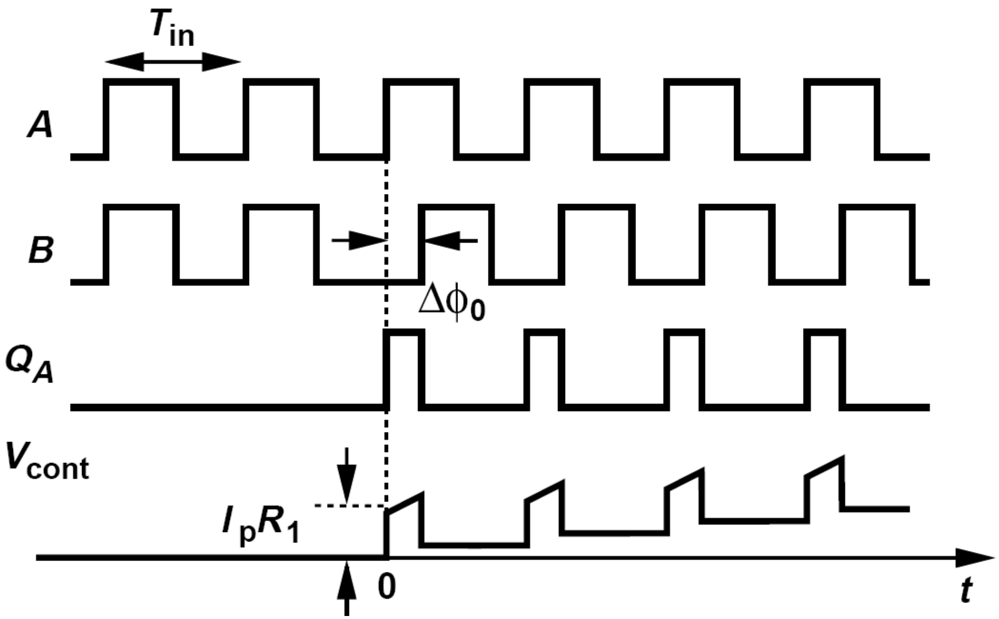
$$\omega_{max} = \frac{1}{\sqrt{L_1(C_1 + C_{min})}}$$

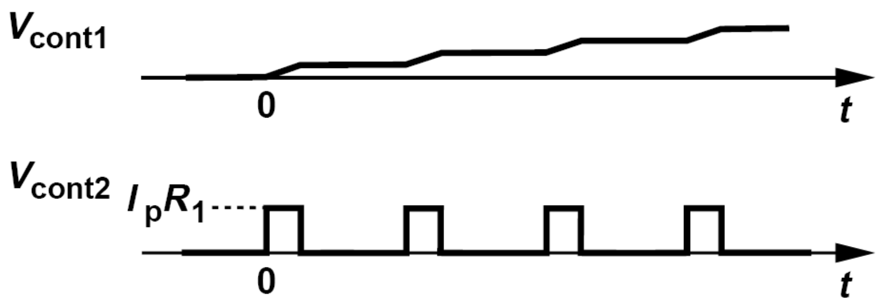
Charge-Pump PLL



- If one of the integrators becomes lossy, the system can be stabilized.
- This can be accomplished by inserting a resistor in series with C_1. The resulting circuit is called a "Charge Pump PLL" (CPPLL)

Computation of the Transfer Function





Approximate the pulse sequence by a step of height *(I_pR_1)[$\Delta\Phi_0$/(2π)]*:

$$V_{cont}(t) = \frac{\Delta\phi_0}{2\pi}\frac{I_p}{C_1}tu(t) + \frac{\Delta\phi_0}{2\pi}I_pR_1u(t)$$

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(\frac{1}{C_1 s} + R_1\right) \Rightarrow \boxed{H(s) = \frac{\frac{I_pK_{VCO}}{2\pi C_1}(R_1C_1s+1)}{s^2 + \frac{I_p}{2\pi}K_{VCO}R_1s + \frac{I_p}{2\pi C_1}K_{VCO}}}$$

Stability of Charge-Pump PLL

Write the denominator as $s^2 + 2\zeta\omega_n s + \omega_n 2$

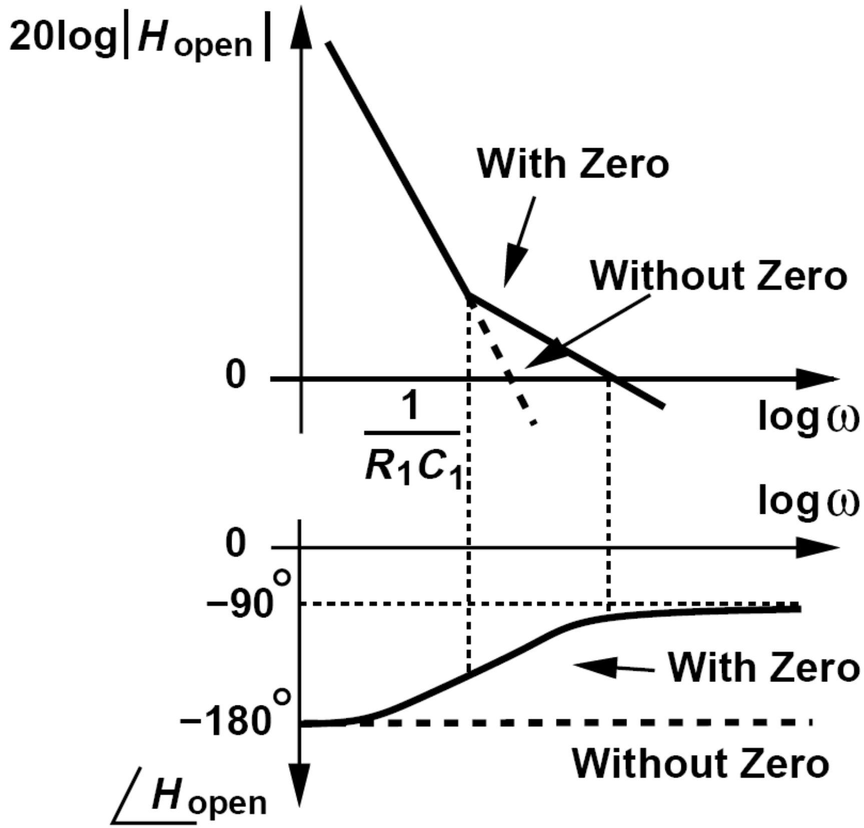
$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}}$$
$$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}}.$$

- As C_1 increases, so does ζ --- a trend opposite to that observed in type-I PLL
- No trade-off between stability and ripple amplitude

Closed-loop poles are given by

$$\omega_{p1,2} = [-\zeta \pm \sqrt{\zeta^2 - 1}]\omega_n$$

A closed-loop zero at $-\omega_n / 2\zeta$



$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(\frac{R_1 C_1 s + 1}{C_1 s}\right)$$

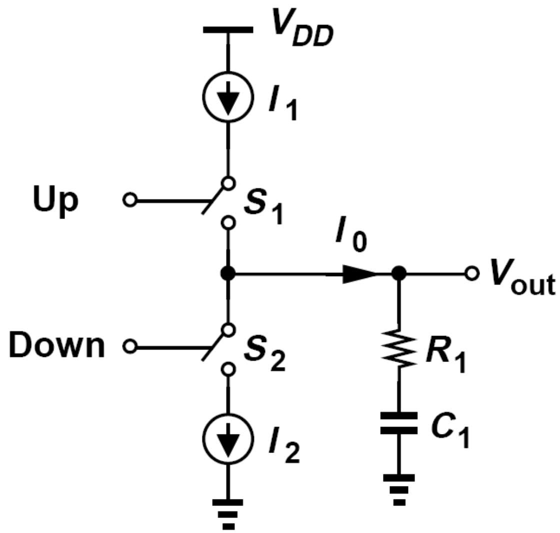
Frequency-Multiplying CPPLL

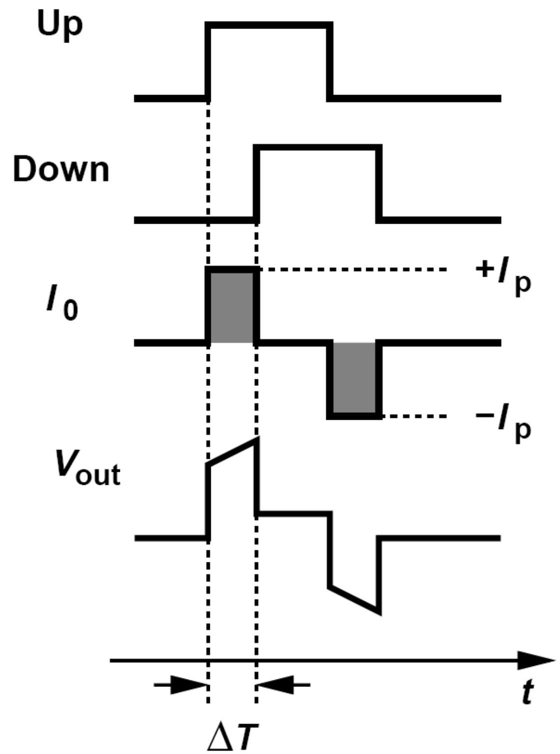
$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi}\frac{K_{VCO}}{M} R_1 s + \frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}}$$

$$\begin{aligned} \zeta &= \frac{R_1}{2}\sqrt{\frac{I_p C_1}{2\pi}\frac{K_{VCO}}{M}} \\ \omega_n &= \sqrt{\frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}}. \end{aligned}$$

Division of K_{VCO} by M makes the loop less stable, requiring that I_p and/or C_1 be larger.

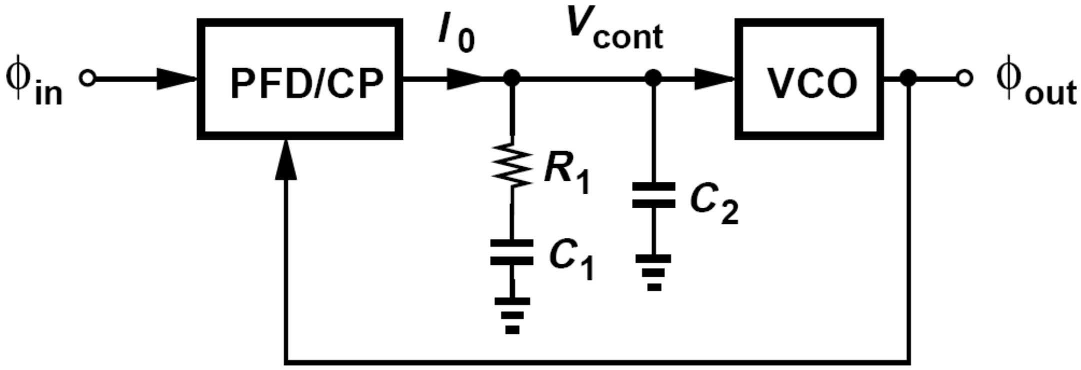
Higher-Order Loops: Drawback of Previous Loop Filter

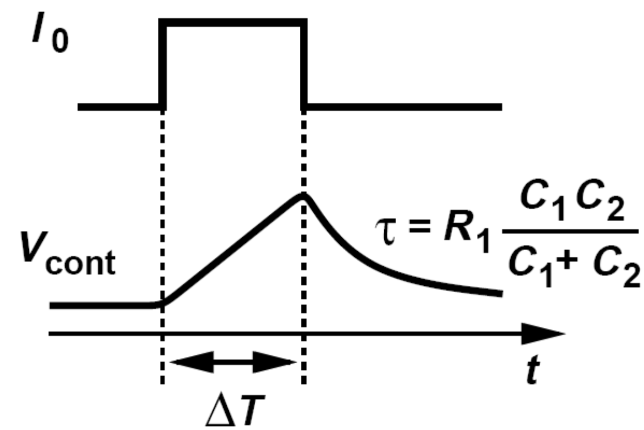




- The loop filter consisting of R_1 and C_1 proves inadequate because, even in the locked condition, it does not suppress the ripple sufficiently.
- The ripple consists of positive ad negative pulses of amplitude I_pR_1 occurring every T_{in} seconds.

Addition of Second Capacitor to Loop Filter





- Add C_2

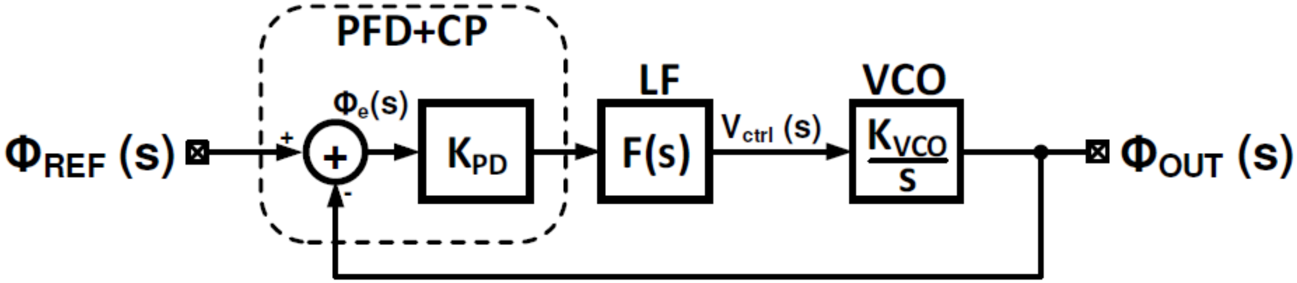
$$PM \approx \tan^{-1}(4\zeta^2) - \tan^{-1}\left(4\zeta^2 \frac{C_{eq}}{C_1}\right)$$

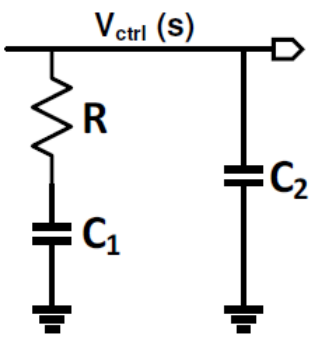
We therefore choose $\zeta = 0.8$ -1 and $C_2 \approx 0.1C_1$ in typical designs.

An upper bound derived for R_1 :

$$R_1^2 \leq \frac{2\pi}{I_p K_{VCO} C_{eq}}$$

Modeling of Charge-Pump PLL





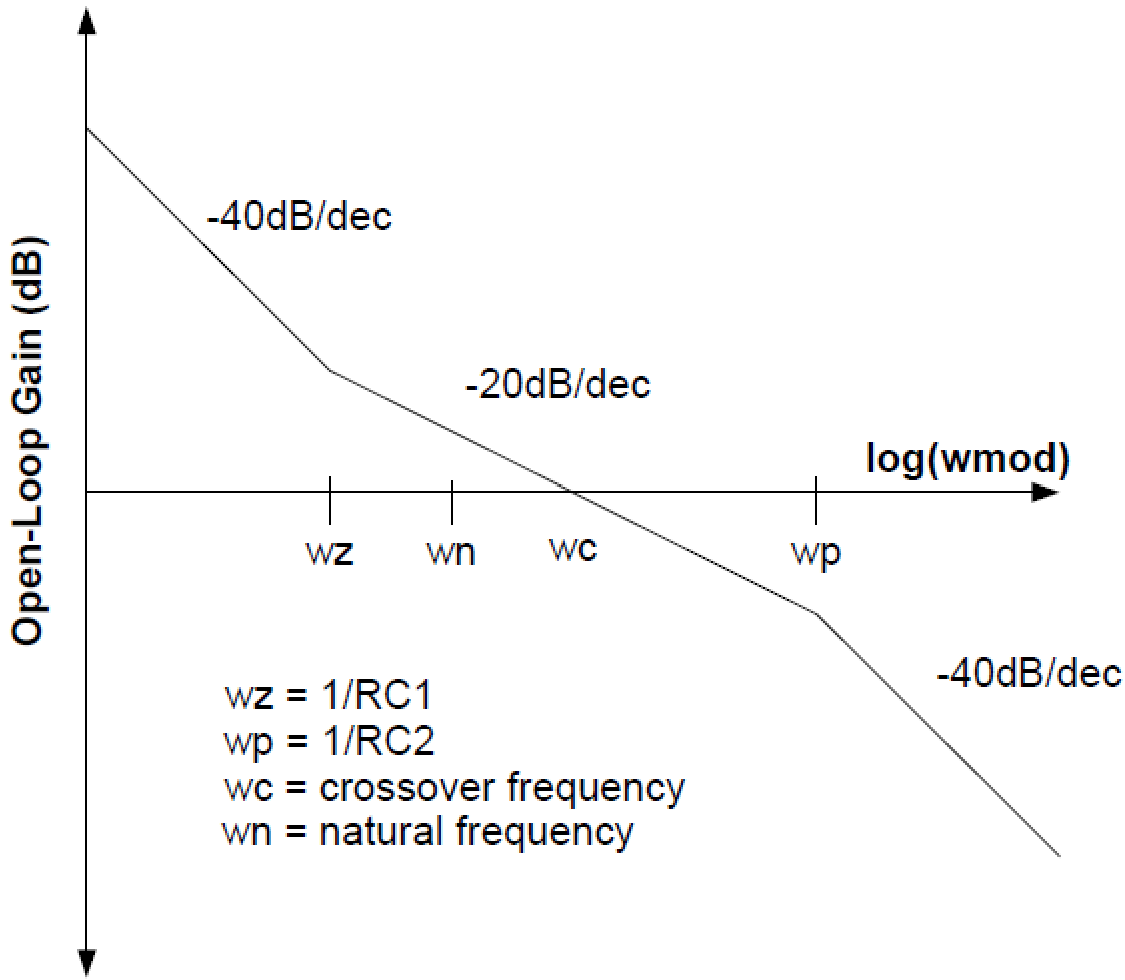
$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$

$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1 + C_2}{RC_1 C_2}\right)}$$

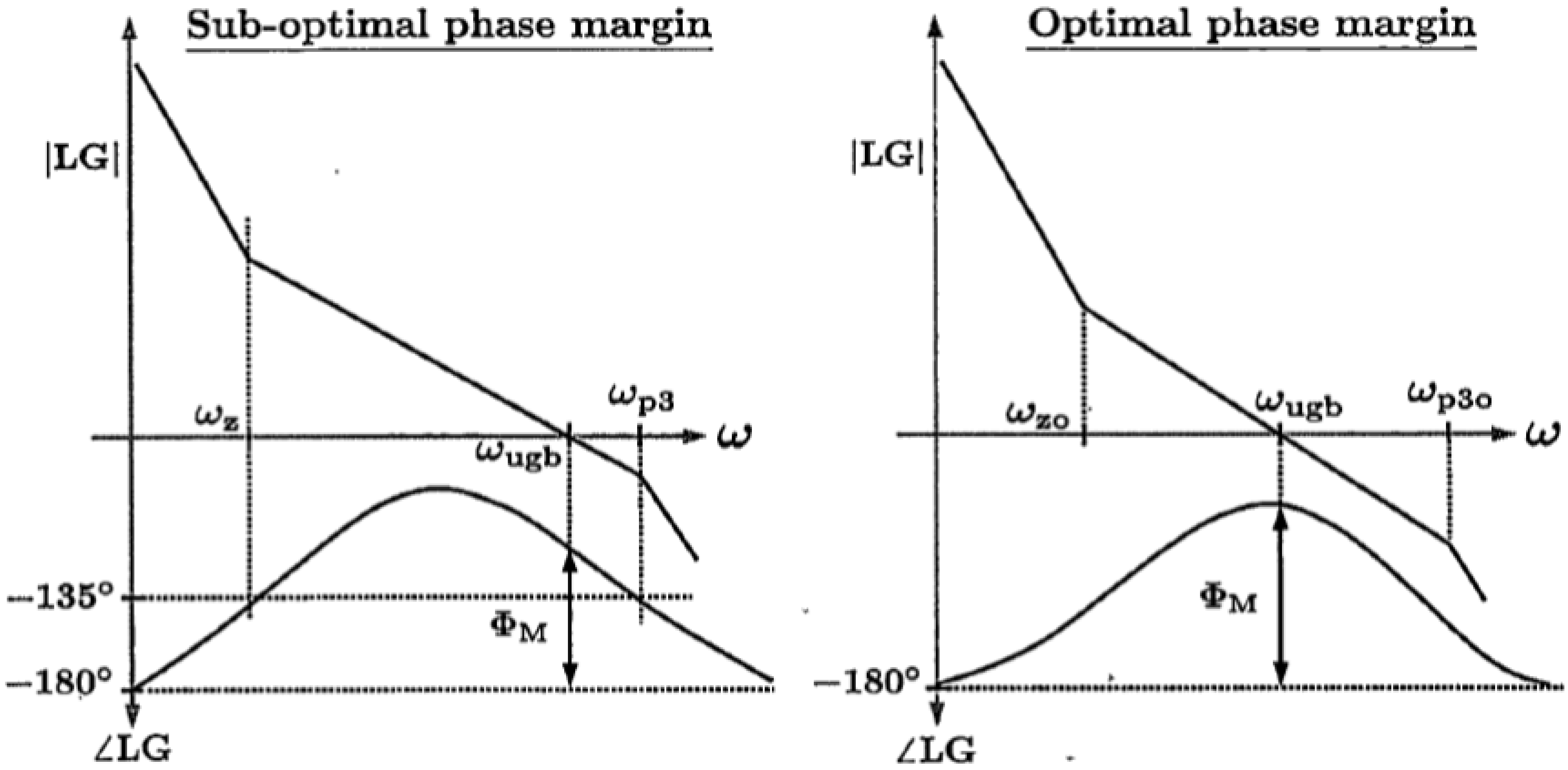
$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0;\ \omega_{p3} = \frac{C_1 + C_2}{RC_1 C_2}$$

$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right)$$

Open Loop Transfer Function



Loop Gain and Phase Margin



Linear Model of Charge-Pump PLL

$$LG(s) = K_{PD} \cdot F(s) \cdot \frac{K_{VCO}}{s}$$

$$= K_{PD} \cdot K_{VCO} \cdot \frac{s + \frac{1}{RC_1}}{C_2 s^2 \left(s + \frac{C_1+C_2}{RC_1C_2}\right)}$$

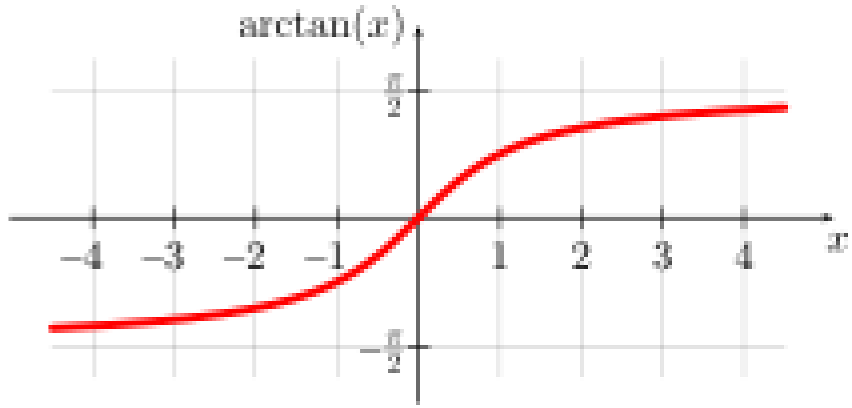
$$\omega_z = \frac{1}{RC_1};\ \omega_{p1} = \omega_{p2} = 0; \omega_{p3} = \frac{C_1 + C_2}{RC_1C_2}$$

$$\phi_M = \arctan\left(\frac{\omega_{ugb}}{\omega_z}\right) - \arctan\left(\frac{\omega_{ugb}}{\omega_{p3}}\right)$$

$$\omega_{ugb} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}$$

$$\phi_{M\_max} = \arctan(\sqrt{\frac{C_1}{C_2} + 1}) - \arctan(\frac{1}{\sqrt{\frac{C_1}{C_2} + 1}})$$

What is arctangent ?



If C_1/C_2 = 10, then Phase Margin is

arctan(sqrt(11)) = 73.2213451 degree — arctan(1 / sqrt(11)) = 16.7786549 degree = **57 degree**

Loop Filter Design Procedure

1. Choose desired bandwidth ω_{ugb}, phase margin ϕ_M and resistor R according to specification. Then calculate the K_c from Eq. 4.6:

$$K_c = \frac{C_1}{C_2} = 2(\tan^2(\phi_M) + \tan(\phi_M\sqrt{\tan^2(\phi_M) + 1})) \tag{4.6}$$

2. From Eq. 4.4 we have:

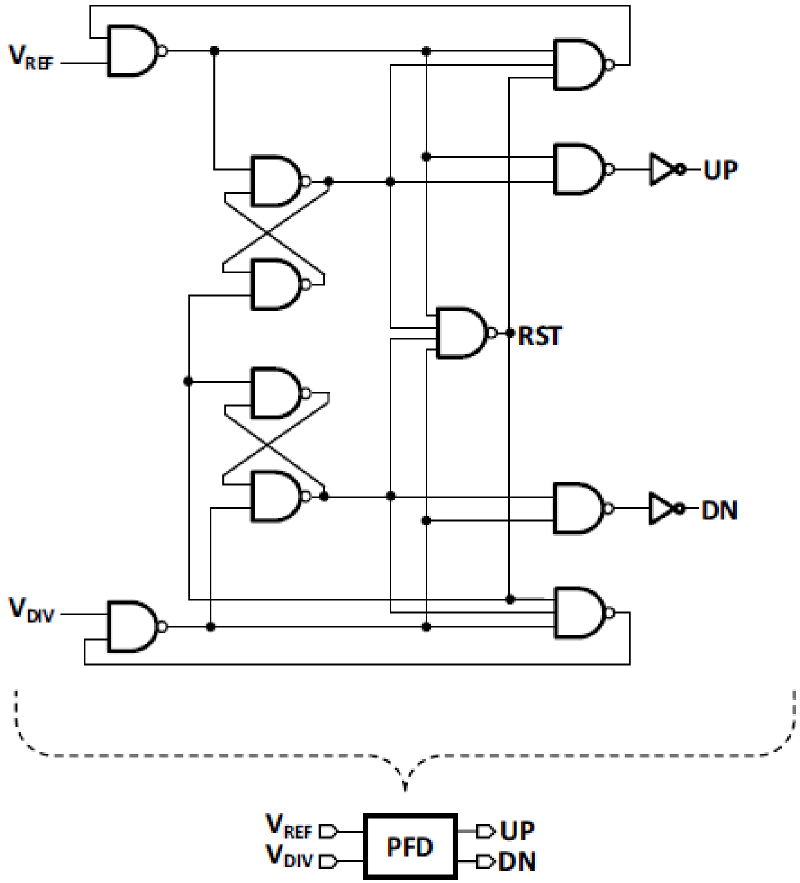
$$\omega_z = \frac{\omega_{ubg}}{\sqrt{\frac{C_1}{C_2} + 1}} \tag{4.7}$$

$$C_1 = \frac{1}{\omega_z R}; C_2 = \frac{C_1}{K_c}; \tag{4.8}$$

3. From aforementioned equations, we can determine the value for I_{CP}:

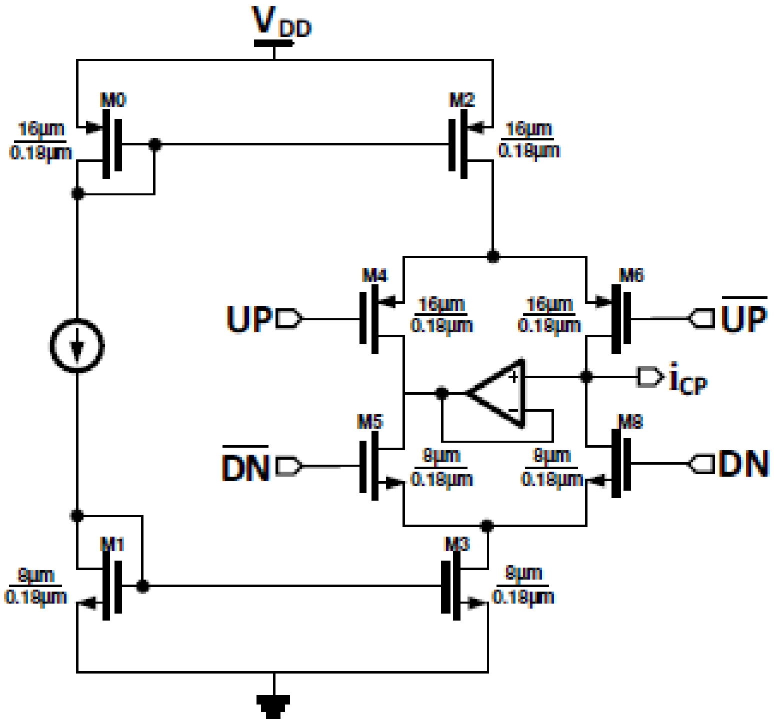
$$I_{CP} = \frac{2\pi C_2}{K_{VCO}} \cdot \omega_{ugb}^2 \cdot \sqrt{\frac{\omega_{p3}^2 + \omega_{ugb}^2}{\omega_z^2 + \omega_{ugb}^2}} \tag{4.9}$$

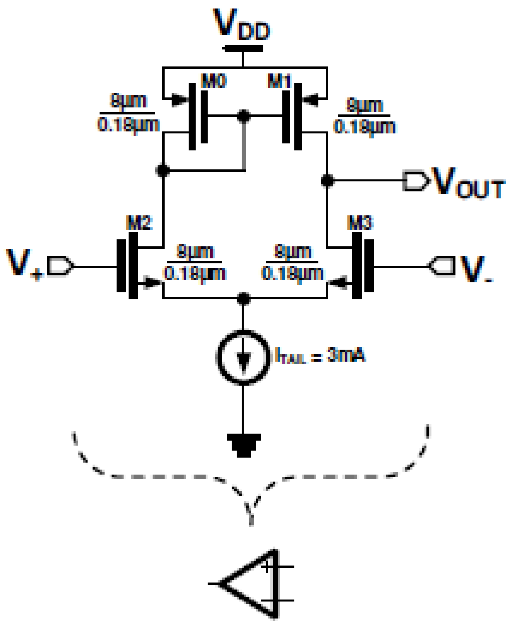
Example Circuit* - PFD



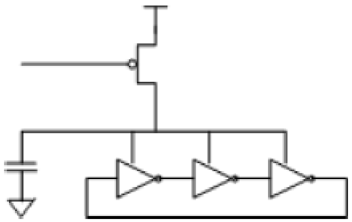
*Rishi Ratan, MS Thesis, UIUC, 2014

Example Circuit - CP

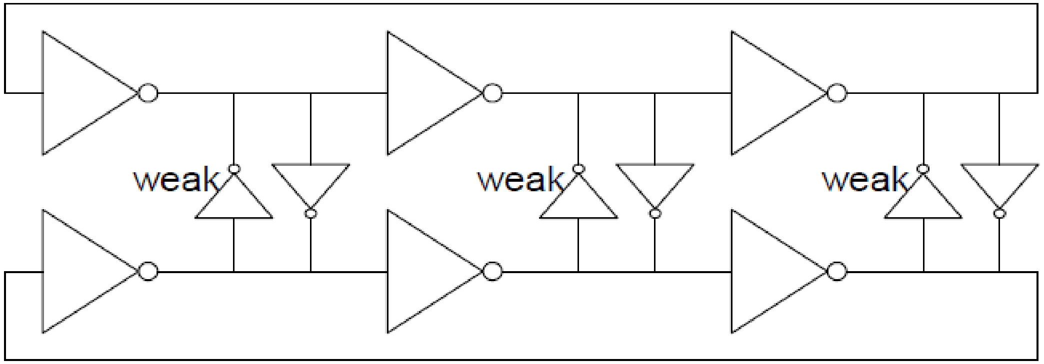




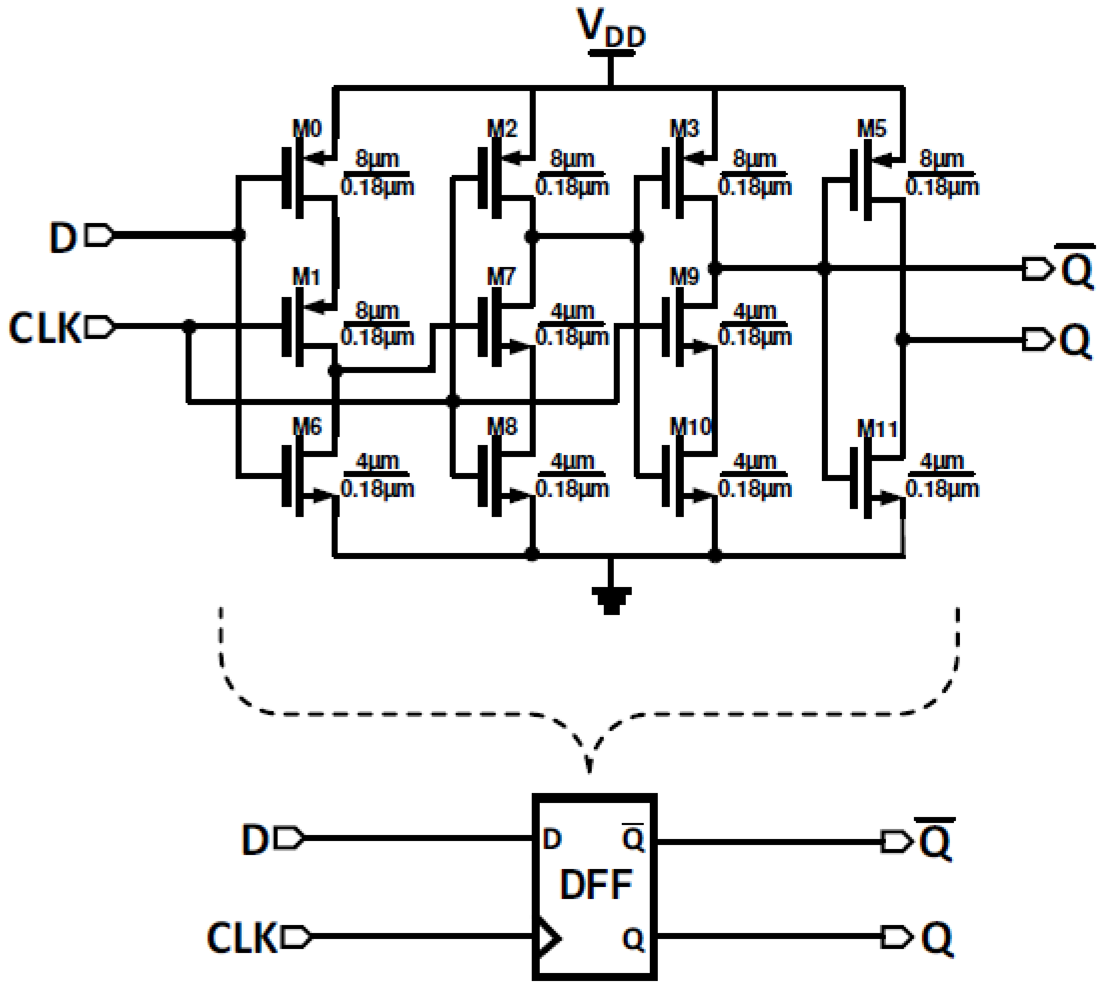
Example Circuit - VCO



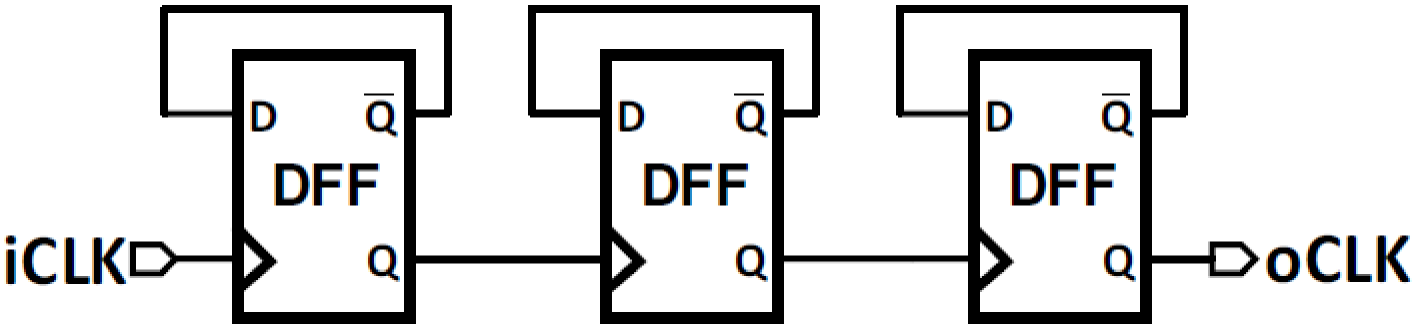
- RO VCO usually consists of two circuits
  - bias generator (e.g. V_{ctl} to I_{ctl})
  - voltage or current controlled ring oscillator (RO)
- Usually odd # of stages (usually 5+). Even # ok if differential RO
- Feedback INV → usually weaker by > ~3-4×
- Tune frequency by adjusting "VDD" of inverters – changes delay
- "Vdd" for inverters is regulated output of VCO V2I



Example Circuit – DFF Using TSPC

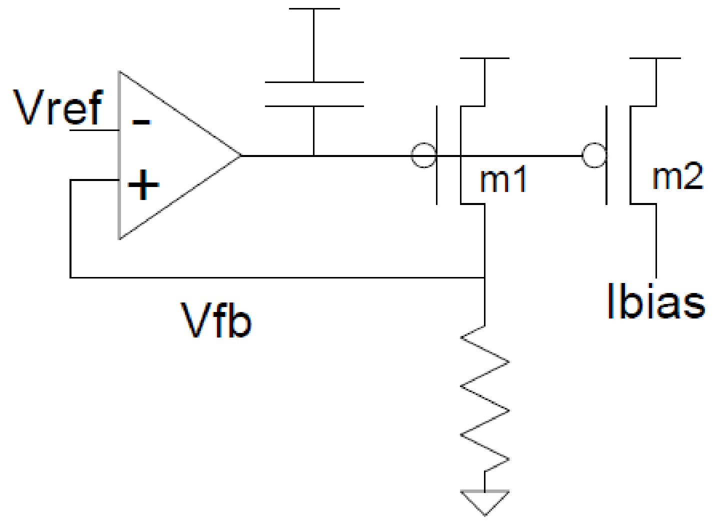


Example Circuit – Divider



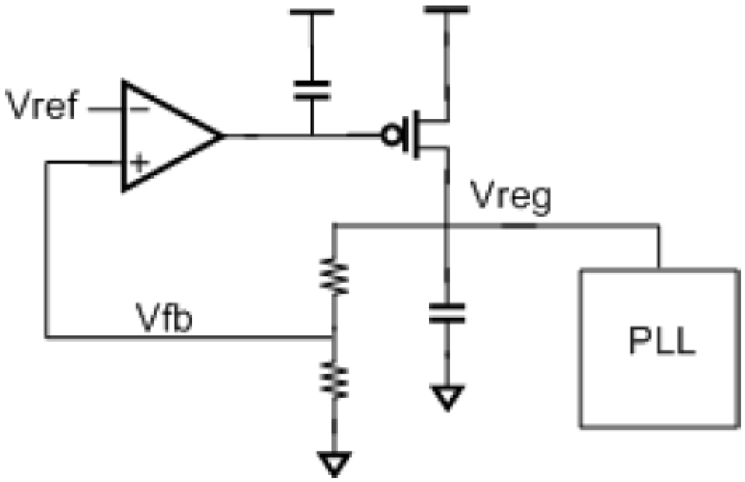
Example Circuit – Ibias

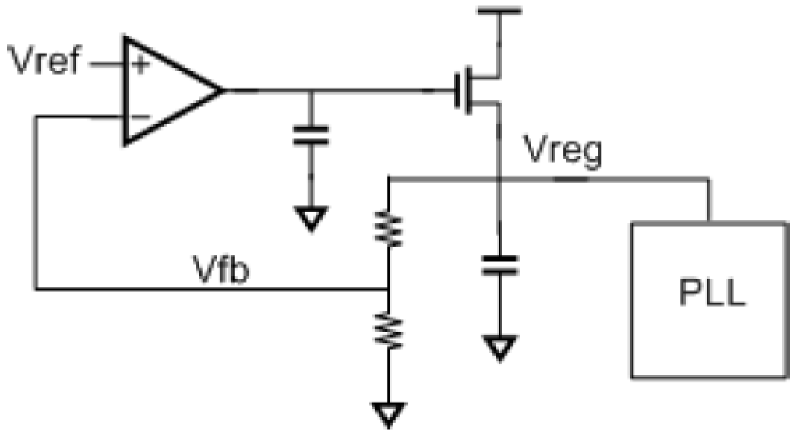
- $I_b \sim V_{ref} / R$
- V_{ref} generated from PVT-insensitive bandgap reference
- Con: feedback loop may oscillate
  - capacitor added to improve stability
  - resistor in series w/cap provides stabilizing zero *(not shown)*
- Pro: VDD-independent, mostly Temp independent
- Pro: Icp*Rlpf = constant → less PVT-sensitive loop dynamics



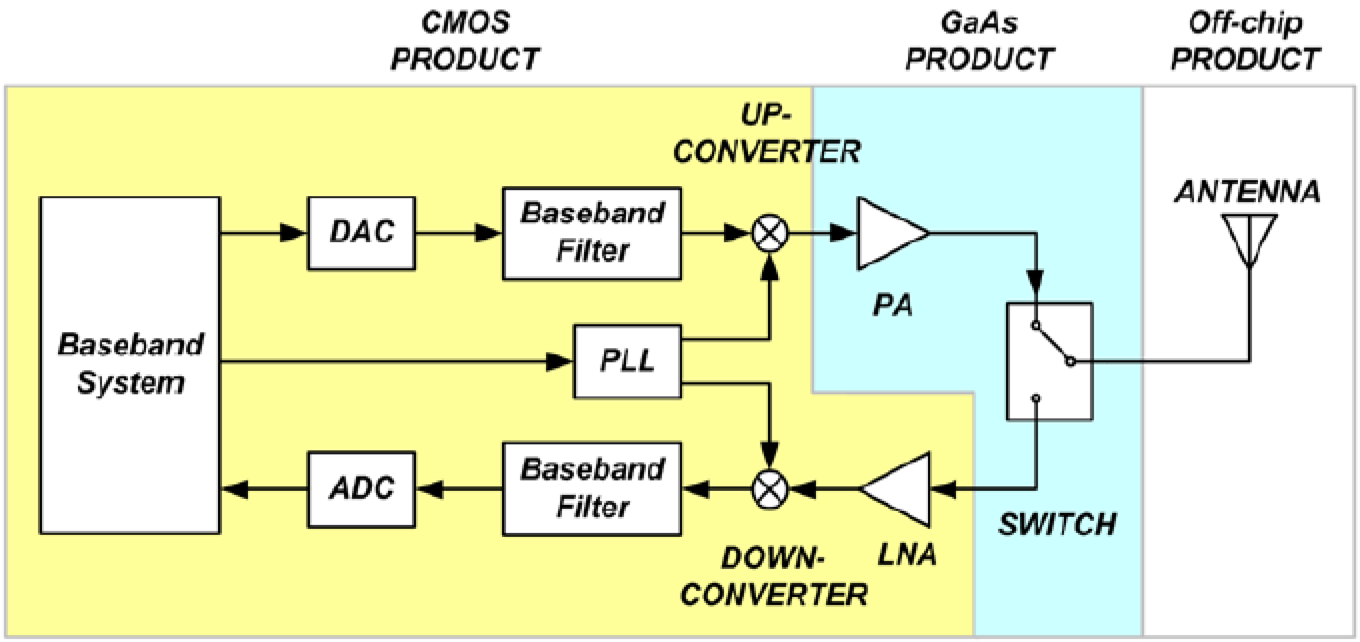
Example Circuit – Voltage Regulator

- Hard to stabilize over wide Iload and Cload ranges
- NMOS source-follower output stage
  - Requires more headroom
  - Faster response and easier to stabilize
- PMOS common-source output stage
  - Can handle larger current loads → larger Vgs





Block Diagram of Direct Conversion System



Power Amplifier Performance Metrics

- **Metrics defined in standards**
  - Output Power
  - Spectral Mask
  - ACPR (Adjacent Channel Power Ratio)
  - Signal Modulation

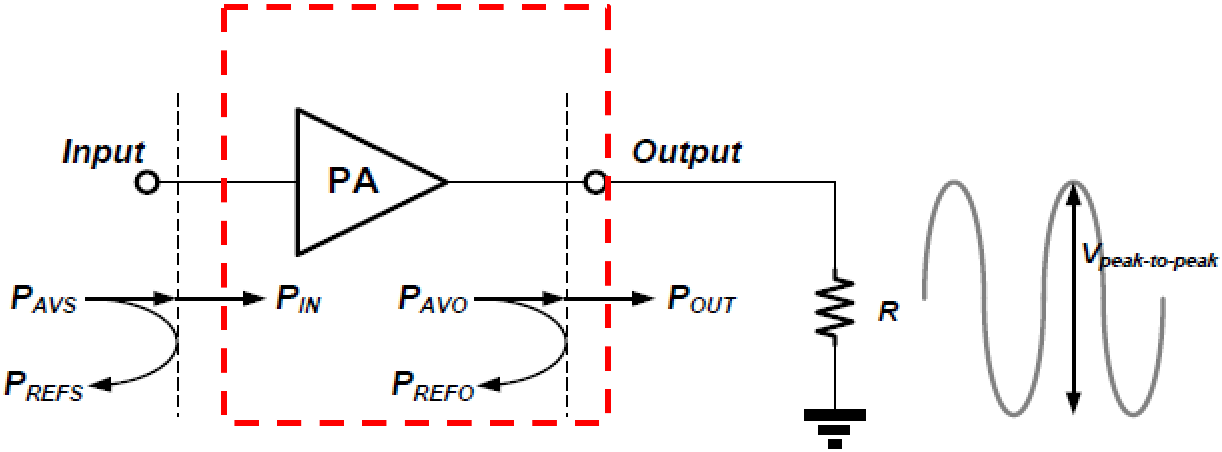
- **Metrics not defined in standards**
  - PAE (Power Added Efficiency)
  - Drain Efficiency
  - Power Gain
  - IP3
  - P1dB

Output Power

- Maximum output power varies drastically among different standards

Standard	Modulation	Max. P_{out}
AMPS	FM	31 dBm
GSM	GMSK	36 dBm
CDMA	O-QPSK	28 dBm
DECT	GFSK	27 dBm
PDC	$\pi/4$ DQPSK	30 dBm
Bluetooth	FSK	16 dBm
802.11a	OFDM	14-19 dBm
802.11b	PSK-CCK	16-20 dBm

Definition of Power and Gain



Transducer Gain (G_T) = P_{OUT} / P_{AVS}
Power Gain (G_P) = P_{OUT} / P_{IN}
Available Gain (G_A) = P_{AVO} / P_{AVS}

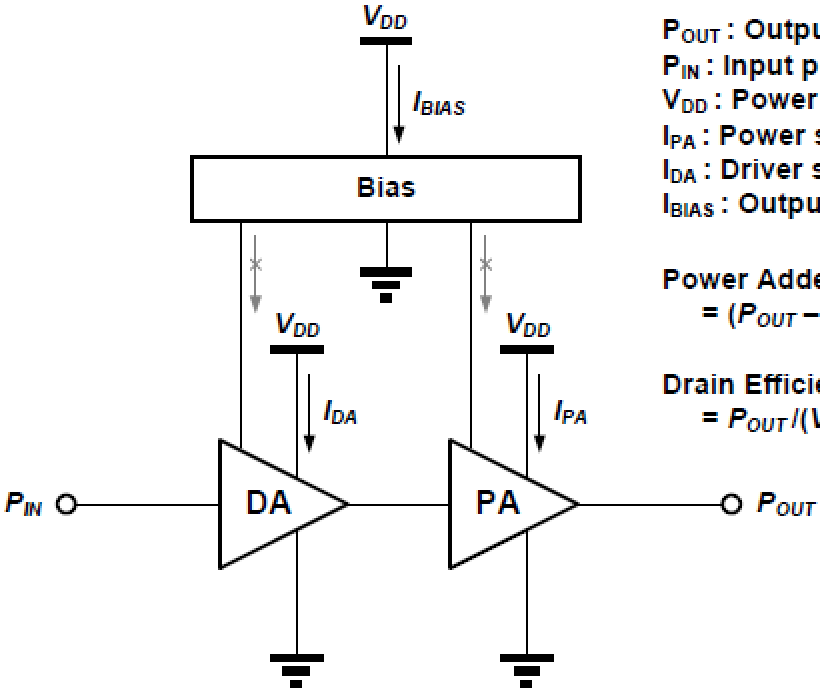
$$P_{OUT} = \frac{\left(\frac{V_{\text{peak-to-peak}}}{2}\right)^2}{2 \cdot R}$$

$$\text{Transducer Gain } (G_T) = \frac{P_{OUT}}{P_{AVS}},$$

$$\text{Power Gain } (G_P) = \frac{P_{OUT}}{P_{IN}} = G_T\left(1 + \frac{P_{REFS}}{P_{IN}}\right),$$

$$\text{Available Gain } (G_A) = \frac{P_{AVO}}{P_{AVS}} = G_T\left(1 + \frac{P_{REFO}}{P_{OUT}}\right)$$

Efficiency of PA



P_{OUT} : Output power
P_{IN} : Input power
V_{DD} : Power supply voltage
I_{PA} : Power stage current
I_{DA} : Driver stage current
I_{BIAS} : Output power

Power Added Efficiency (*PAE*)
= $(P_{OUT} - P_{IN})/(V_{DD} \times (I_{PA} + I_{DA} + I_{BIAS})) \times 100[\%]$

Drain Efficiency (η)
= $P_{OUT}/(V_{DD} \times I_{PA}) \times 100[\%]$

Drain Efficiency

$$\eta(DE) = \frac{P_{OUT}}{P_{DC}} = \frac{P_{OUT}}{P_{DC} \cdot I_{PA}}$$

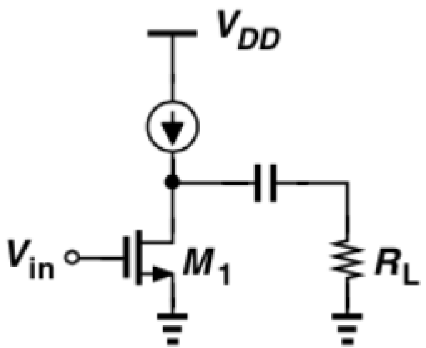
Power Added Efficiency

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}$$

Output Power and Voltage Swing

- Ex: 1 W (30 dBm) into a resistive 50 Ω load (e.g. antenna).

$$P = \frac{V_p^2}{2R_L}$$



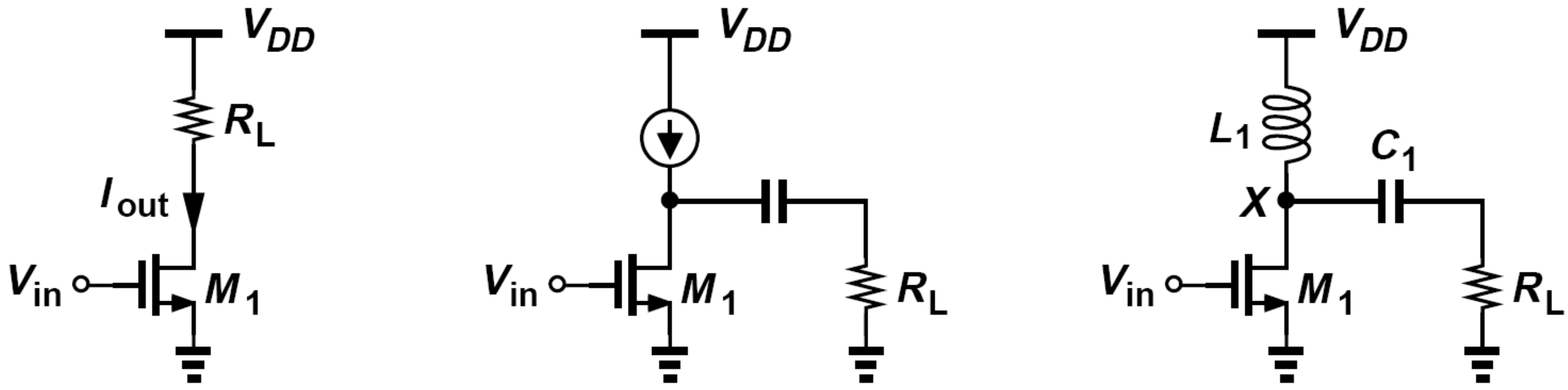
=> 10 V_p, I_p = 200 mA.

- How can we achieve this with nm-CMOS?

=> Impedance transformation: lower voltage, more current

- For high-power PAs: as high supply voltage as possible, and impedance transformation.

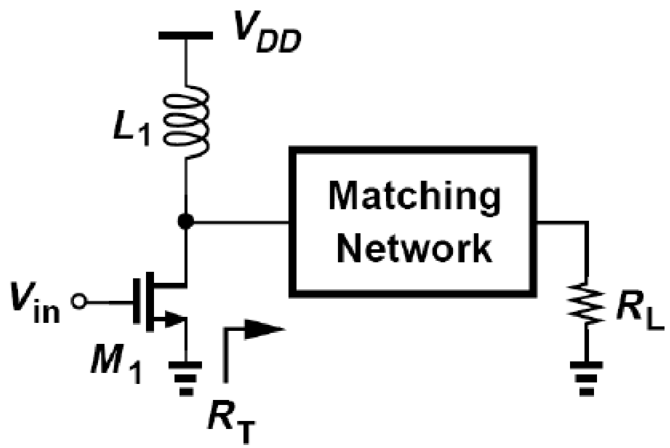
Output Power and Voltage Swing

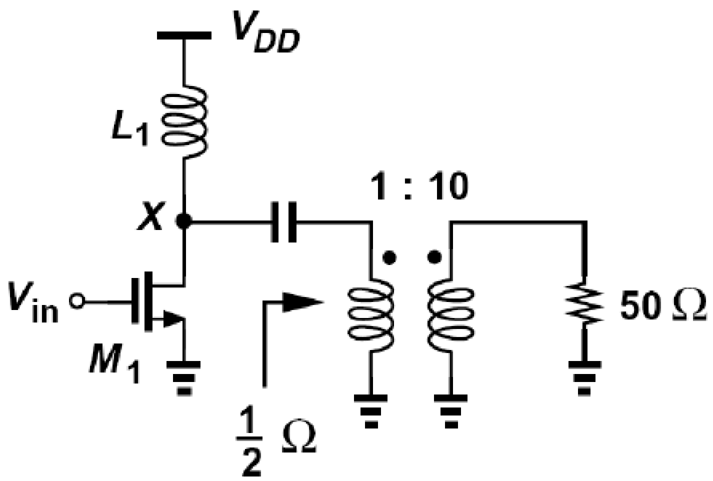


- For a common-source (or common-emitter) stage to drive the load directly, a supply voltage greater than V_{pp} is required.
- If the load is realized as an inductor, the drain ac voltage exceeds V_{DD}, even reaching $2V_{DD}$ (or higher). But the maximum drain-source voltage experienced by M_1 is still at least 20 V if the stage must deliver 1 W to a 50-Ω load.

Matching Network

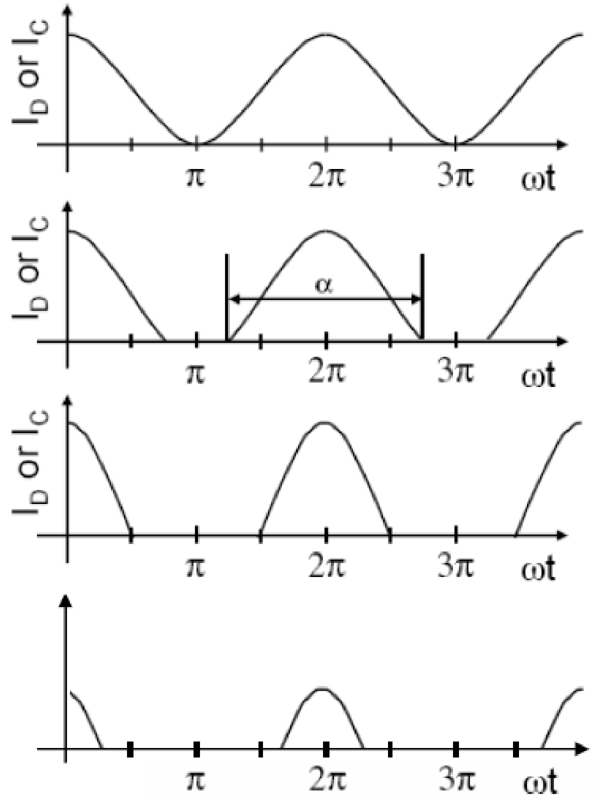
- In order to reduce the peak voltage experienced by the output transistor, a matching network is interposed between the PA and the load. This network transforms the load resistance to a lower value, R_T, so that smaller voltage swings still deliver the required power.





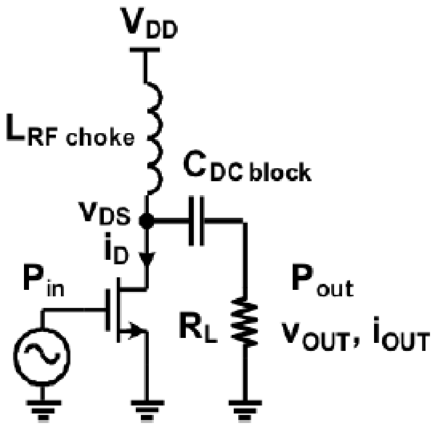
Linear PA Classes

Conduction Angle:

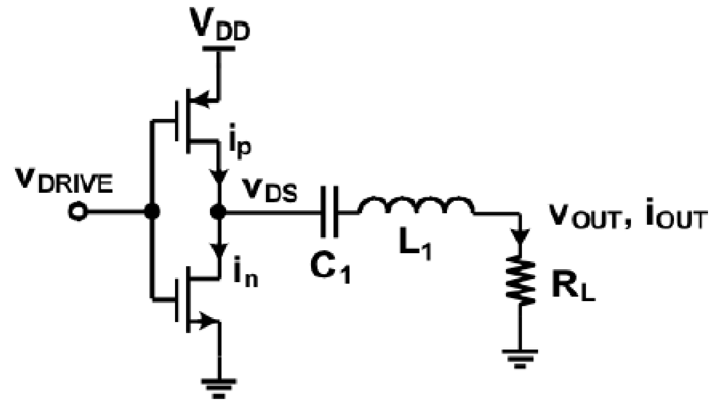


Class A:		$\alpha = 2\pi$
Class AB:		$\pi < \alpha < 2\pi$
Class B:		$\alpha = \pi$
Class C:		$\alpha < \pi$

PA Classes

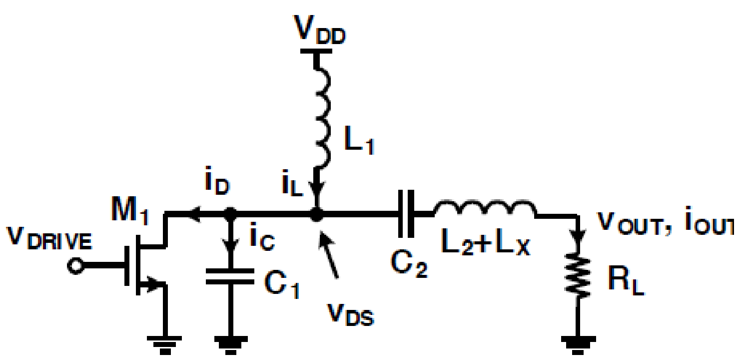


class-A/AB/B/C (linear)

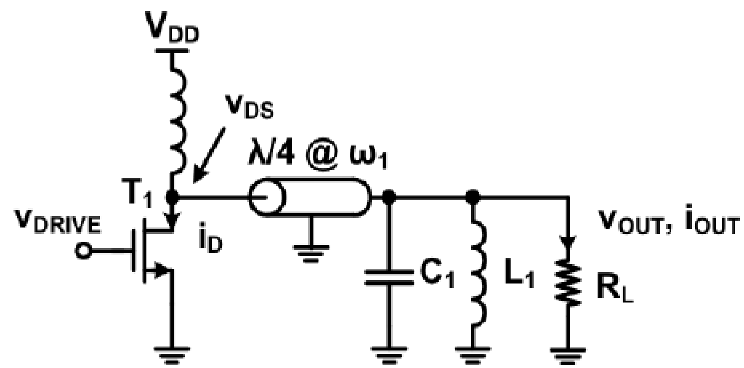


inverter-based class-D (switched)

class-E (switched)

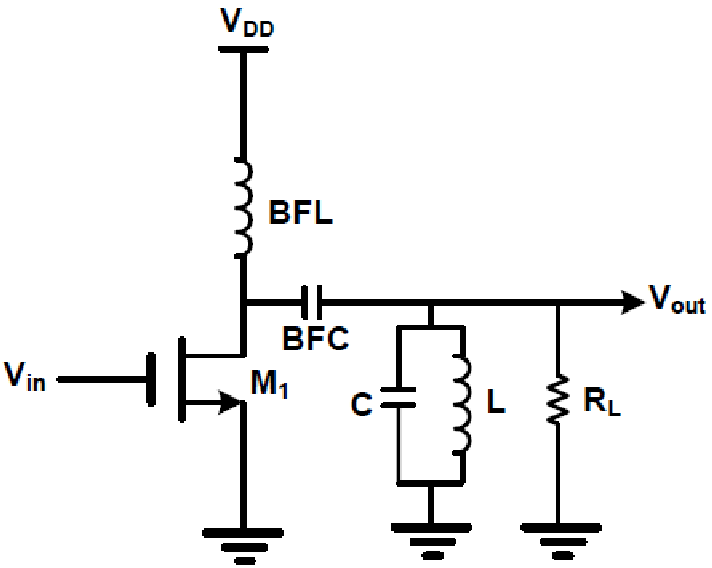


class-F (switched)



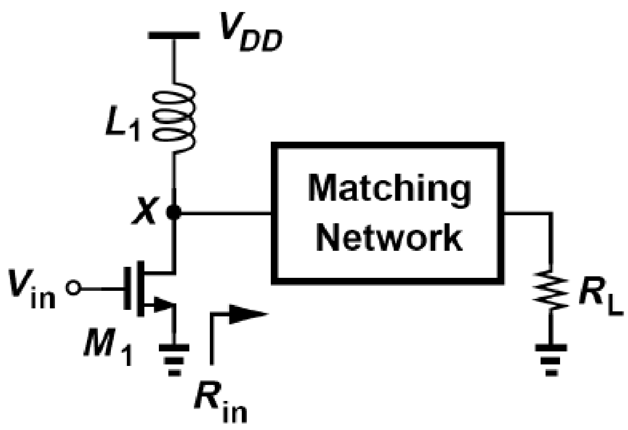
Linear PA Classes – A,B,C

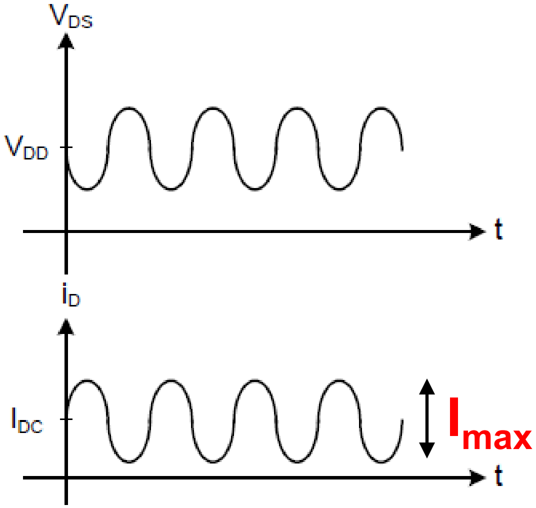
- Output power delivered to R_L.
- A "big fat" inductor (BFL) feeds DC power to the drain. It is big enough to create a constant current.
- BFC prevents DC dissipation in the load.
- The tank absorbs the parasitics of the transistor.
- LC tank filters out of band emissions created by non-linearities in the transistor.
- Different gate-biases => linear class A, AB, B, C.



Class A

- Since BFL presents a DC short, the drain voltage (which is the sum of DC and the signal voltage) has a symmetrical swing around V_{DD}.
- The drain voltage and current has a 180° phase difference.
- The product of drain current and voltage is positive; the transistor always dissipates power.



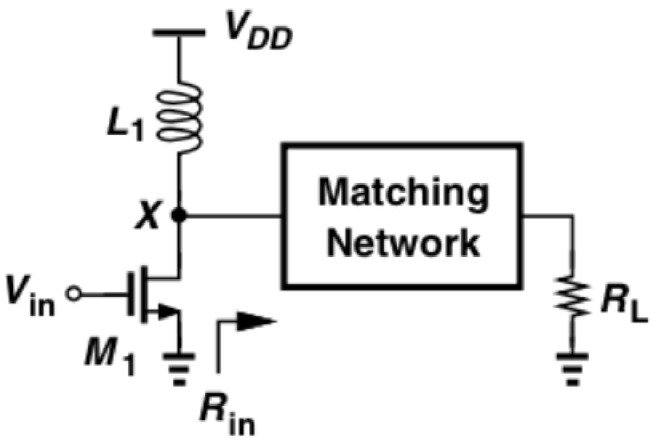


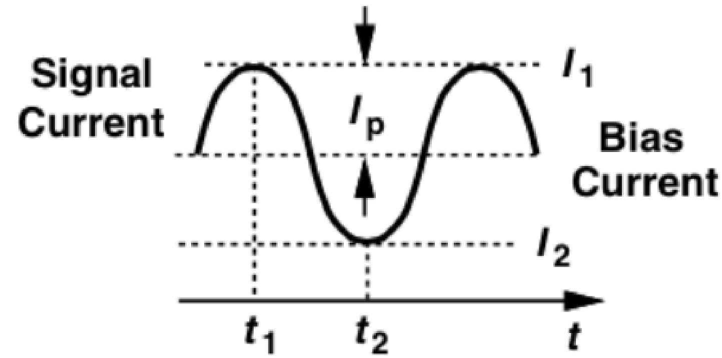
Class A

- Device biased to ~ $I_{max}/2$ to never switch off.
- Good linearity.
- Efficiency <= 50 %.
- V_x swings up to 2 x V_{DD} and the peak drain current is $2V_{DD}/R_L$. The device must be able to manage this stress!

$$\frac{I_{max}}{2} = \frac{V_{DD}}{R_L}$$

$$\begin{aligned} \eta &= \frac{V_{DD}^2/(2R_{in})}{V_{DD}^2/R_{in}} \\ &= 50\%. \end{aligned}$$





Efficiency of Class-A

$$\boxed{\eta = \frac{P_1}{P_{dc}} = \frac{I_{1,rms}.V_{1,rms}}{I_{dc}.V_{dc}}}$$

Class A: $\begin{cases} I_1 = \dfrac{I_{MAX}}{2},\ \ I_{dc} = \dfrac{I_{MAX}}{2} \\ \eta = \dfrac{\left(\dfrac{I_{MAX}/2}{\sqrt{2}}\right)\left(\dfrac{V_{DD}}{\sqrt{2}}\right)}{\left(\dfrac{I_{MAX}}{2}\right).V_{DD}} = 50\%\ \max. \end{cases}$