UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

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Wednesday, February 18, 2:10~3:30pm

PROBLEM 1 DC Analysis (10 points)

A world-renowned researcher in Berkeley has recently invented a three-terminal device. She named it "volristor" — it is basically a resistor whose resistance is controlled by a voltage applied to its third terminal. Schematic symbol and R-V characteristic are shown in Fig. 1. Please note the polarity of the voltage defined in Fig. 1 ($V_{AB} = V_A - V_B$).

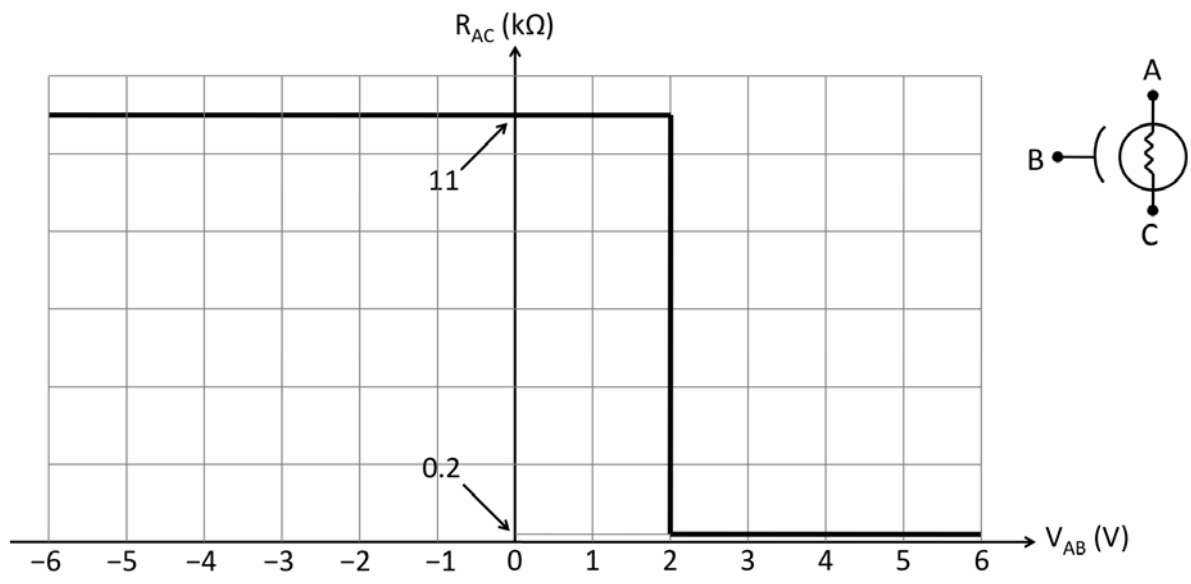


Figure 1 Schematic Symbol and R-V Characteristic of the New Device.

(1) One of last year's EE141 students played with the device and constructed a logic inverter as shown in Fig. 2. Sketch the voltage transfer characteristic (VTC) of this inverter in the space provided in Fig. 3. *(4 pts)*

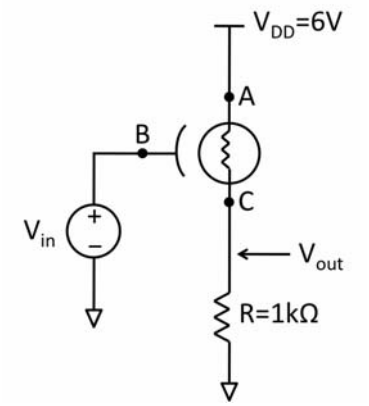


Figure 2 An Inverter that Employs the New Device.

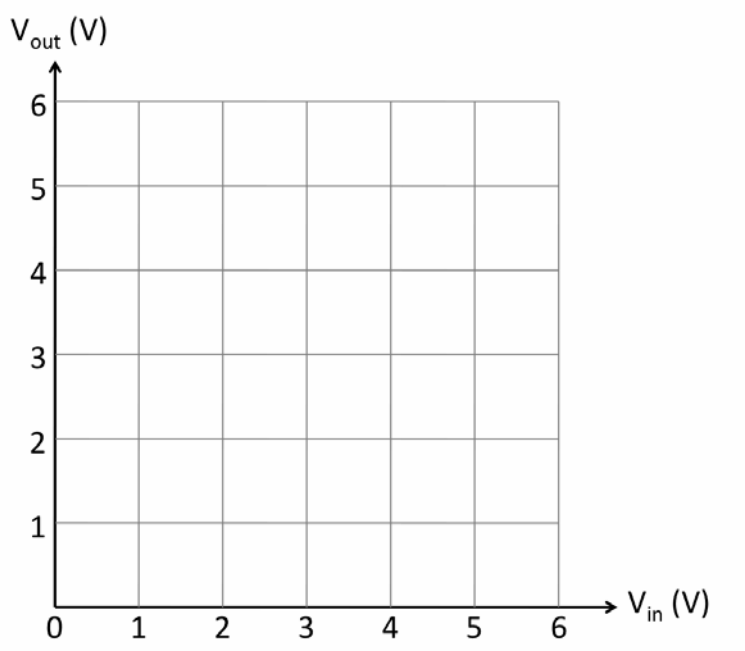


Figure 3 VTC of the Inverter in Fig. 2.

(2) Compute the noise margins (NM_H and NM_L) of the inverter in Fig. 2. *(3 pts)*

NM_H =
NM_L =

(3) You may have noted from the VTC plot that the inverter's threshold voltage V_M is away from $V_{DD}/2$. This is often undesirable for digital operations. To improve that, the EE141 student designed another inverter that incorporates a current source. Schematic of the new inverter is shown in Fig. 4. Amplitude of the current source I_S is 0.4mA. Design the value of the resistor R_X so that $V_M = V_{DD}/2$. *(3 pts)*

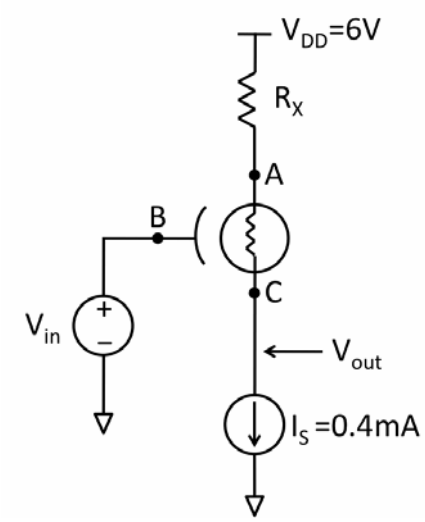


Figure 4 New Inverter Designed to Improve V_M.

SOLUTION

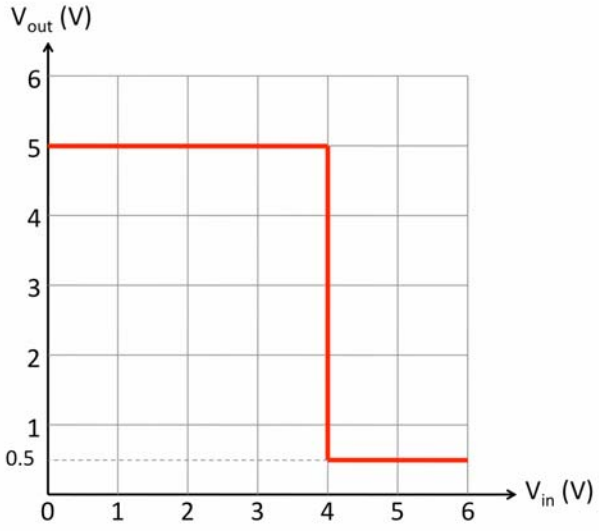
(1) When $0V \le V_{in} < 4V$, $2V < V_{AB} \le 6V$. $R_{AB}=0.2k\Omega$. V_{out} is divided down from V_{DD} by R_{AB} and the $1k\Omega$ load resistor

$$V_{out} = \frac{1}{1+0.2} \times 6V = 5V \quad \text{(1 pts)}$$

Similarly when $4V \le V_{in} \le 6V$, $0V \le V_{AB} \le 2V$. $R_{AB}=11k\Omega$.

$$V_{out} = \frac{1}{1+11} \times 6V = 0.5V \quad \text{(1 pts)}$$

VTC of the inverter is therefore



(2 pts)

(2) From the inverter's VTC,

$$V_{OH} = 5V \quad \text{(0.5 pts)}$$
$$V_{OL} = 0.5V \quad \text{(0.5 pts)}$$
$$V_{IH} = V_{IL} = 4V \quad \text{(1 pts)}$$

Therefore

$$NM_H = V_{OH} - V_{IH} = 1V \quad \text{(1 pts)}$$
$$NM_I = V_{IL} - V_{OL} = 3.5V \quad \text{(1 pts)}$$

(3) V_M is the switch threshold at which the inverter's output reverses polarity. According to the R-V characteristic in Fig. 1, $V_{AB}=2V$ at when $V_{in}=V_M$. Therefore

$$V_{AB} = V_A - V_B = \left(V_{DD} - I_S \times R_X\right) - V_{in} = \left(V_{DD} - I_S \times R_X\right) - V_M \quad \text{(2 pts)}$$

Equivalently

$$2V = \left(6V - 0.4mA \times R_X\right) - 3V$$
$$R_X = 2.5k\Omega \quad \text{(1pts)}$$

PROBLEM 2 – Logical Effort (15 Points)
Given the complex gate below:

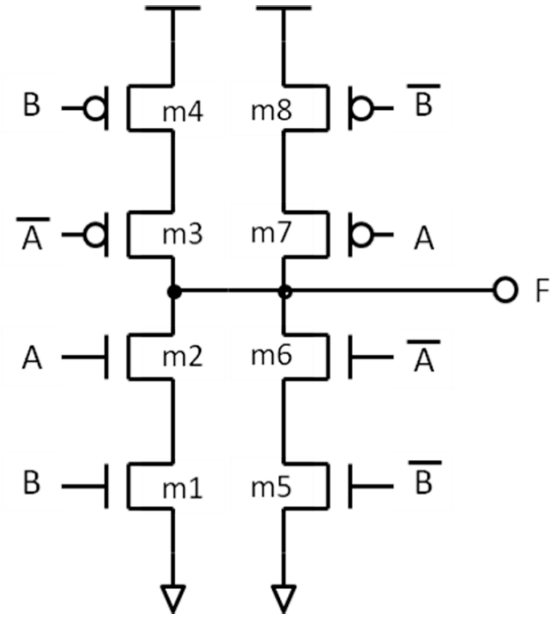


Figure 1 Complex gate.

(1) Draw the truth table and determine the logic function of the complex gate shown in Fig. 1. *(1 pt)*

F =

(2) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What is logical effort of this gate for each input (A, $\overline{A}$, B, $\overline{B}$)? *(3 pts)*

m1=m2= m5=m6=

m3=m4= m7=m8=

LE_A=

LE_B=

$LE_{\bar{A}}$=

$LE_{\bar{B}}$=

(3) Suppose we are only interested in the delay of the falling output transition **when both input A and input B are pulled high**. Size the transistor m1 and m2 to make the logical effort of this gate for the input A the same as a unit inverter. For transistors m3-m8, use the sizes you found in (2). (Use m3=m4…=m8=2 if you do not know the answer to part (2)) *(1 pt)*

m1=m2=

(4) Suppose we are only interested in the delay of the falling output transition **when both input A and input B are pulled high**. Assume we can arbitrarily choose the size of any transistor in this gate and the **only sizing constraint is m1=m2**. What are the maximum and minimum logical efforts we can achieve for the input A? *(2 pts)*

Max LE_A=
Min LE_A=

The designer finally settles on the relative transistor sizing shown in Fig. 2a (that is, all transistors are equal). This gate is used in the complex logic network shown in Fig. 2b (Really complex…☺). Assume the initial input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) equals (L, H, H, L), where L means logical low and H means logical high.

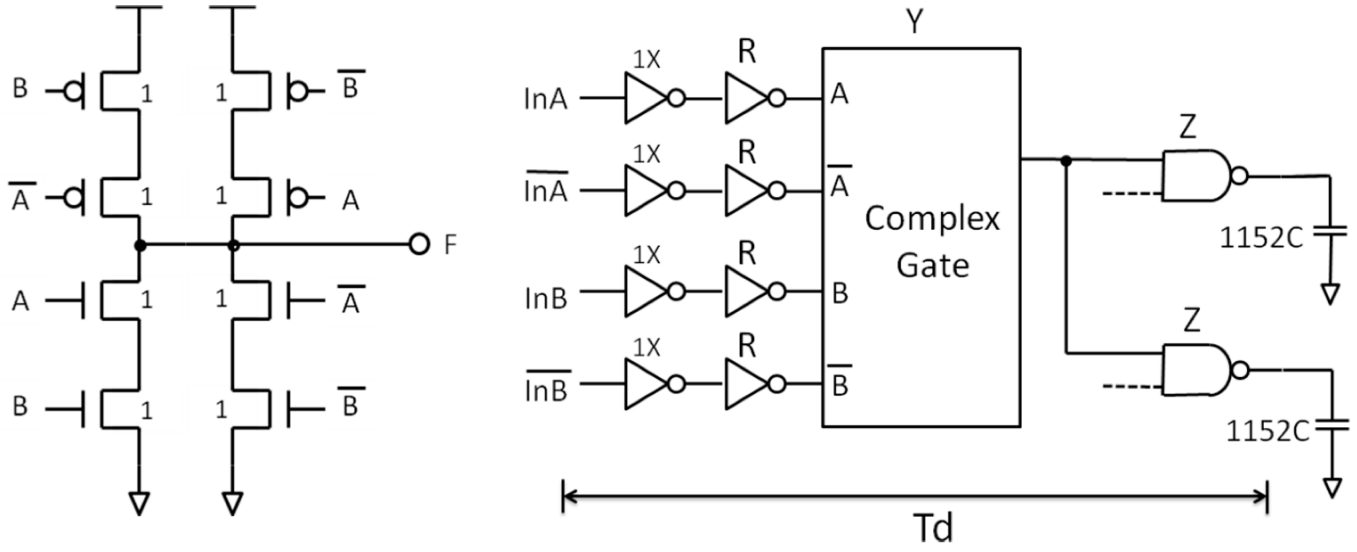


Figure 2: (a) Finalized transistor sizing; (b) Complex logic network.

(5) Size the inverter R, the complex gate Y, and the NAND Z to minimize the propagation delay Td_{11} from input to output when the input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) switches from (L, H, H, L) to (H, L, H, L). *(5 pts)*

R=

Y=

Z=

(6) Using the transistor sizes you found in (5), calculate the delay Td_{11}, and the propagation delay Td_{01} from input to output when the input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) switches from (H, L, H, L) back to (L, H, H, L). Assume $\gamma = 1$. *(3 pts)*

$Td_{11} = t_{p0}$

$Td_{01} = t_{p0}$

SOLUTION:

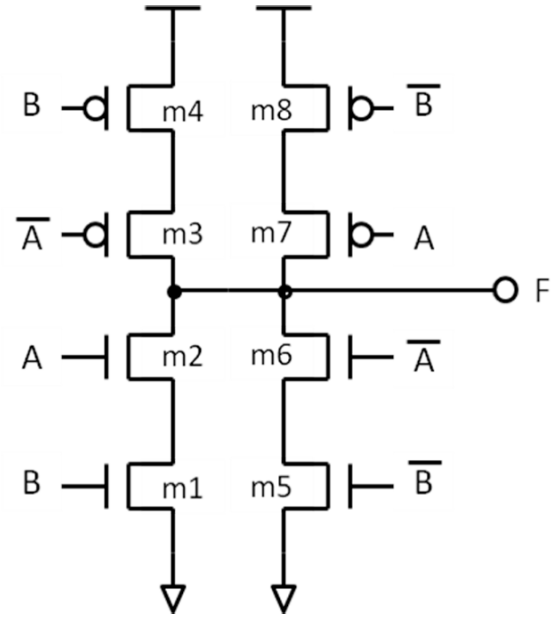


Figure 1 Complex gate.

(1) Draw the true table and determine the logic function of the complex gate shown in Fig. 1. (1 pt)

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

(0.5 pt)
This is an XOR gate. (0.5 pt)

(2) Size the transistors such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What is logical effort of this gate for each input (A, $\overline{A}$, B, $\overline{B}$)? (3 pts)

m1=m2=m5=m6=2 (0.5 pt)

m3=m4=m7=m8=4 (0.5 pt)

$LE_A = (2+4)/3 = 2$ (0.5 pt)

$LE_B = (2+4)/3 = 2$ (0.5 pt)

$LE_{\overline{A}} = (2+4)/3 = 2$ (0.5 pt)

$LE_{\overline{B}} = (2+4)/3 = 2$ (0.5 pt)

(3) Suppose we are only interested in the delay of the falling output transition **when both input A and input B are pulled high**. Size the transistor m1 and m2 to make the logical effort of this gate for the input A the same as a unit inverter. For the transistor m3-m8, use the same transistor size you find in (2). (Use m3=m4…=m8=2 if you do not know the answer in part (2)) (1 pt)

$$LE_A = \left(\frac{\frac{(4+m2)}{\frac{m2}{2}}}{3} \right) = 1 \quad \text{(0.5 pt)}$$

$$\Rightarrow m2 = 8$$

m1=m2=8 (0.5 pt)

(4) Suppose we are only interested in the delay of the falling output transition **when both input A and input B are pulled high**. Assume we can arbitrarily choose the size of any transistor in this gate and the **only sizing constraint is m1=m2**. What are the maximum and minimum logical efforts we can achieve for the input A? (2.5 pts)

$$LE_A = \left(\frac{\frac{(m7+m2)}{\frac{m2}{2}}}{3} \right) \quad \text{(0.5 pt)}$$

Choose $m7 >> m2$, if $m7 \to \infty \Rightarrow LE_A \to \infty$ (0.5 pt)

Choose $m2 >> m7$, if $m2 \to \infty \Rightarrow LE_A \to 2/3$ (0.5 pt)

Max $LE_A = \infty$ (0.5 pt)

Min $LE_A = 2/3$ (0.5 pt)

The designer finally decides the relative transistor sizing of this complex gate, as shown in Fig. 2. This complex gate is used in a complex logic network shown in Fig. 3 (Really complex…☺). Assume the initial input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) is equal to (L, H, H, L), where L means logical low and H means logical high.

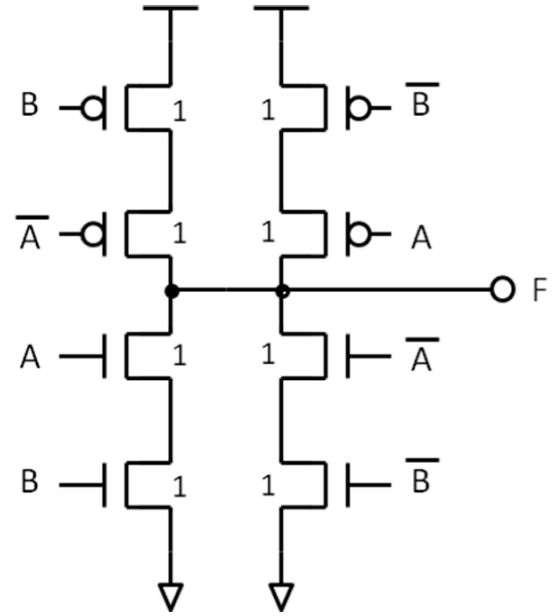


Figure 2 Complex gate.

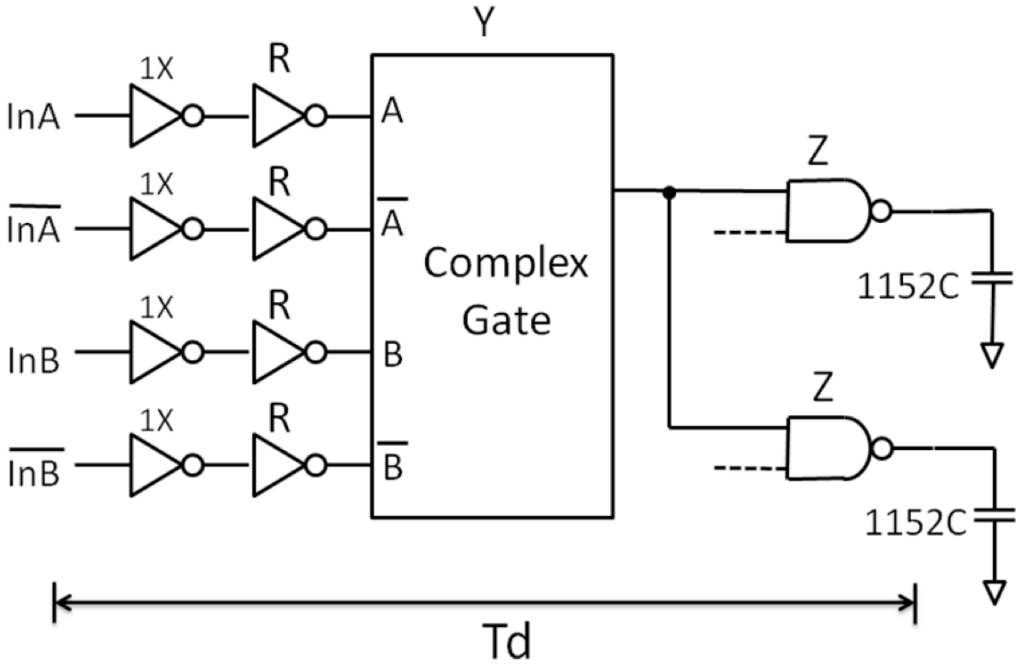


Figure 3 Complex logic network.

(5) Size the inverter R, the complex gate Y, and the NAND Z to minimize the propagation delay Td_{11} from input to output when the input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) switches from (L, H, H, L) to (H, L, H, L). (5 pts)

$G = 1 \times 1 \times \frac{4}{3} \times \frac{4}{3} = \frac{16}{9}$ (0.5 pt)

$B = 2$ (0.5 pt)

$F = 1152$ (0.5 pt)

$h = \sqrt[4]{GBF} = \sqrt[4]{\frac{16 \times 2 \times 1152}{9}} = 8$ (0.5 pt)

$f_1 = \frac{h}{g_1} = \frac{8}{1} = 8,\ f_2 = \frac{h}{g_2} = \frac{8}{1} = 8,\ f_3 = \frac{h}{g_3} = \frac{8}{\frac{4}{3}} = 6,\ f_4 = \frac{h}{g_4} = \frac{8}{\frac{4}{3}} = 6$

Sizing of gates accordingly:

$s_1 = 1$

$R = \frac{f_1 g_1}{g_2} = \frac{8 \times 1}{1} = 8$ (0.5 pt)

$Y = \frac{f_1 f_2 g_1}{g_3} = \frac{8 \times 8}{\frac{4}{3}} = 48$ (0.5 pt)

$Z = \frac{f_1 f_2 f_3 g_1}{2 g_4} = \frac{8 \times 8 \times 6}{2 \times \frac{4}{3}} = 144$ (0.5 pt)

R=8 (0.5 pt)
Y=48 (0.5 pt)
Z=144 (0.5 pt)

(6) Use the same transistor size you find in (5), Calculate the delay Td_{11}, and the propagation delay Td_{01} from input to output when the input pattern (InA, $\overline{\text{InA}}$, InB, $\overline{\text{InB}}$) switches from (H, L, H, L) back to (L, H, H, L). Assume $\gamma = 1$. (3 pts)

$$p_{11} = 1 + 1 + \frac{8}{3} + 2 = 6\frac{2}{3} \text{ (0.5 pt)}$$

$$\frac{Td_{11}}{t_{p0}} = \sum\left(p_i + \frac{f_i g_i}{\gamma} \right) = 6\frac{2}{3} + \frac{1}{\gamma}(8 + 8 + 8 + 8) = 38\frac{2}{3} \text{ (0.5 pt)}$$

$$p_{01} = 1 + 1 + \frac{16}{3} + 2 = 9\frac{1}{3} \text{ (0.5 pt)}$$

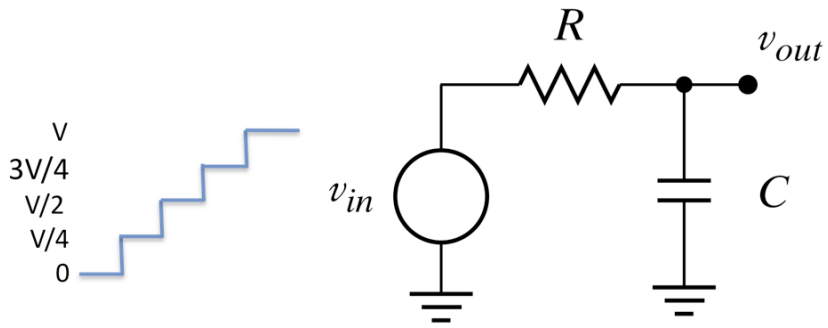
$$\frac{Td_{01}}{t_{p0}} = \sum\left(p_i + \frac{f_i g_i}{\gamma} \right) = 9\frac{1}{3} + \frac{1}{\gamma}\left(8 + 8 + 6 \times \frac{8}{3} + 8 \right) = 49\frac{1}{3} \text{ (0.5 pt)}$$

$$Td_{11} = 38\frac{2}{3} t_{p0} \text{ (0.5 pt)}$$

$$Td_{01} = 49\frac{1}{3} t_{p0} \text{ (0.5 pt)}$$

PROBLEM 3: Energy (5 pts)

A capacitor is charged using the input waveform shown in the Figure below.



a. Compute the total energy taken from the supply during the charging. Compare this to the case where the input would be raised from 0 to V in one step (3 Pts). NOTE: You may assume that the output voltage reaches steady state after every step.

E(small steps) =

E(one step) =

b. Estimate what the total energy consumption would be if the consecutive steps were made infinitesimally small. Explain. (2 Pts)

E(very small steps) =

SOLUTION:

a. E(one step) is well known and equals CV^2.
Charging a capacitance over a voltage range ΔV from a supply V takes the following amount of energy:

$$E(step) = \int_0^{\infty} V i_C dt = V \int_{V1}^{V2} C dv = CV(V2 - V1) = CV\Delta V$$

Hence, over the 4 steps (for each of which ΔV = V/4), the total energy taken from the supply equals:

$$E = E1 + E2 + E3 + E4$$
$$= C(\frac{V}{4})(\frac{V}{4} + \frac{2V}{4} + \frac{3V}{4} + \frac{4V}{4}) = \frac{5}{8}CV^2$$

b. Assume N steps:

$$E = C(\frac{V}{N})(\frac{1 + 2 + \ldots + N}{N})V = CV^2 \frac{N(N+1)}{2N^2} = \frac{CV^2}{2}$$ (for N going to infinity)

When a capacitor is charged using a very slow slope, the energy dissipated in the resistor approaches zero as the voltage over the resistor is close to zero at all times. Hence the energy taken from the supply is the energy ending up on the capacitor, which we know is $CV^2/2$.