

**San José State University**  
**Department of Electrical Engineering**  
**EE178, Digital Design with FPGAs, Spring 2017**

<b>Instructor:</b>	Eric Crabill
<b>Office Location:</b>	ENG345
<b>Telephone:</b>	1-408-316-1182 (voice and sms)
<b>Email:</b>	<a href="mailto:admin@ee178.crabill.org">admin@ee178.crabill.org</a>
<b>Office Hours:</b>	TR 20:45 – 21:00 (see classroom protocol)
<b>Class Days/Time:</b>	TR 19:30 – 20:45
<b>Classroom:</b>	ENG345
<b>Prerequisites:</b>	EE118 (with grade C or better)

### **Course Web Page and Messaging**

Copies of the course materials such as the syllabus and assignments are found on the course web page at <http://www.ee178.crabill.org>. You are responsible for joining the course discussion group linked from the course web page, a forum for all course related discussion and questions. You are responsible for regularly checking the course web page and the course discussion group to learn of any updates. The instructor phone is provided for urgent or private matters only.

### **Course Description**

This course will expose you to digital design with programmable logic devices using Verilog-HDL. Additionally, you will learn about FPGA devices, synthesis and simulation, and additional topics applicable to synchronous systems.

### **Course Goals and Student Learning Objectives**

The course goal is to provide a background, at an intermediate level, of a digital circuit design flow including capture in Verilog-HDL, synthesis, implementation, and hardware validation. Students will gain experience in application of the design flow using a state-of-the-art CAD tool and FPGA devices. ABET compliant learning objectives include, but are not limited to:

1. The ability to understand major selection criteria for implementation technologies and identify compelling advantages of FPGA devices.
2. The ability to understand and apply a hardware description language to capture design behavior and use that same hardware description language to exercise the captured design to evaluate its behavior.
3. The ability to use CAD software, tools, and instruments as part of a design flow to render digital circuits which meet their functional and performance specifications.

4. The ability to work in a group. Related, the ability to collaborate to prepare and present technical documentation of results.

## Course Policies

Use common sense during lectures and office hours. Show respect for all members of the class. If you are not sure if something is allowed, ask.

Use of the course discussion group is preferred over office hours for two reasons. First, the instructor monitors the discussion group and will generally answer questions within 24 hours. Second, on-line discussions are available for all students to review, which ensures all students have access to the same information and assistance. This eliminates redundant question for the instructor through office hours and email, and helps maintain a “level playing field” for all.

Posted office hours are the 15 minutes following the official meeting time. It is the instructor’s policy to answer all questions brought by students, so office hours may run substantially longer. To prevent abuse of the “no question left unanswered” policy, you must arrive in the officially scheduled 15 minutes and add your name to the waiting list.

## Department Policies

### Honor Code

The Electrical Engineering Department will enforce the following honor code that must be read and accepted by all students:

*I have read the honor code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:*

- *Take an exam in place of someone, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it for re-grading*
- *Leave the exam room without returning the exam to the instructor*

Measures Dealing with Occurrences of Cheating:

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University
- A student’s second offense will result in a Department recommendation of suspension

### Professional Attitude

In addition to the honor code, students understand that a professional attitude is necessary to maintain a comfortable academic environment. For example:

- Do not skip the lecture and then later ask the instructor to summarize the lecture
- Come to the lectures on time and remain for the entire duration of the session
- To minimize possible tension during exams, follow the exam rules closely

## University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. is available from the Office of Graduate and Undergraduate Programs at <http://www.sjsu.edu/gup/syllabusinfo>.

## Required Texts and Materials

### Required Textbook

There is no required textbook for this course. The instructor will provide electronic copies of the lecture material on the course web page.

### Required Materials

- Digilent Basys3 board (Xilinx Artix 7 FPGA) from <http://www.digilentinc.com>
- Laptop or desktop PC with Microsoft Windows 10 (64-bit) and a USB port
- Xilinx Vivado 2016.2 Webpack Edition from <http://www.xilinx.com>

### Other References

Your textbook from EE118 (or equivalent) serves as a fundamental reference.

## Assignments and Grading Policy

All students have the right, within a reasonable time, to know their academic scores, to review their graded work, and to be provided with explanations for the determination of their course grades. Students may request a score summary by contacting the instructor.

### Evaluation Instruments

Lab Exercises:	Four, at 8% each: 32%
Lab Exercise Quizzes:	Four, at 3% each: 12%
Lab Projects:	Four, at 8% each: 32%
Concept Exams:	Two, at 8% each: 16%
Final Presentation:	One, at 8%: 8%

### Grading Policy

100% - 90 %	A+, A, A-
89% - 80%	B+, B, B-
79% - 70%	C+, C, C-
69% - 60%	D+, D, D-
59% - 0%	F

To support ABET accreditation, and deter violations of academic integrity and the honor code, the instructor keeps a copy of all submitted evaluation instruments of all students.

Late work is not accepted and receives zero credit. Please refer to the course schedule for lab, exam, and final presentation dates and times.

### Final Evaluation

University policy requires an appropriate final examination or evaluation at the scheduled time in every course. In this course, the final evaluation consists of the final lab project and associated presentation, a team-based activity.

# EE178, Digital Design with FPGAs, Spring 2017, Course Schedule

*The schedule is subject to change with fair notice. If a change is necessary, it will be communicated via email through MySJSU.*

Week	Date	Topics, Readings, Assignments, Deadlines
1	01/24 01/26	No Class – Conference Day Administrative and kick-off details, Lab 1 Exercise assigned
2	01/31 02/02	Lab 1 Exercise due, Lab 1 Exercise quiz, Lab 2 Project assigned
3	02/07 02/09	
4	02/14 02/16	Lab 2 Project due, Lab 3 Exercise assigned
5	02/21 02/23	Lab 3 Exercise due, Lab 3 Exercise quiz, Concept Exam 1 prep
6	02/28 03/02	Concept Exam 1 Lab 4 Project assigned
7	03/07 03/09	
8	03/14 03/16	Lab 4 Project due, Lab 5 Exercise assigned
9	03/21 03/23	Lab 5 Exercise due, Lab 5 Exercise quiz
10	03/28 03/30	No Class – Spring Break No Class – Spring Break
11	04/04 04/06	Lab 6 Project assigned
12	04/11 04/13	
13	04/18 04/20	Lab 6 Project due, Concept Exam 2 prep Concept Exam 2
14	04/25 04/27	Lab 7 Exercise assigned
15	05/02 05/04	Lab 7 Exercise due, Lab 7 Exercise quiz, Lab 8 Project assigned Lab 8 Proposal due
16	05/09 05/11	
17	05/16 05/18	Presentation preparation Lab 8 Project due, Presentation, in ENG345 from 19:45 to 22:00