EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 12: Latched Comparator

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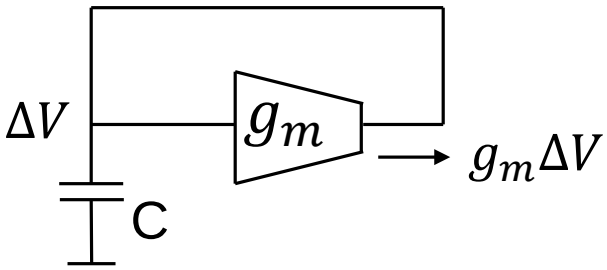
Course Schedule – Subject to Change

Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	~~Finish Flash ADC~~
28-Feb	~~DAC Architectures - Resistor, R-2R~~
5-Mar	~~DAC Architectures - Current steering, Segmented~~
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

Latched Comparator

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

Single-ended Latched Comparator



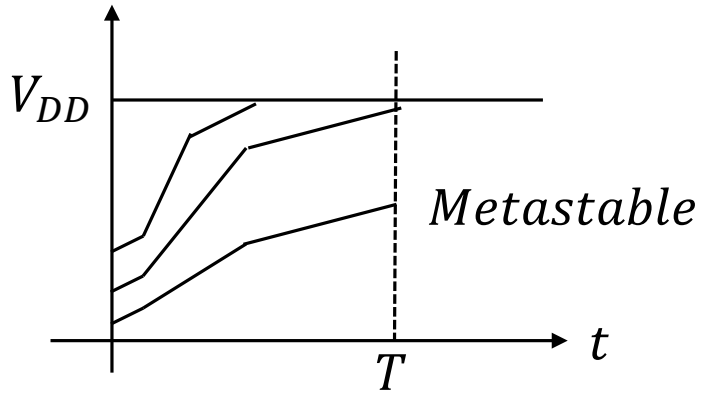
$$C\frac{dV}{dt} = g_m\Delta V$$

$$V(0) = \Delta V$$

$$V(t) = \Delta V e^{\frac{t}{\tau}}$$

$$\tau = \frac{C}{g_m}$$

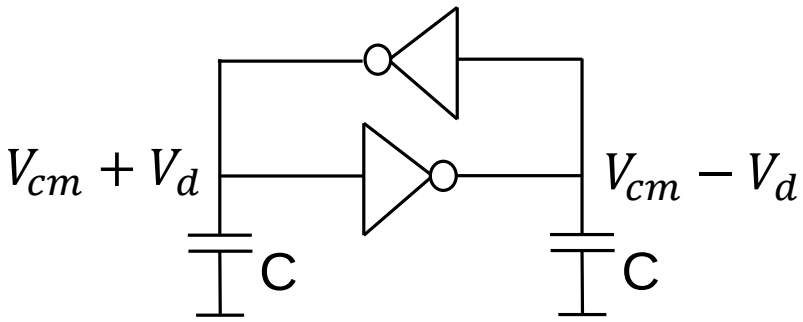
$V(t) = \Delta V e^{\frac{t}{\tau}}$

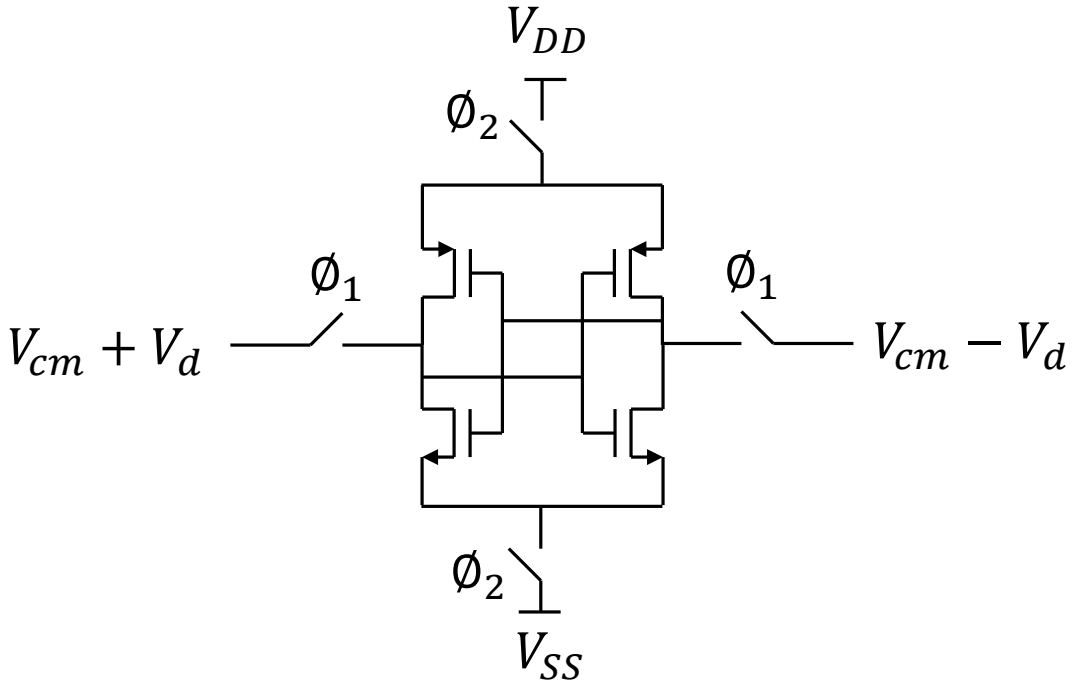


$$Gain = \frac{V_{DD}}{\Delta V} = e^{\frac{t}{\tau}}$$

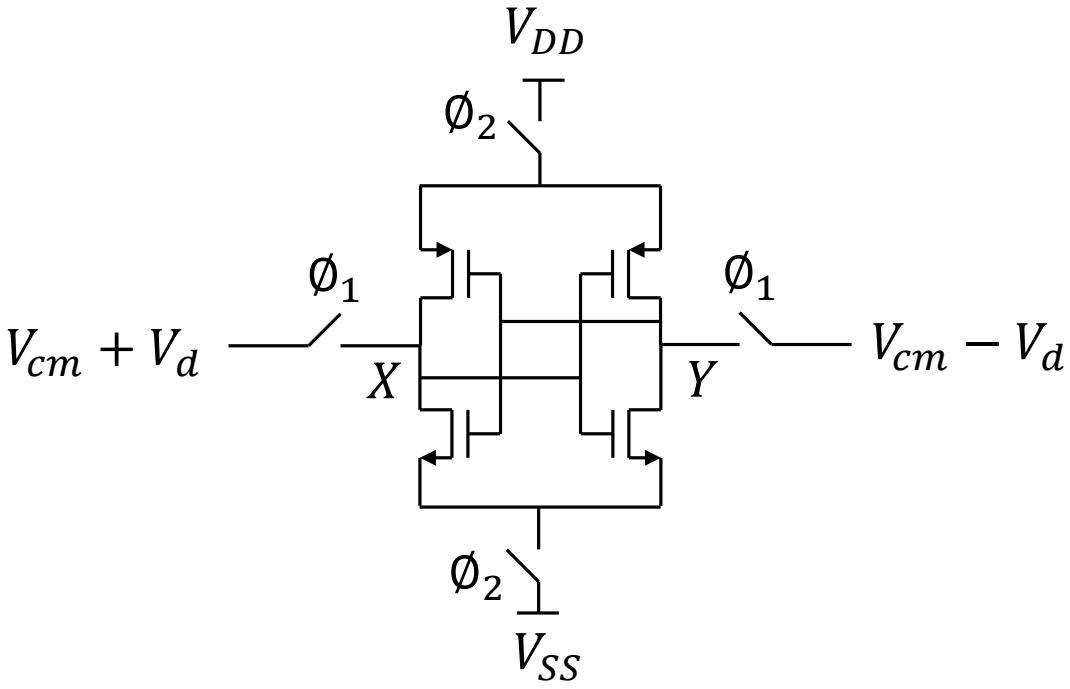
$10bit\ requires\ t = 7\tau$

Differential Latched Comparator





Differential Latched Comparator



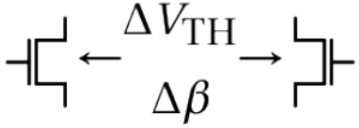
During $\emptyset_1$, input is sampled at X & Y
During $\emptyset_2$, latch regenerates

Nonidealities in Latched Comparator

- Mismatch in transistors
- Mismatch in switch
- Mismatch in Capacitance
- Dynamic mismatch

MOSFET Mismatch

- Mismatch between two identically drawn transistors
  - Vth mismatch
  - Beta mismatch



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{\beta}{2}(V_{GS} - V_{TH})^2$$

- Important contributions are t_{ox} and Dopant concentration in the channel region
- Improves with scaling in t_{ox}

$$\sigma_{\Delta VTH} = \frac{A_{VTH}}{\sqrt{WL}}$$

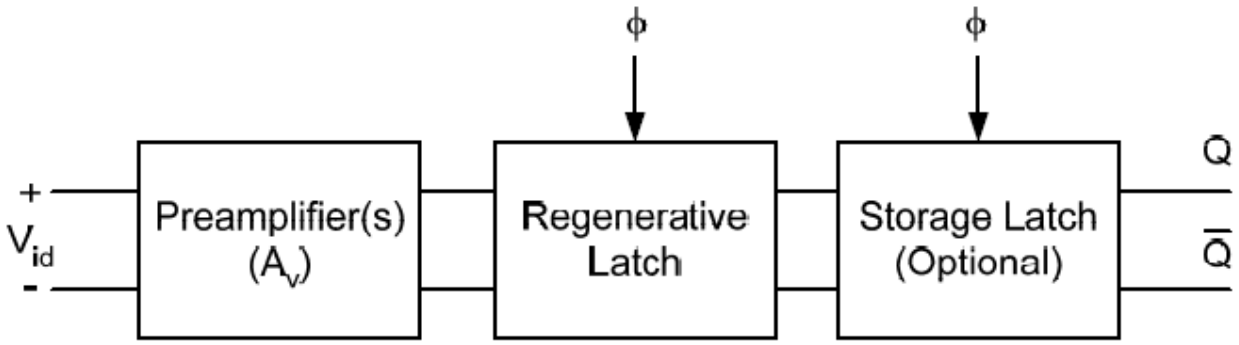
Technology parameter

Best guess

$$\frac{A_{VTH}}{t_{ox}} \approx \frac{\text{mV}\cdot\mu\text{m}}{\text{nm}}$$

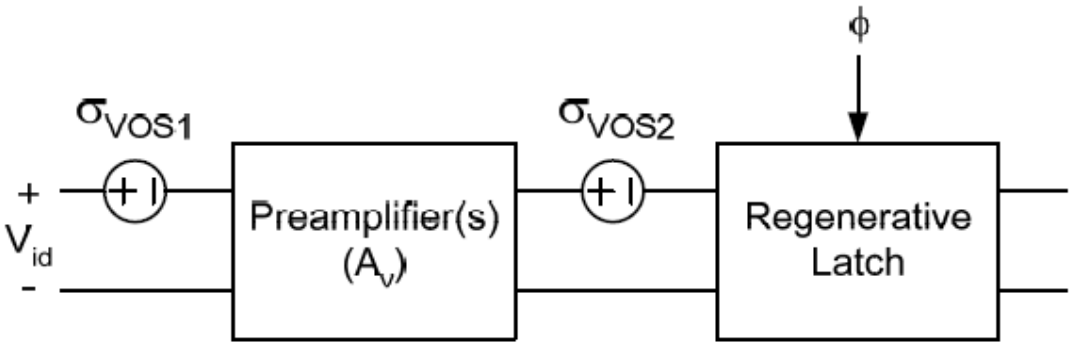
To reduce Vth mismatch
(1) Use transistor with low A_{vth}
(2) Increase the size of the transistors

Latched Comparator with Preamp



- Why bother using pre-amplification (A_v)?
  - Offset
    - Hard to build latches with offset < 10…100mV
    - Use pre-amplification to lower input referred offset
  - Common mode rejection
  - Attenuate "kickback noise"
  - Metastability

Input Referred Offset

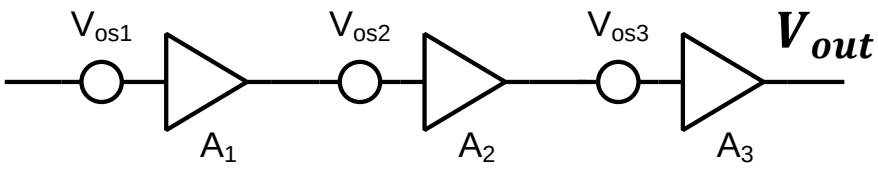


$$\sigma_{VOS}^2 = \sigma_{VOS1}^2 + \frac{1}{A_v^2}\sigma_{VOS2}^2$$

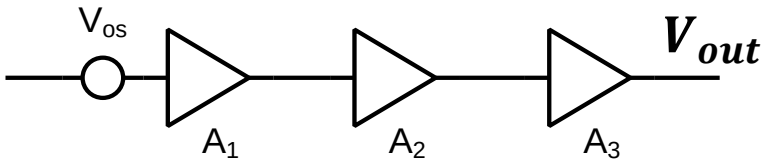
- Example: σ_{VOS1}=3mV, σ_{VOS2}=30mV, A_v=10

$$\sigma_{VOS} = \sqrt{(3\text{mV})^2 + \frac{1}{10^2}(30\text{mV})^2} = 4.2\text{mV}$$

Multi-Stage Amp Offset



Individual stage



Total input-referred

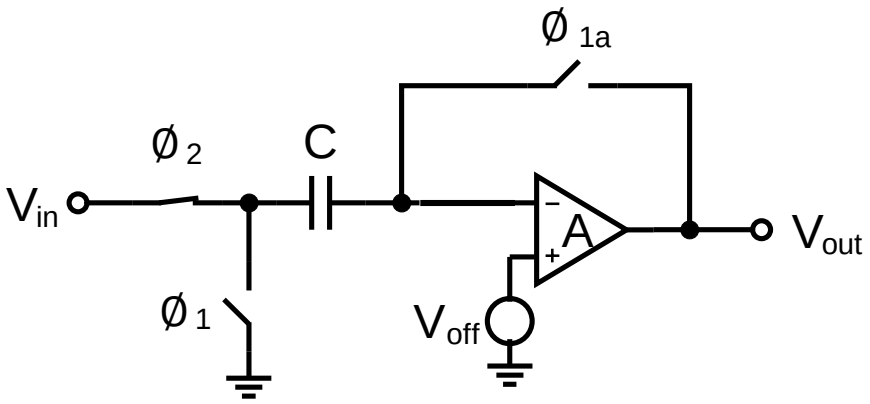
$$\boldsymbol{V_{out} = V_{os1}A_1A_2A_3 + V_{os2}A_2A_3 + V_{os3}A_3}$$

$$\boldsymbol{V_{out} = V_{os}A_1A_2A_3}$$

$$A_T = A_1 \cdot A_2 \cdot A_3$$

$$V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}$$

Input Offset Cancellation

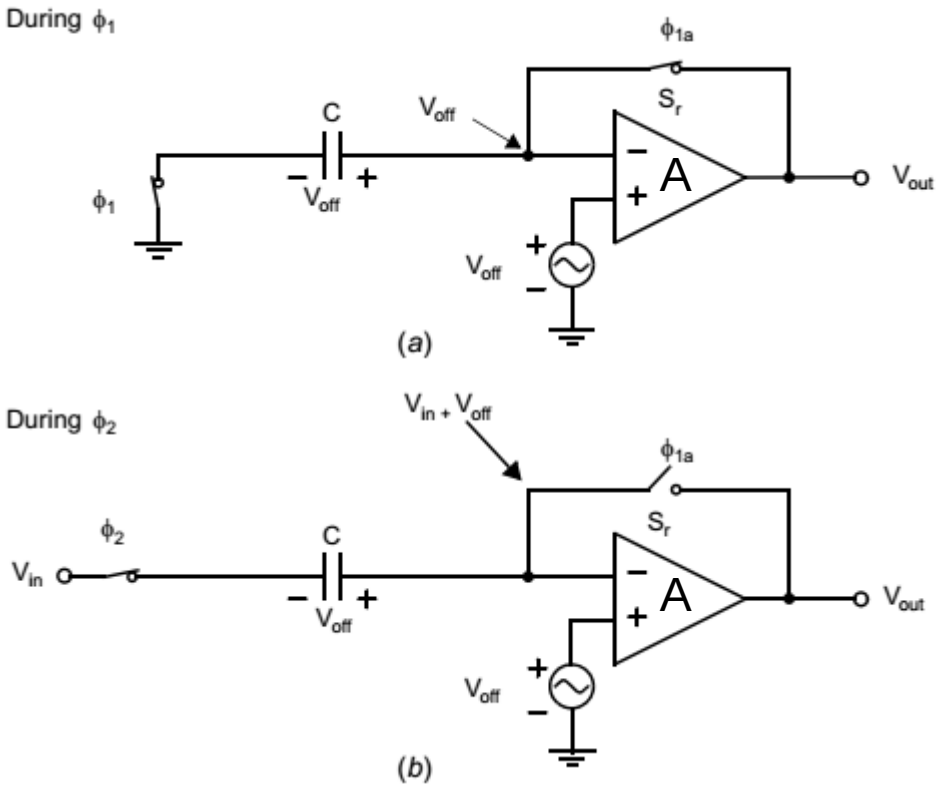


Two-phase operation,

(a) Reset phase (Φ_1) to store offset into the capacitor

(b) Comparison phase (Φ_2) to subtract the offset from the input

Input Offset Cancellation



$$V_c = A(V_{off} - V_c)$$
$$= \frac{A}{1+A} \cdot V_{off}$$
$$\approx V_{off}$$

$$V_{out} = -A(V_{in} + V_c - V_{off})$$
$$= -A\left(V_{in} - \frac{V_{off}}{1+A}\right)$$

Closed loop stability required

Input-referred offset :

$$V_{os,in} = \frac{V_{os}}{1+A}$$