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Fifty Applications of the CMOS Inverter—Part 5

In this article, we complete our study of the CMOS inverter's applications. As in previous articles, we evaluate each circuit by designing and simulating it in the slow–slow corner of 28-nm CMOS technology with a supply voltage of 0.95 V and at 75 °C.

The Three-Stage Operational Amplifier

The ability of CMOS inverters to operate at low supply voltages makes them attractive for operational amplifier (op amp) design. With a voltage gain of 5–10 per inverter, we expect that a three-stage op amp will prove useful in many applications.

Consider the chain shown in Figure 1(a), where C_A, C_B, and C_C denote the total capacitance at nodes A, B, and C, respectively. Modeling each inverter by a transconductance, G_m, and an output resistance, R_{out}, we express the circuit's voltage gain as $A_{123}=-(G_{m1}R_{out1})(G_{m2}R_{out2})(G_{m3}R_{out3})$. Exhibiting three poles, the cascade is likely to suffer from a poor phase margin (PM).

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To compensate the amplifier, we can create a dominant pole at A by Miller multiplication of a capacitor, C_M [Figure 1(b)] [1]. The resulting right-half-plane zero, $\omega_z \approx G_{m2}/C_B$, degrades the PM, necessitating the use of R_M to move ω_z to infinity or place it atop the first nondominant pole. Miller compensation also leads to pole splitting, raising the pole at B from $1/(R_{out2}C_B)$ to approximately G_{m2}/C_B, i.e., by a factor of 5 to 10.

The PM can be further improved through the use of feedforward, as practiced in previous op amps [2] and depicted in Figure 1(c) [1]. At high frequencies, the main path displays less gain and more phase shift, while the feedforward path, Inv_4, dominates, thus reducing the input–output phase shift. Equivalently, this path introduces a left-half-plane zero, which can be calculated by noting that both paths share the pole at node C and

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_{123}}{\left(1+\frac{s}{\omega_A}\right)\left(1+\frac{s}{\omega_B}\right)\left(1+\frac{s}{\omega_C}\right)} + \frac{A_4}{1+\frac{s}{\omega_C}}. \quad (1)$$

Here, each ω denotes the pole corresponding to a node after frequency compensation, and $A_4 = -G_{m4}R_{out3}$. (We neglect, for now, the reduction in R_{out3} due to the presence of Inv_4.) It follows that

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_{123}+A_4\left(1+\frac{s}{\omega_A}\right)\left(1+\frac{s}{\omega_B}\right)}{\left(1+\frac{s}{\omega_A}\right)\left(1+\frac{s}{\omega_B}\right)\left(1+\frac{s}{\omega_C}\right)}. \quad (2)$$

Feedforward, in fact, creates two zeros because the main path contains three poles. Nonetheless, if pole splitting and proper choice of R_M have moved up ω_B so much that $|A_4|\,\omega_B \gg 4\,|A_{123}|\,\omega_A$, then the lower zero due to feedforward is given by

$$\omega_{z,FF} \approx \frac{-A_{123}}{A_4}\omega_A. \quad (3)$$

This zero is a multiple of the dominant pole, ω_A, and it can be positioned so as to deflect the phase upward at frequencies below the unity-gain bandwidth, ω_u.

We should make two remarks. First, because of the input capacitance of Inv_1, the circuit incurs a *fourth* pole if it is placed in a resistive feedback loop. Second, the

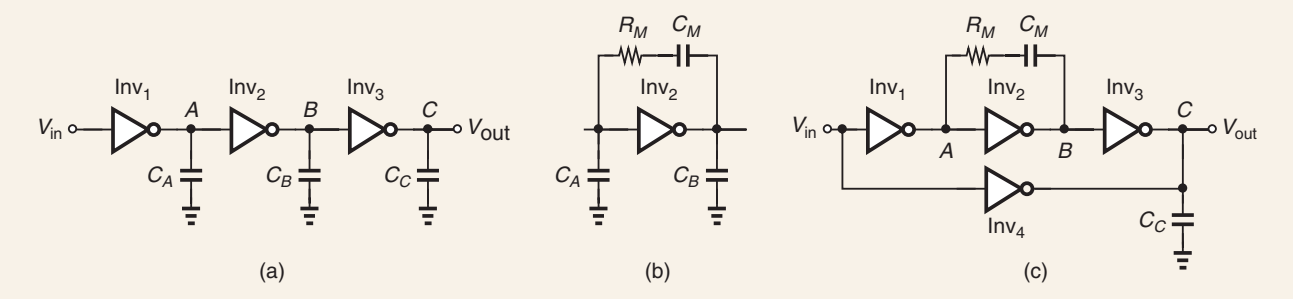

FIGURE 1: (a) Three inverters forming an amplifier, (b) the Miller compensation network, and (c) the use of feedforward.

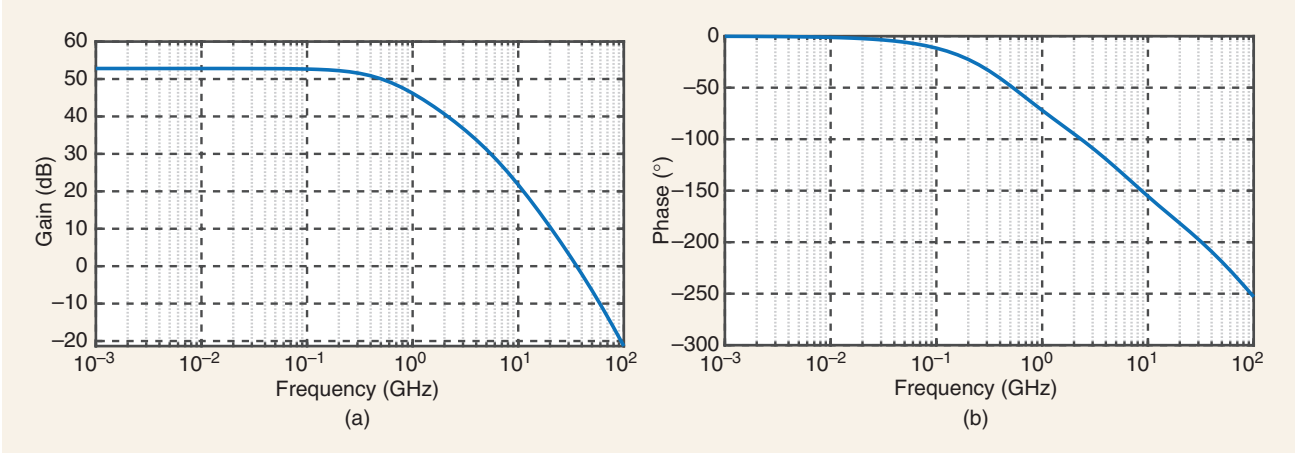

FIGURE 2: (a) Gain and (b) phase plots of uncompensated amplifier.

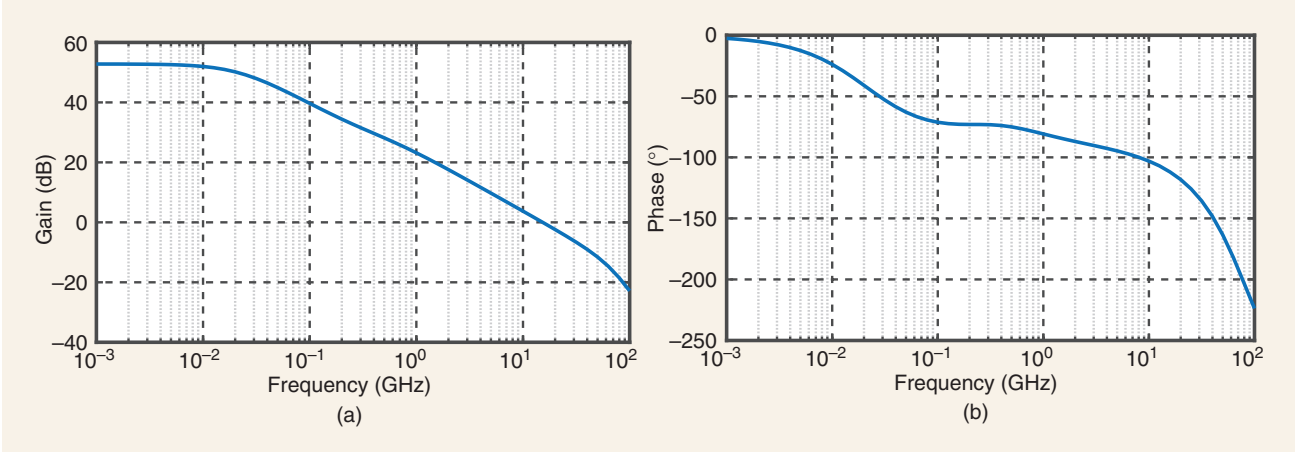

FIGURE 3: (a) Gain and (b) phase plots of compensated amplifier.

feedforward path, in fact, reduces the overall gain as it lowers the output resistance of the third stage and hence A_{123}, even though G_{m4} contributes additional gain.

In practice, two such chains can form a pseudodifferential op amp, improving the supply rejection and lowering the distortion.

We design the circuit of Figure 1(a) with $(W/L)_P = 2(W/L)_N = 8$ µm/30 nm while assuming a load capacitance, C_L, of 500 fF. One chain draws 2 mW. Plotted in Figure 2, the open-loop frequency response reveals an ω_u of approximately $2\pi \times (30\,\text{GHz})$, at which the phase shift reaches -210°. The op amp would therefore be unstable in a unity-gain feedback loop. Each inverter provides a gain of about 8.

We now select $C_M = 1$ pF and $R_M = 600\,\Omega$, arriving at the results shown in Figure 3. We have $\omega_u = 2\pi \times (15\,\text{GHz})$ with PM = 58°.

The efficacy of the feedforward path in Figure 1(c) depends on the load capacitance. For $C_L = 500$ fF, it negligibly changes the PM. For $C_L = 50$ fF, on the other hand, simulations indicate an increase of about 10° but at the cost of a 3-dB gain reduction.

The High-Gain Transimpedance Amplifier

We have seen in a previous article [3] that a single inverter with resistive feedback can serve as a transimpedance amplifier (TIA) in an optical receiver front end. We can extend the concept to a cascade of three inverters (Figure 4), seeking a higher value for R_F so as to increase the gain and decrease its noise contribution. In contrast to the three-stage op amp studied in the previous section, the large photodiode capacitance, C_{PD}, creates

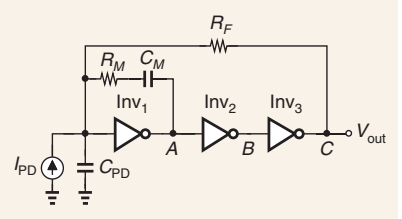

FIGURE 4: A three-stage TIA.

a dominant pole at the *input* here. We then place the compensation network around Inv_1, moving this pole to a lower frequency and raising ω_A. The poles at *A* and *B* remain unchanged and ultimately limit the achievable bandwidth.

We simulate the circuit of Figure 4 with $(W/L)_P = 2(W/L)_N = 8$ µm/30 nm, $C_{PD} = 200$ fF, $R_F = 2$ kΩ, $C_M = 1$ pF, and $R_M = 200\,\Omega$. The closed-loop response shown in Figure 5(a) indicates a 3-dB bandwidth of 16 GHz. To obtain the input-referred noise current, we plot the output noise

voltage spectrum in Figure 5(b), integrate it up to 100 GHz, divide it by the low-frequency gain and the 3-dB bandwidth, and take the square root of the result. We obtain 35 pA/$\sqrt{\text{Hz}}$. According to simulations, 70% of this noise arises from R_F at low frequencies. The peak at 11 GHz stems from R_M as C_M presents a low impedance at this frequency. The TIA consumes 2 mW.

The Duty-Cycle Distortion Circuit

High-speed clocks and LO waveforms experience duty-cycle distortion (DCC) as they travel through circuits and interconnects. We presented a DCC stage in [3], but it did not include a means of *measuring* the distortion. We now study an alternative that does.

We begin with a structure whose output rise and fall times can be controlled, namely, a "starved" inverter [Figure 6(a)]. We observe that, as V_{cont} increases, the pull-down branch consisting of M_1 and M_3 becomes stronger while the pull-up branch comprising M_2 and M_4 becomes weaker. Displayed in Figure 6(b), the output duty cycle thus increases from $(t_2 - t_1)/T_0$ to $(t_4 - t_3)/T_0$, where T_0 denotes the period. The difficulty here is that the inverter dies of starvation if the DCC loop begins with $V_{\text{cont}} = 0$ or $V_{\text{cont}} = V_{DD}$. We then add M_5 and M_6 to keep the circuit alive even at these extreme cases.

To obtain a wider DCC range, we can cascade a number of these stages. However, we must bear in mind that each stage inverts, changing a duty cycle of greater than 50% to less and vice versa. For proper operation, therefore, a simple inverter must be interposed between every two DCC stages. The

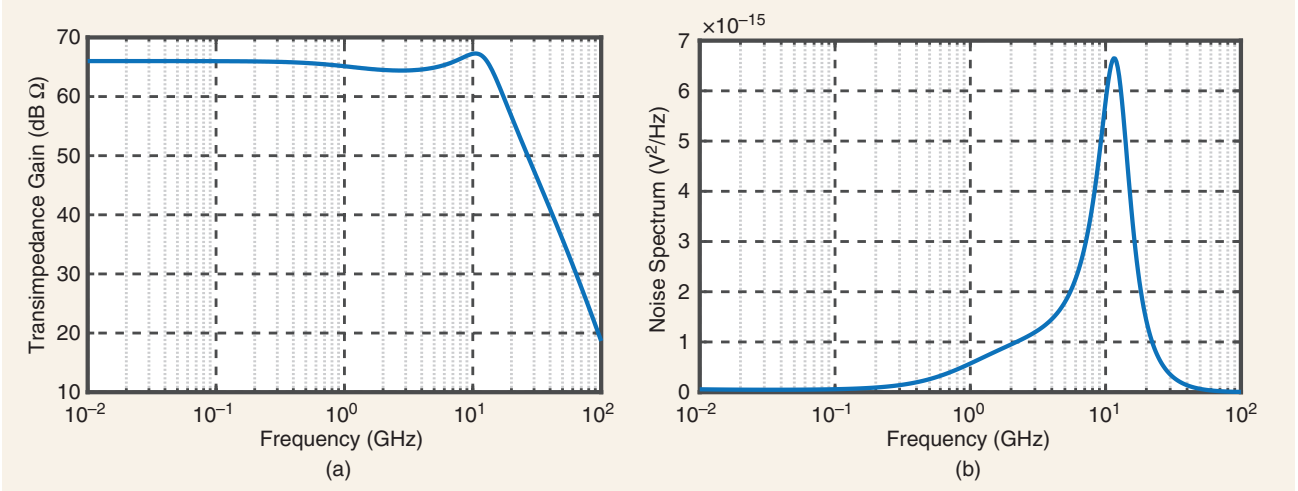

FIGURE 5: (a) Gain and (b) output noise plots of the TIA.

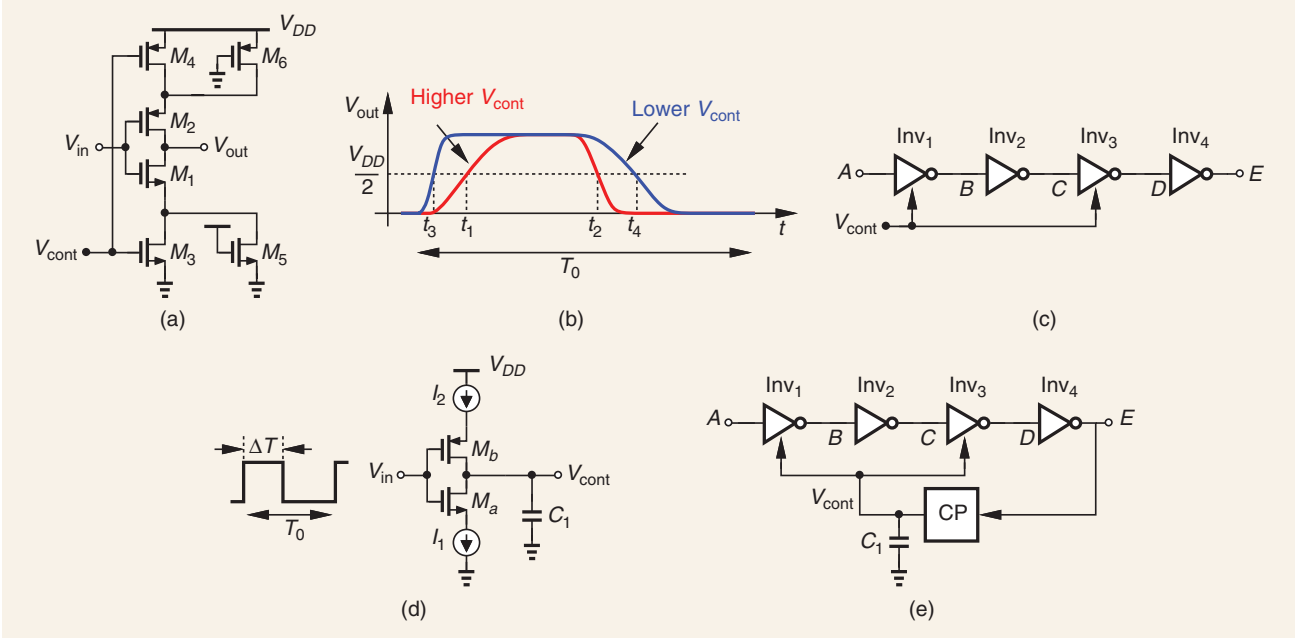

FIGURE 6: (a) A starved inverter, (b) the effect of V_{cont} on the duty cycle, (c) the DCC cascade, (d) a CP, and (e) the complete DCC loop. CP: charge pump.

resulting chain emerges as shown in Figure 6(c), where Inv_1 and Inv_3 increase the duration of the high level at their outputs as V_{cont} rises.

Next, we seek an arrangement that measures the DCC and generates V_{cont} accordingly. Shown in Figure 6(d) is a simple charge pump (CP) that discharges C_1 by I_1 for ΔT seconds and charges it by I_2 for the remainder of the period. If $I_1 = I_2$, then V_{cont} is bounded only if $\Delta T = T_0 - \Delta T$ and hence $\Delta T = T_0/2$.

In the last step of our design, we form the DCC loop, as presented in Figure 6(e). The reader is encouraged to verify that the feedback is negative.

We simulate the DCC circuit with $(W/L)_1 = 0.5\ \mu\text{m}/30\ \text{nm}$, $(W/L)_3 = 1\ \mu\text{m}/30\ \text{nm}$, and $(W/L)_5 = 250\ \text{nm}/240\ \text{nm}$ in Figure 6(a). (The PMOS devices are twice as wide.) We also select $(W/L)_P = 2(W/L)_N = 2\ \mu\text{m}/30\ \text{nm}$, $I_1 = I_2 = 50\ \mu\text{A}$, and $C_1 = 0.5\ \text{pF}$ in Figure 6(d).

Plotted in Figure 7(a) are the input and output waveforms of Figure 6(e) at 10 GHz while the former incurs a duty cycle of 40%. We note that the output duty cycle is about 51%. Figure 7(b) displays the settling of the control voltage. The circuit dissipates 1.2 mW.

The PAM4 Driver With Back Termination

We have seen that a self-biased inverter having a transconductance of G_m presents an input impedance of $1/G_m$ if channel-length modulation is neglected. The same holds true for its *output* impedance [Figure 8(a)].

This property proves useful in high-speed driver design because of

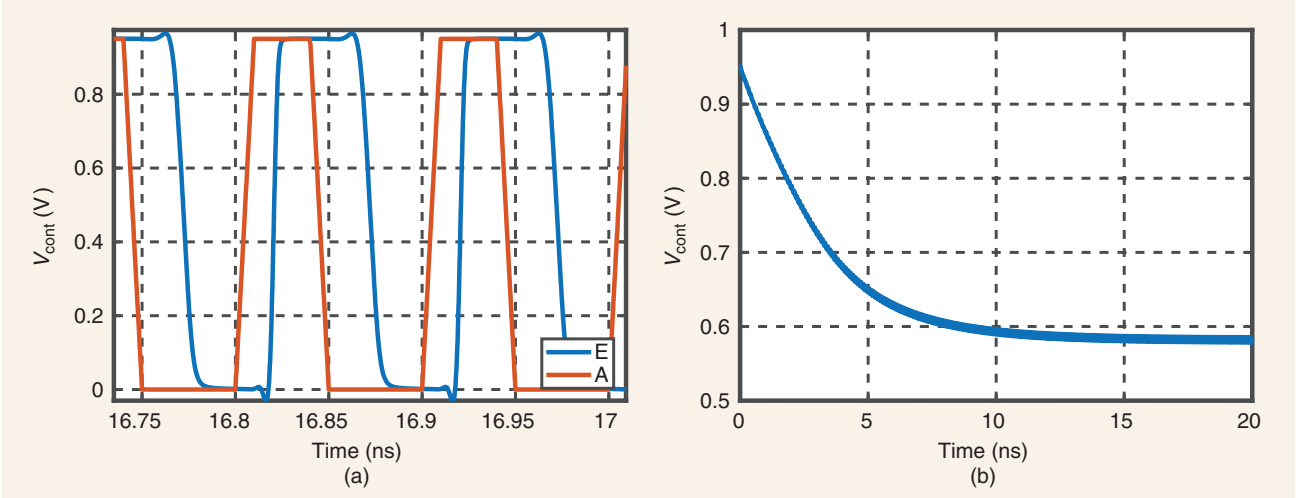

FIGURE 7: (a) DCC input and output waveforms and (b) behavior of control voltage.

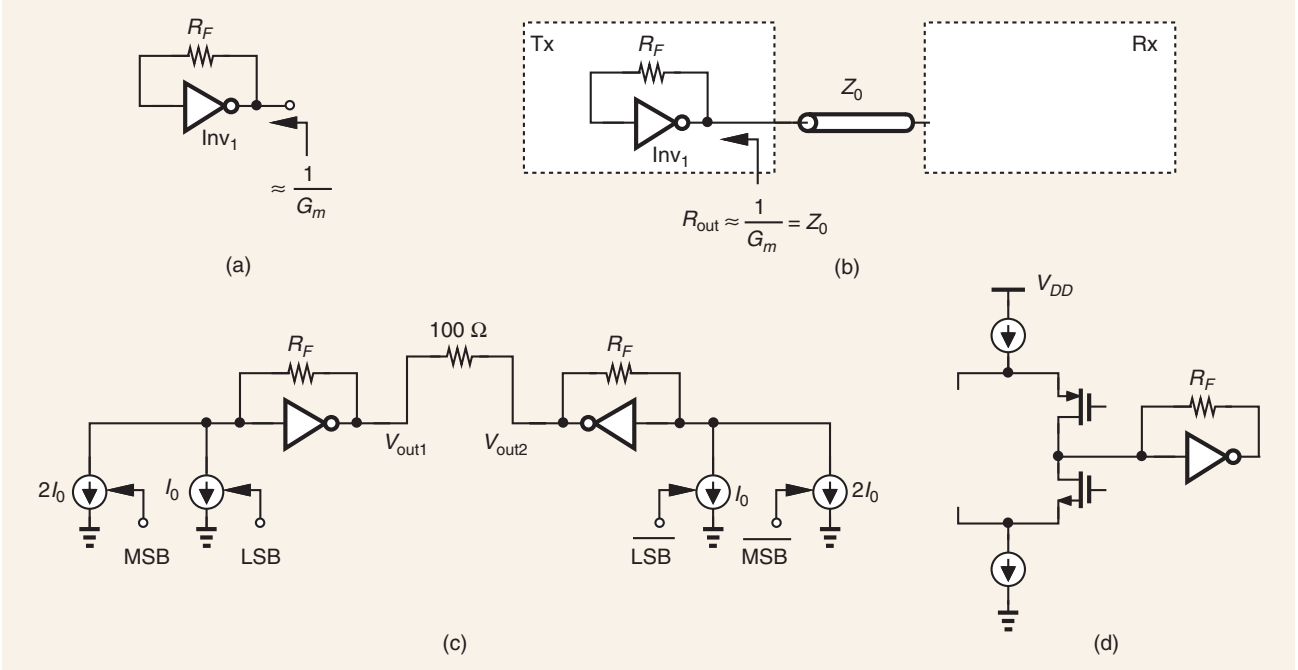

FIGURE 8: (a) Output impedance of a self-biased inverter, (b) use of the circuit to provide back termination, (c) addition of DACs, and (d) the complementary DAC topology.

the need for proper "back termination." Illustrated in Figure 8(b) [4], the idea is to set the driver output impedance equal to the characteristic impedance of the transmission line, Z_0, so that reflections from the far-end receiver are absorbed upon returning to the Tx.

The reader may wonder about the necessary output impedance of the stage *preceding* the inverter in Figure 8(b). If not sufficiently high, this impedance lowers the loop gain around the inverter, yielding $R_{out} > 1/G_m$. We thus prefer to apply a current source to the input. In this spirit, we can extend the idea to four-level PAM (PAM4). As shown in Figure 8(c) for differential signaling, a 2-bit current-steering DAC drives the input of each driver [4]. The 100-Ω load models the channel.

We should remark that V_{out1} and V_{out2} in Figure 8(c) are differential waveforms only if the input currents toggle between positive and negative values—rather than between a positive value and zero. That is, the DACs must incorporate both PMOS and NMOS current sources [Figure 8(d)].

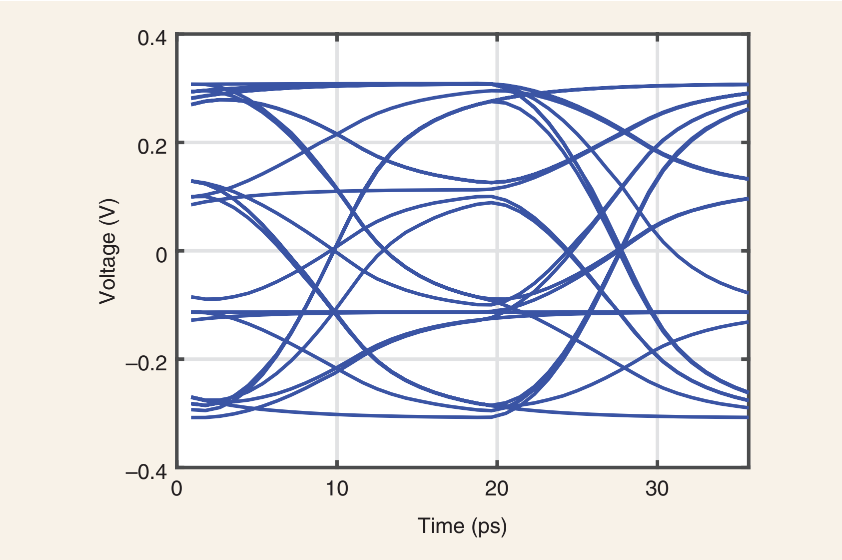

FIGURE 9: PAM4 driver output eye diagram.

We simulate the circuit with $(W/L)_P = 2(W/L)_N = 16$ µm/30 nm and $R_F = 500\,\Omega$. These values are chosen so as to provide a 50-Ω output resistance. We also have $I_0 = 0.5$ mA. Plotted in Figure 9 is the output PAM4 waveform at 112 Gb/s. The circuit's speed is limited primarily by the input time constant of the inverters, which amounts to

$$\tau = \frac{R_F + r_{ON} \| r_{OP} \| Z_0}{1 + G_m (r_{ON} \| r_{OP}) \| Z_0} C_{in} \qquad (4)$$

where the first fraction represents the input resistance, and C_{in} is the inverter's input capacitance. The driver draws 3.4 mW.

The DT Integrator

Some oversampling data converters and analog filters incorporate DT integrators. Shown in Figure 10(a), such a structure periodically samples V_{in} on C_1 and transfers its charge to C_2 through the virtual ground, X. In differential implementations, the op amp output requires common-mode (CM) feedback.

We can replace the op amp in Figure 10(a) with an inverter [Figure 10(b)], but we must ponder how the dc level at X should be defined to ensure that Inv_1 operates in its high-gain region. In fact, if, for example, $V_{in} \approx V_{DD}/2$ and the

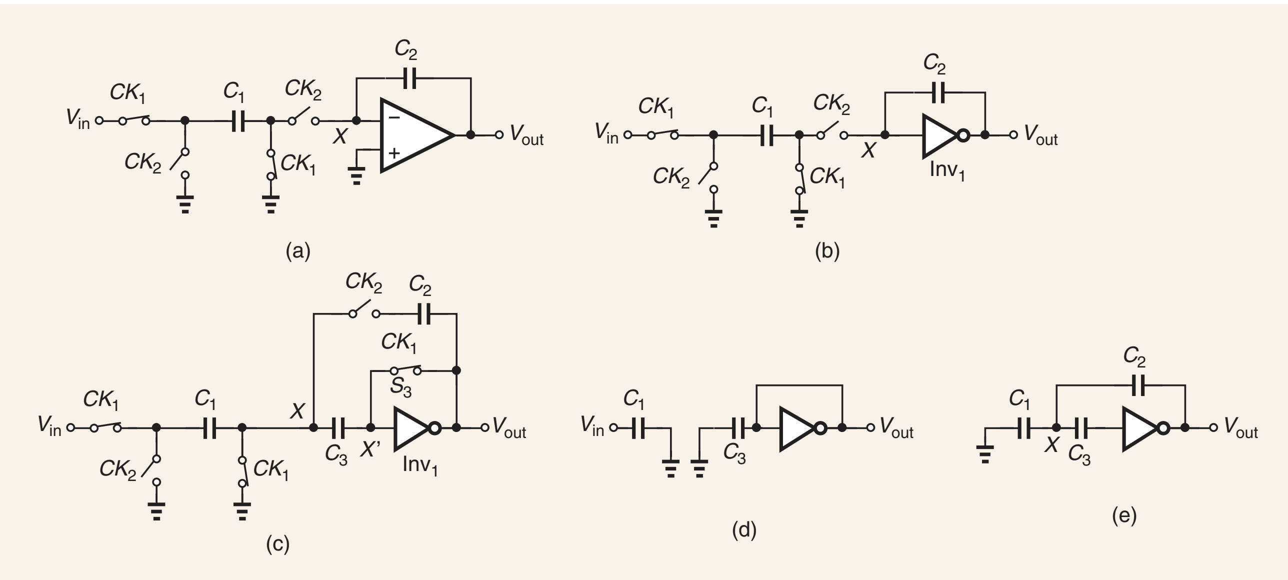

FIGURE 10: (a) A DT integrator, (b) realization using an inverter, (c) addition of reset switch, (d) the circuit in sampling mode, and (e) the circuit in integration mode.

circuit begins with $V_X = 0$, Inv_1 has no ability to create a virtual ground at this node. We therefore modify the structure, as depicted in Figure 10(c) [5], where S_3 biases Inv_1 properly during CK_1, storing the necessary voltage on C_3 [Figure 10(d)]. After C_1 samples V_{in}, its right plate is connected to X and its left plate to ground [Figure 10(e)], delivering its charge to C_2.

We simulate the circuit of Figure 10(e) with $(W/L)_P = 2(W/L)_N = 8\ \mu\text{m}/30\ \text{nm}$ for Inv_1, $C_1 = C_2 = 0.2$ pF, and $C_3 = 0.1$ pF (about 10 times the input capacitance of Inv_1). Figure 11 plots the output waveform at a clock frequency of 1 GHz. The integrator consumes 0.5 mW. In practice, we employ two such configurations for pseudodifferential operation.

The integrator merits two remarks. First, the low voltage gain of inverters limits the linearity of this realization. Second, this topology yields a "return-to-zero" output as a result of the inverter reset operation in every cycle. This leaves less time for the next stage to sense the result.

The Polyphase Filter

At very high frequencies, we may resort to polyphase filters to generate quadrature phases of a clock or LO from differential phases. Consider the passive realization displayed in Figure 12(a), where a differential input represented by $+V_1$ and $-V_1$ produces signals $\pm V_X$ and $\pm V_Y$. It can be readily shown that $+V_X$ and $+V_Y$ bear a phase difference of 90°, and so do $-V_X$ and $-V_Y$. The amplitudes are equal if the input frequency is chosen according to $\omega_{\text{in}} = 1/(R_1 C_1)$, at which $|V_X/V_1| = \sqrt{2}/2$. We say that the filter incurs 3 dB of loss.

For a 90° phase shift, we can alternatively consider an *integrator*, e.g., an ideal G_m stage driving a capacitor [Figure 12(b)]. We have $V_{\text{out}}/V_{\text{in}} = -G_m/(C_1 s)$. Let us extend the idea to differential signals and modify the topology of Figure 12(a) to that shown in Figure 12(c). The feedback resistors establish proper biasing for the inverters. The vertical branches appear redundant because $+V_Y \approx V_1$ and $-V_Y \approx -V_1$, but they do create the same output impedance for $\pm V_Y$ as that for $\pm V_X$. This is necessary for retaining accuracy while the circuit drives the next stage.

We simulate the circuit of Figure 12(c) at 28 GHz with $(W/L)_P = 2(W/L)_N = 2\ \mu\text{m}/30\ \text{nm}$, $C_1 = 10$ fF, and 5-kΩ feedback resistors. The waveforms presented in Figure 13 reveal reasonable quadrature accuracy but some amplitude mismatch, which can be suppressed by applying these outputs to additional inverters. Interestingly, $+V_Y$ and $-V_Y$ exceed the supply rails (why?).

The Downconverter With a Translational Virtual Ground

RF receivers often incorporate a cascade consisting of a G_m stage, passive mixers, and baseband low-pass TIAs [Figure 14(a)]. Such an arrangement offers two benefits: the voltage swings at A and B are minimized,

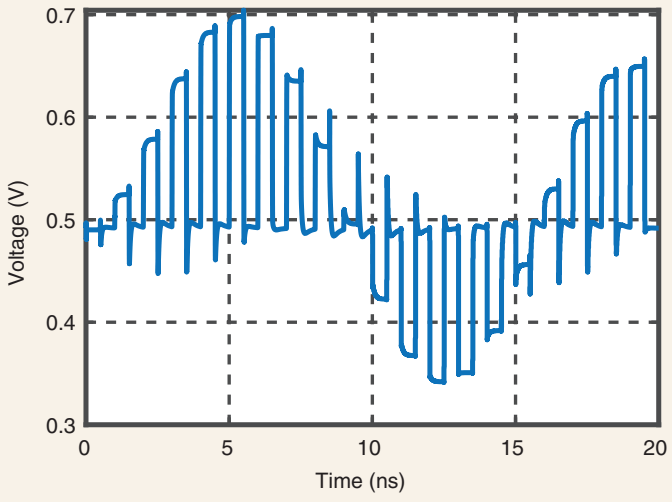

FIGURE 11: The integrator output waveform.

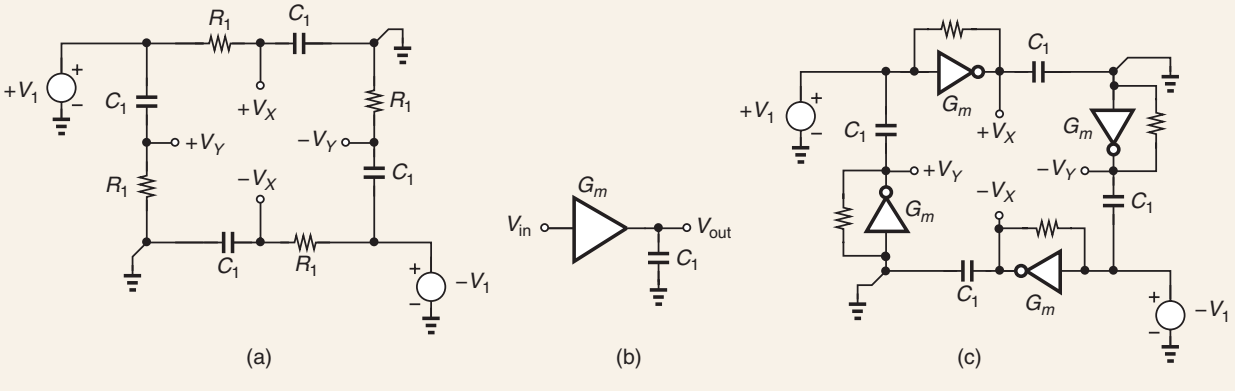

FIGURE 12: (a) A passive polyphase filter, (b) a 90° phase shift circuit, and (c) a polyphase filter using inverters.

improving the linearity, and the mixer contributes little noise as its output is dictated by the current delivered by the G_m stage. However, the virtual ground created by the TIA at B and A experiences excessive voltage excursions in the presence of large blockers. This happens because the TIA does not provide sufficient loop gain at the downconverted blocker frequency.

This issue can be alleviated as follows. First, consider the arrangement shown in Figure 14(b), where the four mixer switches are driven by four nonoverlapping LO phases with a period of T_{LO}. We observe that $Z_{in} = R_L$ here because, at any given point in time, only one of the resistors is tied to A.

Next, we add a capacitor in parallel with each resistor [Figure 14(c)], assuming $R_L C_L \gg 1/(4T_{LO})$. The input impedance of this N-path filter then emerges as [6]

$$Z_{in} = \frac{R_L}{4[1 + jC_L R_L(\omega - \omega_{LO})]}. \quad (5)$$

At input frequencies close to the LO frequency, we have $Z_{in} \approx R_L/4$. Thus, the *hold* operation offered by C_L lowers the input *resistance* by a factor of 4, attenuating the blocker-induced voltage swings.

We can now transform the baseband networks of Figure 14(c) to TIAs with the aid of amplifiers [6], e.g., inverters. Illustrated in Figure 14(d), the result establishes an input resistance of $1/G_{mi}$ in parallel with each C_L at the blocker frequency. We therefore have $Z_{in} \approx 1/(4G_{mi})$.

We simulate the circuit of Figure 14(d) with $(W/L)_P = 2(W/L)_N = 2\,\mu m/30\,nm$, $C_L = 8$ pF, and $R_F = 5\,k\Omega$. Setting the input and LO frequencies to 5 GHz and 5.1 GHz, respectively, we obtain the waveforms shown in Figure 15 for the voltage at node A with and without C_L. It is observed that C_L reduces the swing by about a factor of 3. The circuit consumes 2 mW.

The Low-Voltage Active Mixer

Active mixers are typically realized by differential pairs, facing tradeoffs among noise, linearity, conversion gain, and voltage headroom. It is possible to configure an inverter so that it operates as an active mixer with a low supply voltage.

Let us begin with the inverter shown in Figure 16(a), where we have $V_{DD} = V_{GS1} + |V_{GS2}|$. To accommodate a lower supply voltage, we can capacitively couple V_{in} to one of the gates, as depicted in Figure 16(b). Here, the bias current of M_2 is defined independently, allowing V_{DD} to be less than $V_{GS1} + |V_{GS2}|$. Next, we incorporate mixing by switching both M_1 and M_2 [Figure 16(c)] [7].

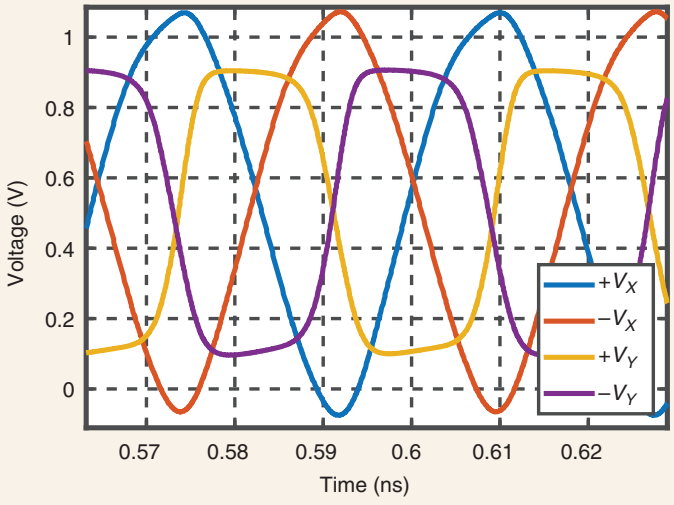

FIGURE 13: Polyphase output waveforms.

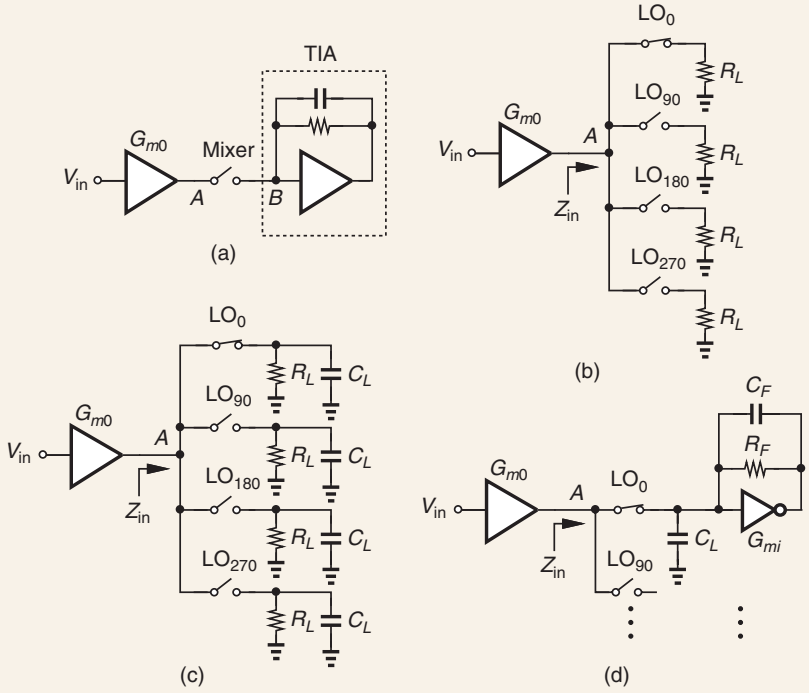

FIGURE 14: (a) A typical RF receiver chain, (b) a simple current-driven downconverter, (c) the addition of hold capacitors, and (d) the use of inverters to create a virtual ground.

With ideal switches, the circuit's voltage gain now toggles between zero (when M_1 and M_2 are off) and $-(g_{m1}+g_{m2})(r_{01}\|r_{02})$ (when they are on).

It is preferable for mixers to produce differential outputs even though their input is single ended. We therefore employ two instances of the circuit, with one driven by $\overline{\text{LO}}$ [Figure 16(d)]. The remaining issue is that the output CM level is poorly defined here. We finally arrive at the topology shown in Figure 16(e), where R_1 and R_2 provide CM feedback to the gates of M_2 and M_4, yielding an output CM voltage of $V_{DD}-|V_{GS2,4}|$. Moreover, we drive the sources of M_1–M_4 by inverters [7].

The mixer thus obtained can suffer from a high NF due to the flicker noise of Inv_1 and Inv_2, which modulates the switching time of M_1–M_4. For this reason, the two inverters must incorporate wide transistors. We simulate the mixer of Figure 16(e) with $(W/L)_P=2(W/L)_N=16\,\mu\text{m}/30\,\text{nm}$ for the core and the inverters. We also have $C_1=500$ fF and $R_1=R_2=10\,\text{k}\Omega$. At an LO frequency of 5 GHz, the circuit draws 1.7 mW and exhibits the double-sideband NF plotted in Figure 17. The conversion gain is 9 dB.

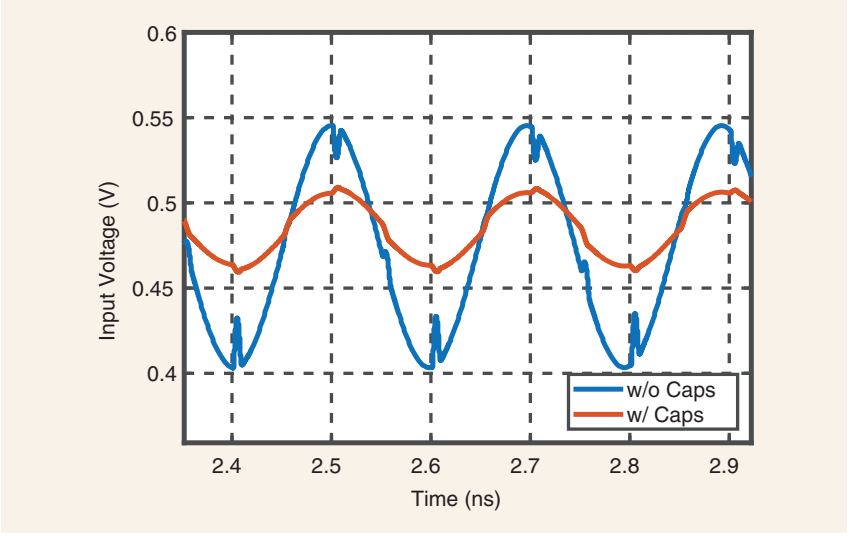

FIGURE 15: The input voltage waveform of the downconverter. w/o: without; w/: with; Caps: capacitors.

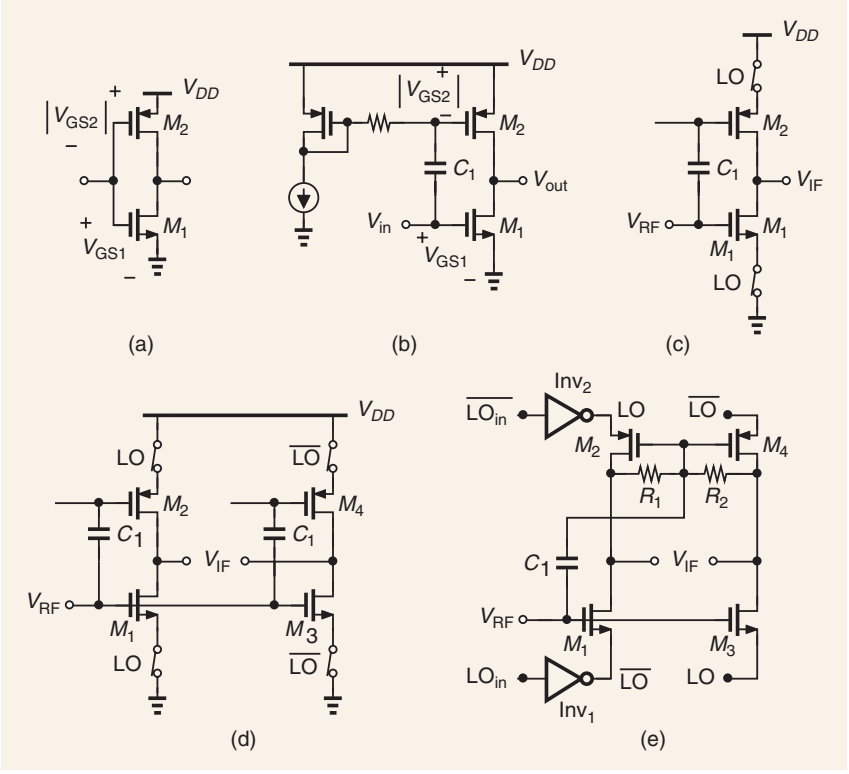

FIGURE 16: (a) An inverter showing its supply voltage limitation, (b) capacitive coupling to the PMOS device, (c) the addition of switches to form a mixer, (d) modification to obtain differential outputs, and (e) the addition of CM feedback.

The Bidirectional Hybrid

High-speed links between chiplets may allow data transfer on a single wire in *both* directions. Displayed conceptually in Figure 18(a), such a system doubles the data rate per wire. However, each side must employ a "hybrid" to ensure that the transmitted signal, e.g., D_{TX1}, does not corrupt the received data, e.g., $D_{RX1}=D_{TX2}$.

To develop a hybrid, we begin with the topology shown in Figure 18(b), where the output resistance of Inv_1, R_{out1}, and R_T add up to Z_0, creating proper back termination. We wish to connect the receiver input to node A such that it is free from D_{TX1}. As illustrated in Figure 18(c), we generate a complementary replica of D_{TX1} by means of Inv_2 and Inv_3 and sum the result with D_{TX1} at virtual ground B [8]. An appropriate choice of R_1 and R_2, in principle, cancels D_{TX1} completely. It is desirable to select $R_1 \gg Z_0/2$ so as to negligibly attenuate the transmitted signal.

The hybrid of Figure 18(c) must deal with incomplete cancellation arising from the delay mismatch between Inv_1 and the cascade of Inv_2 and Inv_3. To ameliorate this issue, we replace this cascade with a transmission gate [Figure 18(c)] so that the two paths exhibit approximately equal delays.

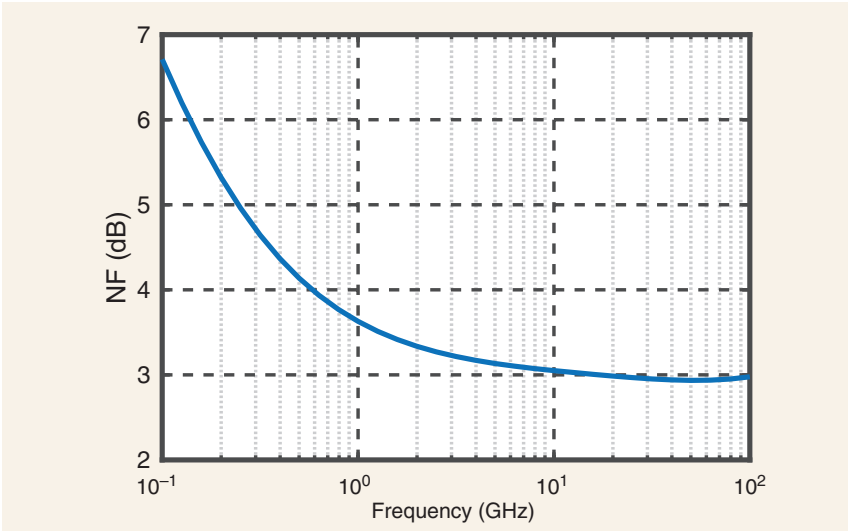

FIGURE 17: The mixer NF.

We simulate the hybrid at 56 Gb/s with $(W/L)_P = 2(W/L)_N$ and equal to 16 µm/30 nm for Inv_1 and Inv_4 and 8 µm/30 nm for the transmission gate. We also have $R_T = 30\,\Omega$, $R_1 = 600\,\Omega$, $R_2 = 1.4$ kΩ, and $R_F = 500\,\Omega$. Figure 19(a) plots V_{RX} with TX_1 in Figure 18(a) transmitting while TX_2 remains inactive. We observe a residual signal of 20 mV_{pp} along with glitches due to the timing mismatch. Next, we activate TX_2 as well, selecting its data edges to coincide with the middle of the TX_1 data eye to represent the worst case. The received eye at the output of Inv_4 is shown in Figure 19(b).

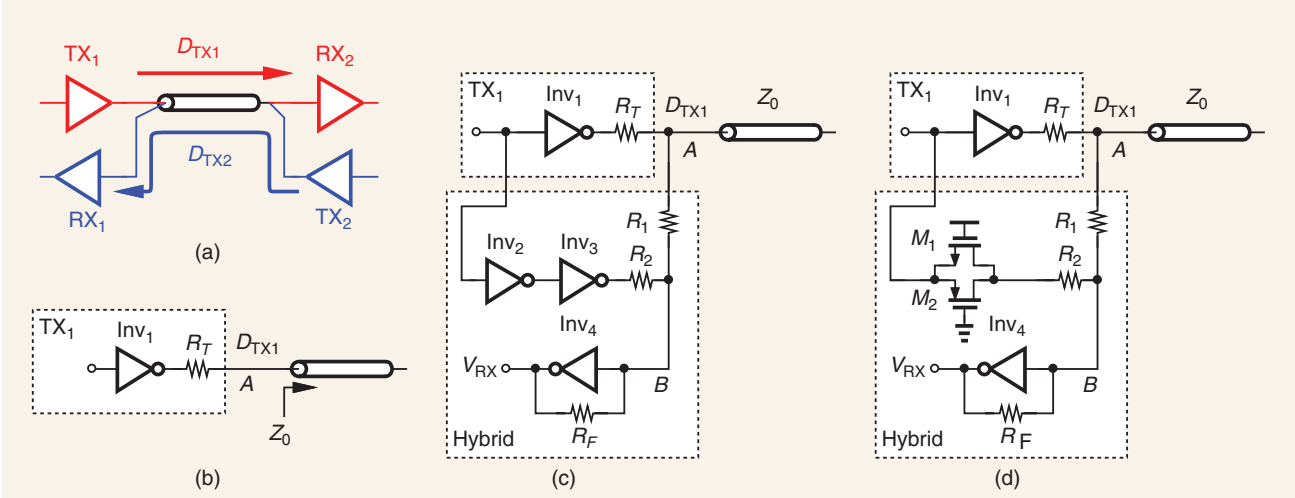

FIGURE 18: (a) A bidirectional data transfer, (b) a simple driver, (c) the addition of a hybrid, and (d) use of a transmission gate instead of inverters.

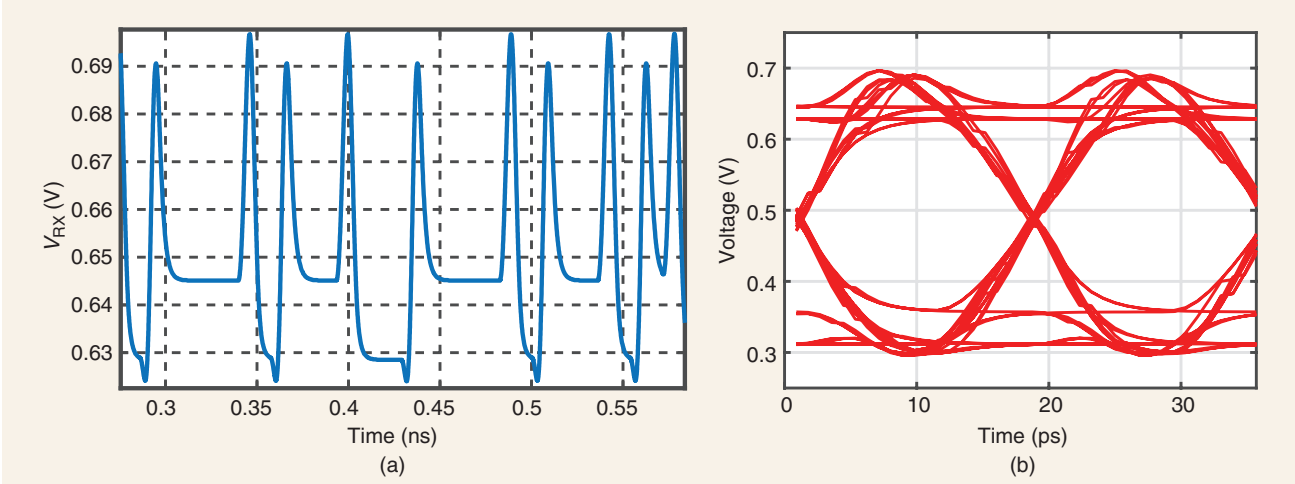

FIGURE 19: The hybrid output with TX_2 (a) inactive or (b) active.

(continued on p. 28)

combination of the binary-weighted and thermometric-weighted delay lines can achieve relatively higher frequencies while maintaining a large range and having a minimal DNL. Yet the problem of area is still coupled to the lowest frequency of operation, which results in a large area for lower frequency support, with the added problem of DNL while switching between coarse and fine sections of the delay line. This is a result of a PVT mismatch between the coarse section and the fine section of the delay line.

Closing Remarks

In today's advanced microelectronic systems, chiplet architectures are becoming increasingly prevalent. Die-to-die interfaces will continue to incur overheads, and mitigation of these overheads will rely on optimizing timing and synchronization circuits, like the DLL. There continues to be research in the area of fully synthesizable DLLs so that the overheads associated with using them in die-to-die interconnects are minimized [11]. Moving to a fully synthesizable regime can improve productivity, decrease time to market, and mitigate long validation cycles.

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Appendix Related Articles

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THE ANALOG MIND *(continued from p. 17)*

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