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EECS 141: FALL 99 —MIDTERM 1

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:

$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last First

GRAD/UNDERGRAD	

Problem 1:

Problem 2:

Problem 3:

Total	

PROBLEM 1: Transient Response

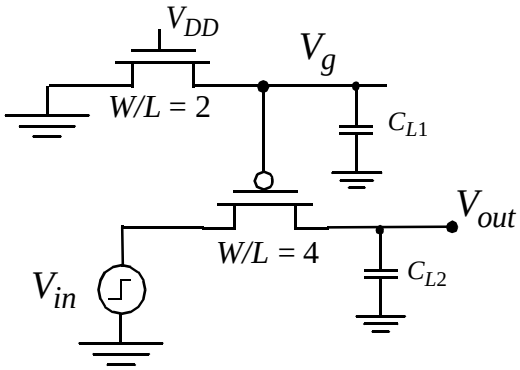

FIG. 1 Digital circuit

Consider the circuit of FIG. 1. Use the transistor parameters indicated on the first page of the midterm, with one modification. For both PMOS and NMOS, assume that $\gamma = 0$. $\boldsymbol{V_{DD} = 2.4\ V}$. $C_{L1} = C_{L2} = 20$ fF. Leakage effects should not be considered in this question.

a. Assume that the initial voltage on $V_{out} = 0$. A step from 0 to V_{DD} is applied at the input. Determine the final voltage at V_{out}.

$\boldsymbol{V_{out}}$ **(final) =**

b. Subsequently, a negative step (from V_{DD} to 0 V) is applied at the input. Determine again the final voltage at V_{out}.

$\boldsymbol{V_{out}}$ **(final) =**

c. Determine the propagation delay between input and output for the latter (negative going) transition. Derive first the equivalent resistance of the PMOS transistor over the interval of interest. To make your life easier, we have precomputed a number of currents through the transistor over a number of port values - pick the closest match.

Table 1: PMOS Currents

V_{GS}	V_{DS}	I_D
-1.0 V	< -0.6 V	-21.6 μA
-1.2 V	< -0.8 V	-38.4 μA
-1.4 V	< -1 V	-60 μA
-1.6 V	< -1 V	-84 μA
-1.8 V	< -1 V	-108 μA
-2.0 V	< -1 V	-132 μA
-2.2 V	< -1 V	-156 μA
-2.4 V	< -1 V	-180 μA

R_{eq} =

$t_{p(\text{for } Vin \text{ going from } VDD \rightarrow 0)}$=

d. Determine the energy consumed in the transistors during that transition.

$E_{\text{(for } Vin \text{ going from } VDD \rightarrow 0)} =$

PROBLEM 2: CMOS Inverter DC Characteristics

Consider the CMOS inverter from FIG. 2.a, implemented in 0.25µm CMOS technology with minimum device channel lengths.

a. If the NMOS transistor has channel width W_n and the PMOS transistor has channel width, W_p, label the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes:

A: W_n = 5µm, W_p = 5µm

B: W_n = 1µm, W_p = 5µm

C: W_n = 5µm, W_p = 1µm

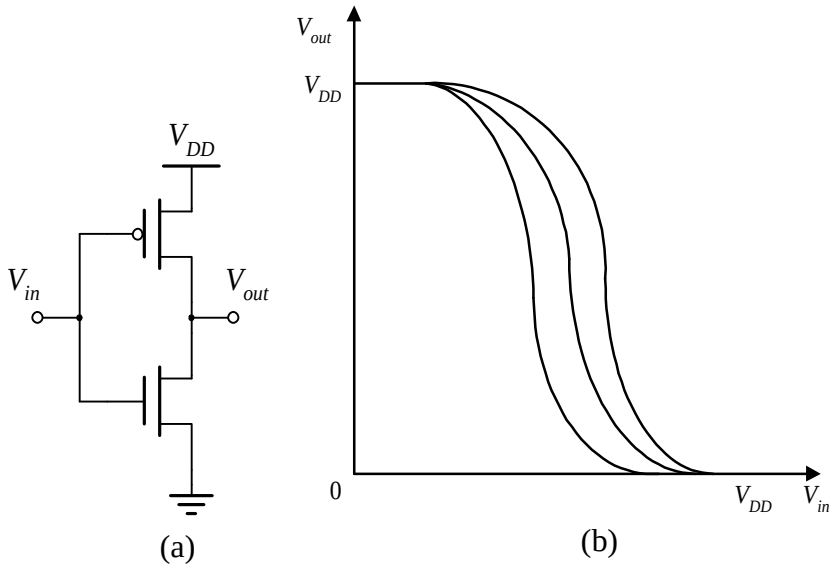

FIG. 2 CMOS inverter and Voltage Transfer Characteristics

b. A CMOS inverter with supply voltage V_{DD1} = 2V, has to interface to a second CMOS inverter with V_{DD2} = 2.5V supply, as shown in FIG. 3.

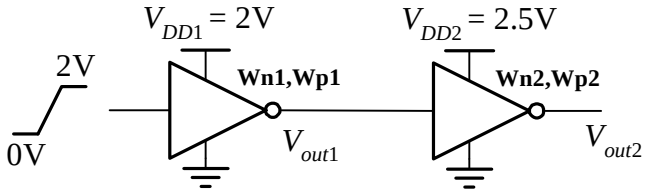

FIG. 3 Cascaded inverters

The transistor widths of the second inverter W_{n2}, W_{p2}, should be determined to assure reliable interfacing, since the high output voltage level of the first inverter is V_{OH1} = 2V. If W_{n2} = 5µm, determine the value of W_{p2}, such that these inverters are interfaced with maximum and symmetrical noise margins.

W_{p2} =

c) The inverter from FIG. 4. has W_n = 1 µm and W_p = 2.5µm. V_{DD} = 2.5V.

Determine the value of V_{OH}? Assume that the PMOS transistor operates in triode region and that $\left|\frac{V_{DS}}{2}\right| << |V_{GS} - V_T|$. Determine also the value of V_{OL}.

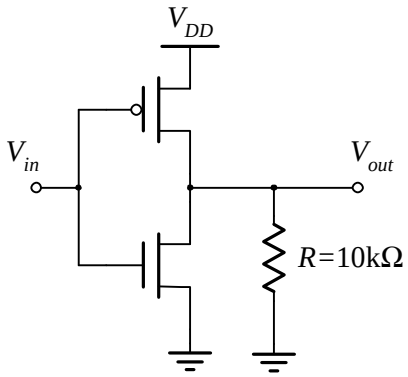

FIG. 4 CMOS inverter with resistive load

V_{OH} =
V_{OL} =

Problem 3: Device parameters

An enthusiastic student of ee143 received a batch of newly processed silicon wafers and took the following set of measurements of a single MOS transistor.

Table 2: Measured device parameters

Measurement number	VGS (V)	VDS (V)	VSB (V)	ID (μA)	Operation Region?
1	-2.5	-2.5	0	-84.375	
2	1	1	0	0.0	
3	-0.7	-0.8	0	-1.04	
4	-2.0	-2.5	0	-56.25	
5	-2.5	-2.5	-1	-72.0	
6	-2.5	-1.5	0	-80.625	
7	-2.5	-0.8	0	-66.56	

Our goal is to derive the important device parameters from these data points. As the measured transistor is processed in a deep-submciron technology, the '**unified model**' holds. From the material constants, we also could determine that the saturation voltage V_{DSAT} equals -1V. You may also assume that $-2\Phi_F = -0.6V$.

NOTE: The parameter values tabulated on the first page do NOT hold for this problem.

NOTE: For questions b. to d., indicate each time which of the measurements you used to derive the answer (e.g measurements #3 and #6). State also your assumptions.

a. Is the measured transistor a PMOS or an NMOS device? Explain your answer.

NMOS ☐

PMOS ☐

b. Determine the value of V_{T0}.

V_{T0}=

c. Determine γ.

γ=

d. Determine λ.

λ=

e. Given the obtained answers, determine for each of the measurements the operation region of the transistor (choose from *cutoff, resistive, saturated, and velocity saturated*). Annotate your finding in the right-most column of the Table above.