This is a simple tutorial on using the new Cadence version 6 for creating an inverter. This tutorial covers setting up the environment, and designing a simple inverter from beginning to LVS clean.

First, log into a computer in the lab. This can be done sitting in the lab, using VNC, or through ssh. If using ssh, use the -Y option to ensure all the X11 comes back to your computer.

Start a terminal session. (Right click, and select terminal)

items you should type are shown in a `typewriter` style font

the stylized ↙ indicates the carriage return or the enter key

Create a directory for the 45nm sub-threshold work. I'll use st45 for sub-threshold forty five.

```
mkdir st45↙
```

Change to that directory

```
cd st45↙
```

copy the setup data to the directory (there is a period typed before the carriage return)

```
cp ~morris/setup45/* .↙
```

Check and see the correct files were copied

```
ls↙
```

You should get

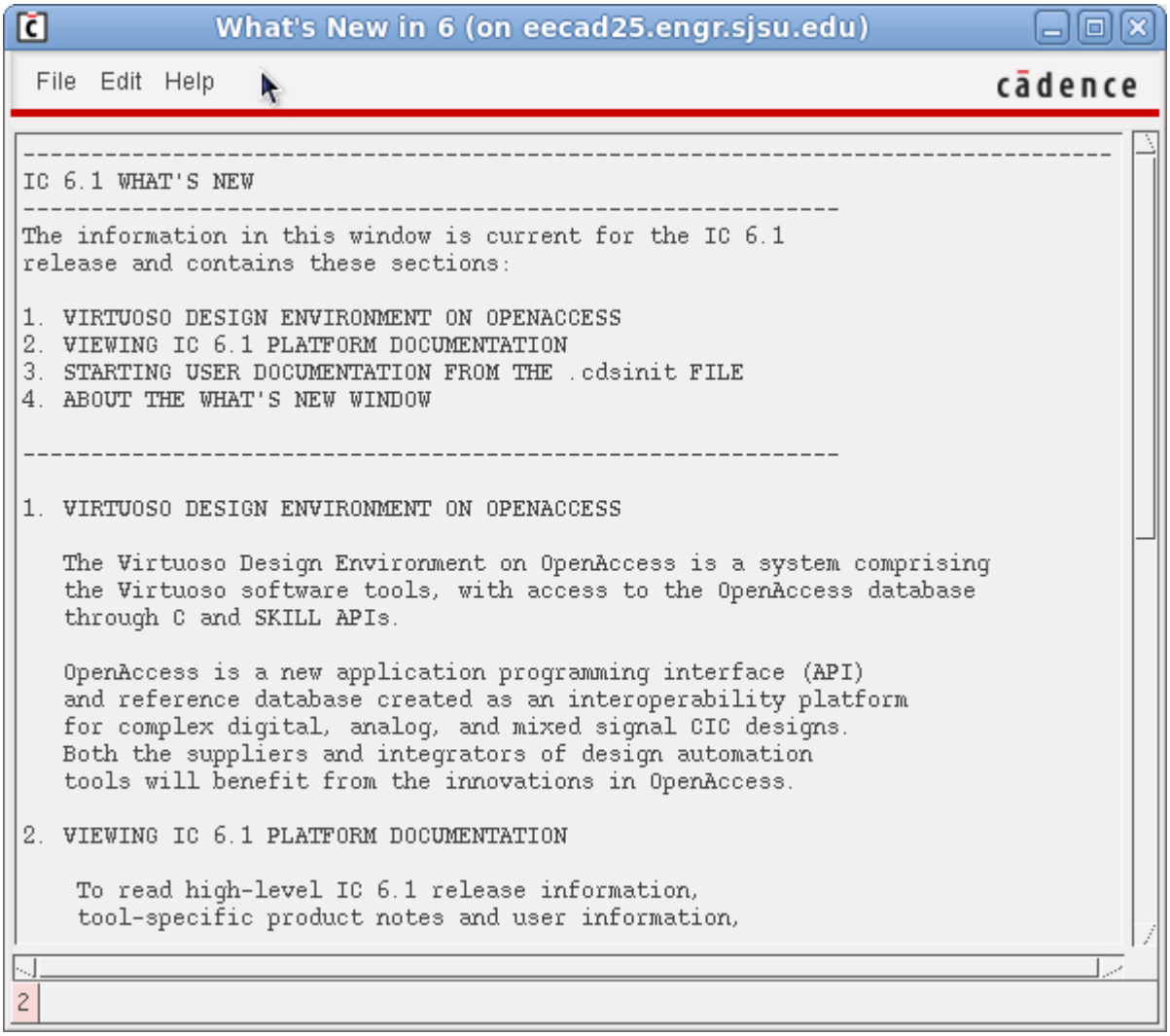
cds.lib s45 s45.csh

start Cadence 6.1 with the following command

```
./s45↙
```

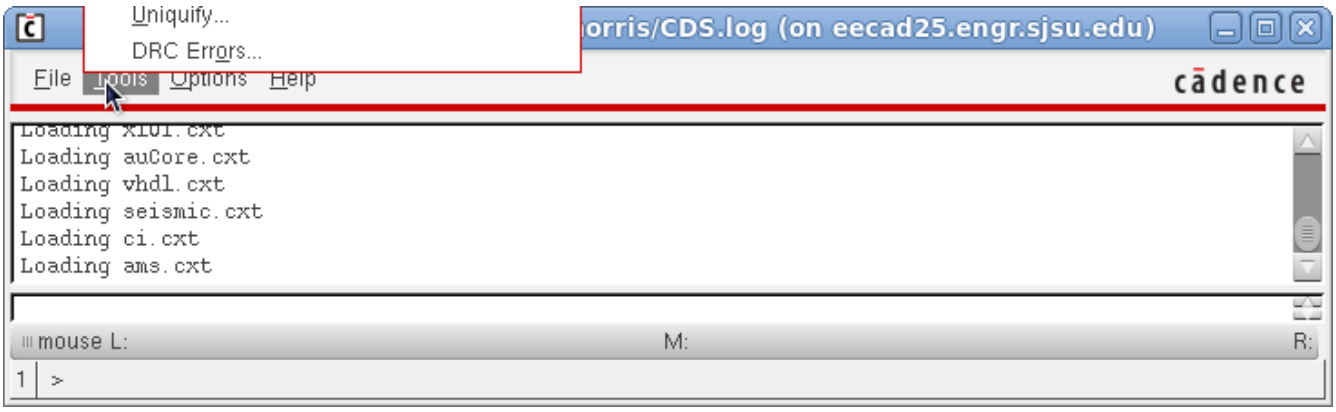
This will set up an environment and start the cadence system

It may take a while, but you should eventually see:

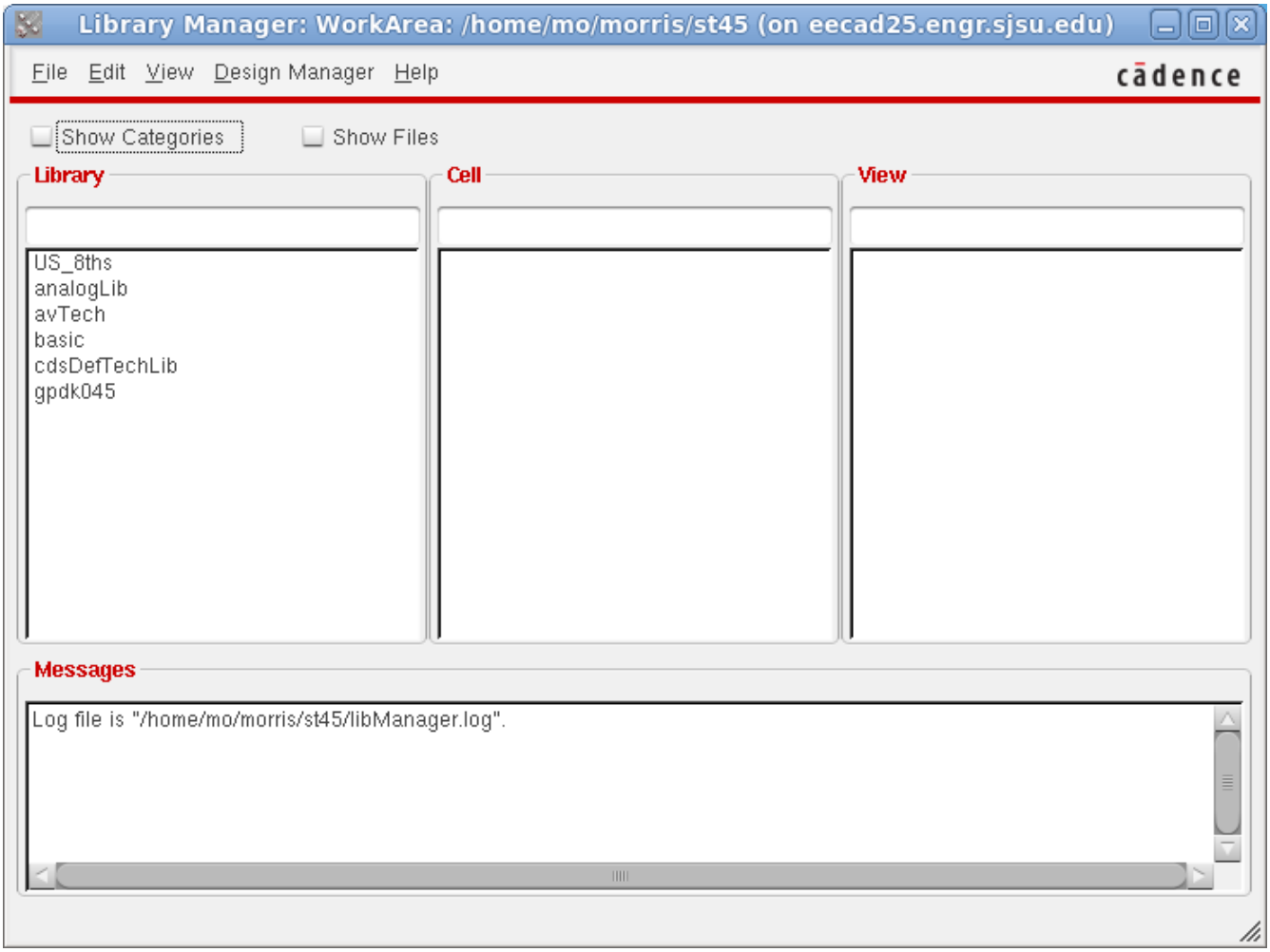


Close this window by clicking on <file> and then <close>

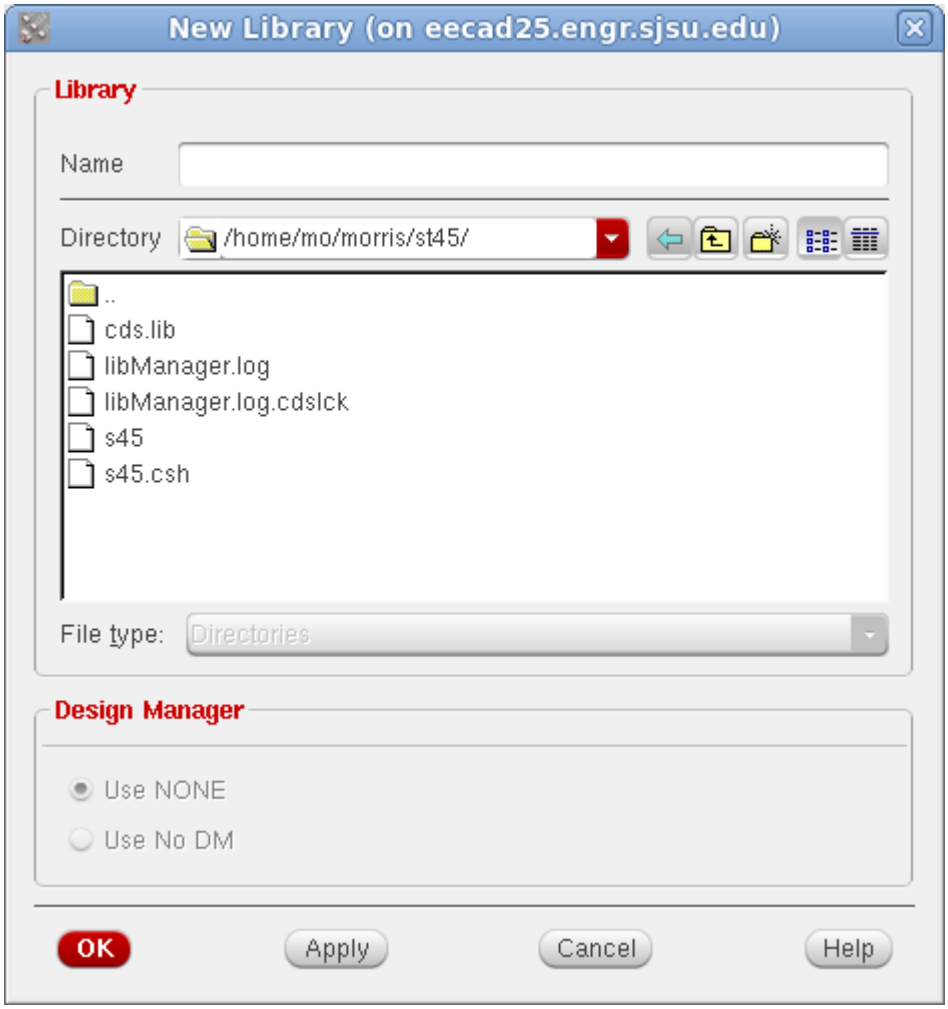
You should now have the basic virtuoso window (Looks about like the old ICFB window)



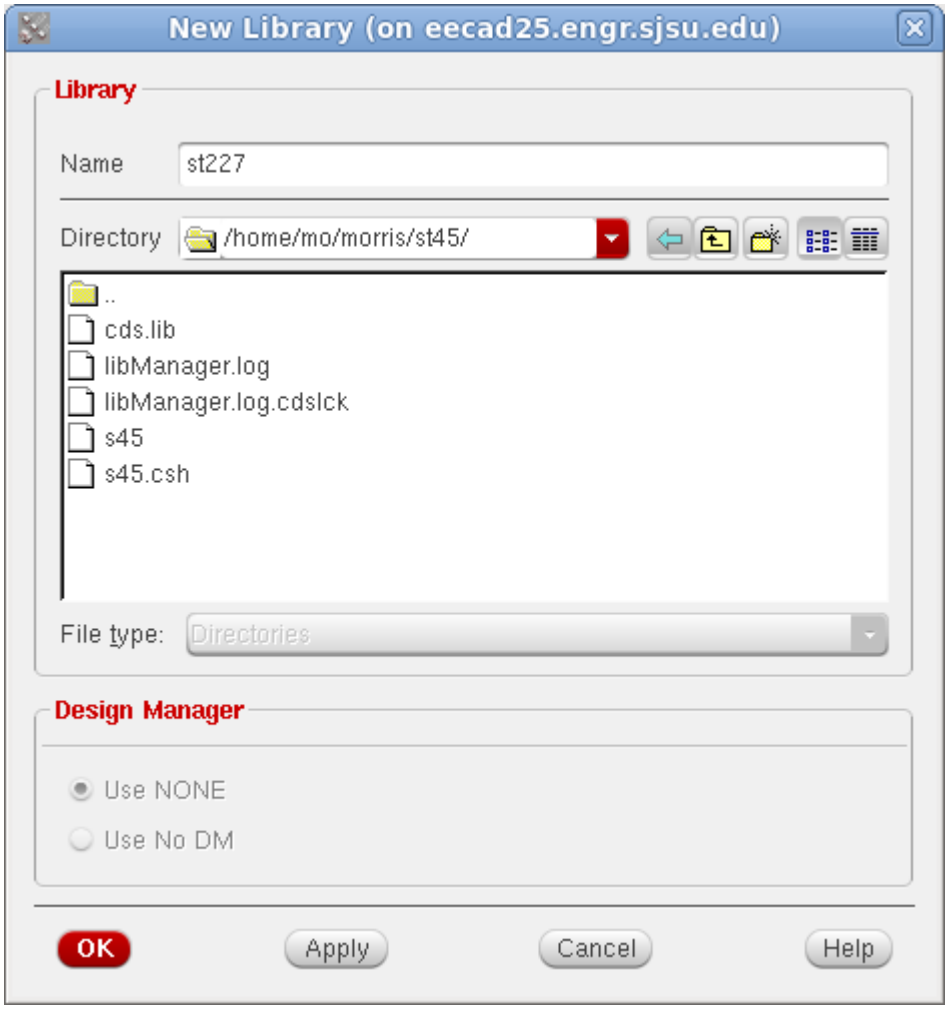
Click on <tools> and then <library manager> to start the library manager. This came up automatically in the old system, but not in this one.



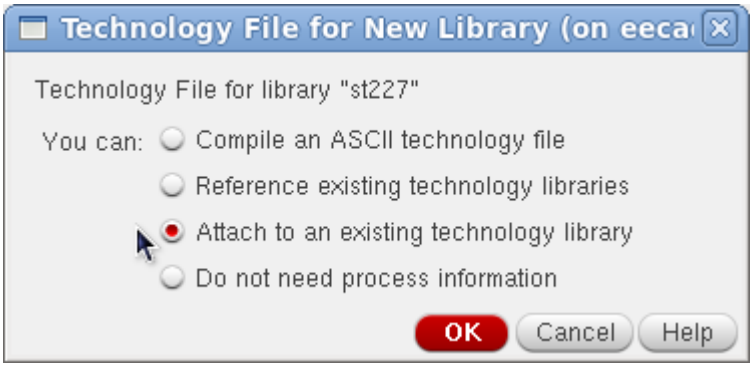
Click on <file> then cursor over to <new> then to <library> and click <library>



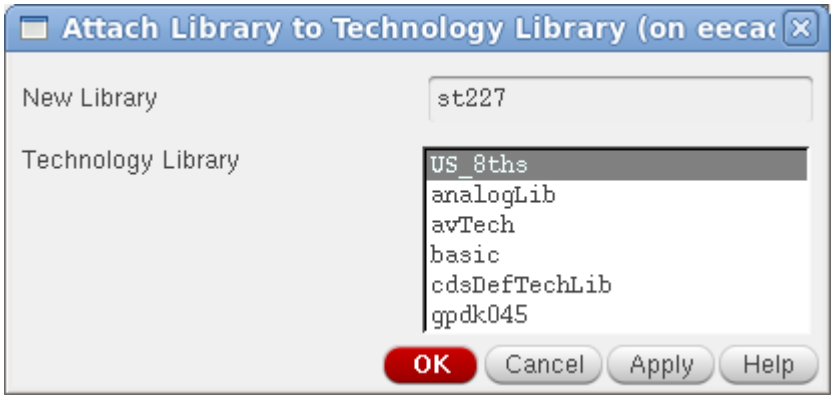
Enter the name of your library in the name field (I used st227). Note: your directory path will be different than mine.



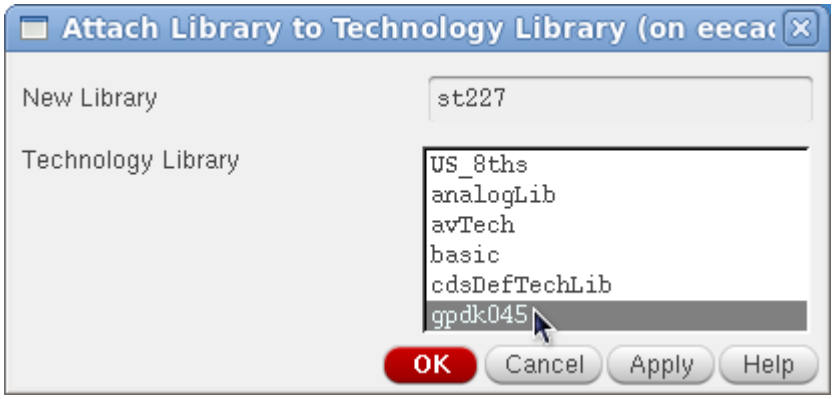
Click on OK at the bottom. You will get a small screen. It is very important that you click on "attach to an existing technology library".



Then clock OK at the bottom. A screen will pop up asking which library to select.

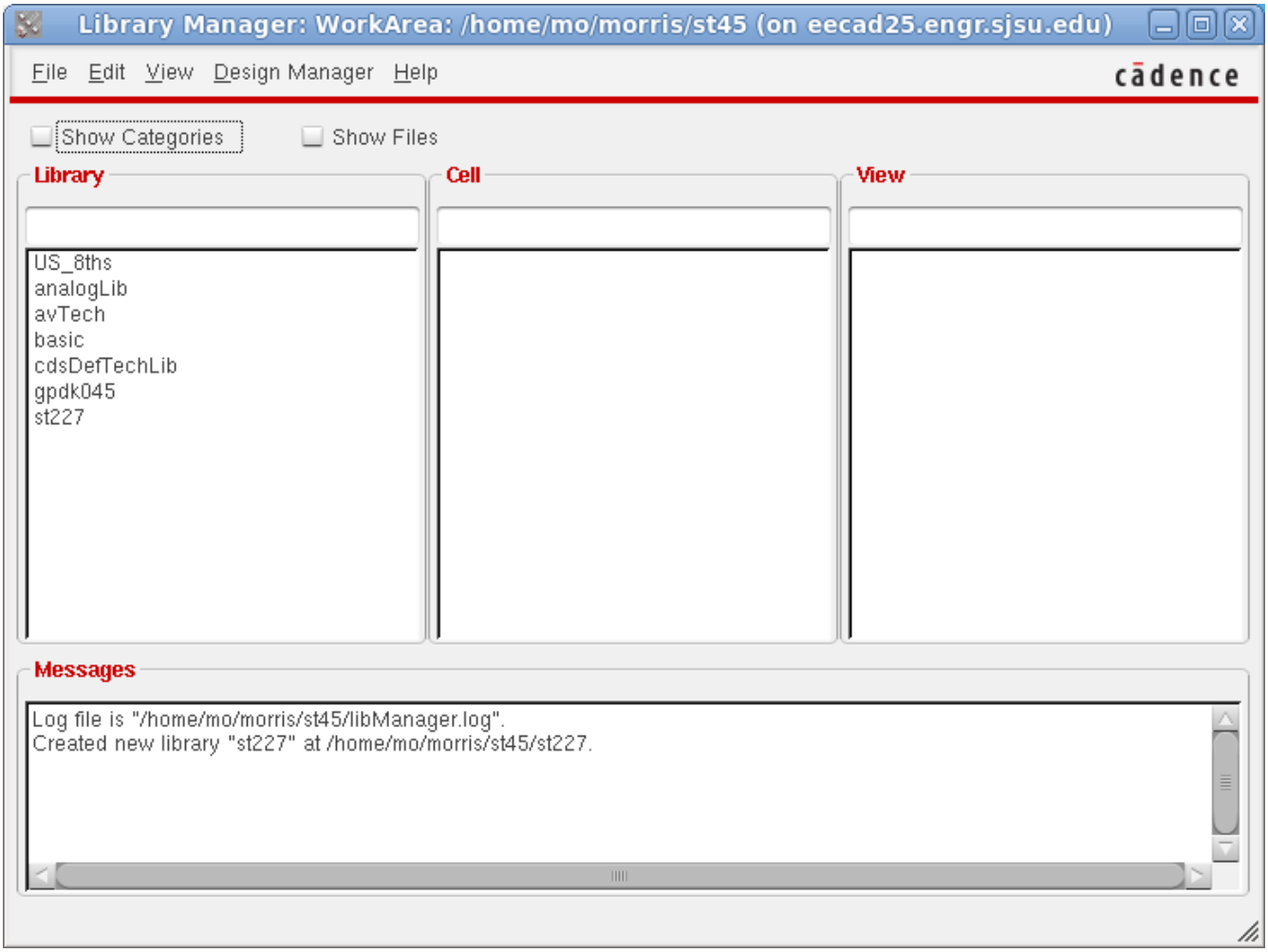


Select the gpdk045 option by clicking in the list. (If the screen is too small, you may need to scroll the list)

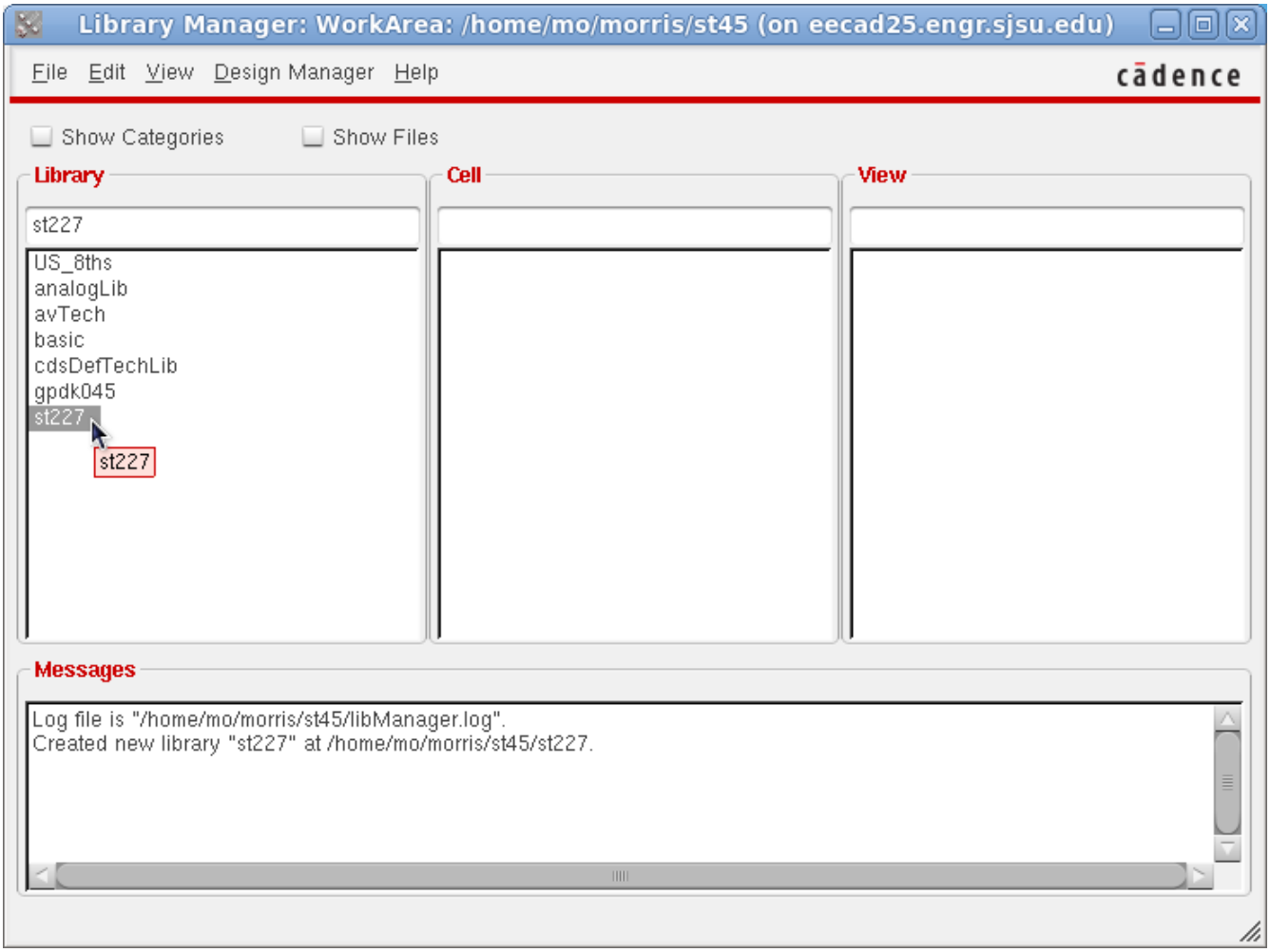


click on OK

The library manager will now show the new library



Select the new library by clicking on the name (st227 in this case)



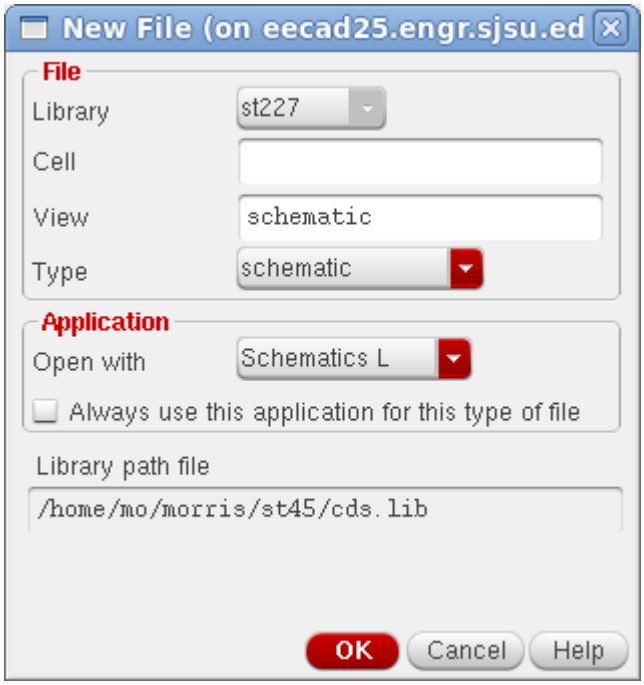
You may not get the little pink box. It appears when you leave the cursor there for a period of time.

For practice, the tutorial will now create an invertor, and walk through the steps of simulating it.

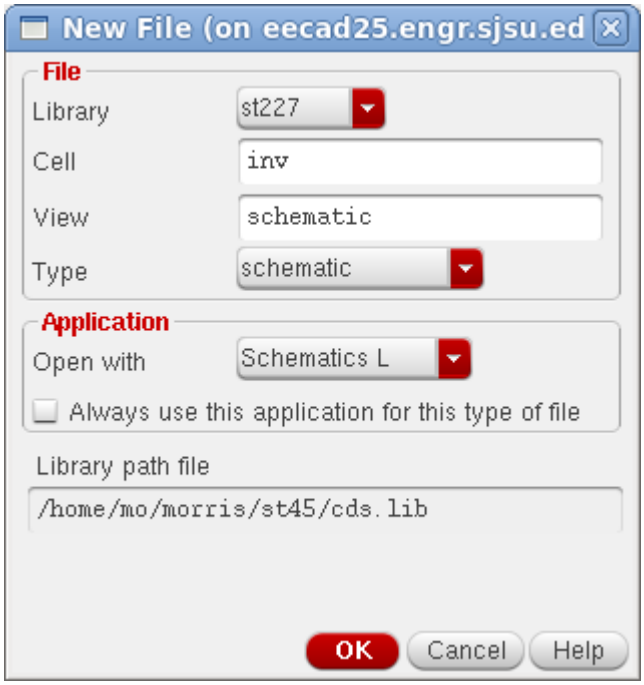
First, create the schematic.

Click on <file> then cursor over to <new> then to <cell view>

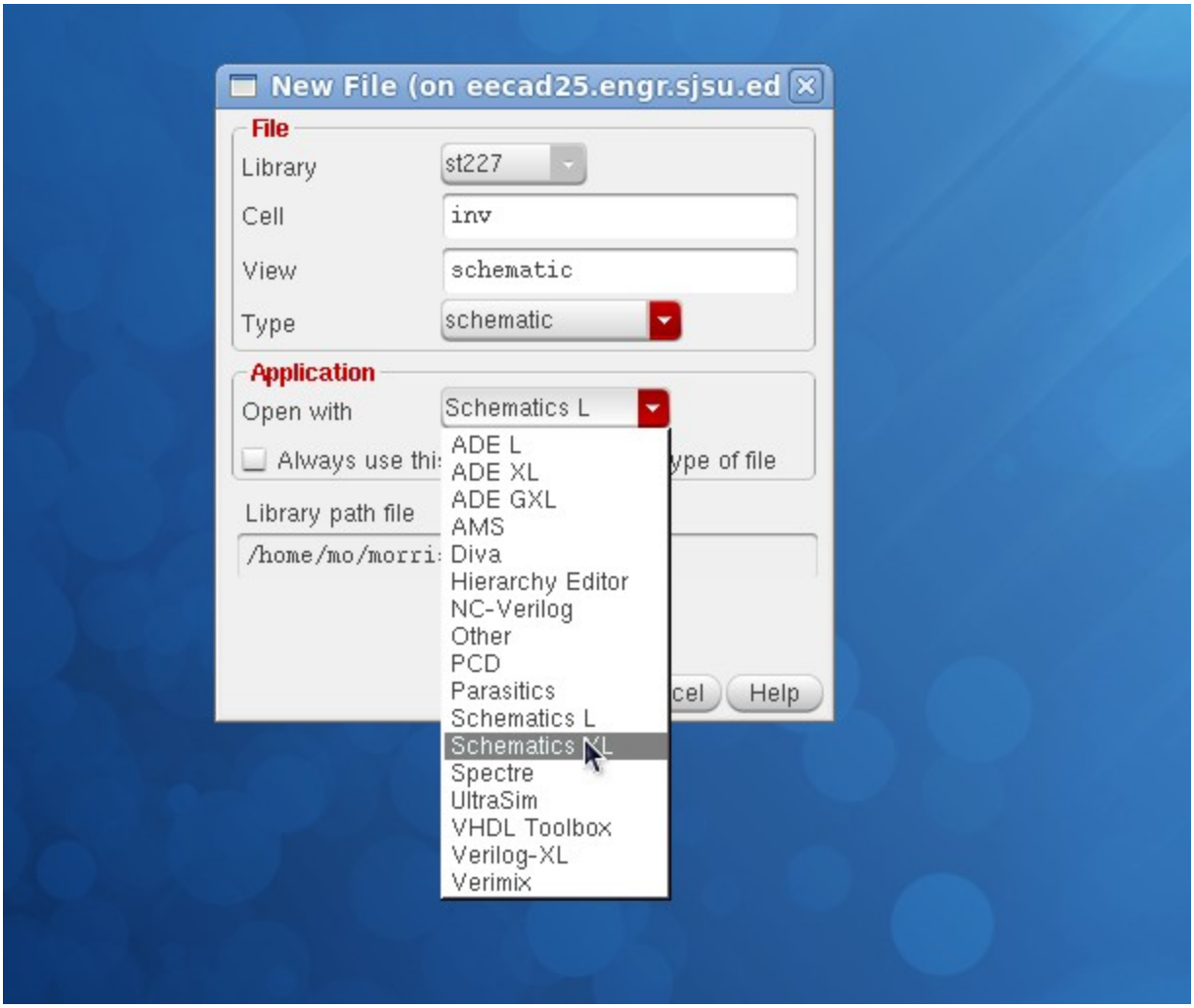
A small menu should pop up.



In the field for Cell, enter the name of the cell. “inv” is used in this case.

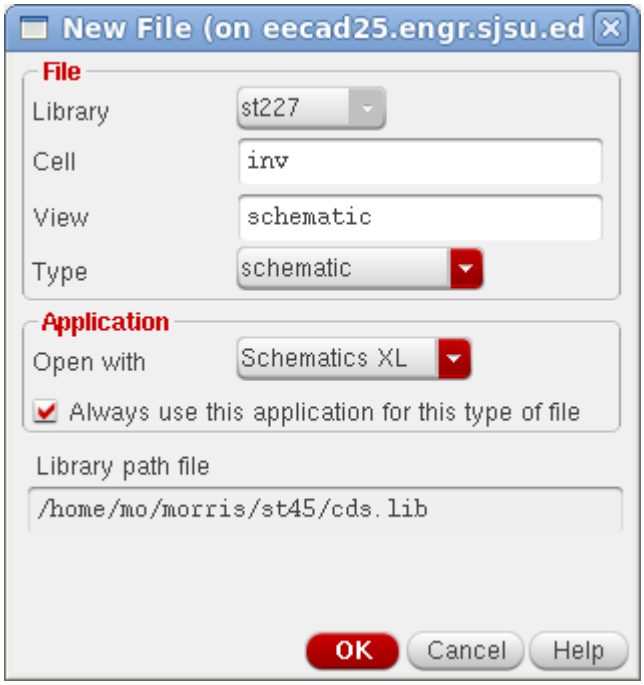


In the Application box that says “Open with” click on the red pull down arrow. Then select Schematics XL

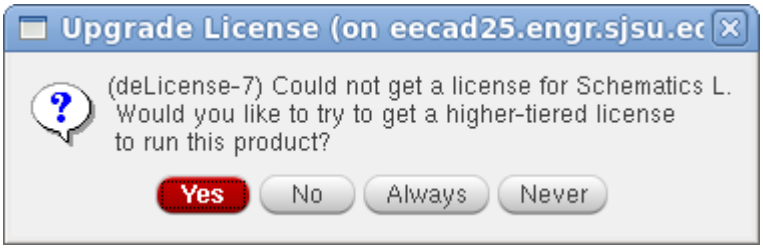


Click on the “Schematics XL”

Click on the box that says “always use this application for this type of file”

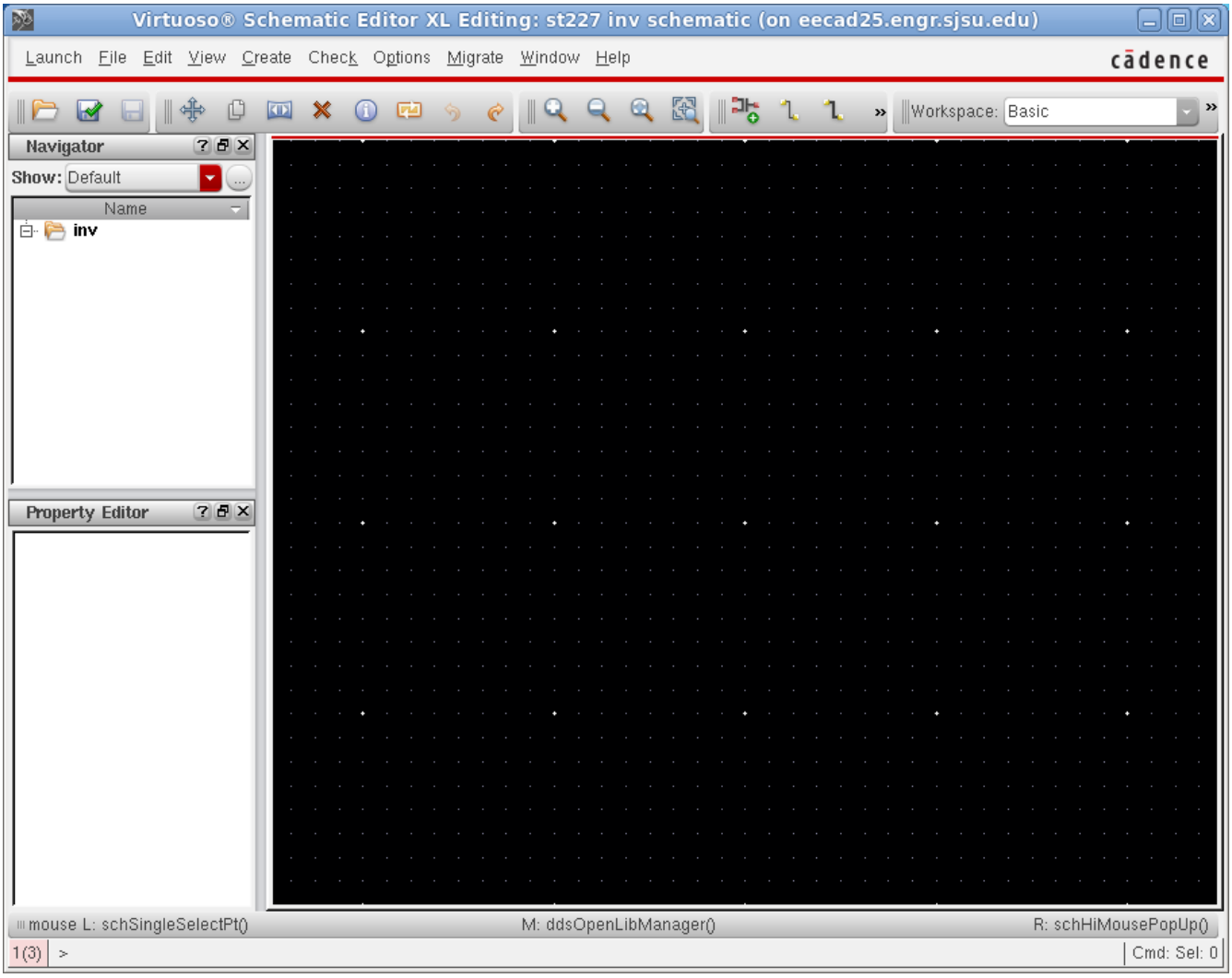


Click OK. You will often get a small window asking about a license. We are licensed for the best tools they have, and are using a mid range tool.



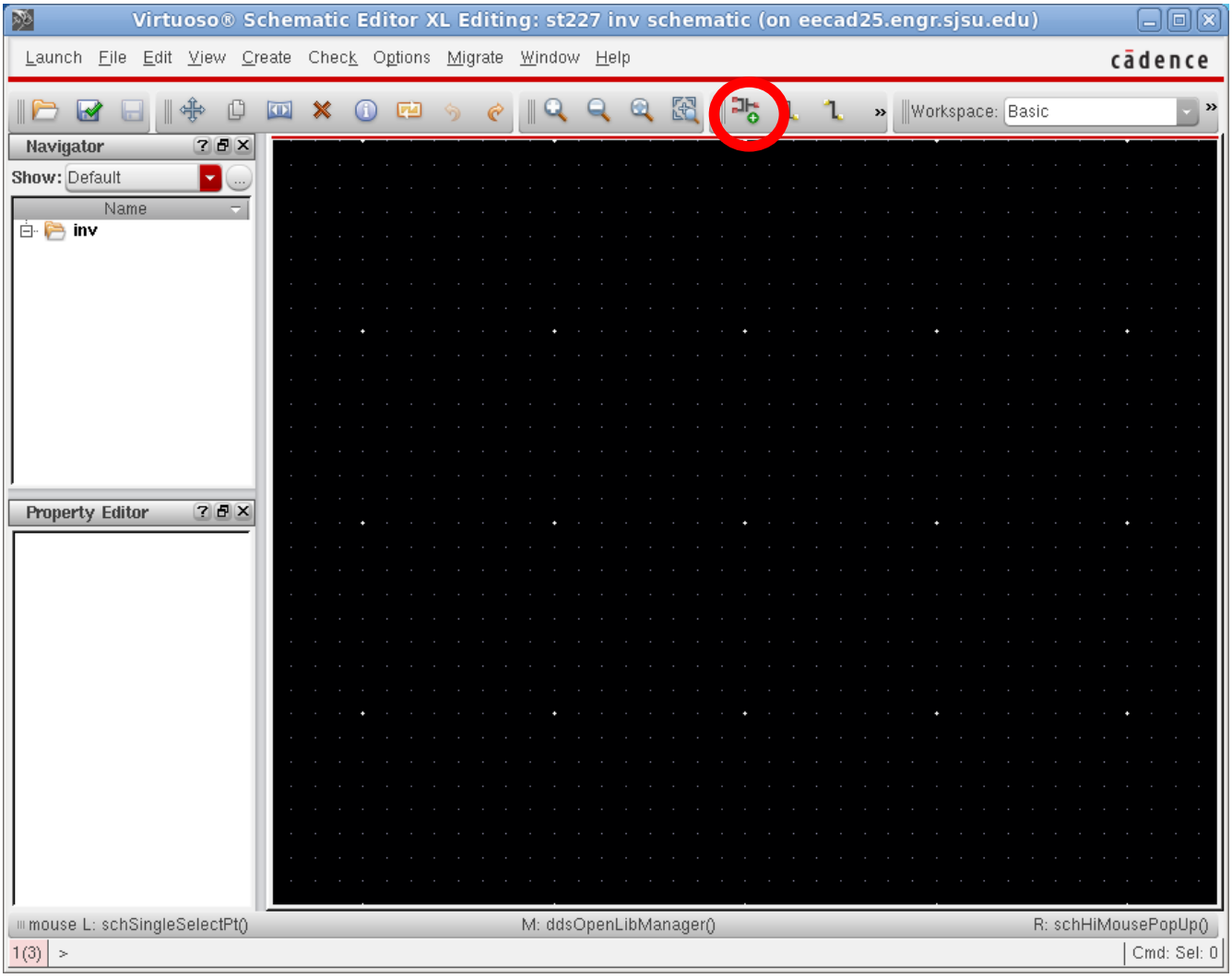
Click OK.

You should now get the schematic editing screen.

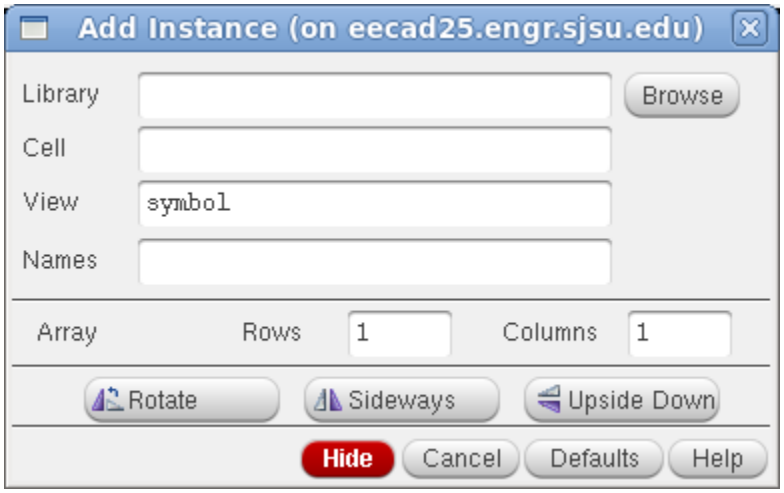


Now, the steps of making an inverter.

First, add a N transistor. Select a component by clicking on the transistor symbol. (Highlighted below with a red circle)



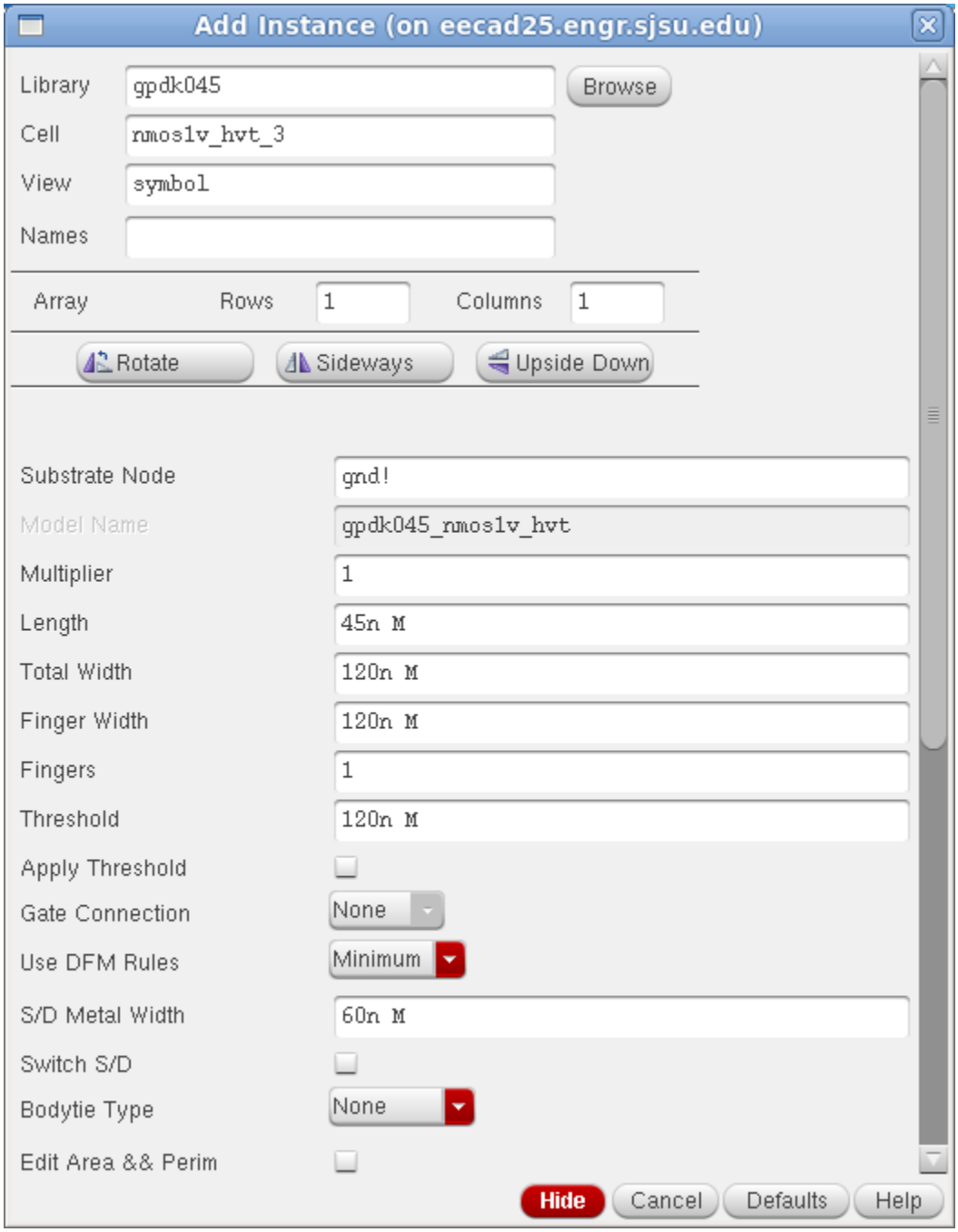
This gives a small selection screen



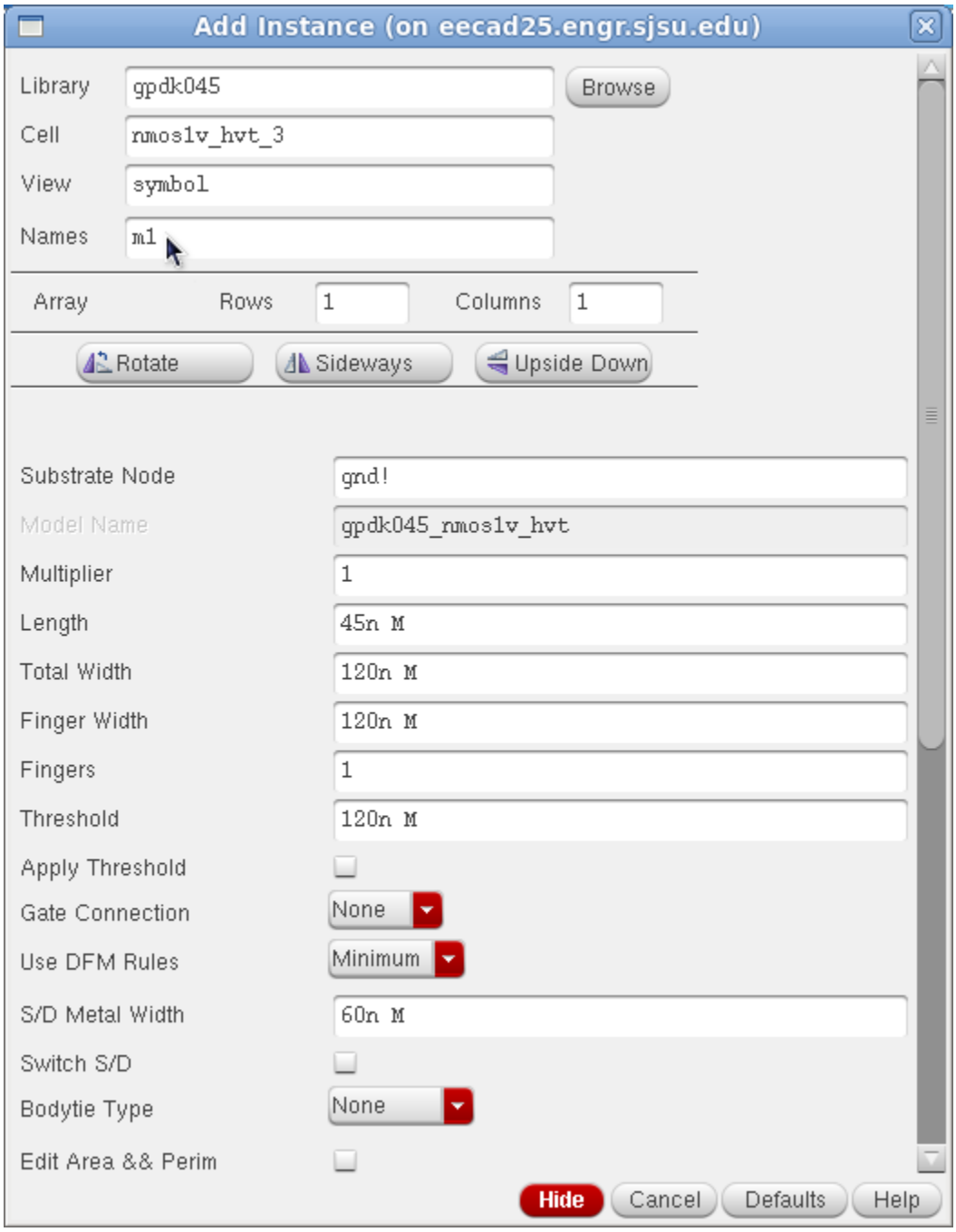
Click Browse to select the library.

Now select gpdk045, then the transistor for this inverter N transistor. In this case, a nmos 1 Volt 3 terminal transistor with a high voltage threshold (nmos1v_hvt_3). Then select the symbol for inclusion in the schematic.

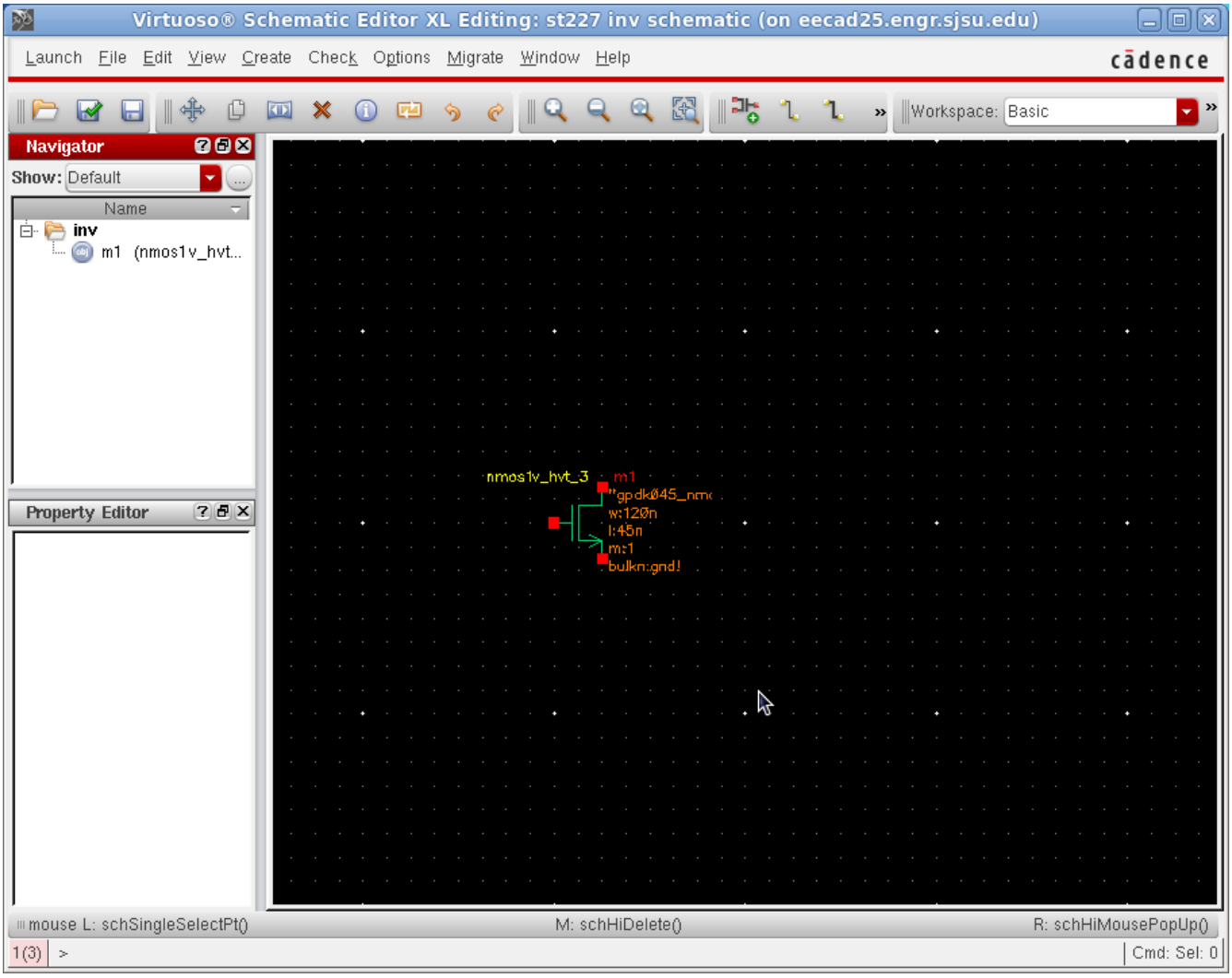
You can click close, or leave this window open. The add instance window will now appear with all the device characteristics as below.



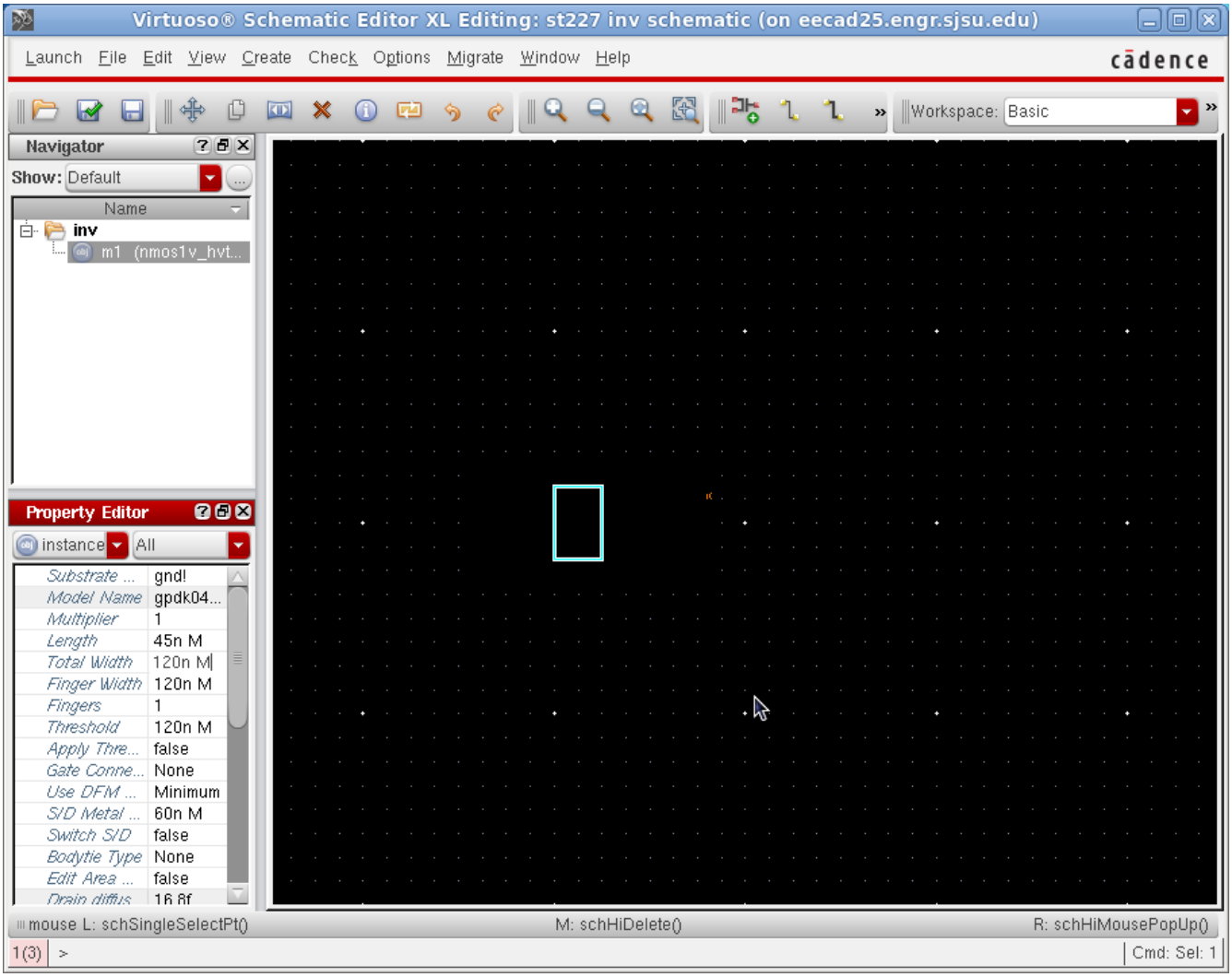
If the View doesn't say symbol, type that in. Add the name for this transistor. (I will use m1). You can change the device sizes now, or later. For this example, they will be left minimum size.



Select Hide to minimize this screen, or select the schematic page to place a transistor on the schematic. Place the transistor by clicking on the schematic screen.



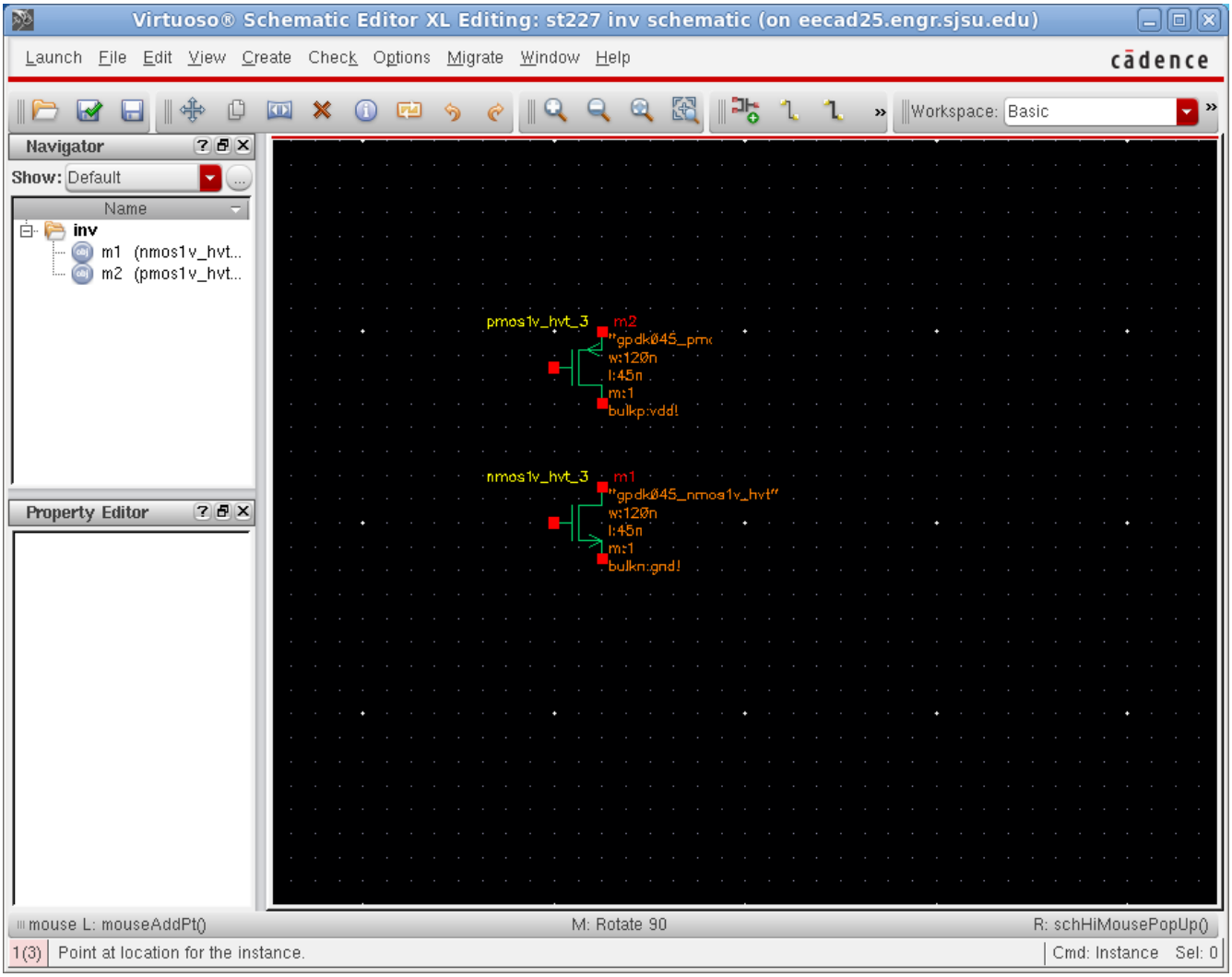
Notice the cell name appears on the left in a tree list, and the property editor is below that. You can just click on the device name in the first list, and the properties will show up in the property editor.



The device properties can be changed in the property editor. (Device sizes, names, etc).

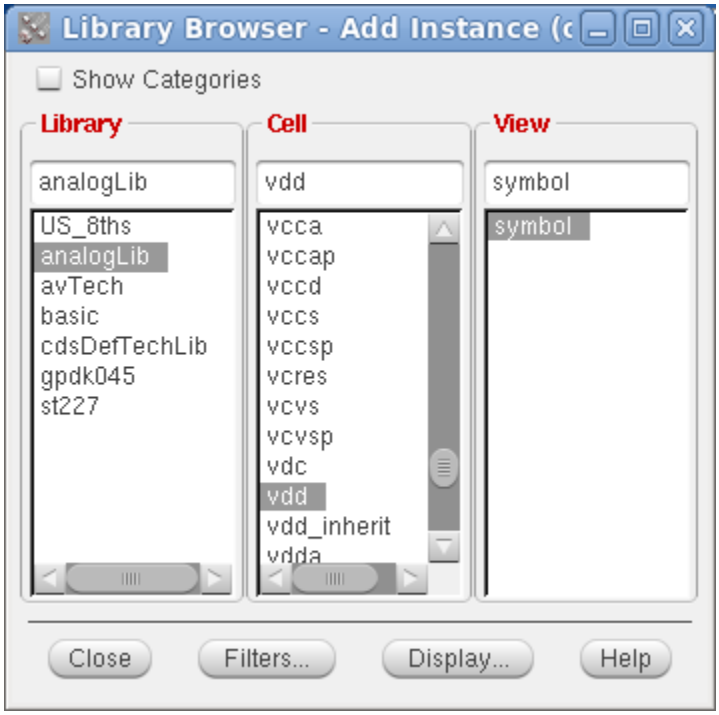
Now, add a pmos transistor.

The click by click steps are the same as for the N transistor, except select pmos1v_hvt_3, and name it m2. Place it on the schematic by clicking above the N transistor location.

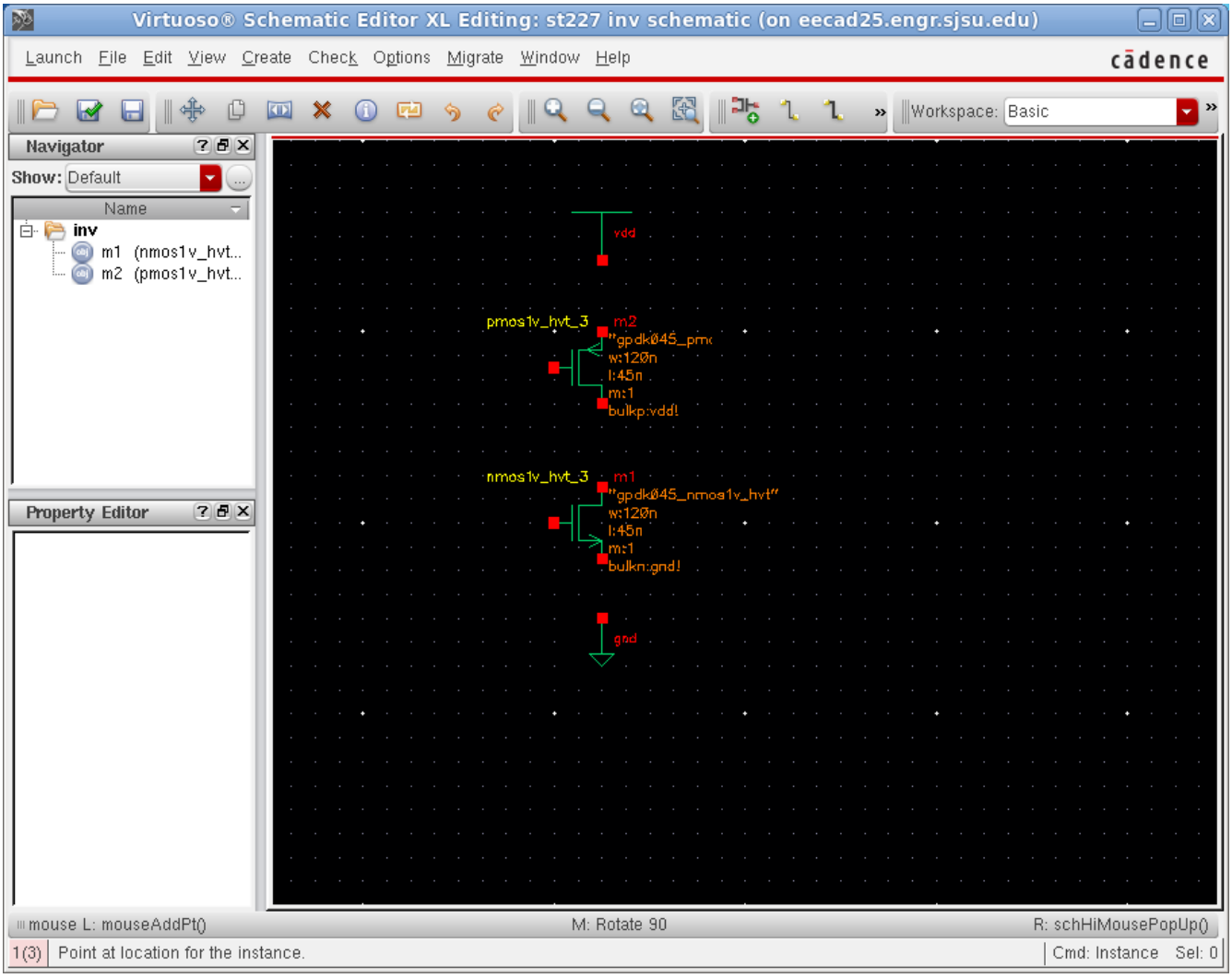


Now select a component for Vdd and Gnd. And place them on the schematic.

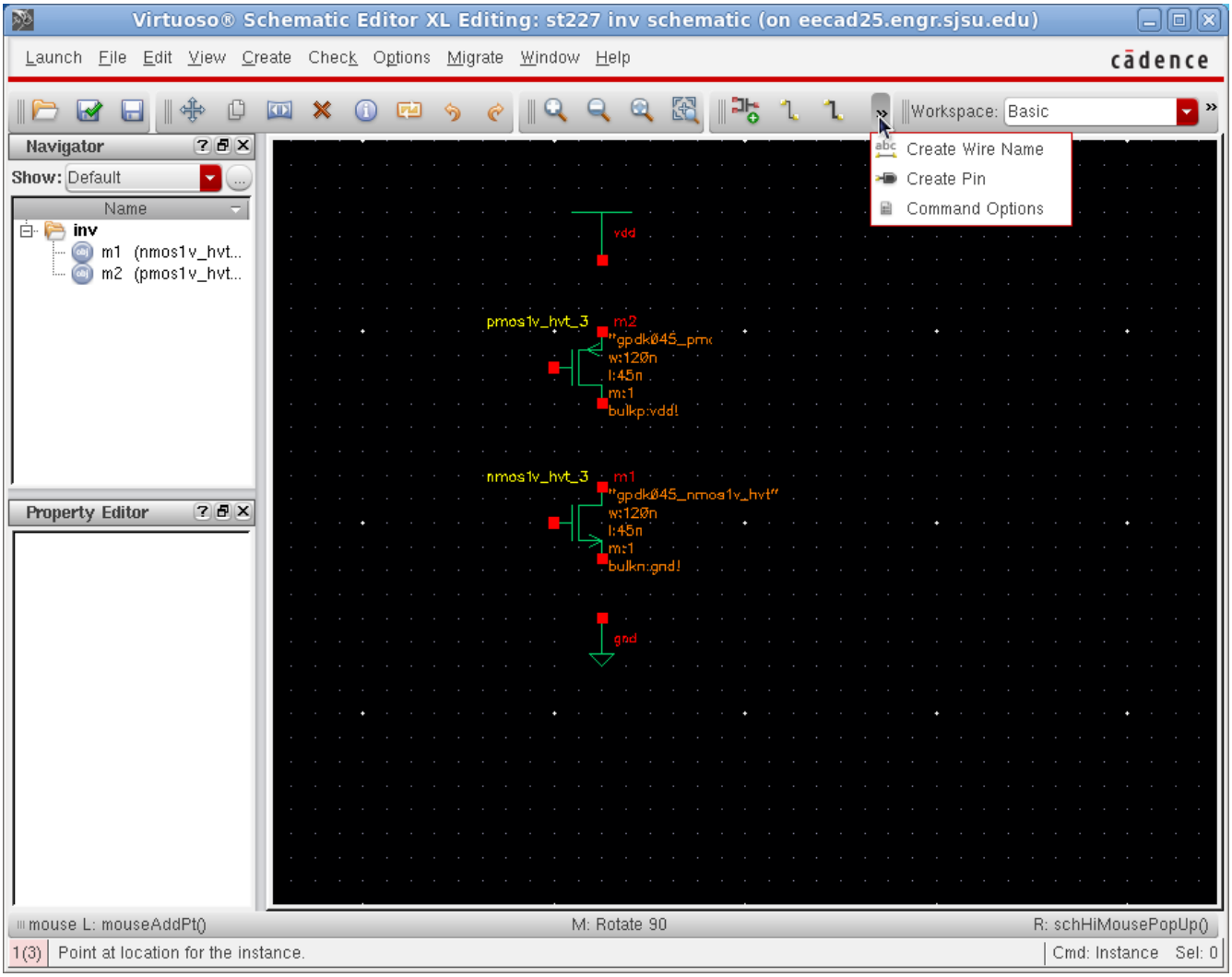
These are found in analogLib.



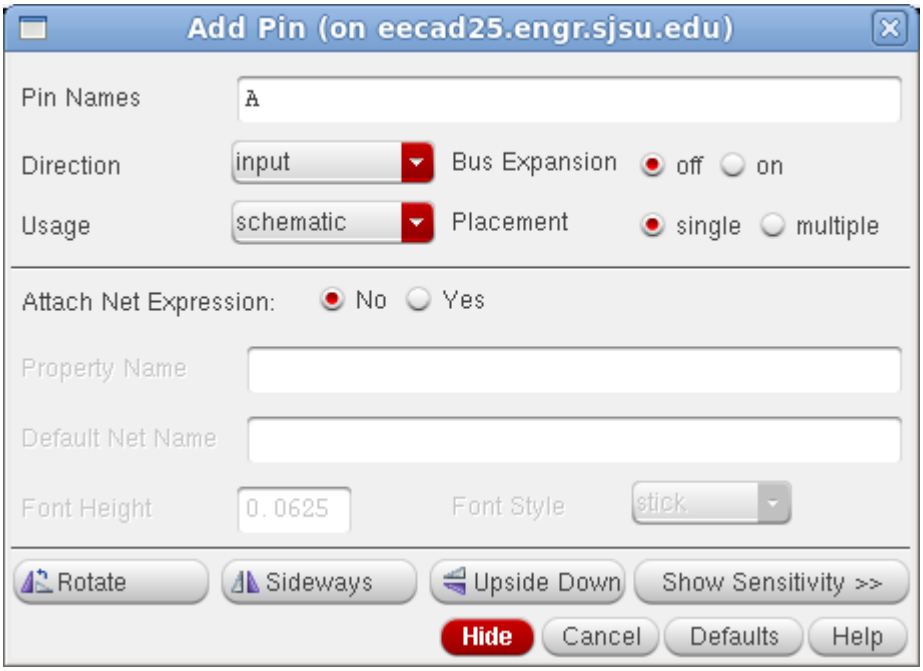
If you press close or hide, you can get the menus back by selecting the transistor schematics again. I named the symbols v1 and g1.



If not everything on a menu shows on the screen, (as in this example), you can get the rest of the menu items by clicking on the >> symbol.



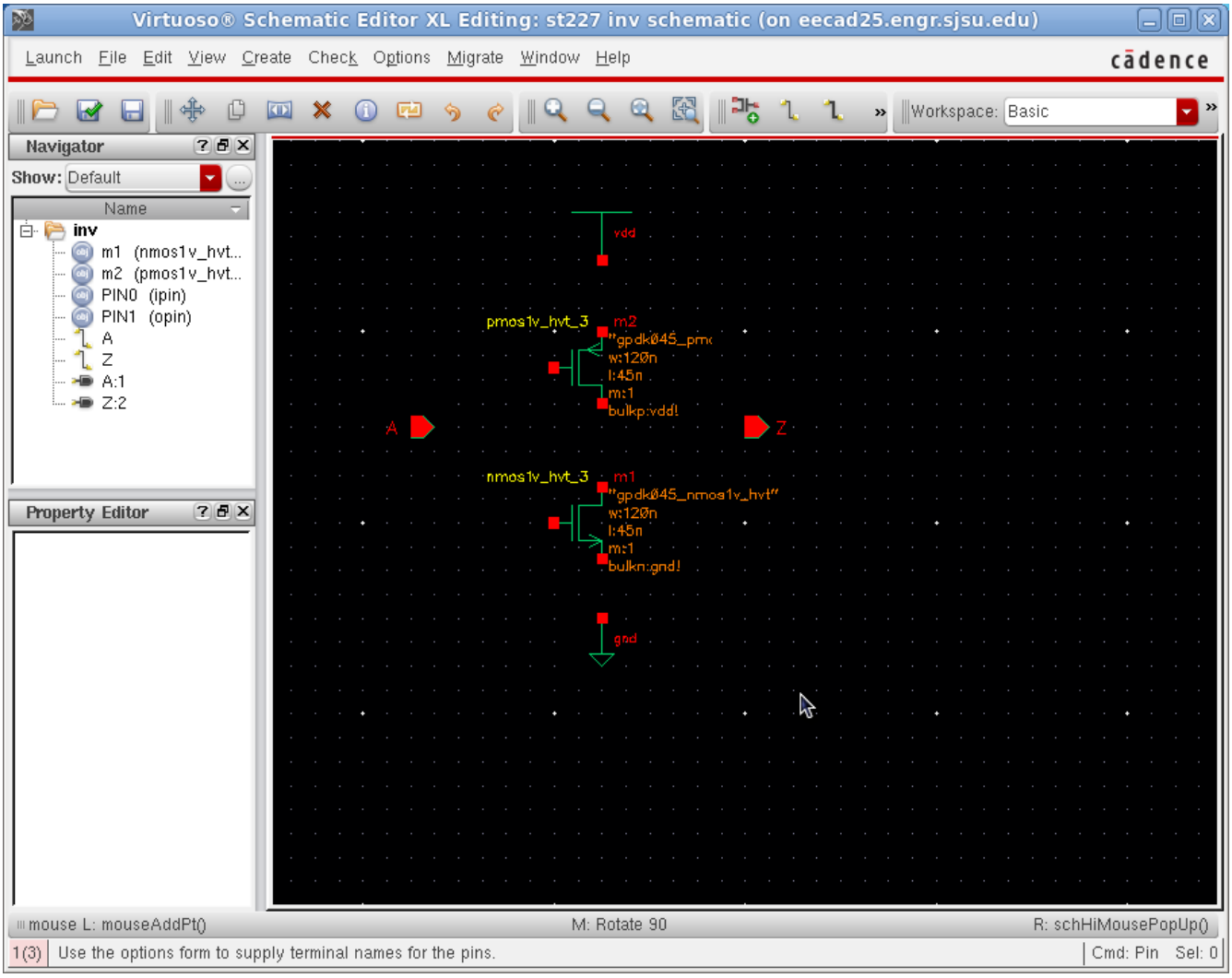
Select the symbol next to create pin. This may already be visible on your terminal, or you will need to click on the >> symbol. Alternately, you could click on the create and then pin items in the menu. The tool bars generally allow single click selection.



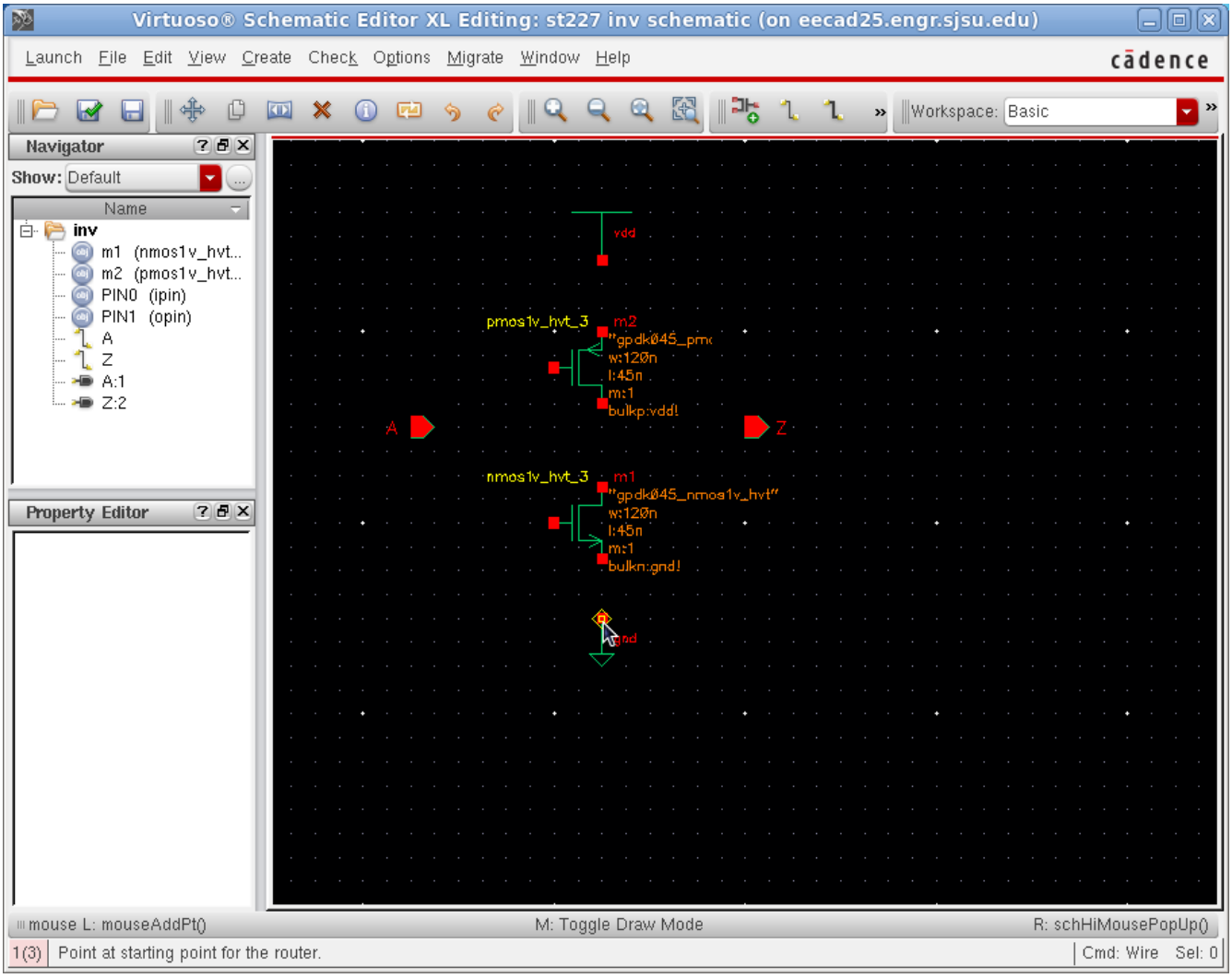
Give the pin a name, and select the desired direction. In this case upper case A for the name, and input for the direction. Upper and lower case matter in some tools and not in others in the design system. It is important to always use the same case in the names throughout the design. More than one pin of the same type can be entered. Just put spaces between the names.

If signals will be connected together as is often the case later in analog, (but not digital), then the direction should be inputoutput, not output.

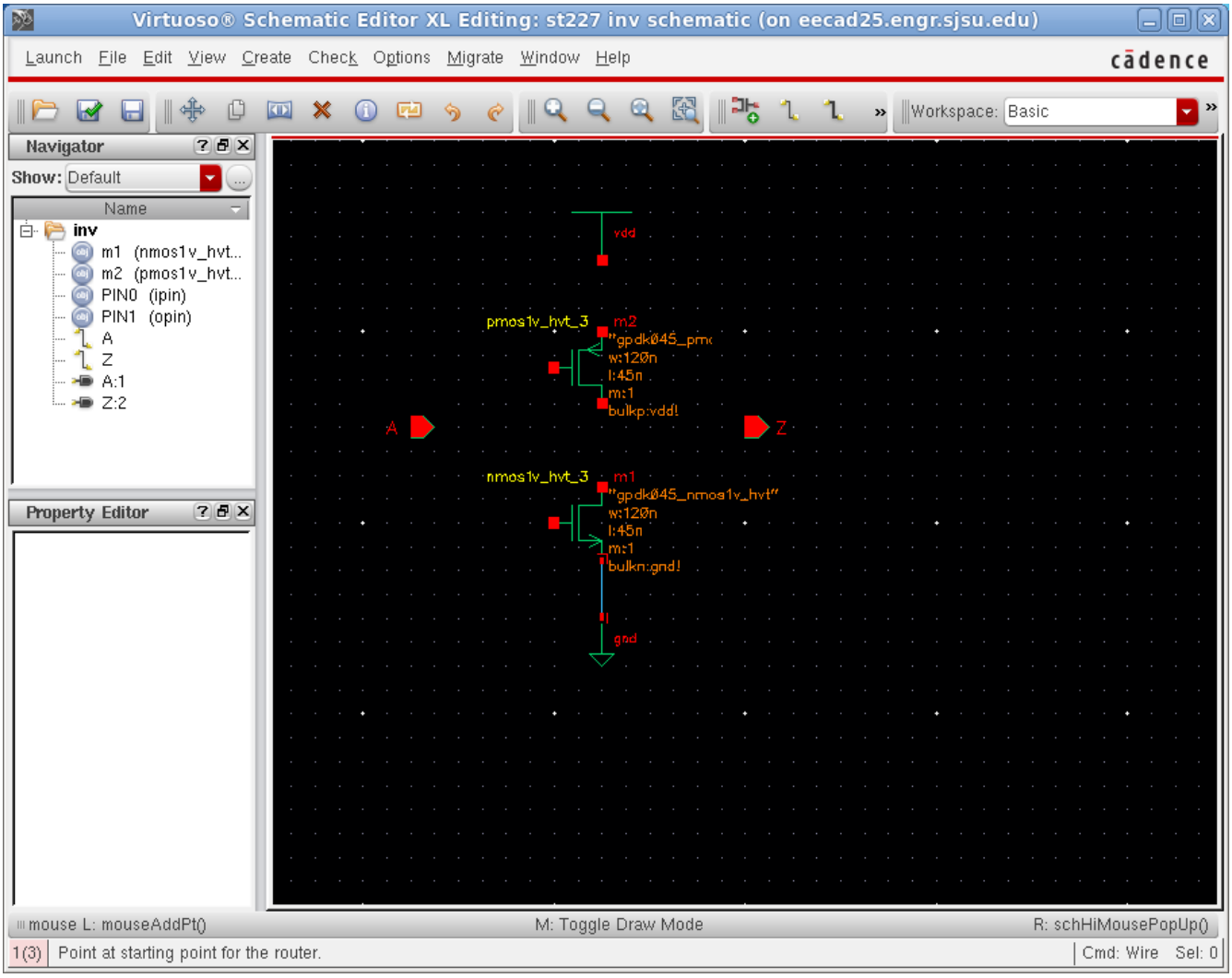
Place the pin on the schematic. Next, create an output pin called upper case Z and place it on the schematic.



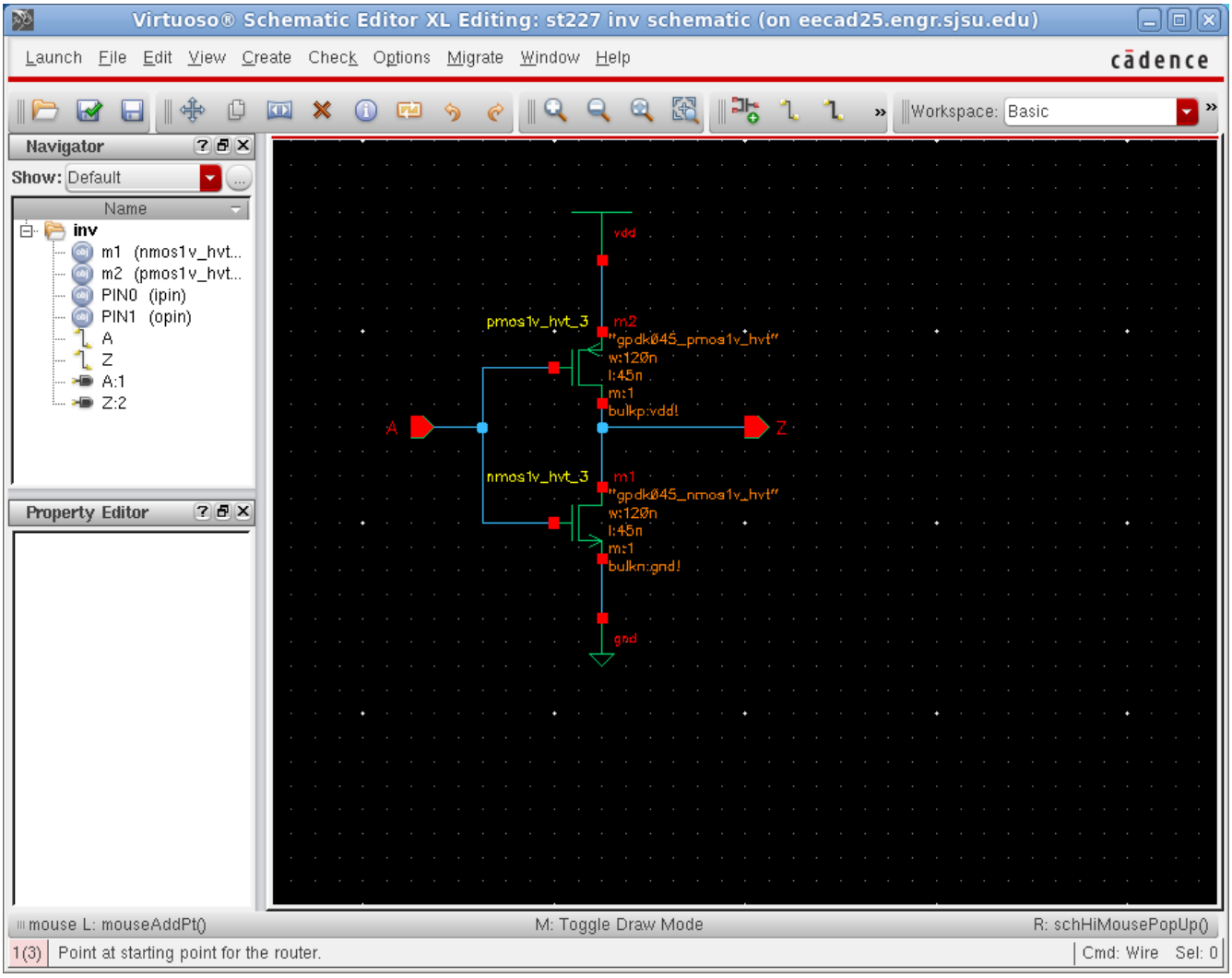
Now time to add some wire to the schematic. The single width wire is just to the right of the transistor symbol. Click on it, and then move the cursor to the first point to be wired. It should highlight with a yellow diamond.



Click, and then move the pointer to the second point and click to draw the wire.



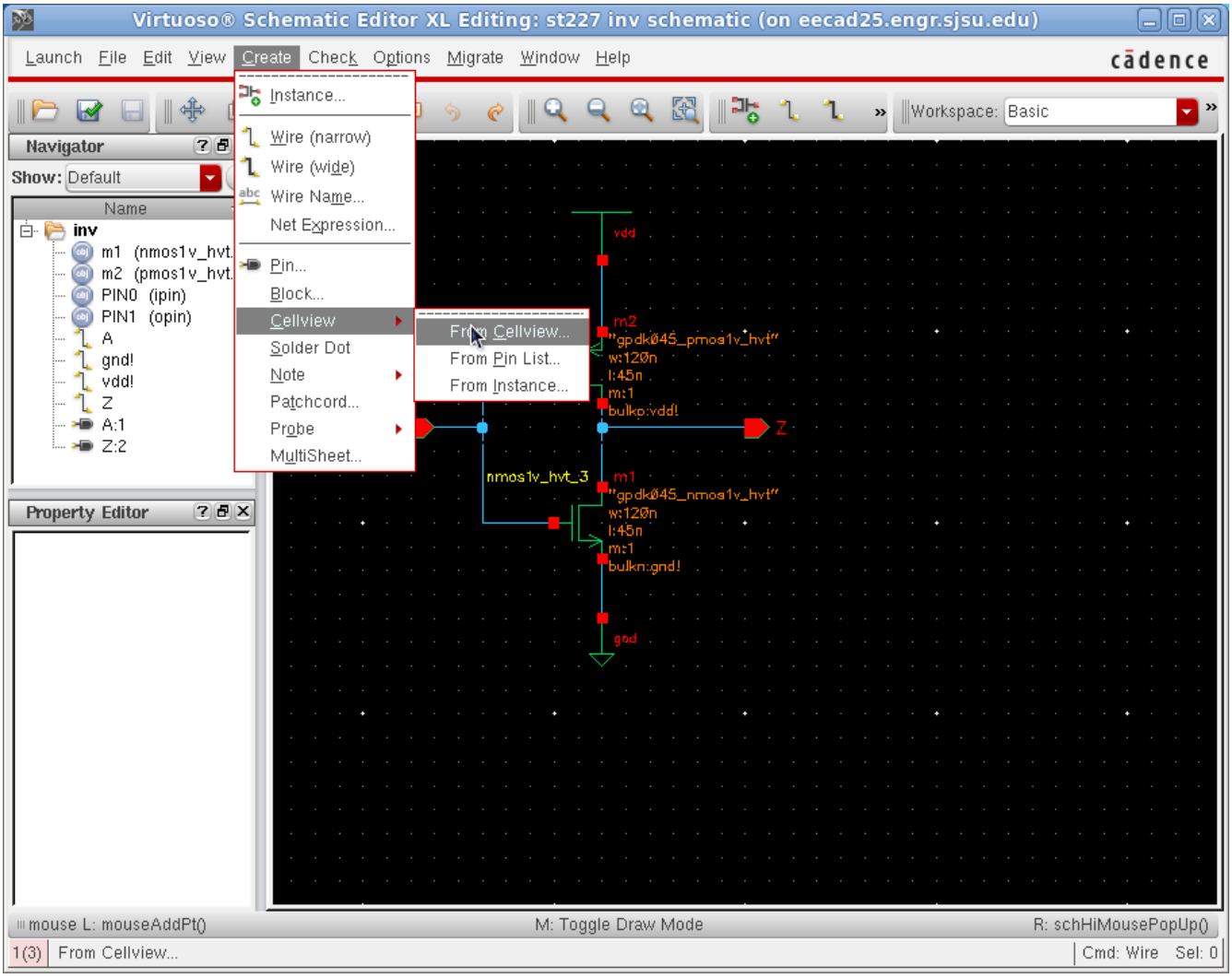
Repeat this process to wire the schematic as shown below. You man not need to click on the thin wire symbol each time as long as it is wiring mode.



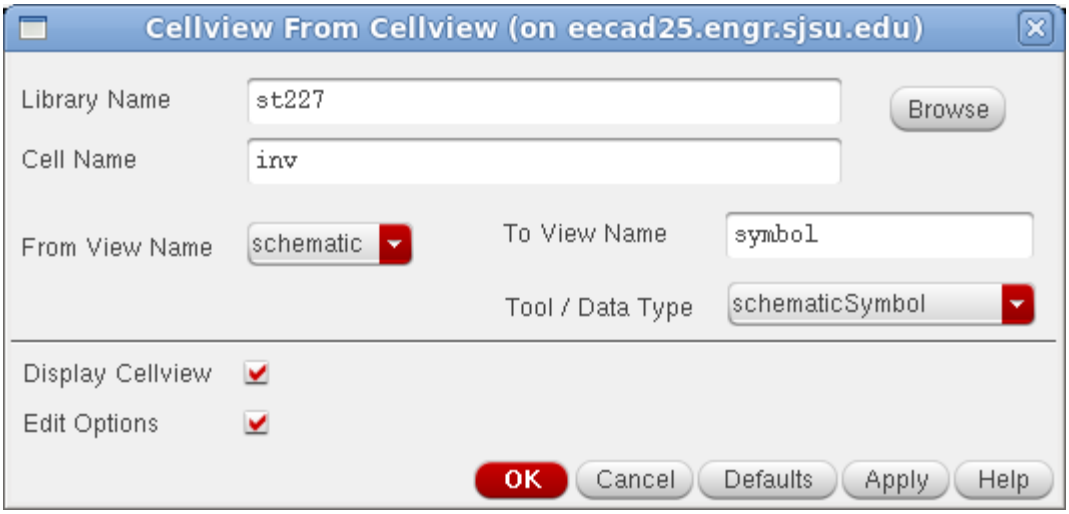
Some notes, cadence doesn't allow 4 connections at a point. If you make a mistake, then press the escape key. Click on the wire in error if any is left, and then click on edit then delete.

Now, click on the floppy disk with the green arrow. This will check the design and save it. If all goes well, it should work.

For simulation, a symbol will be created of the inverter. Click on <create> then cursor over to <cellview> then click on <from cellview>

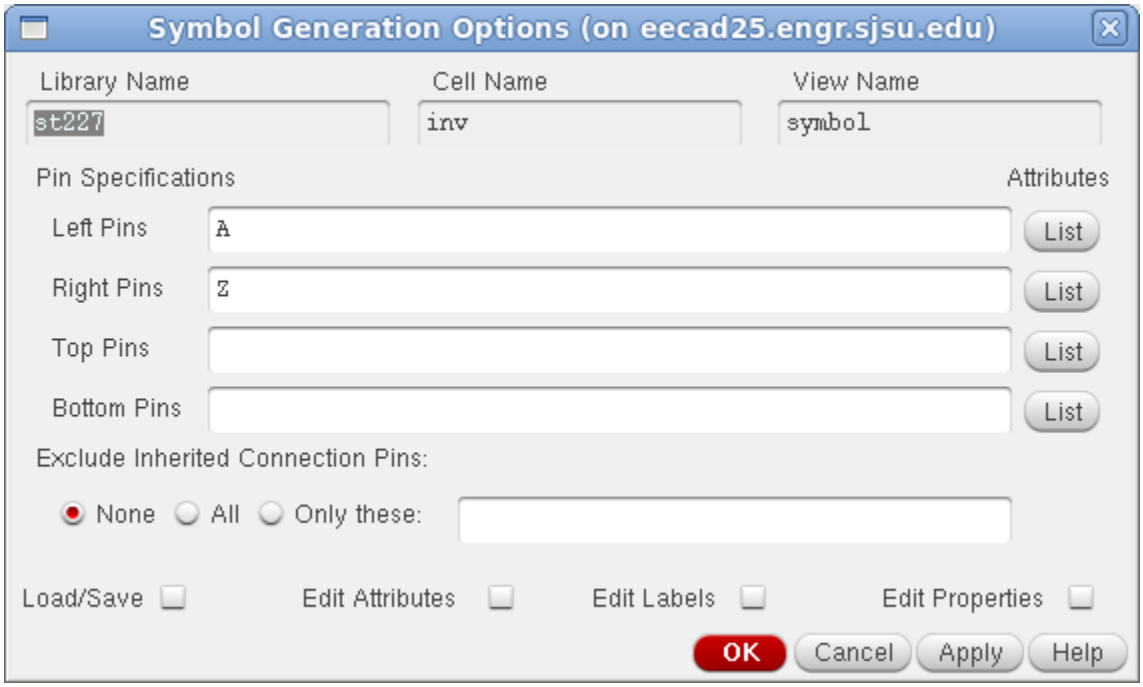


This should give

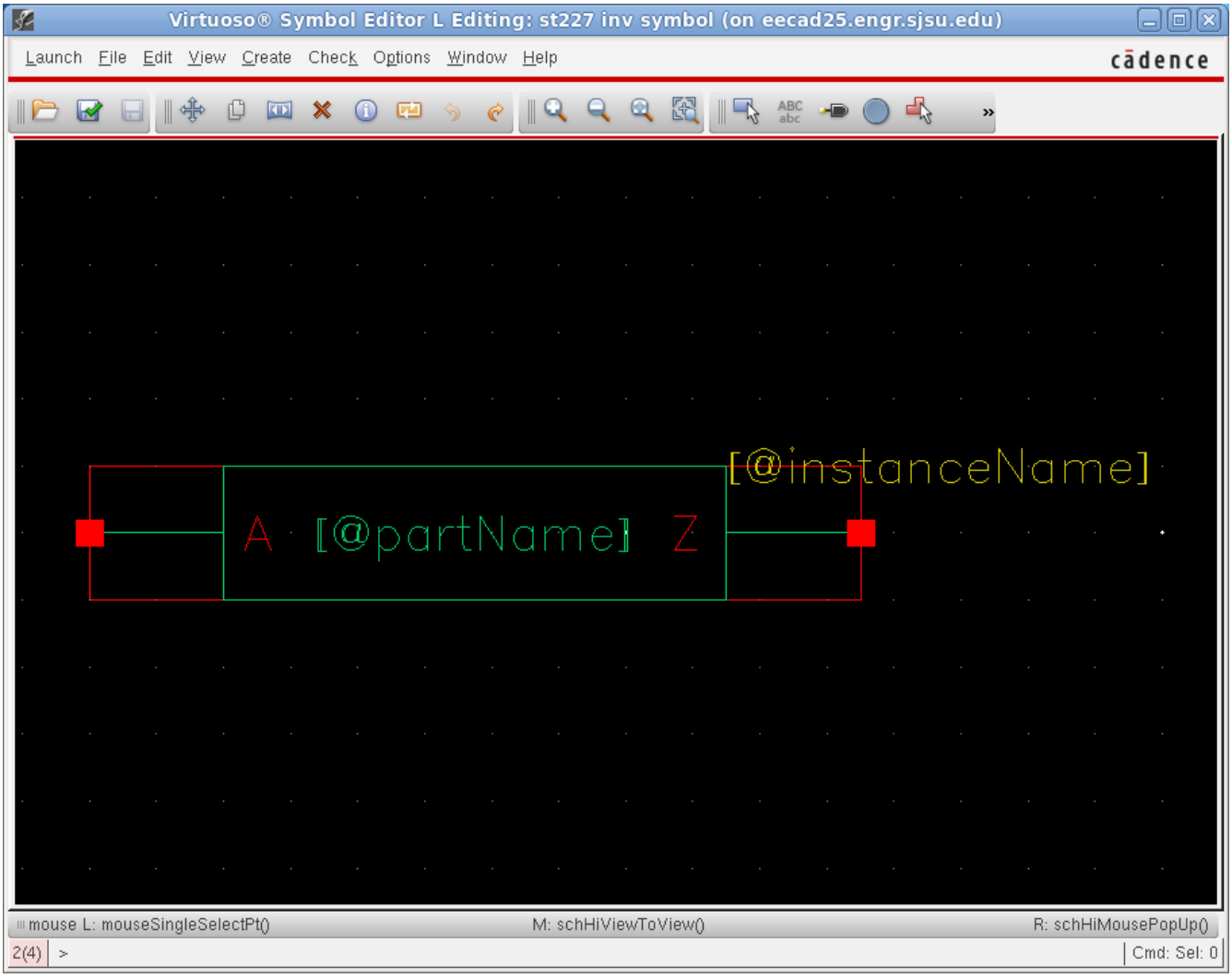


Make sure the to View Name is symbol (It normally is), and the type is schematicSymbol. Click on OK.

This brings up a screen with the pins on the top, bottom, left and right. You can move them where you like. In this case, They are fine, and you can click OK.



This opens the symbol editor.



If you like the symbol, just press the check and save floppy disk symbol with the green check mark.

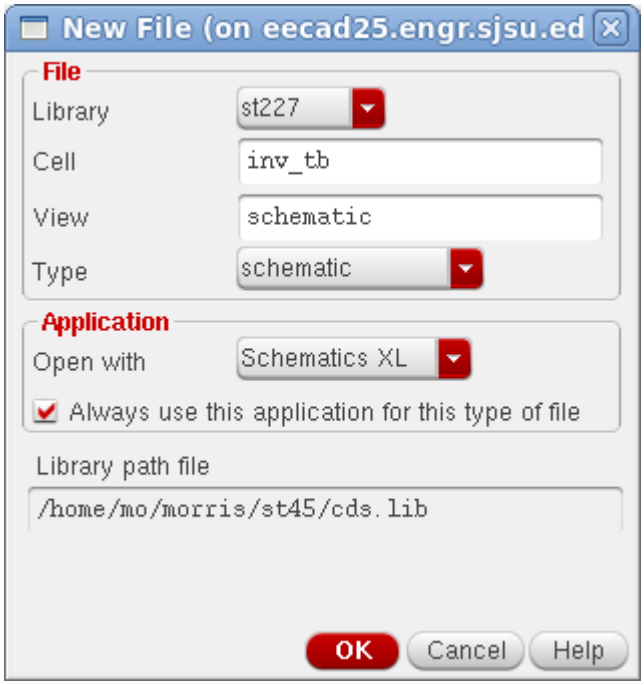
At this point, the symbol is created, so just click on <file> and then click on <close>

The schematics for the inverter are completed, so close that file by switching to the schematics, and clicking on <file> and then <close>

The library manager should be on the screen, or it may be minimized on the toolbar. If so, bring it up on the screen.

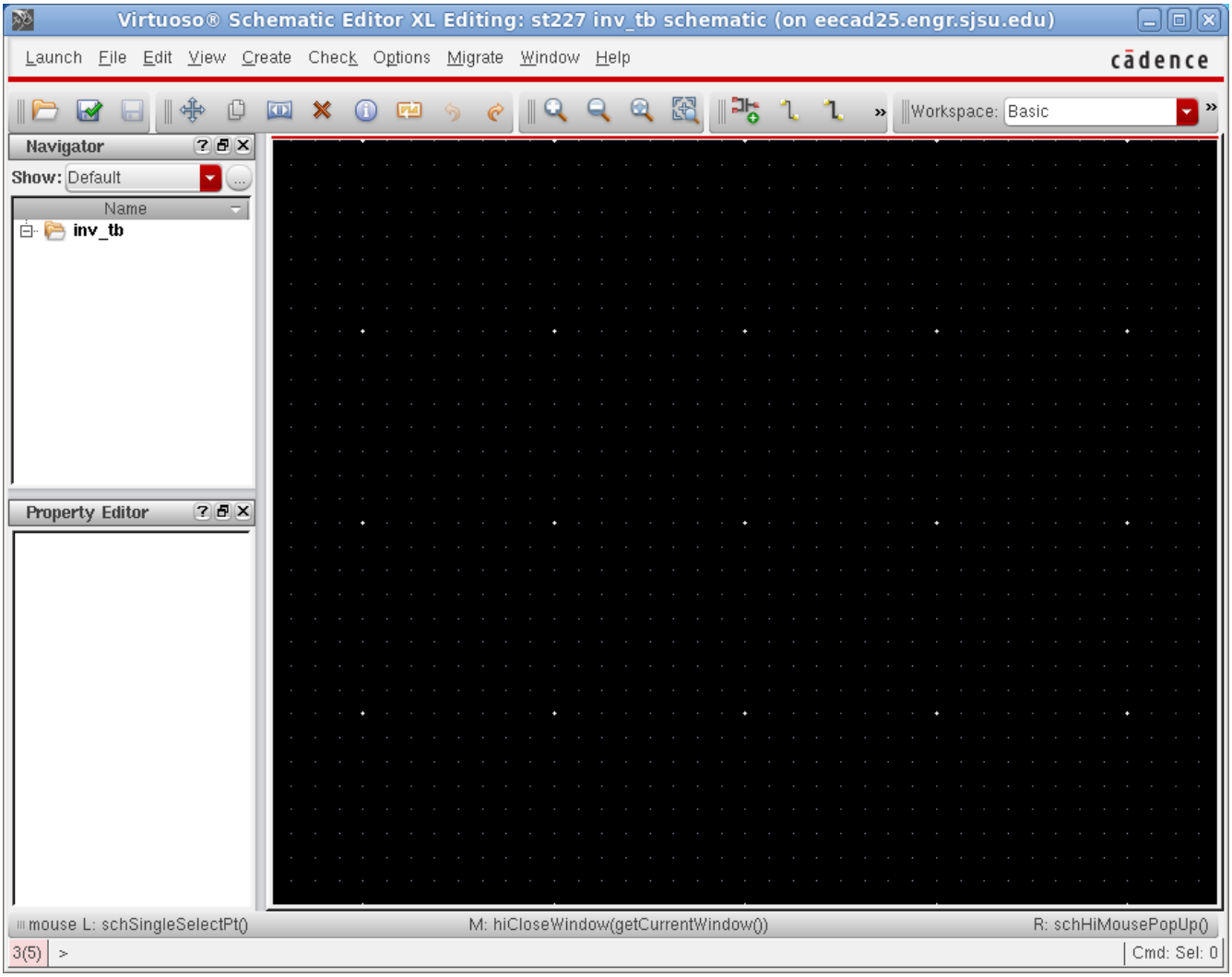
Now, create a test bench for the inverter. Click on <file> then <new> then <cellview>

name this schematic sheet inv_tb (for test bench). Use tool schematic XL.



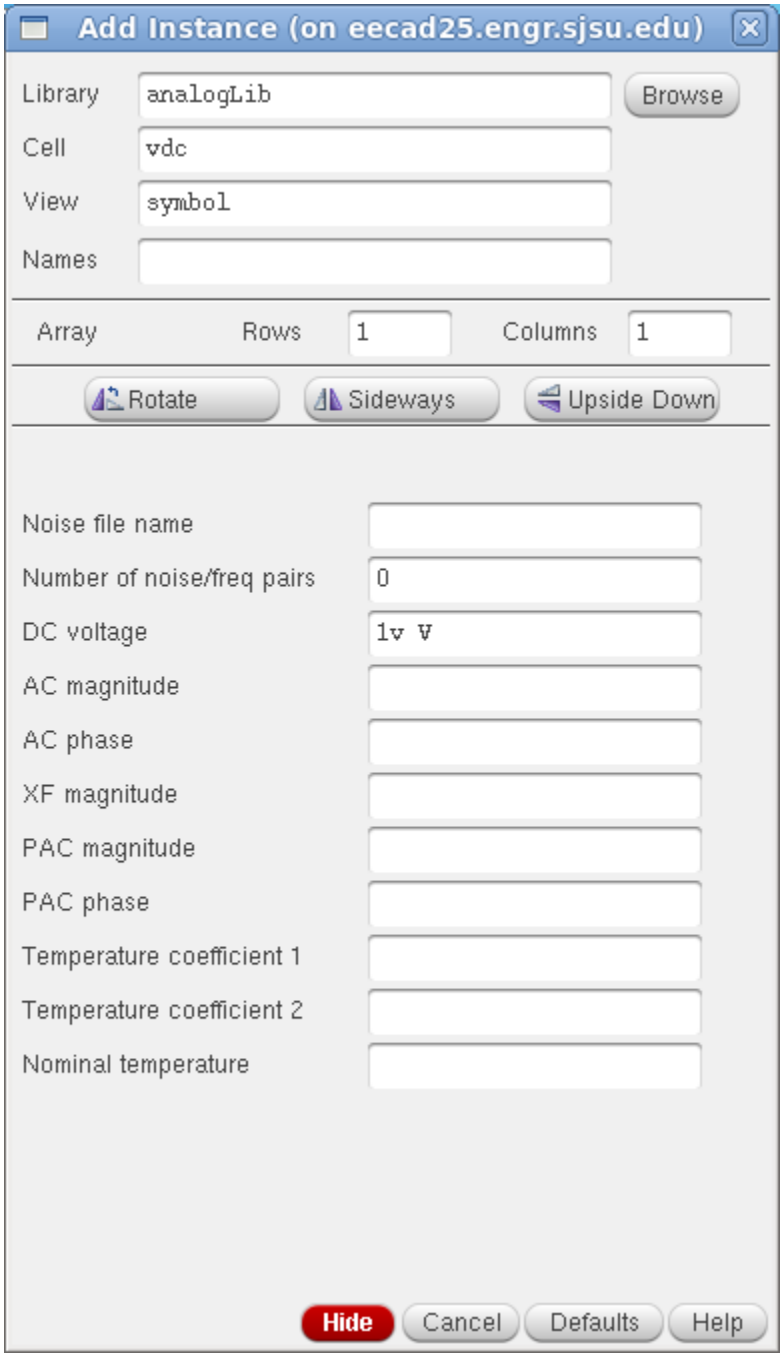
Click on <OK>

You should be back in the schematic editor.



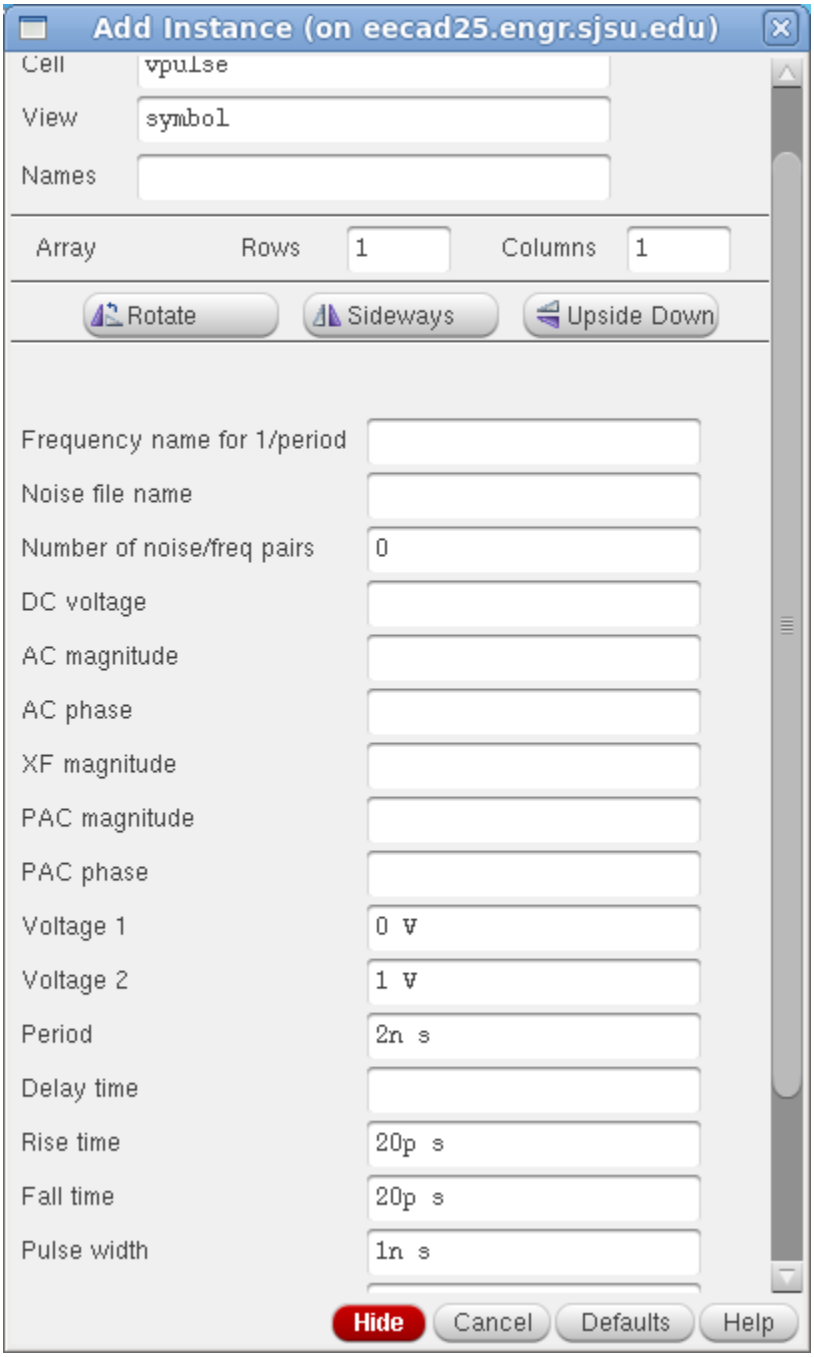
Using what you learned from creating the inverter, place the symbol from the library (it will be in the st227 library), a power, ground, vdc and vpulse on the schematic as illustrated below.

Set up the vdc for 1v operation

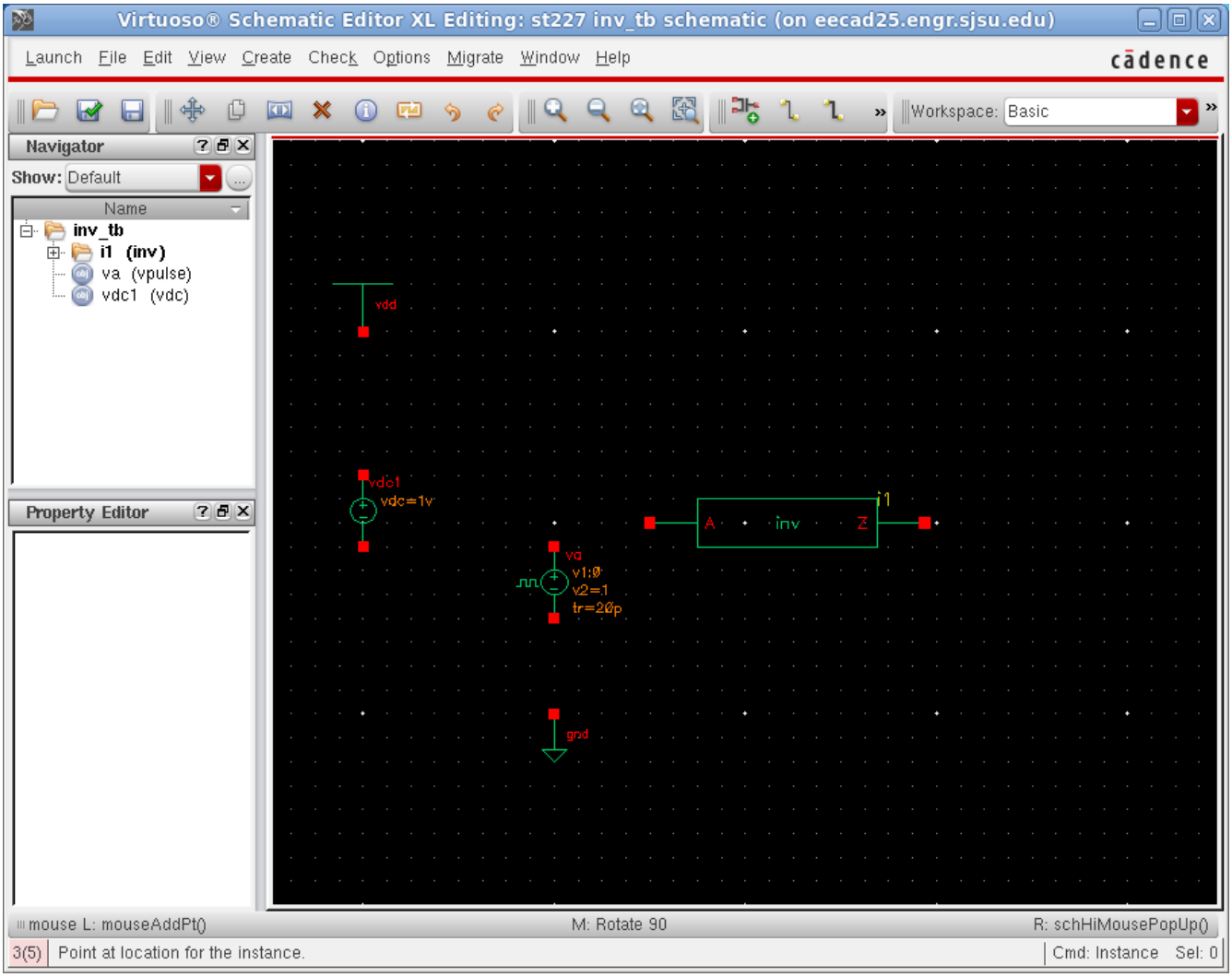


You should not add a symbol until you give it a name. Then you can place it on the schematic.

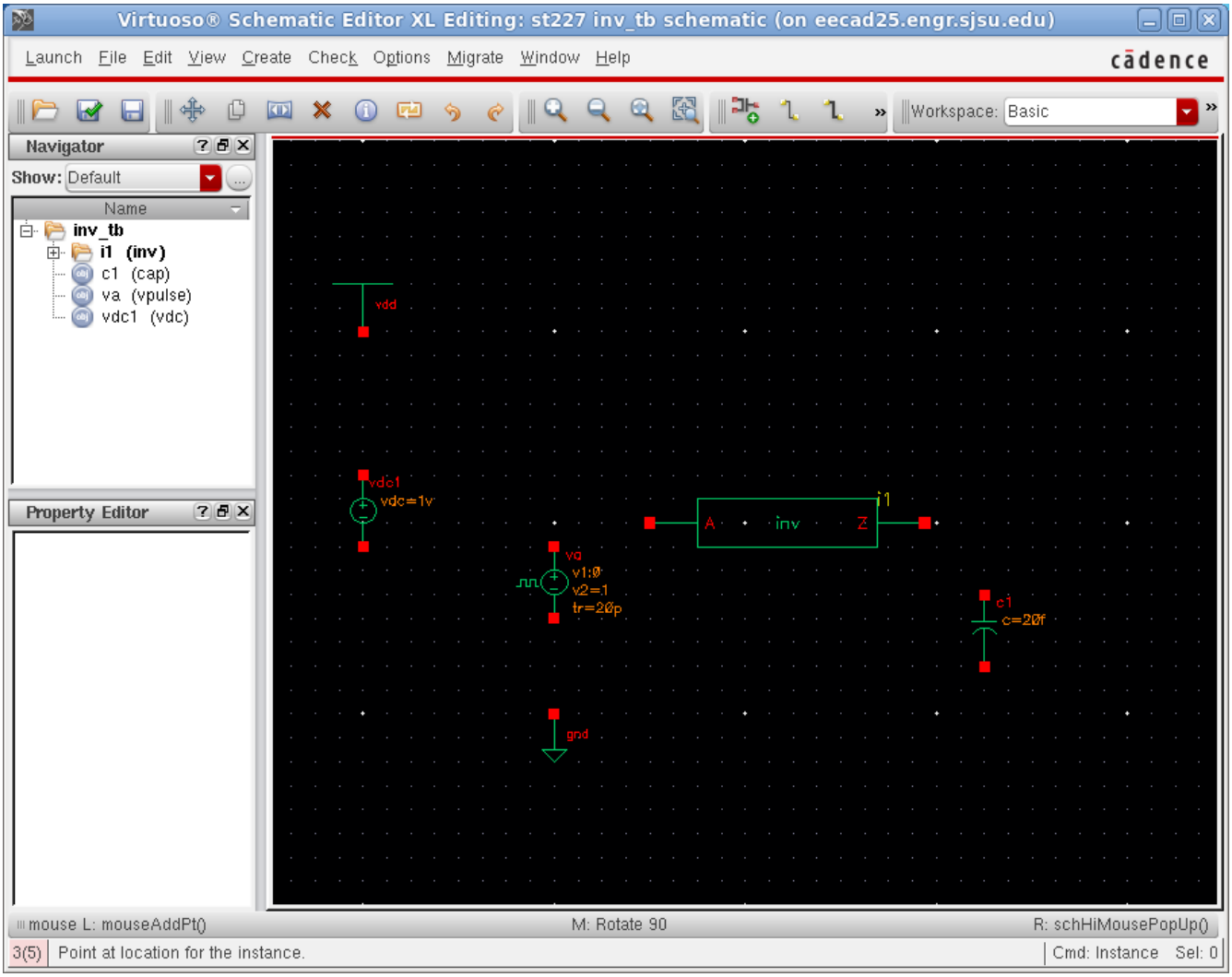
Set up the vpulse for a 1ns pulse train. You may have to scroll up and down to get to all the DC parameters. The first set of things are for AC analysis.



Your schematic should look something like:

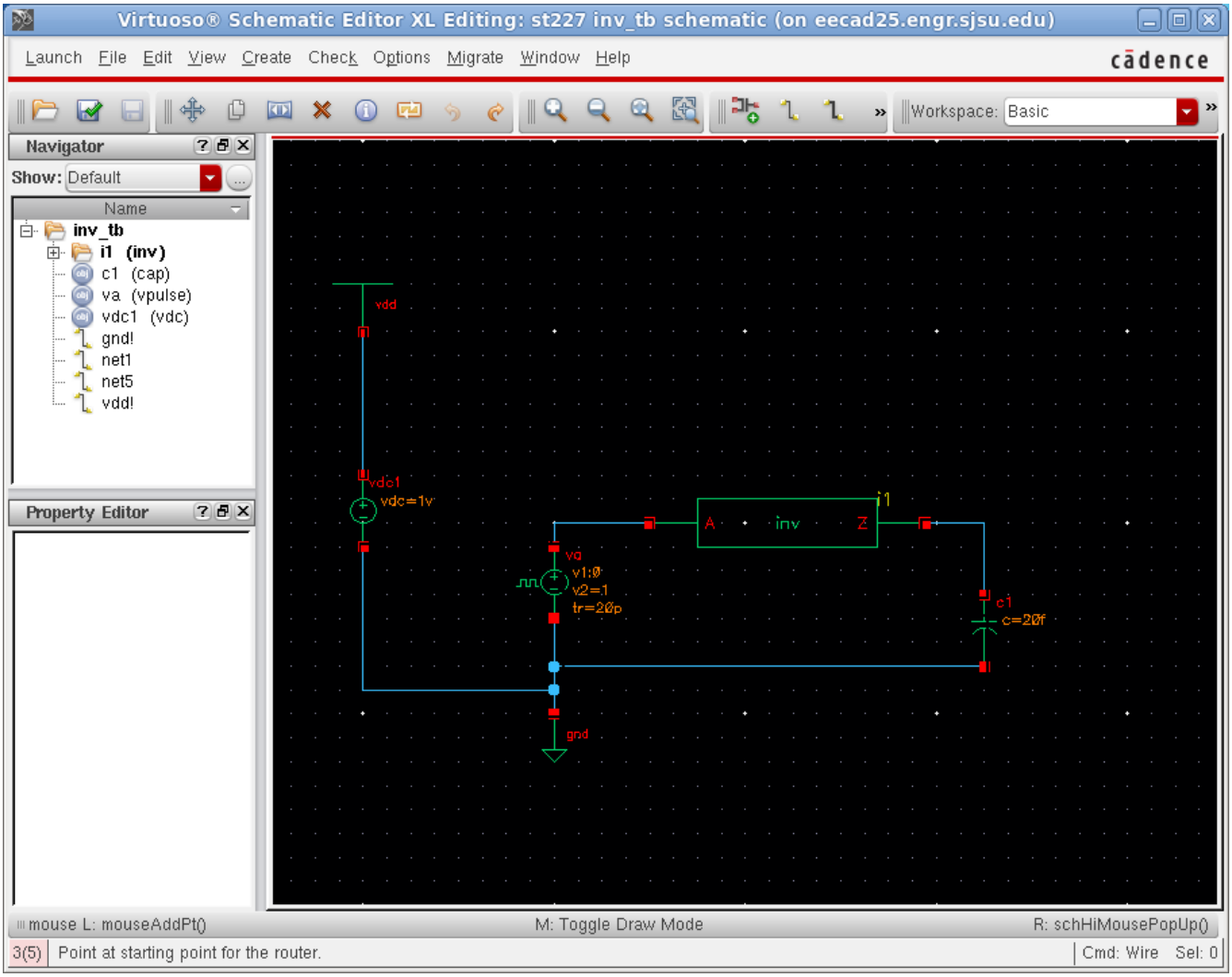


Now add a 20f capacitor for load on the inverter.



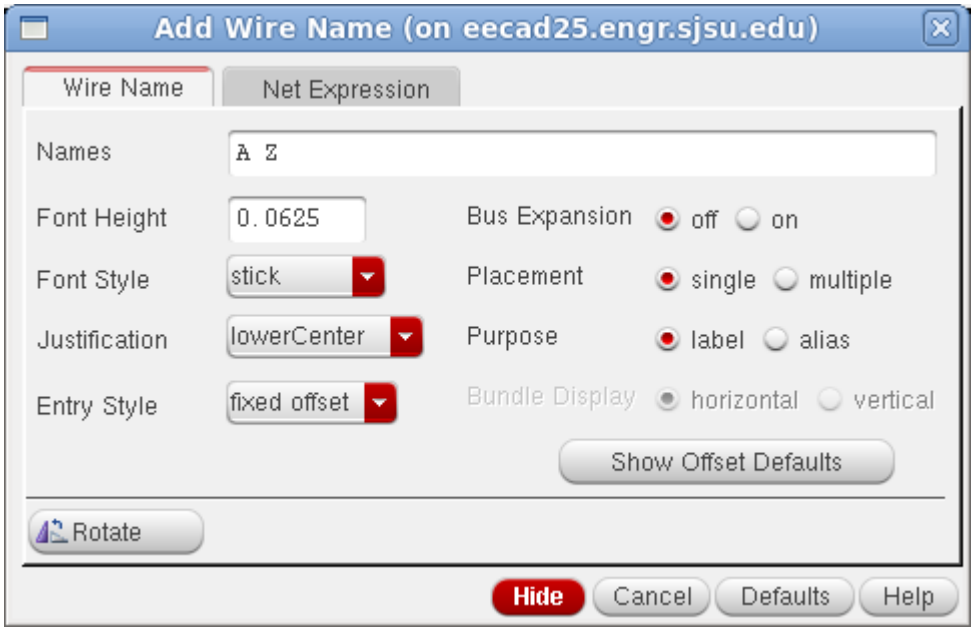
Next using the thin wire, connect as below.

When you have it connected properly, press the check and save floppy disk.

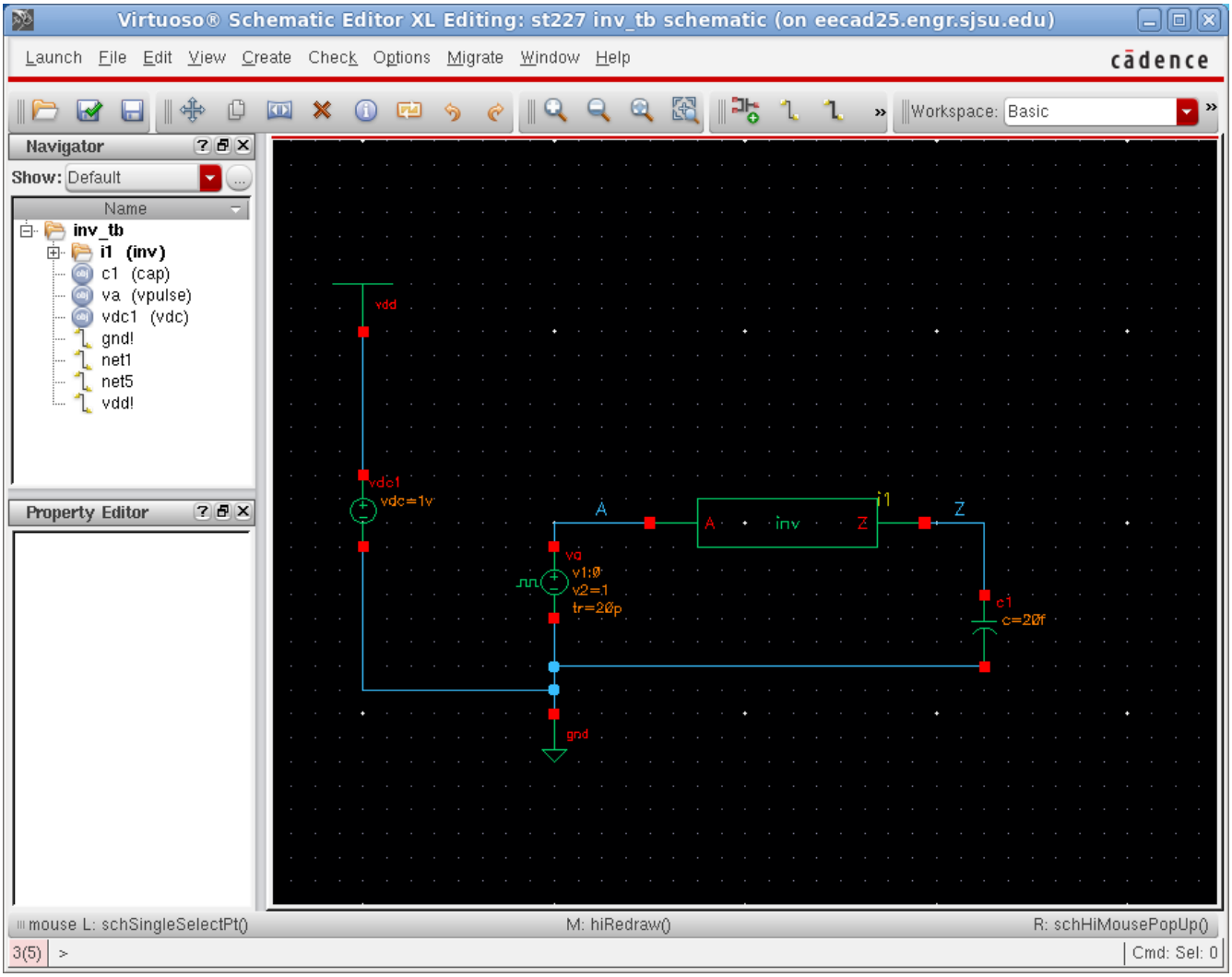


If all goes well, it should be OK. If not, correct any errors.

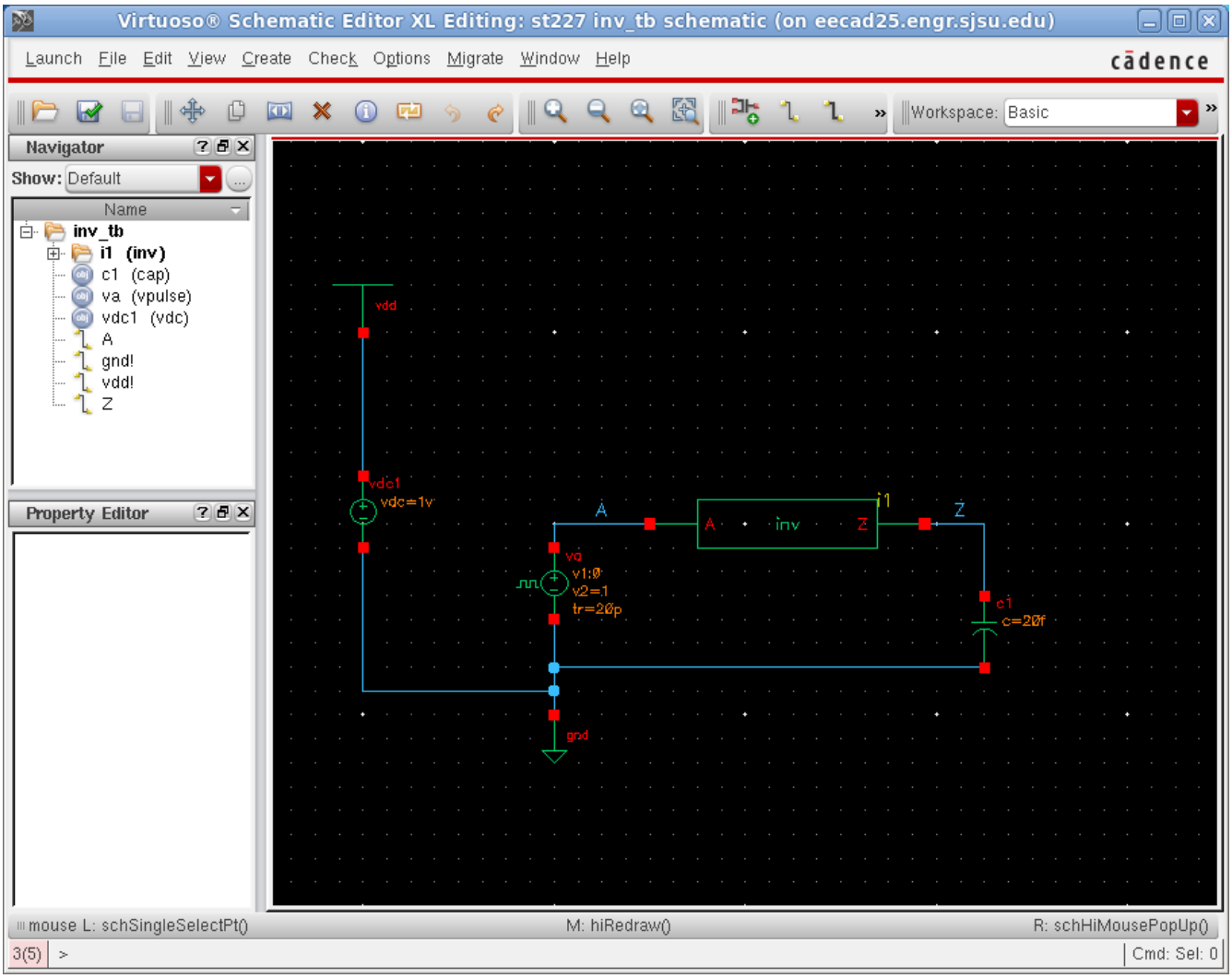
Note that the input and output nets have silly names. This will drive you nuts later in debug. Take a few moments, and give these nets a name. Use the <create> <wirename> option, or on this screen, the >> and then the wire with abc above it.



The two signal names are typed as a list. Then place the cursor over a wire and click. The name should switch to the next one on the list. Place both names on the schematic. (A as the input, and Z as the output).



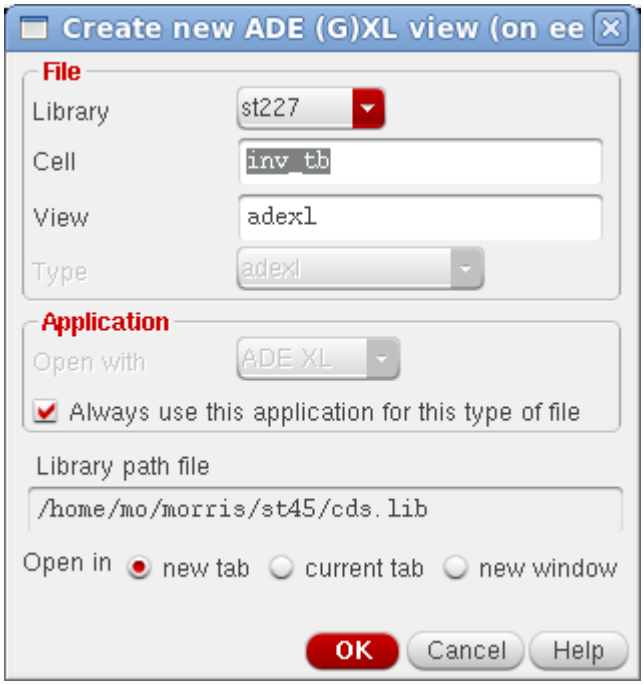
Note that the pull down menu won't update until you check and save the schematic. Check and save the schematic, and it should now appear as:



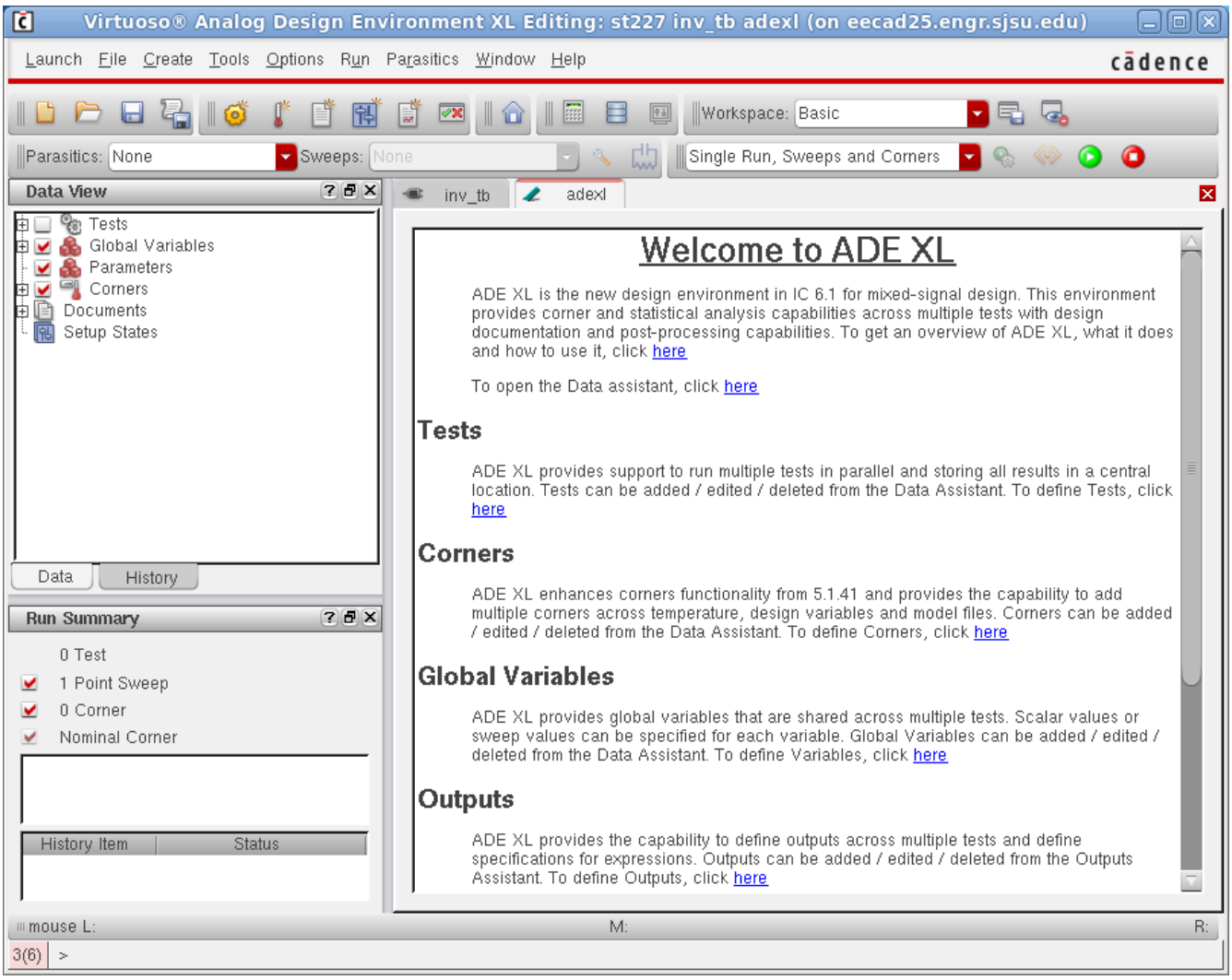
The schematic has been created and things have names. It is now time to try some simulation.

Click on <launch> then <ADE XL>

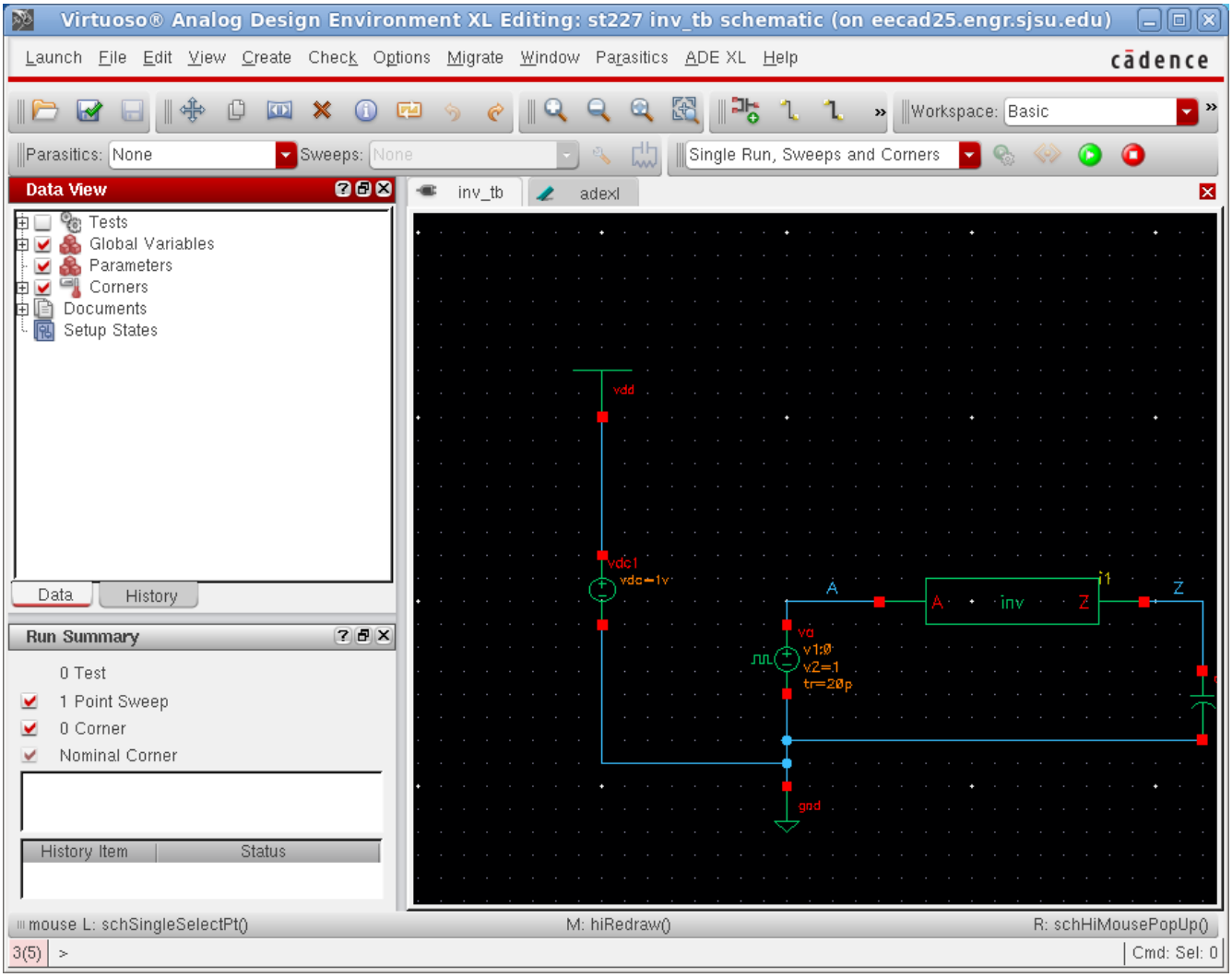
When the menu appears, click on Create New View



The setup should be OK. Your path names will be different. Click on OK. It may take a while as it sets things up. You should now get:



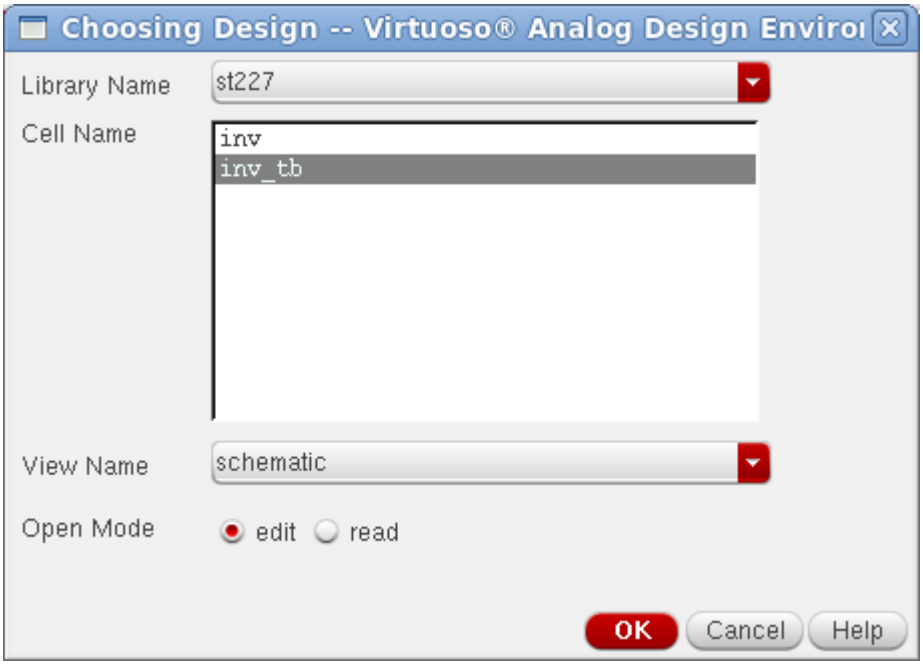
This window tells you about some of the neat stuff you can do with ADE XL. Most of it won't be used for now. To get to the design, click on the tab <inv_tb>



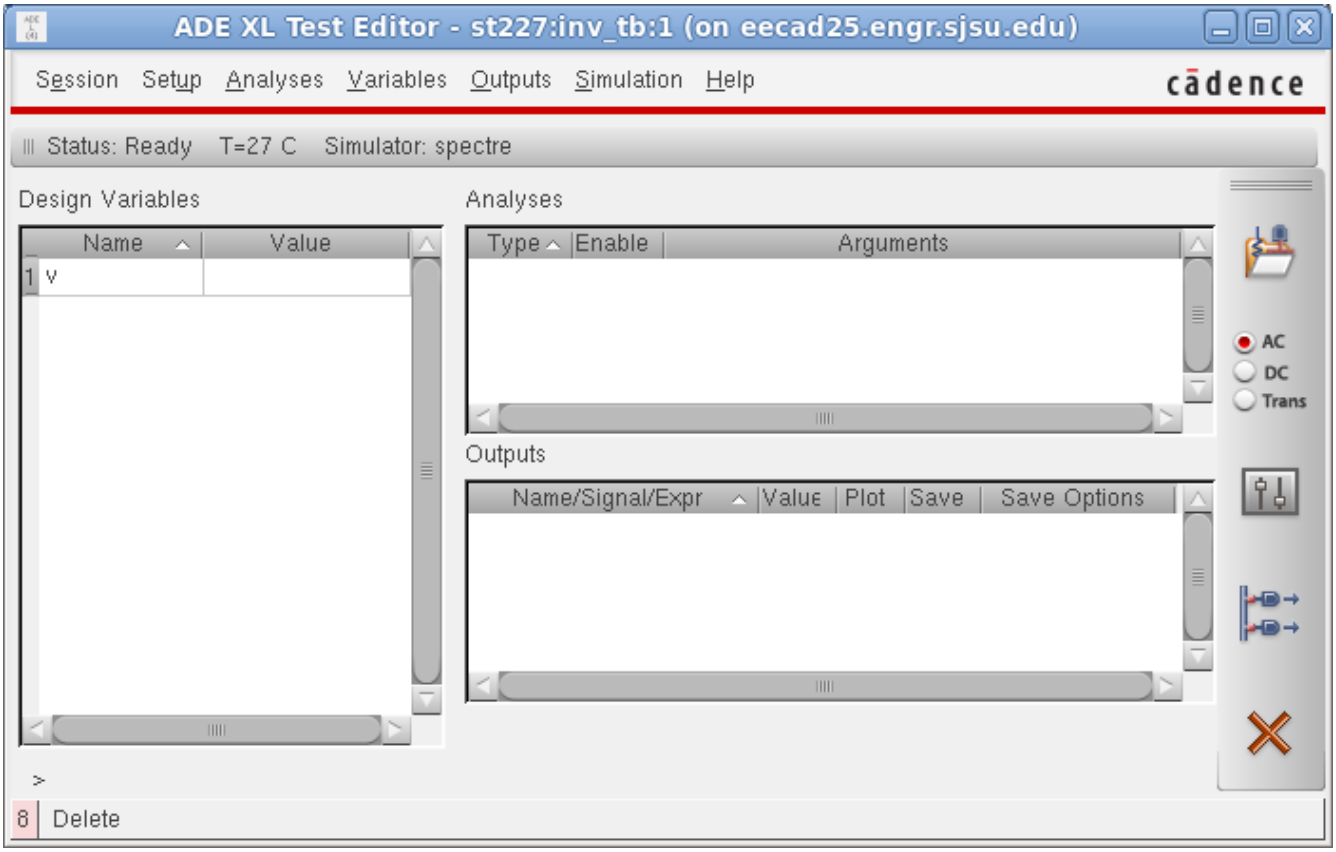
This screen is very different than ADE L (Which is much like the old Cadence).

Click <ADE XL> then <create test>

A screen will pop up, and then another one with

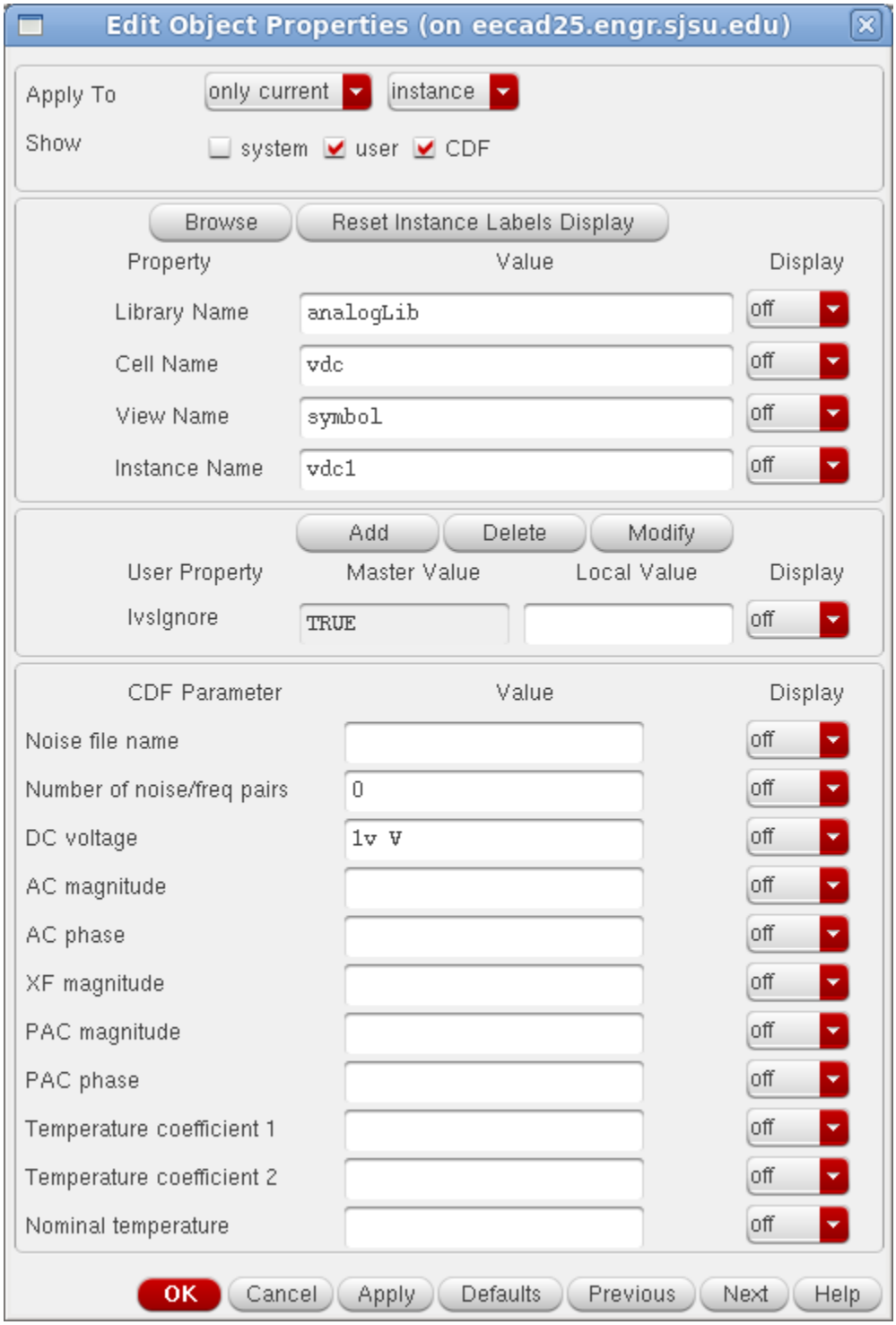


Select the inv_tb, and then click OK



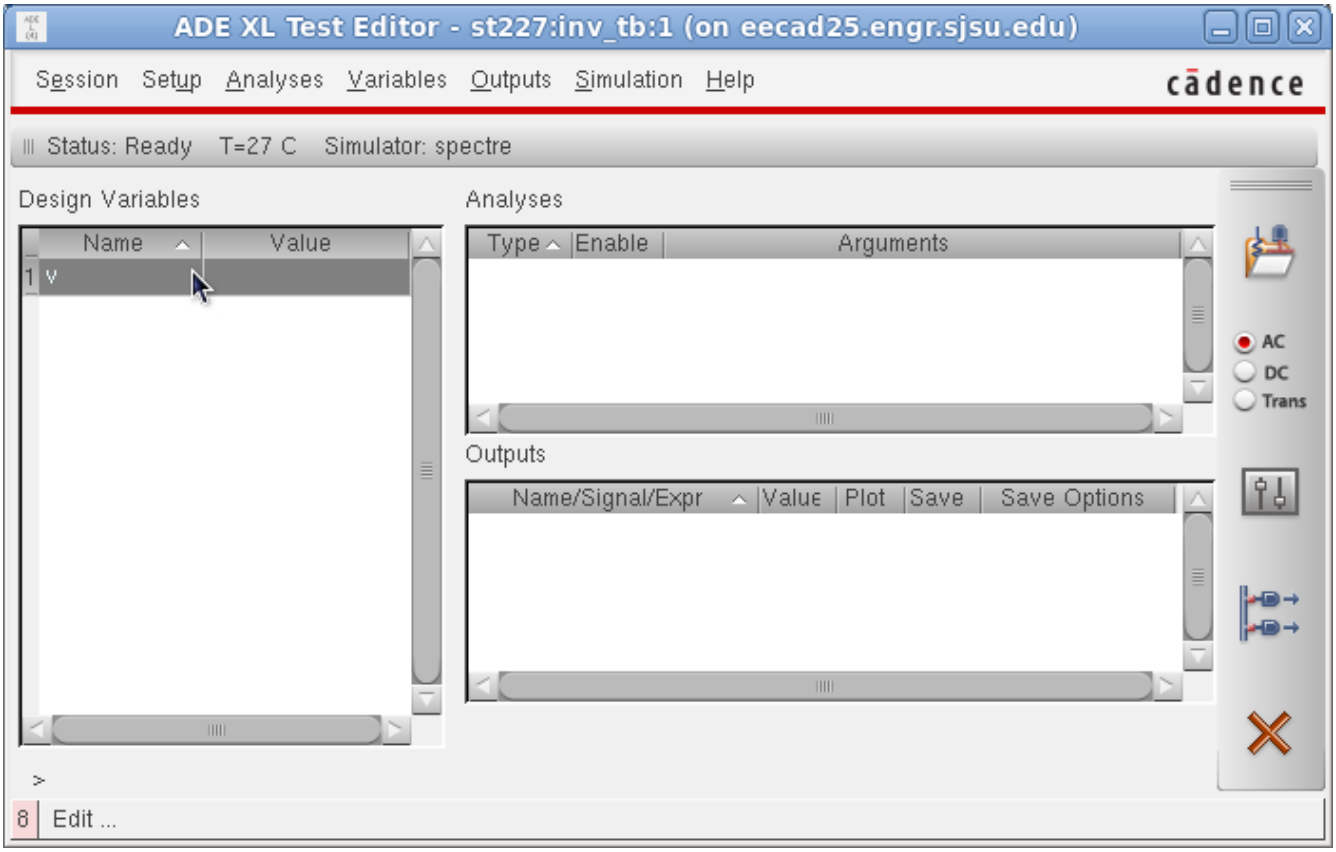
This screen is used to set up the simulation. (It should look familiar to the old Cadence) At this point, you can see that one of the voltage sources has the v used for Volt next to a number. A common mistake. You would normally have to go all the way back to the schematic editing system to fix it, but you are actually in the schematic editing system. Go back to the ADE XL

screen with the inv_tb tab. Select the vdc (Where the error was located). Then click on <edit> and <properties>

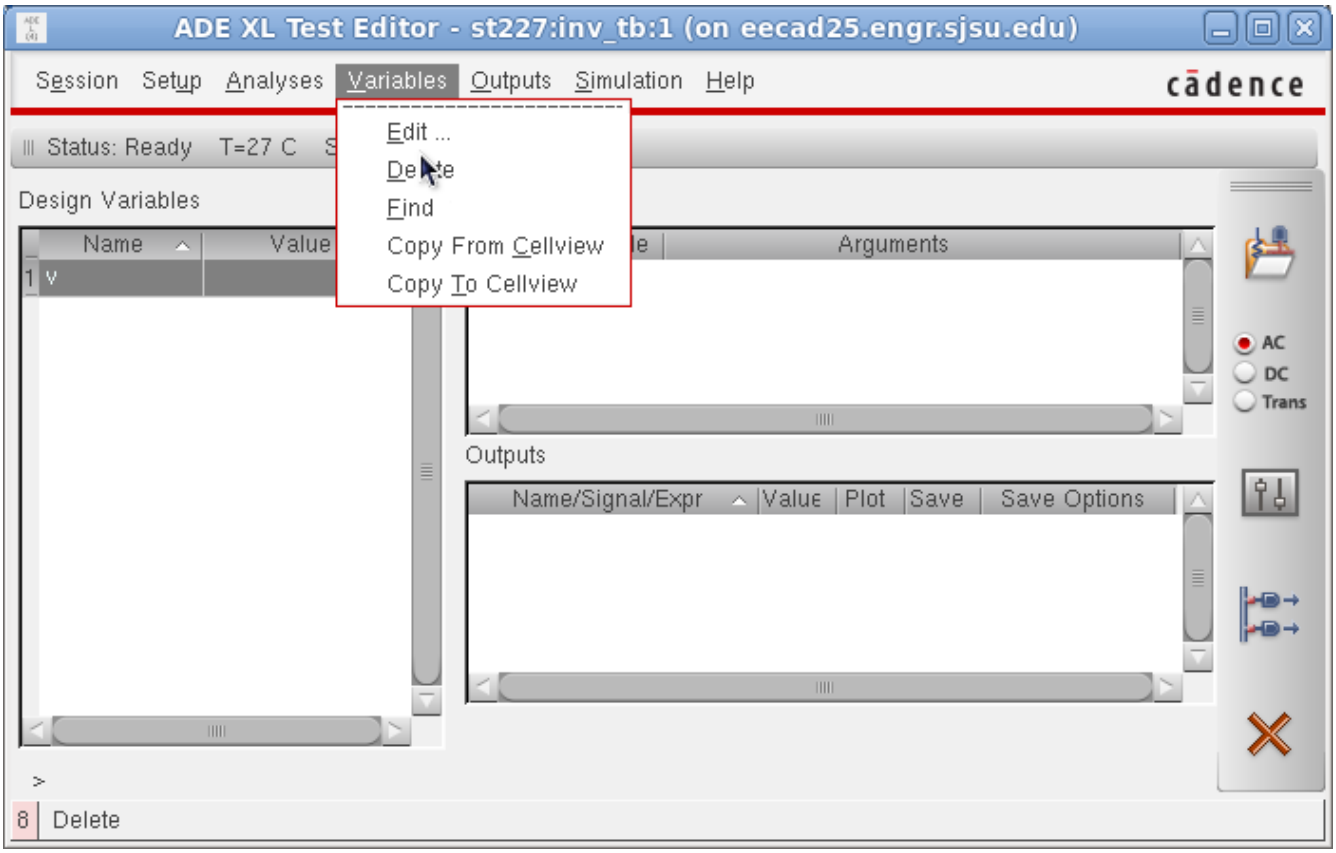


Change the 1v to 1 and click OK.

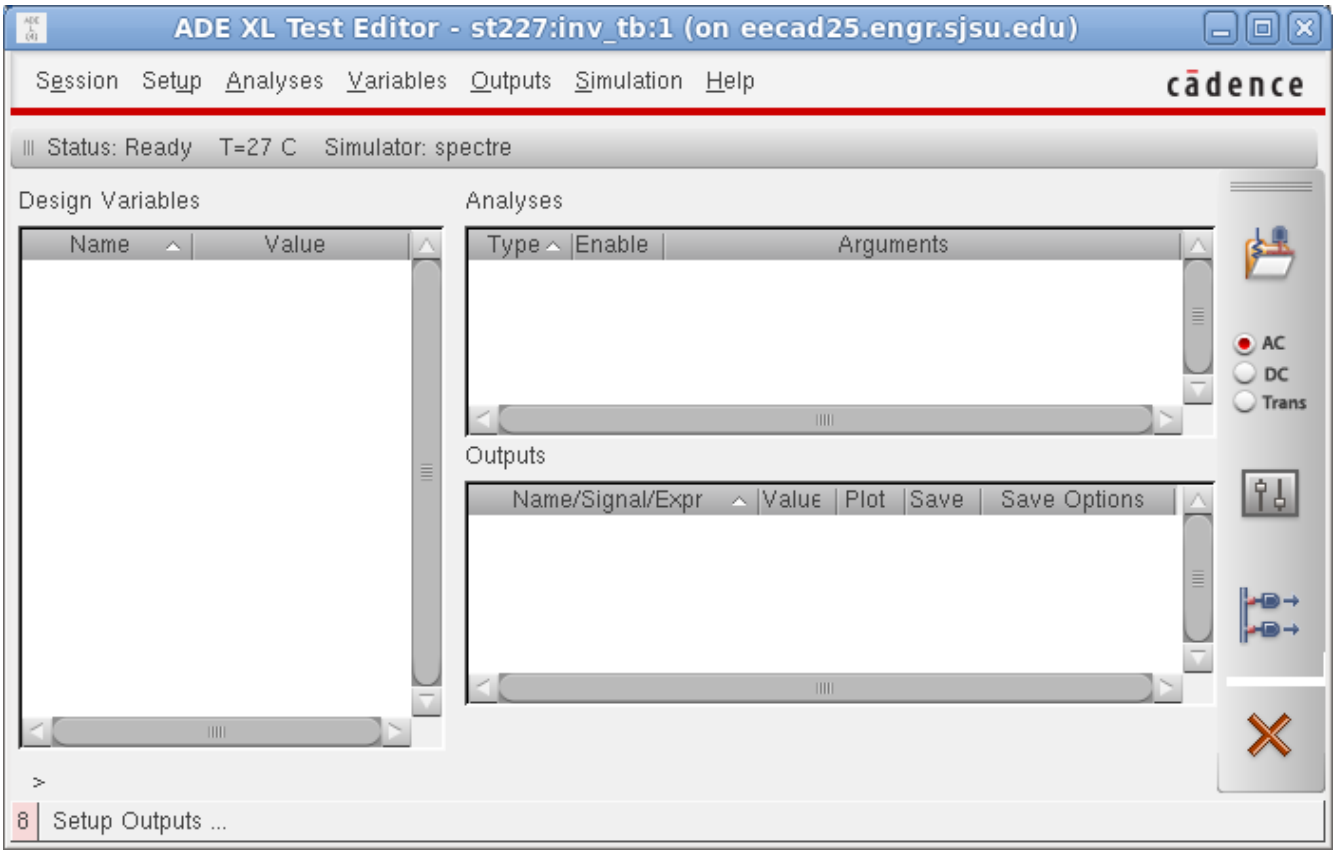
Click on the check and save and go back to the ADE XL test editor screen. The variable v is still there.
Click on the line with the v to select it



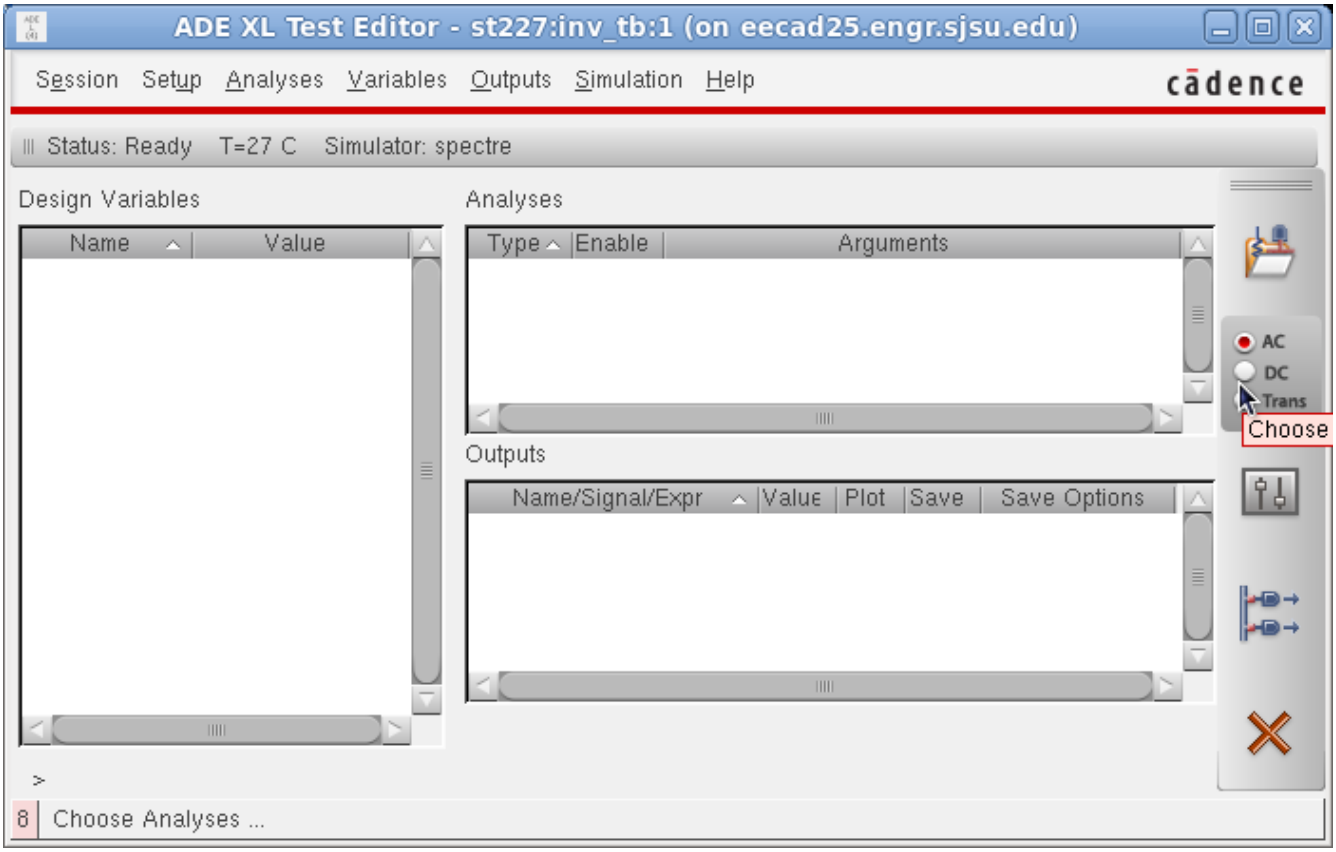
Now, click on <variable> and then <delete> to remove it



Problem fixed...

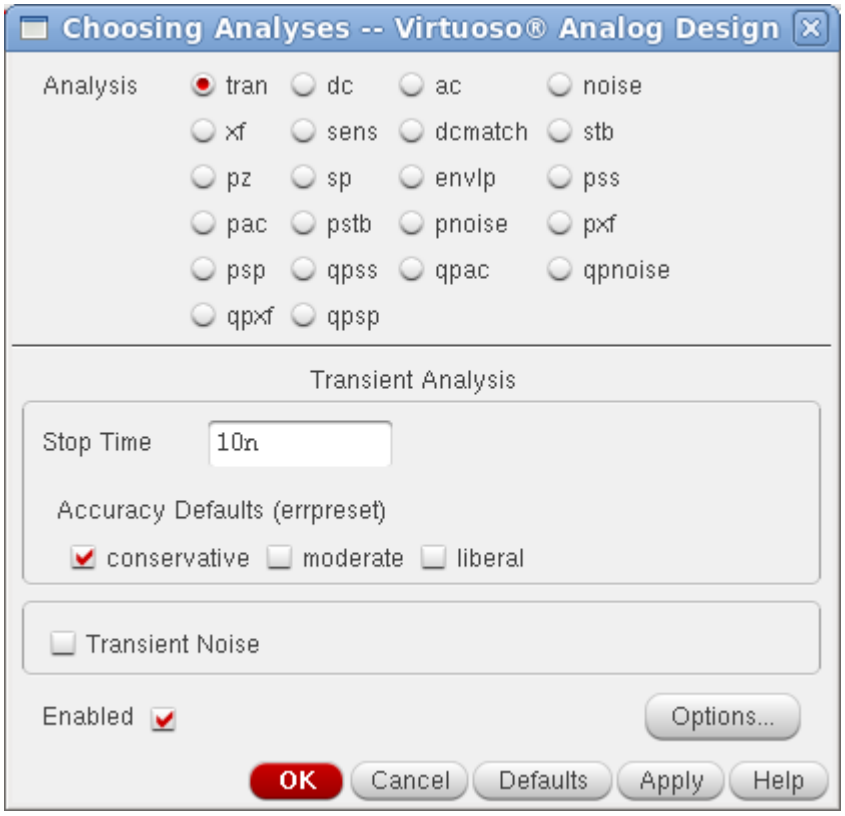


Now to set up the simulation. Click on the choose analysis button.

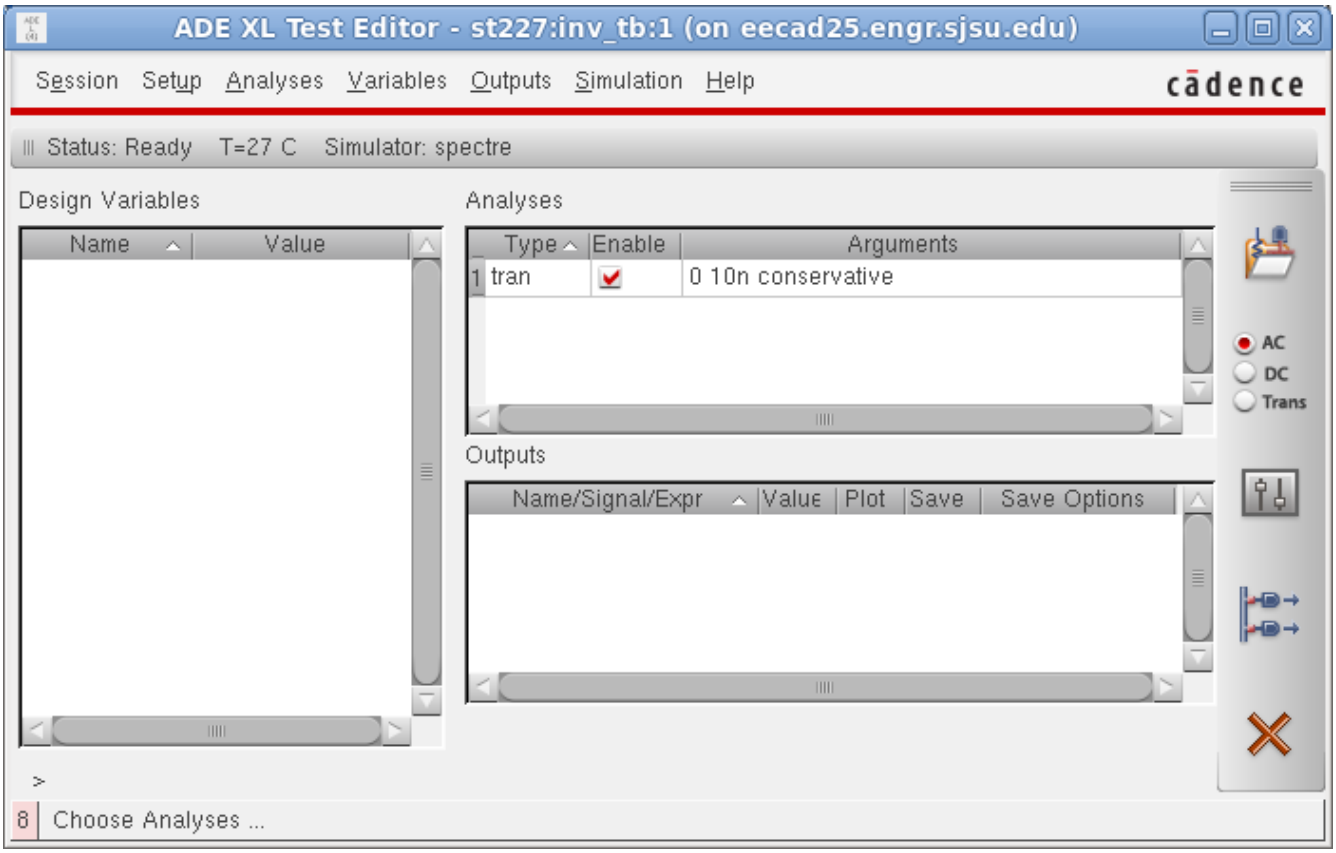


This pops up a window with the simulation options. Notice there are a lot more of them than in the past versions of cadence. Make sure the transient analysis is selected, and set it up for 10n of simulation time.

All EE227 simulation should be performed in conservative mode.

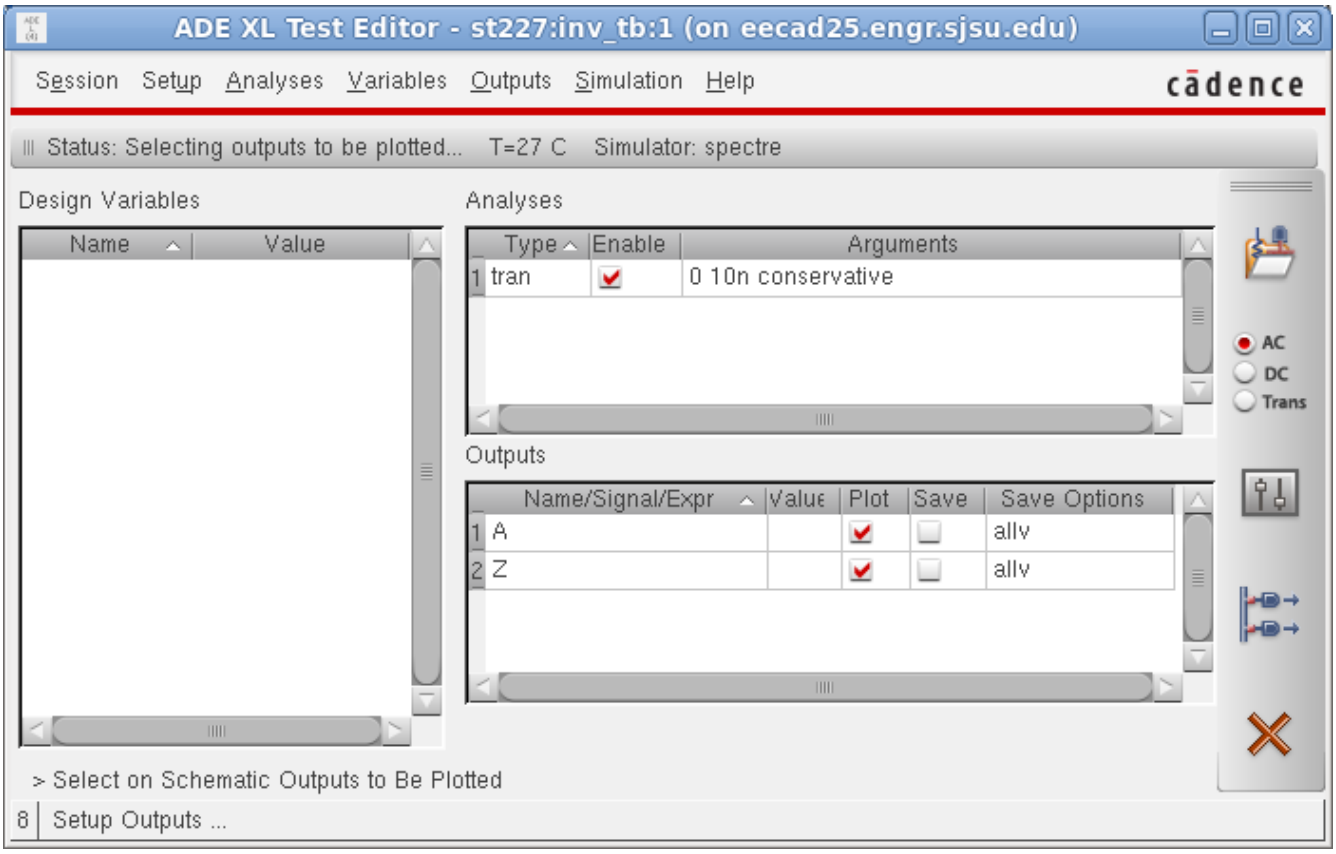

Choosing Analyses -- Virtuoso® Analog Design
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
pz
sp
envlp
pss
pac
pstb
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
Transient Analysis
Stop Time
10n
Accuracy Defaults (errpreset)
conservative
moderate
liberal
Transient Noise
Enabled
Options...
OK
Cancel
Defaults
Apply
Help

Click OK


ADE XL Test Editor - st227:inv_tb:1 (on eecad25.engr.sjsu.edu)
Session
Setup
Analyses
Variables
Outputs
Simulation
Help
cadence
Status: Ready
T=27 C
Simulator: spectre
Design Variables
Name
Value
Analyses
Type
Enable
Arguments
1
tran
0 10n conservative
AC
DC
Trans
Outputs
Name/Signal/Expr
Value
Plot
Save
Save Options
>
8
Choose Analyses ...

The results is listed. Note that the simulations can be enabled and disabled. This is a nice feature.

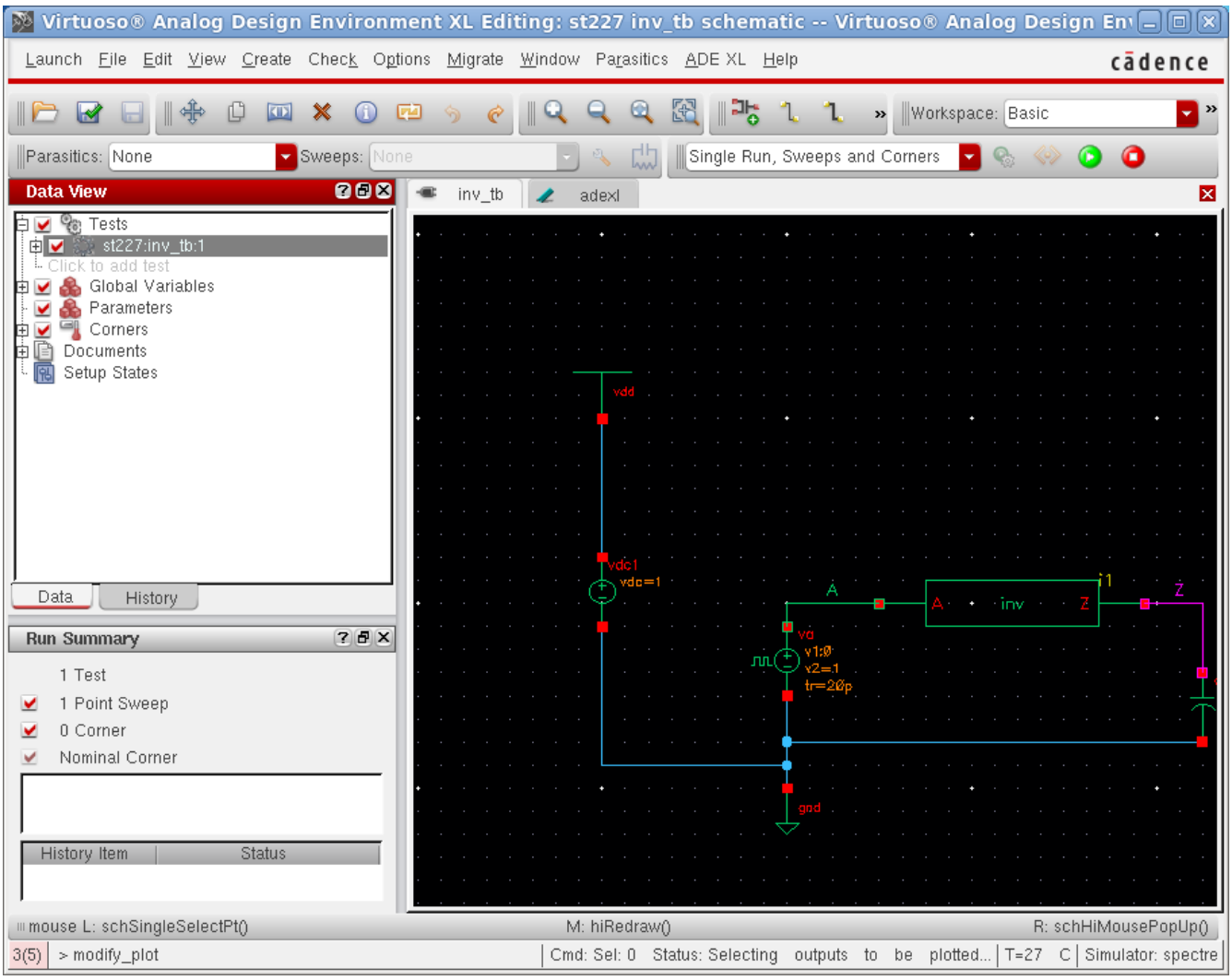
Now, select the outputs. It's just like the old Cadence. Use <outputs> then <select on schematics>. This will select the schematic editor. There, you can click on the wires for the signals desired. If you want currents, click on the terminals, and a circle is drawn on the schematic indicating what has been selected. When you go back to the simulation setup screen, you should see:



So far, things look the same as the old Cadence. However, there is no place here to actually run the simulation.

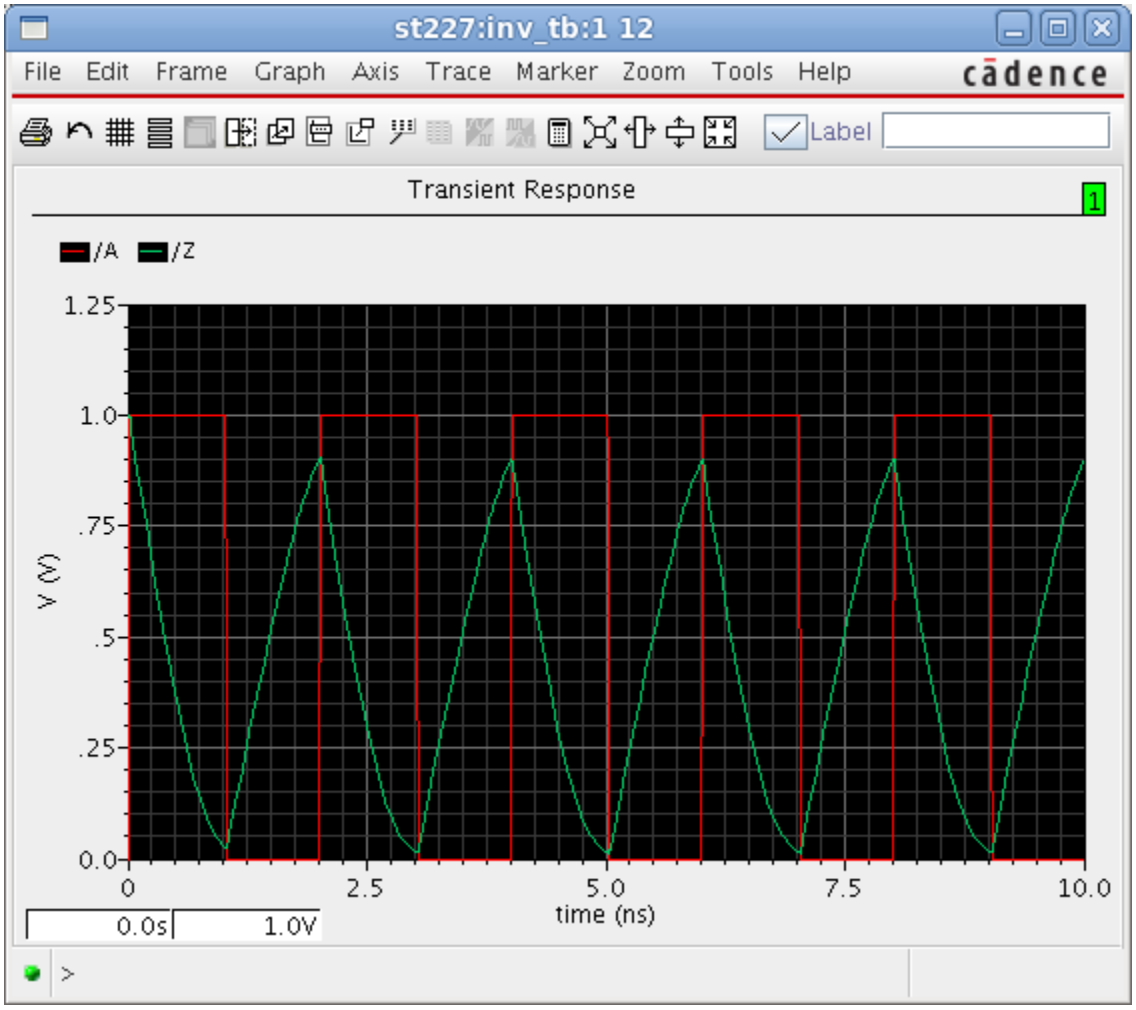
Click <session> and save the state. The defaults are fine for now.

Click on session quit, and then you should bring up the ADE XL screen. On the left, you will see the simulation description you just set up. Click on it to highlight.

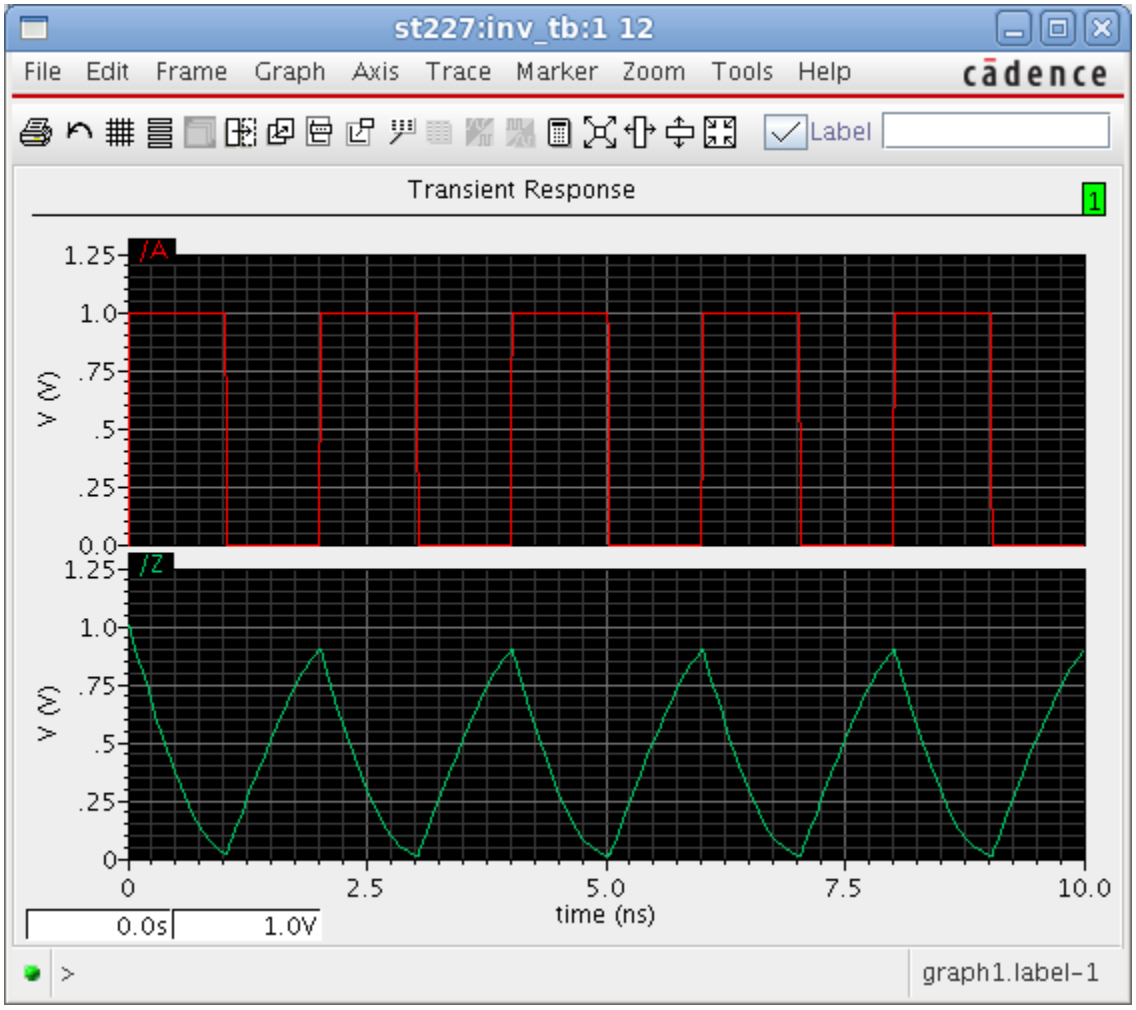


Off the the right of the upper region of the screen is a green circle with a play type button (triangle shape). Click on this to run the simulation.

It may take a while, but eventually the simulation will finish and a display screen will appear. This one is a little different. For one thing, it can be scrolled if too many things are on the screen.



Yes, this is very slow logic. This transistor has a .5 volt Vt. Explore what this display mechanism can do. It is very nice in some respects, and at the same time different. The stripe icon is the set of rectangles. Give it a try, and you will get:

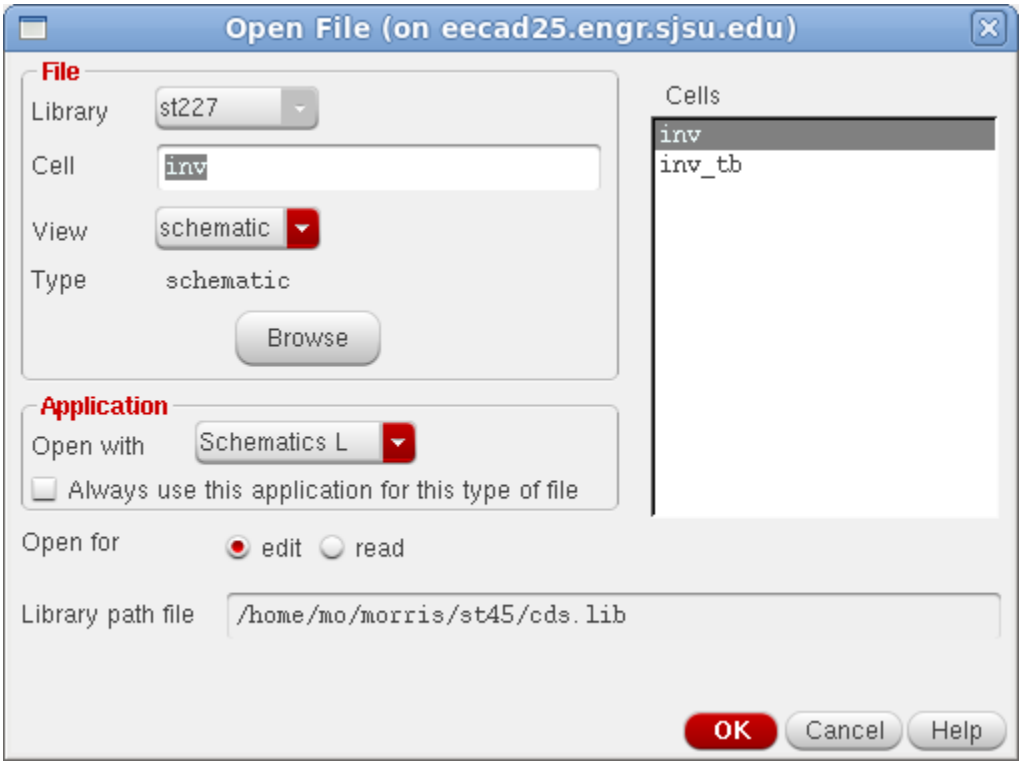


When you are done, you can shut down the graph window, and the ADE XL for now.

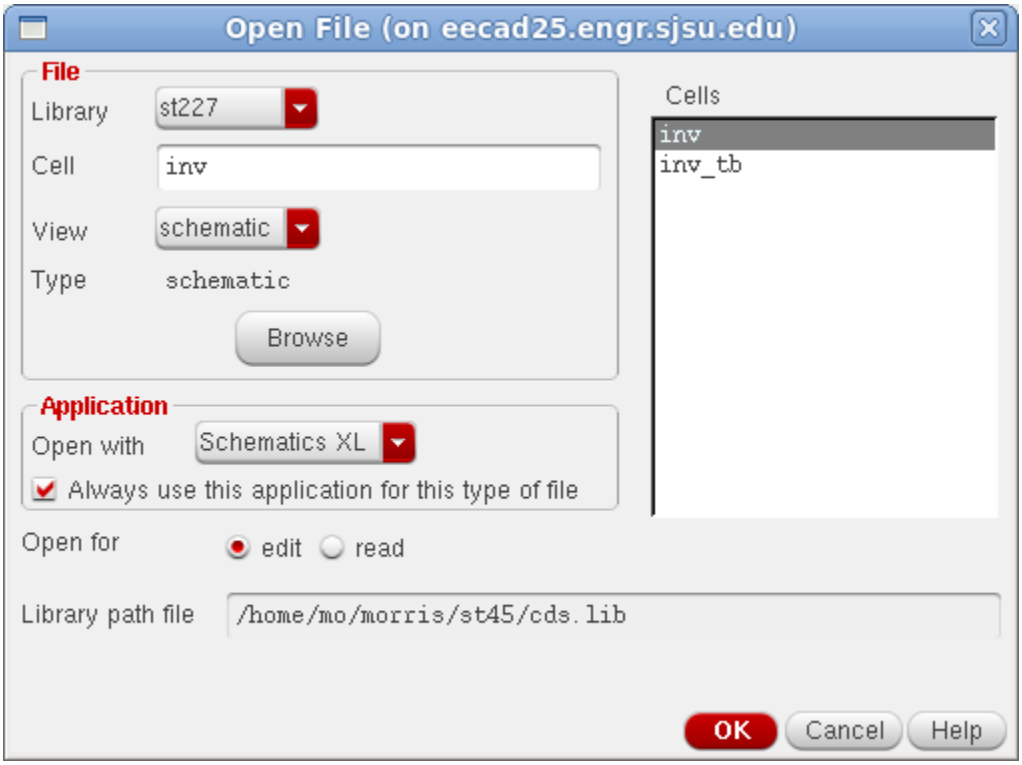
Click on <file> then <close> to shutdown the tool.

Open the file manager window (It may be minimized, but should still be open)

click on the library, then on the inv. This should show schematic and symbol. If you just double click on schematic, it will open a lower level schematic editor. For most work, you should use the XL version of the editor. To get this editor, right click on the schematic, and then use <open with>.

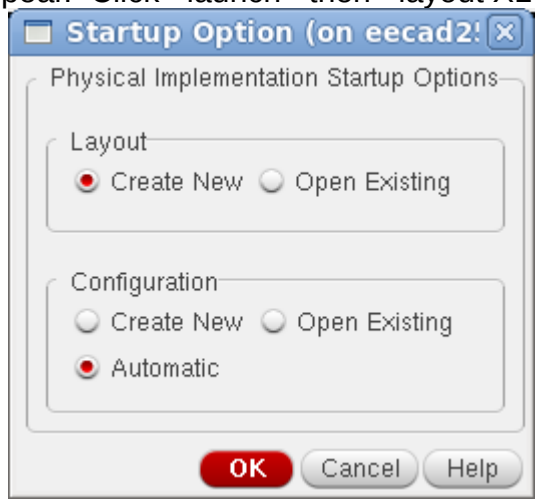


In the Application area, click on the red down arrow, and select schematics XL. You can click the always use this application for this type of file, but it doesn't seem to remember it all the time.

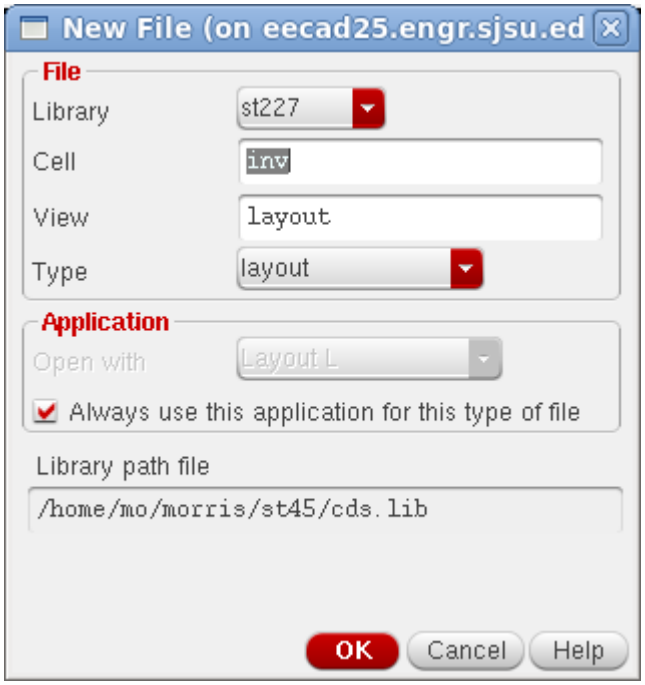


Click OK

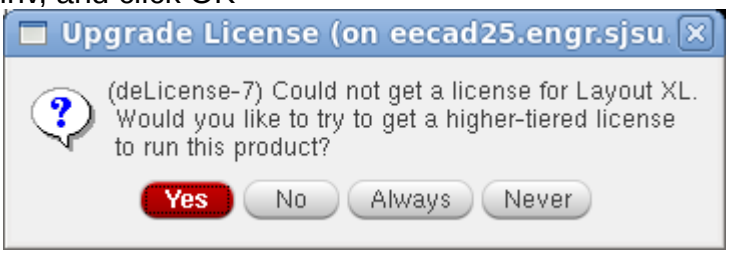
The schematic editor will appear. Click <launch> then <layout XL>



Make sure “Create New” is selected, then click OK

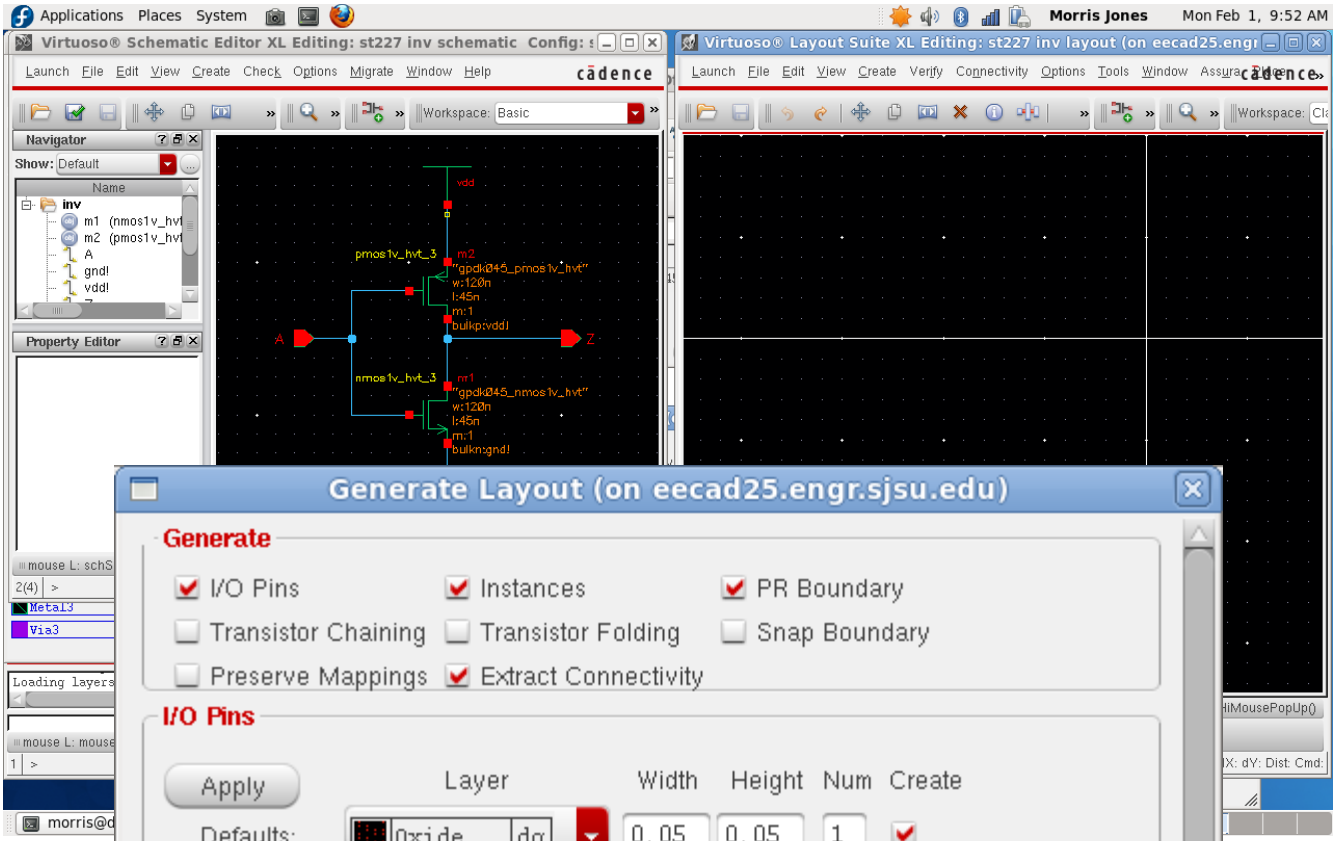


Make sure the cell is inv, and click OK



If you get the above screen. Click Yes to get a license. (We have the highest level licenses)

After dancing around and opening/moving things, you should have a screen that contains the schematic on one side, the layout on the other side, and a LSW window (Layer selection window). There is an about whats new window you can close.



Generate Layout (on eecad25.engr.sjsu.edu)

Generate

- [x] I/O Pins
- [x] Instances
- [x] PR Boundary
- [ ] Transistor Chaining
- [ ] Transistor Folding
- [ ] Snap Boundary
- [ ] Preserve Mappings
- [x] Extract Connectivity

I/O Pins

Apply | Defaults: | Layer: Oxide dg | Width: 0.05 | Height: 0.05 | Num: 1 | Create: [x]

Select: | Number Selected: 0 | Add a Pin

Term Name	Net Name	Layer	Width	Height	Num	Create
"A"	"A"	("Poly" "drawing")	0.045	0.045	1	t
"Z"	"Z"	("Oxide" "drawing")	0.05	0.05	1	t
"gnd!"	"gnd!"	("Oxide" "drawing")	0.05	0.05	1	t
"vdd!"	"vdd!"	("Oxide" "drawing")	0.05	0.05	1	t

Update | A A | Layer: Poly dg | Width: 0.045 | Height: 0.045 | Num: 1 | Create: [x]

Pin Label Shape: ( ) Label ( ) Text Display (•) None | Pin Label Options...

PR Boundary

Shape: Rectangle | Left: 0 | Bottom: 0

Boundary Area Estimation

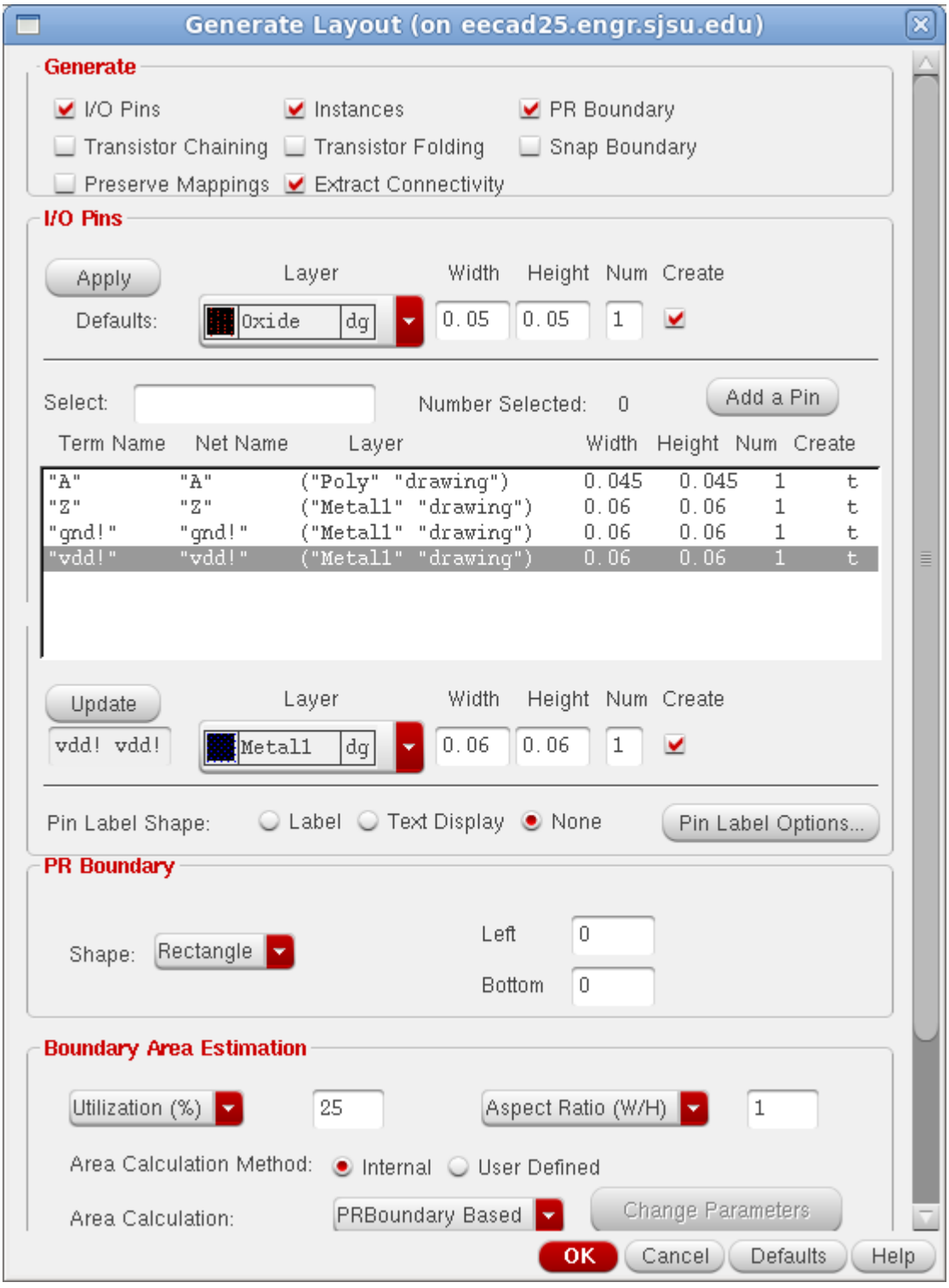
Utilization (%): 25 | Aspect Ratio (W/H): 1

Area Calculation Method: (•) Internal ( ) User Defined

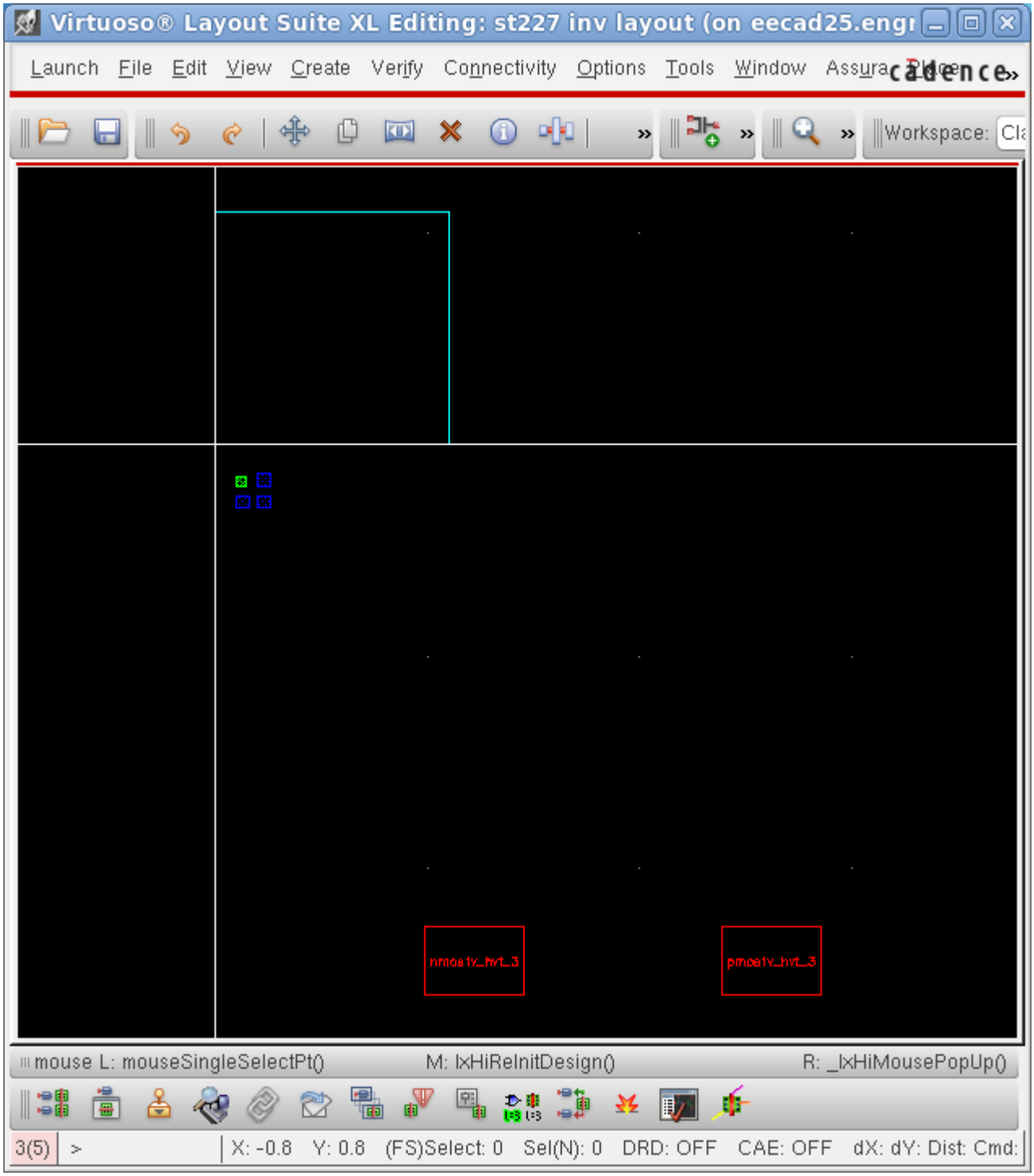
Area Calculation: PRBoundary Based | Change Parameters

OK | Cancel | Defaults | Help

Change the other pins to metal 1



Click OK



The layout items have been created. To improve the view, click <options> then <display>

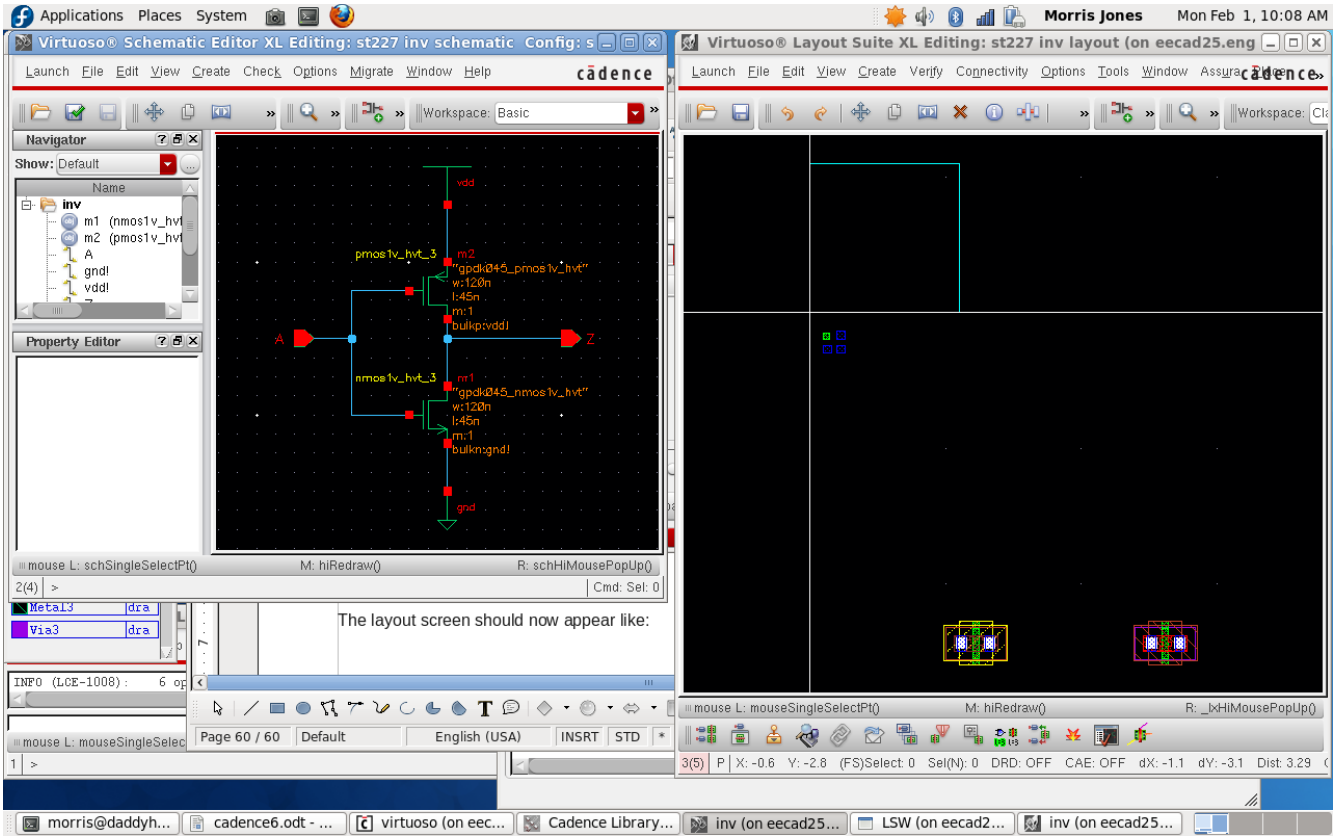
Change the display levels stop near the bottom of the screen to 20.

Set the X and Y snap to 0.025

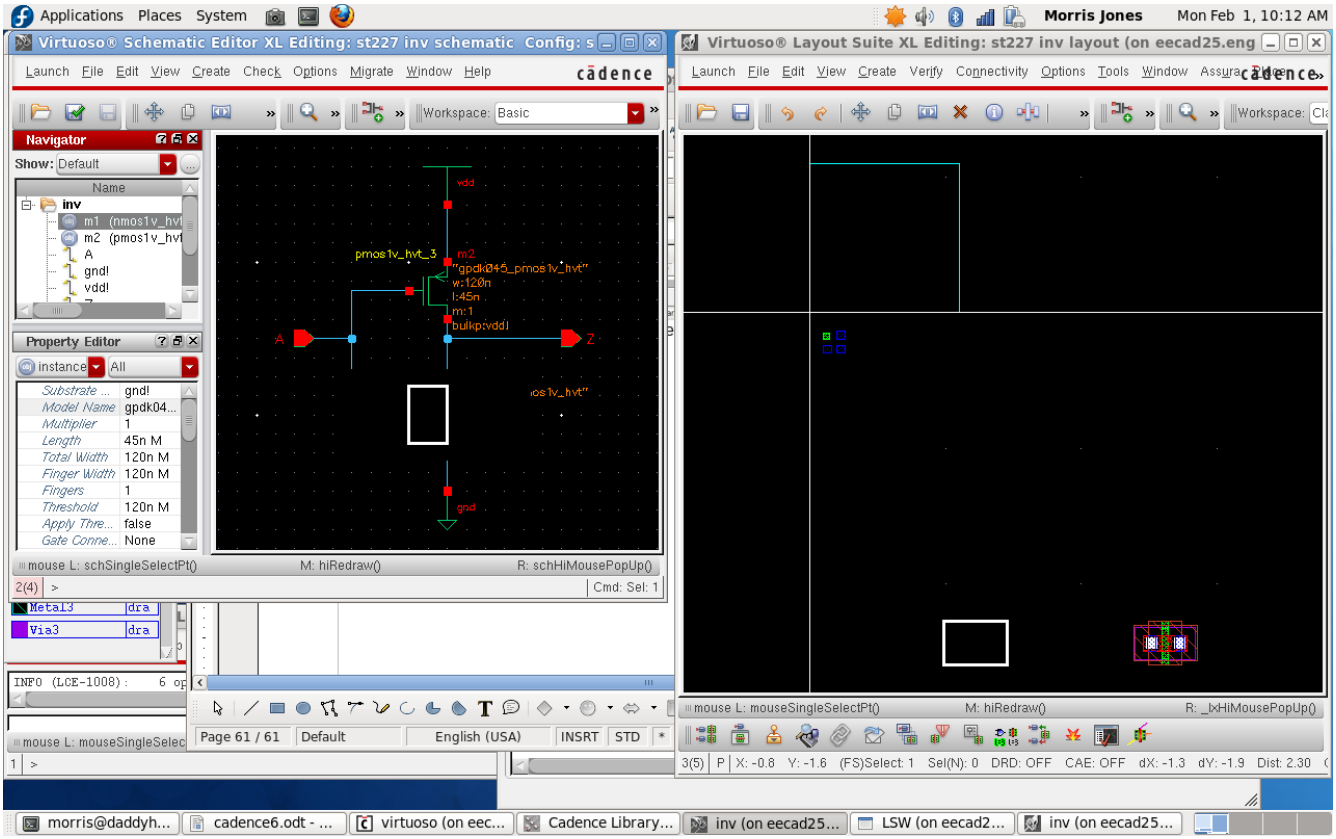
To keep these settings, click save to

Click OK

The layout screen should now appear like:

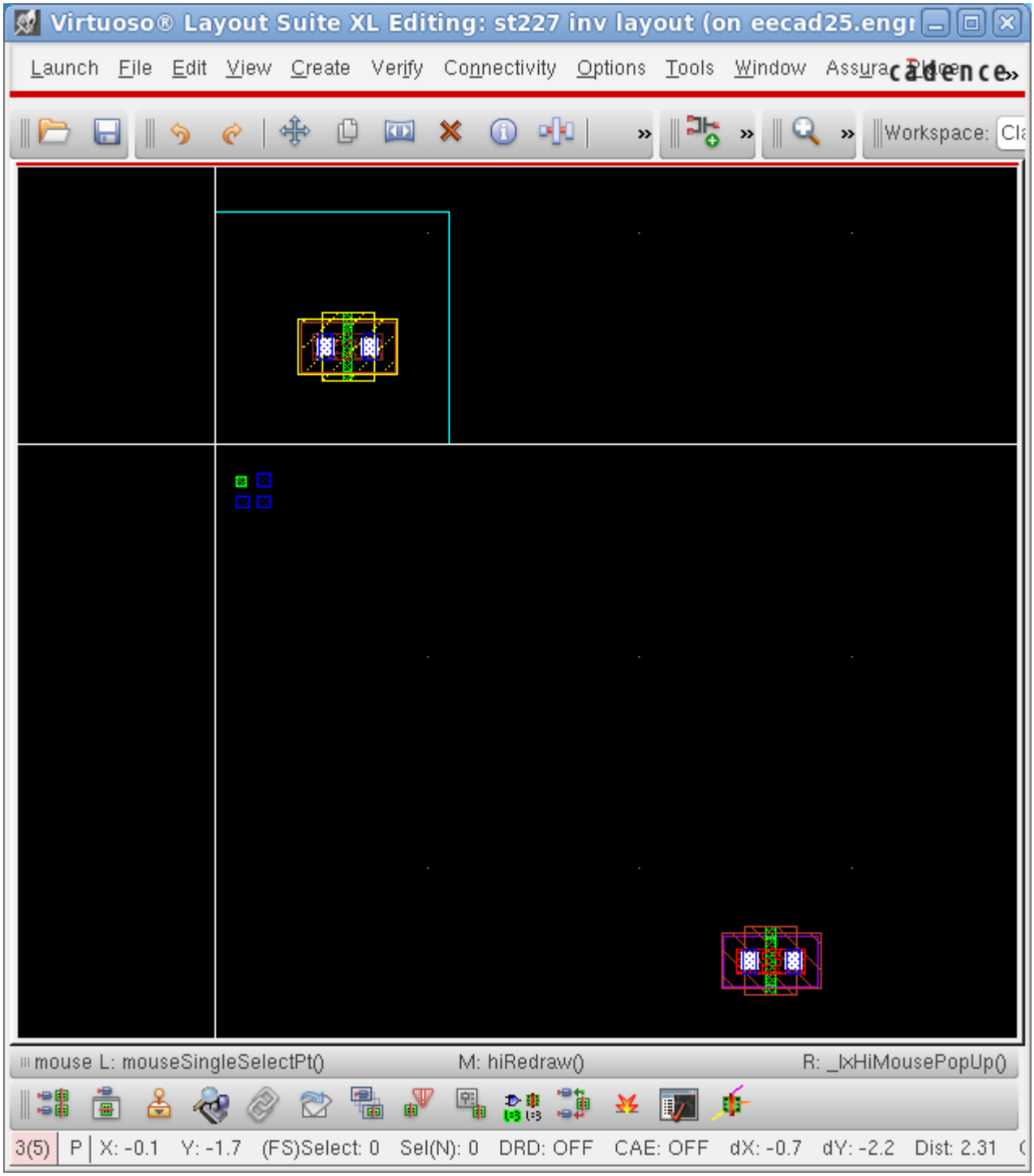


In the navigator window of the schematic screen, select the N transistor. It will be highlighted in the schematic and the layout.



Move the cursor to the N transistor in the layout. Click in the white box, When the cursor becomes a “+”, move the N transistor in the layout until you have it where you want it. On long moves, you can move horizontal, or vertical, but not both. It takes two or more moves. If the image disappears, click <view> then <redraw>

The orange lines that appear indicate what each pin should be connected to on the layout. (This is a big help if you are used to the old Cadence 5).



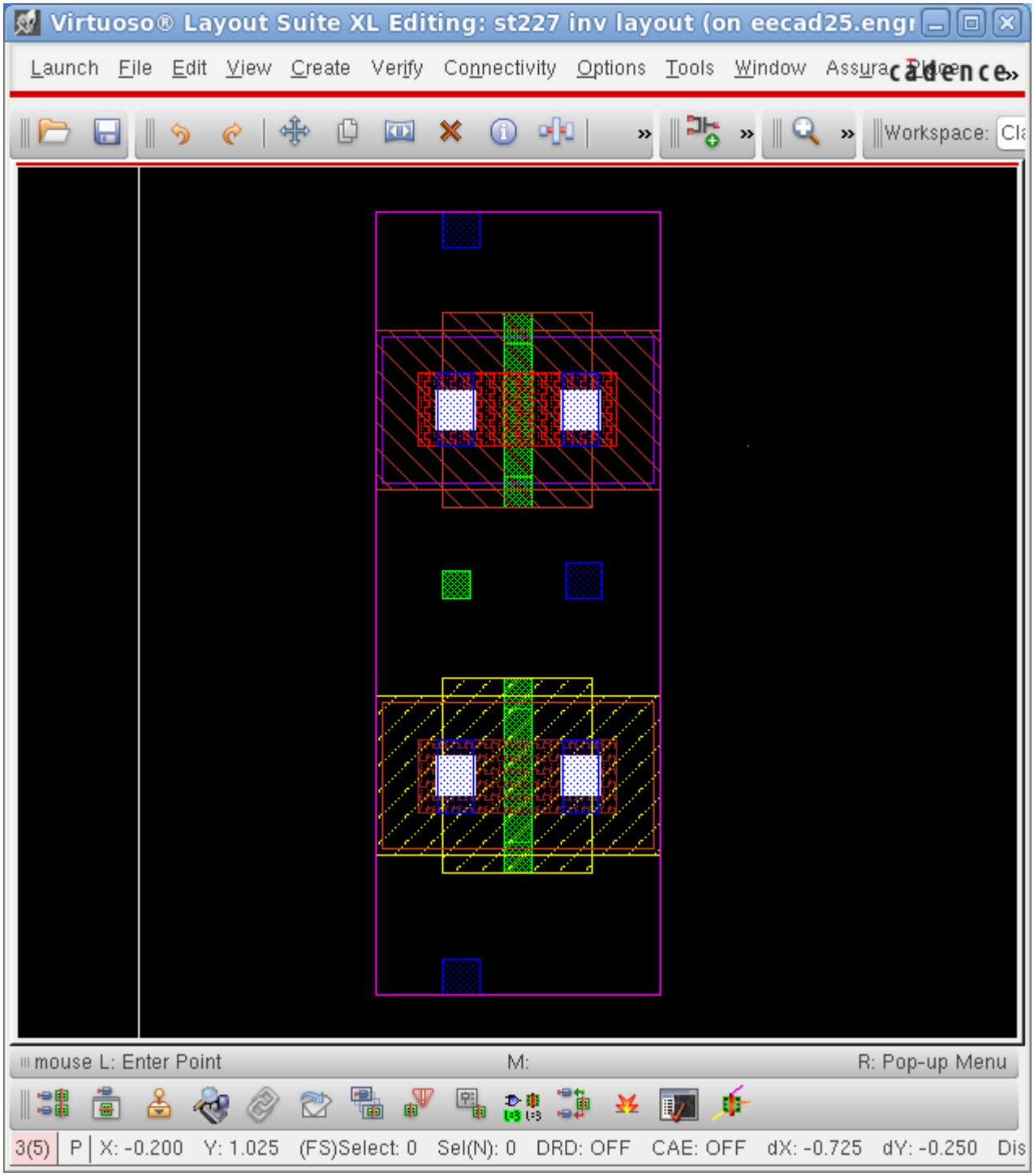
The blue box is for place and route, and isn't needed at this time. Click on it. When it selects

white, click on <edit> then <delete> . It should go away. After press the escape key to exit delete mode.
Now, move the P, and the pins with the Vdd above the P and the ground below the N. I placed the output pin (Z) to the right of the transistors.

This is a good time to save the design by clicking on the floppy disk symbol in the layout window.

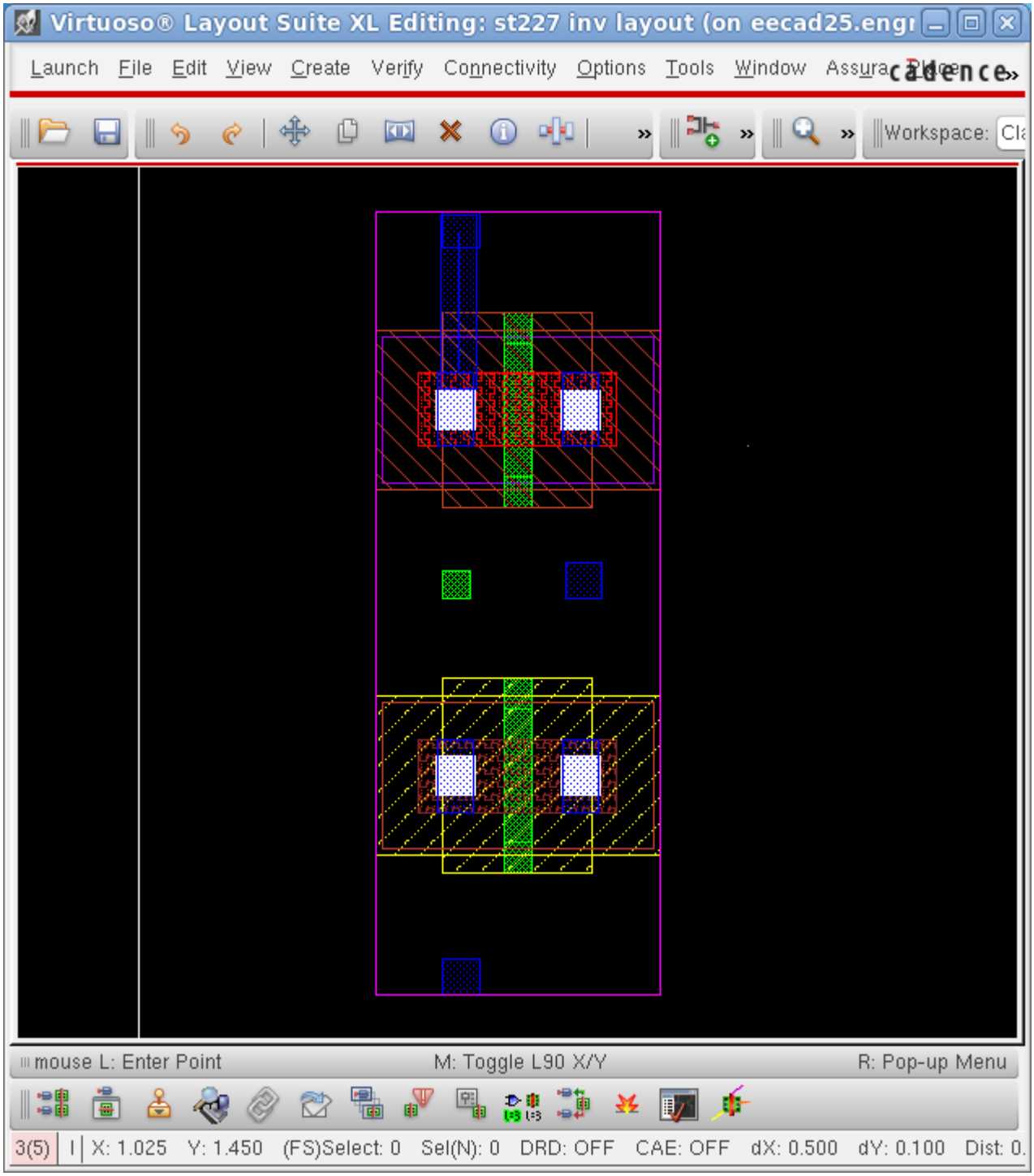
Click on the magnifying glass icon and if required >> then zoom to fit.

You should now have something like:

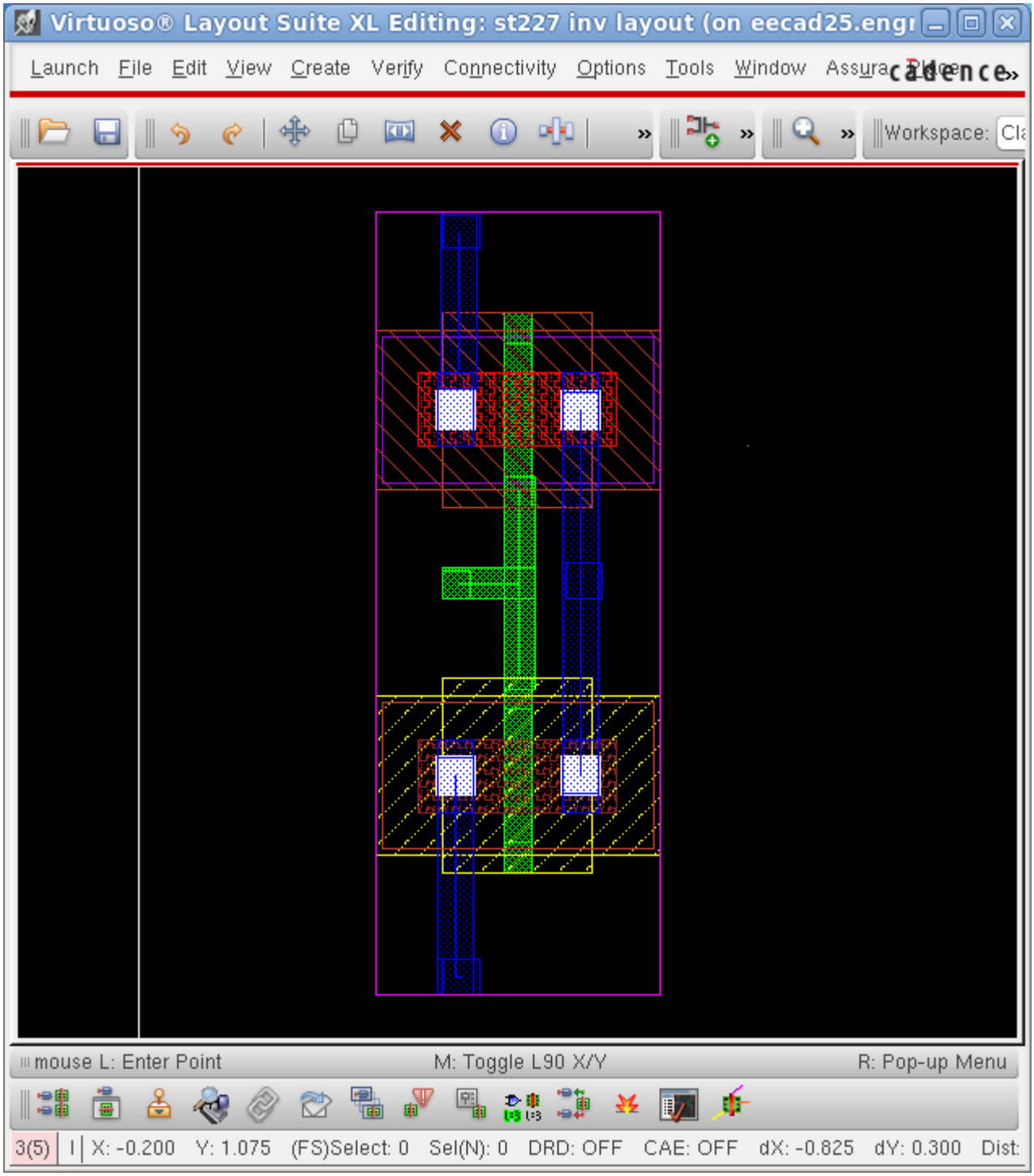


It is now time to start wiring up the elements. This is somewhat automated.
Click on <create> then <wire>, or you can use the menu that starts with the transistor.

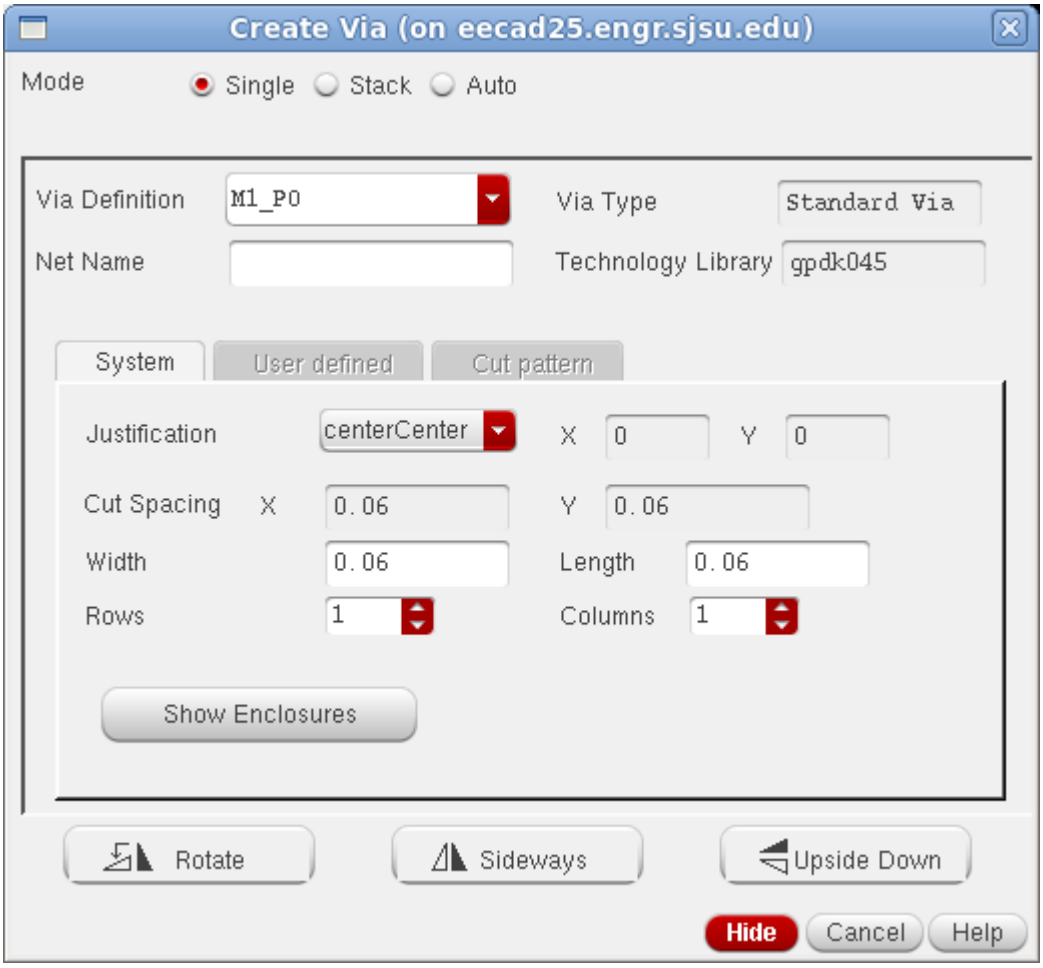
Place the cursor next to the P transistor source Below the Vdd contact. Click. If you get a menu asking which layer to use, select metal 1.
Pull the wire up to the contact, and double click to terminate the wire. You can single click, and then keep adding wire segments. You can change the width of the wire as a property later if required. (As is often the case for analog design).



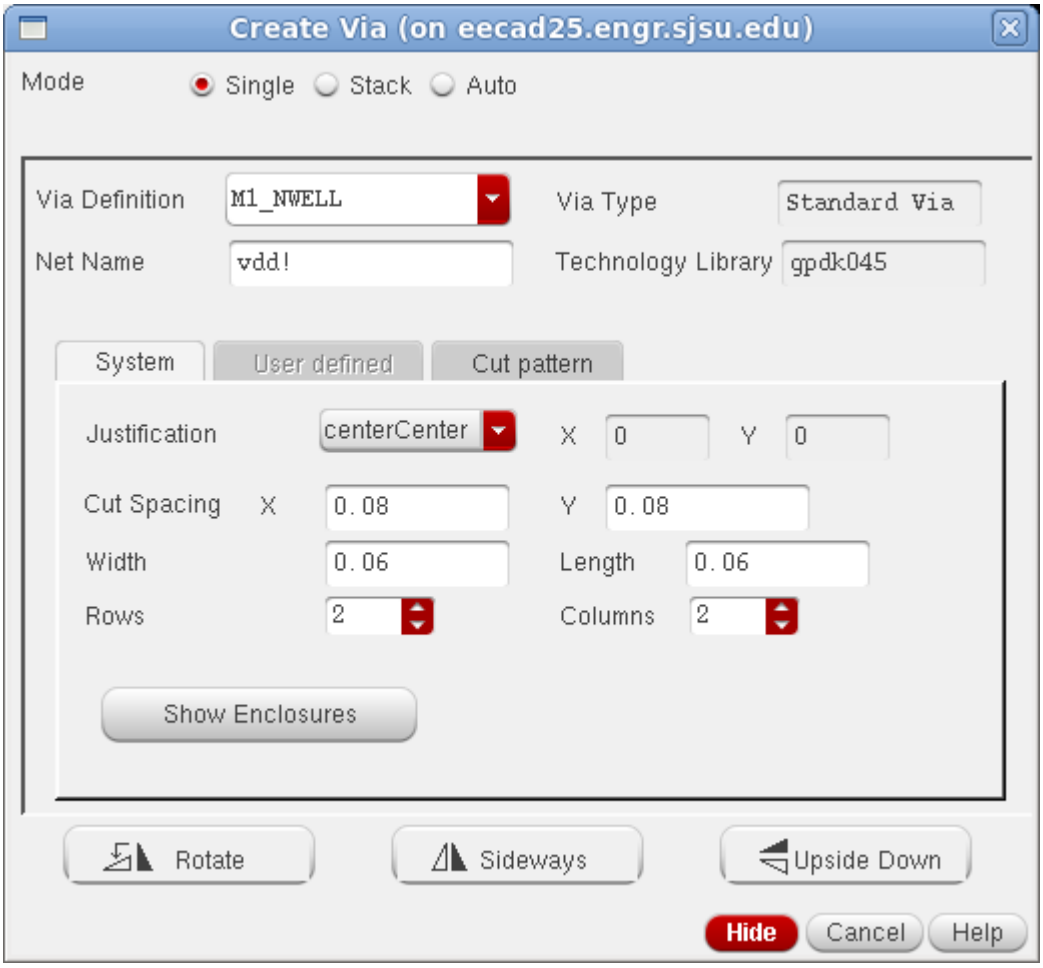
Now, add the rest of the wires. Make sure the gates are connected with poly. (They should route in poly if you start at the gate. No layer changes are required in this design. If they were used, you need to create vias. Your design should look like:



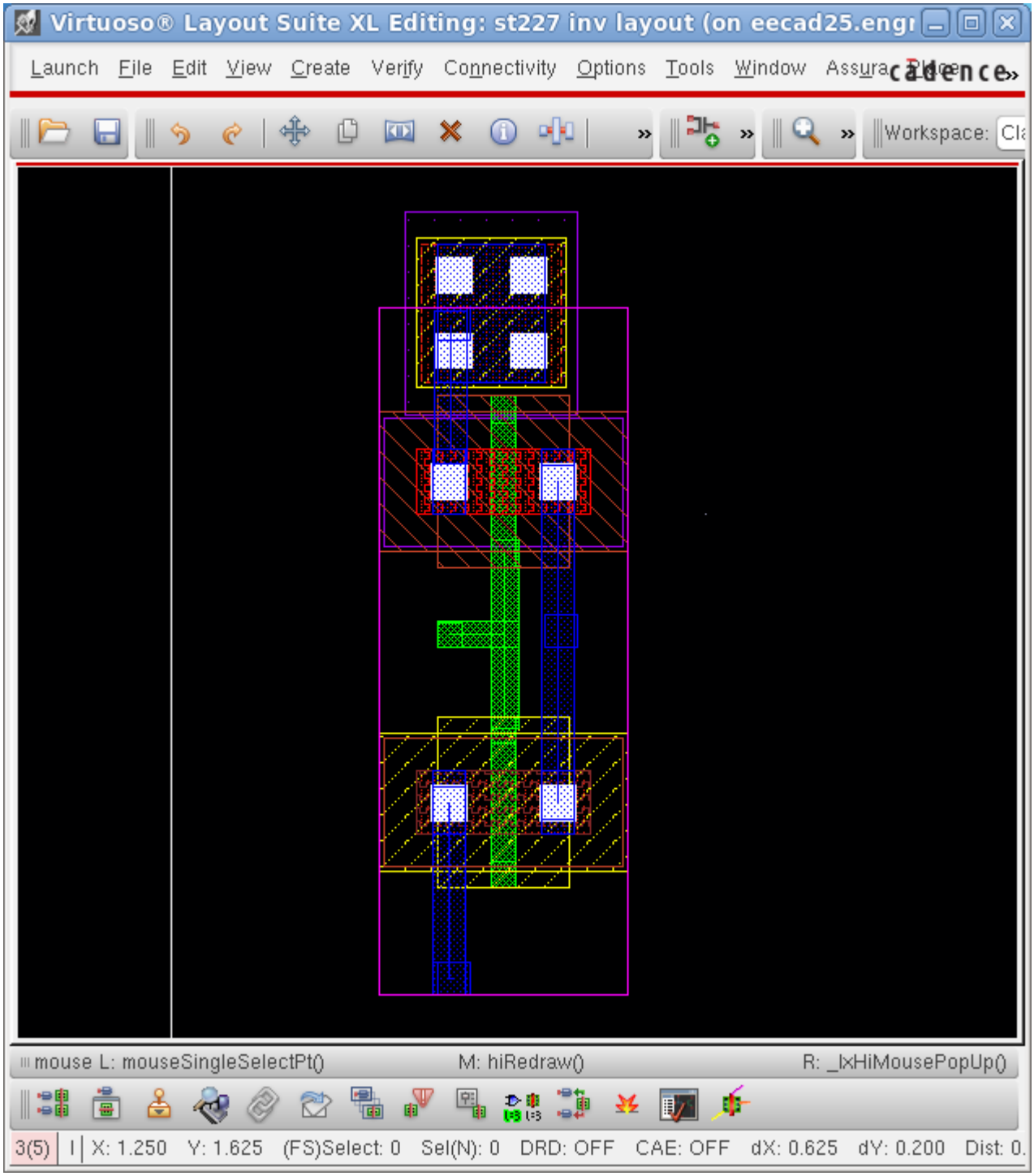
At this point, there are no well contacts. Create them by using the <create> then <via> menu.



Under via definition, use the red pull down arrow, and select m1_nwell, place vdd! As the net name. Change the rows and columns to 2. (You can use the arrows)



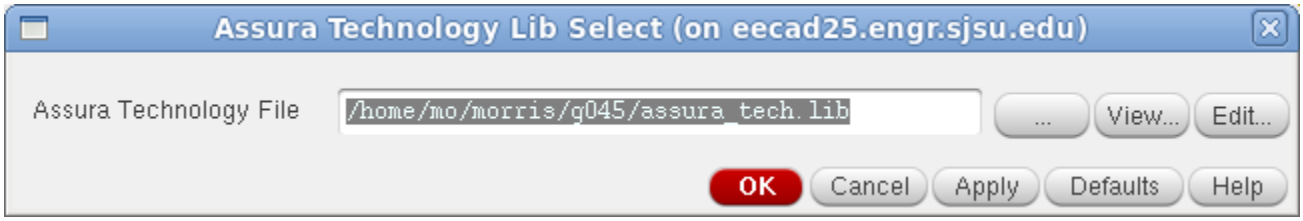
Move to the layout and place the contact above the P transistor.



Now, do the same for M1 to p substrate. Place it below, and name it gnd!
Then click the floppy disk to save the file.

It is now time to set up the Assura for DRC and LVS. We will not be using the DIVA DRC or LVS with this technology. (You will like Assura more as you get used to it).

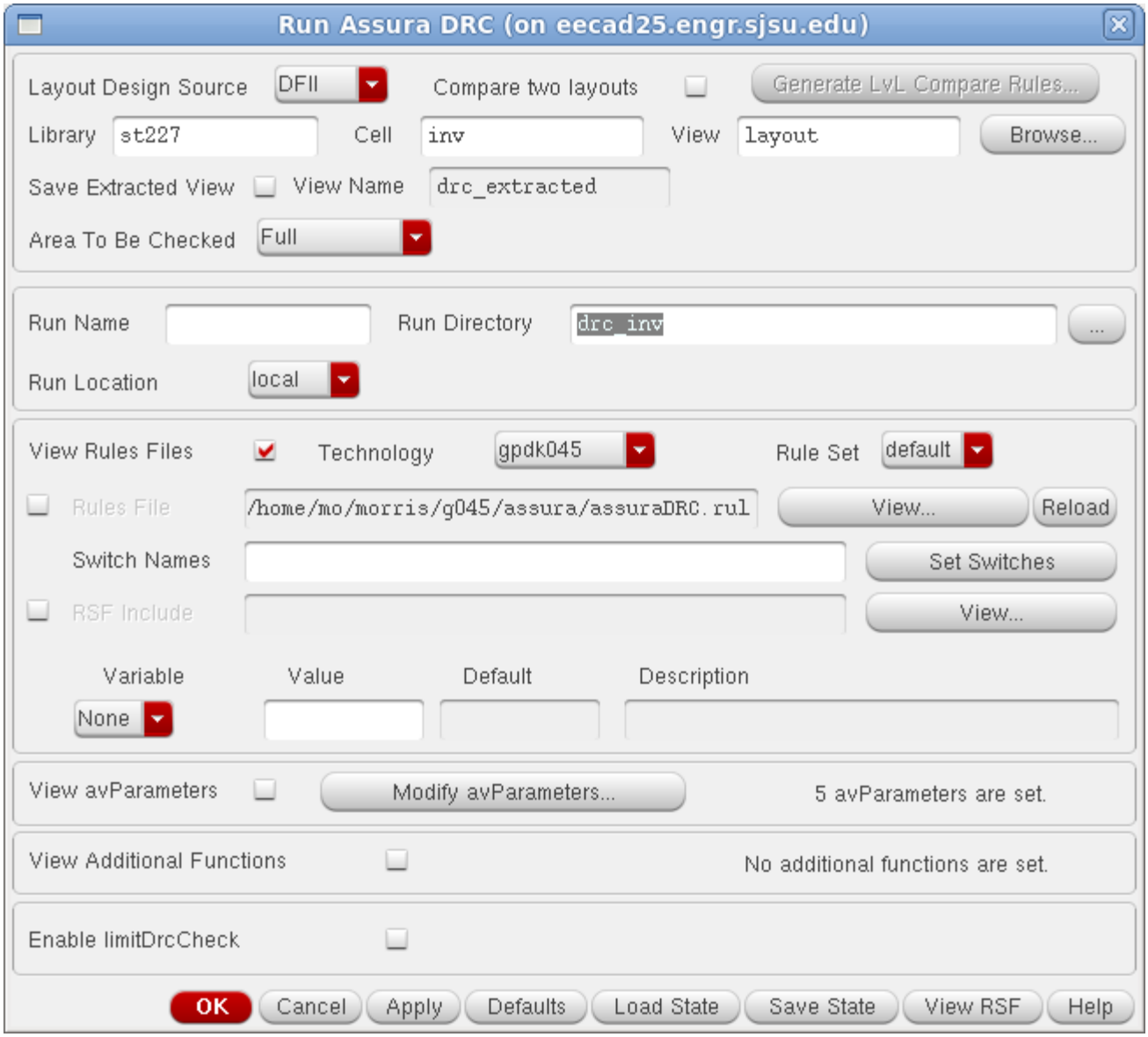
First, click on <Assura> and then on <Technology> Type in the name of the assura library as shown below:



click <OK>

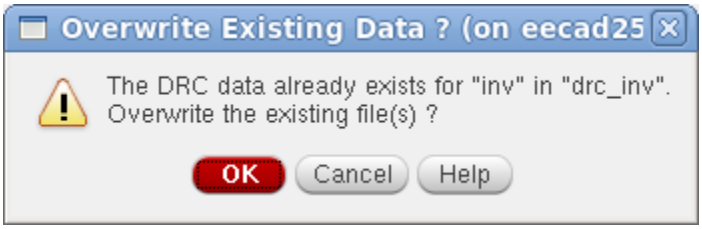
In the layout screen, click on <assura> and then <run DRC>

Filll the screen out with the directory name as drc_inv, select the technology as gpdk045 as shown below:



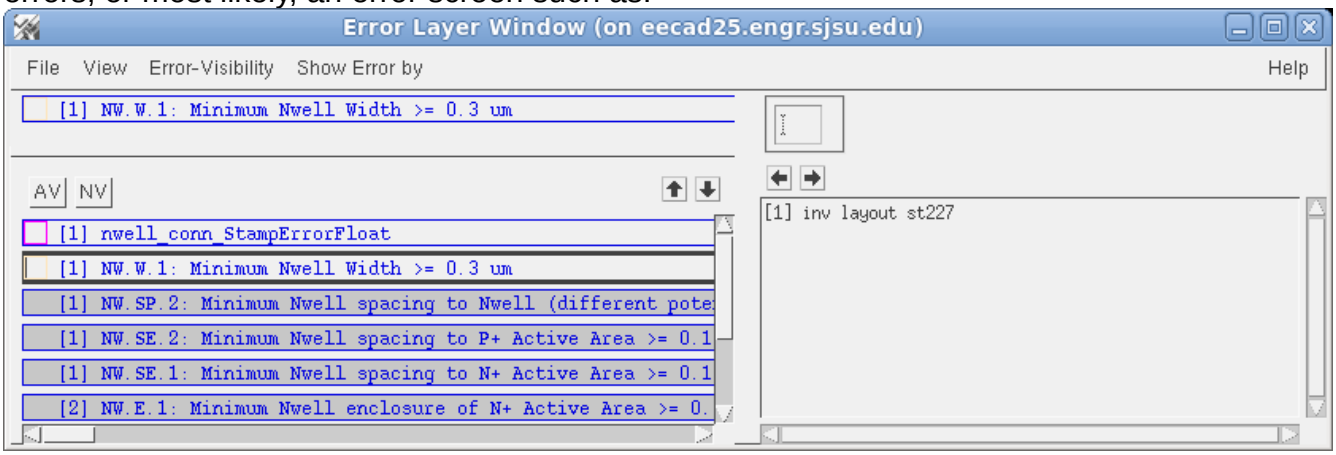
click OK. It will take a while.

If you get a message:



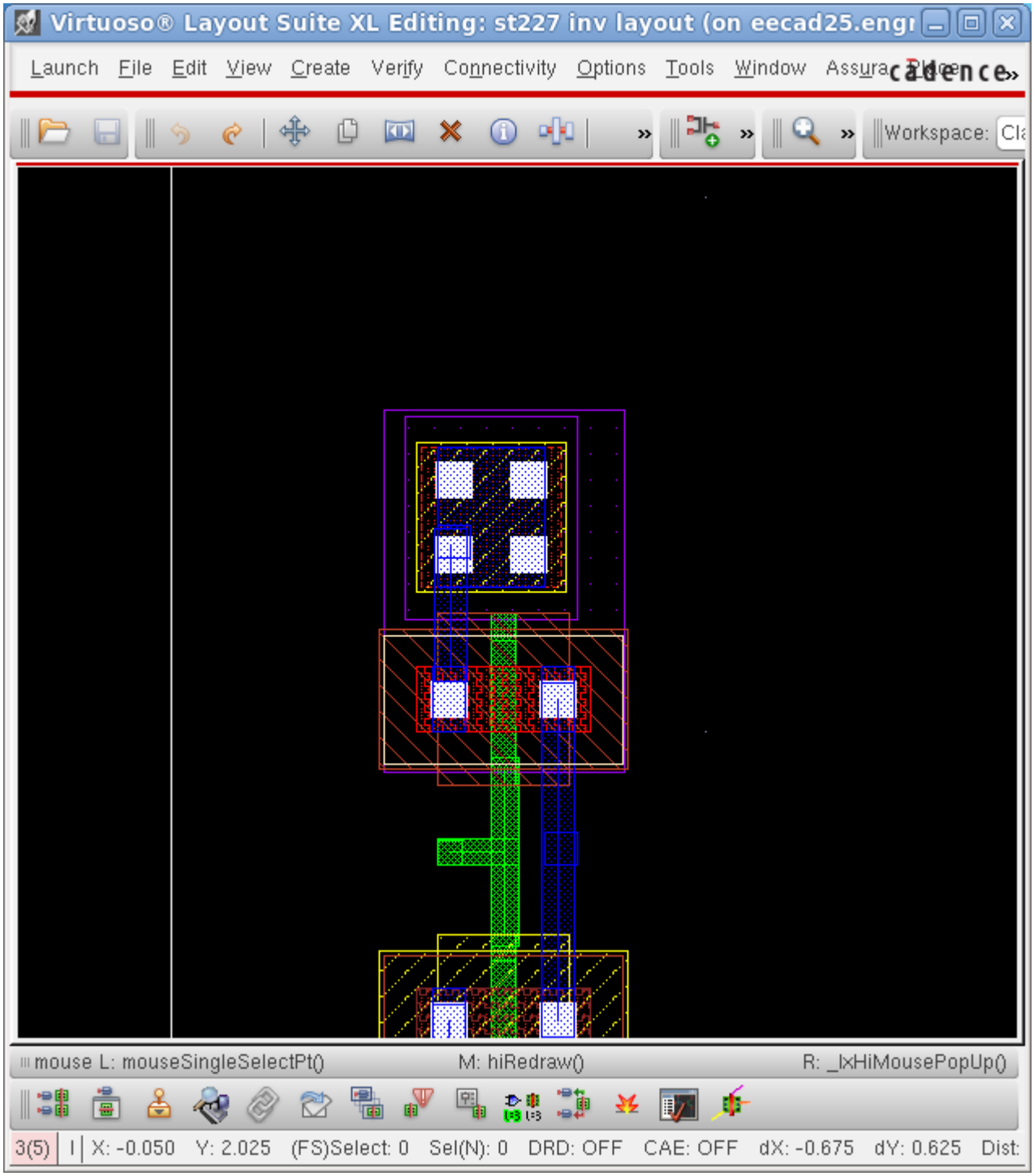
Just click OK. If not, don't worry about it.

You may get some overwrite windows. Eventually, you will get a screen saying there were no errors, or most likely, an error screen such as:

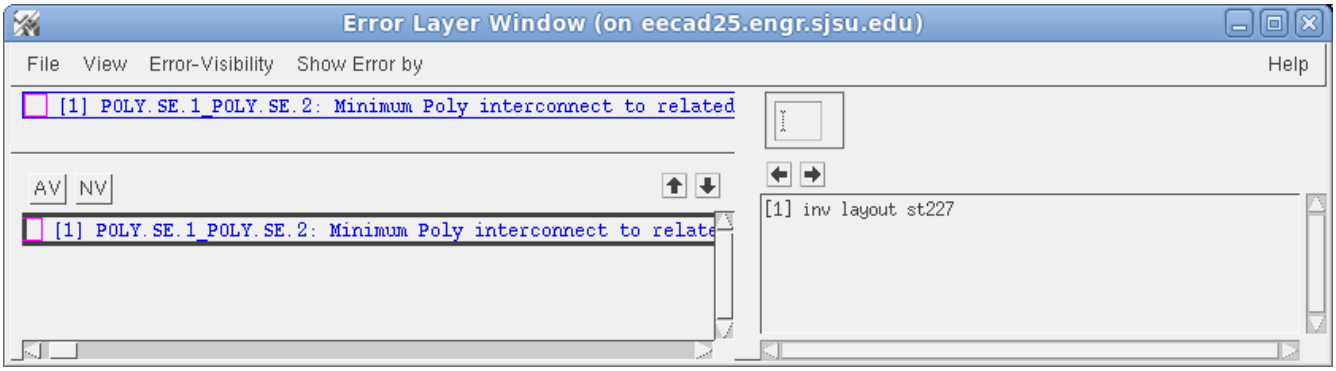


Each error is explained. If you click on an error, it will show the problem on the layout.

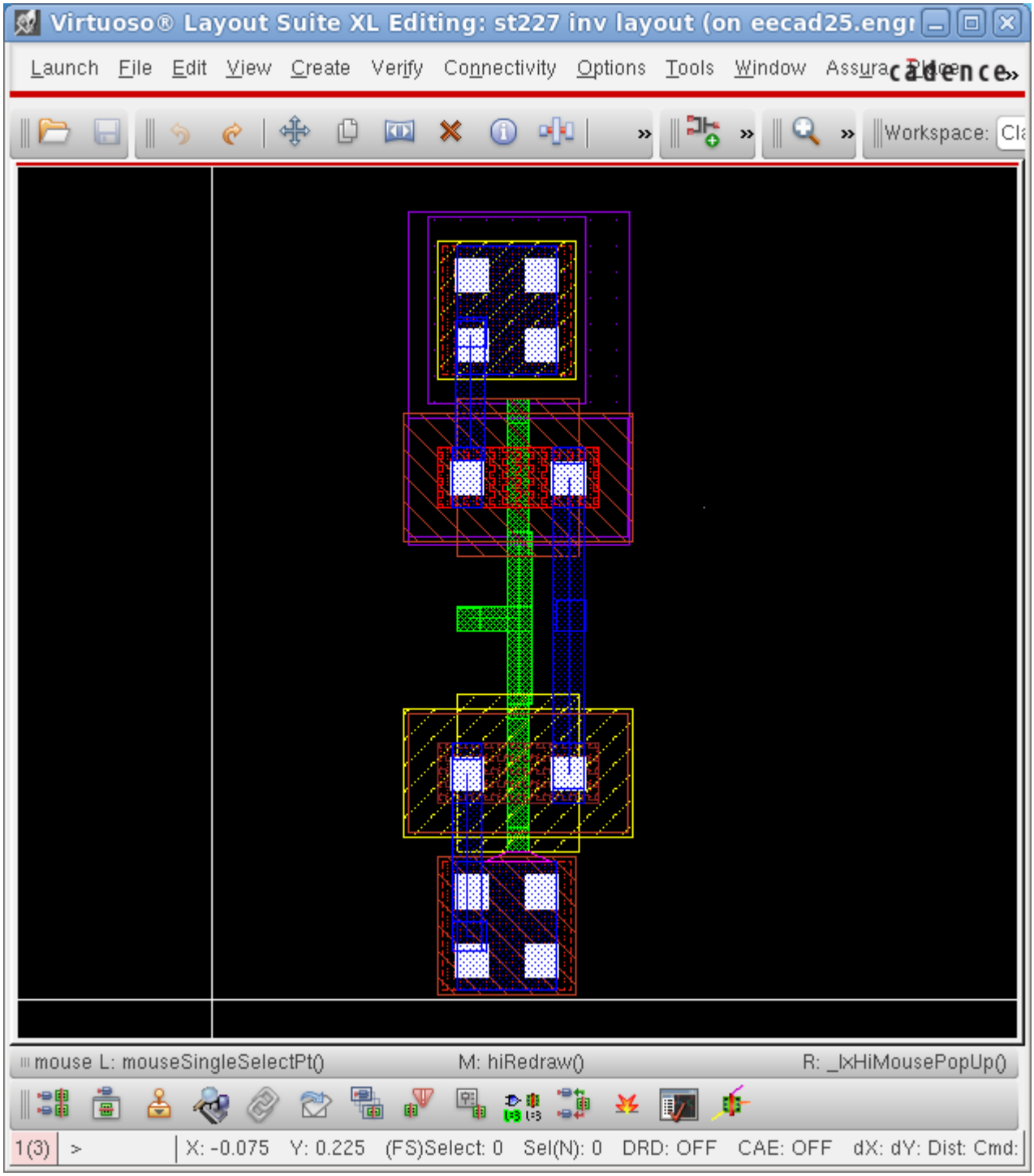
These come from not having a proper N-Well. I'll add a rectangle of N-Well to the layout. Click <create> then <shape> then <rectangle> On the LSW screen, select Nwell. Click on one corner, and drag to the other corner. Release the mouse. I moved the contact higher in the well. You should have:



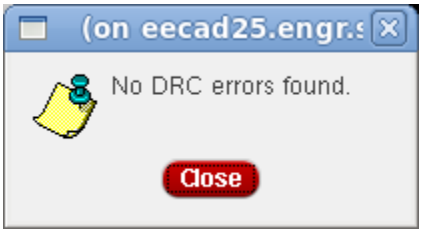
Click the save floppy, then run the DRC again.
I still have one error



Select the error, and then click on <Show Error by> and then <Edit in Place> . The error will show up on the layout. This is my example:



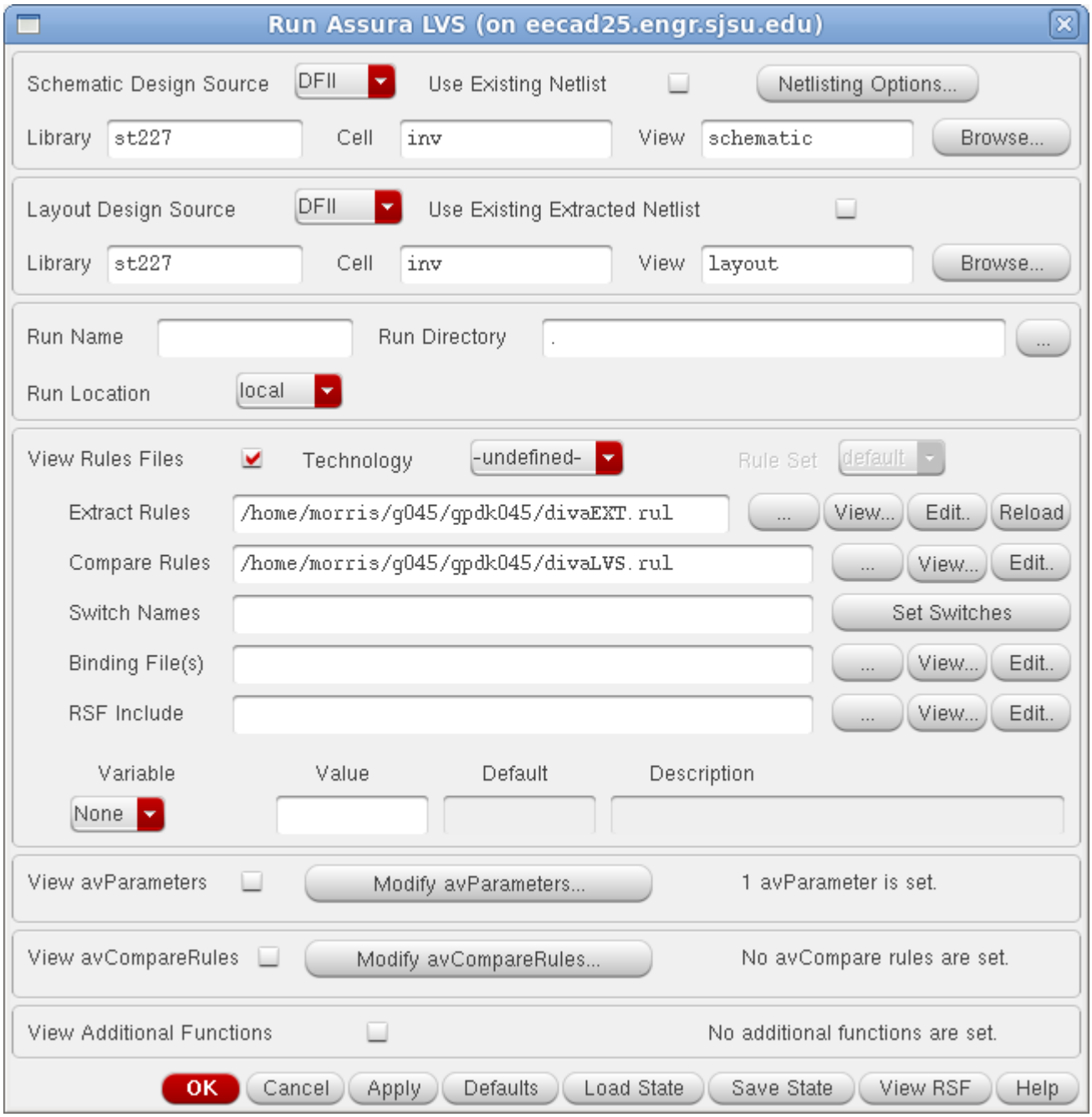
The purple area shows the problem is the spacing from the poly to the contact is too close. Move it down a little, and then save it and run DRC again.



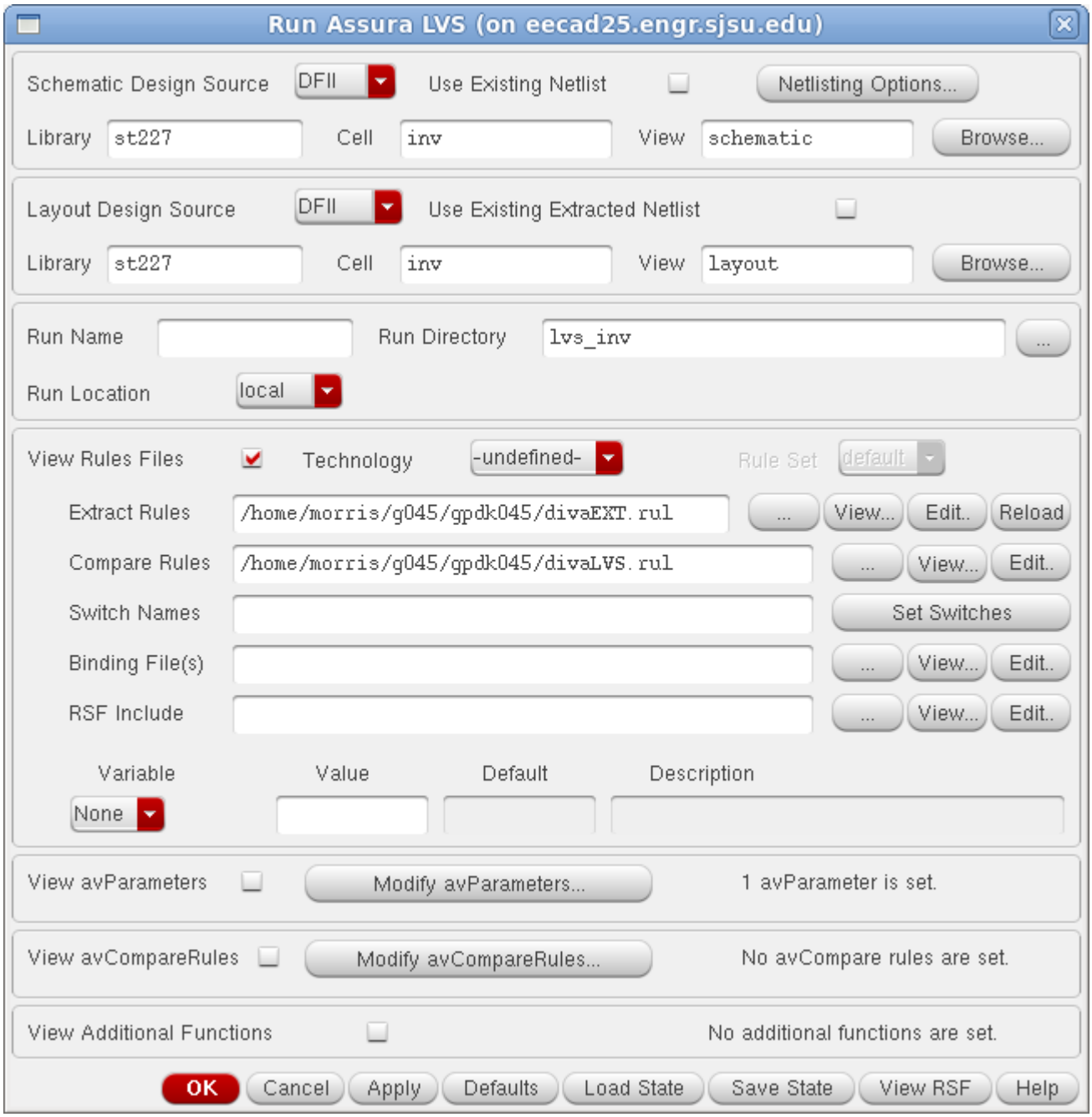
The DRC is now OK.

Now to run LVS and check it to the schematic.

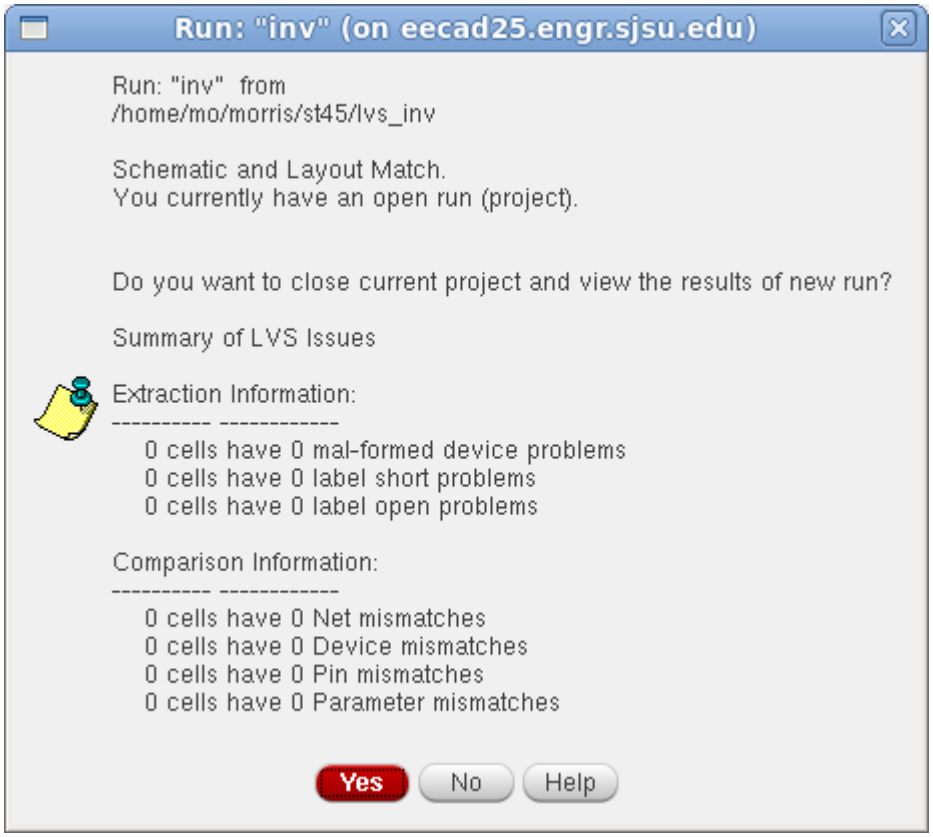
Click on <assura> then <run LVS> You will get a screen like:



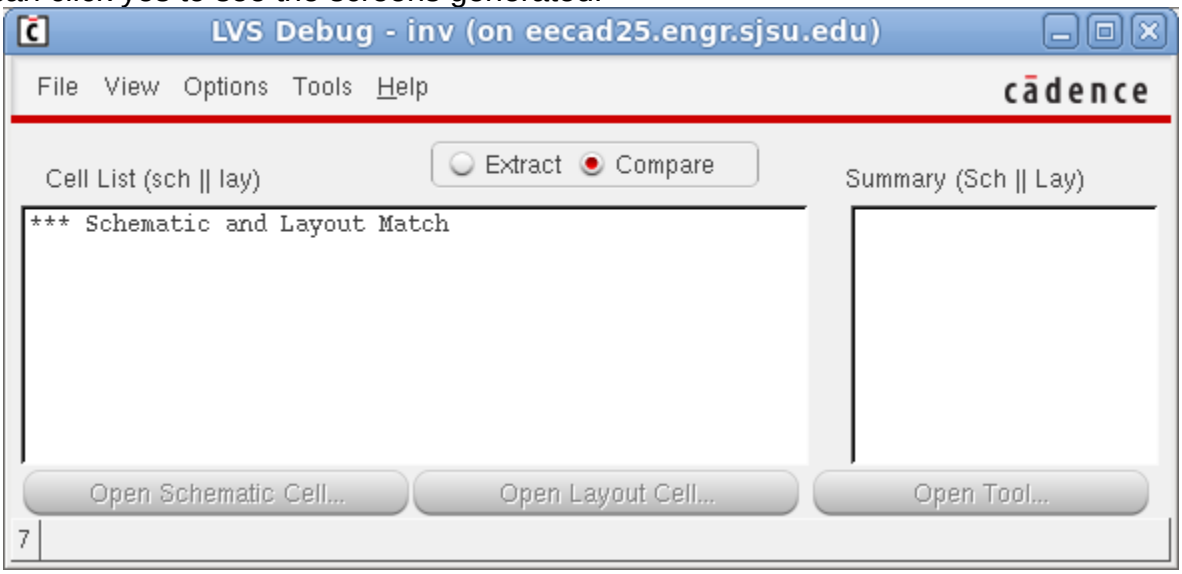
Change the run directory to lvs_inv, and then click OK.



The LVS takes a while to run. Since this is a simple design, there are no errors.



You can click yes to see the screens generated.



If there were errors, this screen would help find them.

Congratulations, you now have an inverter. The power and ground busses should be expanded by placing a rectangle of M1 that goes to the cell edge. There is always more to do. The poly might want a via to M1.