Sequential Circuit

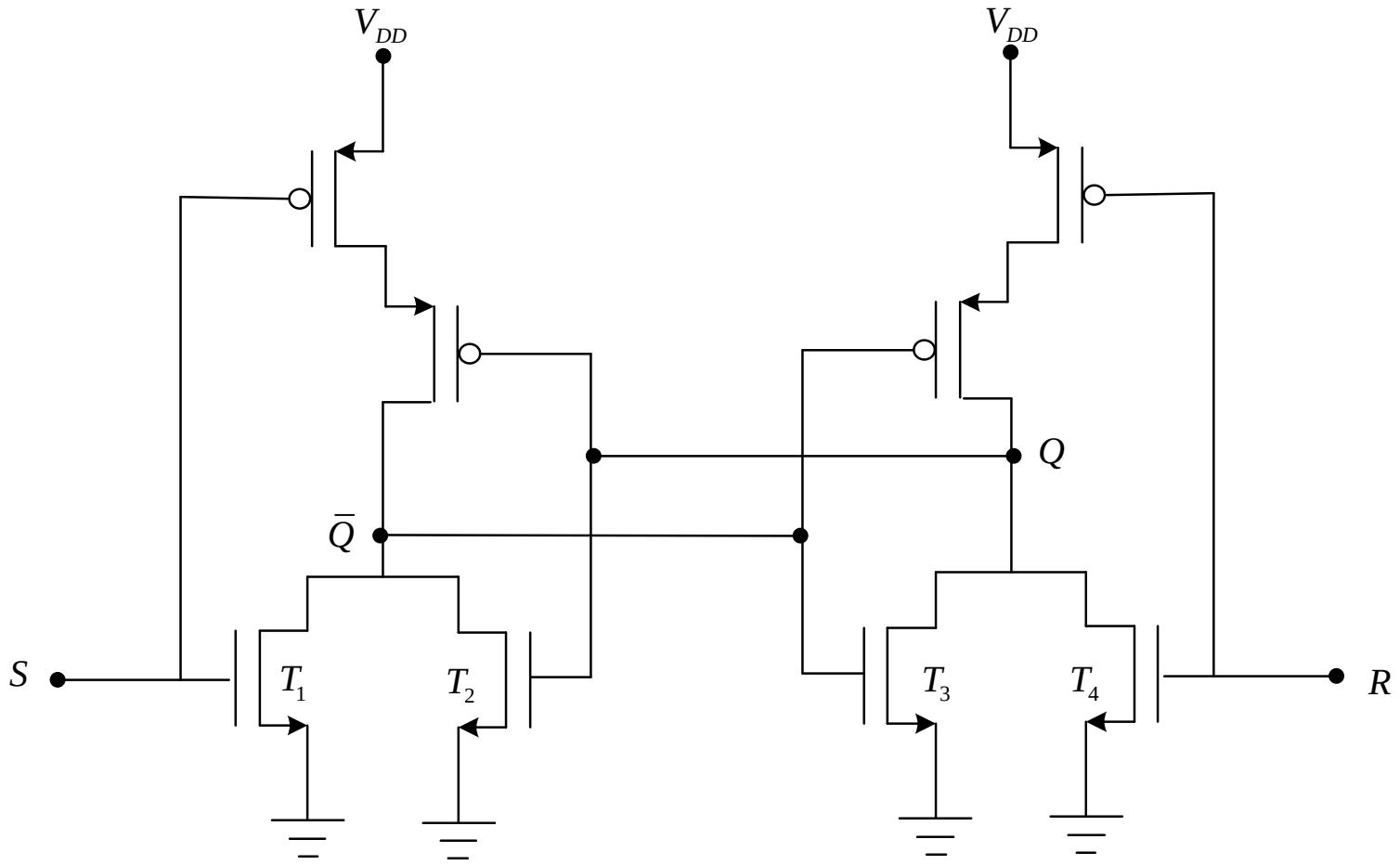
Lecture 15

- Gates:
  - Acyclic logic gates, no memory, no clock
  - Cyclic
- Gates:
  - Sequential circuits: Output depends on present & previous inputs.
  - Combinational logic: Output of circuit depends only on the input.
- Gates:
  - Non regenerative circuits: (no feedback between I/O)
  - Regenerative (feedback between I/O)

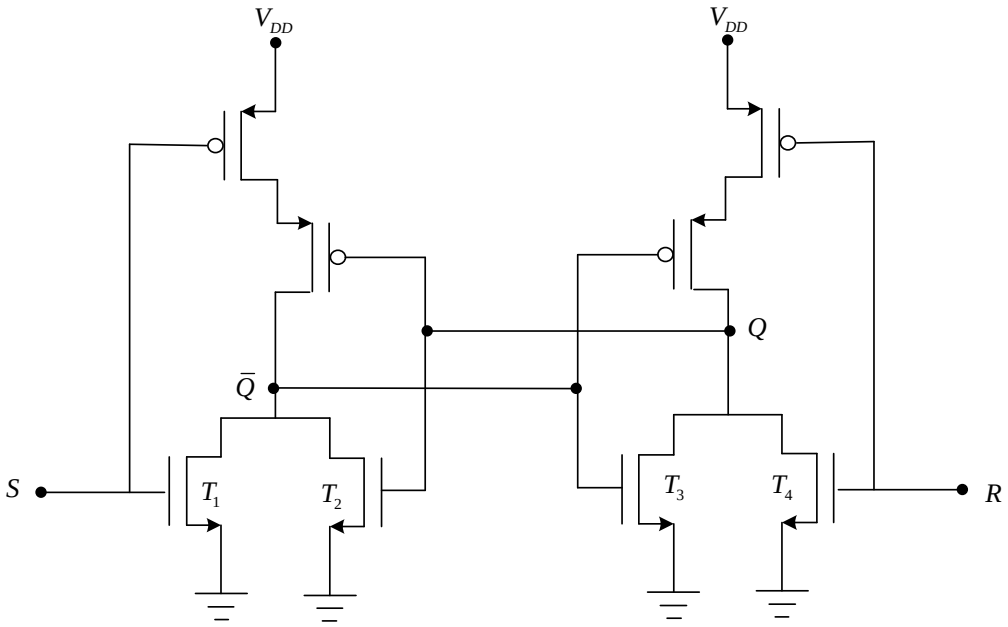
- Regenerative circuits (Class of multivibrators):
- Bi-stable circuits (circuit under certain input & output condition has 2 stable states, example, flip-flops, latches, registers)
- Mono-stable circuits (one stable state even with external perturbation)
- Astable circuits (circuit cannot preserve stable state for certain time, example, ring oscillator)

- SR Latches:
- Have two complementary outputs Q and $\bar{Q}$
- Two triggering input: Set (S) and Reset (R).
- Set state: $Q = 1 \text{or High}$ and $\bar{Q} = 0 \text{ or low}$
- Reset state: $Q = 0$ and $\bar{Q} = 1$
- Hold its states as long as power supply voltage is provided
- Added switches to cross-coupled inverter to allow change of the state by external triggering by overpower the feedback loop.

- Asynchronous CMOS NOR-Gate Based SR Latch:

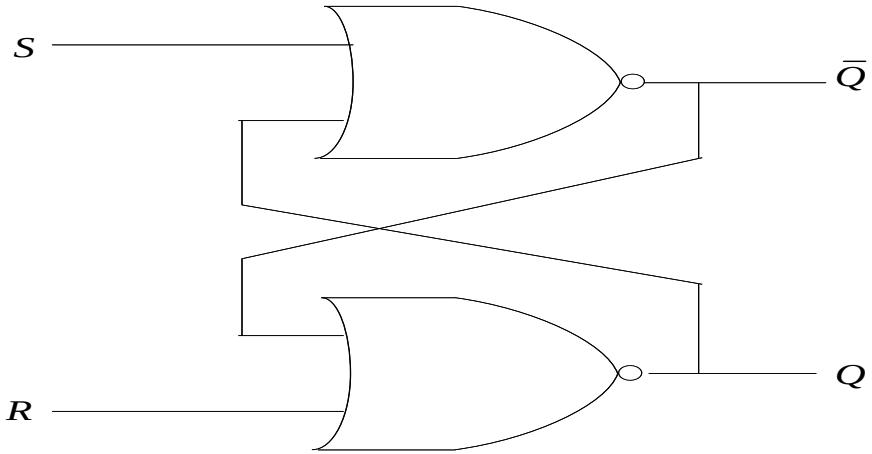


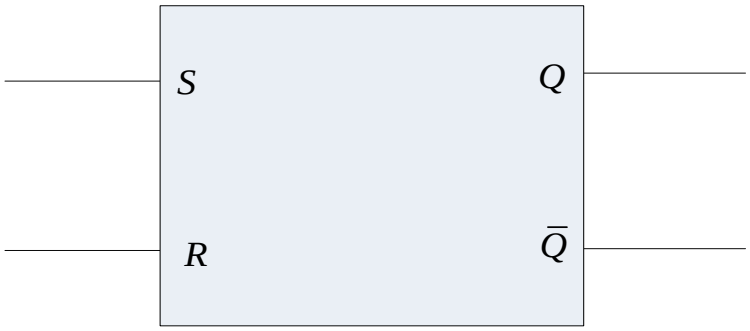
- Asynchronous SR Latch Operation:



- Set Operation: Set: High, Reset: Low, Q: High, $\bar{Q}$: Low. Regardless of previous stage
- Reset Operation: Reset: High, set: Low, Q: low, $\bar{Q}$: High. Regardless of previous stage
- Not allowed condition: Set: High, Reset: High, Q: Low, $\bar{Q}$: Low. Contradictiory.
- Previous state: Set: Low, Reset: Low, $Q_n : Q_{n-1}$, $\bar{Q}_n : \bar{Q}_{n-1}$.

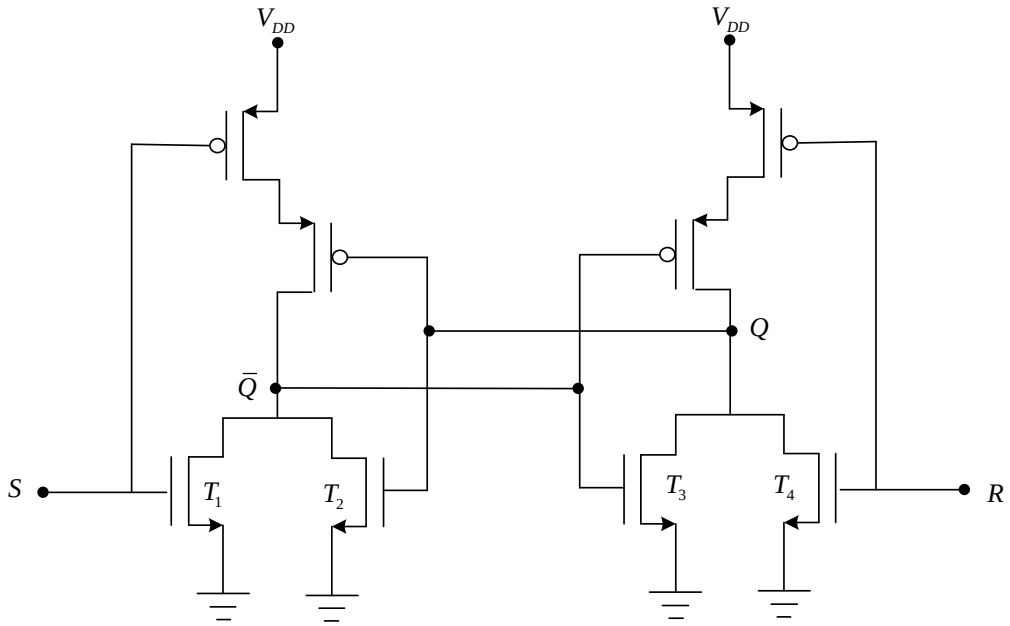
- Asynchronous SR Latch NOR Gate Based:





R	S	Q_n	$\bar{Q}_n$	Operation
0	0	Q_{n-1}	$\bar{Q}_{n-1}$	Hold
1	0	1	0	Set
0	1	0	1	Reset
1	1	0	0	Forbidden State

- Asynchronous SR Latch Operation:



S	R	Q	$\bar{Q}$	Operation
V_{OH}	V_{OL}	V_{OH}	V_{OL}	T_1 and T_2 : ON T_3 and T_2 : OFF
V_{OL}	V_{OH}	V_{OL}	V_{OH}	T_1 and T_2 : OFF T_3 and T_2 : ON
V_{OL}	V_{OL}	V_{OH}	V_{OL}	T_1 and T_4 : OFF T_2 : ON or
V_{OH}	V_{OH}	V_{OL}	V_{OL}	T_1 and T_4 : OFF T_3 : ON

- SR Latch Transient response: (Consider a state change)
- Apply set signal, output nodes undergo voltage transition from logic low to logic high.
- Or apply reset signal, output nodes undergo voltage transition from logical high to logical low.
- Both of the output nodes undergo a state change simultaneously in either case
- Estimate the amount of time required for the simultaneous switching of the two output nodes.
- Exact solution requires the simultaneous solution of two coupled differential equations, one each for each output node.
- Simplified solution with an overestimation of switching time are possible by assumption of two events take place in sequence rather than simultaneously.

- SR latch switching time:
- Find the total parasitic capacitance associated with each output node.

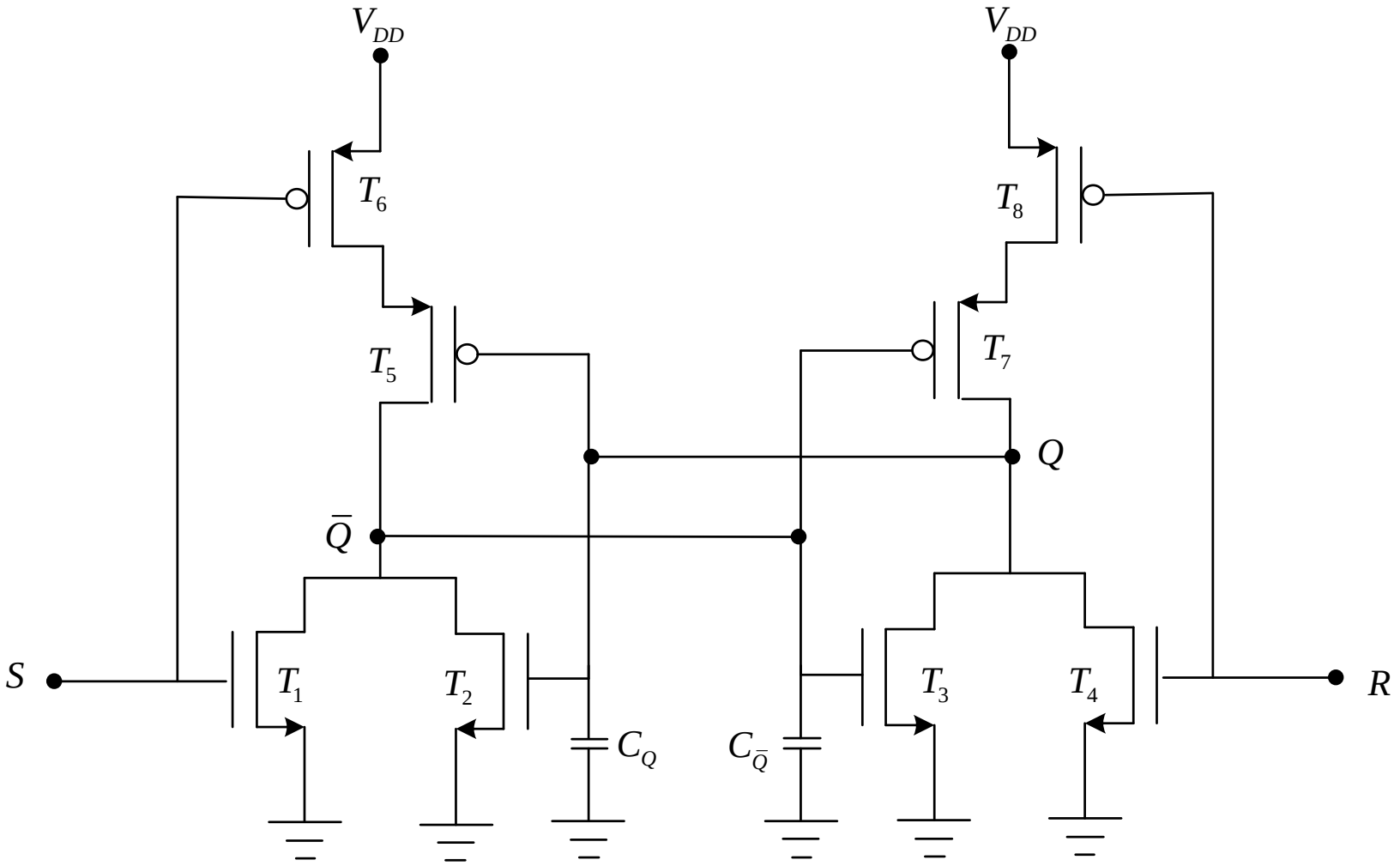
$$C_Q = C_{gb,2} + C_{gb,5} + C_{db,3} + C_{db,4} + C_{db,7} + C_{sb,7} + C_{db,8}$$

$$C_{\overline{Q}} = C_{gb,3} + C_{gb,7} + C_{db,1} + C_{db,2} + C_{db,5} + C_{sb,5} + C_{db,7}$$

- Assuming that the latch is initially reset and that a set operation is being performed by applying $S = 1$ and $R = 0$.
- The rise time of node Q is:

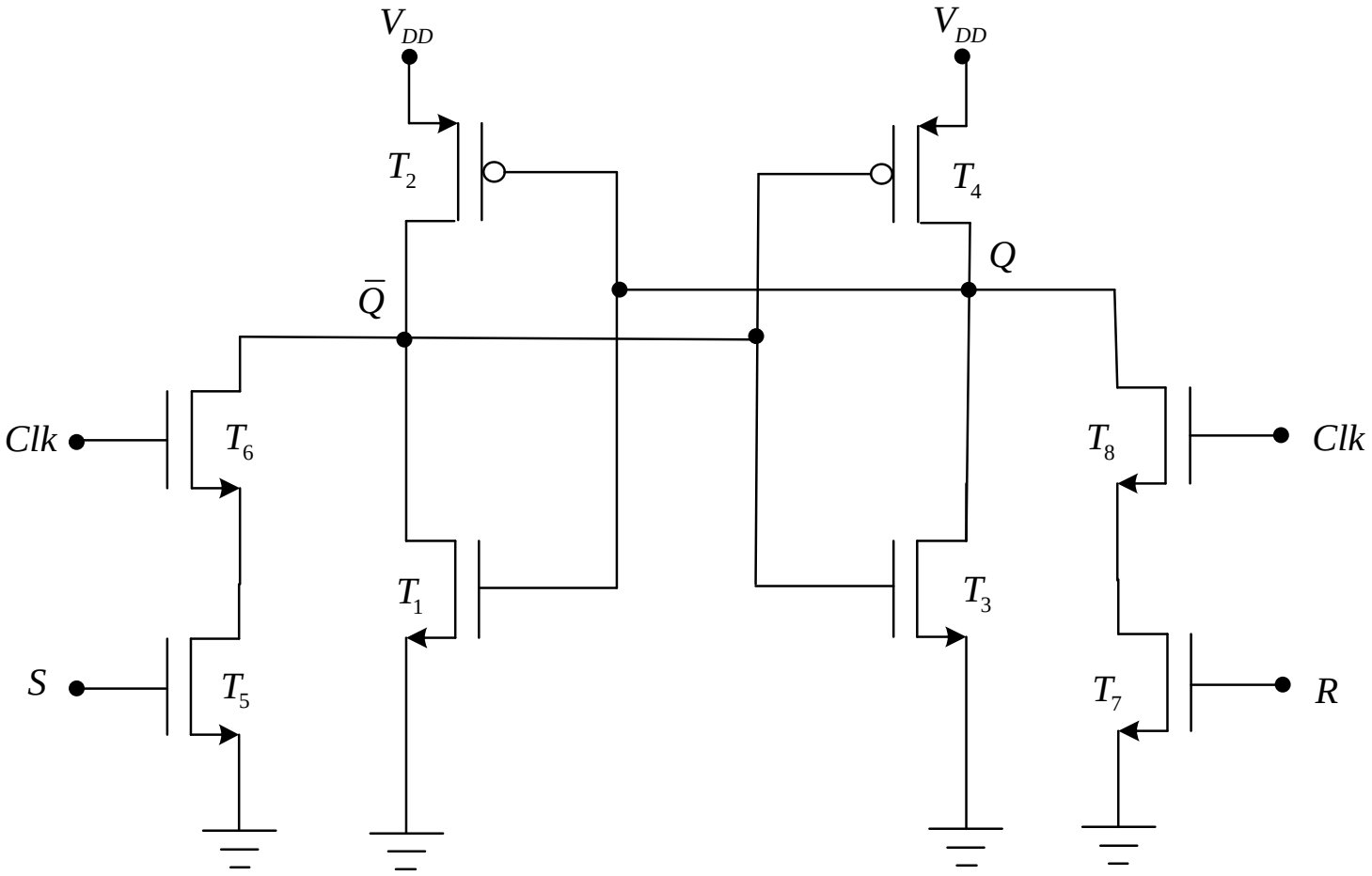
$$\tau_{\text{rise,Q(SR-Latch)}} = \tau_{\text{rise,Q(NOR-gate)}} + \tau_{\text{fall,}\overline{\text{Q}}\text{(NOR-gate)}}$$

- Asynchronous CMOS NOR-Gate Based SR Latch with Lumped Capacitors:

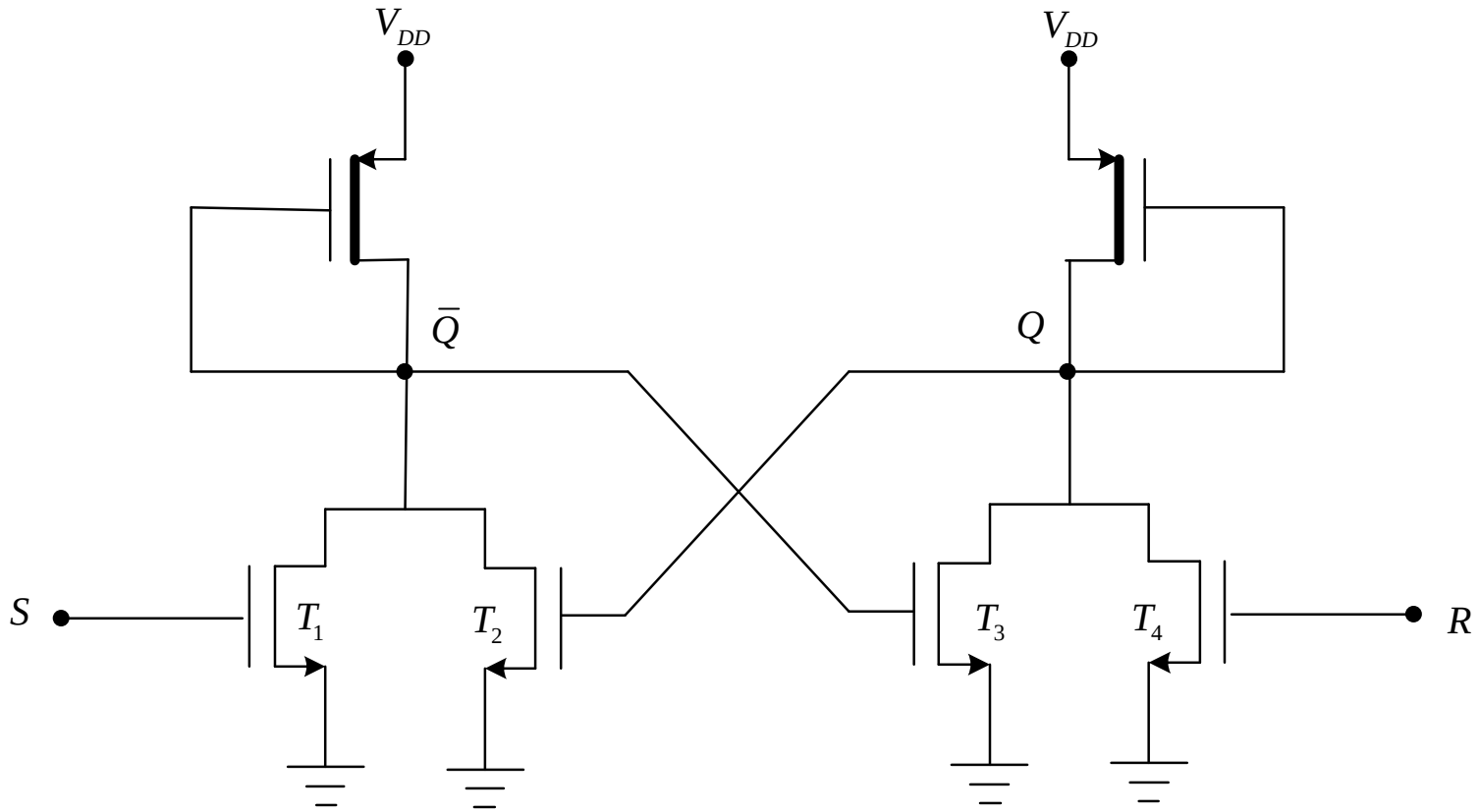


- Calculation of switching time $\tau_{\text{rise,Q(SR-Latch)}}$ requires two separate calculation for NOR gates.
- Two steps calculations:
- ❶ The output node voltage $\overline{Q}$ falling from high to low, due to turn on of T_1. Find $\tau_{\text{fall,}\overline{\text{Q}}\text{(NOR-gate)}}$
- ❷ The output node voltage Q rising from low to high, due to turn-off of T_3 . Find $\tau_{\text{rise,Q(NOR-gate)}}$
- Both T_2, and T_4 can be assumed to be off in this process. Although T_2 can be turned on as Q rises, thus shortening the $\overline{Q}$ node full time. (This is cause of over-estimation)

- Synchronous SR Latches:

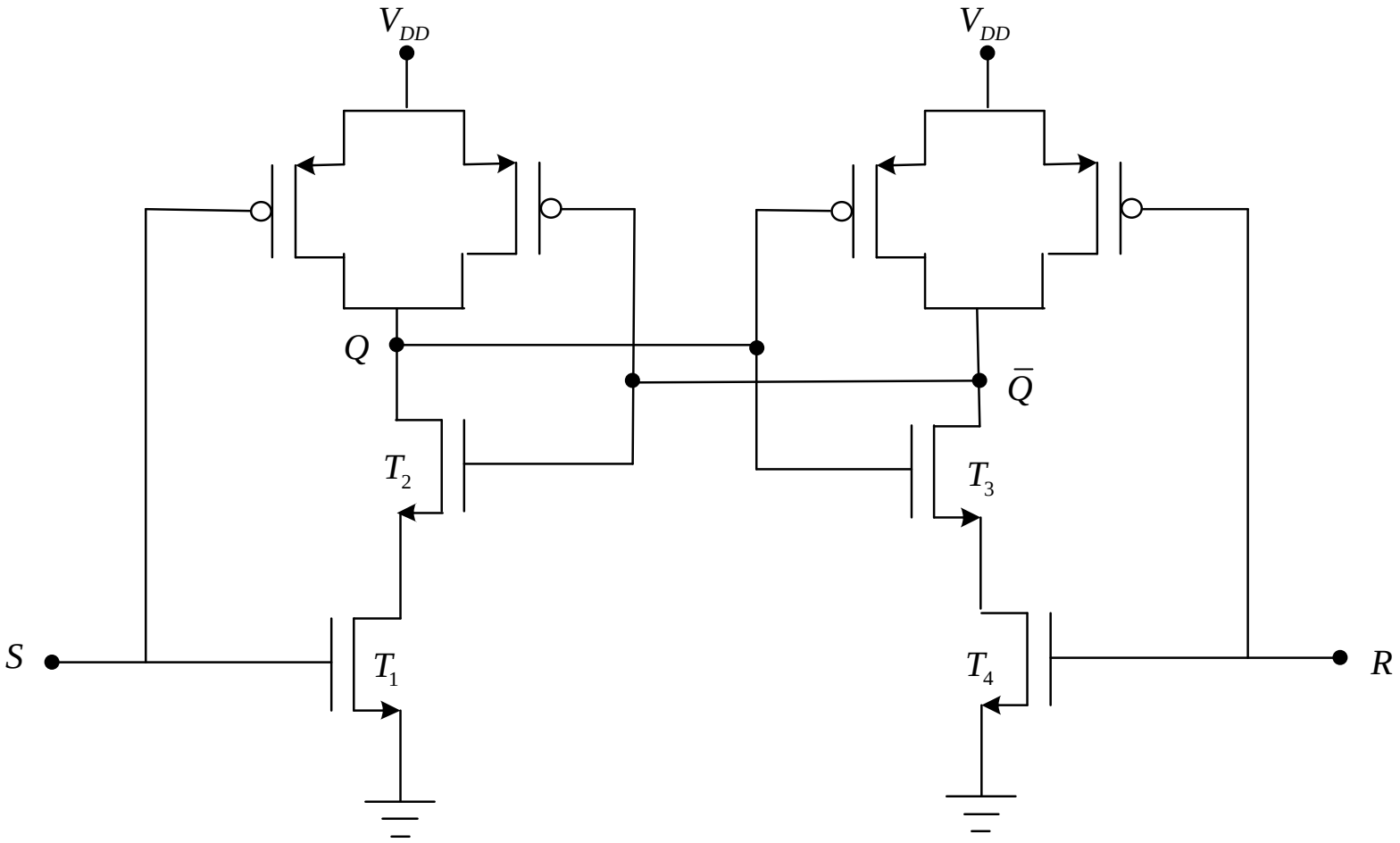


- Asynchronous Depletion-Load nMOS NOR Gate Based SR Latch:

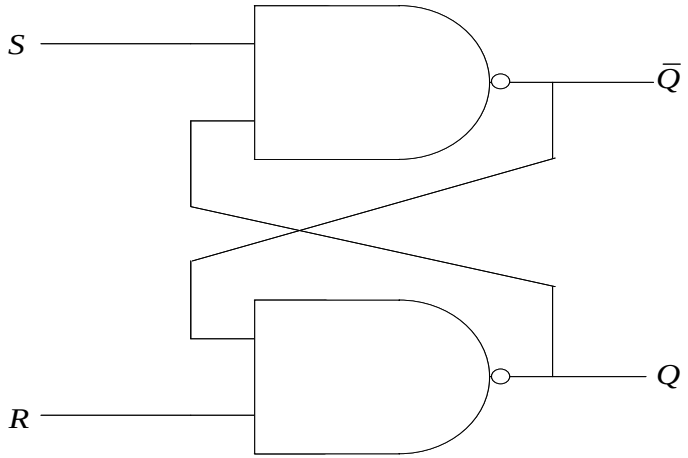


- Disadvantages: The power dissipation and noise margin

- Asynchronous CMOS NAND Gate Based SR Latch:

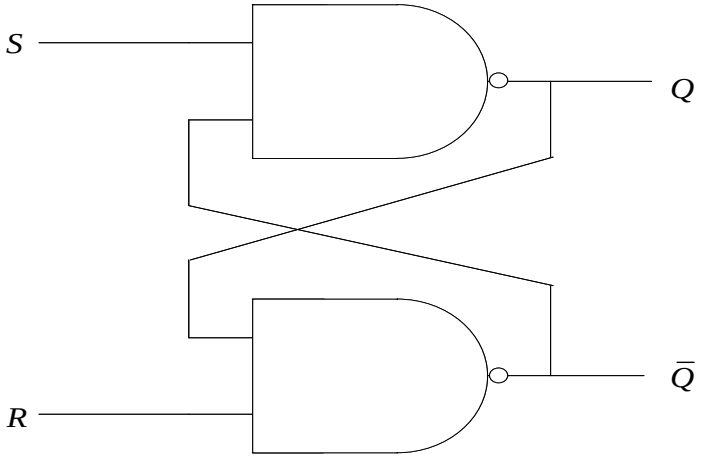


- Asynchronous SR Latch NAND Gate Based:



- SR latch NAND gate based operation
- Set high reset: high to hold
- Set: low reset: High Q : High $\overline{Q}$: low
- Reset : low set : high Q : low $\overline{Q}$: high

- Asynchronous SR Latch NAND Gate Based:



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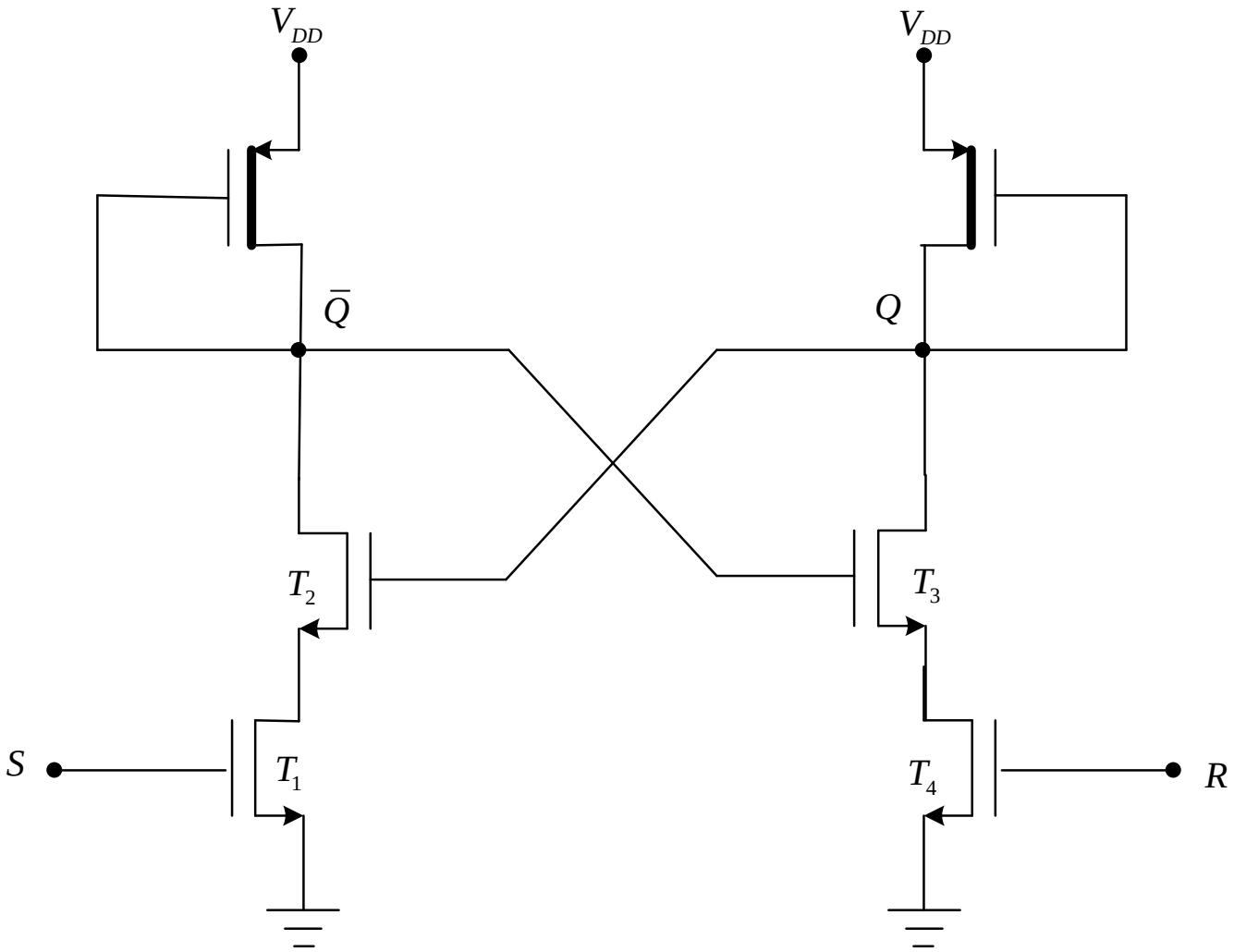
1	1	Q_{n-1}	$\bar{Q}_{n-1}$	Hold
1	0	1	0	Set
0	1	0	1	Reset
0	0	1	1	Forbidden State

- Asynchronous Depletion-Load nMOS NAND Gate Based SR Latch:



- To reset Q : high to Q : low
- Q is high
- A pulse applied to R
- To make the latch switch to low, Q node should come below the switching threshold of T_1 and T_2 .
- Positive feedback invert state
- Increase the size of T_5 ,T_6 , T_7 and T_8 .
- T_4, T_7 , T_8 form ratioed inverter.
- If $V_m = \frac{V_{DD}}{2}$

$$\text{and } \left(\frac{W}{L}\right)_{T1} = \left(\frac{W}{L}\right)_{T3} = \frac{0.5um}{0.25um} \quad \text{and } \left(\frac{W}{L}\right)_{T2} = \left(\frac{W}{L}\right)_{T4} = \frac{1.5um}{0.25um}, \quad Q: low$$

Design minimum size T_5 , T_6 , T_7 and T_8 to make the SR latch switchable

- Q: low to Q: high
- Pseudo-NMOS inverter ($T_5 - T_6$)- T_2 low level should be below the switching threshold of the inverter

$$T_3 - T_4 = \frac{V_{DD}}{2}$$

$$V_Q = 0 \text{ and } V_G(T_2) = 0 \text{ as long as } V_{\overline{Q}} > V_M$$

- Transistor sizing: equate current through inverter for $V_{\overline{Q}} = \frac{V_{DD}}{2}$
- The currents are determined by saturation.
- Since

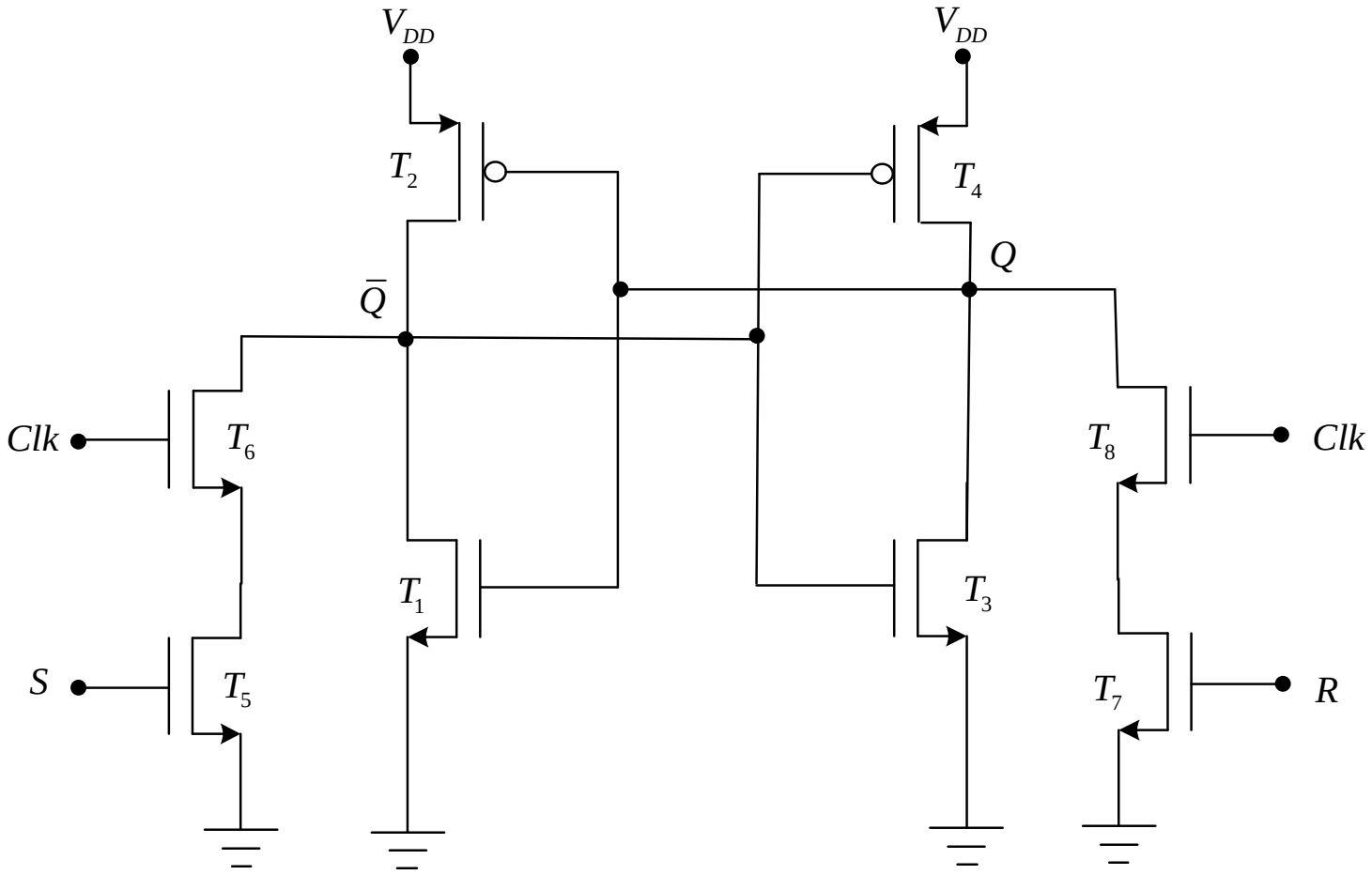
$\left(\frac{W}{L}\right)_{T5-T6}$ is the effective ratio of the series connected devices

$$L_{T5-T6} = 2L_{T5} = 2L_{T6}$$

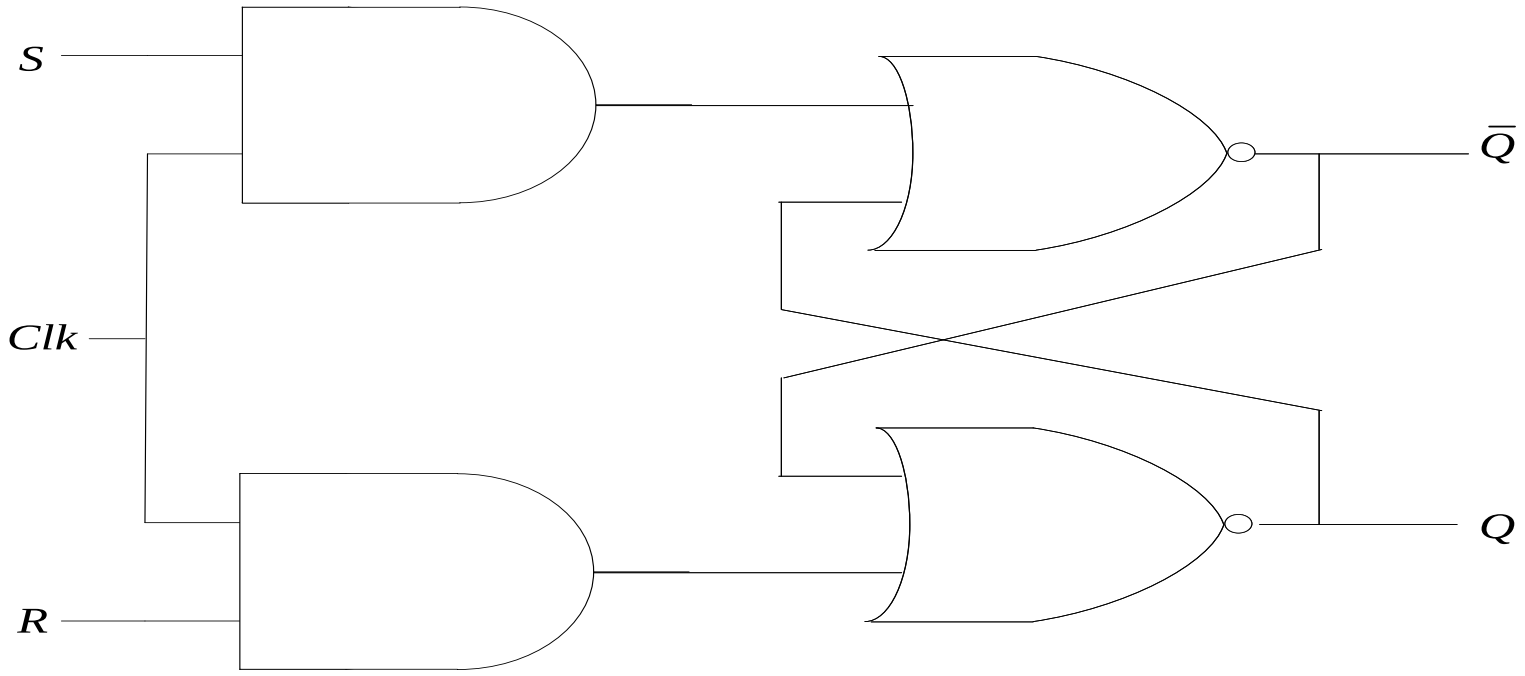
$$k_n'\left(\frac{W}{L}\right)_{T5-T6}\left[(V_{DD} - V_{Tn})V_{Dsatn} - \frac{V_{DSatn}^2}{2}\right] = k_p'\left(\frac{W}{L}\right)_{T2}\left[(-V_{DD} - V_{Tp})V_{Dsatp} - \frac{V_{DSatp}^2}{2}\right]$$

$$\left(\frac{W}{L}\right)_{T5-T6} \geq 2.26, \quad \left(\frac{W}{L}\right)_{T5} = \left(\frac{W}{L}\right)_{T6} = 4.5$$

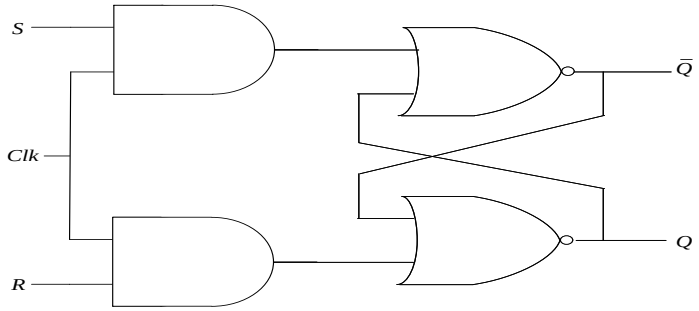
- Synchronous NOR Gate Based SR Latches:

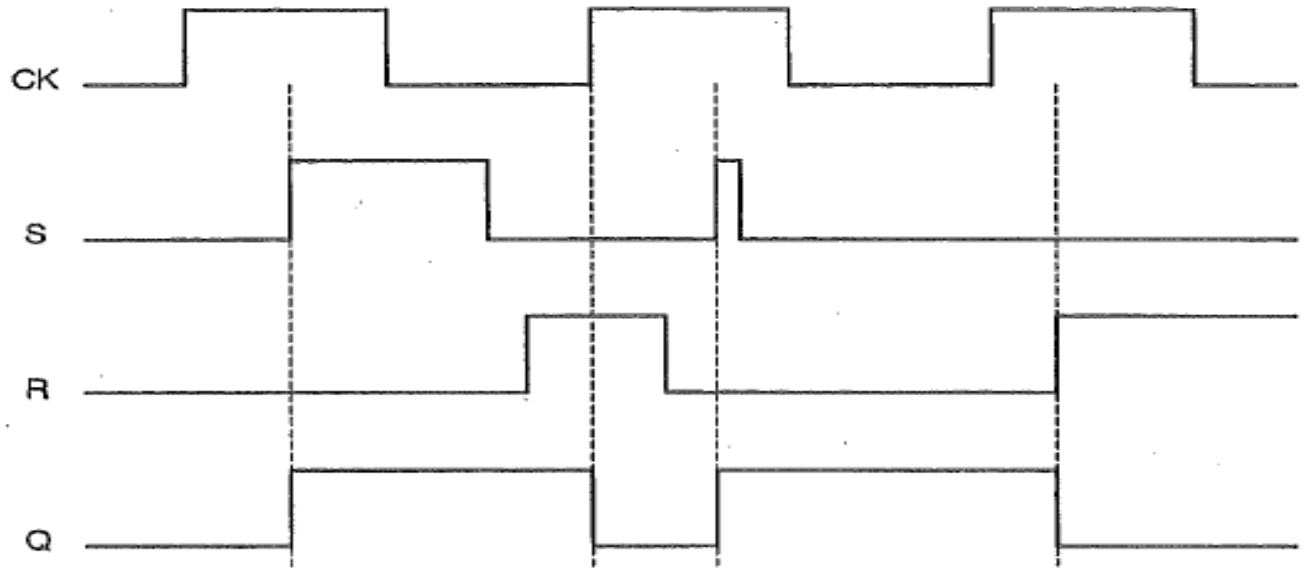


- Gate-Level Synchronous clocked NOR-Based SR Latches:

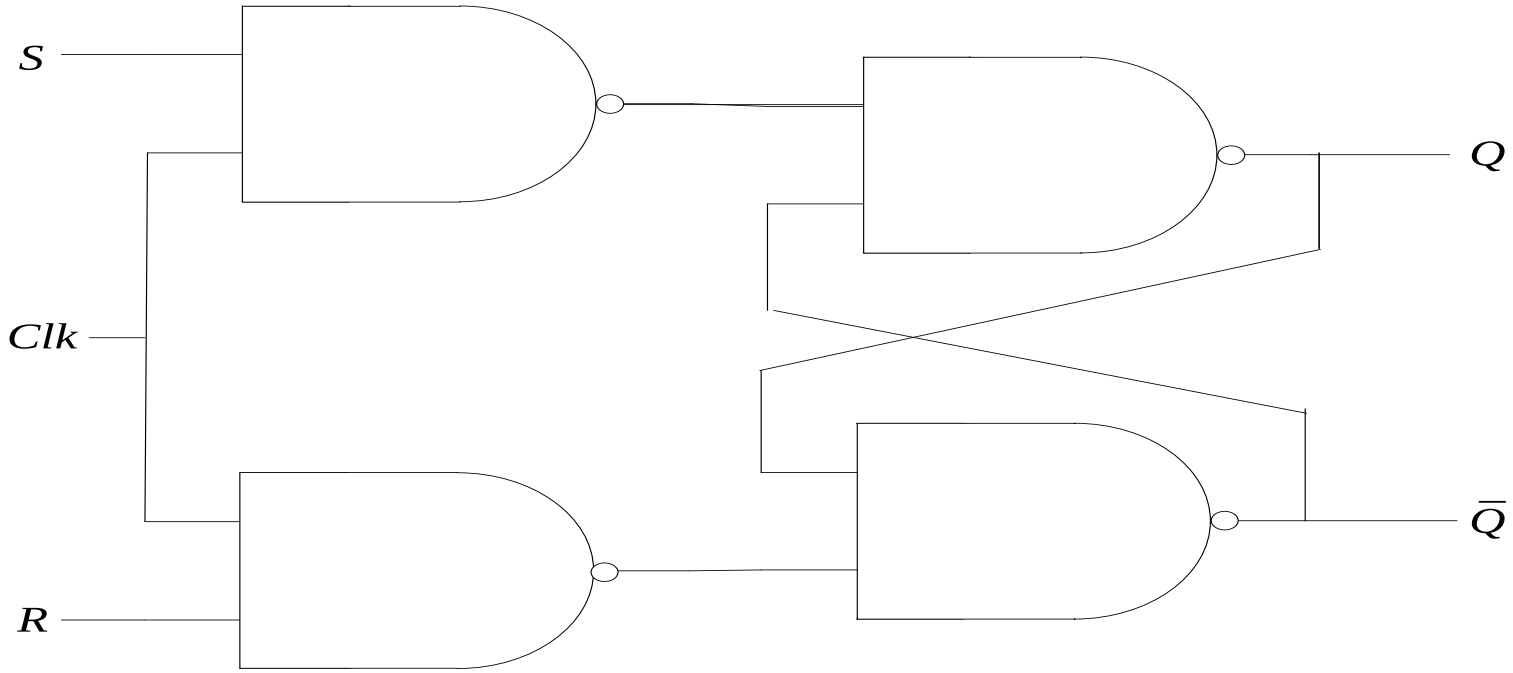


- Gate-Level Synchronous clocked NOR-Based SR Latches:

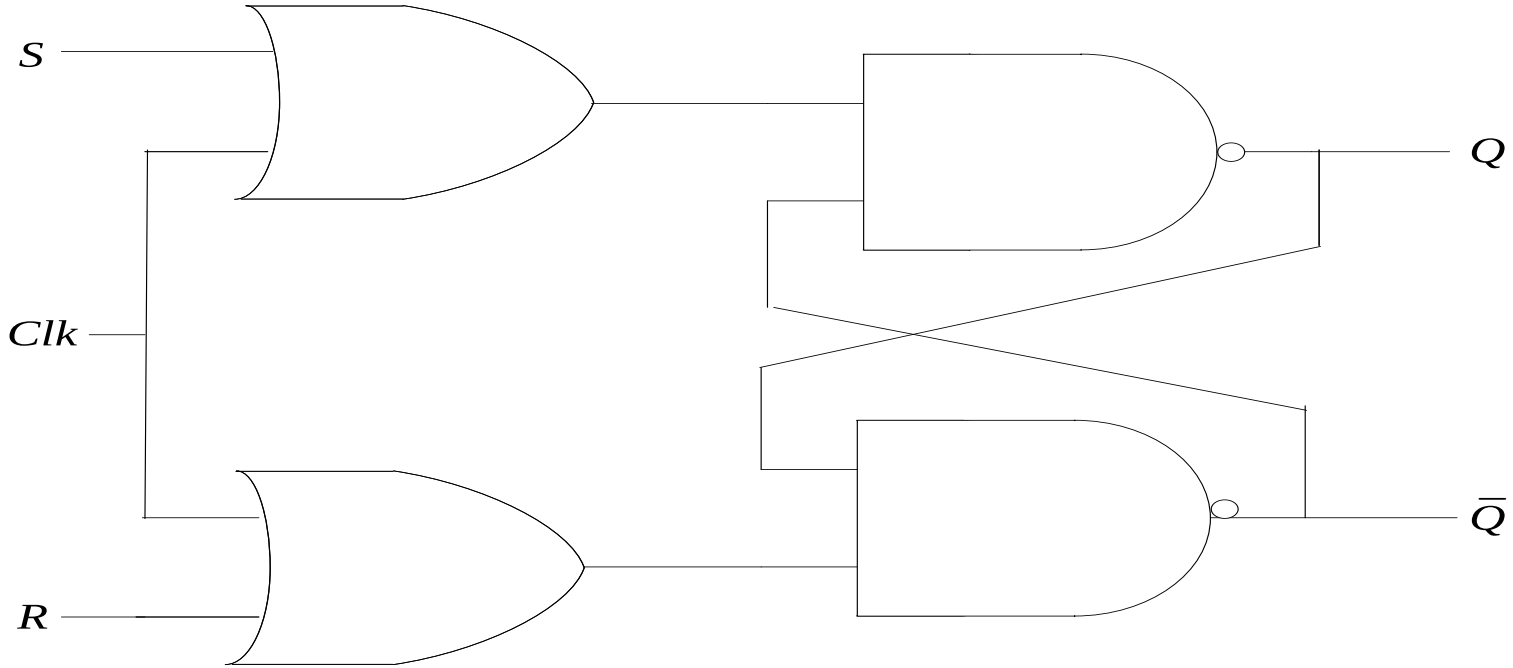




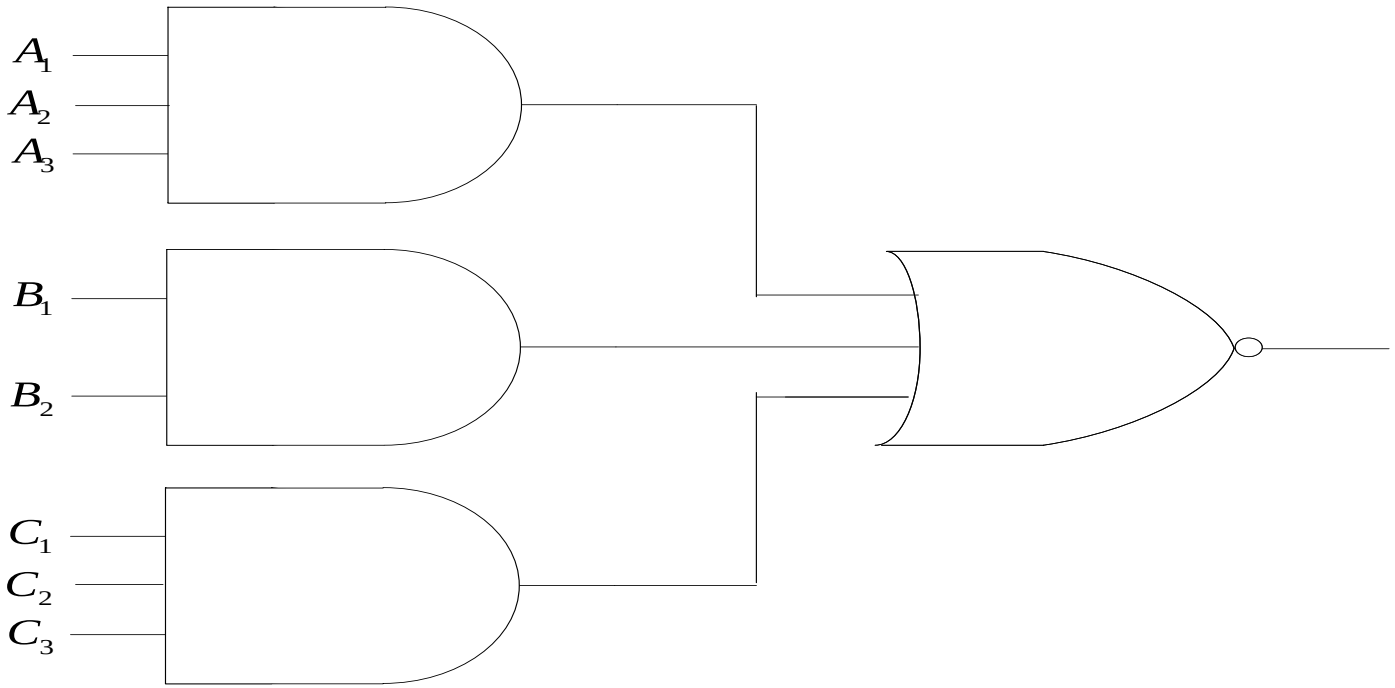
- Gate-Level Synchronous clocked NAND-Based SR Latch,
- with Active High Input :



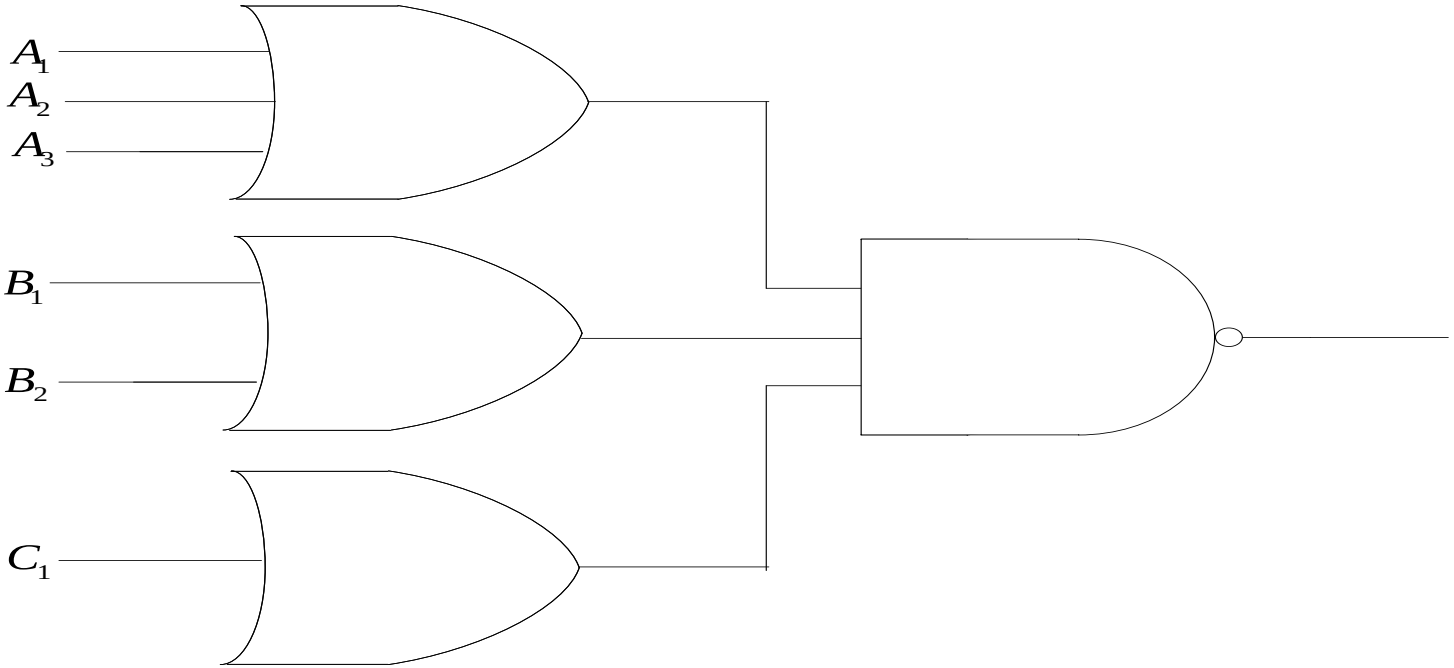
- Gate-Level Synchronous clocked NAND-Based SR Latch,
- with Active Low Input :



- AND-OR-INVERT (AOI) Gates:
- Pull-down Logic



- OR-AND-INVERT (OAI) Gates:
- Pull-down Logic



- AOI-based Clocked NOR Gate Based SR Latch: