EE141-Spring 2010 Digital Integrated Circuits

Lecture 17
Domino Logic
Registers

Administrativia

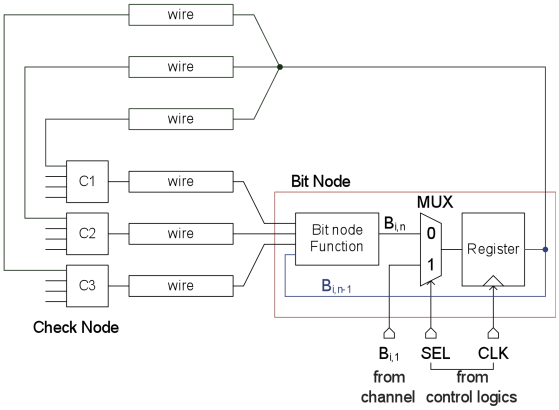
- Phase 2 announced. Launched in the next 24 hours.
- Hw 6 due on Fr.

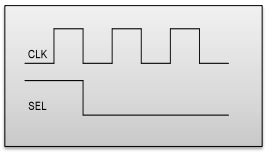
Class Material

- Last lecture
  - Ratioed Logic
  - Dynamic Logic
- Today's lecture
  - Domino Logic
  - Registers
- Reading (Ch 6, Ch 7)

Dynamic Logic

Phase 2 – Design the Bit Node



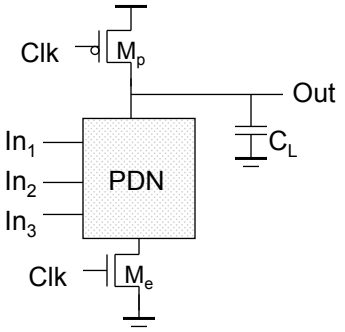


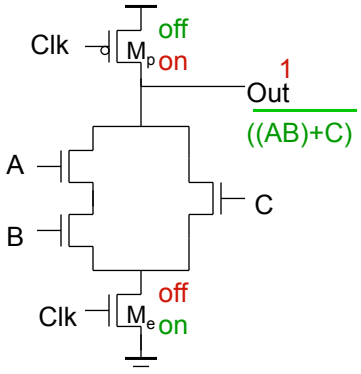
Goals: - Design bit-node so that clock frequency is minimized
- Layout bit and check nodes

Due Date: Wednesday April 13

Dynamic Logic

Dynamic Gate





Two phase operation

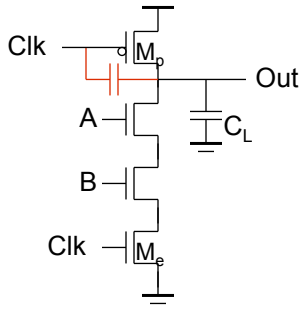
Precharge (Clk = 0)

Evaluate (Clk = 1)

Challenges of Dynamic Gates

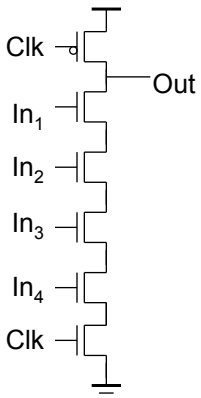
- Noise sensitivity and small noise margins
- Leakage
- Charge sharing
- Clock feedthrough

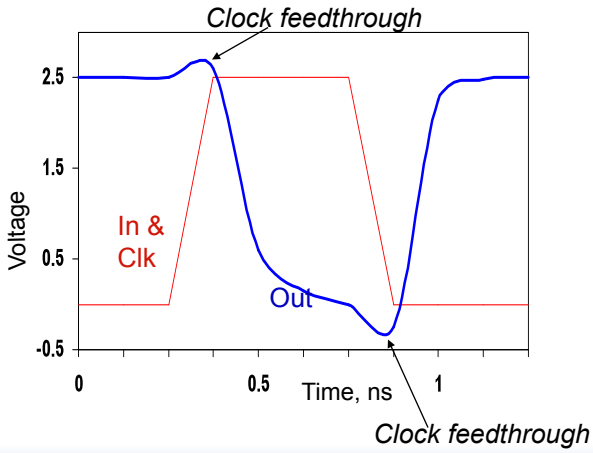
Issues in Dynamic Design 3: Clock Feedthrough



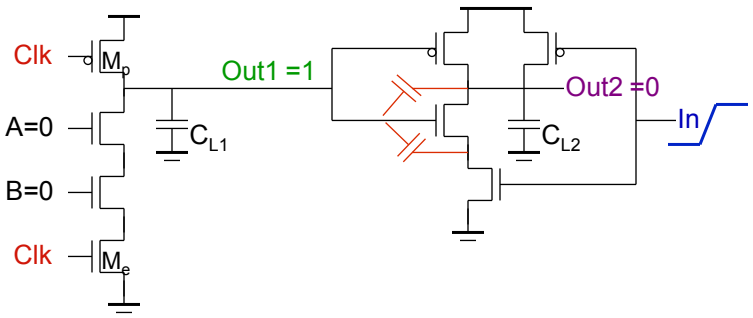
Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

Clock Feedthrough



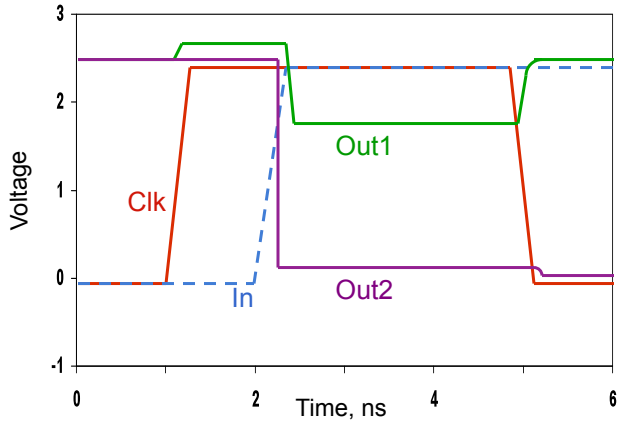


Issues in Dynamic Design 4: Backgate Coupling



Dynamic NAND Static NAND

Backgate Coupling Effect

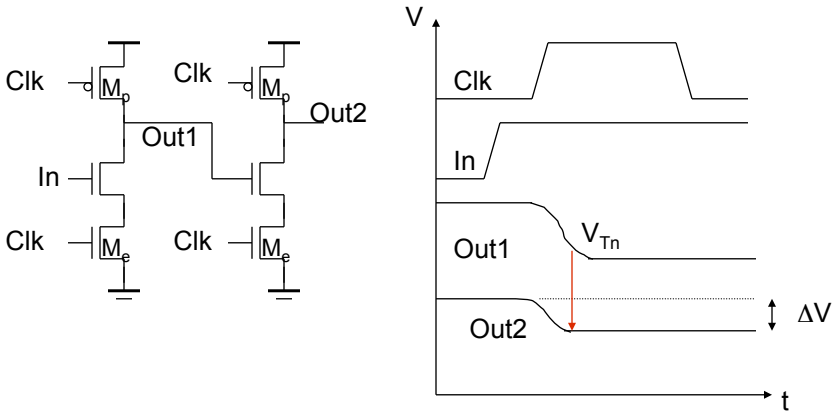


Other Effects

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)

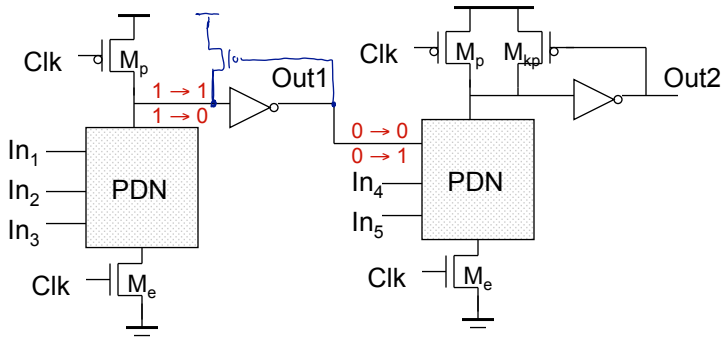
Domino Logic

Cascading Dynamic Gates

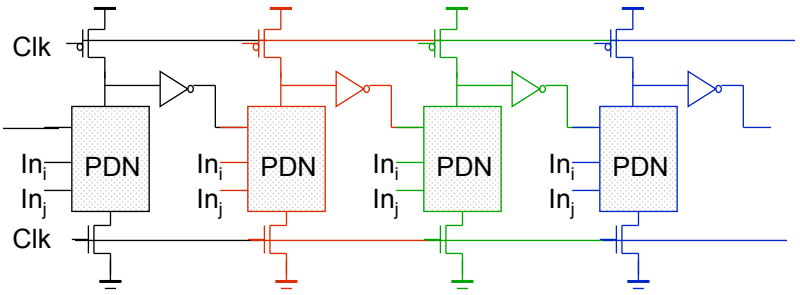


Only 0 → 1 transitions allowed at inputs!

Domino Logic



Why Named Domino?

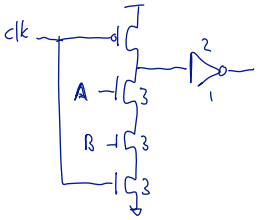


Like falling dominos!

Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

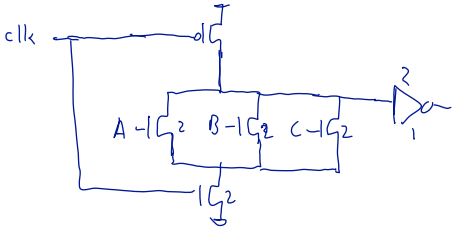
Domino Logic LE



$LE_{dyn} =$

$LE_{inv} = 1$

$\pi LE =$



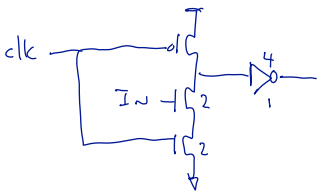
$LE_{dyn} =$

$LE_{inv} = 1$

$\pi LE =$

$LE_{static} = \frac{7}{3}$

Domino Logic LE (skewed static gate)

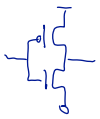


$LE_{dyn} =$

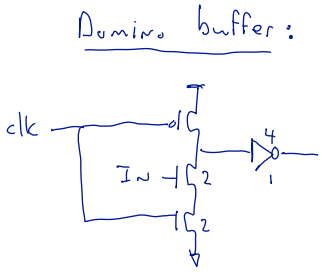
$LE_{inv} =$

$\pi LE =$

reference inverter:



Buffer "Average" LE



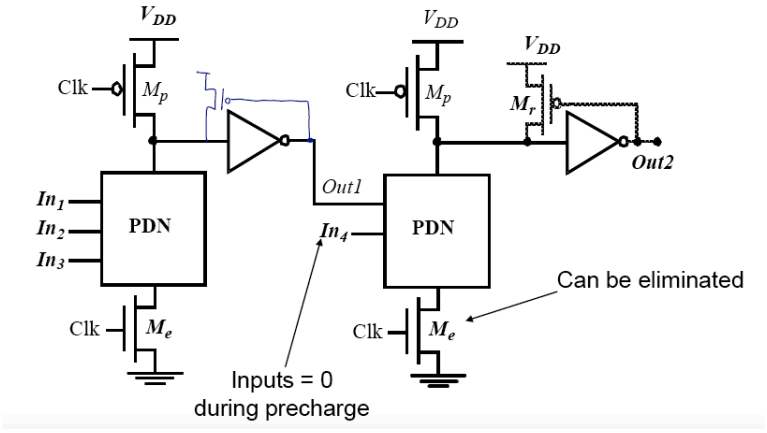
$LE_{dinv} = \frac{2}{3}$

$LE_{sinv} = \frac{5}{6}$

$\Pi LE = \frac{10}{18}$

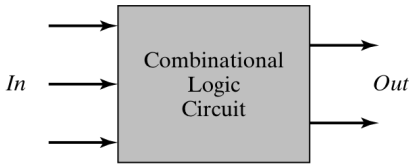
"Average" $LE = \sqrt{10/18} \approx \frac{3}{4}$

Designing with Domino Logic



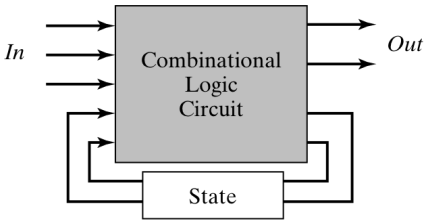
Sequential Logic

Combinational vs. Sequential Logic



(a) Combinational

Output = *f*(*In*)



(b) Sequential

Output = *f*(*In, Previous In*)

Why Sequencing?

Two key (related) reasons that we need sequencing:

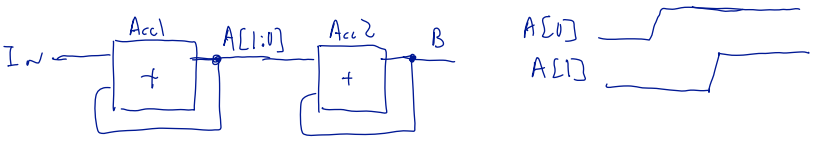
(1) Want to know when an input has a "new" value

Why Sequential Logic?

Two key (related) reasons that we need sequencing:

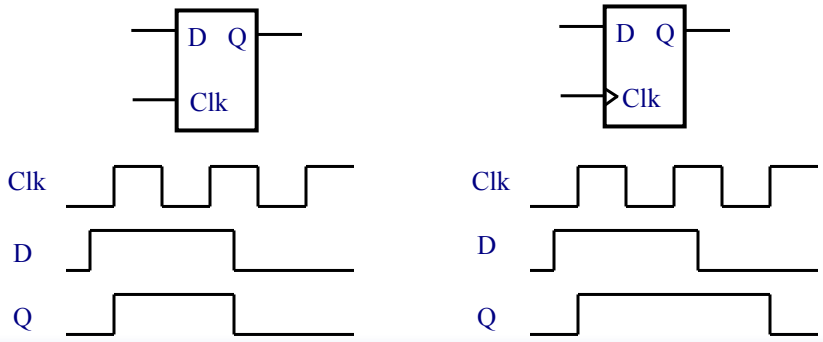
(2) Need to slow down signals that are too fast

- In order to keep them aligned with slower ones

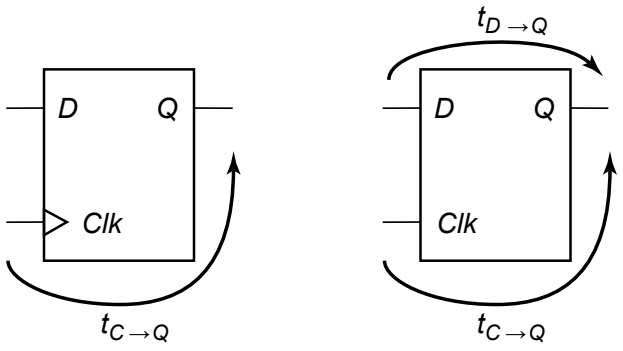


Latch versus Register (Flip-flop)

- Latch: level-sensitive
  clock is low - hold mode
  clock is high - transparent
- Register: edge-triggered
  stores data when
  clock rises

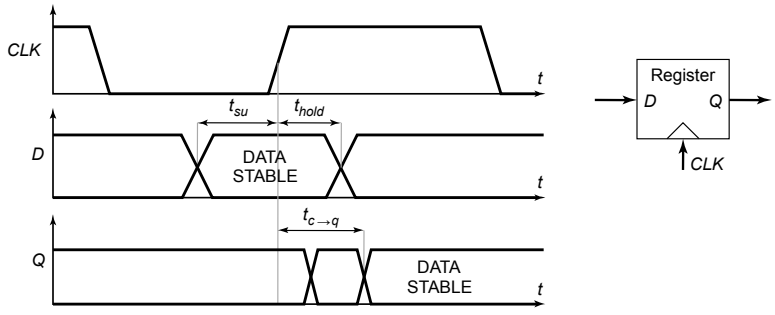


Characterizing Timing



Register Latch

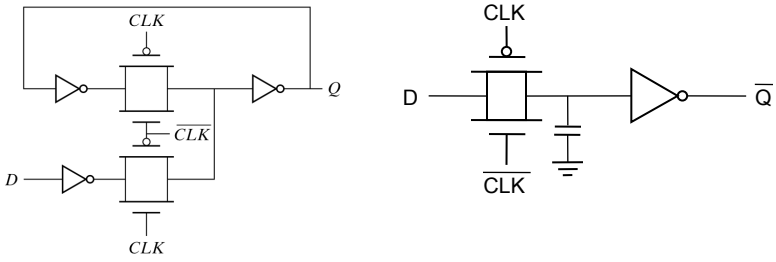
Timing Definitions - REVIEW



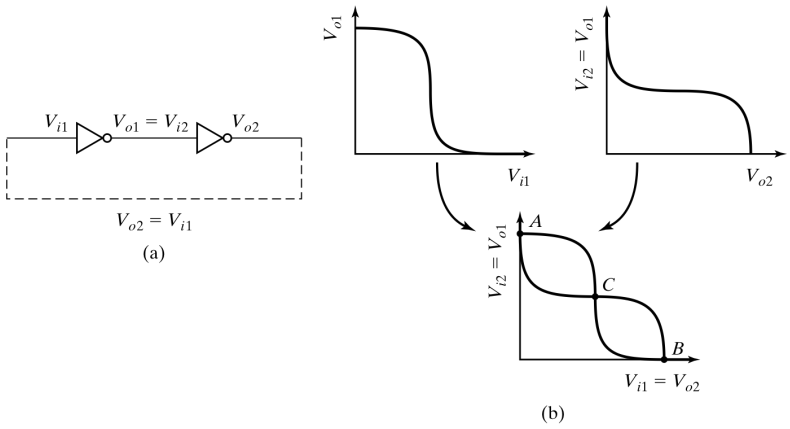
Storage Mechanisms

Static

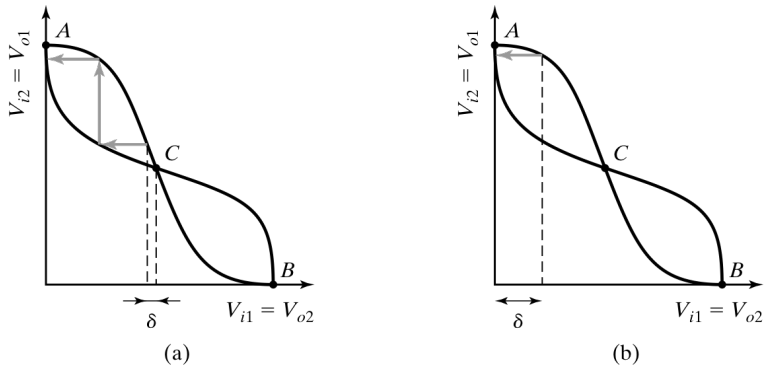
Dynamic



Positive Feedback: Bi-Stability



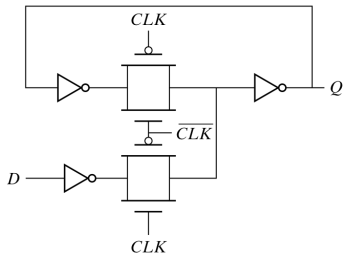
Meta-Stability



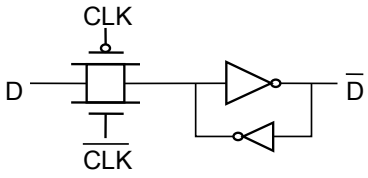
Gain should be larger than 1 in the transition region

Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

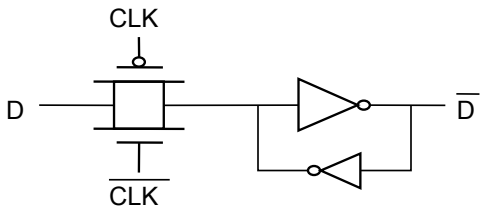


Converting into a MUX



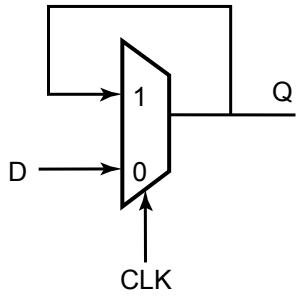
Forcing the state
(can implement as NMOS-only)

Pseudo-Static Latch



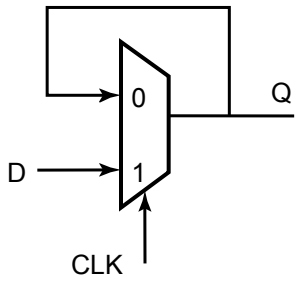
Mux-Based Latches

Negative latch
(transparent when CLK= 0)



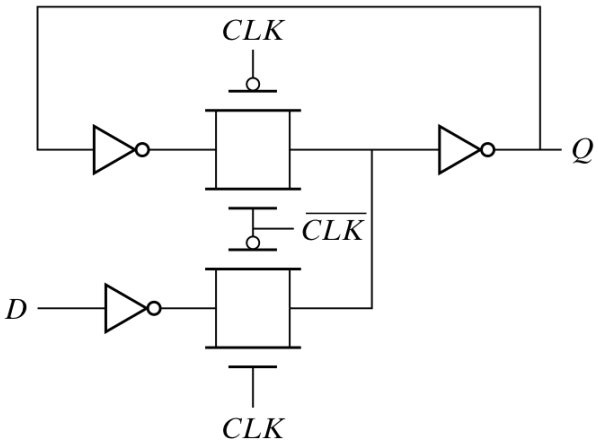
$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

Positive latch
(transparent when CLK= 1)

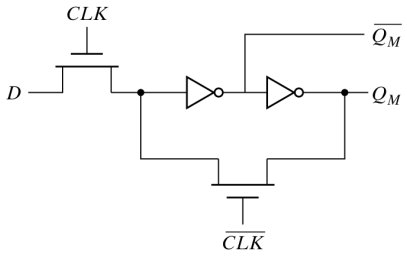


$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

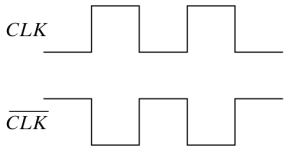
Mux-Based Latch



Mux-Based Latch



(a) Schematic diagram



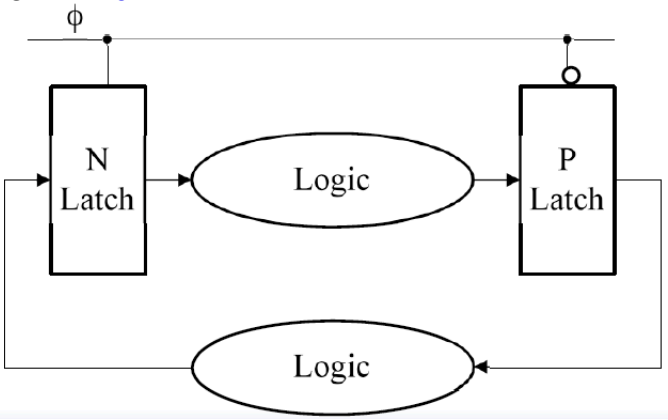
(b) Non overlapping clocks

NMOS only

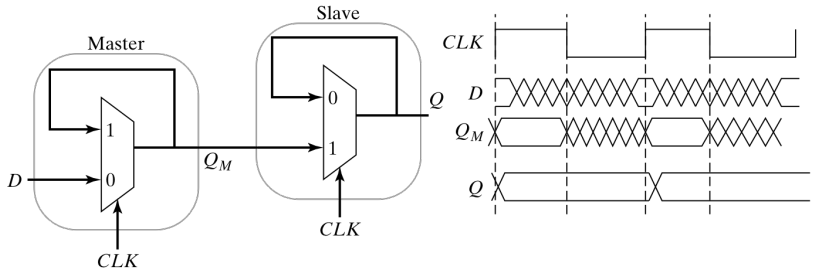
Non-overlapping clocks

Latch-Based Design

- N latch is transparent when $\Phi = 0$
- P latch is transparent when $\Phi = 1$



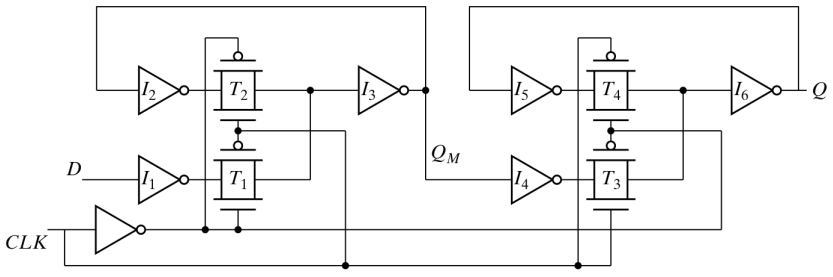
Master-Slave (Edge-Triggered) Register



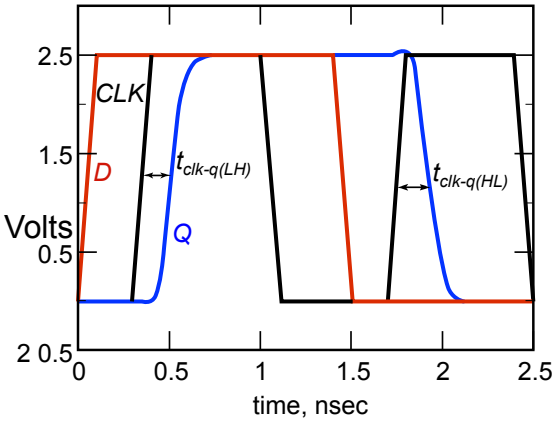
Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

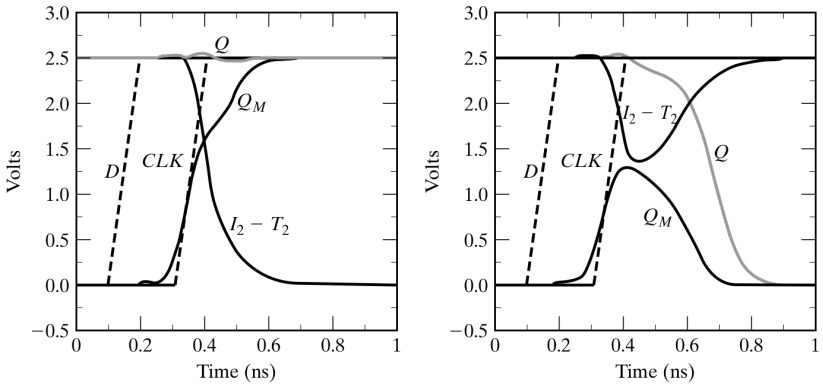
Multiplexer-based latch pair



Clk-Q Delay

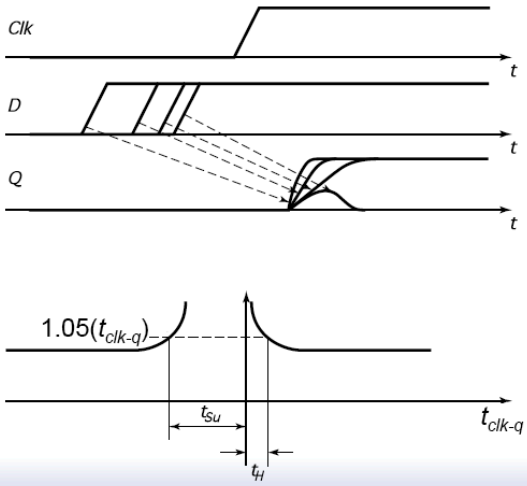


Setup Time



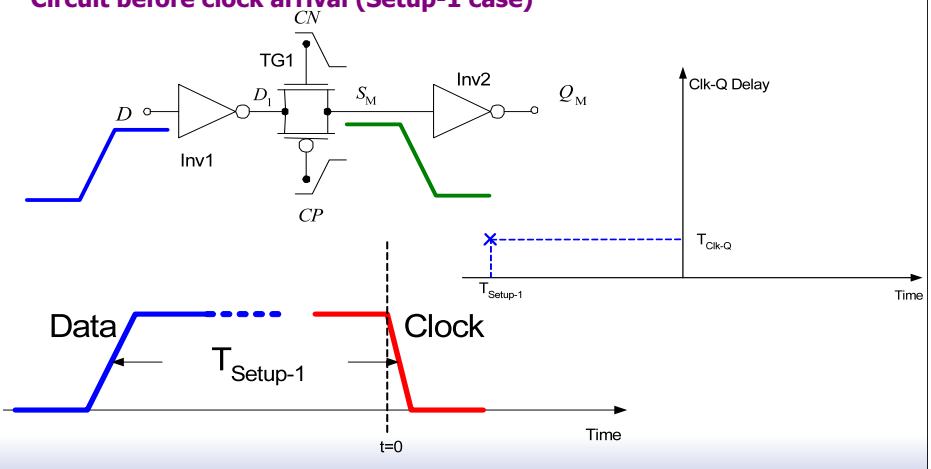
(a) T_{setup} = 0.21 ns (b) T_{setup} = 0.20 ns

More Precise Setup Time



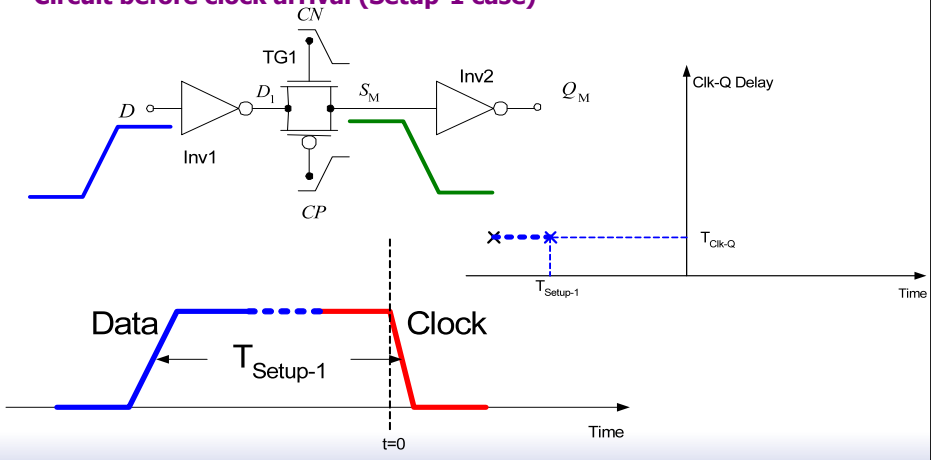
Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)



Setup-Hold Time Illustrations

Circuit before clock arrival (Setup-1 case)