EE141-Spring 2010 Digital Integrated Circuits

Lecture 7
Wires

Administrativia

- No lab next week
- Midterm on Fr Febr 19 6:30-8pm in 2060 Valley LSB
- Review Session: TBA (most likely on Th)

Class Material

- Last lecture
  - Optimizing complex logic
- Today's lecture
  - Applying what we learned on memory decoders
- Reading (Ch 6.2, 12.1,12.3)

Logical Effort

$$t_{pgate} = t_{inv}\,(p\gamma + LE \times f)$$

Measure everything in units of t_{inv} (divide by t_{inv}):

p – intrinsic delay ($k\gamma_g$) - gate parameter ≠ f(W)
LE – logical effort (k) – gate parameter ≠ f(W)
f – electrical effort (effective fanout)

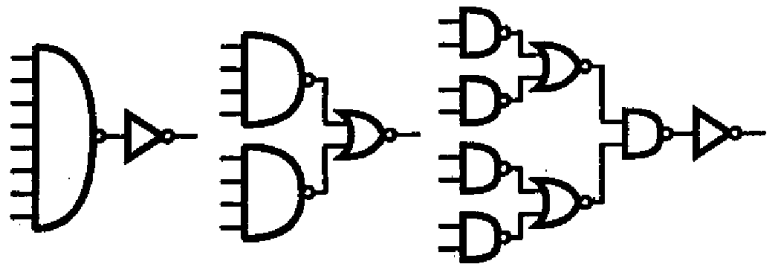
Normalize everything to an inverter:
LE_{inv} =1, p_{inv} = γ

Method of Logical Effort

- Compute the path effort: PE = (ΠLE)*BF*
- Find the best number of stages $N \sim \log_4 PE$
- Compute the effective fanout/stage $EF = PE^{1/N}$
- Sketch the path with this number of stages
- Work either from either end, find sizes: $C_{in} = C_{out}$*LE/EF

Reference: Sutherland, Sproull, Harris, "Logical Effort, Morgan-Kaufmann 1999.

Example – 8-Input AND

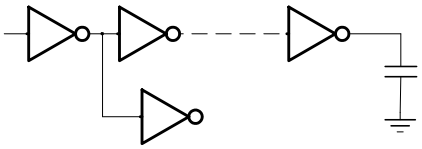


LE=10/3 1	*LE*=2 5/3	*LE*=4/3 5/3 4/3 1
ΠLE = 10/3	ΠLE = 10/3	ΠLE = 80/27
P = 8 + 1	P = 4 + 2	P = 2 + 2 + 2 + 1

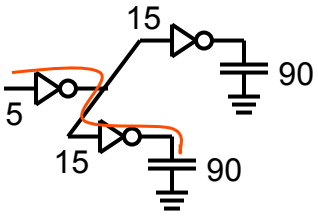
Add Branching Effort

Branching effort:

$$b = \frac{C_{on-path} + C_{off-path}}{C_{on-path}}$$



Branching Example 1



LE	=	1
FO	=	90/5 = 18
PE	=	18 (wrong!)
SE_1	=	(15+15)/5 = 6
SE_2	=	90/15 = 6
PE	=	36, not 18!

Introduce new kind of effort to account for branching:

- Branching Effort: $b = \frac{C_{on\text{-}path} + C_{off\text{-}path}}{C_{on\text{-}path}}$
- Path Branching Effort: $B = \prod b_i$

Now we can compute the path effort:

- Path Effort: $PE = \prod LE \cdot FO \cdot B$

Branching Example 2

Select gate sizes *y* and *z* to minimize delay from *A* to *B*

Logical Effort: $LE = (4/3)^3$

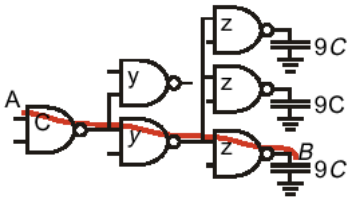
Electrical Effort: $FO = C_{out}/C_{in} = 9$

Branching Effort: $B = 2 \cdot 3 = 6$

Path Effort: $PE = \prod LE \cdot FO \cdot B = 128$

Best Stage Effort: $SE = PE^{1/3} \approx 5$

Delay: $D = 3 \cdot 5 + 3 \cdot 2 = 21$



Work backward for sizes:

$$z = \frac{9C \cdot (4/3)}{5} = 2.4C$$

$$y = \frac{3z \cdot (4/3)}{5} = 1.9C$$

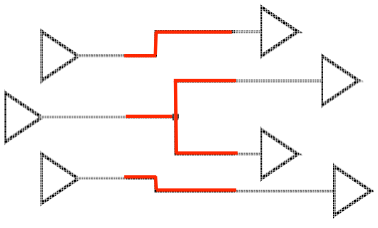
Method of Logical Effort

- Compute the path effort: PE = (ΠLE)*BF*
- Find the best number of stages $N \sim \log_4 PE$
- Compute the effective fanout/stage $EF = PE^{1/N}$
- Sketch the path with this number of stages
- Work either from either end, find sizes: $C_{in} = C_{out} * LE/EF$

Reference: Sutherland, Sproull, Harris, "Logical Effort, Morgan-Kaufmann 1999.

Wires

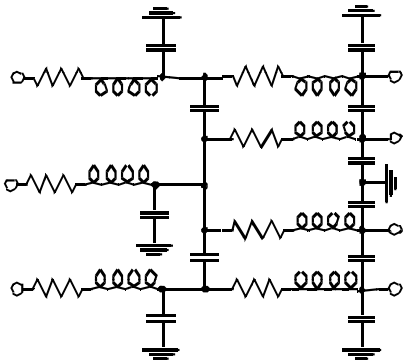
The Wire



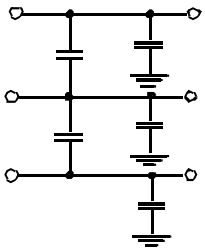
Schematic

Physical

Wire Models



All-inclusive model

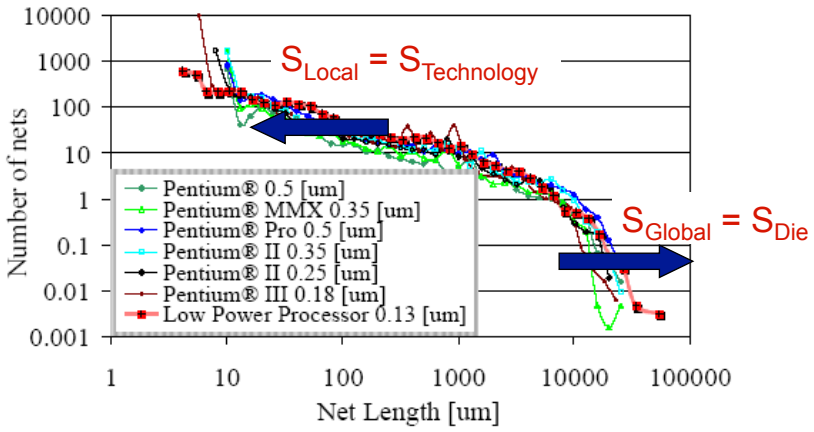


Capacitance-only

Impact of Interconnect Parasitics

- Interconnect and its parasitics can affect all of the metrics we care about
  - Cost, reliability, performance, power consumption
- Parasitics associated with interconnect:
  - Capacitance
  - Resistance
  - Inductance

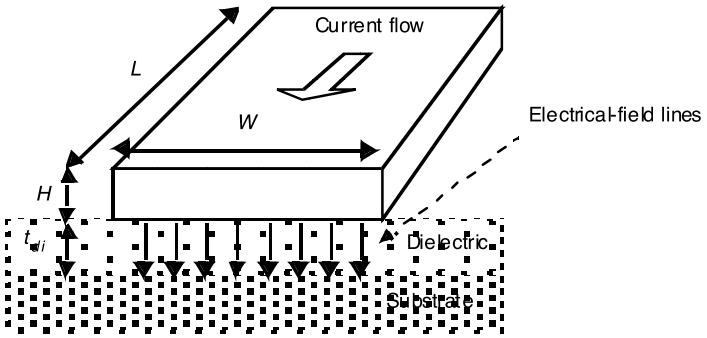
Interconnect Length Distribution



From Magen et al., "Interconnect Power Dissipation in a Microprocessor"

INTERCONNECT

Capacitance: The Parallel Plate Model



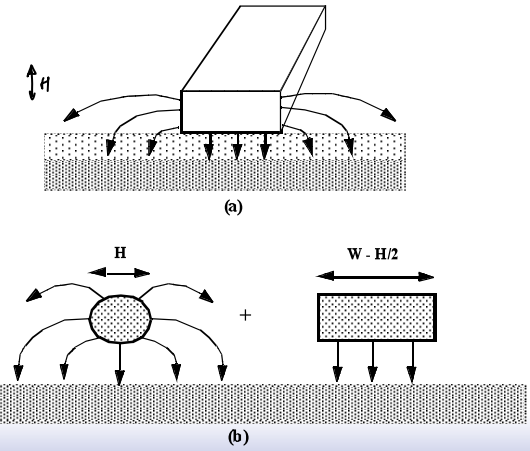
$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

Permittivity

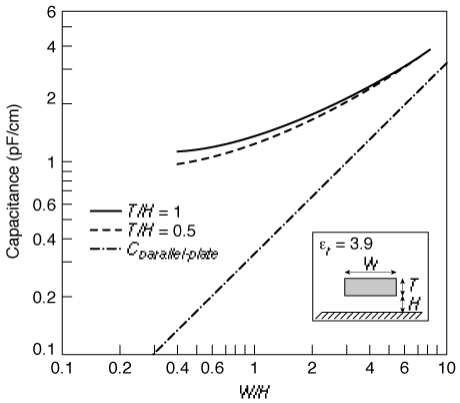
Material	ε_r
Free space	1
Aerogels	~1.5
Polyimides (organic)	3-4
Silicon dioxide	3.9
Glass-epoxy (PC board)	5
Silicon Nitride (Si_3N_4)	7.5
Alumina (package)	9.5
Silicon	11.7

Fringing Capacitance

$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

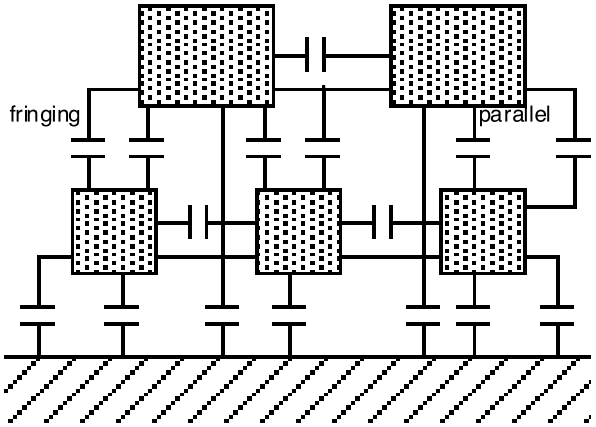


Fringing versus Parallel Plate



(from [Bakoglu89])

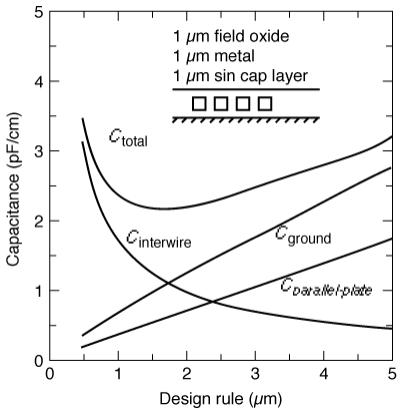
Interwire Capacitance



Capacitive coupling and noise

Coupling Capacitance and Delay

Impact of Interwire Capacitance



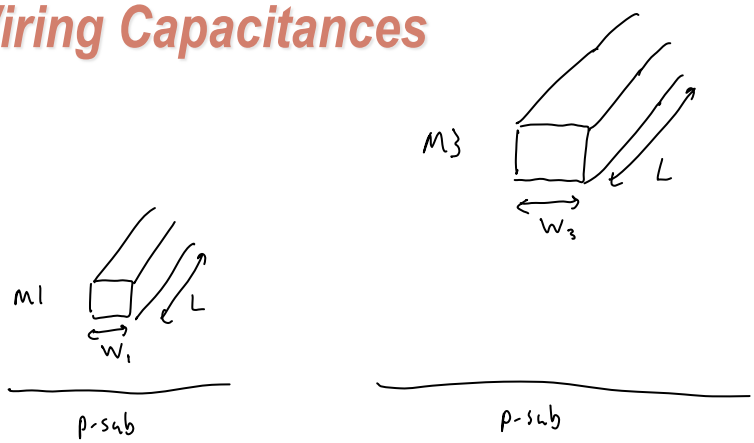
(from [Bakoglu89])

Wiring Capacitances (0.25 μm CMOS)

Bottom plate

Top plate	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88	aF/μm²					
	54	aF/μm					
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

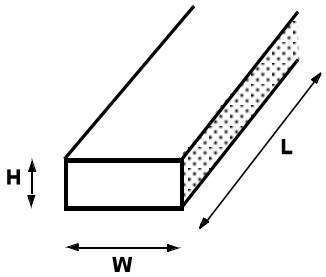
Wiring Capacitances



$$C = C_{pp} \cdot W \cdot L + 2C_{fringe} L$$

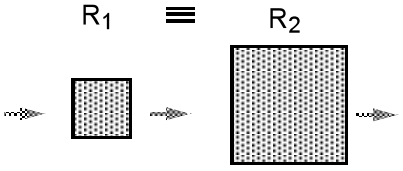
INTERCONNECT

Wire Resistance



$$R = \rho \frac{L}{HW}$$

Sheet Resistance
R_o



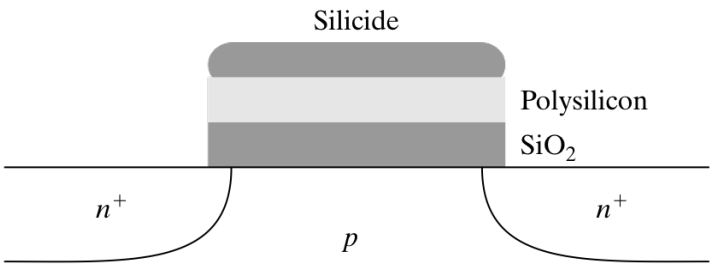
Interconnect Resistance

Material	ρ (Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Dealing with Resistance

- **Use Better Interconnect Materials**
  - e.g. copper, silicides
- **More Interconnect Layers**
  - reduce average wire-length
- **Selective Technology Scaling**
  - (More later)

Polycide Gate MOSFET

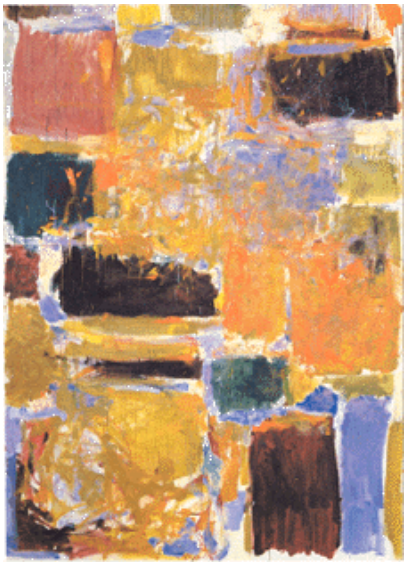


Silicides: WSi_2, $TiSi_2$, $PtSi_2$ and TaSi

Conductivity: 8-10 times better than Poly

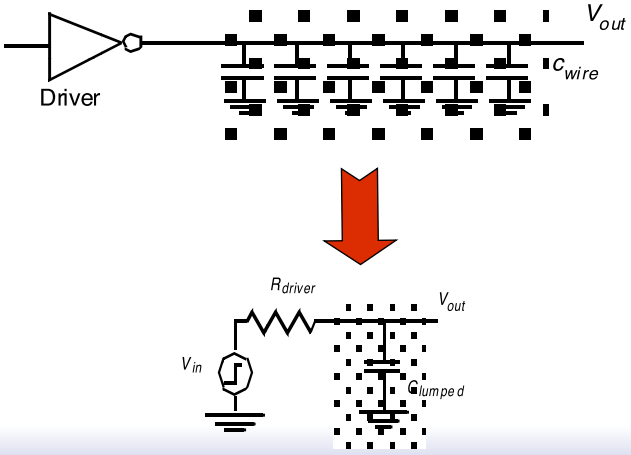
Sheet Resistance

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

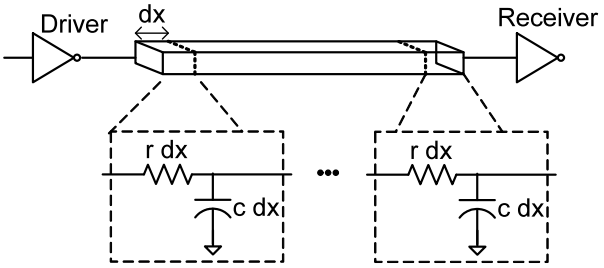


Interconnect Modeling

The Lumped Model

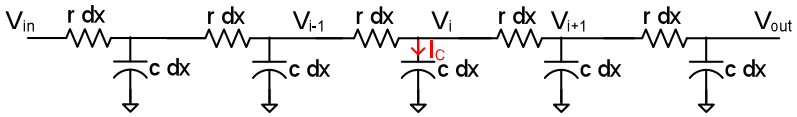


The Distributed RC-line



- Analysis method:
  - Break the wire up into segments of length dx
  - Each segment has resistance (r dx) and capacitance (c dx)

The Distributed RC-line



$$I_C = c\Delta L\frac{\partial V}{\partial t} = \frac{(V_{i-1}-V_i)-(V_i-V_{i+1})}{r\Delta L} \longrightarrow \boxed{rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}}$$

$$\boxed{\tau = \frac{L^2}{2}rc}$$

Wire Model

Model the wire with N equal-length segments:

$$\tau_{DN} = \left(\frac{L}{N}\right)^2 (rc + 2rc + \ldots + Nrc) = (rcL^2)\frac{N(N+1)}{2N^2} = RC\frac{N+1}{2N}$$

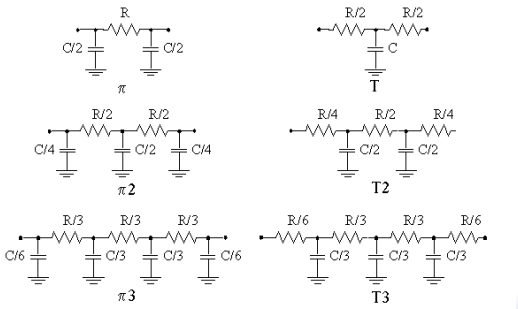
For large values of N:

$$\tau_{DN} = \frac{RC}{2} = \frac{rcL^2}{2}$$

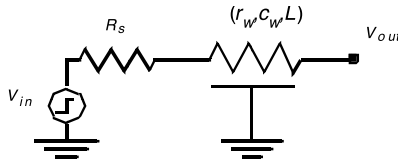
RC-Models

Voltage Range	Lumped RC-network	Distributed RC-network
0→50% (t_p)	0.69 RC	0.38 RC
0→63% (τ)	RC	0.5 RC
10%→90% (t_r)	2.2 RC	0.9 RC

Step Response of Lumped and Distributed RC Networks: Points of Interest.



Driving an RC-line



$$\tau_D = R_s C_w + \frac{R_w C_w}{2} = R_s C_w + 0.5 r_w c_w L^2$$

$$t_p = 0.69 R_s C_w + 0.38 R_w C_w$$