EE141-Spring 2010 Digital Integrated Circuits

Lecture 15
Pass-Transistor Logic
Layout of Complex Logic

Administrativia

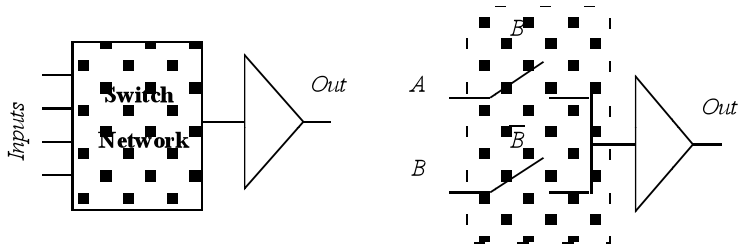
- Hw 6 posted.
- Project phase 1 underway. Mail your group composition (list of names) to ee141@cory.eecs.berkeley.edu
- No lecture on Fr
  - Make-up on Tu March 16 at 3:30pm

Class Material

- Last lecture
  - Optimizing complex logic
  - Pass transistor logic
- Today's lecture
  - Pass transistor logic – continued
  - CMOS Layout
  - Pseudo-NMOS
- Reading (Ch 6)

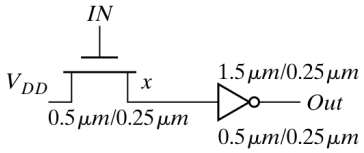
Pass-Transistor Logic

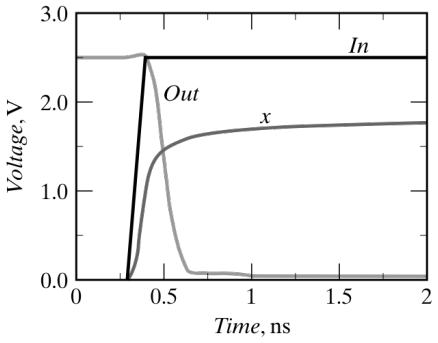
Pass-Transistor Logic



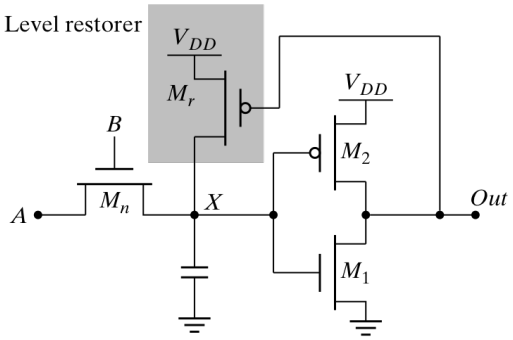
- N transistors
- No static consumption

NMOS-Only Logic



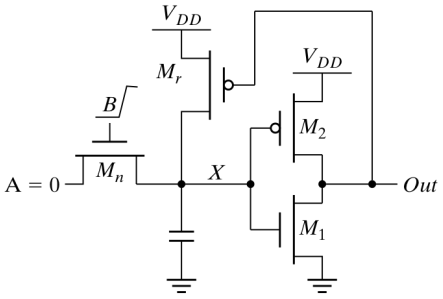


NMOS Only Logic: Level Restoring Transistor



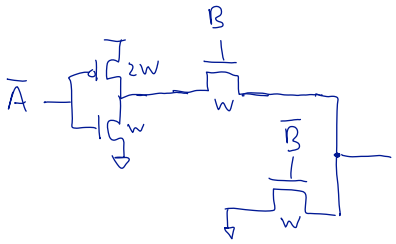
- Advantage: Full Swing
- Restorer adds capacitance, takes away pull down current at X
- Ratio problem

Restorer Sizing



- Upper limit on restorer size
- Pass-transistor pull-down can have several transistors in stack

Pass Transistor Logic LE

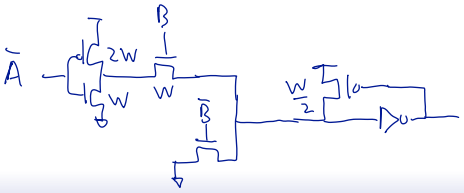


$C_{gate\,B}$ =

$R_{gate\,B}$ =

LE_B =

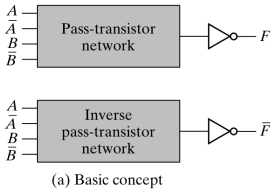
With level restore:



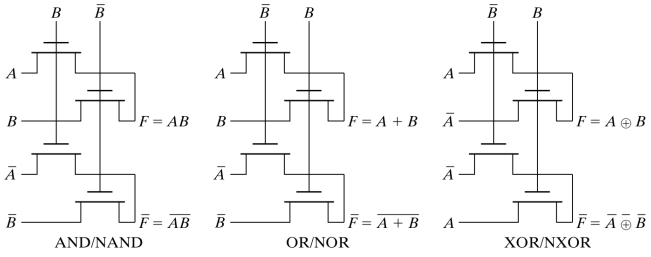
$R_{gate\,B}$ =

LE_B =

Complementary Pass Transistor Logic

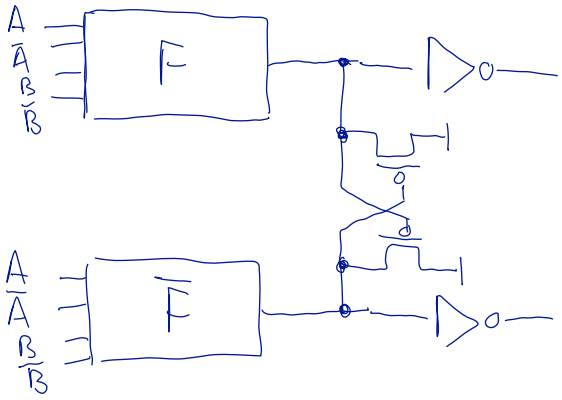


(a) Basic concept



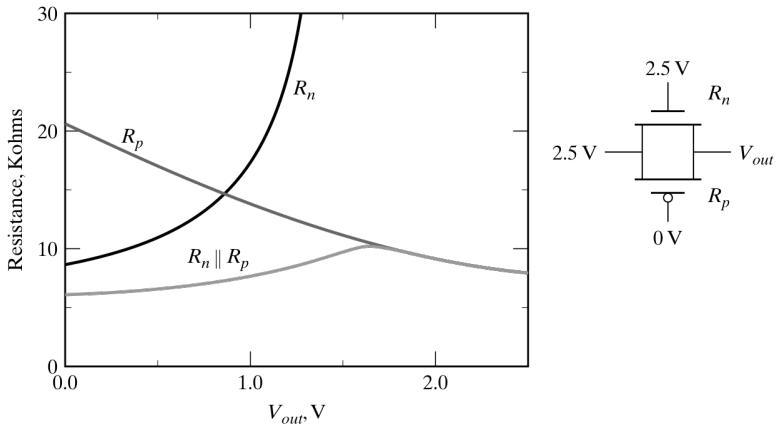
(b) Example pass-transistor networks

CPL Level Restore

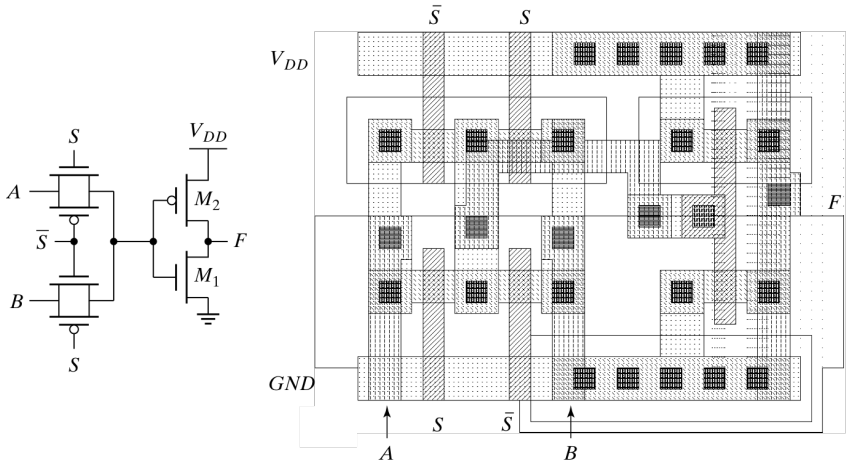


Solution 2: Transmission Gate

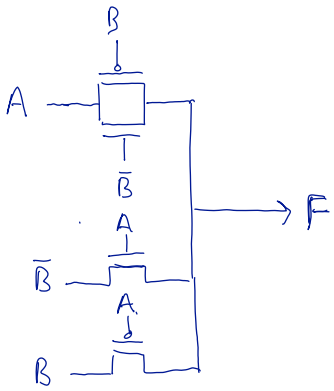
Resistance of Transmission Gate



Pass-Transistor Based Multiplexer

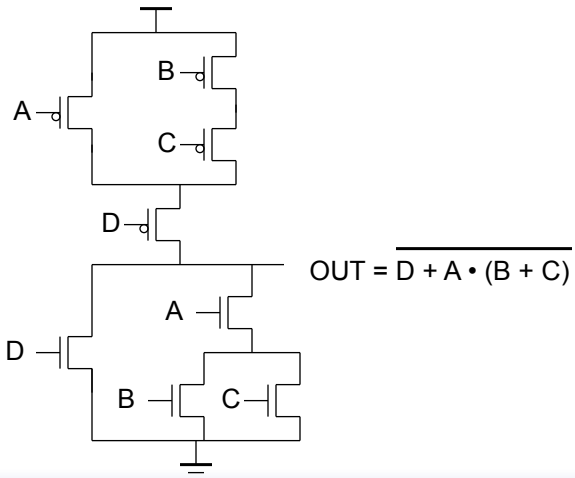


Transmission Gate XOR



CMOS Layout

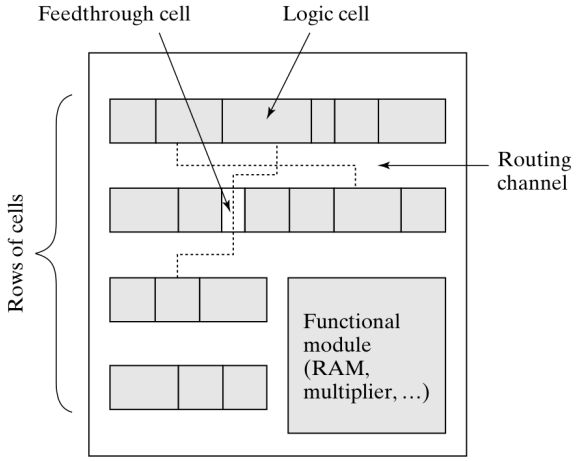
Complex CMOS Gate



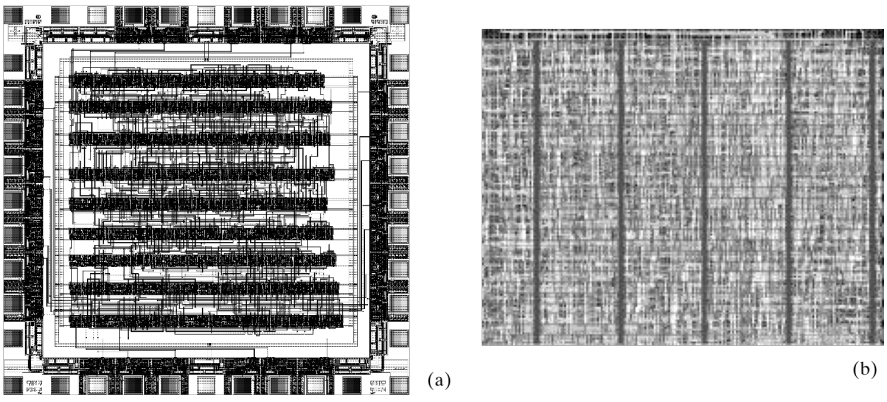
Cell Design

- Standard Cells
  - General purpose logic
  - Used to synthesize RTL/HDL
  - Same height, varying width
- Datapath Cells
  - For regular, structured designs (arithmetic)
  - Includes some wiring in the cell

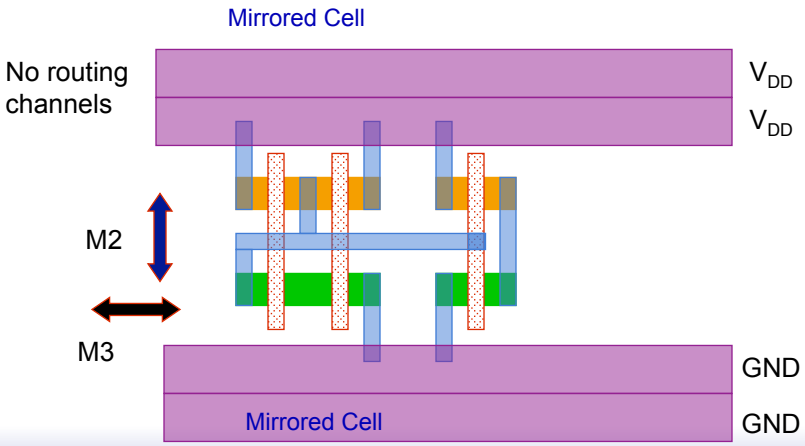
Standard Cell Methodology



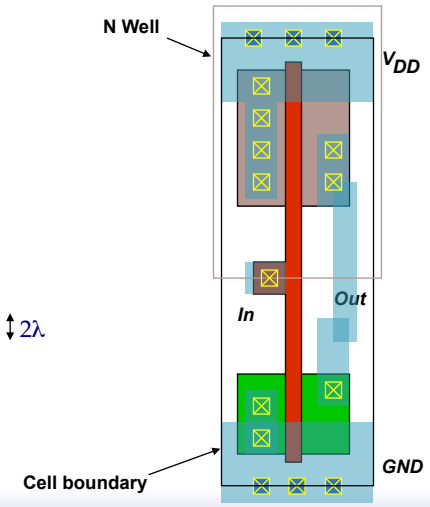
Standard Cells – Then and Now



Standard Cell Layout Methodology – 1990s - Today



Standard Cells



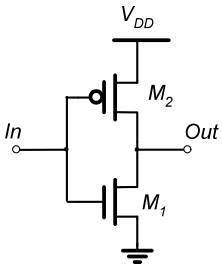
Cell height 12 metal tracks
Metal track is approx. 3λ + 3λ
Pitch =
repetitive distance between objects

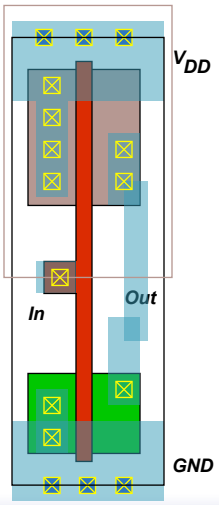
Cell height is "12 Mn pitch"

Rails ~10λ

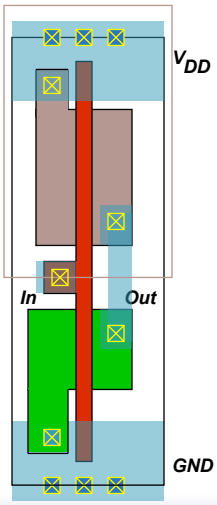
Standard Cells

With minimal diffusion routing

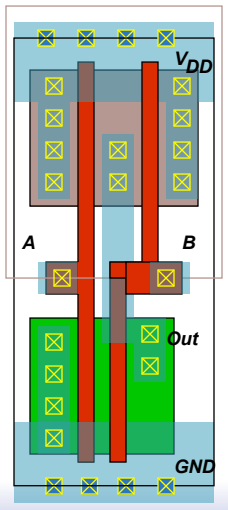




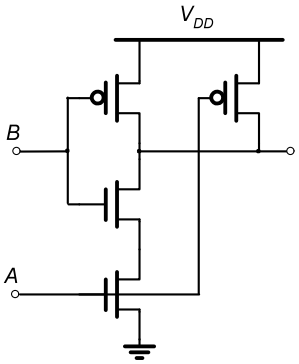
With silicided diffusion



Standard Cells



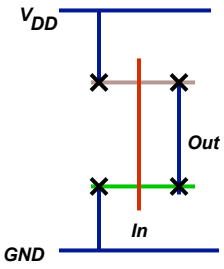
2-input NAND gate



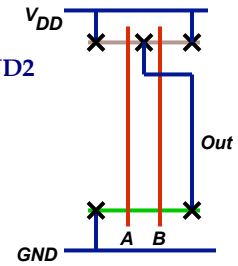
Stick Diagrams

Contains no dimensions
Represents relative positions of transistors

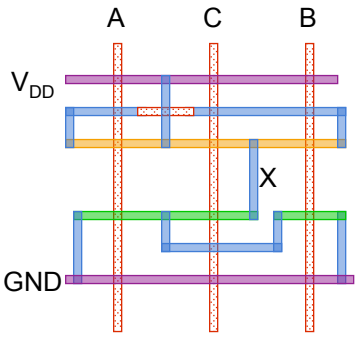
Inverter

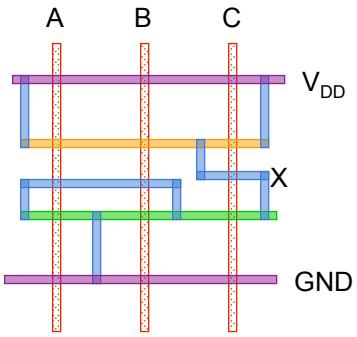


NAND2

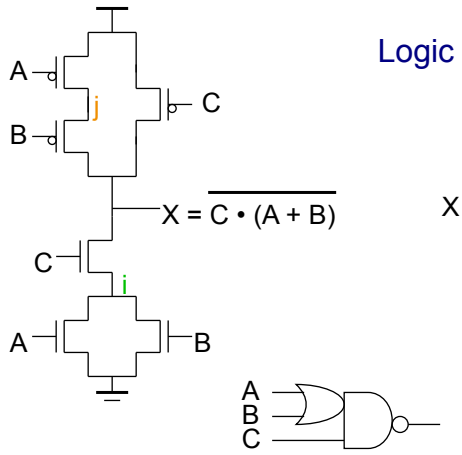


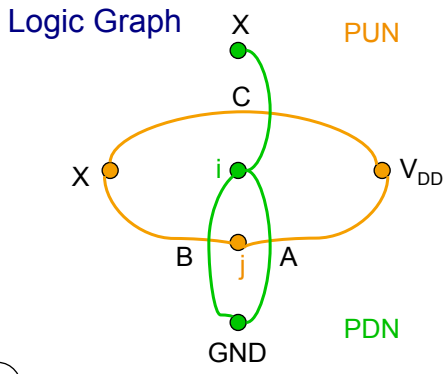
Two Versions of $\overline{C \cdot (A + B)}$





Logic Graphs





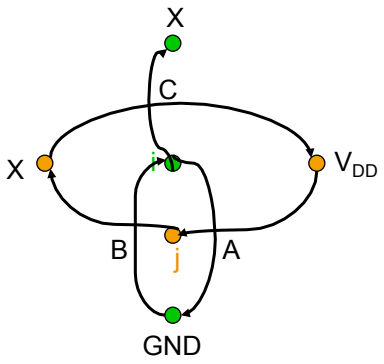
Consistent Euler Path

A B C

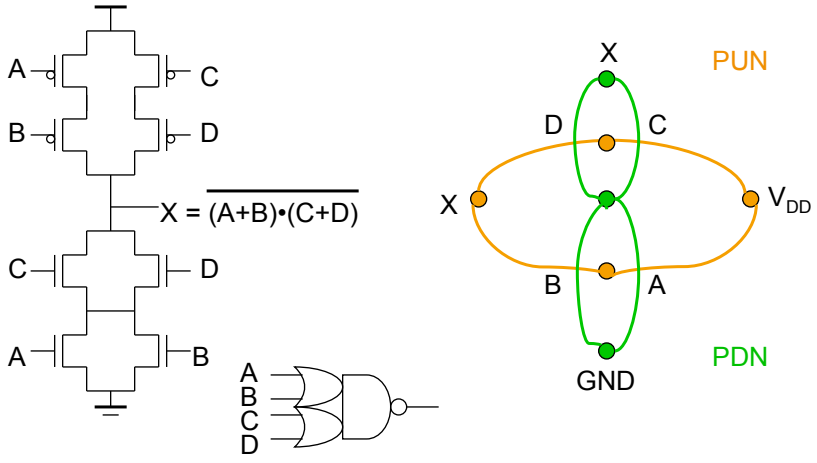
Has PDN and PUN

B C A

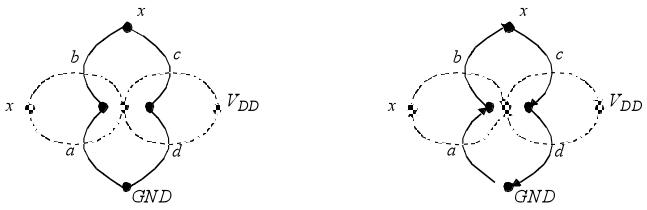
Has PUN, but no PDN



OAI22 Logic Graph

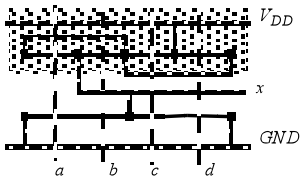


Example: x = ab+cd



(a) Logic graphs for $\overline{(ab+cd)}$

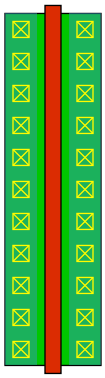
(b) Euler Paths {*a b c d*}



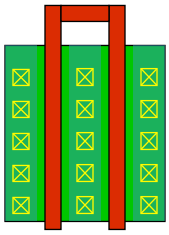
(c) stick diagram for ordering {a b c d}

Multi-Fingered Transistors

One finger



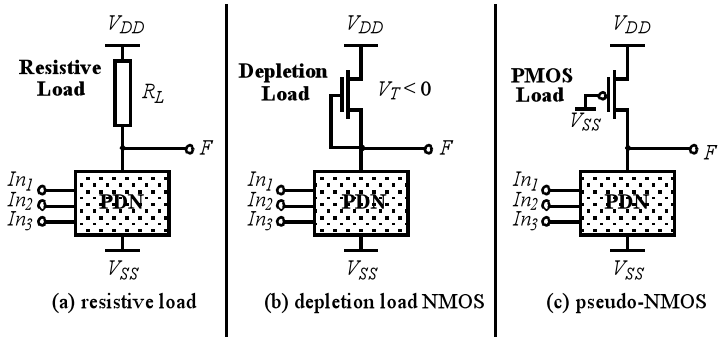
Two fingers (folded)



Less diffusion capacitance

Ratioed Logic

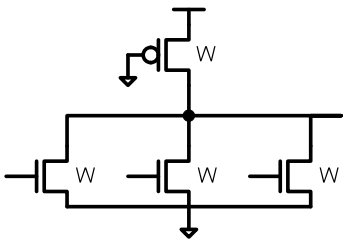
Ratioed Logic

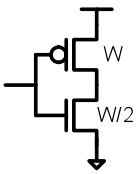


Goal: build gates faster/smaller than static complementary CMOS

Ratioed Logic LE

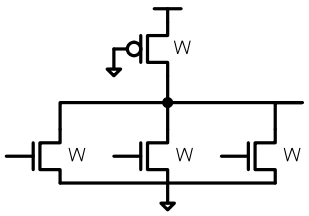
- Rising and falling delays aren't the same
  - Calculate LE for the two edges separately

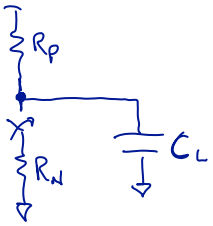




- For tpLH:
  - $C_{gate} = WC_G$ $C_{inv} = (3/2)WC_G$ $LE_{LH} =$

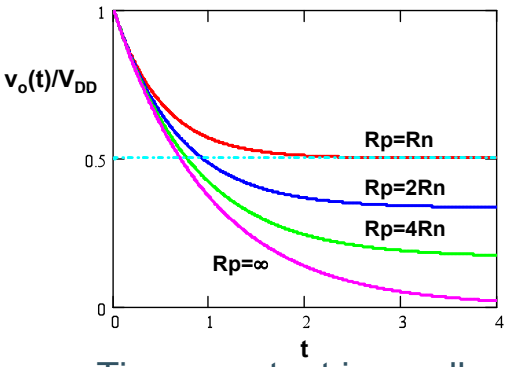
Ratioed Logic LE (pull-down edge)

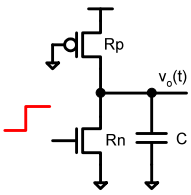




- What is LE for t_{pHL}?
- Switch model would predict $R_{eff} = R_n||R_p$
  - Would that give the right answer for LE?

Response on Falling Edge





$$\tau = \frac{Rn \cdot Rp}{Rn + Rp} \cdot C$$

$$\frac{v_o(t)}{V_{DD}} = \frac{Rn}{Rn + Rp} + \left(1 - \frac{Rn}{Rn + Rp}\right) e^{-t/\tau}$$

- Time constant is smaller, but it takes more time to complete 50% V_{DD} transient (arguably)
  - Rp actually takes some current away from discharging C

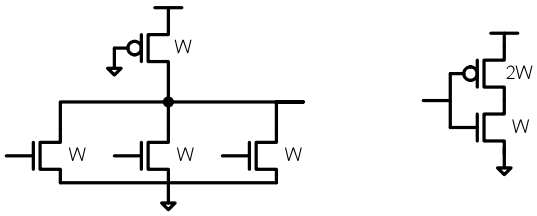
Ratioed Logic Pull-down Delay

- Think in terms of the current driving C_{load}
- When you have a conflict between currents
  - Available current is the difference between the two
  - In pseudo-nMOS case:

$$R_{drive} = \frac{1}{1/Rn - 1/Rp} \longrightarrow R_{drive} = \frac{Rn}{1-(Rn/Rp)}$$

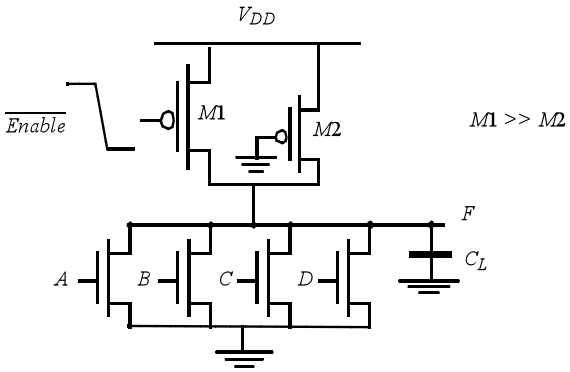
  - (Works because Rp >> Rn for good noise margin)

Ratioed Logic LE (pull-down edge)



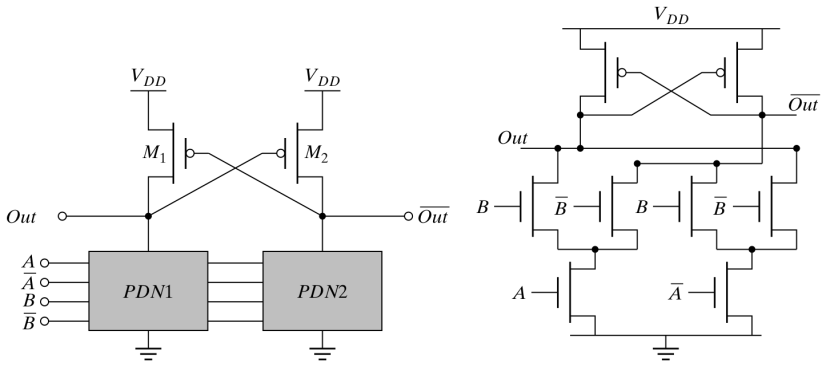
- For t_{pHL} (assuming $R_{sqp} = 2R_{sqn}$):
  - $R_{gate} = R_n/(1\text{-}Rn/Rp) = 2Rn$ $\quad R_{inv} = R_n$
  - $C_{gate} = WC_G$ $\quad C_{inv} = 3WC_G$
  - $LE_{HL} =$
- LE is lower than an inverter!
  - But have static power dissipation…

Improved Loads



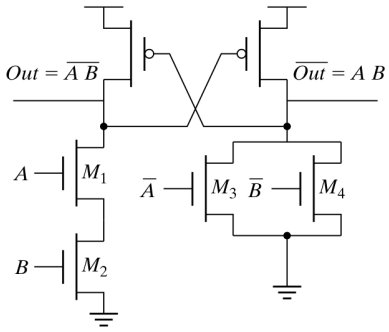
Adaptive Load

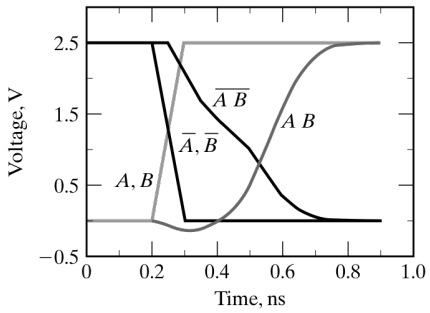
Improved Loads (2)



Differential Cascode Voltage Switch Logic (DCVSL)

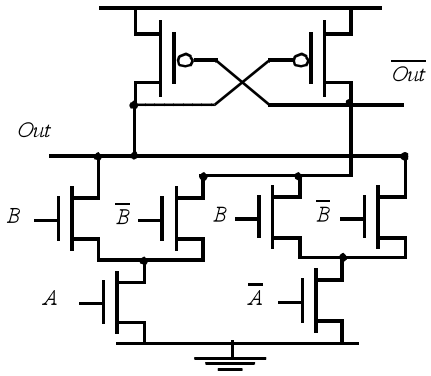
DCVSL Transient Response





DCVSL Example1: AND

DCVSL Example2



XOR/XNOR gate