Texas A&M University
Electrical Engineering Department

ECEN 665

Laboratory #2: Design and Understanding of RF Components: Inductors & Varactors

Objectives: To learn the fundamentals of inductors and varactors for RF CMOS circuits, to learn the design and characterization of inductors and varactors and to understand the use of ASITIC for the simulation of inductors implemented in silicon technologies.

1. VARACTORS

1.1 Explain different types of varactors that are employed in RF CMOS design, and discuss the pros and cons of each. What is the most common use of varactors in RFIC design? Evaluate each different type of varactor and their pros and cons with respect to this common application.

1.2 Use a PMOS transistor (W= 12 x 15um , L=1.2um) to create a varactor. What type of varactor is this? Obtain the Capacitance vs. Vgs plots of this varactor at 1GHz, 1.9GHz and 2.4GHz. Show your simulation setup and include a detailed explanation of how you obtained these characterization plots. *(Hint : Use the "family" and "value" functions of Cadence)*

2. INDUCTORS

2.1. ASITIC Installation

ASITIC is a widely used software employed for the design and optimization of integrated inductors.

The installation files and documentation can be found in:

Main page: http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

FAQ: http://rfic.eecs.berkeley.edu/~niknejad/doc-05-28-01/faq.html

Copy the files provided by the TA in a directory named ASITIC in your UNIX account.

The file asitic_sun is the executable file. Make sure that the file is in executable mode after you transfer it to your account. If this is not the case type: chmod 750 asitic_sun .

The files tsmc18.tek and tsmc35.tek contain the important technology and substrate parameters required for the inductor design in tsmc 0.18um and tsmc 0.35 process. In this lab we will be using the technology file tsmc35.tek (see APENDIX A). A sample session of ASITIC is given in APPENDIX B and a brief manual is given in APPENDIX C.

2.2 Explain the impact of inductor design parameters (metal layer, radius, metal width, etc.) on the inductor performance (inductance, quality factor, parasitics, etc.). Discuss the non-idealities and loss mechanisms in a monolithic inductor. Discuss why in new RF CMOS processes there is a dedicated metal layer for inductors? What are the main distinguishing characteristics of this metal layer?

2.3 Following the sample session, design 10 different inductors (with different shapes, sizes and dimensions for the metal lines). The aim of this exercise is to see the realistic inductor values in this technology (i.e. maximum Q you can achieve with realistic inductance values, etc.) and have an idea of the area it will cost you.
Make a table to show the design parameters you picked for each inductor, include the inductance and quality factor at 1.9GHz (use "pix" command to monitor this). Discuss your observations.
(Some sample dimensions can be taken from: S. S. Mohan, et. Al., "Simple Accurate Expressions for Planar Spiral Inductances", IEEE Journal of Solid-State, Vol. 34, No. 10, October 1999.)

3. INDUCTOR QUALITY FACTOR ANALYSIS

The quality factor Q, of an inductor is characterized by the below equation:

$$Q = IM(Z) / RE(Z)$$

where Z represents the impedance of the inductor and its parasitic elements.

Quality Factor vs. Frequency

3.1 Pick three of the inductors you designed in section 2.3 and check the pi model and quality factor of the inductor at several different frequencies using the ***pix*** command to obtain a plot of Q vs. Frequency. (Note that for a given geometry, inductance will slightly change at different frequencies, as long as this change is small, you can ignore it.). What is the qualitative explanation behind the shape of the Q vs.f curve, what effects are dominant in different parts of this plot?

Quality Factor vs. Inductance

The behavior of the Q factor with respect to the inductance value is of particular interest in RF design. In this section we will obtain Q vs. L curves by changing the geometric properties of inductors.
Figure 1 shows Q vs.L plot for an inductor at 900MHz. The plot is obtained by sweeping the inner radius of the inductor. The two curves also show the effect of different NT values. Figure 2 shows a sample of the inductor layout as R is swept.

3.2 Obtain Q vs. L plots as shown in the figures. Pick a sweep parameter to obtain a plot similar to Figure 1. Perform the pi model analysis for your inductors at three different frequencies to obtain three plots.

Hint : Use pix command for accuracy and keep eddy calculation mode ON for realistic Q values. Don't forget to check your resonance frequency during the pi model analysis of each inductor. The pi model calculation is not accurate and doesn't make sense unless $f_{res} >> f_o$. So make sure all of your designs satisfy $f_{res} \geq 3f_o$

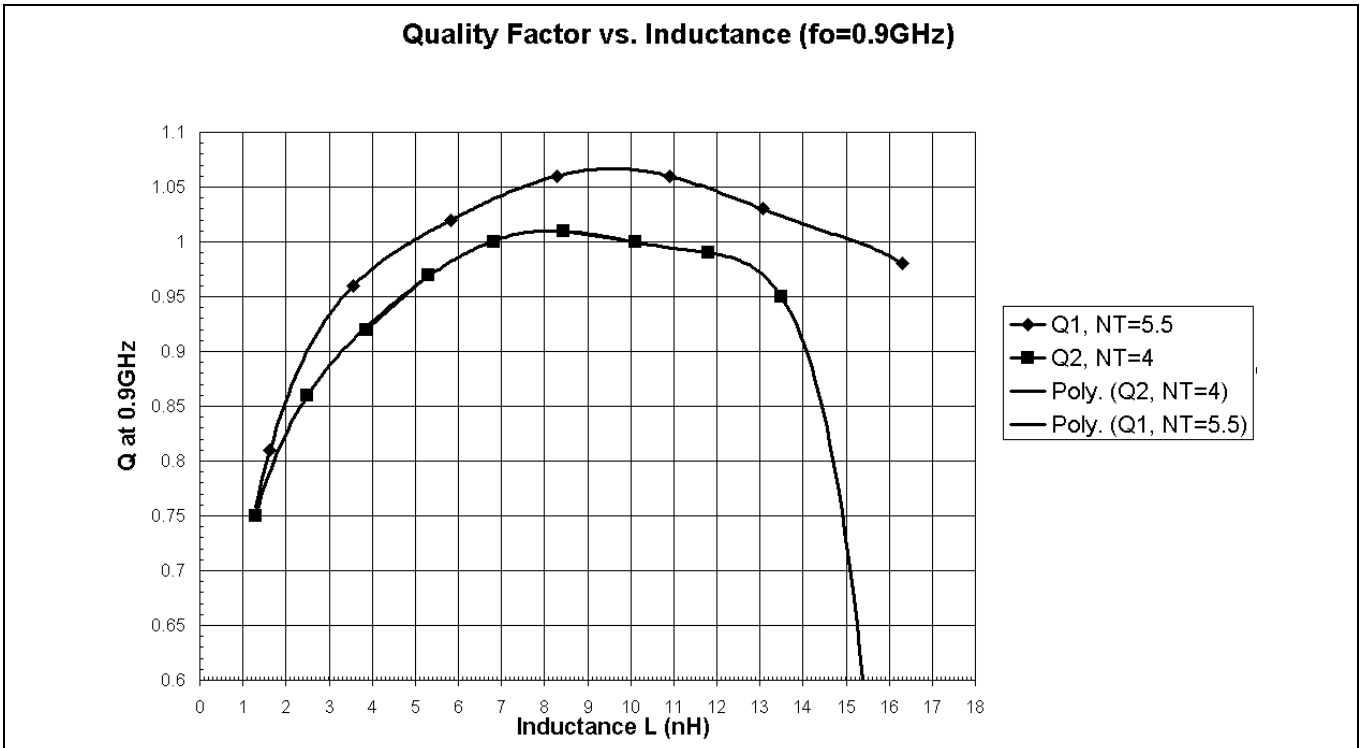

Fig. 1 Q vs. L at 900MHz

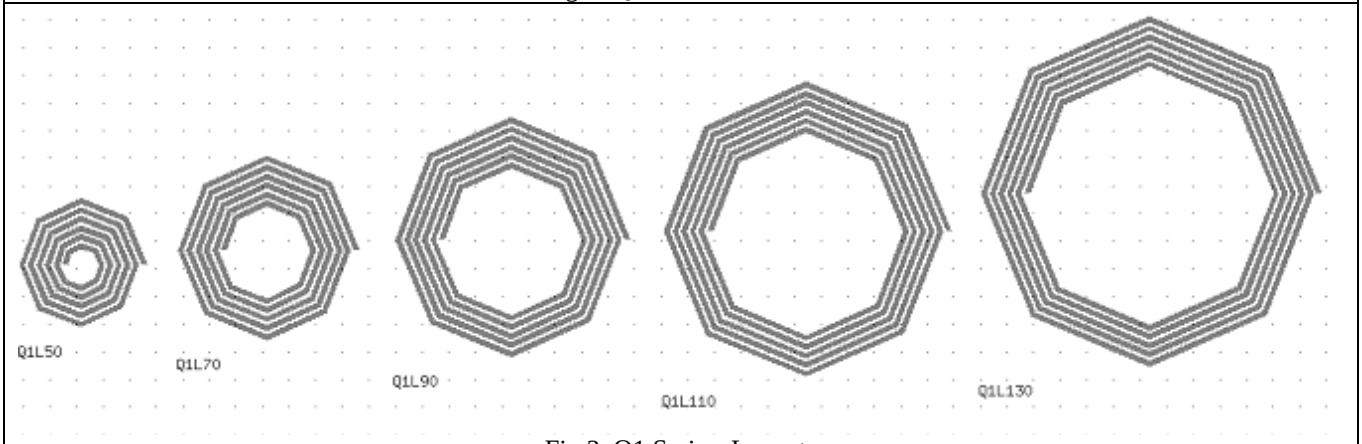

Fig 2. Q1 Series, Layouts

Inductor Quality Factor Optimization

As we saw from section 3.2, for certain frequencies or inductor ranges, Q decreases with increasing inductance value.

Let's take an inductor L1 with Q1 = ωL1 / R1 . Theoretically, if we add two of these inductors in series we will have equivalent inductance Leq = 2L1 but the effective Q will be Qeq = Q1. Figure 3. shows this.

However, we have seen that under certain conditions Q decreases for increasing inductance for a single inductor. Then, we could form large inductors from series combination of smaller inductors and therefore obtain a better Q than we would have by using one large inductor. Figure 4 represents this statement.

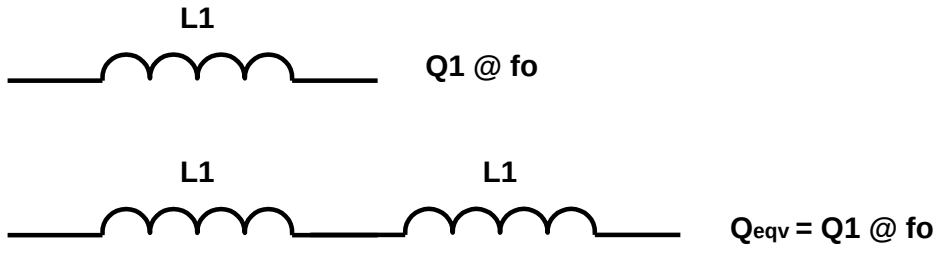

Figure 3. Equivalent Q of Series Connection of inductors

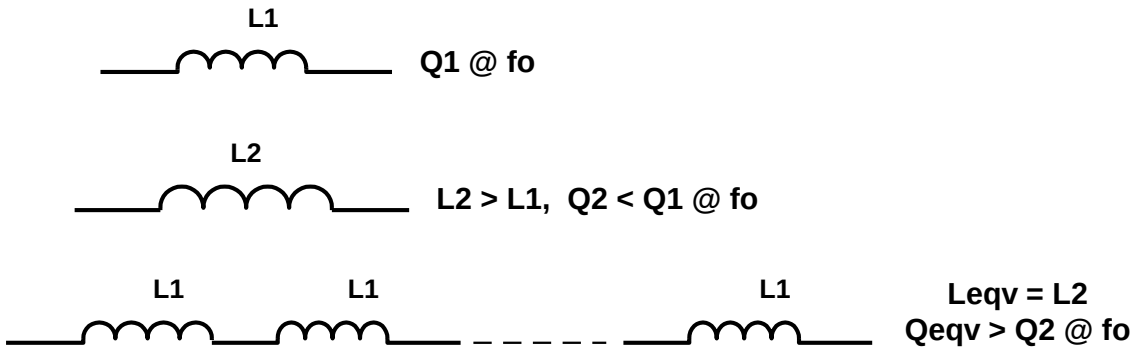

Figure 4. Q improvement of a large inductor through distributed implementation

3.3 Is the above statement true? Please clearly state your answer. Support your answer with theoretical physical reasoning and ASITIC examples. You can use "join" command to perform series addition of inductors. (For any inductor you use in your explanation, give the values of all the geometry parameters for that inductor as well as the pi model results for a particular frequency. Make sure that you are doing a fair comparison between inductors.)

Below are some ASITIC tips to help with this section of the exercise. Please refer to the Appendix for detailed information on ASITIC.

• You can change the chip size that you are working on, to fit more inductors on it. Use the command "chip"
• You can hide the inductors to open some empty space in your layout, use "hide"
• To move an inductor you can either use the "move" commands (check: help edit). Or, you can select an inductor with your mouse and then drag it by clicking the middle button of your mouse to move it.
• To see the current flow directions in an inductor, use "Showdir".
• You can join two inductors in series with "join" command. Please read more about this from the ASITIC website and help documentation. Check the latest version of this documentation from the website.
• You can split joined inductors using "split" command. You can choose the segment to split the inductor from. For example, to join two inductors and then split them back to two separate inductors:

Final Remarks:
Your reports for this lab are due next week's lab session.