**University of California**
**College of Engineering**
**Department of Electrical Engineering**
**and Computer Sciences**

**D. Markovic**

**TuTh 11-12:30**

**Thursday, October 6, 6:30-8:00pm**

# EECS 141: FALL 05—MIDTERM 1

| **NAME** | **SOLUTION**<br>Last First |
|---|---|

| **SID** | |
|---|---|

**Problem 1 (15): 15**

**Problem 2 (13): 13**

**Problem 3 (12): 12**

| **Total (40)** | **40** |
|---|---|

**PROBLEM 1: VTC, Delay (15 pts)**

Consider the digital circuit shown in Fig. 1a. Assume **short-channel** transistor and you may also assume that **all capacitances are constant and linear over the operation range**. External load capacitance $C_L$ = 1fF, $V_{DD}$ = 2.5V, $R$ = 40kΩ. Parameters of NMOS transistor are given below:

| |
|---|
| k' = 100 μA/V$^2$, $V_{T0}$ = 0.5V, $V_{DSAT}$ = 0.5V, γ = 0, λ = 0, W / L = 0.5μm / 0.25μm |
| WL·$C_{ox}$ = 0.6 fF, $C_{DB}$ = $C_{SB}$ = 0.1 fF, $C_{GD,overlap}$ = $C_{GS,overlap}$ = 0.1 fF |

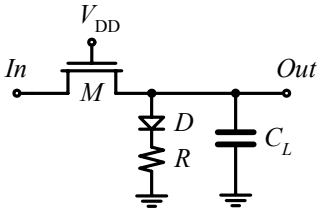
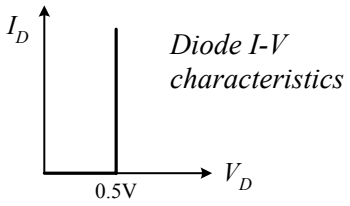
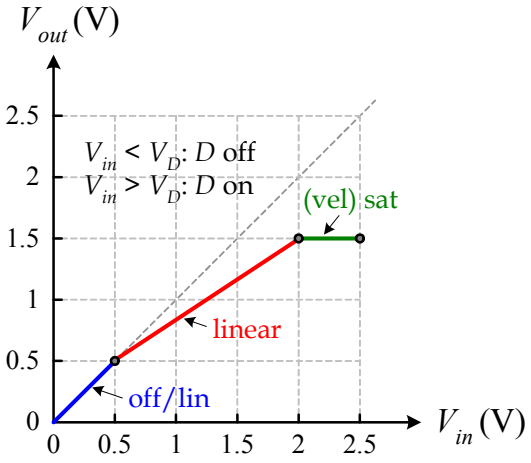


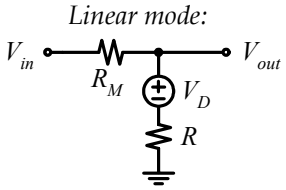

**Fig. 1a**




**a.** Sketch the VTC for this circuit using the diagram below. Clearly indicate break points and operation modes of transistor $M$ and diode $D$. What is $V_{out}$ when $V_{in} = V_{DD}$? **(5 pts)**




**$V_{out}$ ($V_{in}$ = $V_{DD}$) = 1.5V**




**Solution:**

**(1pt)** $0 < V_{in} < 0.5\text{V} \Rightarrow$ Diode **off** $\Rightarrow I_D = 0$, ($M$ **off/lin**) $\Rightarrow V_{out} = V_{in}$

**(1pt)** $V_{in} = 2.5\text{V}$ (large bias voltage) $\Rightarrow$ **assume vel sat**

$$V_{out} = V_D + R \cdot k' \frac{W}{L}\left[\left(V_{DD} - V_{T0} - V_{out}\right)\cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}\right] = 1.5\text{V}$$

**(0.5pts)** Verify assumption: $V_{DS} = V_{in} - V_{out} = 1\text{V} > V_{DSAT}$
Also: $V_{GT} = 0.5\text{V} = V_{DSAT} \Rightarrow$ edge of **sat / vel sat** $\Rightarrow$ good assumption!

**(1.5pts)** **(Vel) sat** & λ = 0 $\Rightarrow$ constant current until $V_{DS} = V_{DSAT}$ ($V_{in} = 1.5\text{V} + V_{DSAT} = 2\text{V}$)
Current: $I_M = I_D = (V_{out} - V_D) / R = 25\mu\text{A}$, $\boldsymbol{V_{out}}$ **= const = 1.5V**

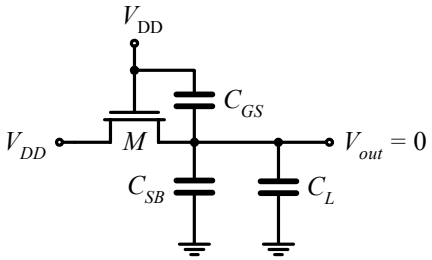
**(1pt)** $V_{DS} = V_{in} - V_{out}$, $V_{GT} = V_{DD} - V_{out} - V_{T0} \Rightarrow$ **linear** when $V_{in} < V_{DD} - V_{T0}$
Equivalent $R_M$ ($V_{in}$ = 2V, $V_{out}$ = 1.5V): $R_M = V_{DS} / I_M = 0.5\text{V} / 25\mu\text{A} = 20\text{k}\Omega$
Linear mode: $V_{out} = V_D + R / (R + R_M)\, V_{in} \Rightarrow$ $\boldsymbol{V_{out}}$ **= 0.5V + 2/3** $\boldsymbol{V_{in}}$

**b.** Calculate the delay of the circuit in Fig. 1a when the input changes from 0 to $V_{DD}$. Let $V_M = 1$V and assume that $V_{in}$ was at 0 for a long time before the transition. If you are not sure of your answer in (a), assume that the output reaches final value $V_{high} = 1.75$V. What are the equivalent capacitance, equivalent resistance, and the delay? **(5 pts)**

**Solution:**

**$C_{eq}$ = 1.6fF**
**$R_{eq}$ = 13.8kΩ**
**$t_p$ = 18.7ps (or 24.3ps)**

**(1pt)** Calculation of $C_{eq}$:



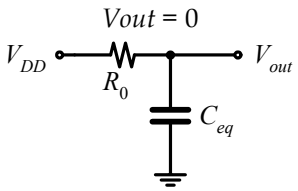

Transistor capacitances are shown in the figure.

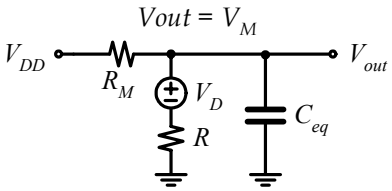
$M$ is **vel sat** at the beginning of transition:
$C_{eq,M} = C_{SB} + C_{GS,overlap} + 2/3 \cdot WL \cdot C_{ox} = 0.6$fF

Equivalent capacitance is therefore:
$\boldsymbol{C_{eq} = C_{eq,M} + C_L = 1.6\text{fF}}$

**(3pts)** Calculation of $R_{eq}$:

Equivalent circuits at the beginning and mid-point are shown below.
In both cases, $V_{min} = V_{DSAT}$, so $M$ is in **velocity saturation**.




Observe: For $V_{GS} = V_{DS} = V \Rightarrow R_{NMOS} = \dfrac{V}{k'\dfrac{W}{L}\left[(V - V_{T0}) \cdot V_{DSAT} - \dfrac{V_{DSAT}^2}{2}\right]}$

$R_0$ calc: $V_{DS} = V_{DD} \Rightarrow R_0 = 14.3\text{k}\Omega$ (1pt)
$\boldsymbol{R_{eq}(V_{out} = 0) = 14.3\text{k}\Omega}$

$R_M$ calc: $V_{DS} = V_{DD} - V_M \Rightarrow R_M = 20\text{k}\Omega$ (1pt)
$\boldsymbol{R_{eq}(V_{out} = V_M) = R \parallel R_M = 13.3\text{k}\Omega}$ (0.5pts)

Therefore: $\boldsymbol{R_{eq} = (R_{eq}(V_{out} = 0) + R_{eq}(V_{out} = V_M)) / 2 = 13.8\text{k}\Omega}$ (0.5pts)

**(1pt)** Calculation of delay:

Notice that $V_M$ is not at 50% of full swing, so we go back to basic principles.
Starting from $V_{out}(t) = V_{high} \cdot \left(1 - e^{-t/\tau}\right)$, we derive propagation delay as follows:

$t_p = \tau \cdot \ln \dfrac{V_{high}}{V_{high} - V_M} \Rightarrow \boldsymbol{t_p = 0.85 \cdot R_{eq} C_{eq} = 18.7\text{ps}}$

Using $V_{high} = 1.5$V from part (a) yields $\boldsymbol{t_p = 1.1 \cdot R_{eq} C_{eq} = 24.3\text{ps}}$

**c.** What is the energy dissipated as heat during high-to-low transition at the output? Assume input voltage step from $V_{DD}$ to 0 and initial $V_{out} = 1.75$V. **(1 pt)**

**Solution:**

**$E_{diss}$ = 2.45fJ**

Energy stored on the output capacitor is dissipated as heat during the discharge operation. Therefore, $\boldsymbol{E_{diss} = 0.5 \cdot C_{eq} V_{out}^2 = 2.45\text{fJ}}$ (1pt)

**d.** For the circuit in Fig. 1b, determine the final value of $V_A$, $V_B$, $V_C$, assuming initial condition at each of the nodes is 3V and $V_{TP} = -0.5$V (ignore body effect). **(2 pts)**

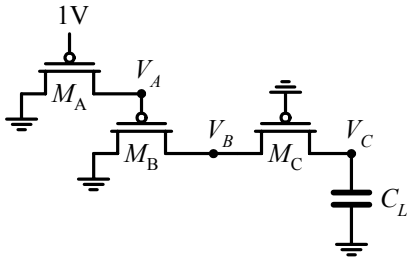



**Fig. 1b**

**$V_A$ = 1.5V**
**$V_B$ = 2V**
**$V_C$ = 2V**

**Solution:**

No current flows into the gate $\Rightarrow I_{DA} = 0 \Rightarrow V_A = V_{GA} - V_{TA} = 1.5$V (0.5pts)
Since $V_A <$ initial $V_B$, $M_B$ is also **off** $\Rightarrow V_B = V_A - V_{TB} = 2$V (0.5pts)
Finally, $M_C$ passes logic "1" to the output $\Rightarrow V_C = 2$V (1pt)

**e.** Assuming that switch closes at time $t = 0$, what is the output voltage at $t = 0^+$ and $t = \infty$ for the circuit in Fig. 1c? $C_L$ was initially discharged, $V_{TP} = -0.5$V. Briefly explain your answer (one line for each point). **(2 pts)**

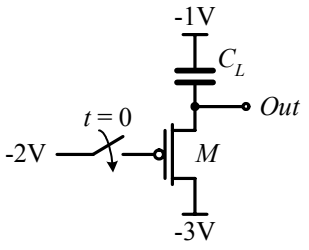



**Fig. 1c**

**$V_{out}$ ($t = 0^+$) = –1V**
**$V_{out}$ ($t = \infty$) = –1.5V**

**Solution:**

**$t = 0^+$:** Voltage across $C_L$ cannot change instantaneously $\Rightarrow$ $V_{out}$ stays at –1V (1pt)

**$t = \infty$:** No DC current through $C_L$ $\Rightarrow$ $M$ is **off** $\Rightarrow V_{out} = V_G - V_{TP} = -1.5$V (1pt)

**PROBLEM 2: Sizing (13 pts)**

Assume the inverters are implemented in standard CMOS with symmetrical VTC. Furthermore, assume $C_{intrinsic} = C_{gate}$ ($\gamma = 1$). Equivalent resistance and input capacitance of unit-sized inverter are $R$ and $C$, respectively. Sizing factor $S \geq 1$.

**a.** For inverters in Fig. 2a, pick the best sizing factors $S_2$ and $S_3$ to minimize propagation delay. What is the minimum delay (in terms of $t_{p0}$)? **(3 pts)**

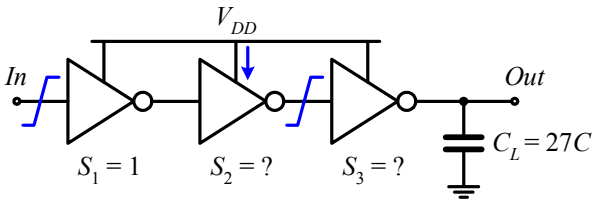



**Fig. 2a**

**$S_2 = 3$**
**$S_3 = 9$**
**$t_p = 12t_{p0}$**

**Solution:**

Standard buffer problem, size increases geometrically.
Optimal fanout is: $f_{opt} = \sqrt[3]{27} = 3$ (1pt)

Using well-known geometric mean result, we get:
$S_2 = 3$, $S_3 = 9$ (1pt)

All stages have equal delay, so propagation delay is given by:
$t_p = 3t_{p,stage} = 3t_{p0} \cdot (1 + f_{opt}) = 12t_{p0}$ (1pt)

**b.** What is the total energy drawn from supply when the input switches from 0 to $V_{DD}$? What is the total energy dissipated as heat by the circuit? (Answer in symbolic terms: $C$, $V_{DD}$) **(2 pts)**

**Solution:**

**$E_{supply} = 12CV_{DD}^2$**
**$E_{diss} = 26CV_{DD}^2$**

The total switched capacitance during 0→1 at the input is:
$C_{sw} = C_{intrinsic,stage\text{-}2} + C_{gate,stage\text{-}3} = f \cdot C + f^2 \cdot C = 12C$

The total energy taken out of supply (second stage) is: $\boldsymbol{E_{supply} = 12CV_{DD}^2}$ (1pt)

Energy stored on $C_{sw}$ is $E_{C,0\to1} = 0.5C_{sw}V_{DD}^2 = 6CV_{DD}^2$.
Energy dissipated as heat is obtained by taking the difference + energy discharged from caps of the first ($2CV_{DD}^2$) and third stage ($18CV_{DD}^2$).

Therefore, $\boldsymbol{E_{diss} = 26CV_{DD}^2}$ (1pt)

**c.** For inverters in Fig. 2a (previous page), pick the best sizing $S_2$ and $S_3$ to minimize energy consumption. You may assume square wave at the input with period $T$. What is the total energy consumed for a full cycle ($0\rightarrow1$, $1\rightarrow0$)? **(3 pts)**

**Solution:**

**Energy = min** when total **C = min**. (1pt)
$S_{min} = 1 \Rightarrow S_2 = S_3 = 1$. (1pt)

The total capacitance charged during a full cycle ($0\rightarrow1$, $1\rightarrow0$) is:
$C_{cycle} = (C_{int,stage\text{-}1} + C_{gate,stage\text{-}2}) + (C_{int,stage\text{-}2} + C_{gate,stage\text{-}3}) + (C_{int,stage\text{-}3} + C_L) = 32C$
The total energy consumed for a full cycle is: $\boldsymbol{E_{cycle} = 32CV_{DD}^2}$ (1pt)

$\boldsymbol{S_2 = 1}$
$\boldsymbol{S_3 = 1}$
$\boldsymbol{E_{cycle} = 32CV_{DD}^2}$

**d.** What is the delay (in terms of $t_{p0}$) of the circuit in Fig. 2b? **(2 pts)**

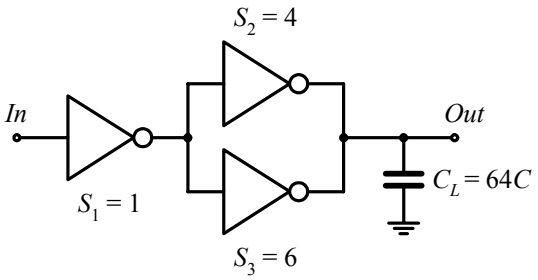



**Fig. 2b**

**Solution:**

Parallel inverters can be replaced with equivalent inverter of size $S = 10$. (1pt)

The delay is simply calculated as:
$t_p = t_{p0}\cdot(1+10) + t_{p0}\cdot(1+64/10)$ (1pt)
$\boldsymbol{t_p = 18.4t_{p0}}$

$\boldsymbol{t_p = 18.4t_{p0}}$

**e.** Assume you can choose the sizing $S_2$ and $S_4$ for inverters in Fig. 2c. What are the optimal values for minimum delay? What is the delay (expressed in terms of $t_{p0}$)? **(3 pts)**

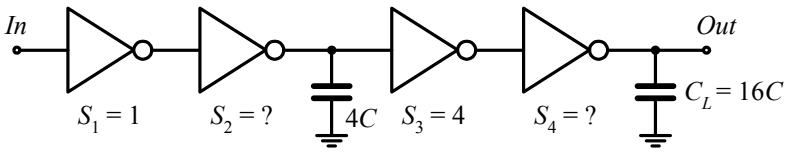



**Fig. 2c**

**Solution:**

To find the optimal sizing factors for minimum delay, we start from the delay expression. The delay of the circuit in Fig. 2b, normalized to $t_{p0}$ is:

$$d = (1+S_2) + (1+8/S_2) + (1+S_4/4) + (1+16/S_4) \qquad \text{(1pt)}$$

Taking partial derivative with respect to $S_2$ and $S_4$, we get:

$$1 - \frac{8}{S_2^2} = 0 \;\Rightarrow\; S_2 = 2\sqrt{2}$$

$$\frac{1}{4} - \frac{16}{S_4^2} = 0 \;\Rightarrow\; S_4 = 8 \qquad \text{(1pt)}$$

Finally, we compute the delay. Observe that the delay of the first two stages is equal (opt fanout = $f_{12} = 2\sqrt{2}$ ) and the delay of the last two stages is equal (opt fanout = $f_{34} = 2$).

$$t_p = 2\cdot(1+f_{12})\cdot t_{p0} + 2\cdot\left(1+\frac{16}{f_{34}}\right)\cdot t_{p0} = 4\cdot\left(2+\sqrt{2}\right)\cdot t_{p0} \qquad \text{(1pt)}$$

$\boldsymbol{S_2} = 2\sqrt{2}$
$\boldsymbol{S_4} = 8$
$\boldsymbol{t_p} = 4\cdot\left(2+\sqrt{2}\right)\cdot t_{p0}$

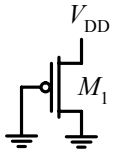
**PROBLEM 3: General Knowledge (12 pts)**

**a.** Determine the region of operation (Off, Linear, Saturation, Velocity saturation) in the following configurations. You may assume that all transistors are **short-channel devices** and have identical sizes, $V_{DD} = 2.5\text{V}$. Assume following transistor parameters:

NMOS: $V_{Tn} = 0.4\text{V}$, $k_n = 115\mu\text{A/V}^2$, $V_{DSATn} = 0.6\text{V}$, $\lambda = 0$, $\gamma = 0.4\text{V}^{1/2}$, $2\Phi_F = -0.6\text{V}$
PMOS: $V_{Tp} = -0.4\text{V}$, $kp = -30\mu\text{A/V}^2$, $V_{DSATp} = -1\text{V}$, $\lambda = 0$, $\gamma = -0.4\text{V}^{1/2}$, $2\Phi_F = 0.6\text{V}$

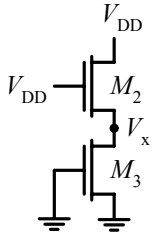
Explain your reasoning and show your derivations if needed. **(5 pts)**

**Solution:**



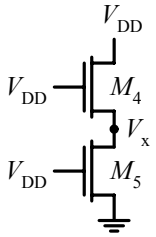

$V_{GS1} = V_{DS1} = -2.5\text{V}$

$|V_{DSAT1}| < |V_{GT1}| < |V_{DS1}| \Rightarrow$ **$M_1$ velocity saturation** (1pt)




$V_{GS3} = 0 < V_{T3} \Rightarrow$ **$M_3$ off** (1pt)

$V_x = V_{DD} - V_{T2} \Rightarrow$ **$M_2$ off** (1pt)




$V_{T4} > V_{T5}$ (body effect) $\Rightarrow V_{DS5} < V_{GT5} \Rightarrow$ **$M_5$ linear** (1pt)

Assume $M_4$ **vel sat** and ignore body effect in the first iteration:

$$\left(V_{DD} - V_{T4}\right) \cdot V_x - \frac{V_x^2}{2} = \left(V_{DD} - V_x - V_{T5}\right) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}$$

$V_x = 0.435\text{V} \Rightarrow$ **$M_4$ velocity saturation** (1pt)

**Note:** Body effect will only lower $V_x$ and increase $V_{DS4}$, $V_{GT4}$ (0.435V is the worst-case).

**b.** The first row of the table given below lists the characteristics of a successful microprocessor designed for desktop systems. A low power version for portable use is desired and several changes are therefore made to the design. Use simple hand calculations to fill in estimates for blank cells in the table. Use the space below to explain your answers (if needed). All transistors exhibit **short-channel I-V characteristics. (5 pts)**

| | $V_{DD}$ / $V_T$ (V) | W, L, $t_{ox}$ (relative) | C (nF) | $I_{SAT}$ (mA) | Clock (GHz) | Area ($mm^2$) | Power (W) |
|---|---|---|---|---|---|---|---|
| **Original** | 2.5 / 0.4 | 1 | 1 | 1 | 2.4 | 100 | 8 |
| **Voltage Scaling** | 1.25 / 0.2 | 1 | 1 | **0.5** | **2.4** | **100** | **2** |
| **General Scaling** | 1.25 / 0.2 | 0.6 | **0.6** | **0.5** | **4** | **36** | **2** |

**Solution:**

Assuming that voltage scaling factor is U and that transistor dimensions scale with factor S, recall following simple formulas from the general scaling theory:

$C \sim WL/t_{ox} \sim 1/S$

$I_{SAT} = v_{sat} \cdot C_{ox} \cdot W \cdot (V_{GT} - V_{DSAT}) \sim U$

$f_{Clk} \sim 1/C \sim 1/S$

$Area \sim WL \sim S^2$

$Power \sim f_{Clk} \cdot C \cdot V_{DD}^2 \sim U^2$

Each entry in the table is worth 0.5pts (total 4.5pts) + 0.5pts for formulas/calculations.

**c.** For each of the following statements, indicate whether it is true or false (circle one answer). **(2 pts, 0.5 for correct answer, –0.25 for wrong one)**

(T) **F** (a) The load capacitance of a static CMOS gate has no effect on its VTC.

**T** (F) (b) The delay of a static CMOS inverter is minimized if $(W/L)_p / (W/L)_n = \mu_n / \mu_p$.

**T** (F) (c) Silicided poly lines improve performance by decreasing the capacitance.

**T** (F) (d) PMOS enters vel. saturation for smaller absolute value of electric field than NMOS.