EE288 Data Conversions/Analog Mixed-Signal ICs
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Lecture 16: DAC 2

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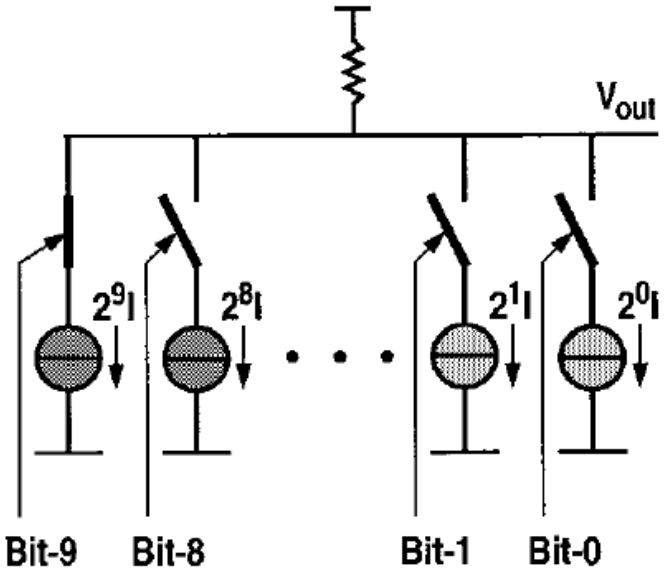
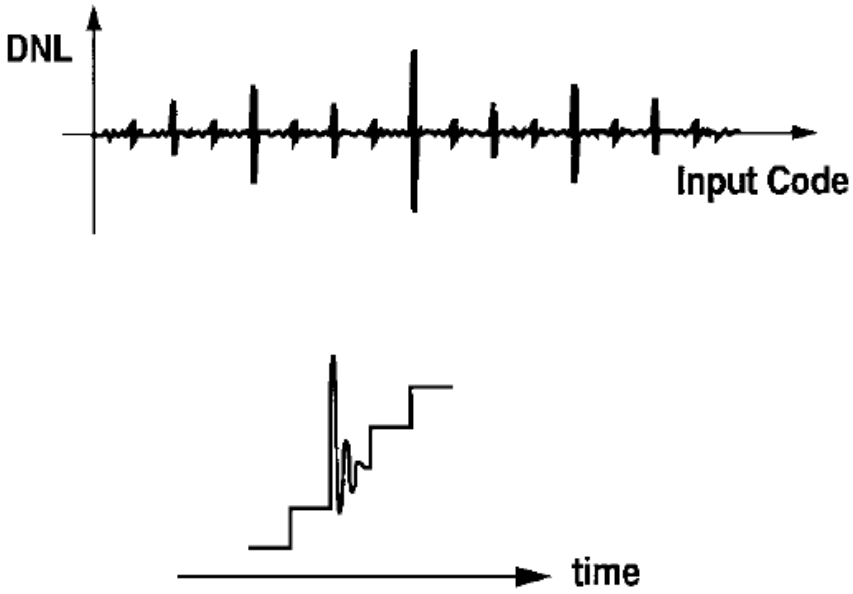
DAC Architectures

- Resistor-string DAC
- Charge-redistribution DAC
- Current-steering DAC

- Binary-weighted DAC
- Unit-element (thermometer-coded) DAC
- Segmented DAC

Binary Weighted Current Steering DAC

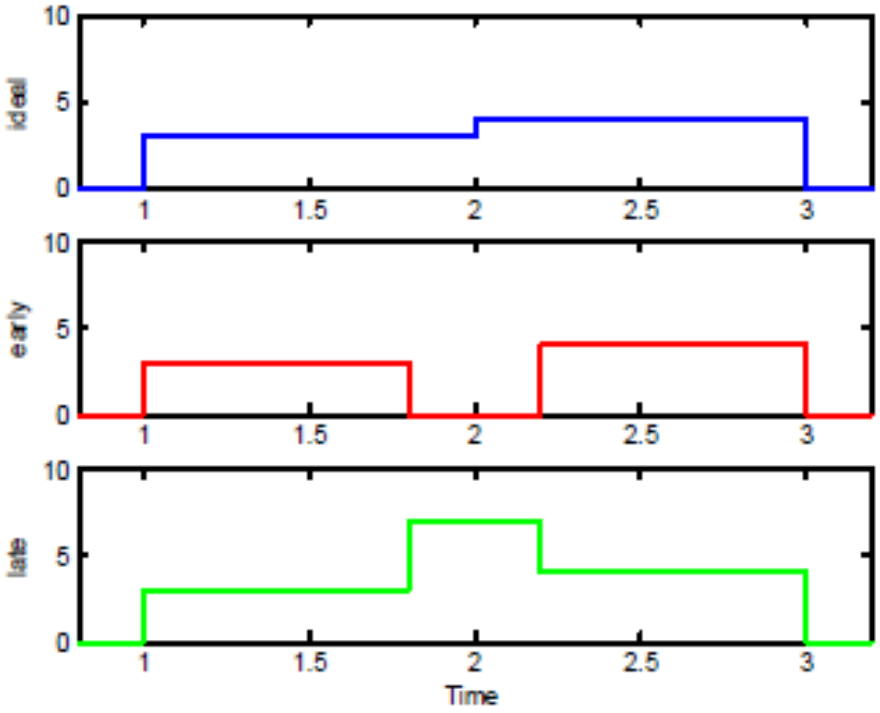




Ref: C.-H. Lin and K. Bult, “A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2,” *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

Glitches of Binary Weighted DAC

- DAC output waveform depends on timing
  - Consider binary weighted DAC transition 0111… → 1000…

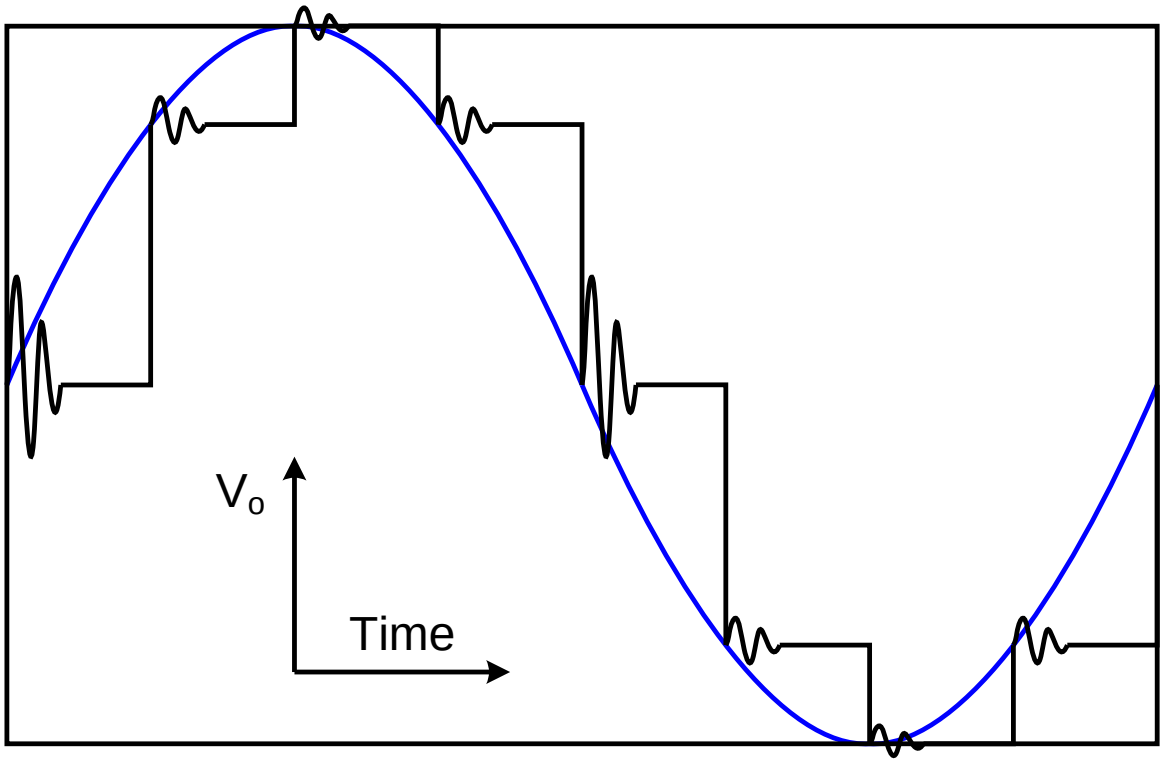


Ideal

LSBs early, MSB late

LSBs late, MSB early

Output Glitches



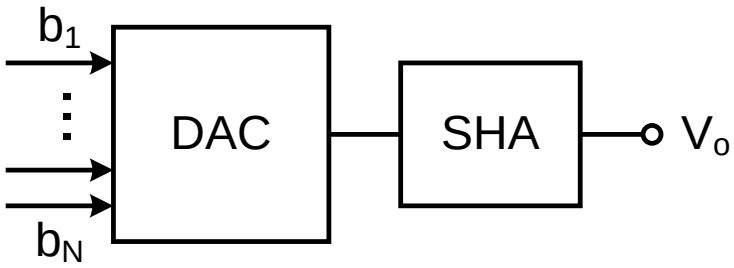
- Cause: Signal and clock skew in circuits
- Especially severe at MSB transition where all bits are switching –

  0111…111 →

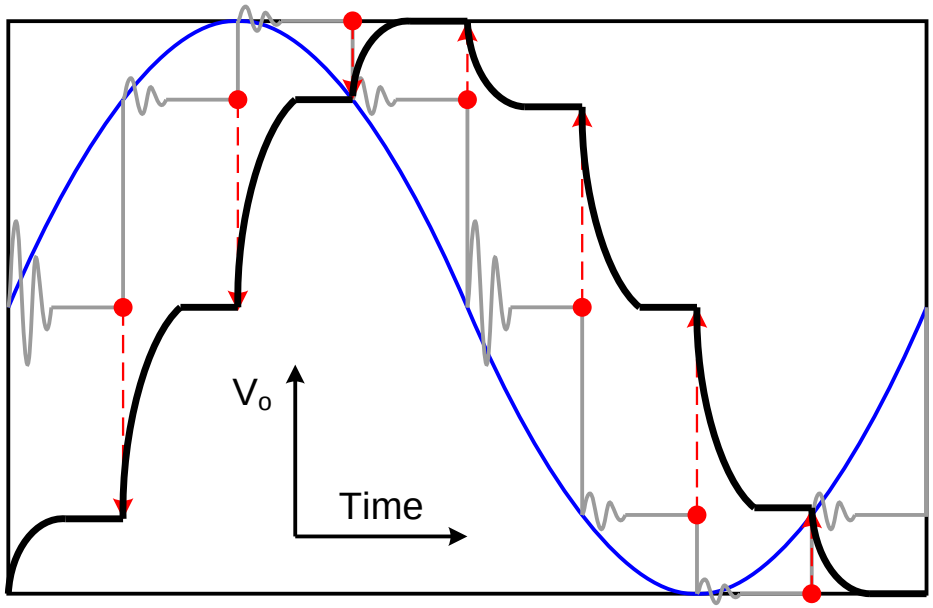
  1000…000

- Glitches cause waveform distortion, spurs and elevated noise floors
- High-speed DAC output is often followed by a de-glitching SHA

De-Glitching SHA

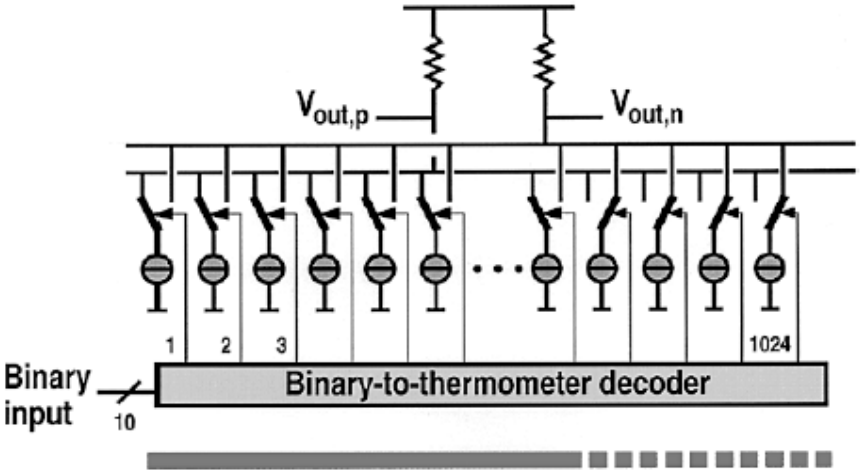


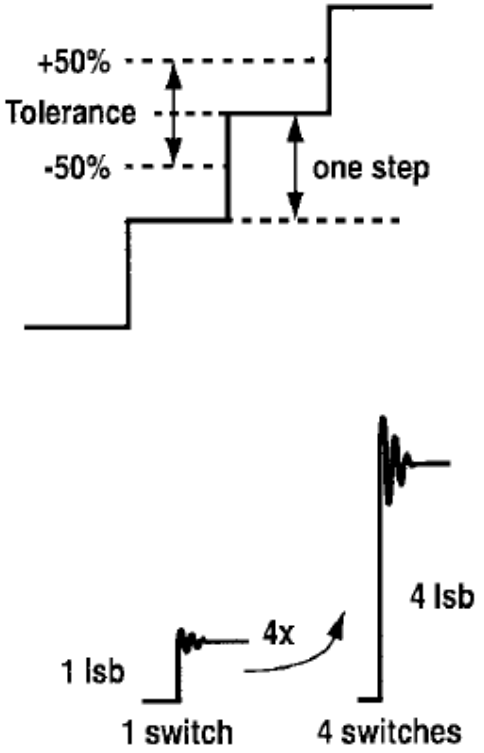
SHA samples the output of the DAC after it settles and then hold it for T, removing the glitching energy.



SHA output must be smooth (exponential settling can be viewed as pulse shaping → SHA BW does not have to be excessively large).

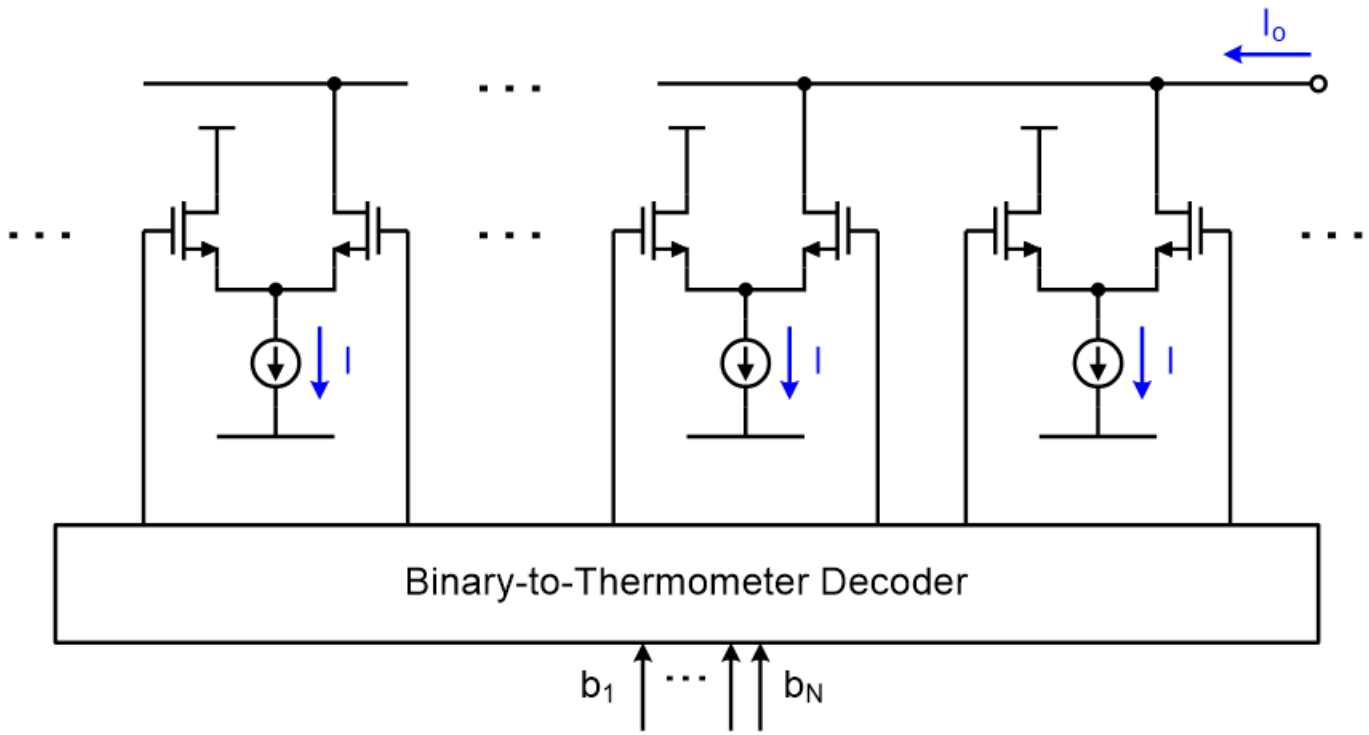
Thermometer Coded Unary DAC





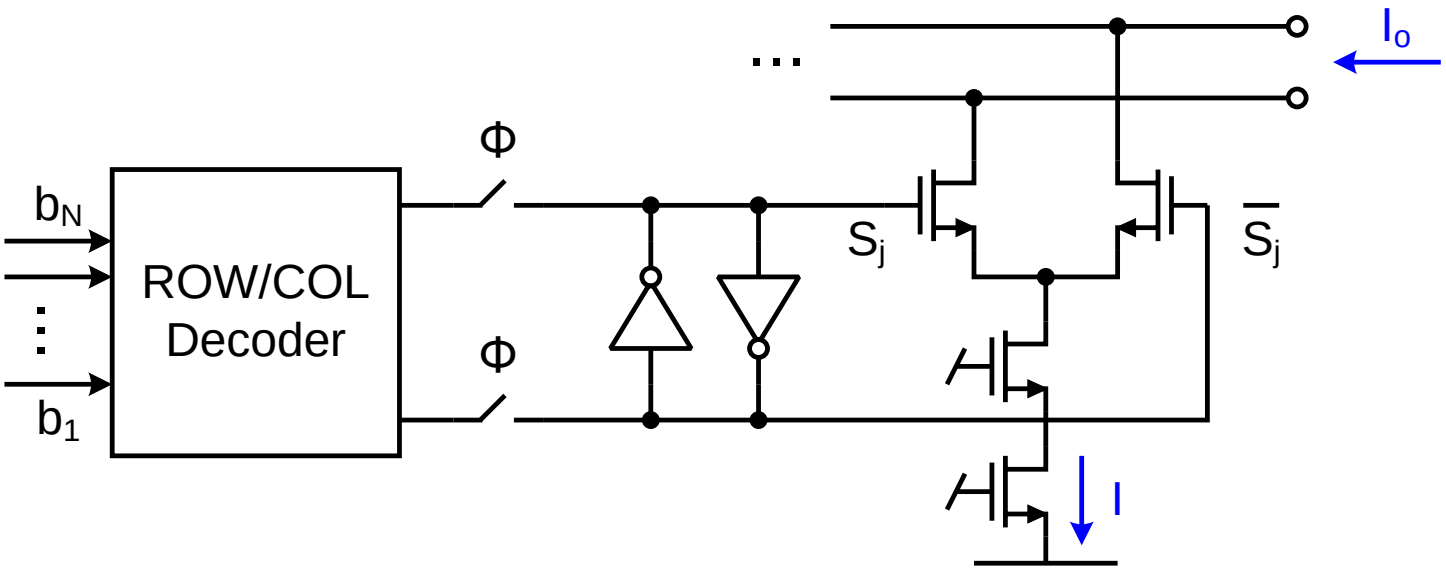
Ref: C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6mm^2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948-1958, issue 12, 1998.

Current Steering DAC



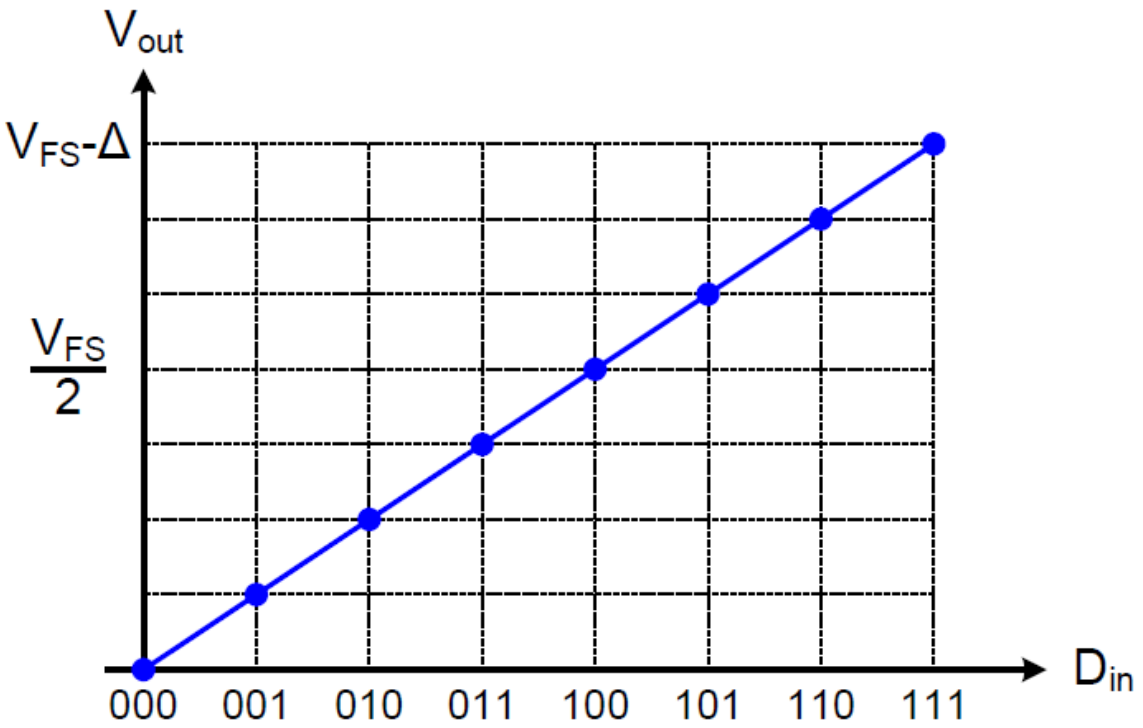
- Fast, inherently monotonic → good DNL performance
- Complexity increases for large N, requires B2T decoder

Current Cell

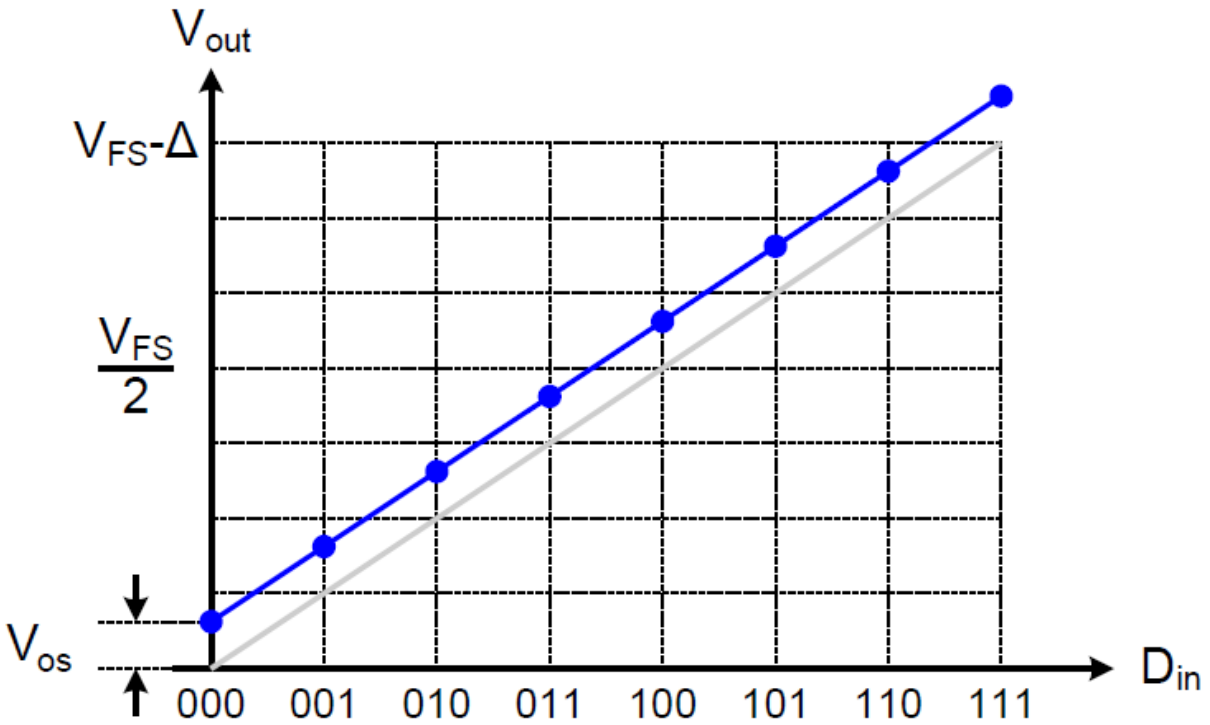


- 2^N current cells typically decomposed into a $(2^{N/2} \times 2^{N/2})$ matrix
- Current source cascoded to improve accuracy (R_o effect)
- Coupled inverters improve synchronization of current switches

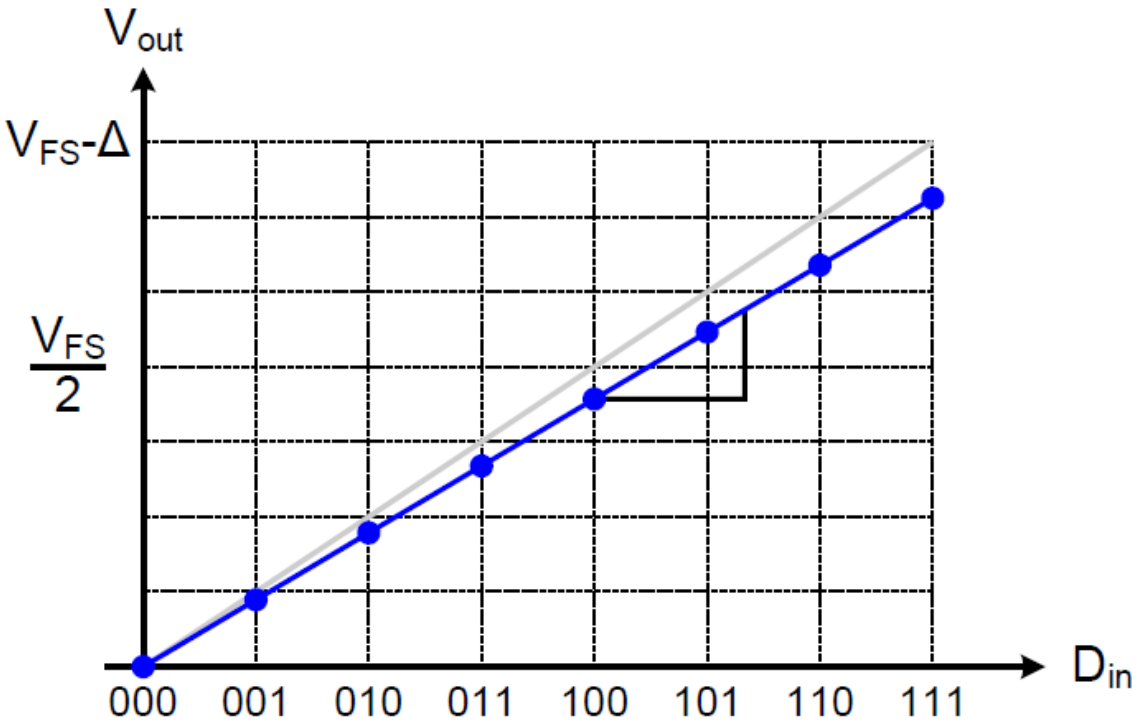
Ideal DAC Transfer Curve



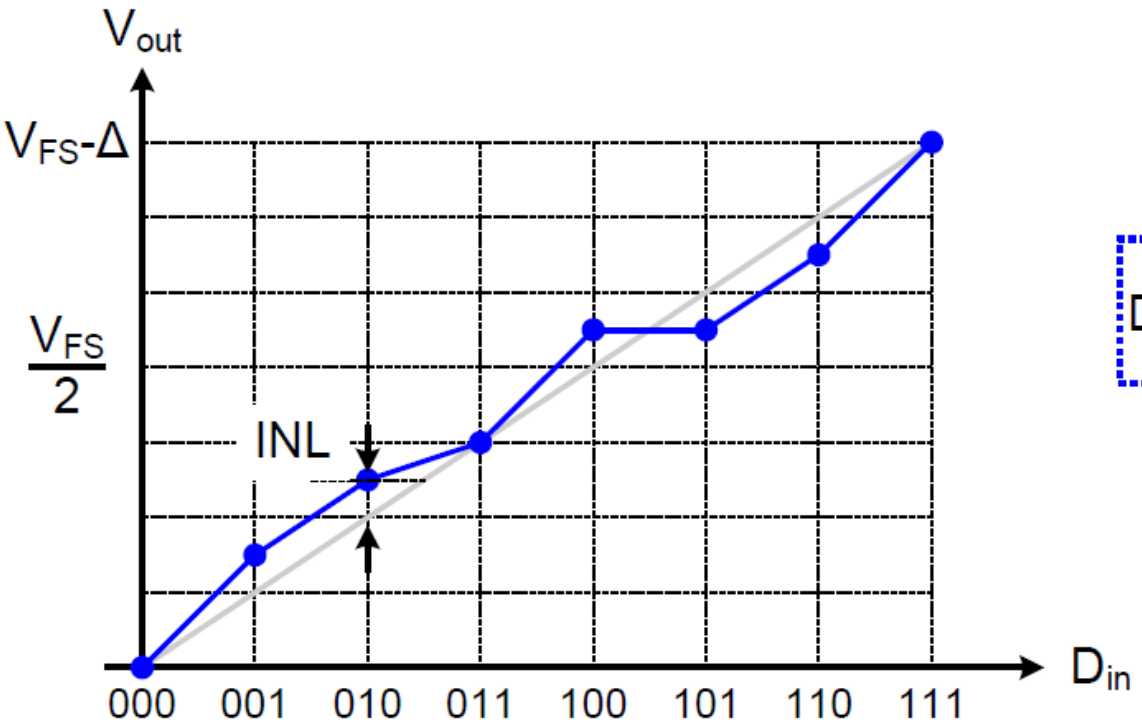
Offset



Gain Error



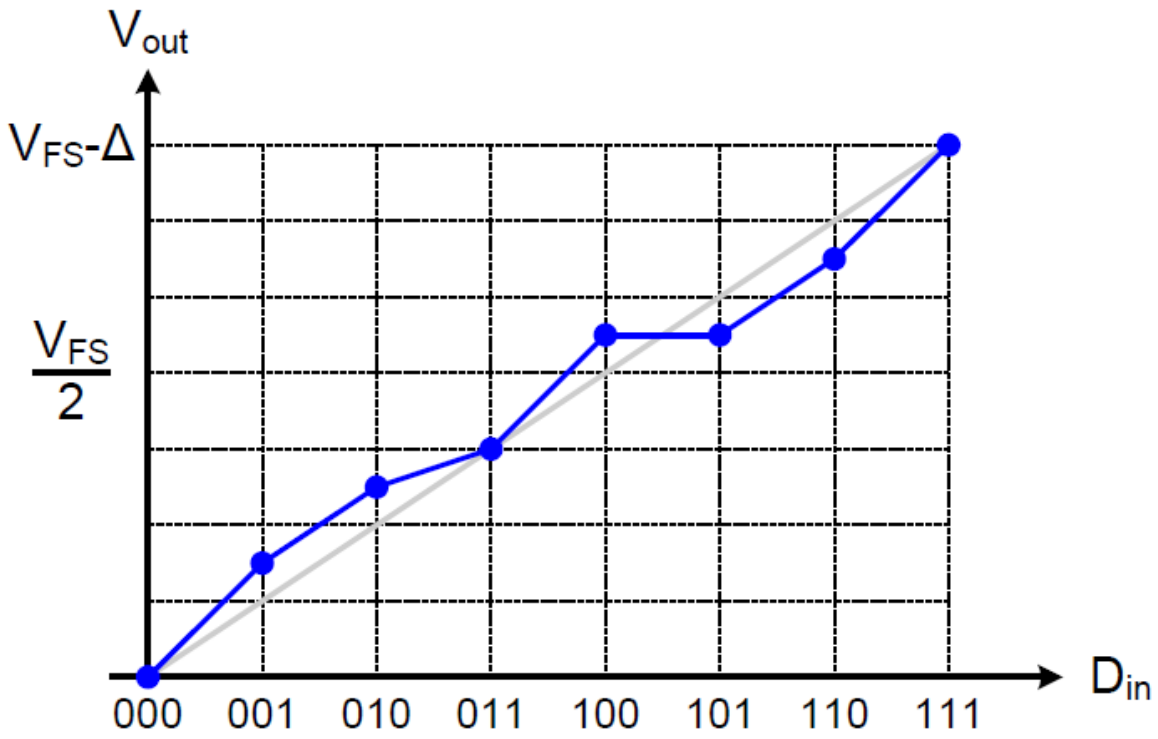
DNL and INL



$$DNL_i = \frac{i^{th}\ \text{Step Size} - \Delta}{\Delta}$$

- DNL = deviation of an output step from 1 LSB (= $\Delta = V_{FS}/2^N$)
- INL = deviation of the output from the ideal transfer curve

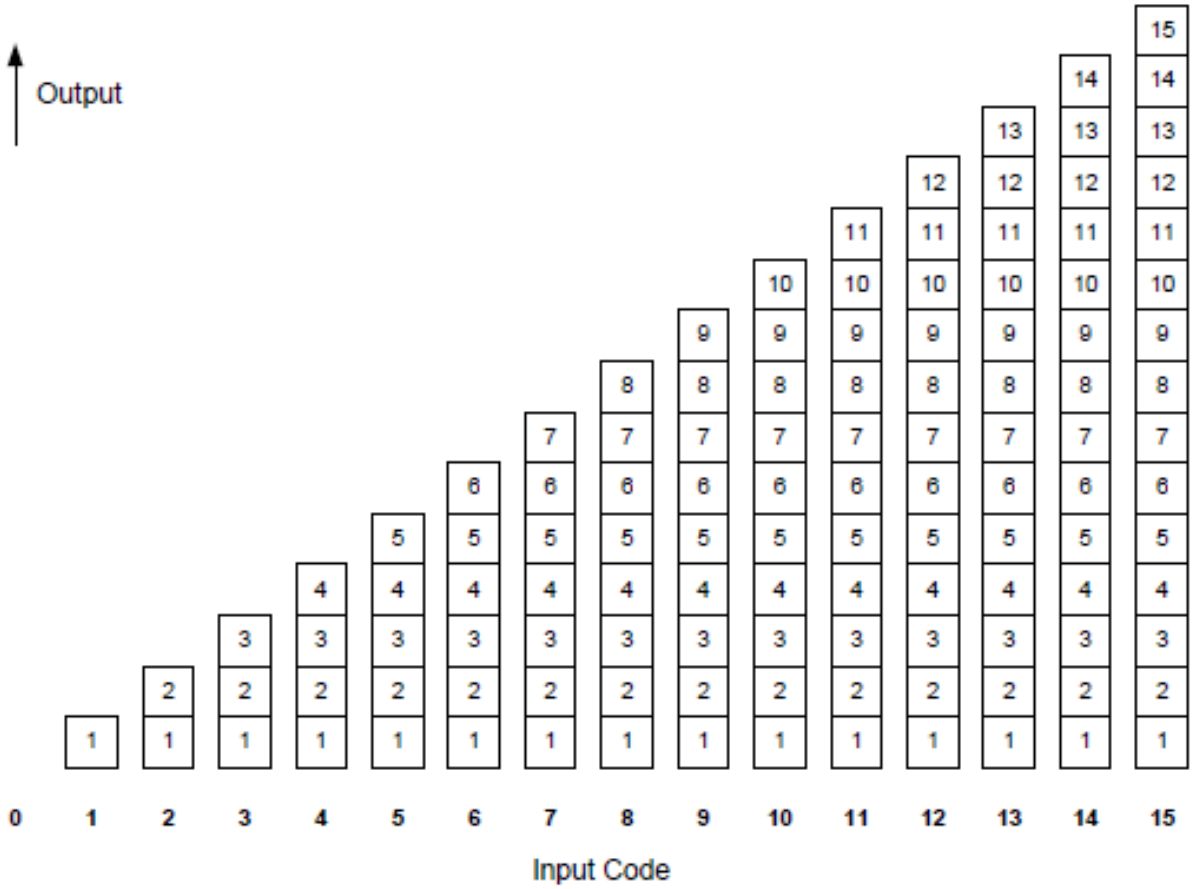
DNL and INL



$$INL_i = \sum_{j=0}^{i} DNL_j$$

INL = cumulative sum of DNL

Unit Element (or Unary) DAC Principle



DNL of Thermometer (or Unary) DAC

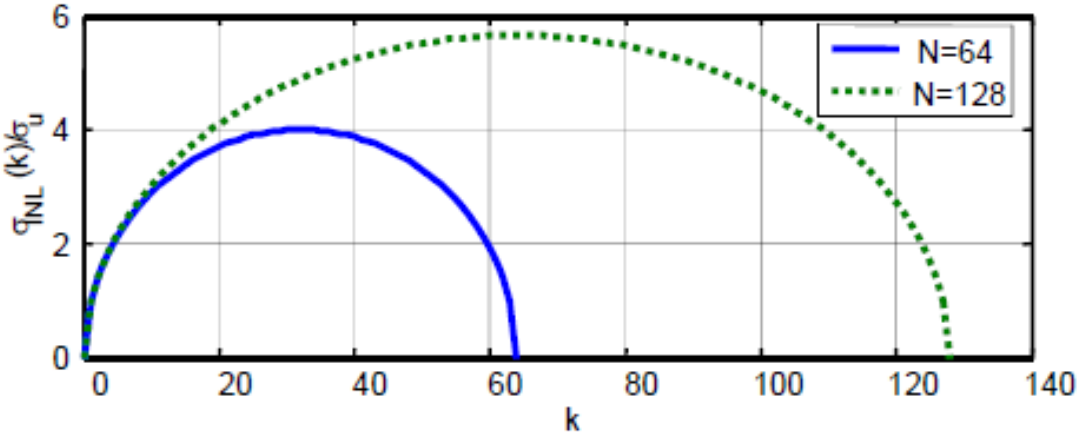
$$DNL(k) = \frac{Step(k) - Step_{avg}}{Step_{avg}} = \frac{I_k - \frac{1}{N}\sum_{j=1}^{N} I_j}{\frac{1}{N}\sum_{j=1}^{N} I_j} \cong \frac{I_k - I}{I} = \frac{\Delta I}{I}$$

$$stdev\left(DNL(k)\right) = stdev\left(\frac{\Delta I}{I}\right) = \sigma_u$$

Standard deviation of DNL for each code is simply equal to relative matching (σ_u) of unit elements

INL

$$INL(k) = \frac{I_{out}(k) - I_{out,uniform}(k)}{Step_{avg}}$$

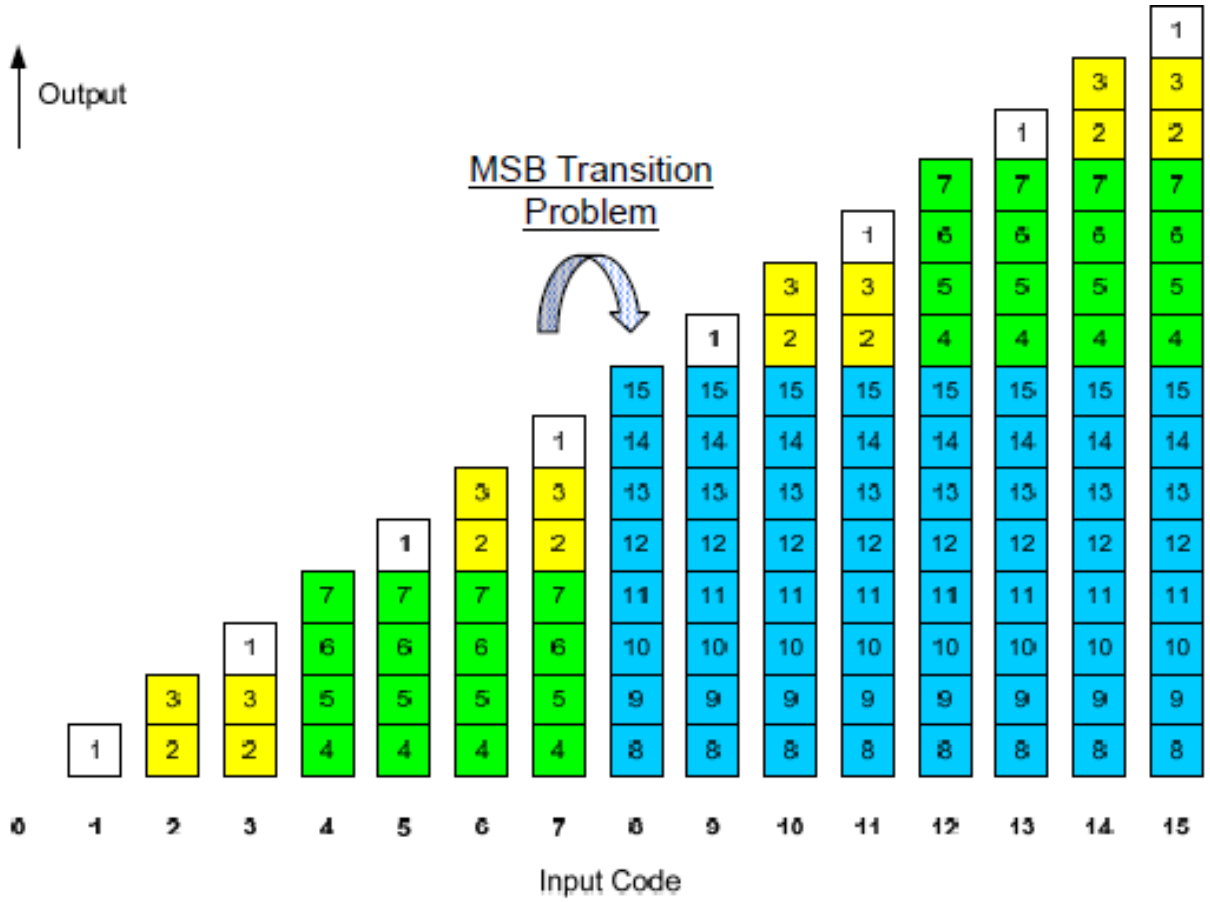


Standard deviation of INL is maximum at mid-scale (k=N/2)

$$\sigma_{INL} \cong \sigma_u \sqrt{\frac{N}{2}\left(1 - \frac{N/2}{N}\right)} = \frac{1}{2}\sigma_u\sqrt{N} \cong \frac{1}{2}\sigma_u\sqrt{2^B}$$

For a more elaborate derivation of this result see
[Kuboki et al., IEEE Trans. Circuits & Systems, 6/1982]

Binary Weighted DAC Principle



DNL/INL of Binary Weighted DAC

INL same as for thermometer DAC

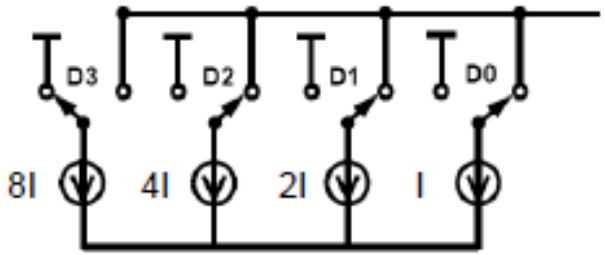
- Why?

DNL is not same for all codes, but depends on transition

Consider worst case: 0111 … → 1000 …

- Turning on MSB and turning off all LSBs

$$\sigma_{DNL}^2 = \underbrace{\left(2^{B-1}-1\right)\sigma_u^2}_{0111\ldots} + \underbrace{\left(2^{B-1}\right)\sigma_u^2}_{1000\ldots} = \left(2^B-1\right)\sigma_u^2$$



Example

- B = 12, σ_u = 1% → σ_{DNL} = 0.64 LSB
- Much worse than thermometer DAC