EE223 Analog Integrated Circuits
Fall 2018

Lecture 7: Common Source Amplifiers

Prof. Sang-Soo Lee
sang-soo.lee@sjsu.edu
ENG-259

Homework

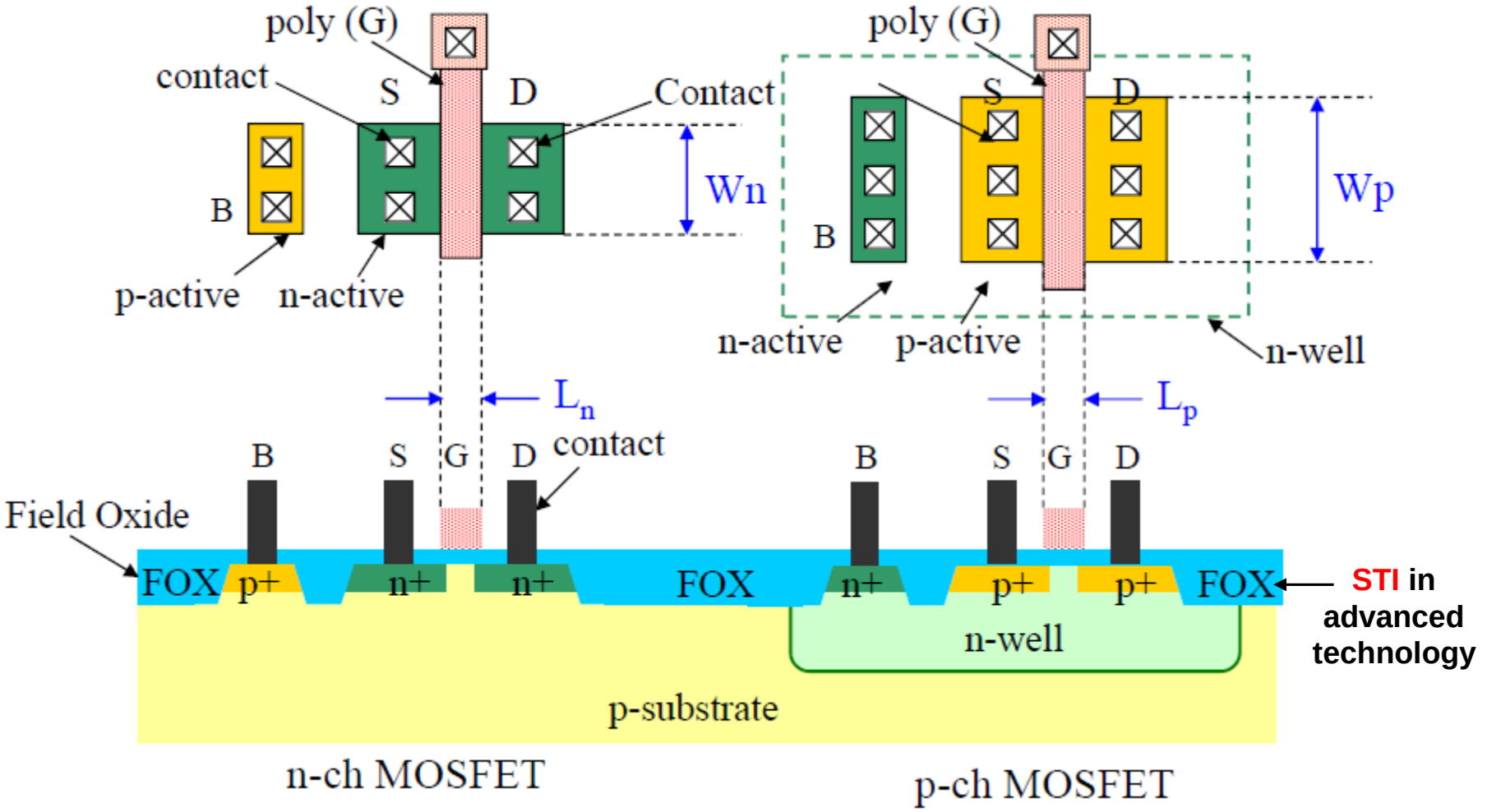
All homework problems should be done individually
and submitted by 6PM on the due date.

Submission: Email to sang-soo.lee@sjsu.edu
File name convention: EE223HW#2_Lastname_Firstname.pdf
Send only one pdf file. No zip file please!

Each HW will be 5 points.

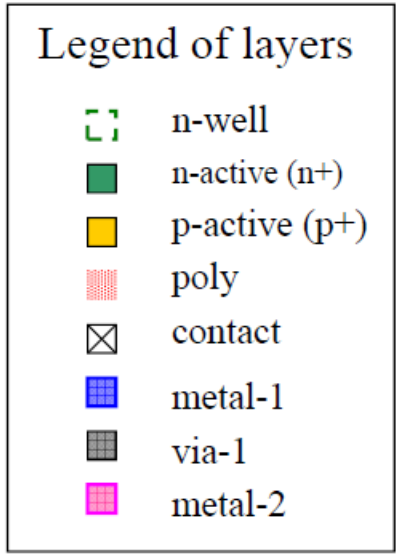
- HW#1 – Cadence exercise due Sept. 12, Wednesday
- HW#2 – Single Stage Amplifier due Oct. 1, Monday
- HW#3 – Beta Multiplier with Startup circuit
- HW#4 – OTA
- HW#5 – Two stage opamp

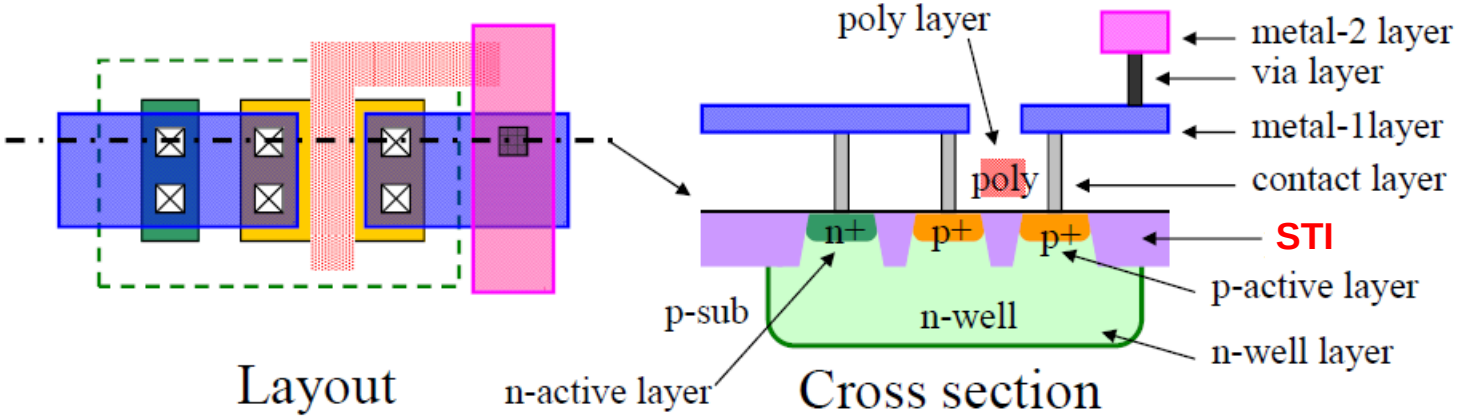
MOS Layout Example



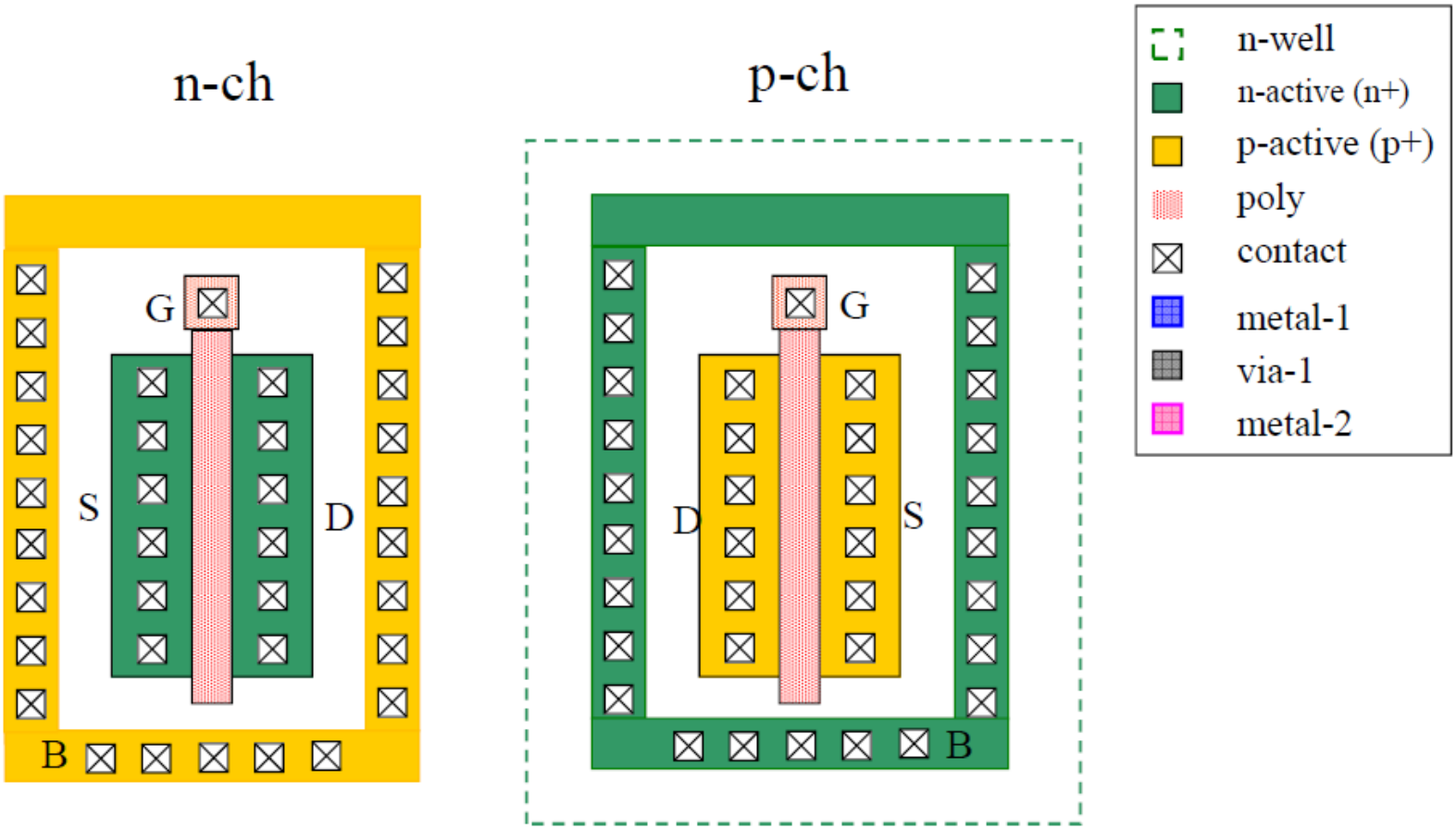
Mask Layers

- Layer numbers are assigned to Well, Active, Poly, Contact, Metal, Via, Silicide Protect, and Dummy, respectively.
- Some layer is automatically generated from the pattern on the drawn layer.
  - ex. FOX and GOX is generated from the pattern on the active layer.

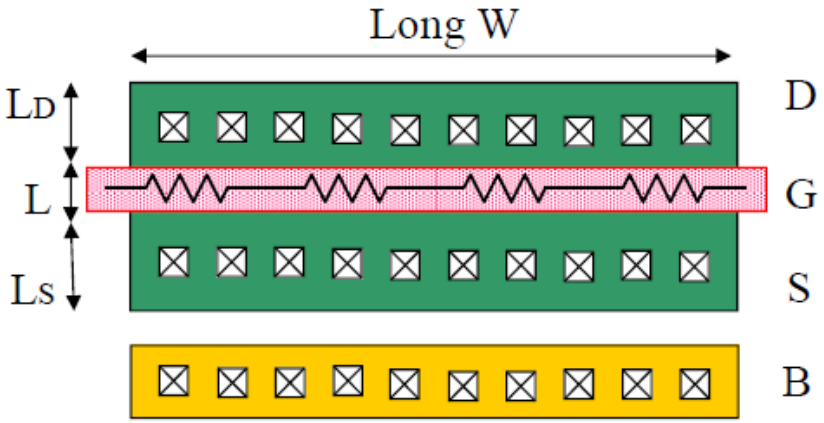


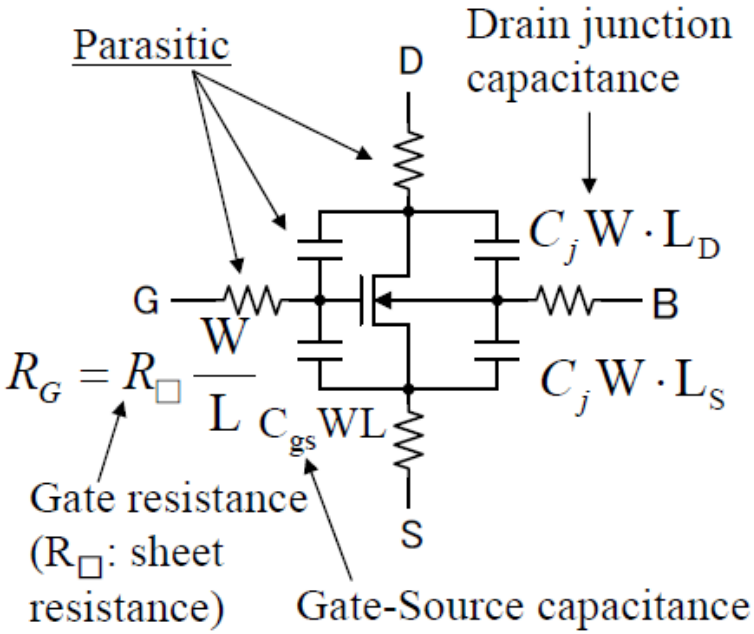


MOS Layout Example



Gate Resistance in MOS Layout





- Long W: large time constant of gate poly-Si
- Long W: large thermal noise of gate poly-Si
- Long LD, LS: large parasitic capacitance and resistance of drain/source area
- Few number of contact: Shift or fluctuation of substrate potential

How can you design the MOSFET with larger W?

MOS Layout Example Using Fingers

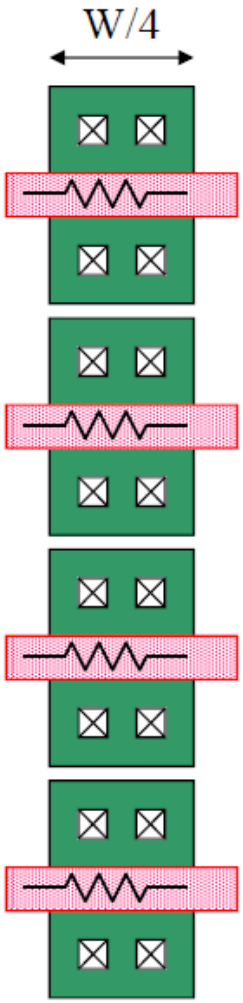
MOFET should be sectioned to reduce the gate resistance.

$$R_{\square}\frac{W}{L} << \frac{1}{g_m}$$

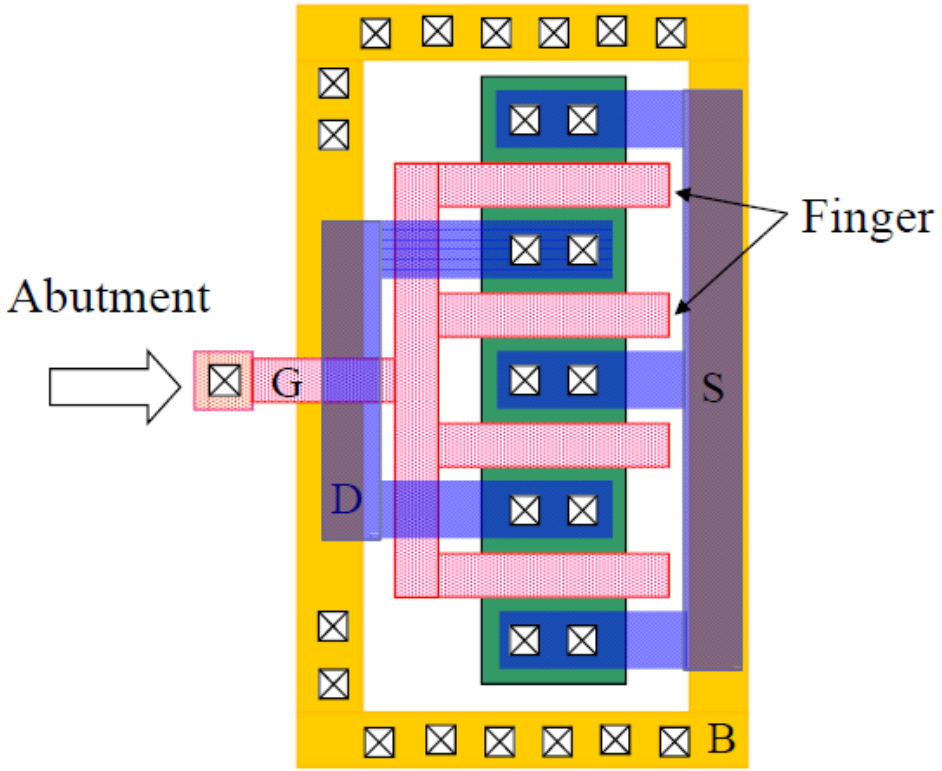
g_m: trans-conductance

$$g_m = y_{21} = \frac{dI_{ds}}{dV_{gs}}$$

This condition is often met in the case of W/L < 20. W/L < 10 is recommended.

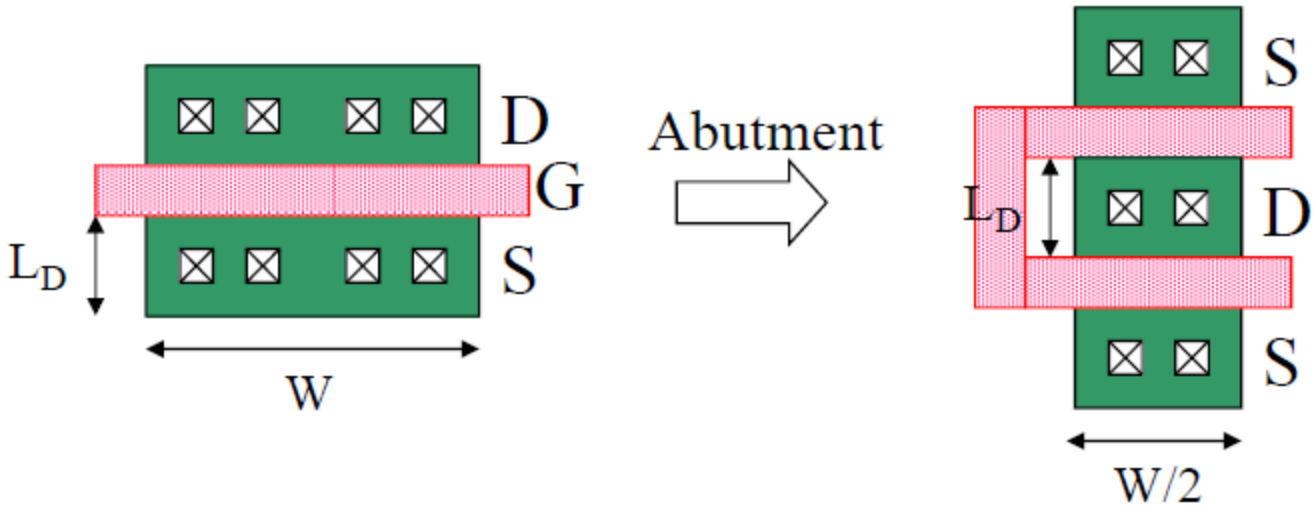


High-performance MOSFET array



Multiply = 4 (W/4 x 4)

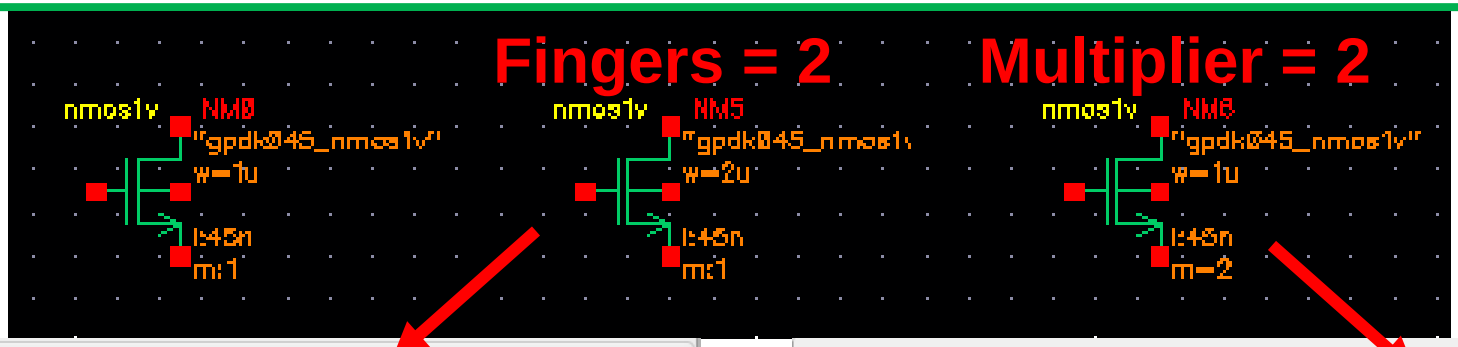
Fingers



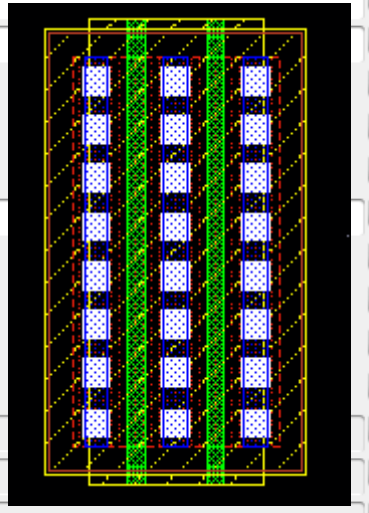
$$C_{DB} = C_j W L_D \quad > \quad C_{DB} = C_j \frac{W}{2} L_D$$

C_j = Capacitance of drain bottom pn junction per area (F/m^2)

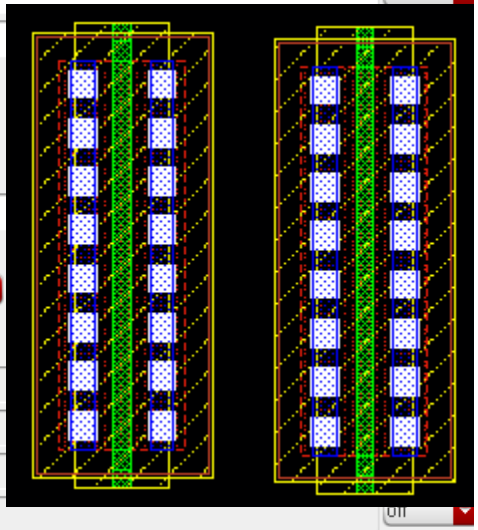
Fingers vs. Multiplier



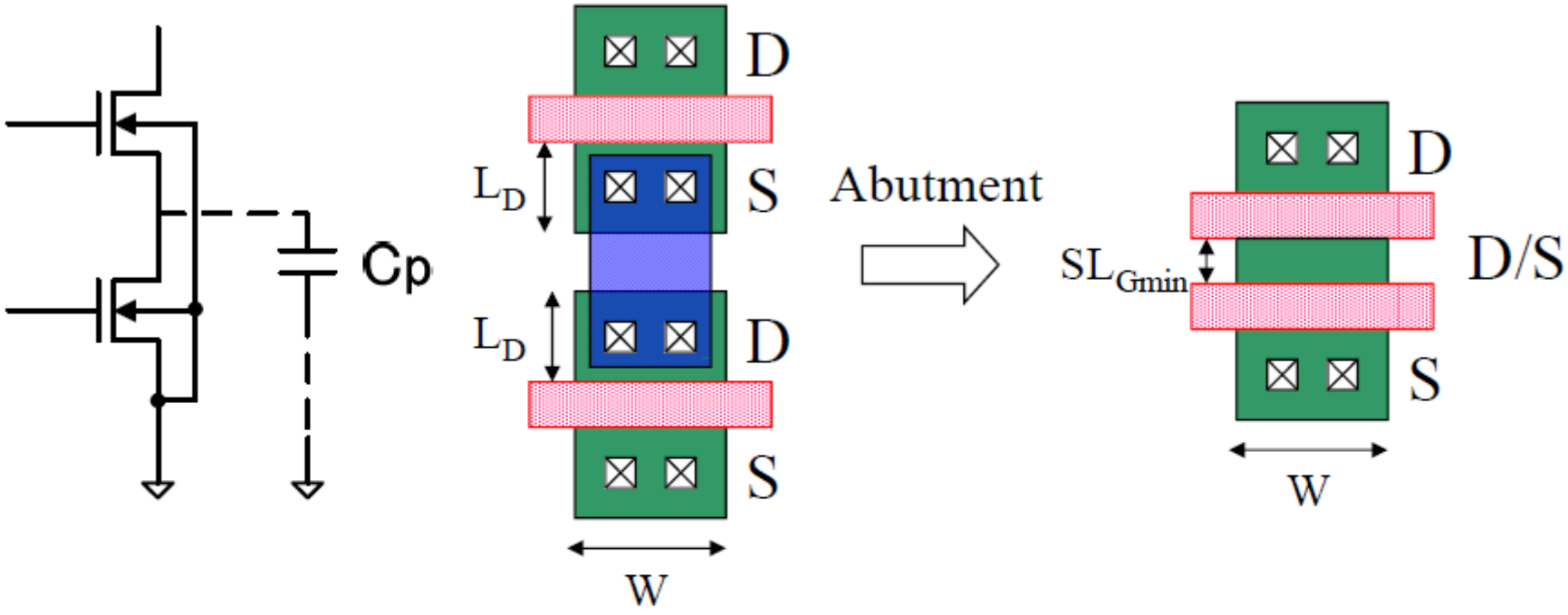
CDF Parameter	Value	Display
Model Name	gpdk045_nmos1v	off
Multiplier	1	off
Length	45n M	off
Total Width	2u M	off
Finger Width	1u M	off
Fingers	2	off
Threshold	120n M	off
Apply Threshold		off
Gate Connection	None	off
Use DFM Rules	Minimum	off
S/D Metal Width	60n M	off
S/D Connection	None	off
Switch S/D		off
Bodytie Type	None	off
Edit Area & Perim		off
Drain diffusion area	160f	off
Source diffusion area	280f	off
Drain diffusion periphery	2.32u M	off
Source diffusion periphery	4.56u M	off
Drain diffusion res squares	40m	off



CDF Parameter	Value	Display
Model Name	gpdk045_nmos1v	off
Multiplier	2	off
Length	45n M	off
Total Width	1u M	off
Finger Width	1u M	off
Fingers	1	off
Threshold	120n M	off
Apply Threshold		off
Gate Connection	None	off
Use DFM Rules	Minimum	off
S/D Metal Width	60n M	off
Switch S/D		off
Bodytie Type	None	off
Edit Area & Perim		off
Drain diffusion area	140f	off
Source diffusion area	140f	off
Drain diffusion periphery	2.28u M	off
Source diffusion periphery	2.28u M	off
Drain diffusion res squares	140m	off
Source diffusion res squares	140m	off



Abutment

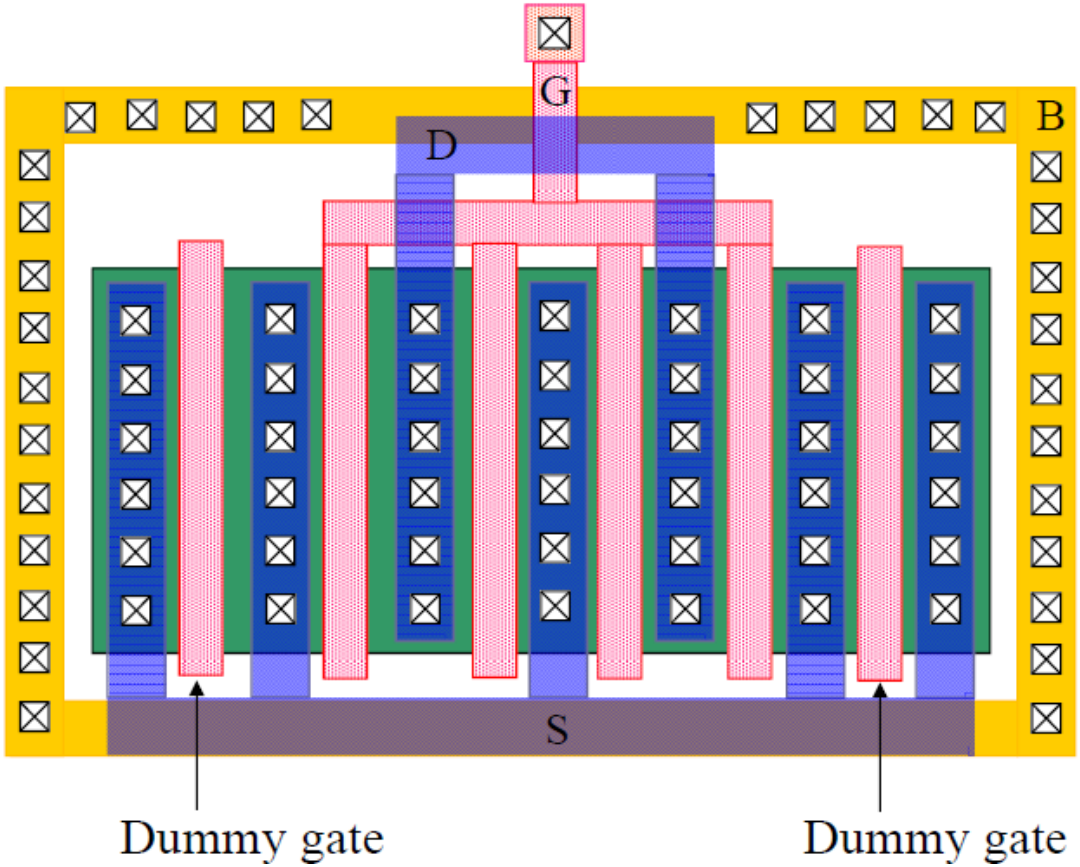


$$C_p = 2C_jWL_D \quad > \quad C_p = C_jWSL_{G\min}$$

C_j = Capacitance of drain bottom pn junction per area (F/m^2)
SL_{Gmin} = minimum gate spacing

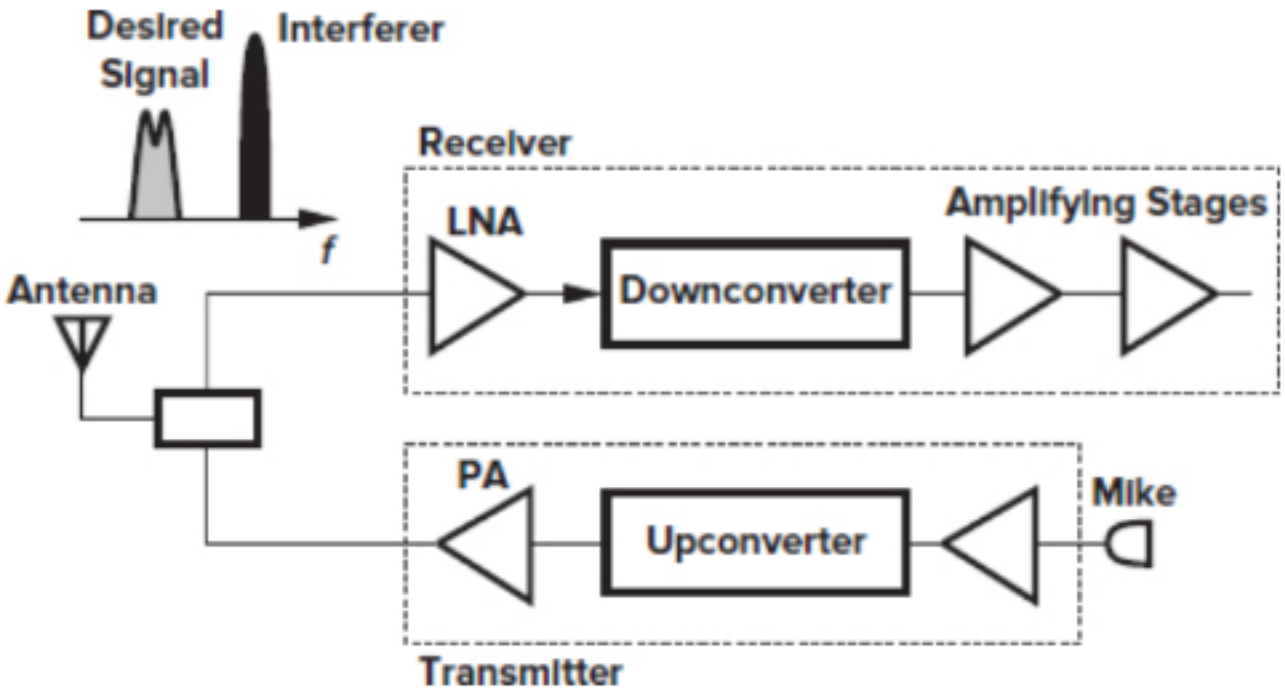
Dummy Pattern

The dummy pattern may be formed to reduce the production tolerance.

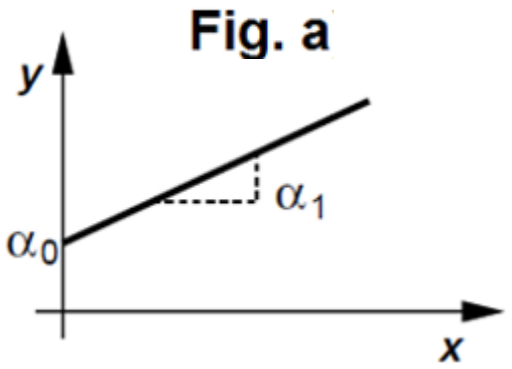


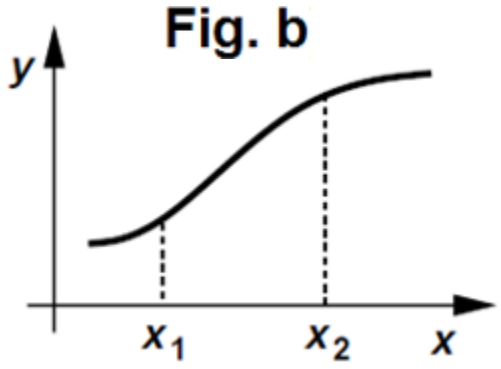
Amplifier Applications

Wireless Communication



Ideal vs Non-ideal Amplifier





- **Ideal amplifier (Fig. a)**

$$y(t) = \alpha_0 + \alpha_1 x(t)$$

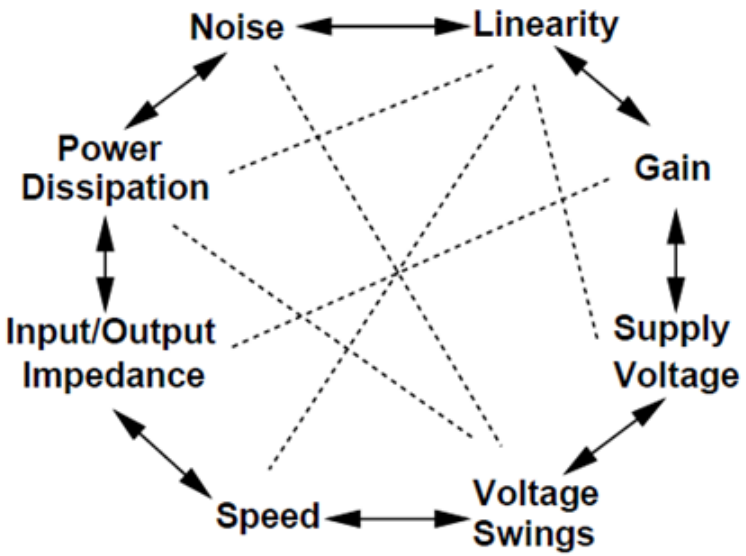
  - **Large-signal characteristic is a straight line**
  - **α_1 is the "gain", α_0 is the "dc bias"**

- **Nonlinear amplifier (Fig. b)**

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t)$$

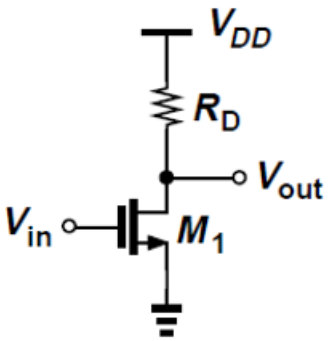
  - **Large signal excursions around bias point**
  - **Varying "gain", approximated by polynomial**
  - **Causes distortion of signal of interest**

Analog Design Tradeoff



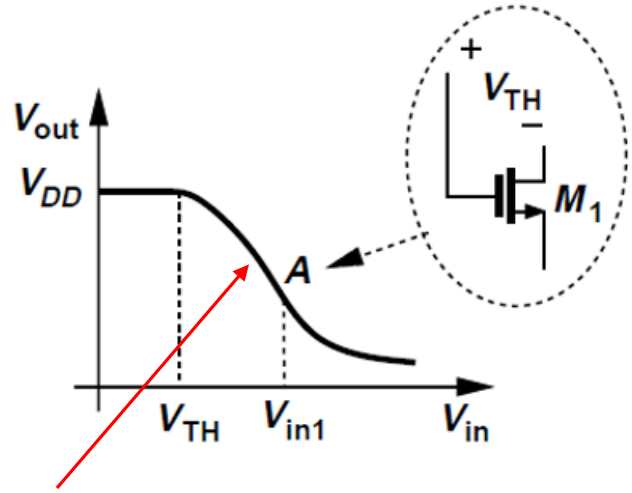
- Along with gain and speed, other parameters also important for amplifiers
- Input and output impedances decide interaction with preceding and subsequent stages
- Performance parameters trade with each other
  - Multi-dimensional optimization problem

Common Source Stage with Resistive Load



- Very high input impedance at low frequencies
- For $V_{in} < V_{TH}$, M_1 is off and $V_{out} = V_{DD}$

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2$$



- When $V_{in} > V_{TH}$, M_1 turns on in saturation region, V_{out} falls
- When $V_{in} > V_{in1}$, M_1 enters triode region
- At point A, $V_{out} = V_{in1} - V_{TH}$

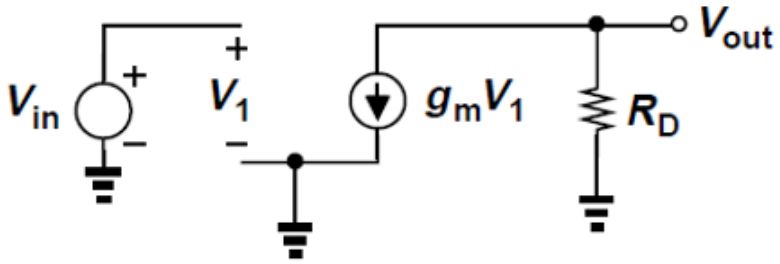
$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2$$

Slope = small-signal gain

Common Source Stage with Resistive Load

$$\begin{aligned} A_v &= \frac{\partial V_{out}}{\partial V_{in}} \\ &= -R_D \mu_n C_{ox} \frac{W}{L}(V_{in} - V_{TH}) \\ &= -g_m R_D. \end{aligned}$$

- Taking derivative of I_D equation in saturation region, small-signal gain is obtained



- Same result is obtained from small-signal equivalent circuit

$$V_{out} = -g_m V_1 R_D = -g_m V_{in} R_D$$

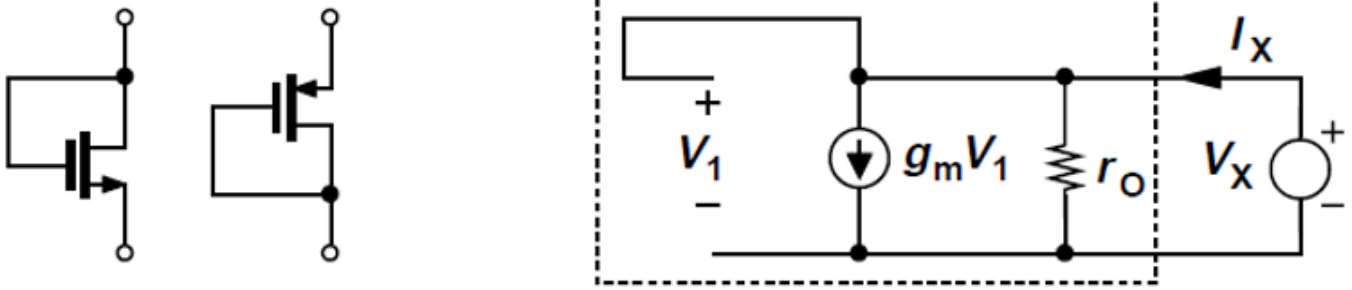
- g_m and A_v vary for large input signal swings according to

$$g_m = \mu_n C_{ox}(W/L)(V_{GS} - V_{TH})$$

- This causes non-linearity

Diode-Connected MOSFET

- A MOSFET can operate as a small-signal resistor if its gate and drain are shorted, called a "diode-connected" device
- Transistor always operates in saturation

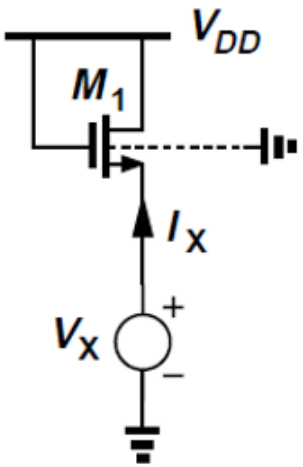


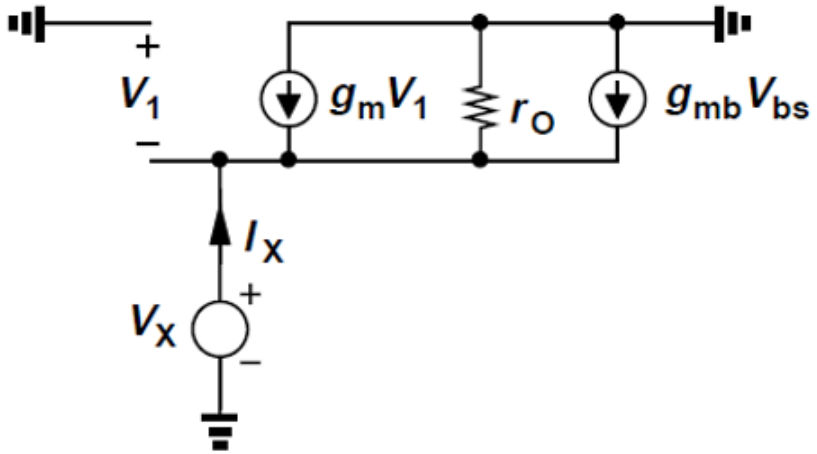
- Impedance of the device can be found from small-signal equivalent model

$$V_1 = V_X \qquad I_X = V_X/r_O + g_m V_X$$

$$V_X/I_X = (1/g_m)\|r_O \approx 1/g_m$$

Diode-Connected MOSFET





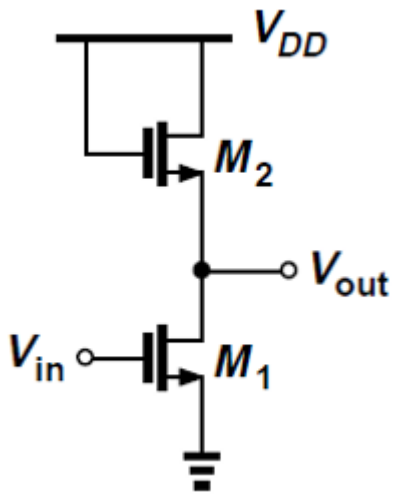
- **Including body-effect, impedance "looking into" the source terminal of diode-connected device is found as**

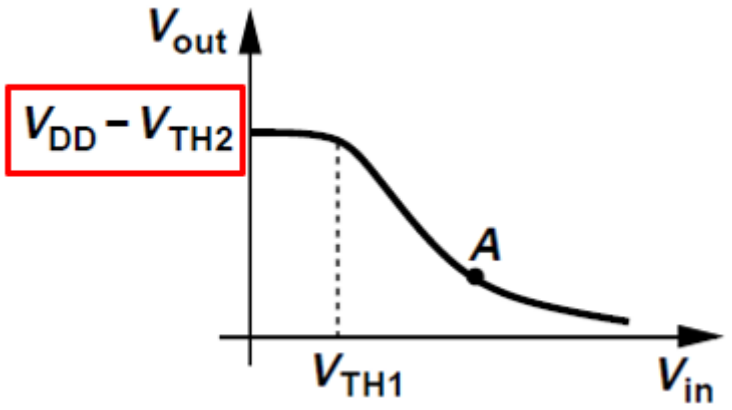
$$V_1 = -V_X \qquad V_{bs} = -V_X$$

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X$$

$$\begin{aligned} \frac{V_X}{I_X} &= \frac{1}{g_m + g_{mb} + r_O^{-1}} \\ &= \frac{1}{g_m + g_{mb}} \| r_O \\ &\approx \frac{1}{g_m + g_{mb}}. \end{aligned}$$

CS Amp with Diode-Connected Load





- For $V_{in} < V_{TH1}$, $V_{out} = V_{DD} - V_{TH2}$
- When $V_{in} > V_{TH1}$, previous large-signal analysis predicts that V_{out} approximately follows a single line
- As V_{in} exceeds $V_{out} + V_{TH1}$ (to the right of point A), M_1 enters the triode region and the characteristic becomes nonlinear.