EE223 Analog Integrated Circuits
Fall 2018

Lecture 14: CMOS Fabrication

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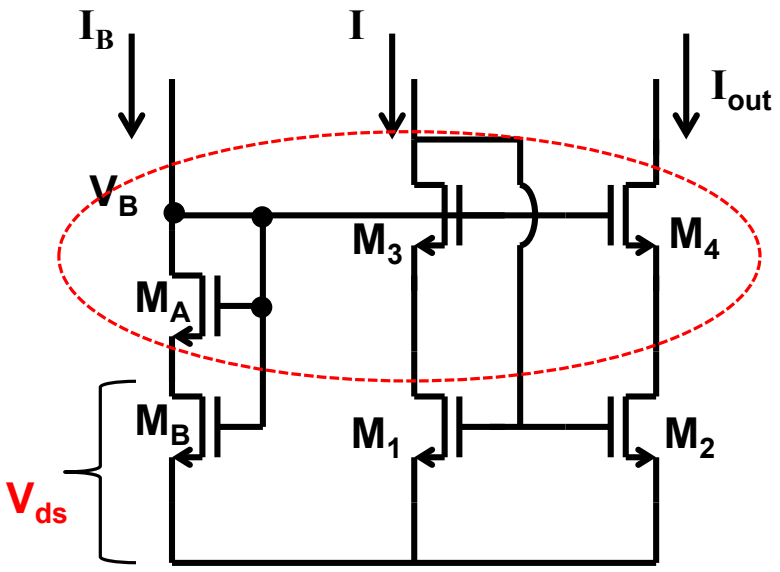
ENG-259

Midterm Exam

- ❑ Oct. 17, Wednesday 6 PM
- ❑ One-page Aid sheet on Front side only allowed
- ❑ Bring two copies of your Aid sheet
  - ✓ Keep one copy yourself during the exam
  - ✓ Write your name and submit another copy for extra 5 points
- ❑ Bring a Calculator

Biasing High Swing Cascode Current Mirror

Practical approach for cascode biasing
→ Will use this biasing scheme extensively

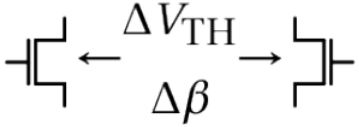


- M_A in Saturation
- M_B in Triode
- $(W/L)_A = (W/L)_3 = (W/L)_4$
- $(W/L)_B$ with large L
- Example:
  - $(W/L)_{A,3,4} = 5/0.18$
  - $(W/L)_B = 5/5$
  - Adjust L of M_B in Simulation to get the Vds you want

If you make the current densities of M_A, M_3 and M_4 are equal, V_{ds} of M_B will be copied over to V_{ds} of M_1 and M_2

MOSFET Mismatch

- Mismatch between two identically drawn transistors.
  - Vth mismatch
  - Beta mismatch



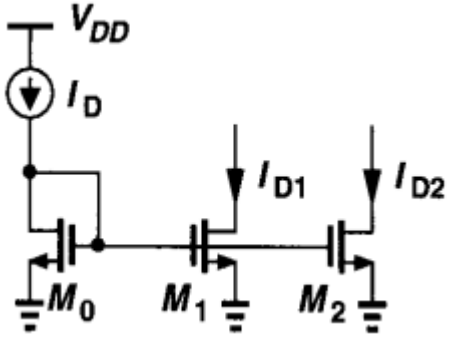
$$I_D = \frac{\mu_n C_{\text{ox}}}{2}\frac{W}{L}(V_{\text{GS}} - V_{\text{TH}})^2 = \frac{\beta}{2}(V_{\text{GS}} - V_{\text{TH}})^2$$

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}}$$

$$\Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}},$$

$$\frac{A_{\text{VTH}}}{t_{\text{ox}}} \approx 1\sim2\ \frac{\text{mV}\cdot\mu\text{m}}{\text{nm}}$$

Current Mirror Mismatch



$$y = f(x_1, x_2, \ldots)$$

$$\Delta y = \frac{\partial f}{\partial x_1}\Delta x_1 + \frac{\partial f}{\partial x_2}\Delta x_2 + \cdots$$

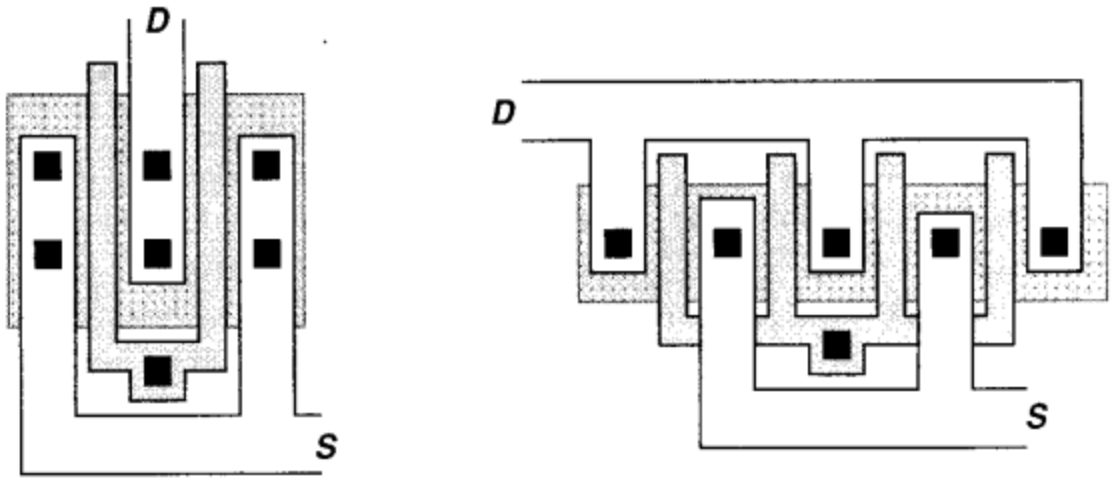
$$I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

$$\Delta I_D = \frac{\partial I_D}{\partial (W/L)}\Delta\left(\frac{W}{L}\right) + \frac{\partial I_D}{\partial (V_{GS} - V_{TH})}\Delta(V_{GS} - V_{TH})$$

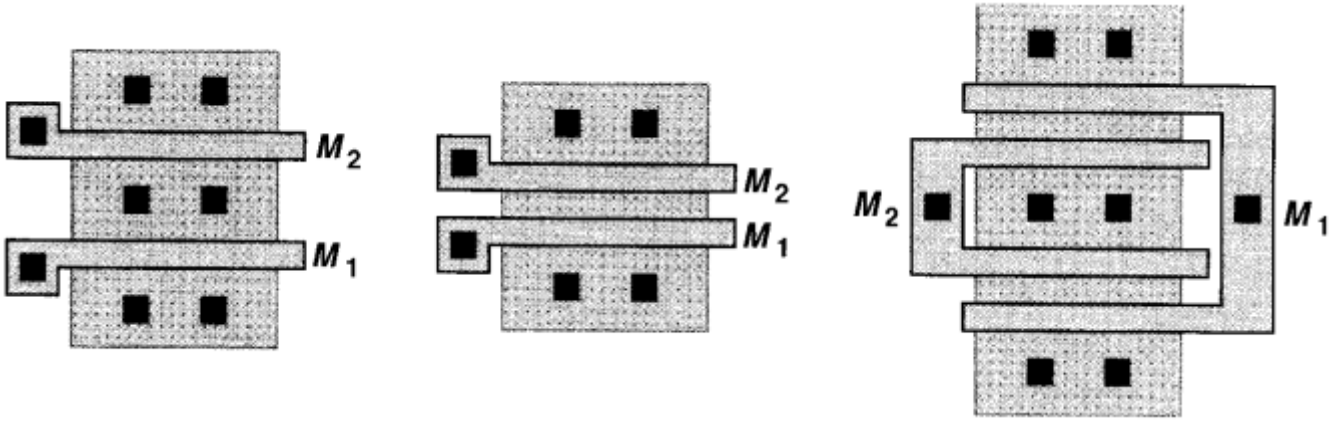
$$\Delta I_D = \frac{1}{2}\mu_n C_{ox}(V_{GS} - V_{TH})^2 \Delta\left(\frac{W}{L}\right) - \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})\Delta V_{TH}$$

$$\boxed{\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{W/L} - 2\frac{\Delta V_{TH}}{V_{GS} - V_{TH}}}$$

Layout of Transistors with Multi Fingers

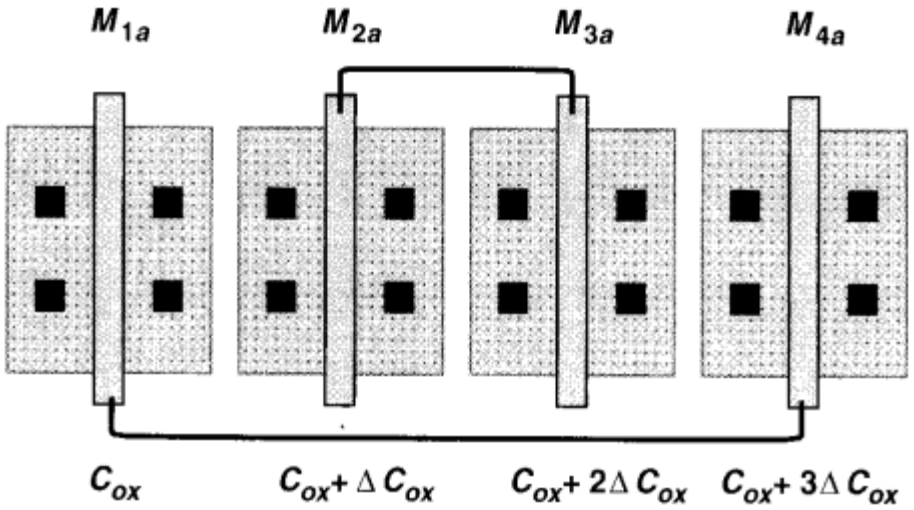


Layout of Cascode Devices



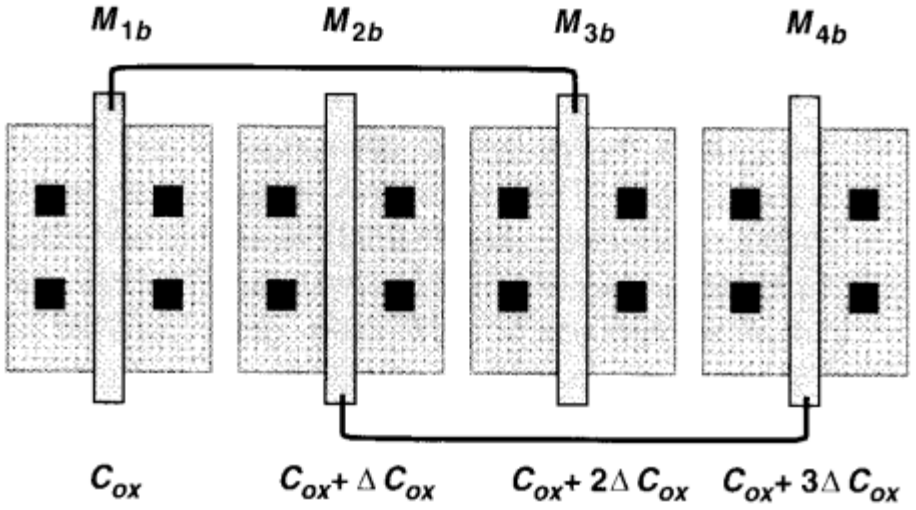
Layout of Current Mirrors

ABBA



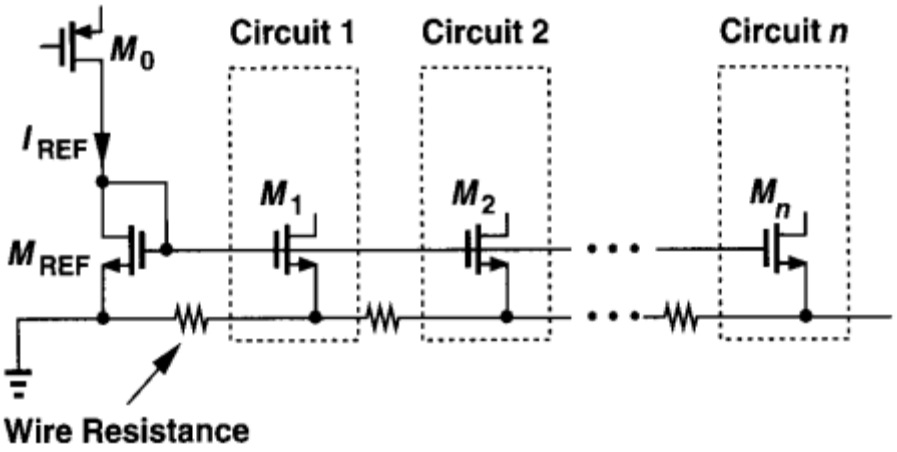
(a)

ABAB

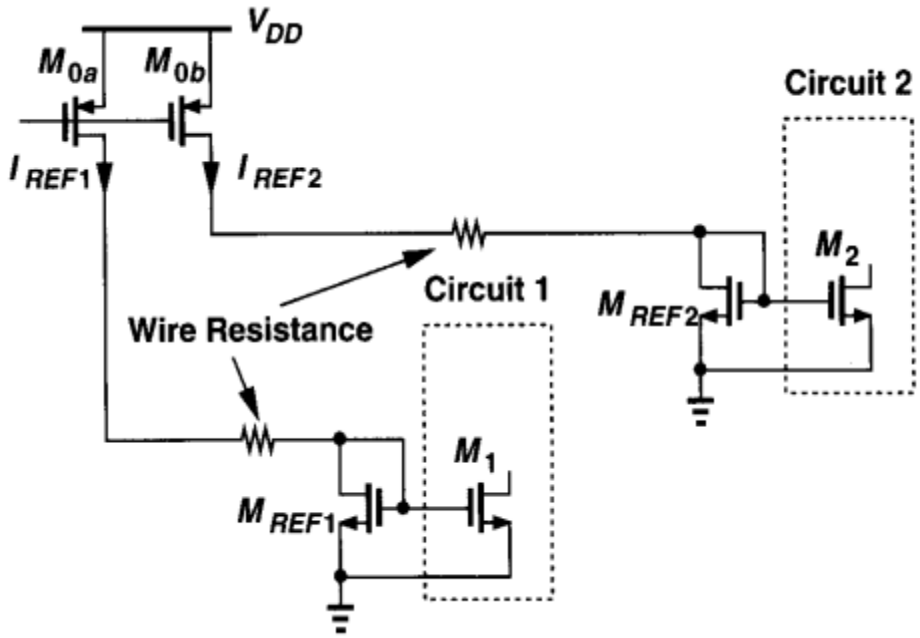


(b)

Reference Distribution in Voltage Domain



Reference Distribution in Current Domain

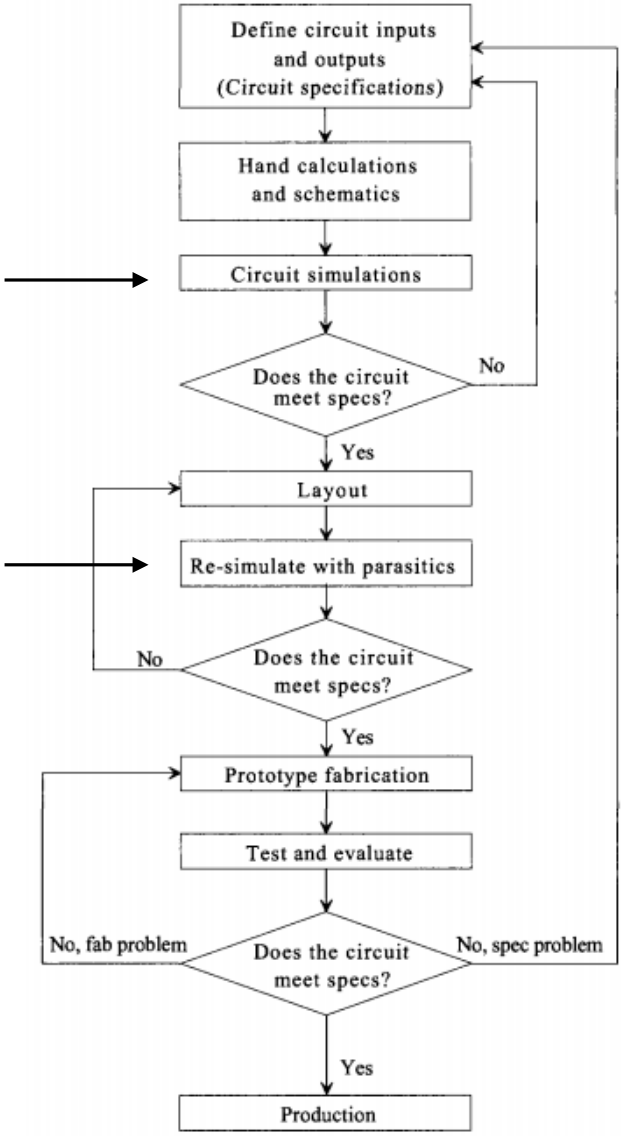


- **CMOS Fabrication**
- **Variability**
- **Analog Layout**
- **Matching**

CMOS IC Design Flow

Schematic Sim
Or Pre-layout Sim
Using Sprectre

Post-layout Sim
Using Sprectre
Including parasitics



Specification

Schematic

Layout

Fabrication

Test

TCAD & ECAD

- Technology Computer Aided Design (TCAD)
  - ✓ Electronic Design Automation (EDA) that models semiconductor fabrication and semiconductor device operation
  - ✓ Sentaurus – Process and Device Simulation Tool from Synopsys

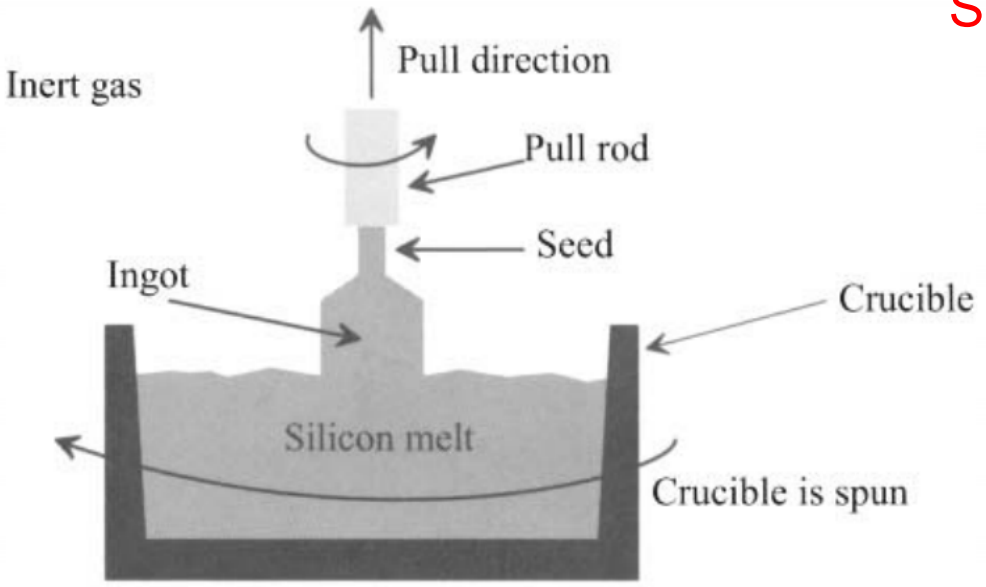
- Electronic Computer Aided Design (ECAD)
  - Circuit simulation
    - Spectre – Cadence Virtuoso
    - HSPICE – Synopsys
  - Layout
    - Custom
    - Place & Route (P&R)
  - Verification
    - DRC
    - LVS
  - LPE (Layout Parasitic Extraction)

CMOS Fabrication

- Unit Process
  - Thermal Oxidation
  - Doping
  - Photolithography
  - Thin Film Removal
  - Thin Film Deposition
- Process Integration
  - FEOL (frontend-of-the-line)
  - BEOL (backend-of-the-line)

Wafer Manufacture

Czochralski (CZ) process

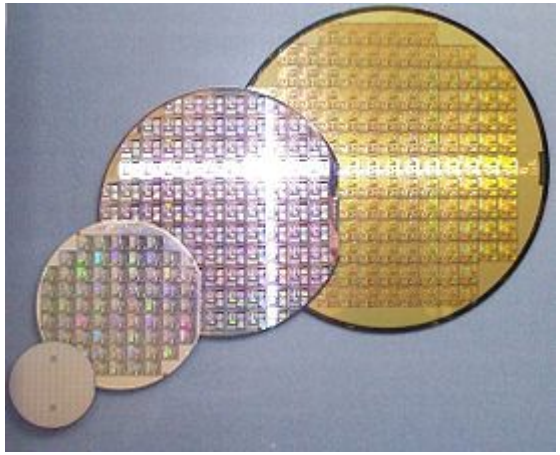


Silicon Ingot

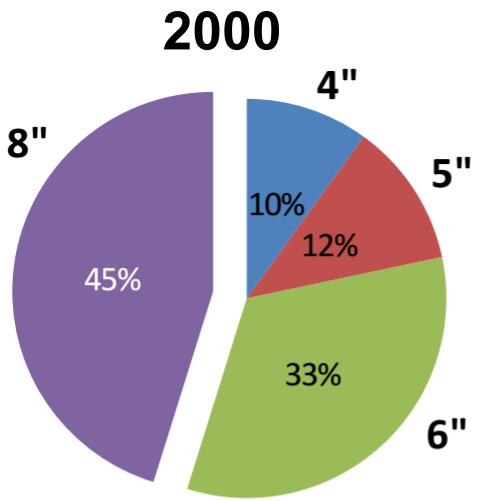
200mm Silicon Ingot

Wafer

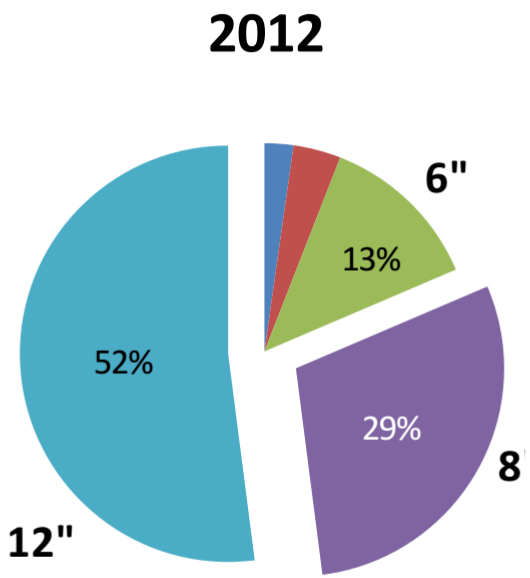
Diameter 100 ~ 300mm
Thickness ~ 1mm



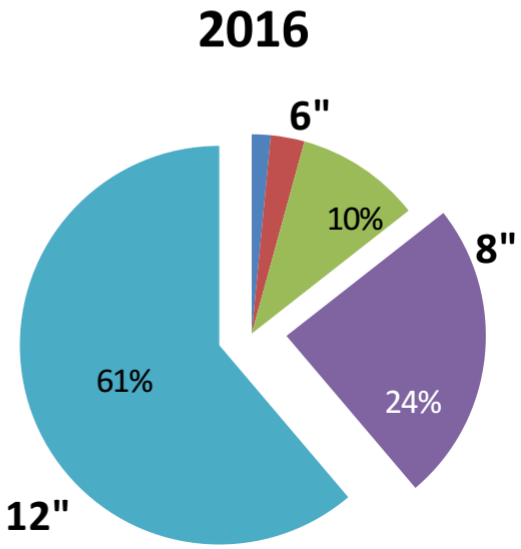
Wafer Size Trends



Source: Gartner (March 2012)



Source: Gartner (March 2012)



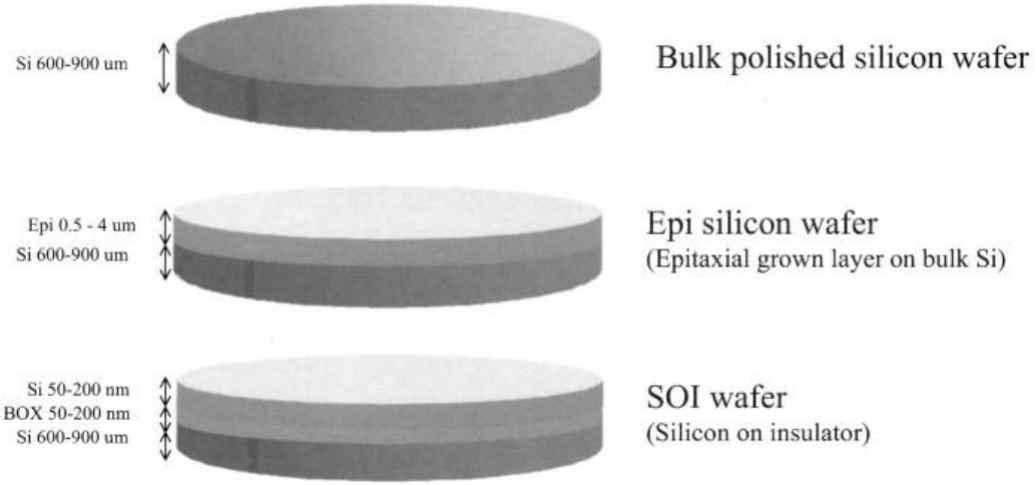
Source: Gartner (March 2012)

- Larger wafers = more die per wafer = lower cost per die
- 300mm (12”) wafers yield more than twice as many die for the same product as a 200mm (8”) wafer

Wafer Types

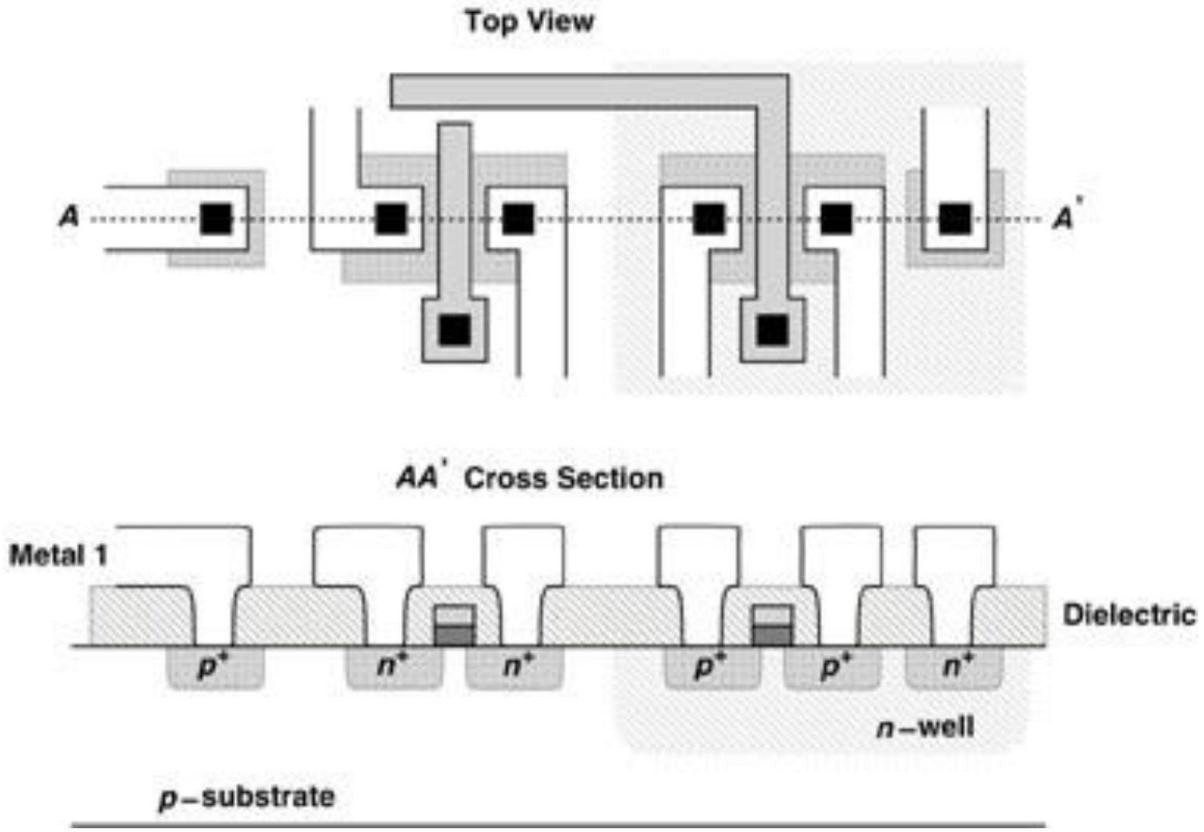
Three types of wafer

- Bulk : Resistivity ~ 10-20 Ω·cm
- Epi : Resistivity ~ 5-20 Ω·cm p- epi on top of 0.01 Ω·cm p++
  Epi thickness : 2~20 μm
  Help preventing latchup
- SOI



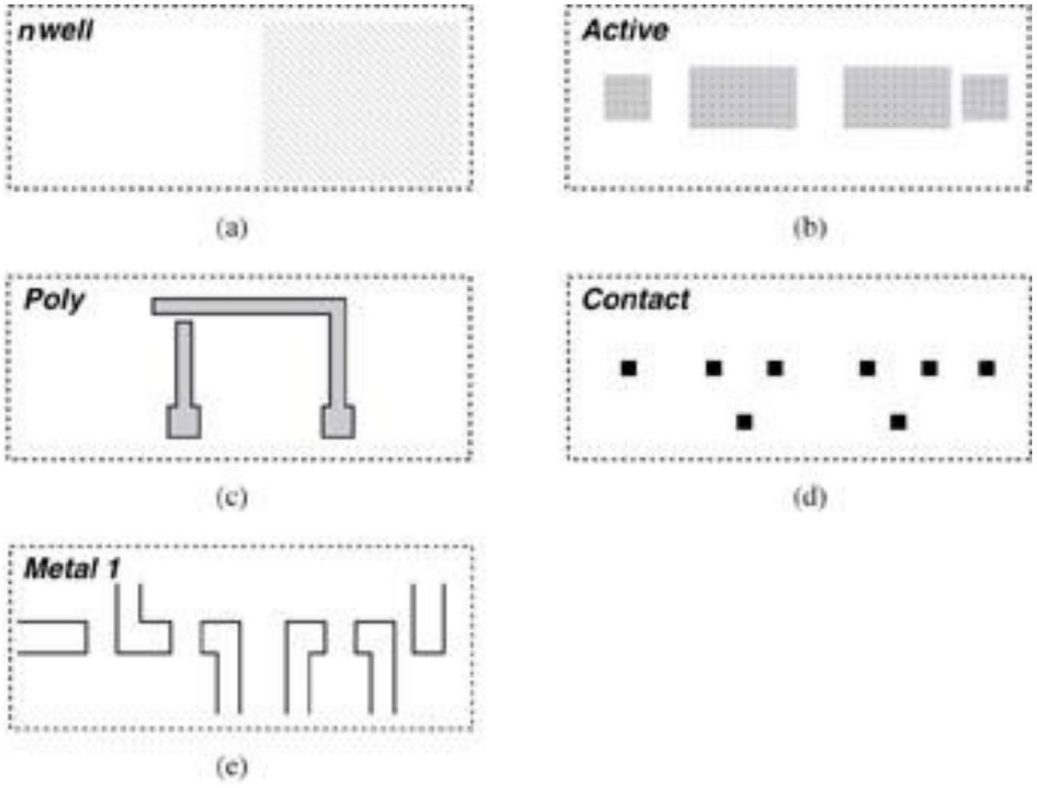
CMOS Structure

- Top and side views of a typical CMOS process

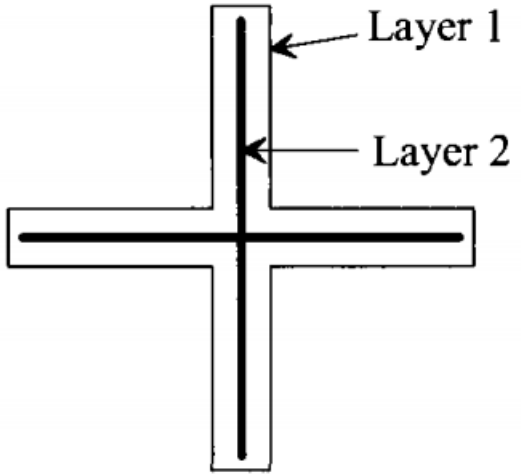


Mask

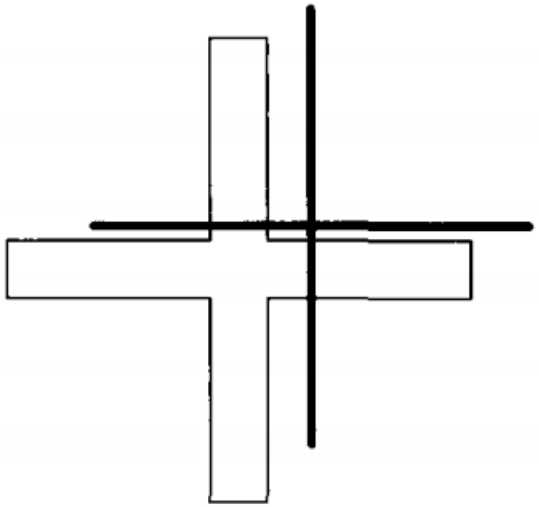
- Different layers comprising CMOS transistors



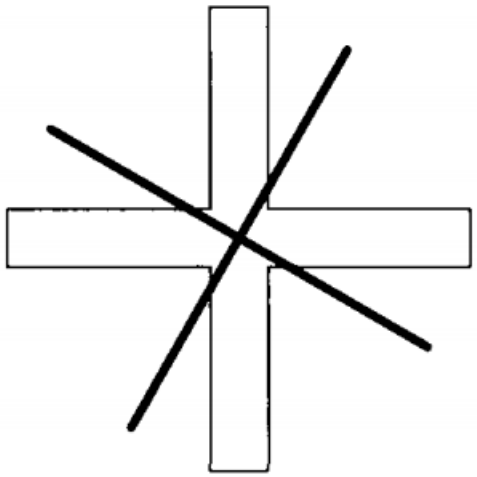
Aligning Masks



(a) No registration error

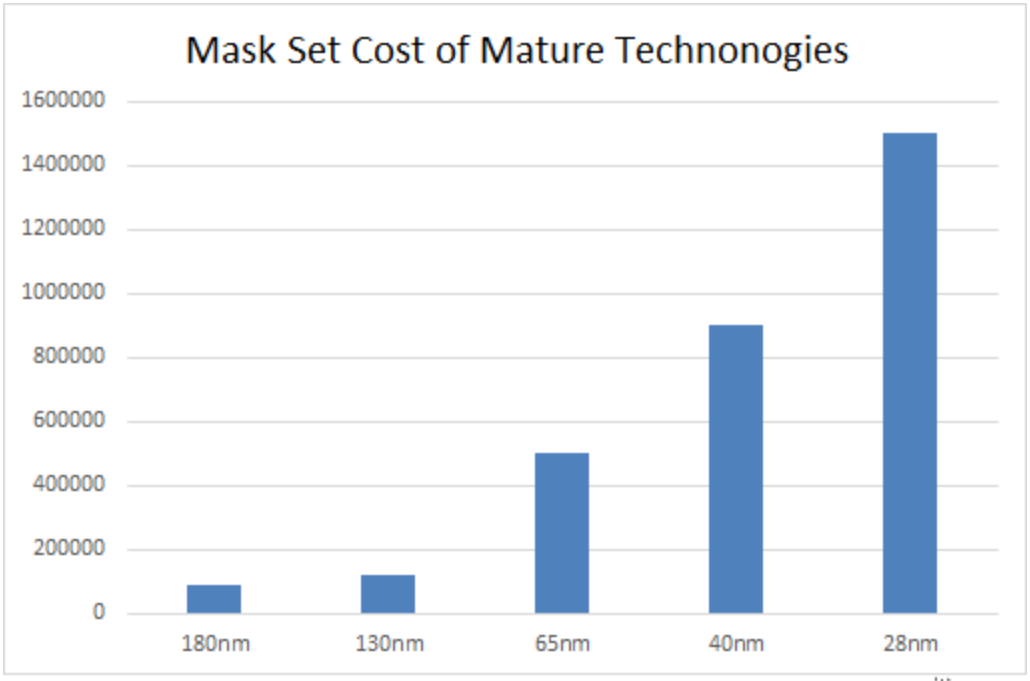


(b) x-y registration error



(c) z-rotation registration error.

Mask Set Cost

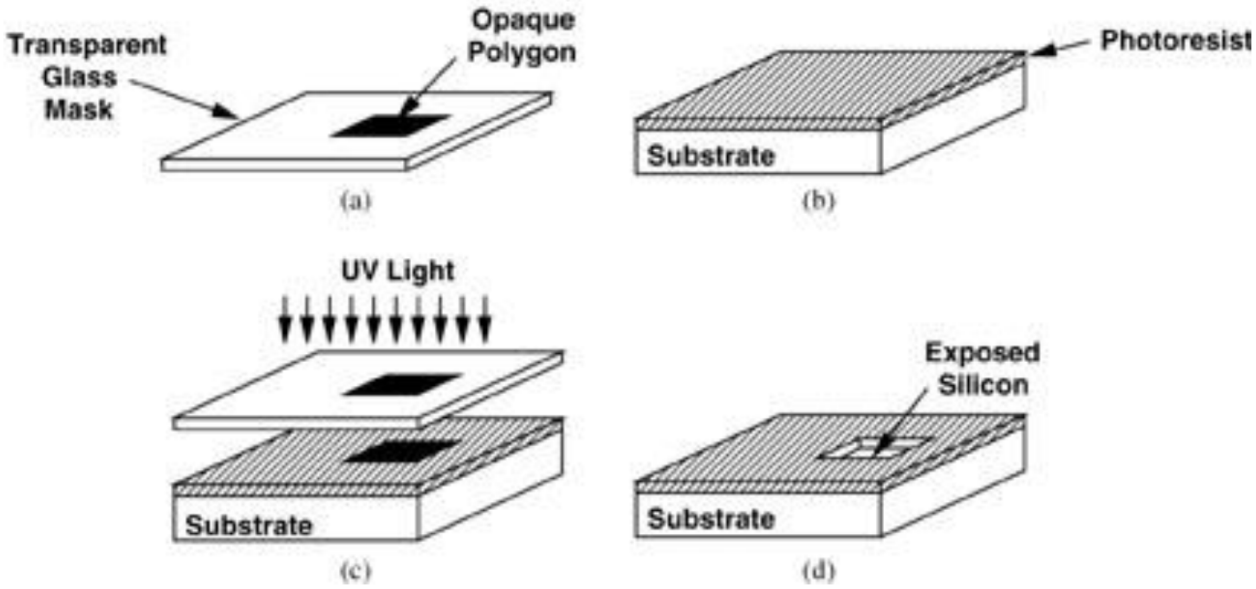


http://anysilicon.com/semiconductor-wafer-mask-costs/

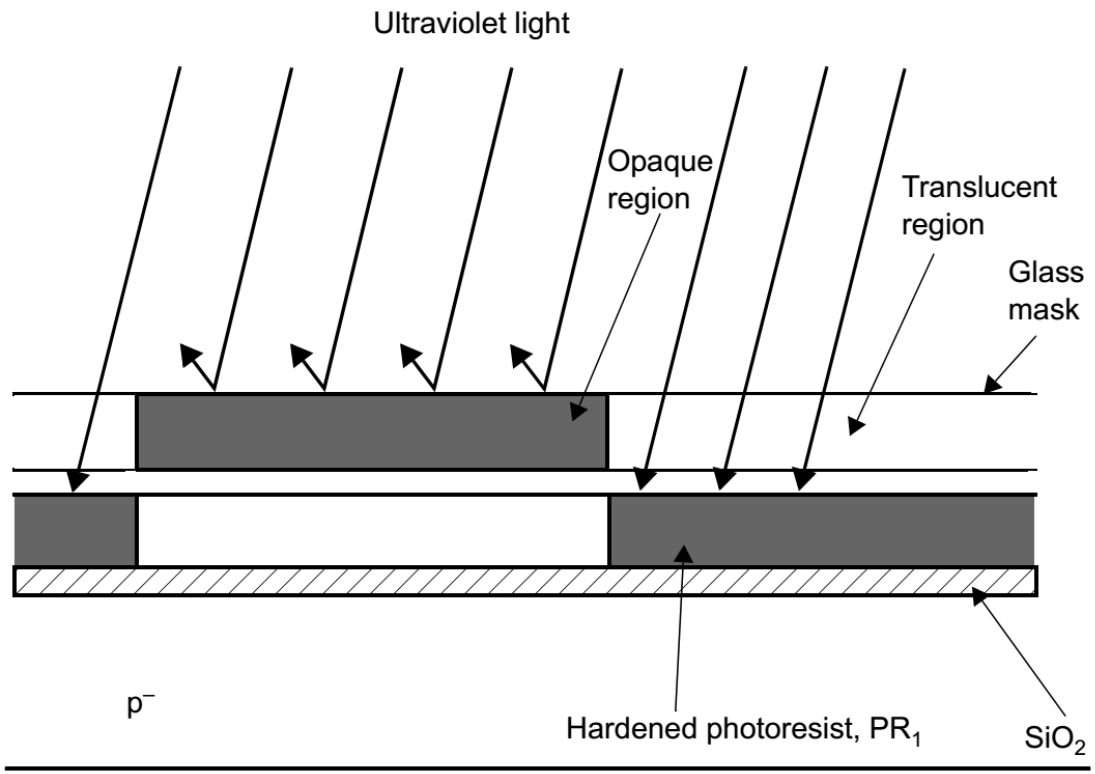
Sept. 15, 2016

Photolithography

- Used to transfer circuit layout information to the wafer



Photolithography



Wavelength = 193nm

↓

Extreme UV
Wavelength = 13.5nm

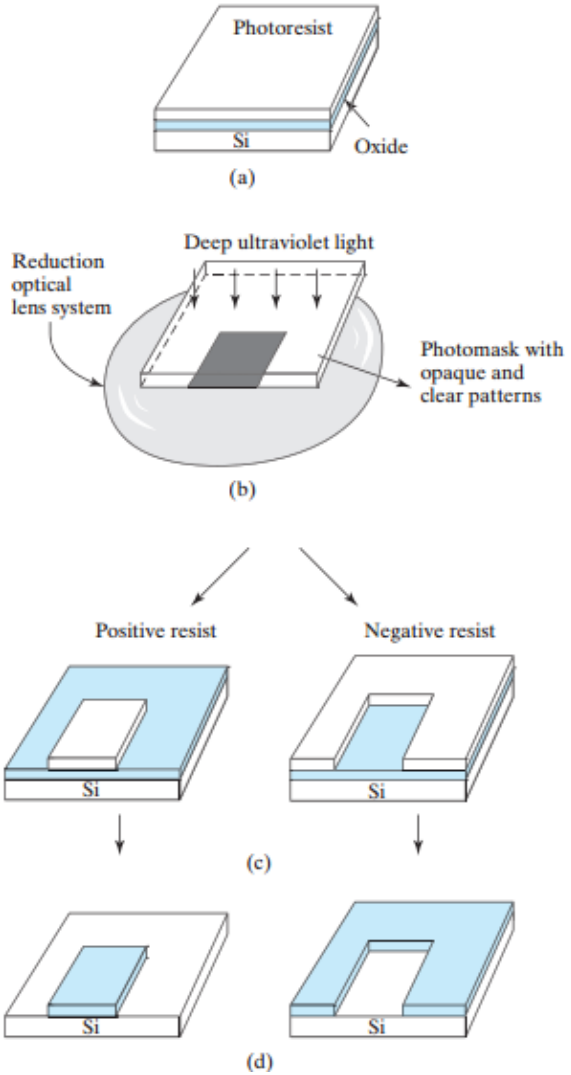
↓

X-ray
Wavelength < 10nm

Two types of photoresist

- Positive – Exposed area is softened
- Negative – Exposed area is hardened

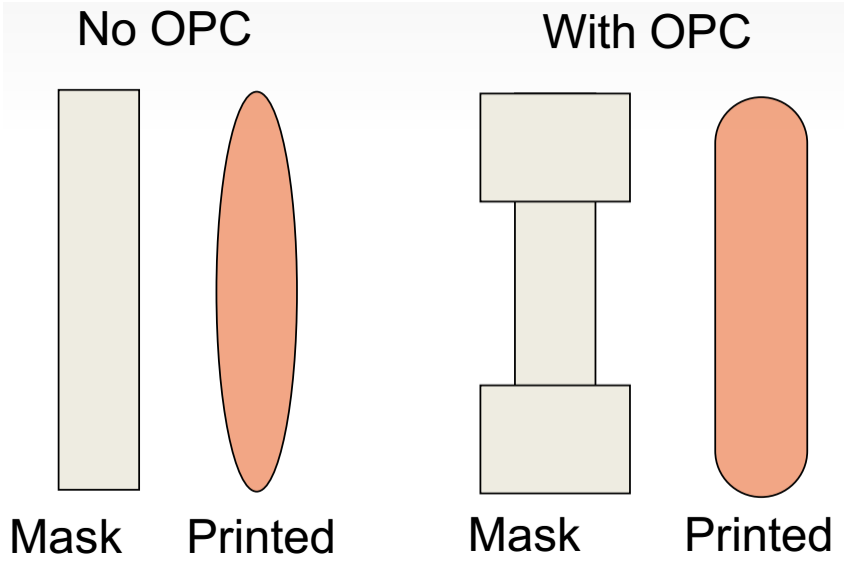
Photoresist

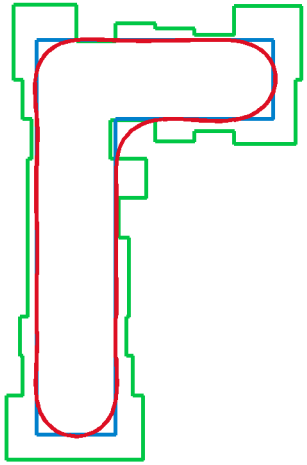


OPC

Optical Proximity Correction (OPC)

Modify the mask pattern so that the resulting geometries more closely match those intended by the designer.



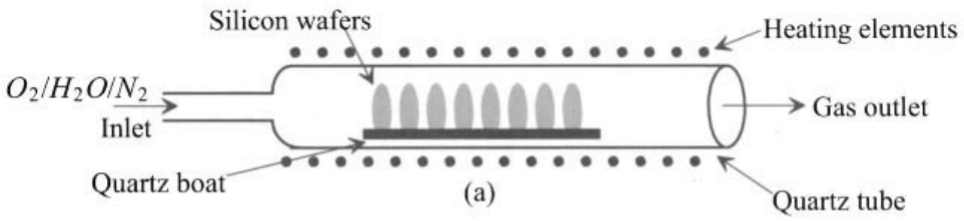


Oxidation

$$Si + O_2 \rightarrow SiO_2 \text{ (dry oxidation)}$$

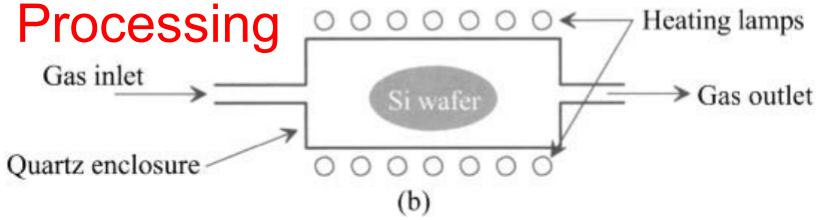
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \text{ (wet oxidation)}$$

Furnace

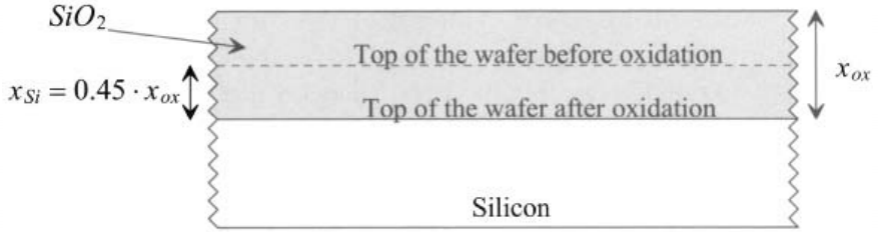


900 ~ 1200 ºC

Rapid Thermal Processing

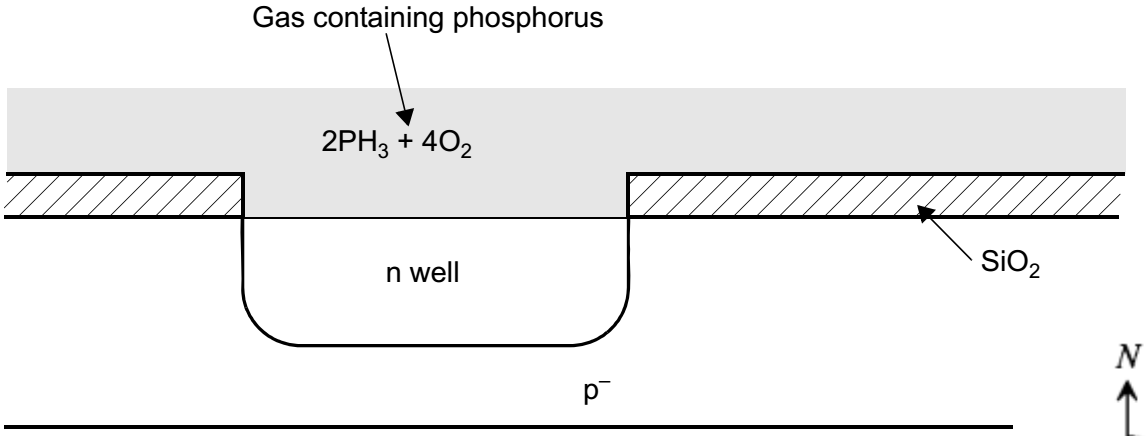


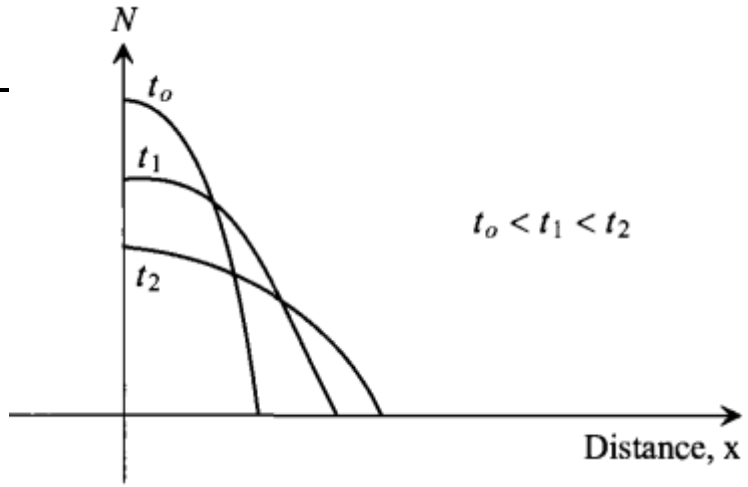
Silicon/Oxide growth interface



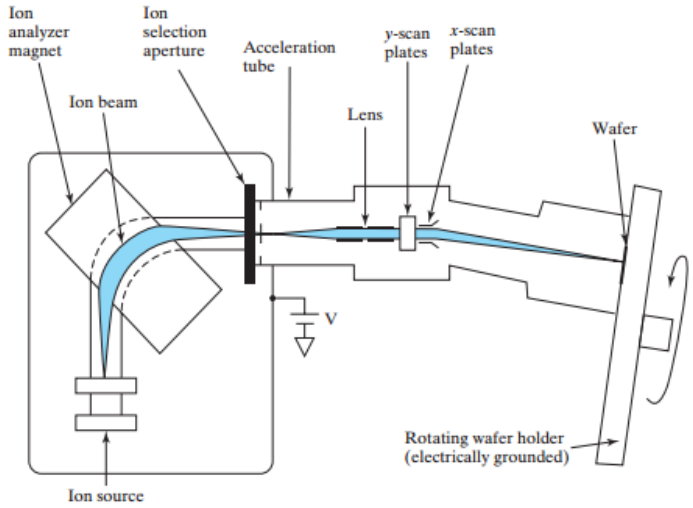
Doping by Diffusion

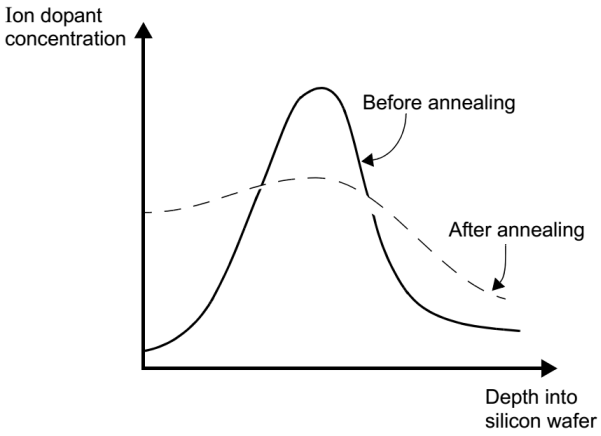
A gas containing the dopant is introduced into the tube.
For N-Well, Phosphorus or Arsenic are used
Temperature, typically 900 to 1 100 °C

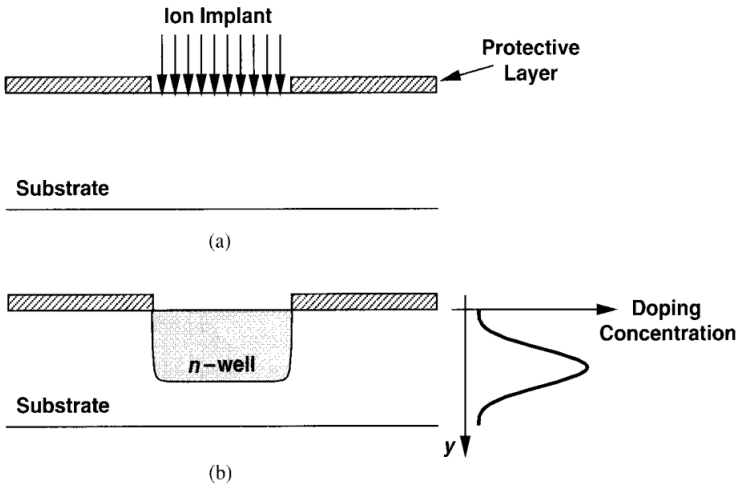


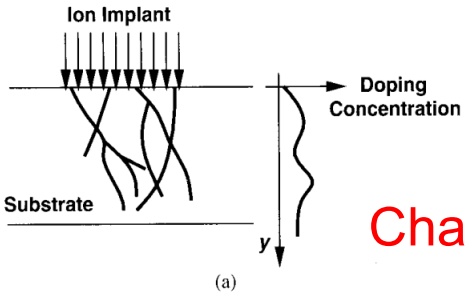


Doping by Ion Implantation

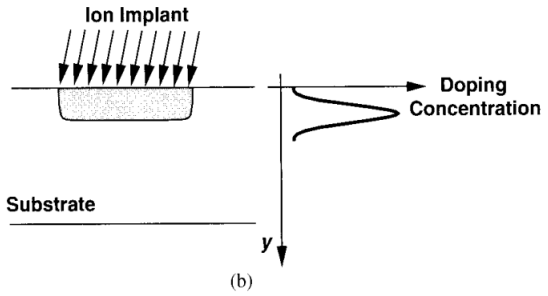




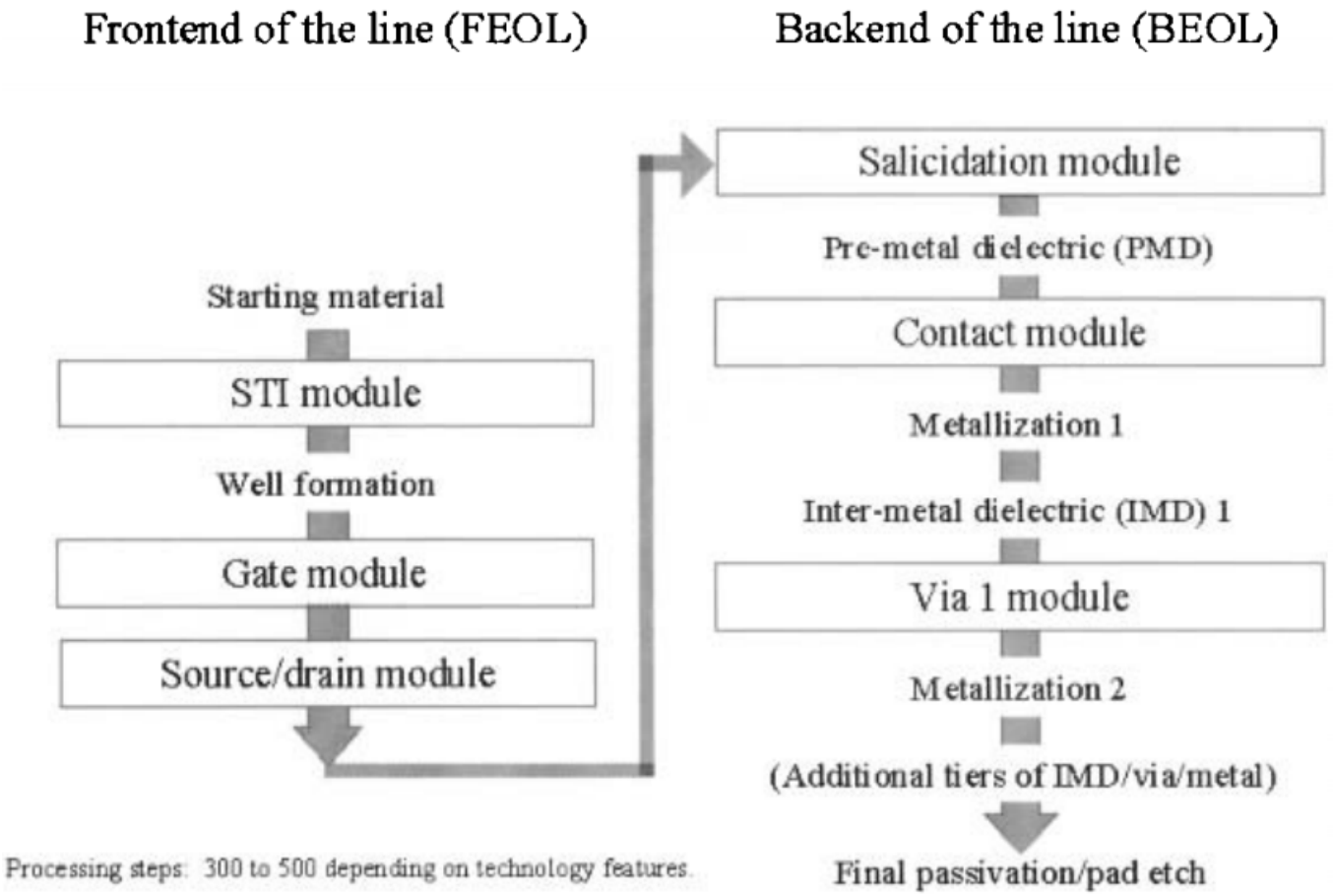




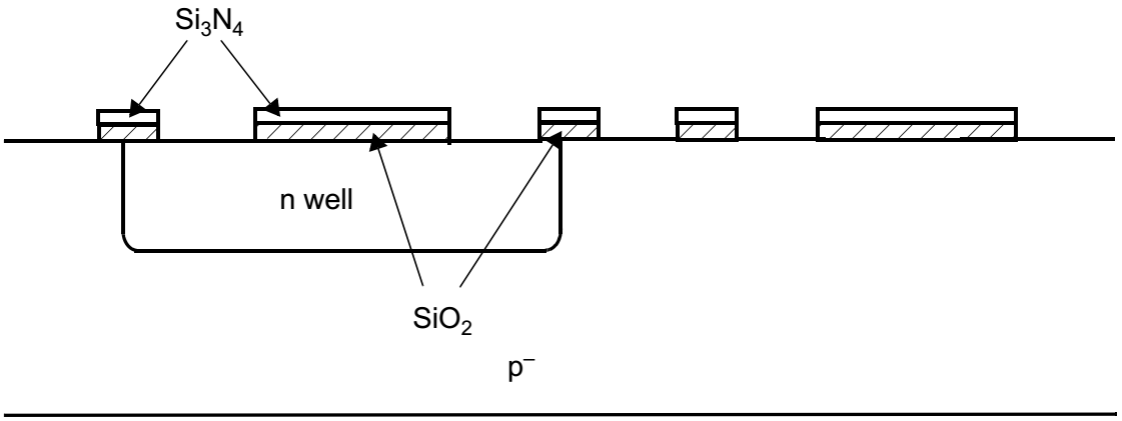
Channeling



Process Integration



Isolation

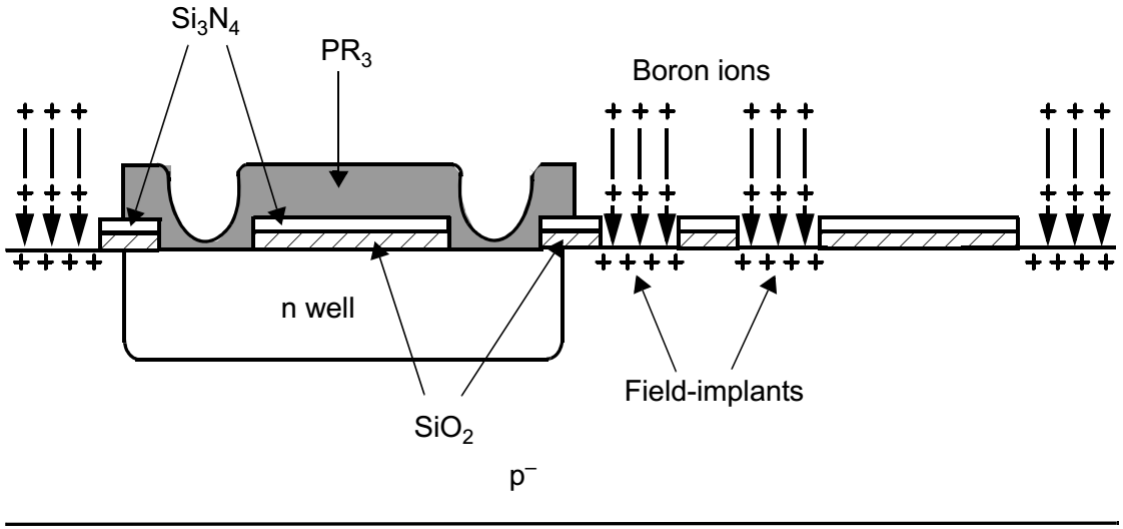


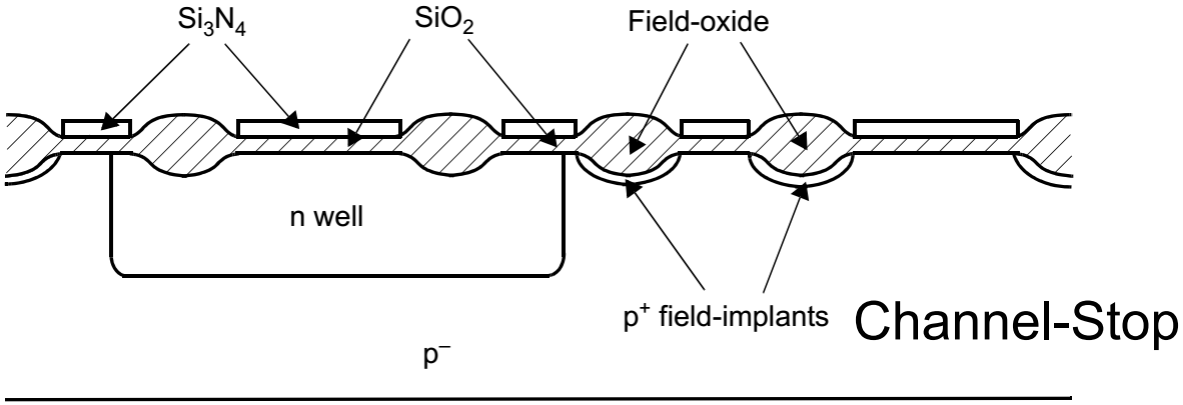
Active Region : OD (Oxide Definition)

Non-Active Region : Field Region formed by

- LOCOS (Local Oxidation of Silicon)
- STI (Shallow-Trench Isolation)

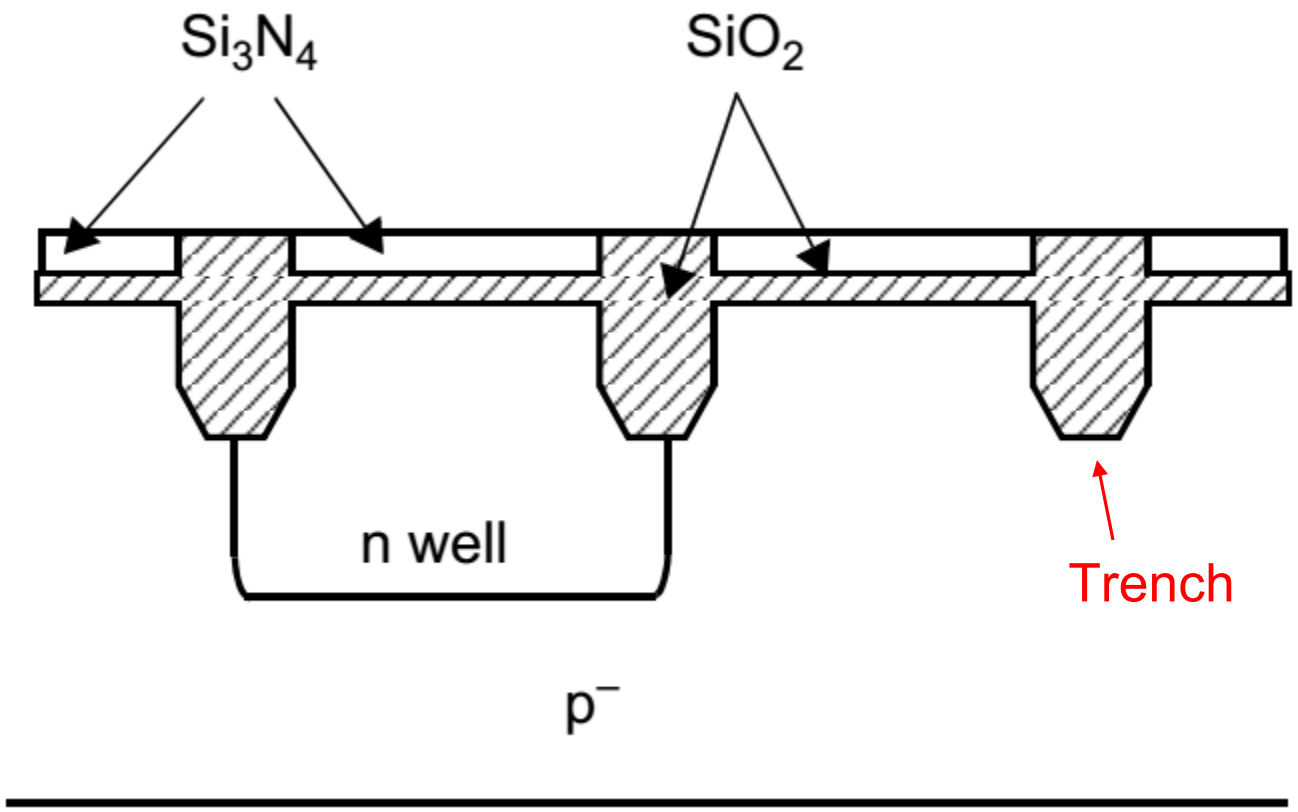
LOCOS



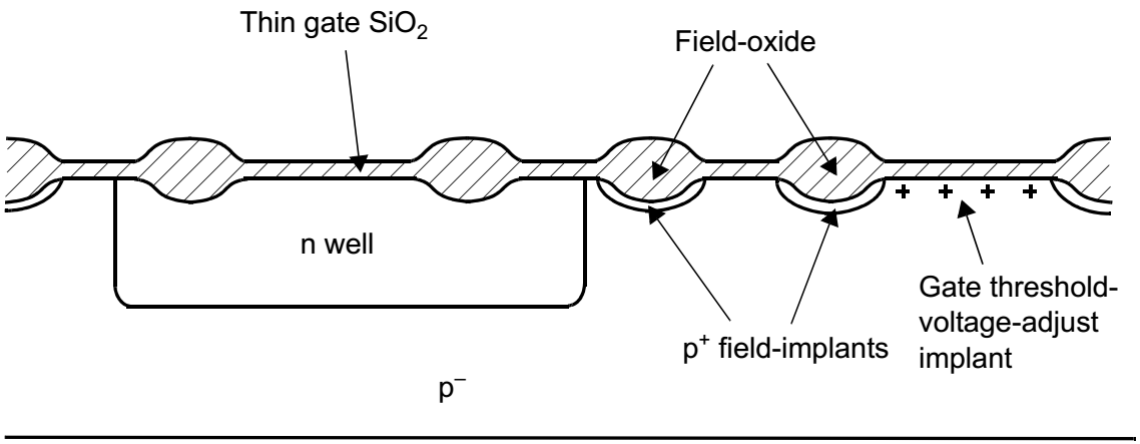


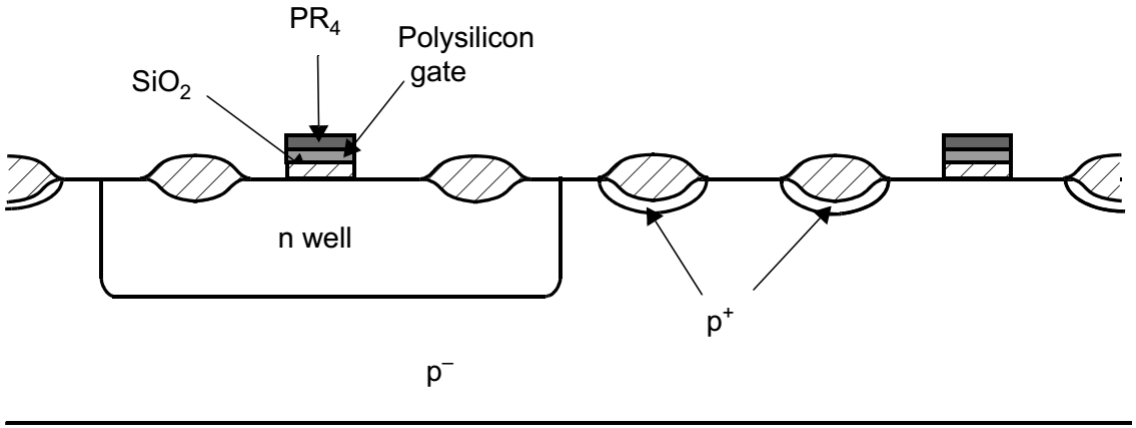
Channel-Stop

STI

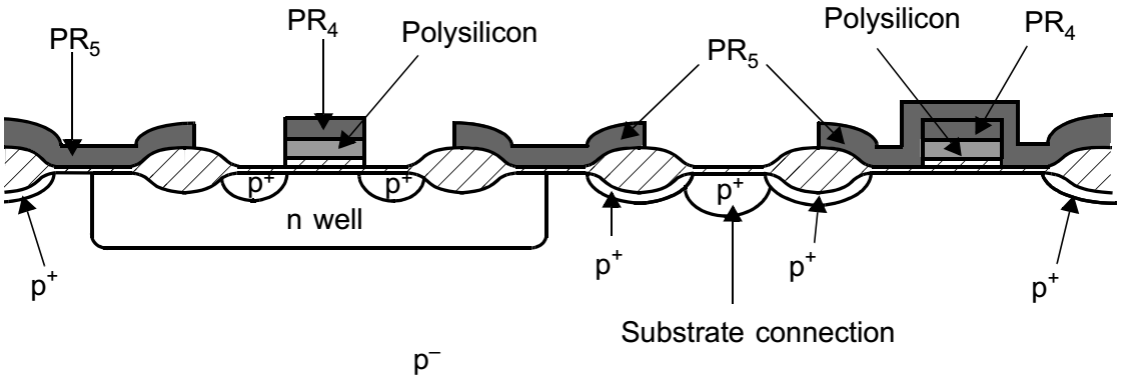


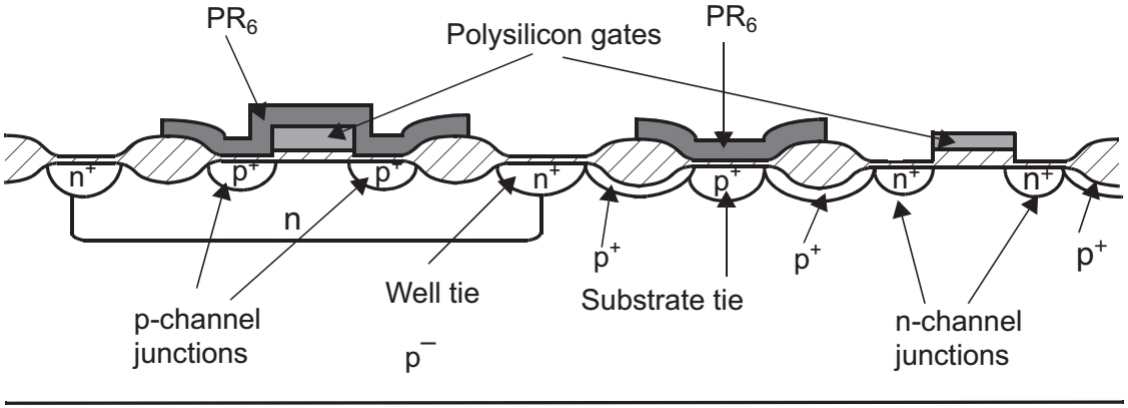
Vt Implant & Gate Definition





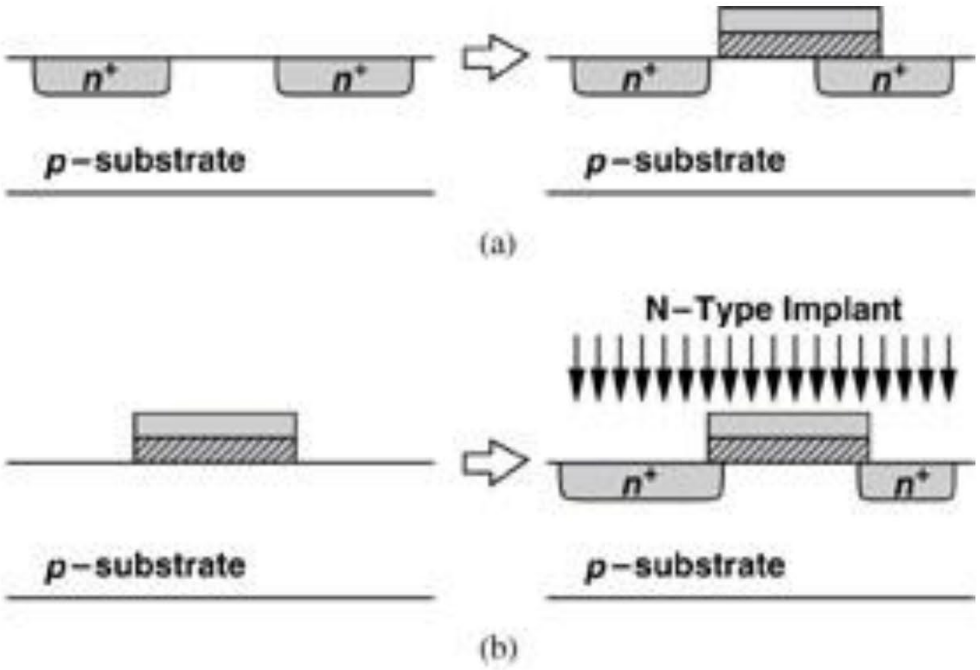
P+ S/D and N+ S/D


PR5
PR4
Polysilicon
PR5
Polysilicon
PR4
p+
p+
n well
p+
p+
p+
p+
Substrate connection
p−


PR6
Polysilicon gates
PR6
n+
p+
p+
n+
p+
n+
n+
n
p+
p+
p+
Well tie
Substrate tie
p-channel
junctions
p−
n-channel
junctions

Self-Aligned Process

- Why source and drain junctions are formed after the gate oxide and polysilicon layers are deposited?

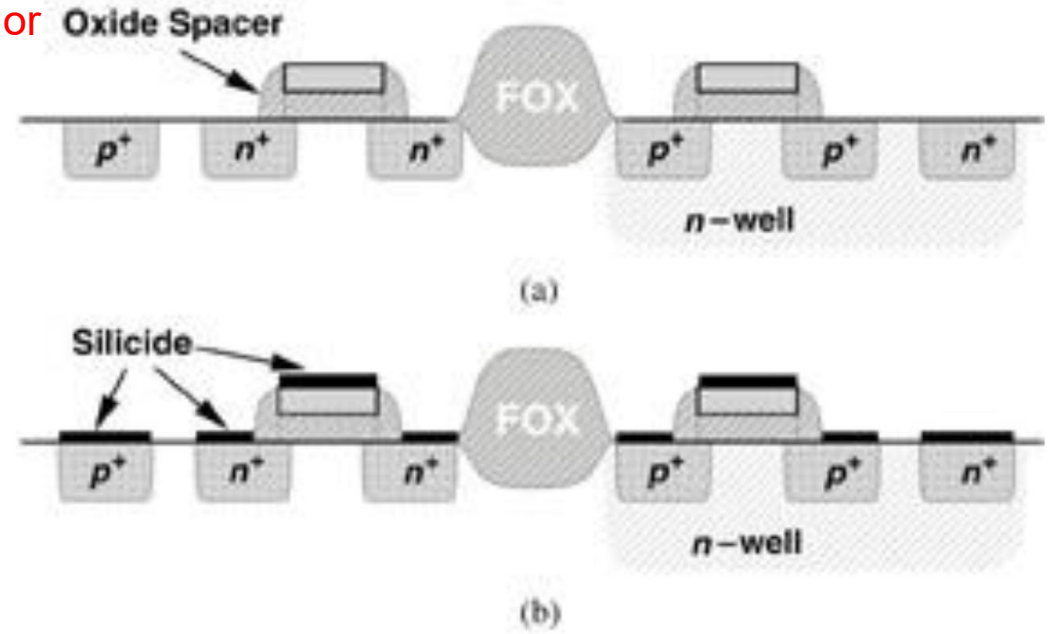


Self-Aligned Process

- Oxide spacers and silicide

Self-Aligned Silicide -> Salicide

Nitride Spacer or



FEOL

- The **front-end-of-line** (**FEOL**) is the first portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor.[1] FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers.
- FEOL contains all processes of CMOS fabrication needed to form fully isolated CMOS elements:
  1. Selecting the type of wafer to be used; Chemical-mechanical planarization and cleaning of the wafer.
  2. Shallow trench isolation (STI) (or LOCOS in early processes, with feature size > 0.25 μm)
  3. Well formation
  4. Gate module formation
  5. Source and drain module formation

BEOL

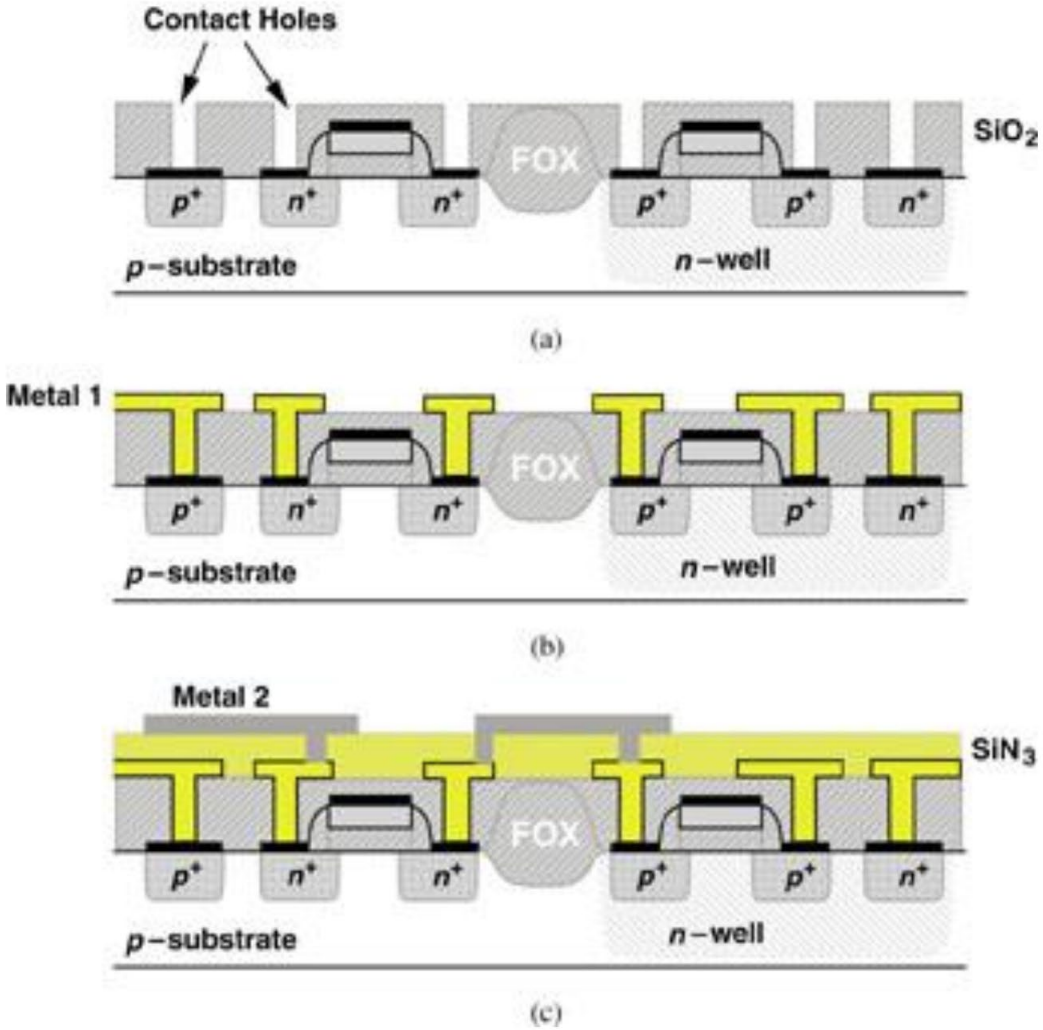
- The **back end of line** (**BEOL**) is the second portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer, the metallization layer. Common metals are copper interconnect and aluminum interconnect.[1]
- BEOL generally begins when the first layer of metal is deposited on the wafer. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.

Steps of the BEOL:

1. Silicidation of source and drain regions and the polysilicon region.
2. Adding a dielectric (first, lower layer is Pre-Metal dielectric, PMD - to isolate metal from silicon and polysilicon), CMP processing it
3. Make holes in PMD, make a contacts in them.
4. Add metal layer 1
5. Add a second dielectric (this time it is Intra-Metal dielectric)
6. Make vias through dielectric to connect lower metal with higher metal. Vias filled by Metal CVD process.
7. Repeat steps 4–6 to get all metal layers.
8. Add final passivation layer to protect the microchip

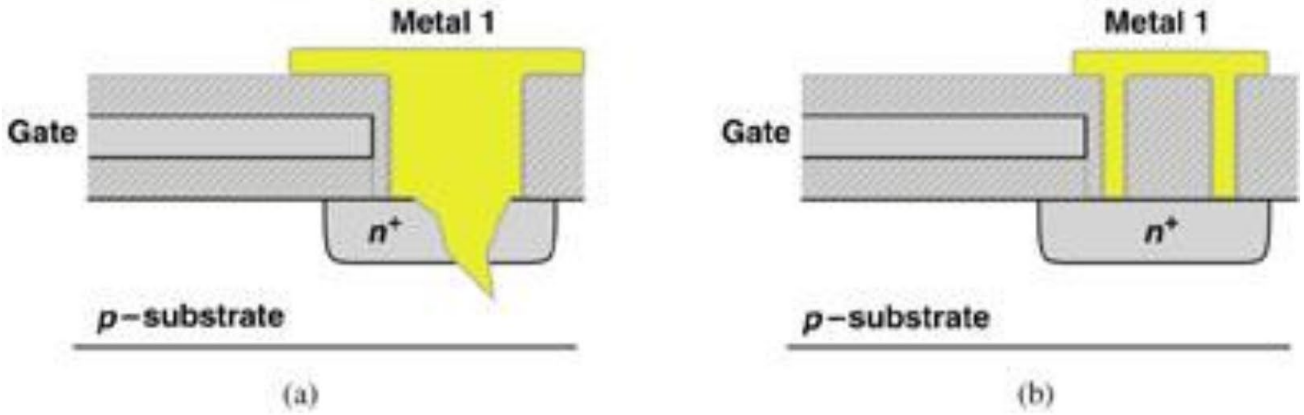
Contact and Metal

- Contact and metal layers fabrication



Spiking due to large Contact

- Large contact areas should be avoided to minimize the possibility of spiking



Passivation

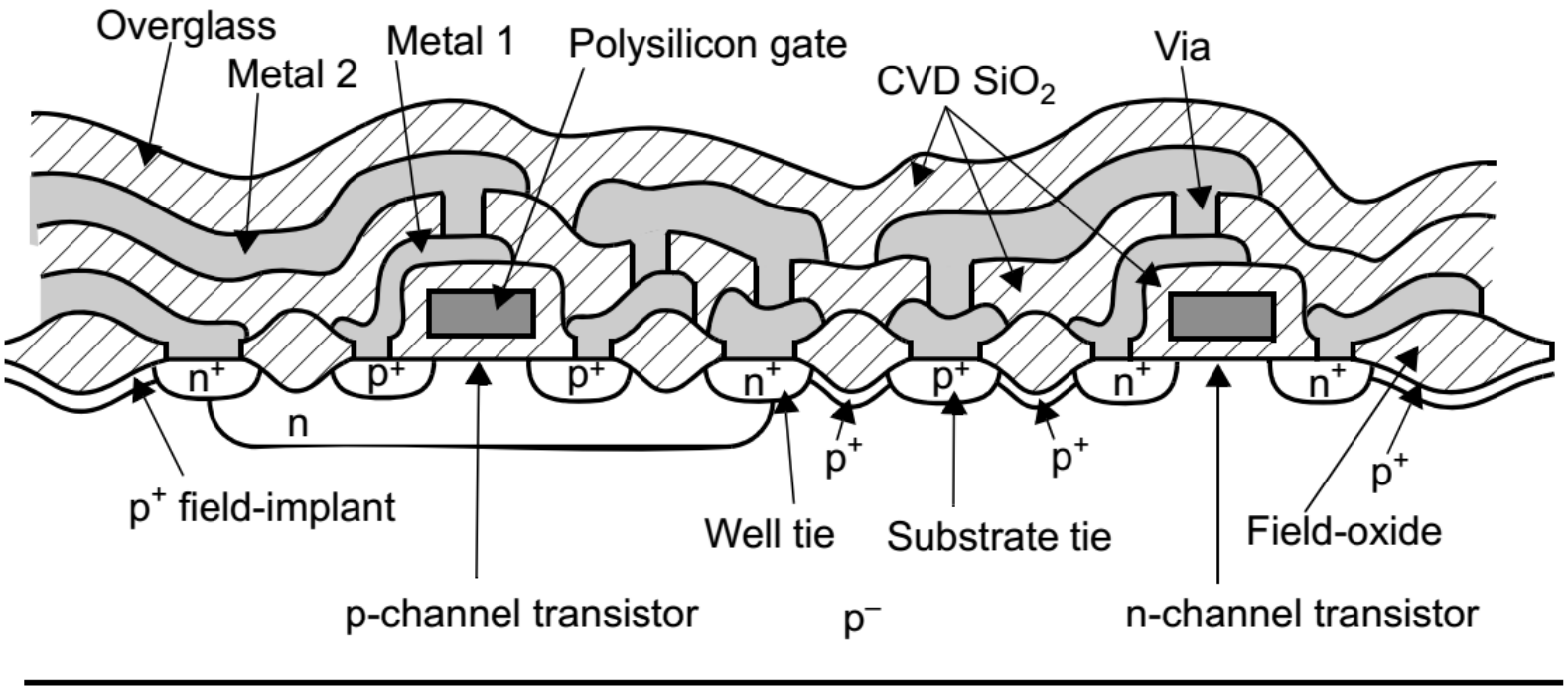
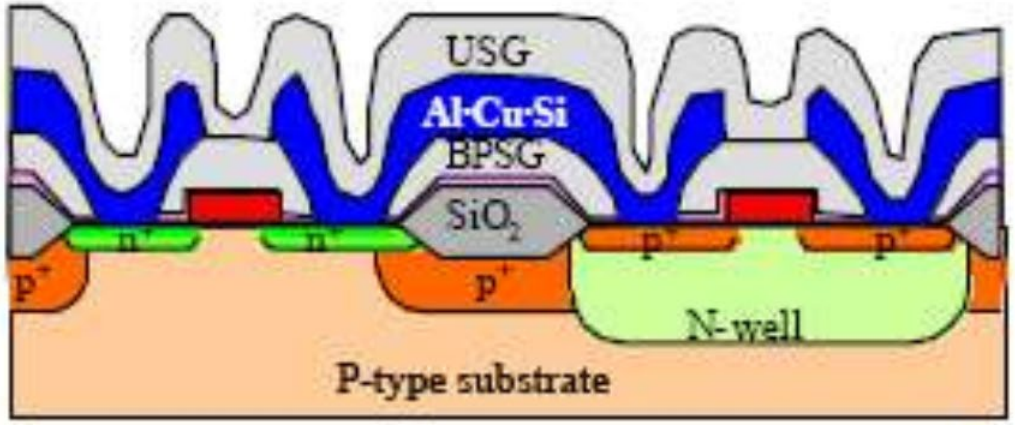


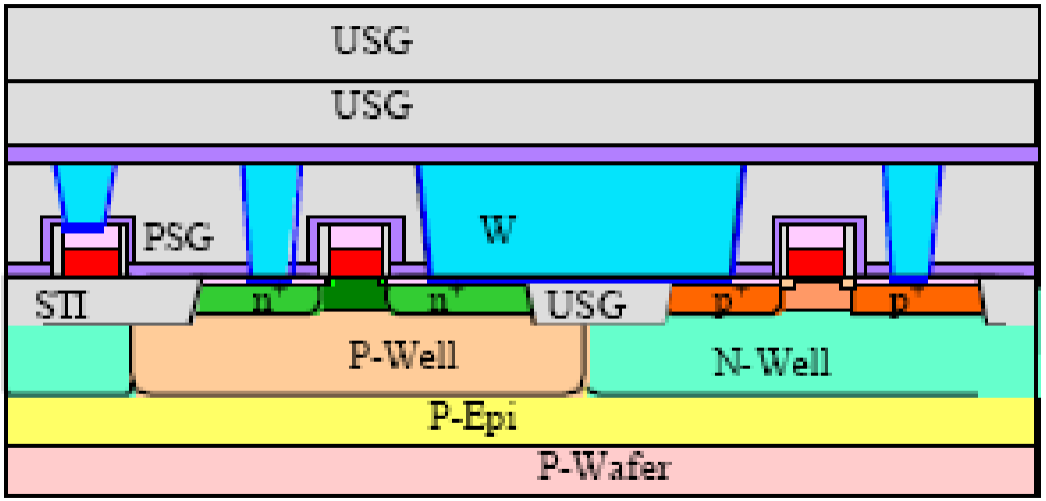
Fig. 2.13 from [Carusone]

CMP (Chemical-Mechanical Polishing/Planarization)

- Without CMP, the wafer will have a lot of topography (mountains and valleys).
- Excessive topography will:
  - Limit how small photo can print
  - Cause thinning of films on side walls
  - Compromise etch uniformity
  - Compromise film deposition uniformity



Process with CMP



Process Technology Nodes

Semiconductor manufacturing processes

10 µm – 1971
6 µm – 1974
3 µm – 1977
1.5 µm – 1982
1 µm – 1985
800 nm – 1989
600 nm – 1994
350 nm – 1995
250 nm – 1997
180 nm – 1999
130 nm – 2001
90 nm – 2004
65 nm – 2006
45 nm – 2008
32 nm – 2010
22 nm – 2012
14 nm – 2014
10 nm – 2017
7 nm – *~2018*
5 nm – *~2020*

Half-shrink

Main ITRS node	Stopgap half-node
250 nm	220 nm
180 nm	150 nm
130 nm	110 nm
90 nm	80 nm
65 nm	55 nm
45 nm	40 nm
32 nm	28 nm
22 nm	20 nm
16 nm	14 nm and 12 nm [1]
10 nm	8 nm
7 nm	6 nm
5 nm	4 nm

Technology Node	0.13/0.11 um	90/80 nm	65/55 nm	45/40 nm	32/28 nm	22/20 nm
Wafer size	8"	12"				
Gate stack	SiON/Poly				HiK/MG	
Lithography & Patterning	248nm	193nm Dry		193nm Immersion		
	NA				Double Patterning	
Strain Eng	NA	Gen-1	Gen-2	Gen-3	Gen-4	Gen-5
	NA			eSiGe		
IMD	Low-K			ELK		
Local Interconnect	NA				Local Interconnect	
Metallization	Aluminum	Copper				

EE223 process node