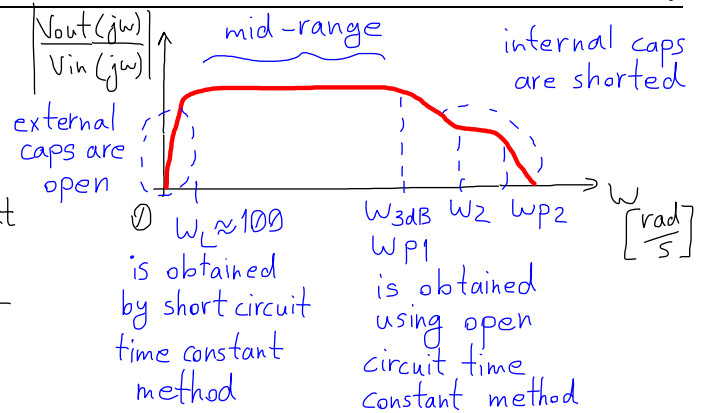
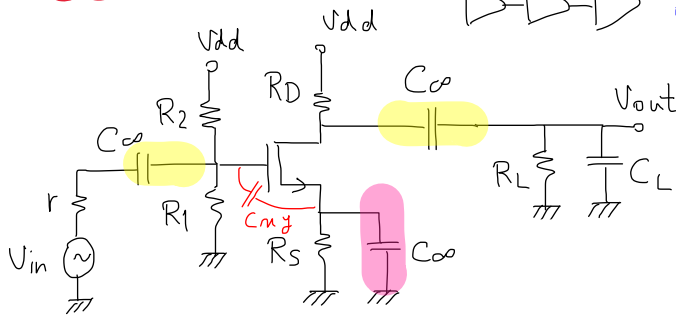


# \* Amplifier Design:



- $C_{cc}$  is in range 10pF
- $C_L$  is in range 100fF
- $C_{ny}$  is in range 10fF

- @  $w \approx 0$ , capacitors are open,  $V_{out} \approx 0$
- @ L.F., external large capacitors get shorted
- @ M.F., external caps are short and internal caps are open and maximum gain is achieved

coupling  $C_{cc}$  caps are used to isolate the biasing of different stages

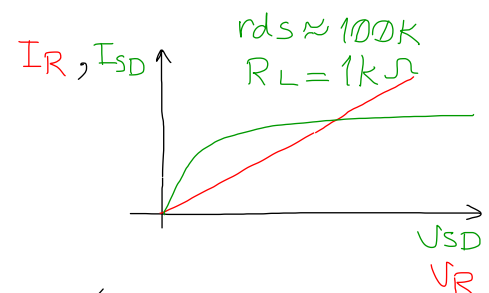
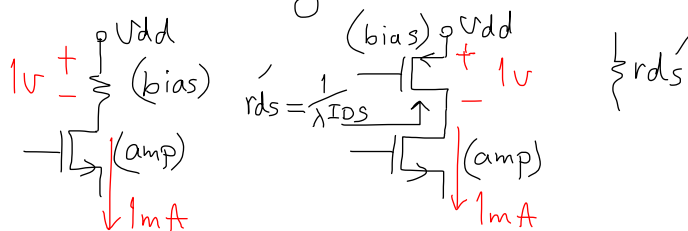
bypass  $C_{cs}$  caps are used to short a node @ high frequency

→  $w_z$ ; zero frequency is obtained using feedback null technique

→  $w_{p2}$ ; is obtained using open conductance method (developed by Dr. Hamedj)

→ in IC design, coupling capacitors use a large area and must be eliminated.

→ in IC design, bias the drain of an amplifier using a transistor rather than using a resistor.

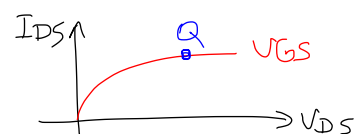
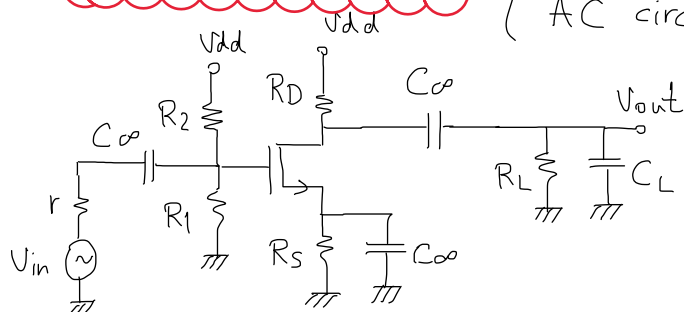


$$|\text{voltage gain}| = g_m(r_{ds} \parallel R_L) \quad |\text{voltage gain}| = g_m(r_{ds} \parallel r_{ds'})$$

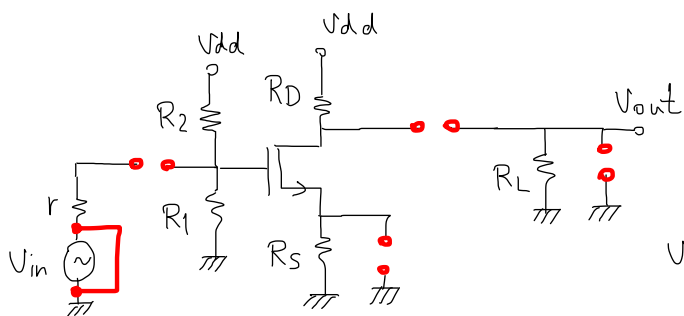
$$10 \times 10^{-3} (100k \parallel 1k) = 10 \quad 10 \times 10^{-3} (100k \parallel 100k) = 500$$

## \* Circuit Analysis:

$\left\{ \begin{array}{l} \text{DC circuit} \rightarrow \text{DC analysis} \\ \text{AC circuit} \rightarrow \text{AC analysis} \end{array} \right\}$  use superposition



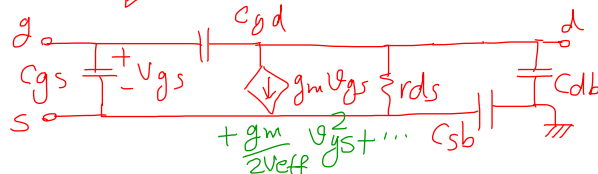
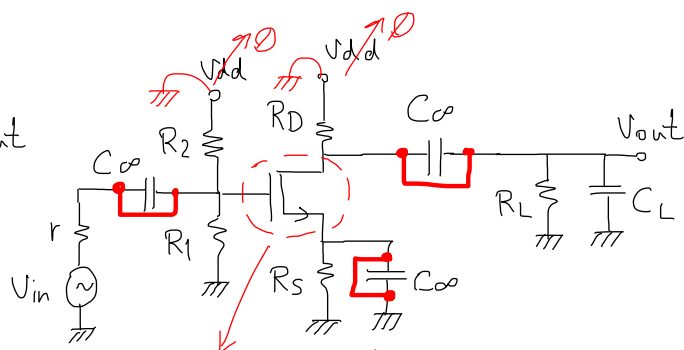
## \* DC circuit

find  $I_{DS}$ ,  $V_{GS}$ ,  $V_{DS}$ 

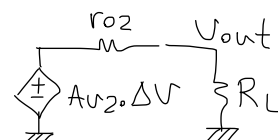
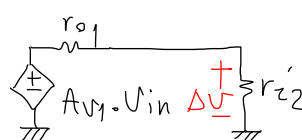
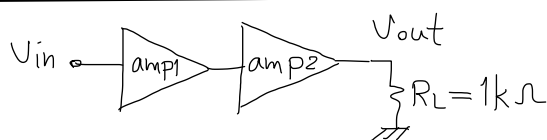
$$\text{active} \begin{cases} V_{GS} \geq V_{th} \\ V_{DS} \geq V_{GS} - V_{th} \end{cases}$$

$$\begin{cases} g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \\ r_{ds} = \frac{1}{\lambda I_{DS}} \end{cases}$$

## \* AC circuit

find  $A_{v0}$ ,  $R_{in}$ ,  $R_{out}$ ,  $\omega_{3dB}$ ,  $\omega_{p2}$ ,  $\omega_z$ 

(C.S, C.D, C.G, S.D, Cascode, diff pair)



$$r_{o1} = 9k\Omega, r_{i2} = 1k\Omega, r_{o2} = 9k\Omega, R_L = 1k\Omega$$

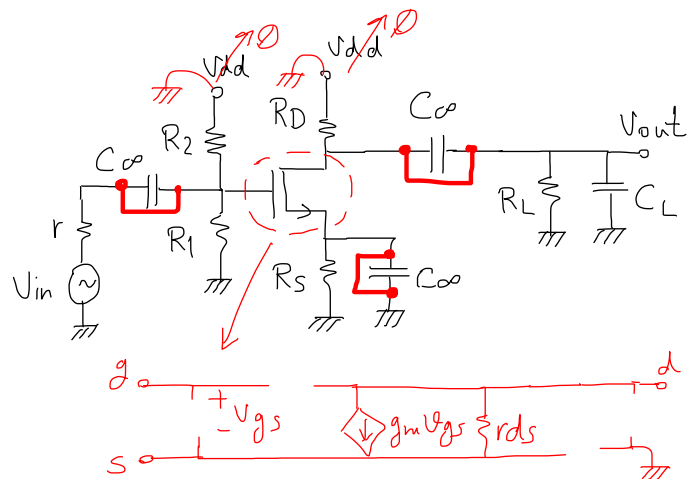
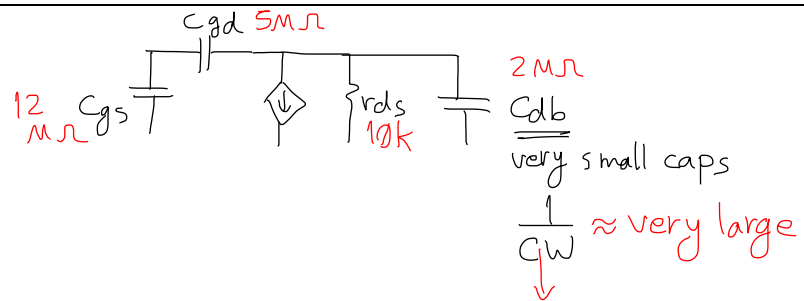
$$V_{out} = A_{v2} \cdot \Delta V \frac{R_L}{r_{o2} + R_L} = A_{v2} \frac{R_L}{r_{o2} + R_L} \times A_{v1} \cdot V_{in} \frac{r_{i2}}{r_{o1} + r_{i2}}$$

$$\frac{V_{out}}{V_{in}} = A_{v1} \cdot A_{v2} \cdot \frac{1}{10} \times \frac{1}{10}$$

\* Find  $A_{v0}$ :

→ open all internal caps

→ find  $\frac{V_{out}}{V_{in}} = A_{v0}$



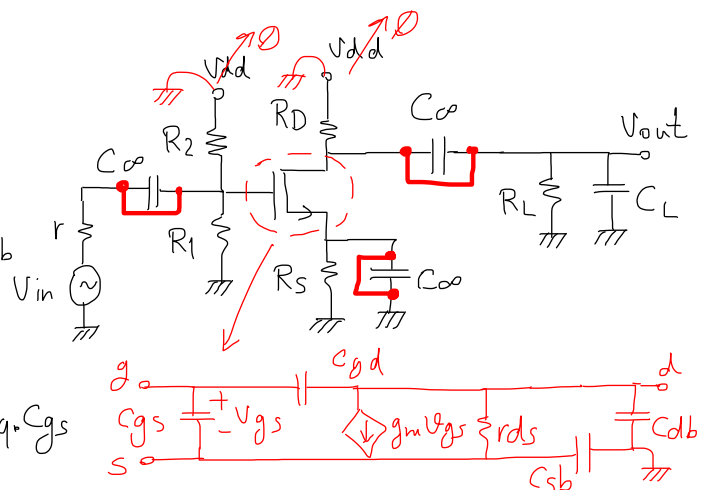
\* find  $W_{3dB}$  (or  $W_{p1}$ ):

→ find time constant for each internal cap

→  $W_{3dB} = \frac{1}{Z_{gs} + Z_{gd} + Z_{db} + Z_{sb}}$

keep  $C_{gs}$ , open other caps

find  $R_{eq}$  across  $C_{gs}$ ,  $Z_{gs} = R_{eq} \cdot C_{gs}$   
repeat for other caps



\* find  $W_z$ :

→ find condition that make output zero  $\Rightarrow$  extract  $W_z$

\* find  $W_{p2}$ :

no method is developed

\* find  $\omega_L$ :

- use short circuit time constant method
- keep a cap and short all other caps find time constant repeat for other caps

$$\omega_L = \frac{1}{\tau_1} + \frac{1}{\tau_2} + \dots$$

