EE141-Spring 2010 Digital Integrated Circuits

Lecture 4
Switch Logic

Administrativia

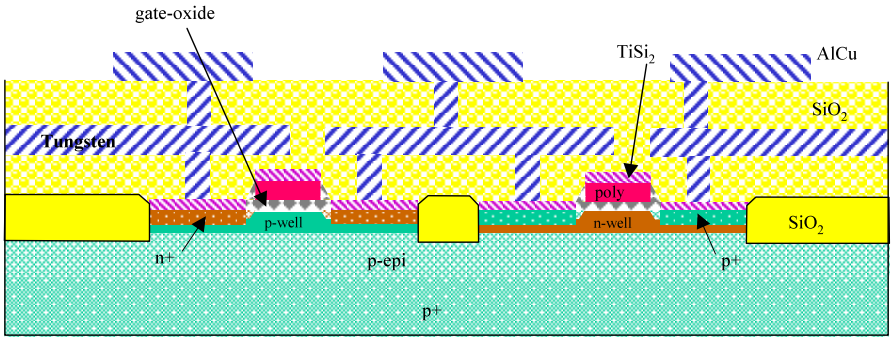
- Assignment #1 due today!
- Assignment #2 to be posted right thereafter
- DIS 101 (Th 11am-noon) in GPB (Genetics and Plant Biology) 107 starting next week
- Office hours of TAs in 557 Cory
- Labs start next week (Monday)

Class Material

- Last lecture
  - Basic metrics for IC design
  - Manufacturing
- Today's lecture
  - Design Rules
  - Introduction to switch logic
- Reading (2.3, 3.3.1-3.3.2)

Intermezzo: Design Rules

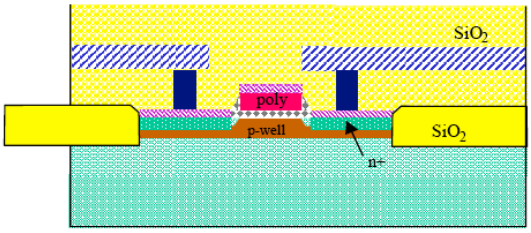
A Modern CMOS Process



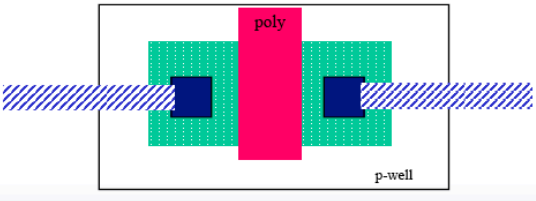
Dual-Well Shallow-Trench-Isolated CMOS Process

Transistor Layout

Cross-Sectional View



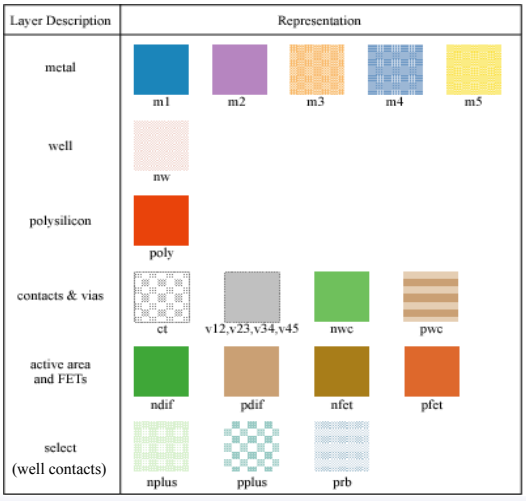
Layout View



CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Well contact (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Layers in 0.25 μm CMOS process



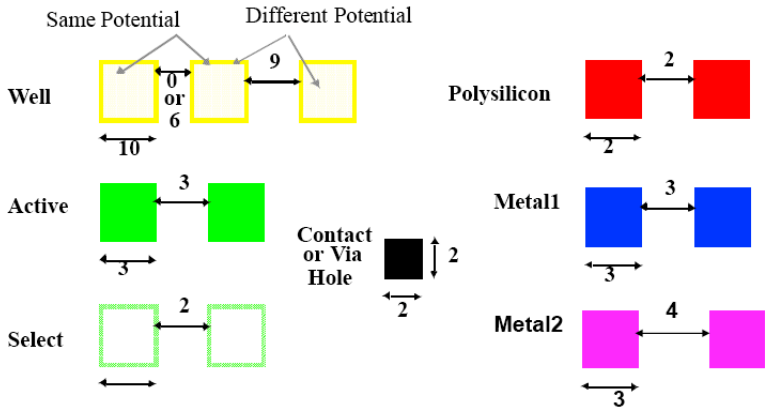
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

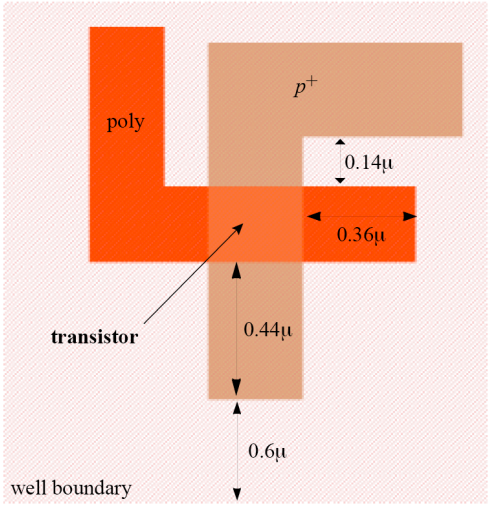
Design Rules

- Intra-layer
  - Widths, spacing, area
- Inter-layer
  - Enclosures, distances, extensions, overlaps
- Special rules (sub-0.25μm)
  - Antenna rules, density rules, (area)

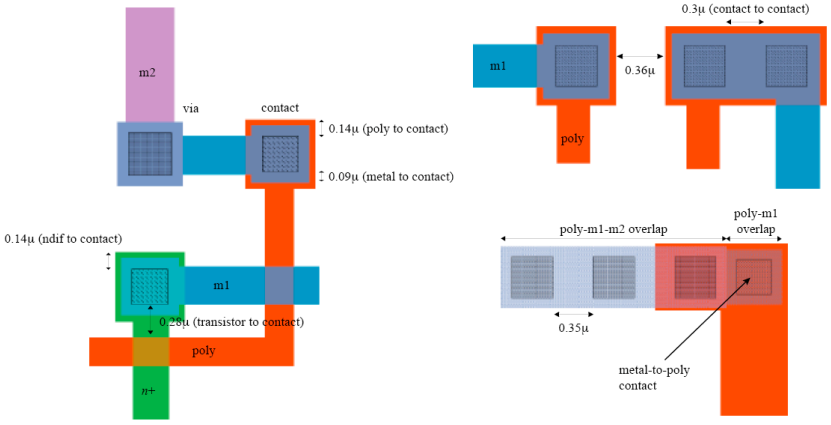
Intra-Layer Design Rules



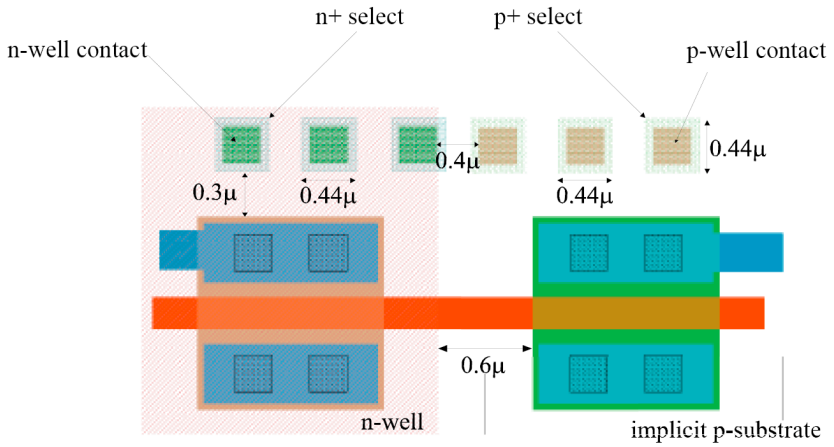
Inter-Layer: Transistor Layout



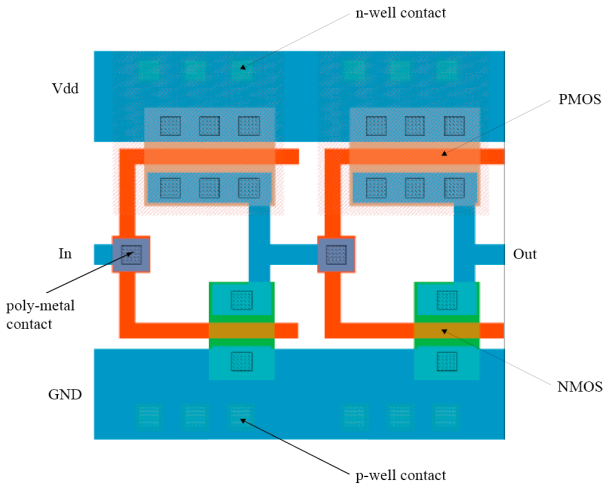
Inter-Layer: Vias and Contacts



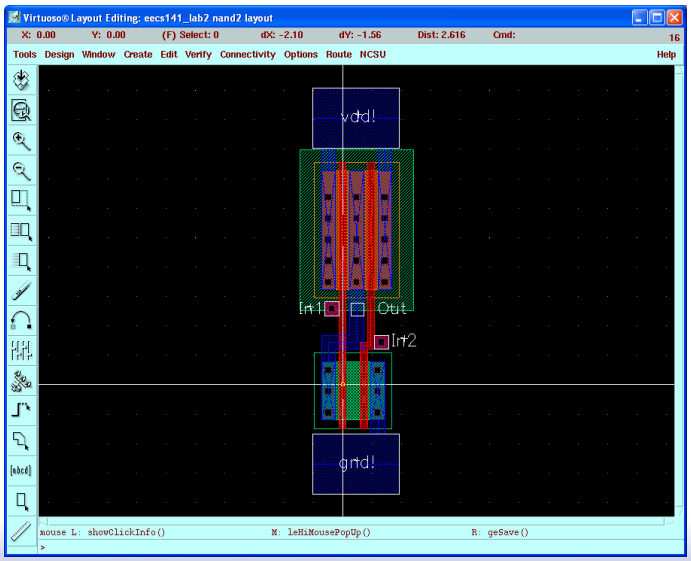
Inter-Layer: Well and Substrate



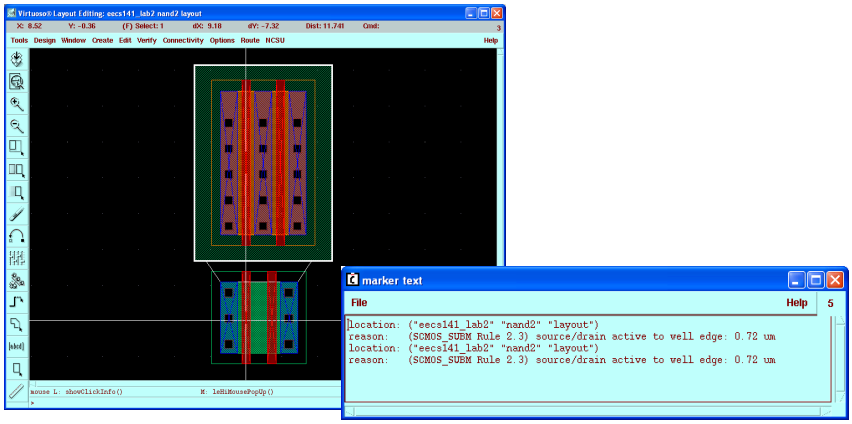
CMOS Inverter Layout



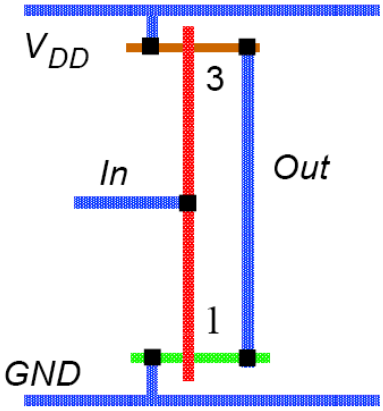
Layout Editor



Design Rule Checker



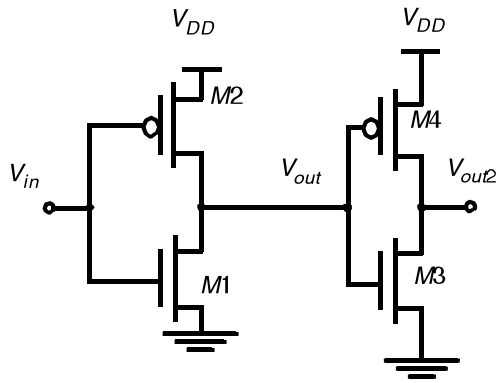
Sticks Diagram



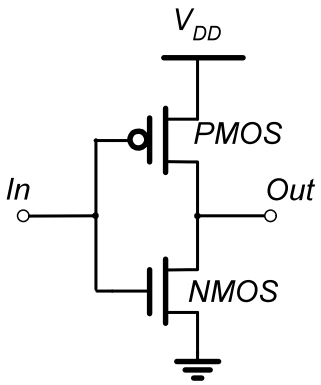
Stick diagram of inverter

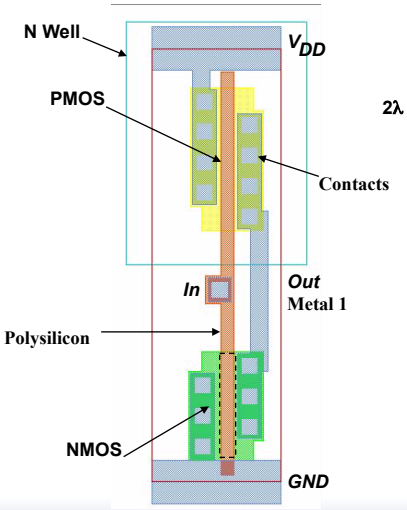
- Dimensionless layout entities
- Only topology is important

Circuit Under Design



CMOS Inverter

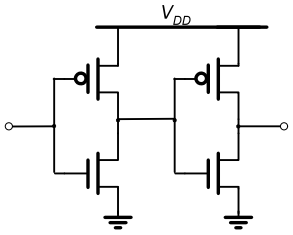


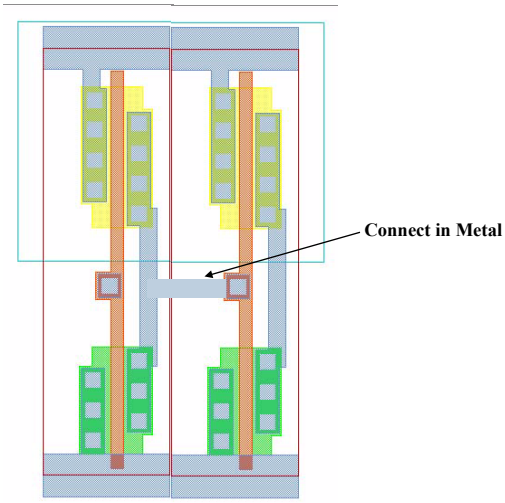


Two Inverters

Share power and ground

Abut cells

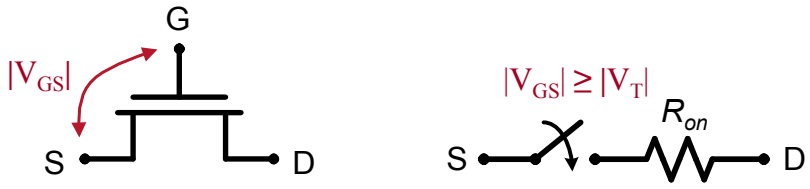




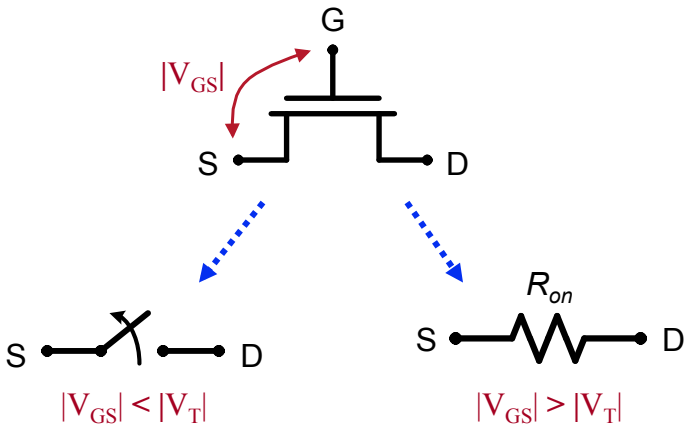
Switch Logic

What is a Transistor?

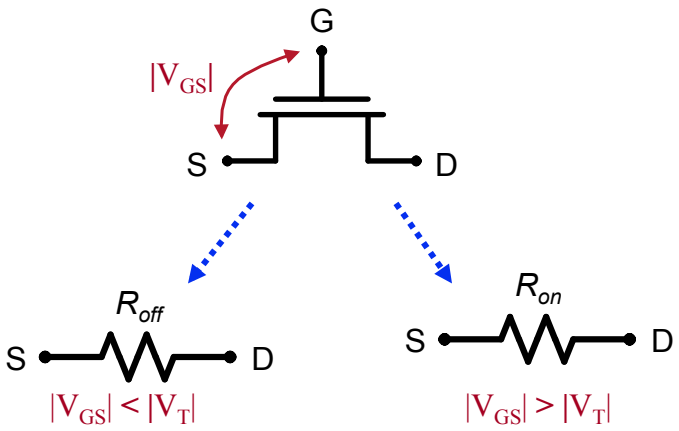
An MOS Transistor ⟷ A Switch!



Switch Model of MOS Transistor

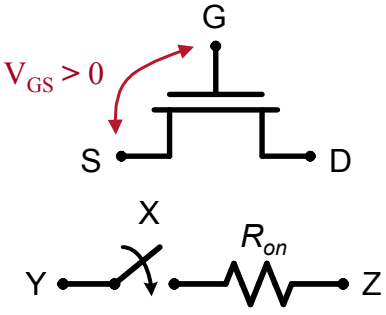


A Modern Sub-100 nm Look …



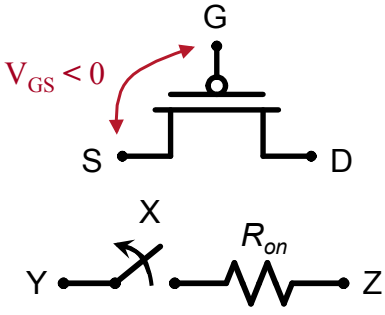
NMOS and PMOS

NMOS Transistor



Y=Z IF X=1

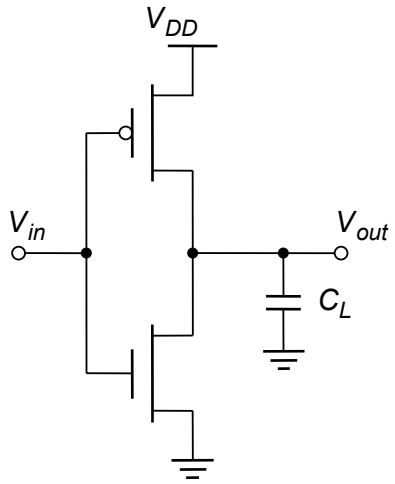
PMOS Transistor



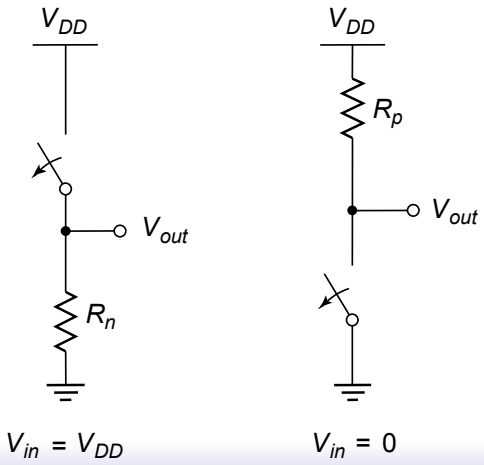
Y=Z IF X=0

Building an Inverter with Switches

The CMOS Inverter: A First Glance



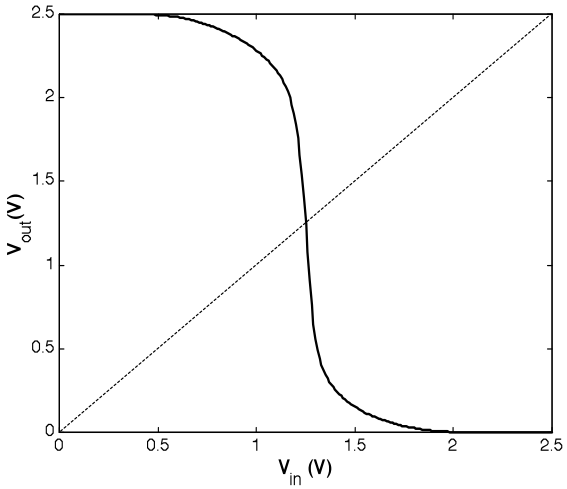
CMOS Inverter
First-Order DC Analysis



$V_{in} = V_{DD}$ $V_{in} = 0$

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

Simulated Inverter VTC (Spice)



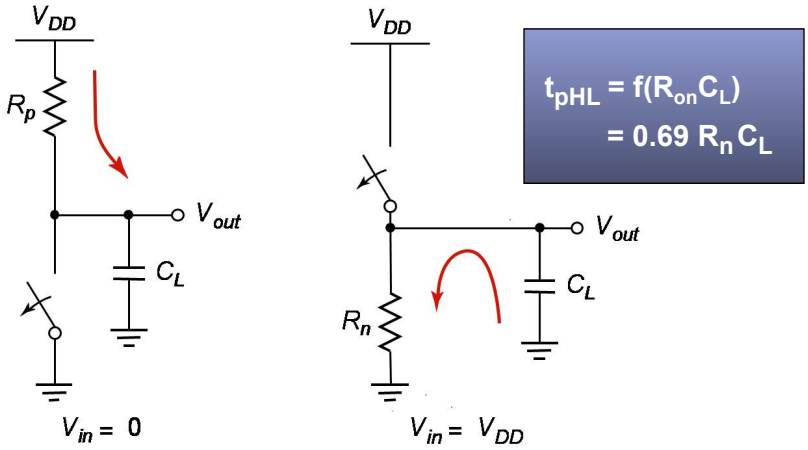
CMOS Inverter: DC Properties

- V_{OH} =
- V_{OL} =
- V_{IL} =
- V_{IH} =
- N_{MH} =
- N_{ML} =
- V_M =

CMOS Inverter: DC Properties

- $V_{OH} = V_{DD} = 2.5V$
- $V_{OL} = 0V$
- $V_M = 1.2V$
- $V_{IL} = 1.05V$
- $V_{IH} = 1.45V$
- $N_{MH} = 1.05V$
- $N_{ML} = 1.05V$

CMOS Inverter: Transient Response



(a) Low-to-high (b) High-to-low

CMOS Properties

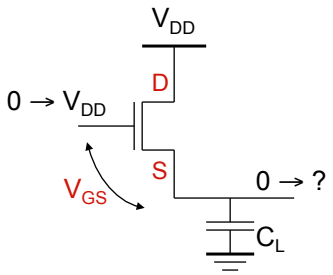
- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation
- Direct path current during switching

Impact on Reliability?

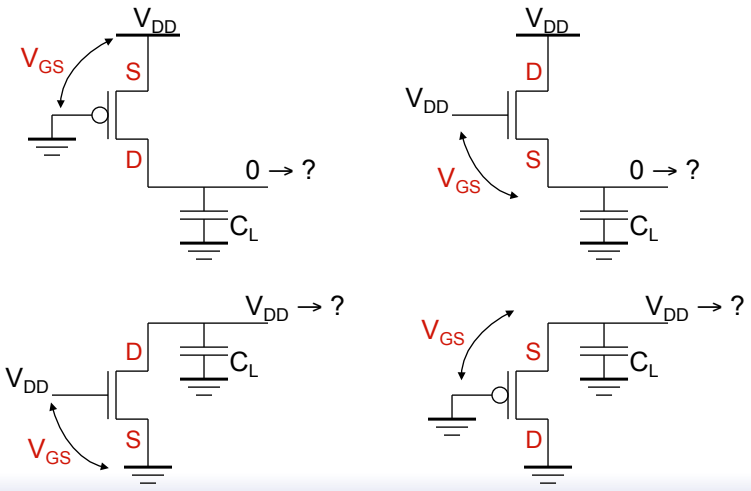
Impact on Performance?

Impact on Power/Energy

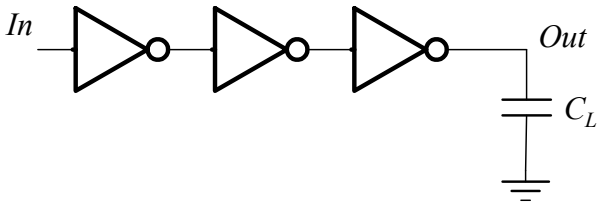
A Side Note: How Good a Switch is the MOS Transistor?



How Good a Switch is an MOS?



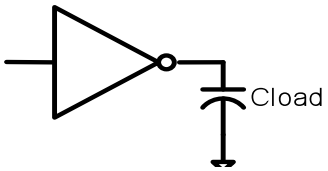
The Next Question: Inverter Chain



- For some given C_L:
  - How many stages are needed to minimize delay?
  - How to size the inverters?
- Anyone want to guess the solution?

Careful about Optimization Problems

- Get fastest delay if build one **very** big inverter
  - So big that delay is set only by self-loading



- Likely not the problem you're interested in
  - Someone has to drive this inverter…

Engineering Optimization Problems in General

- Need to have a set of constraints
- Constraints key to:
  - Making the result useful
  - Making the problem have a 'clean' solution
- For sizing problem:
  - Need to constrain size of first inverter

Delay Optimization Problem #1

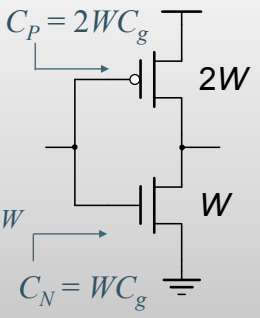
- You are given:
  - A fixed number of inverters
  - The size of the first inverter
  - The size of the load that needs to be driven
- Your goal:
  - Minimize the delay of the inverter chain
- Need model for inverter delay vs. size

Inverter Delay

Delay: $t_{pHL} = (\ln 2)\, R_N C_L$ $t_{pLH} = (\ln 2)\, R_p C_L$

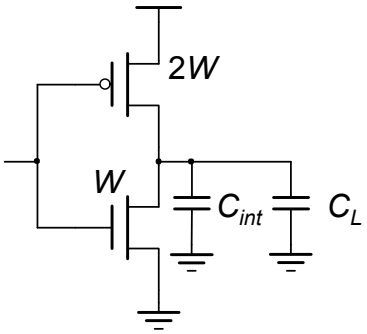
- Assume we want equal rise/fall delays

  $t_{pHL} = t_{pLH}$
  - Need approximately equal resistances, $R_N = R_P$
  - PMOS approximately 2 times larger resistance for same size;
  - Must make PMOS 2 times wider, $W_P = 2W_N = 2W$
  - $t_p = (\ln 2)\,(R_{inv}/W)\, C_L$ with R_{inv} resistance of minimum size NMOS



Loading on the previous stage: $C_{in} = WC_{ginv} = W(3C_G)$

Inverter Delay Model



$R = R_{inv}/W$

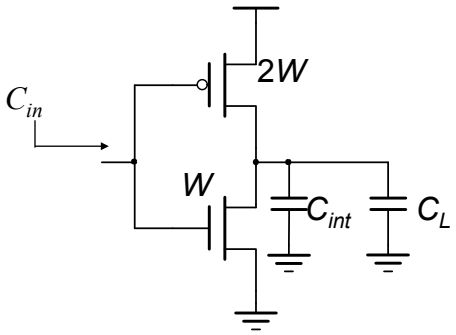
$C_{int} = W(3C_d) = WC_{dinv}$

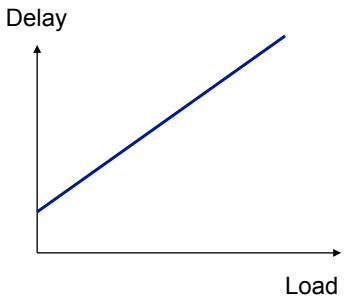
Replace ln(2) with k (a constant):

Delay = $kR(C_{int} + C_{L)}$

Delay = $k(R_{min}/W)(WC_{dinv} + C_L)$

Inverter with Load





Delay = $\boldsymbol{kR\,C_{in}(C_{int}/C_{in} + C_L/C_{in})}$

$= \boldsymbol{kR_{min}C_{ginv}[C_{dinv}/C_{ginv} + C_L/(WC_{ginv})]}$

= Delay (Internal) + Delay (Load)

$C_{dinv}/C_{ginv} = \gamma =$ **Constant independent of size**

Delay Formula

$$Delay \sim R_W \left(C_{int} + C_L\right)$$

$$t_p = kR_W C_{\text{in}} \left(C_{\text{int}} / C_{in} + C_L / C_{in}\right) = t_{inv} \left(\gamma + f\right)$$

$C_{int} = \gamma\, C_{in}$ ($\gamma \approx 1$ for CMOS inverter)

$f = C_L / C_{in}$ – electrical fanout

$t_{\text{inv}} = kR_{min} C_{ginv}$

t_{inv} is independent of sizing of the gate!!!