Design of Common-Gate Amplifier using Surrounding Gate Field Effect Transistors

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***Abstract*—This assignment serves as an introductory to designing Analog integrated circuits using the 10nm silicon nanowire surrounding gate field effect transistor (SGFET). In this assignment, the common-gate (CG) amplifier, which is one of the single-stage amplifier topologies, is designed using both hand analysis & software simulations using Cadence Virtuoso's Analog-Design Environment (ADE).**

***Index Terms*— Cadence virtuoso, Common-Gate Amplifiers, SGFET, Single-Stage Amplifiers**

I. Introduction

SINGLE stage amplifiers are the basis for designing any analog integrated circuit. Each single stage amplifier topology provides certain properties, like gain, voltage swing, bandwidth, & linearity, whose values are chosen according to the application. These amplifiers are used to further build greater circuits like Op-Amps & OTA, thus making it essential to study the characteristics of each topology.[1]

In this assignment, the CG amplifier topology will be designed to meet certain specifications using the 10nm silicon nanowire SGFET technology.[2]

II. Circuit & Specs

The CG amplifier circuit is shown in Fig. 1. The branches of the transistors Q3 & Q4 are used along with a resistance connected to each of them in series to provide a biasing voltage for the main circuit. The transistor Q1 is the main amplifier device, where the input is connected to its source & the output is connected to its drain, while the gate being the common node between the output & the input. Q2 provides the amplifier with the high output resistance necessary for the gain, & it forms a current mirror pair along with Q3.

The specs upon which the circuit is designed are shown in Table I. The hand analysis of the circuit & the sizing of each transistor are done within these specs to ensure that the output wanted is obtained upon applying the input.

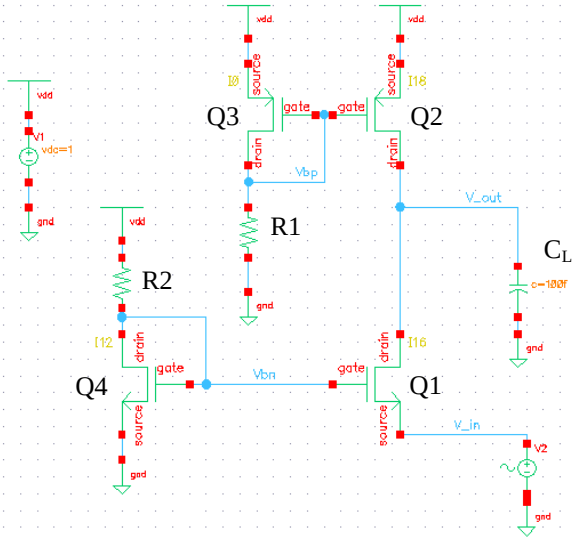

Fig. 1. CG amplifier circuit

TABLE I
The CG Amplifier Design Specs

Specifications	Values
Supply Voltage	1 V
3-dB Bandwidth	> 100 MHz
Low Frequency Voltage Gain	> 20 dB
Voltage Swing	> 0.7 V
Load Capacitance (C_L)	100 fF
P_{diss}	< 1 mW

III. Hand Analysis

A. Parameters

In order to perform the DC analysis & the AC analysis using the square-law equations & the small-signal transistor models, some parameters are needed to be determined.

Approximate values for the parameters K (where K = $\mu.C_{ox}$), V_{th} (where V_{th} is the threshold voltage) & λ (where λ is the channel length modulation factor) are obtained from the I_D-V_{DS} & the I_D-V_{GS} curves from assignment 1. The values for the parasitic capacitances are needed for the small-signal AC modeling of the circuit & are obtained

from the technology files. The approximate values used are shown in Table II.

TABLE II
PARAMETERS' VALUES USED FOR HAND ANALYSIS

Parameters	Values	
	NMOS	PMOS
K	38.16 µA/V^2	13.74 µA/V^2
V_{th}	260 mV	-280 mV
λ	3.345 V^{-1}	3.913 V^{-1}
C_{gs}	~3 aF	~3 aF
C_{gd}	~1 aF	~1 aF
C_{ds}	~1 aF	~1 aF

B. DC Quiescent points

The main goal of the DC analysis is to bias the transistors such that they operate in the right regions. For the circuit to work as an amplifier, the transistors must operate in the saturation region.

The bias voltages, V_{bp} & V_{bn}, are adjusted to provide biasing to Q_2 & Q_1 respectively, & also to control the available voltage swing for the output. These bias voltages can be controlled by Q_3 with R_1 & by Q_4 with R_2 respectively. The transistors Q_1 & Q_2 are chosen to provide the suitable g_m that has a direct impact on the voltage gain, & to ensure that the Q-point of the output node is about half of the supply voltage.

In each of the three branches of the circuit, the current is described by the square-law equations, shown in equation (1) for NMOS & equation (2) for PMOS.

$$I_{Dn} = \mu_n C_{ox} (W/L) (V_{GS}-V_{thn})^2 (1+ \lambda(V_{DS}-V_{eff})) \quad (1)$$

$$I_{Dp} = \mu_p C_{ox} (W/L) (V_{SG}-|V_{thp}|)^2 (1+ \lambda(V_{SD}-V_{eff})) \quad (2)$$

C. AC small-signal model

The AC analysis is conducted by first replacing each transistor with its small-signal model, then finding the equations of the voltage gain & the bandwidth. The approximate values for the low-frequency voltage gain & the 3dB bandwidth can be found by using equations (3) & (4), respectively. As seen from these equations, to control the gain & the bandwidth, the sizes of Q_1 & Q_2 are modified. By increasing $(W/L)_1$, g_{m1} can be increased, & by decreasing (W/L), r_{ds} can be increased for either of Q_1 & Q_2.

$$A_{vo} \approx g_{m1} (r_{ds1} \| r_{ds2}) \quad (3)$$

$$\omega_{p1} \approx 1/ (C_L (r_{ds1} \| r_{ds2})) \quad (4)$$

IV. SIMULATION & RESULTS

After hand analysis, initial values for the sizes of the transistors are obtained & are plugged into the schematic drawn on Cadence Virtuoso. These values are modified during simulations till the wanted specs are met.

The final sizes chosen for this circuit are shown in Table III. The sizes of transistors are defined by *m*, which is the number of transistors in parallel, instead of (W/L), because in this technology, to increase the equivalent (W/L), more transistors are placed in parallel.[3] Finally, the values of the resistances used are R_1 = 50 KΩ & R_2 = 10 KΩ.

TABLE III
TRANSISTOR SIZES

Transistor	Type	m
Q_1	NMOS	9
Q_2	PMOS	32
Q_3	PMOS	52
Q_4	NMOS	76

A. DC Analysis

The DC analysis is performed to make sure of the biasing points & that all transistors are operating in saturation. That is done by checking the node voltages, then modifying the sizes & rerunning the simulation again if needed.

The branches for transistors Q_3 & Q_4 are designed to provide biasing voltages, V_{bp} = 0.58V & V_{bn} = 0.4V, so that the overdrive voltages on both Q_1 & Q_2 would be 0.14V each, resulting in an output voltage swing of 0.72V according to equation (5).

$$V_{swing} = V_{DD} - V_{SD2,min} - V_{DS1,min} \quad (5)$$

Fig. 2 shows a plot drawn by sweeping the input voltage from -150mV to 150mV. The V_{out} VS V_{input} plot shows an almost linear relationship between the output & input when the output swing is about 0.72V around a DC value of about 0.5V.

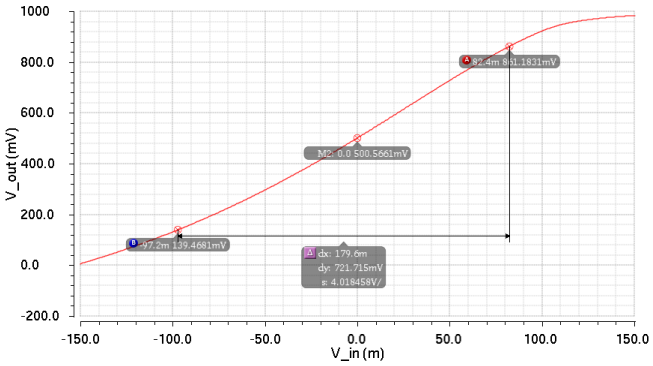

Fig. 2. V_{out} VS V_{input} plot

The dissipated power is also calculated using the DC analysis by multiplying the supply voltage with the total current drawn by the three branches. The total power dissipated by this circuit is 77.78uW.

B. Transient Analysis

For the transient analysis, an AC source is used at the input terminal. In Fig. 3, the output is drawn against time while applying an input of amplitude 1mV & frequency 100MHz. The resulted output has a peak value of about 24mV, which means the gain is equal to 24, which is also equivalent to 27.6dB.

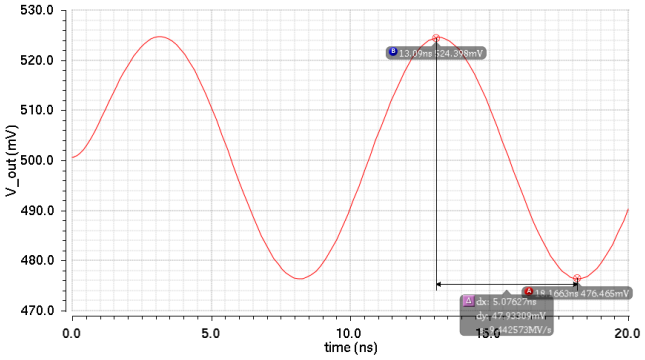

Fig. 3. V_{out} VS time plot, with an input of amplitude 1mV & frequency 100MHz

C. AC Analysis

From the AC analysis on the ADE, the gain & the phase of the transfer function of the circuit are observed across the frequency spectrum, as shown in Fig. 4 & 5, respectively. The low frequency voltage gain is 28.5dB & the 3dB bandwidth is 216.27MHz.

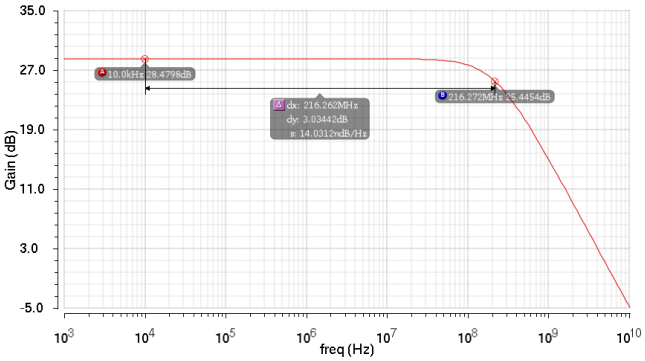

Fig. 4. Gain (in dB) VS frequency

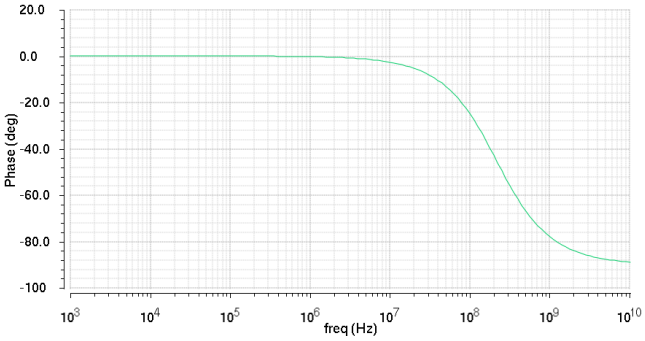

Fig. 5. Phase (in degrees) VS frequency

D. Results

The final results achieved by the circuit are shown in Table IV.

TABLE I
THE CG AMPLIFIER DESIGN SPECS

Specifications	Values
3-dB Bandwidth	216.72 MHz
Low Frequency Voltage Gain	28.48 dB
Voltage Swing	0.72 V
P_{diss}	77.78 uW

V. CONCLUSION

The main idea in designing an analog circuit & choosing the sizes of the transistors is to perform the hand analysis first to obtain the equations that give us an understanding of how the different parts of the circuit interact with each other, then using the simulations, the exact sizes of the transistors can be determined.

This document studied the behavior of the common gate amplifier circuit & discussed the steps of thinking used to design an analog circuit to meet certain design specs. The same basic steps & concepts will be applied when designing other analog circuits.

REFERENCES

[1] B. Razavi, “Design of Analog CMOS Integrated Circuits”, Boston: McGraw-Hill, 2001.

[2] S. Hamedi-Hagh and A. Bindal, “Spice Modeling of Silicon Nanowire Field-Effect Transistors for High-Speed Analog Integrated Circuits,” IEEE Transactions On Nanotechnology, Vol. 7, No. 6, November 2008.

[3] A. Bindal and S. Hamedi-Hagh, “Silicon Nanowire Transistors”, Springer, 2016.