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# Analog Design Experiments With AI—Part 1

With the rapid rise of artificial intelligence (AI) in various fields, we naturally wonder whether it can help or even replace analog designers. In this article series, we embark upon a sequence of experiments with ChatGPT that explore this possibility.

## Study Framework

As with any training, our first task is to assess the trainee's background knowledge. In this first article, therefore, we wish to evaluate ChatGPT's *present* capabilities and, specifically, probe the depth of its conceptual understanding beyond what it can readily find from online resources. Our experiments proceed at the undergraduate level, assuming that someone with a bachelor's degree has completed a series of analog circuits courses and has now turned to ChatGPT for assistance.

To quantify our results, we assign a score between 0 and 4 to ChatGPT's answers. Also, to avoid skewing the evaluation, no feedback is given to ChatGPT. Note that ChatGPT, by default, assumes square-law MOS devices. In this first article, we focus on only one- or two-transistor circuits.

## ChatGPT Interface

The nature of our experiments is partly constrained by ChatGPT's interface limitations. We can enter questions as text or as images. The former confines us to simple queries, offering little assistance with

detailed analysis and design. The latter proves more versatile and will be used extensively in our studies.

ChatGPT's output interface also presents certain challenges. Beyond text and equations, it can plot some parameters based on assumed component values, but it does not produce easy-to-read circuit schematics. ChatGPT also informs us that it cannot perform circuit simulations, a severe impediment to developing intuition, optimizing performance, and dealing with complex designs.

## Basic Questions

**Q1:** If we double the length and width of a MOSFET, what happens to its intrinsic gain?

**ChatGPT:**  $A_I = g_m r_o$ ,  $g_m \propto \sqrt{W/L}$ ,  $r_o \propto L$ ; thus,  $g_m r_o$  is doubled.

**Comments:** This answer is correct if the overdrive voltage is assumed constant; the drain current and  $g_m$  remain unchanged while  $r_o = 1/(\lambda I_D)$  is doubled. Score: 4

**Q2:** Student A says the transconductance of a MOSFET goes up as the overdrive voltage increases. Student B says it goes down. Who is correct?

**ChatGPT:**  $g_m = \mu_n C_{ox} (W/L) V_{ov} = 2I_D/V_{ov}$ . At fixed  $V_{ov}$ , a larger  $V_{ov}$

yields a larger  $g_m$ . At fixed  $I_D$ , increasing  $V_{ov}$  makes  $g_m$  go down.

**Comments:** The first part of the answer is incorrect as it assumes that  $V_{ov}$  is fixed, but it becomes larger! The correct answer is that if  $(W/L)$  is fixed, then increasing  $V_{ov}$  yields a larger  $g_m$ . Score: 2

**Q3:** Is the small-signal model of a PMOS device identical to that of an NMOS device?

**ChatGPT:** Yes.

**Comment:** The answer is correct. Score: 4

## One-Transistor Circuits

**Q4:** Sketch  $I_X$  versus  $V_X$  in the circuit in Figure 1.

**ChatGPT:** For  $V_X \leq V_{TH}$ ,  $I_X \approx 0$ . For  $V_X > V_{TH}$ ,  $I_X$  rises quadratically with  $V_X$ .

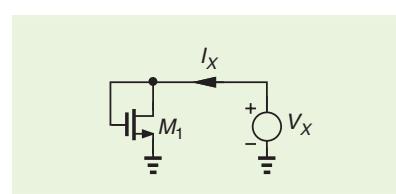
**Comment:** The answer is correct. Score: 4

**Q5:** Sketch  $I_X$  versus.  $V_X$  in the circuit of Figure 2.

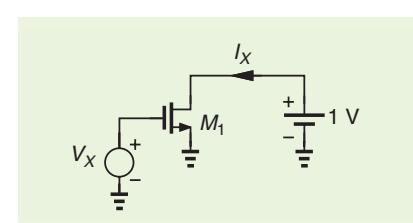
**ChatGPT:** For  $V_{TH} < V_X < V_{TH} + 1 \text{ V}$ ,  $I_X$  rises quadratically. For  $V_X > V_{TH} + 1 \text{ V}$ , it transitions to a straight line.

**Comment:** This answer is correct. Score: 4

**Q6:** Can the device shown in Figure 3 act as a current source?



**FIGURE 1:** ChatGPT correctly predicts the behavior of  $I_X$ .



**FIGURE 2:** ChatGPT correctly predicts the behavior of  $I_X$ .

**ChatGPT:** Yes, it can act as a current source. The device is an NMOS transistor with its gate shorted to its drain and called a *diode-connected MOSFET*.

**Comments:** ChatGPT makes two mistakes here. First, it does not realize that the device presents a low impedance. Second, it thinks that the device is an NMOS transistor. As seen later, ChatGPT does recognize the PMOS symbol in other contexts. Interestingly, it correctly identifies the structure as a diode-connected topology, and yet it believes that it makes a good current source. Score: 0

**Q7:** Analyze the circuit shown in Figure 4.

**ChatGPT:** Transistor  $M_1$  is an NMOS device whose source is connected to  $R_S$ .  $A_v = -g_m R_D / (1 + g_m R_S)$ .

**Comments:** Again, ChatGPT confuses PMOS and NMOS devices. Score: 1

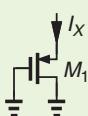
**Q8:** Analyze the circuit shown in Figure 5.

**ChatGPT:** This is a source follower.  $A_v = g_m R_S / (1 + g_m R_S)$ .

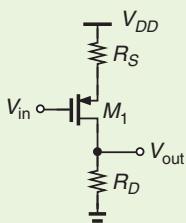
**Comments:** The answer is correct. We will see, however, that a slight modification confuses ChatGPT. Score: 4

**Q9:** Analyze the circuit shown in Figure 6.

**ChatGPT:** This is a common-source amplifier. The input is applied to the gate.



**FIGURE 3:** ChatGPT incorrectly explains that this configuration acts as a good current source



**FIGURE 4:** ChatGPT incorrectly identifies  $M_1$  as an NMOS device.

**Comments:** The answer is incorrect. Strangely, ChatGPT believes that the input is tied to the gate. Score: 0

**Q10:** Analyze the circuit shown in Figure 7.

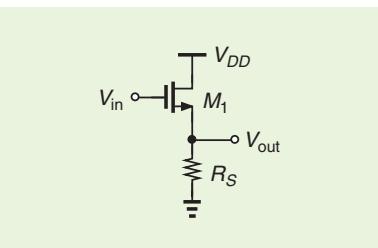
**ChatGPT:** This is a common-gate amplifier. The input is applied at the source (through  $C_1$ ).  $A_v \approx g_m R_D$ .

**Comments:** ChatGPT does identify the topology correctly, but it is oblivious to the short between the source and ground. Score: 1

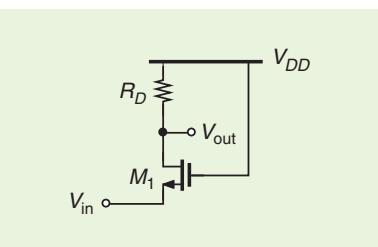
**Q11:** How many poles does the circuit of Figure 8 have?

**ChatGPT:** There are two independent energy-storing nodes. Thus, the circuit has two poles.

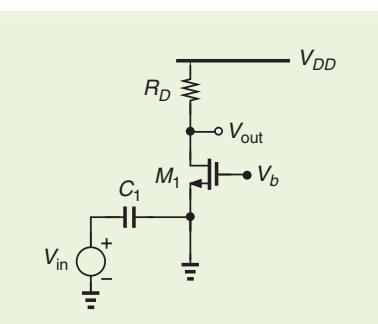
**Comments:** The answer is correct. However, energy storage should be attributed to devices rather than to nodes. Score: 3



**FIGURE 5:** ChatGPT correctly analyzes this source follower.



**FIGURE 6:** ChatGPT incorrectly calls this topology a common-source stage.



**FIGURE 7:** ChatGPT ignores the short from the source of  $M_1$  to ground.

**Q12:** Analyze the circuit shown in Figure 9.

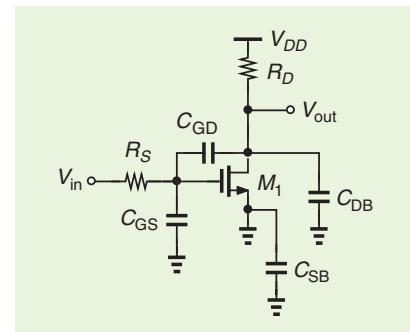
**ChatGPT:**  $M_1$ : NMOS, source at ground.  $R_1-R_2$ : Resistor divider at output. The circuit has negative feedback.

**Comments:** The answer is mostly correct, except that ChatGPT believes that the source of  $M_1$  is grounded. Score: 3

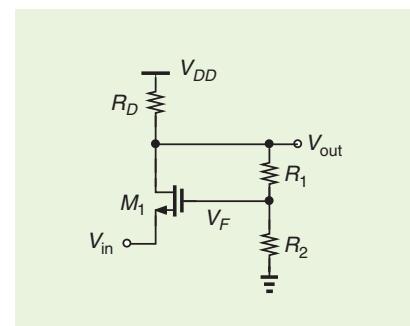
## Two-Transistor Circuits

**Q13:** Analyze the circuit shown in Figure 10.

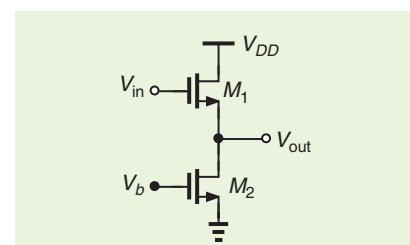
**ChatGPT:**  $M_1$  (NMOS) acts as the main amplifying transistor.  $M_2$



**FIGURE 8:** ChatGPT correctly predicts the number of poles in this circuit.



**FIGURE 9:** ChatGPT correctly explains that this structure includes negative feedback but believes that the source of  $M_1$  is grounded.



**FIGURE 10:** ChatGPT incorrectly identifies this topology as a common-source amplifier.

(NMOS) acts as a current-source load. The circuit is a common-source amplifier with an active load.  $A_v \approx -g_{m1}(r_{o1} \| r_{o2})$ .

**Comments:** The answer is incorrect. Even though this structure is only slightly different from that in Figure 5, ChatGPT does not realize that it is a source follower. Moreover, it lacks the intuition that two NMOS transistors cannot form a common-source stage with an active load. Score: 0

**Q14:** Analyze the circuit of Figure 11(a).

**ChatGPT:** This is the classic CMOS inverter.

**Comments:** The answer is correct, suggesting that ChatGPT recognizes both NMOS and PMOS symbols. Score: 4

**Q15:** Analyze the circuit shown in Figure 11(b).

**ChatGPT:**  $M_1$ : A PMOS transistor;  $M_2$ : An NMOS transistor. This is the CMOS inverter.

**Comments:** The answer is incorrect. While not a useful structure, this example serves to test ChatGPT's conceptual understanding. Evidently, ChatGPT looks for a topology in which the gates of two transistors

are tied to the input signal, concluding that this arrangement must be an inverter. Score: 0

**Q16:** Analyze the circuit of Figure 12.

**ChatGPT:** This is a common-source stage with a diode-connected load.  $A_v = -g_{m1}/(g_{m2} + 1/r_{o2})$ .

**Comments:** The answer is correct. However, ChatGPT decides to include channel-length modulation for  $M_2$  but not for  $M_1$ . Score: 3

**Q17:** Analyze the circuit of Figure 13.

**ChatGPT:** The circuit has two stacked NMOS devices.  $M_2$  acts as a diode-connected load, and  $M_1$  as the amplifying transistor.  $A_v = -g_{m1}/g_{m2}$ .

**Comments:** All parts of the answer are incorrect. ChatGPT does mention that  $V_{in}$  is applied to the gate of  $M_2$ , but it is confused about the rest of the circuit. Score: 0

**Q18:** Find  $R_{out}$  in Figure 14.

**ChatGPT:** This is a cascaded NMOS current source. Looking into the output node (the drain of  $M_1$ , i.e., the node between  $M_1$  and  $M_2$ ),  $R_{out} = r_{o1} + r_{o2} + g_{m2}r_{o1}r_{o2}$ . Intuition: The cascode device  $M_2$  holds the drain of  $M_1$  nearly constant.

**Comments:** ChatGPT is greatly confused here. In addition to mistaking PMOS devices for NMOS transis-

tors, it believes that  $M_2$  is the cascode device, perhaps because it is drawn above  $M_1$ . The  $R_{out}$  expression follows the same mistake. Score: 0

**Q19:** How do we ensure that  $M_2$  is in saturation in Figure 14?

**ChatGPT:** Treat  $M_2$  as the PMOS device whose source is at  $V_{DD}$ . So we ensure that  $M_2$  is in saturation by choosing  $V_{b2}$  so that  $X$  never rises above  $V_{b2} + |V_{T2}|$ .

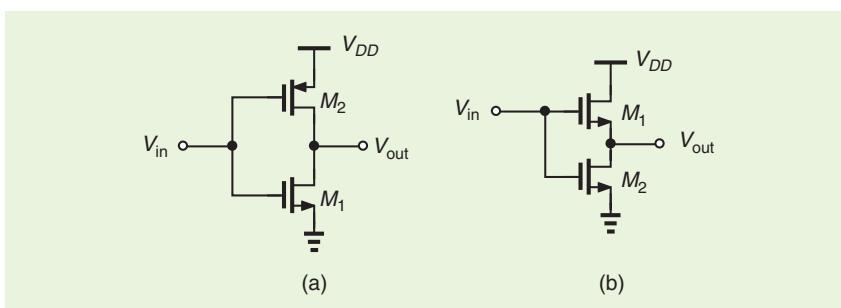
**Comments:** In contrast to the previous question, ChatGPT now identifies at least  $M_2$  as a PMOS device. However, it does not realize that  $V_X$  is primarily controlled by  $V_{b1}$ , i.e.,  $V_{b1}$  must be less than  $|V_{GS2} - V_{TH2}| + |V_{GS1}|$ . Score: 1

**Q20:** Analyze the circuit shown in Figure 15.

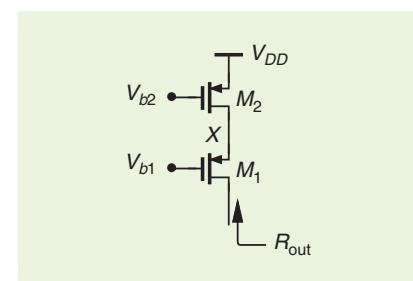
**ChatGPT:** This is a common-source amplifier with an active load.  $M_1$ : NMOS,  $M_2$ : PMOS, with its drain connected to  $X$  and its source to  $V_{out}$ .

**Comments:** The answer is incorrect. Strangely, ChatGPT takes  $M_2$  to be a PMOS device. Even if we accept that, the topology would not qualify as a common-source stage with an active load. Score: 0

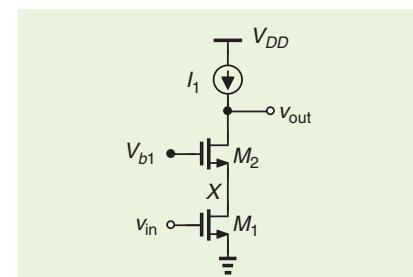
**Q21:** Is the circuit of Figure 16 a cascode structure?



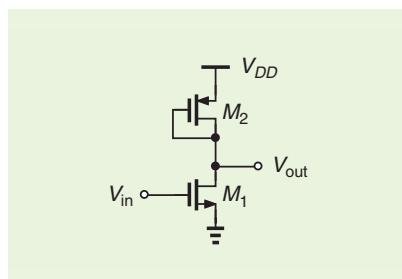
**FIGURE 11:** ChatGPT believes that both of these circuits are CMOS inverters.



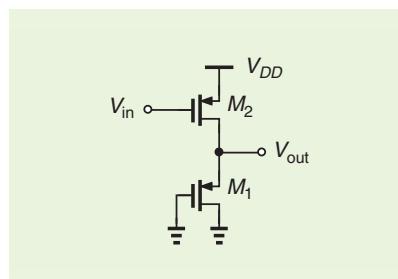
**FIGURE 14:** ChatGPT believes that this is an NMOS cascode.



**FIGURE 15:** ChatGPT incorrectly identifies  $M_2$  as a PMOS device.



**FIGURE 12:** ChatGPT correctly identifies this circuit.



**FIGURE 13:** ChatGPT incorrectly identifies both transistors as NMOS devices.

**ChatGPT:** Yes, this is a cascode structure. The output resistance becomes  $r_{out} \approx g_m r_{O2} r_{O1}$ .

**Comments:** The answer is incorrect. Transistor  $M_1$  acts as a source follower rather than a common-source stage. The output resistance is equal to  $(1 + g_m r_{O2}) / g_m + r_{O2}$ . Score: 0

**Q22:** Explain why the Miller effect is less pronounced in a cascode.

**ChatGPT:** In a cascode, you stack a common-gate device ( $M_2$ ) on top of the common-source device ( $M_1$ ). The drain of  $M_1$  is “clamped” by  $M_2$ , which keeps the voltage at the drain of  $M_1$  relatively constant. So the effective gain across  $C_{gd1}$  is very small.

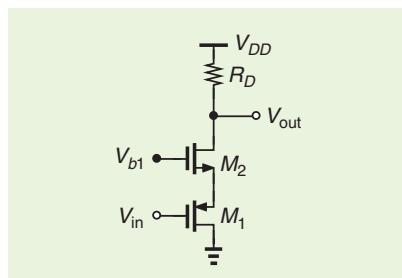
**Comments:** ChatGPT is partially correct. The effective gain across  $C_{gd1}$  is about  $-2$ , hence not very small. Score: 3

**Q23:** Analyze the circuit shown in Figure 17.

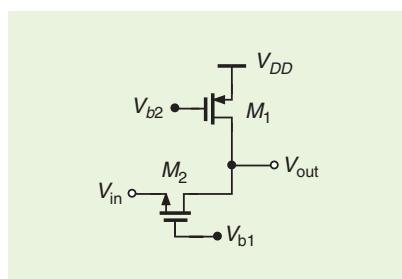
**ChatGPT:**  $M_1$  (PMOS),  $M_2$  (NMOS), its gate receives  $V_{in}$ . This is a common-source amplifier with an active load.  $V_{out} = -g_m r_{O,eq} V_{in}$ .

**Comments:** The answer is incorrect. It is unclear why ChatGPT believes that  $V_{in}$  is applied to the gate of  $M_2$ . Score: 0

**Q24:** How many poles does the circuit of Figure 18 have?



**FIGURE 16:** ChatGPT incorrectly believes that this is a cascode structure.



**FIGURE 17:** ChatGPT calls this circuit a common-source amplifier.

**ChatGPT:** Two poles as there are two independent energy-storing nodes. The output node contains  $C_{GS2}$  (to the ac-grounded gate of  $M_2$ ), etc.

**Comments:** The number of poles is correct. However,  $C_{GS2}$  does not appear at the output node. Score: 3

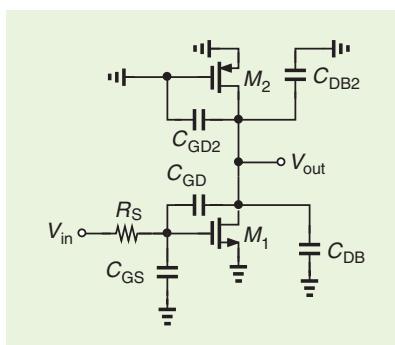
**Q25:** Analyze the circuit shown in Figure 19.

**ChatGPT:** Response 1: This is a two-NMOS series transistor with a resistive load. This is a differential-style cascode, sometimes called a *gain-boosting stage*.  $A_v = -g_m(r_{O1} \| r_{O2} \| R_D)$ . Response 2:  $M_2$  is a diode-connected NMOS. This is the classic NMOS differential amplifier’s “half-circuit.”

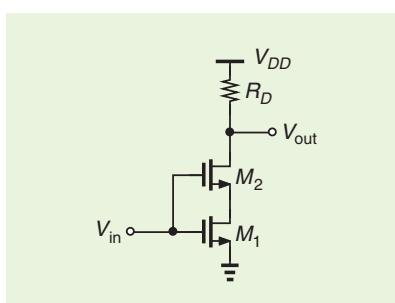
**Comments:** Both answers are incorrect and indicate great confusion. If  $M_1$  and  $M_2$  are identical, this structure is equivalent to a single transistor having twice the channel length. This topology is commonly used today in FinFET technologies if a longer channel is desired. Score: 0

**Q26:** Analyze the circuit of Figure 20.

**ChatGPT:**  $M_1$ : NMOS with its gate driven by  $V_{in}$ ,  $M_2$ : NMOS used as an



**FIGURE 18:** ChatGPT correctly predicts the number of poles in this circuit but believes that  $C_{GS2}$  is tied to the output.



**FIGURE 19:** ChatGPT calls this topology a differential-style cascode or a gain-boosting stage.

active load/current mirror transistor. This is a common-source amplifier with an NMOS cascode.

**Comments:** The answer is incorrect and not even consistent. This arrangement can be viewed as a source follower,  $M_1$ , driving a common-gate stage,  $M_2$ . Score: 0

**Q27:** Explain why the output impedance of the circuit shown in Figure 21 can be inductive.

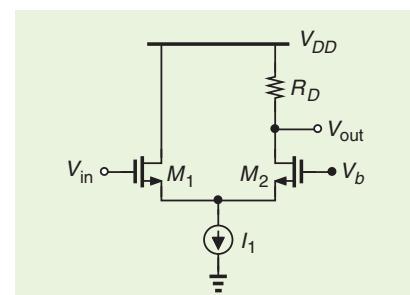
**ChatGPT:** This is a cascode circuit with source degeneration at the input. Looking into the drain of  $M_2$ ,  $Z_{out} \approx g_m R_s / (sC_{gs1})$ . The gate-source capacitance of  $M_1$  combined with  $R_s$  creates a phase shift. After being “buffered” by the cascode transistor,  $M_2$ , this combination mimics an inductor.

**Comments:** The answer is mostly incorrect. The intuition is that  $Z_{out}$  is equal to  $1/g_m$  at very low frequencies and  $R_s$  at very high frequencies (as  $C_{gs1}$  shorts the gate and the source). Score: 2

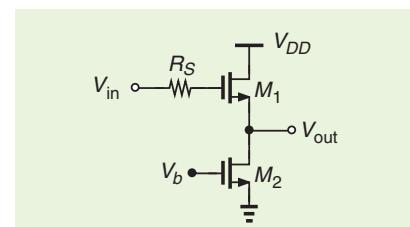
**Q28:** Analyze the circuit shown in Figure 22.

**ChatGPT:**  $M_1$ : NMOS, common-source stage;  $M_2$ : NMOS, diode-connected (its gate and drain are shorted at  $X$ ). The input is a current source.

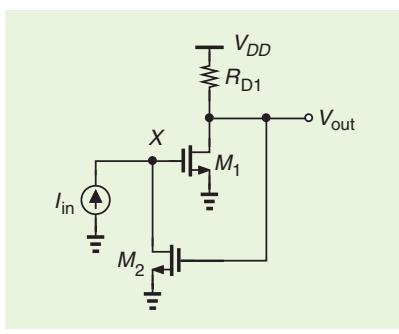
**Comments:** ChatGPT fails to realize that the gate of  $M_2$  is tied to the



**FIGURE 20:** ChatGPT calls this arrangement a common-source amplifier with an NMOS cascode.



**FIGURE 21:** ChatGPT calls this structure a cascode circuit with source degeneration.



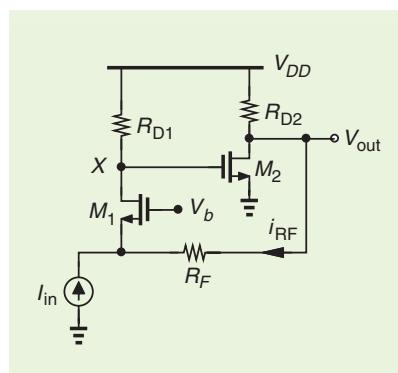
**FIGURE 22:** ChatGPT believes that  $M_2$  is a diode-connected device.

output. As a result, it ignores the (positive) feedback loop around the circuit. Score: 1

**Q29:** Analyze the circuit of Figure 23.

**ChatGPT:**  $M_1$ : NMOS, with gate at  $X$ ;  $M_2$ : NMOS, gate biased at constant  $V_b$ ;  $R_F$ : Feedback resistor.  $M_1$  converts the source voltage into a drain current.  $M_2$  is a common-source amplifier with fixed gate bias  $V_b$ .

**Comments:** ChatGPT is confused about the connections of  $M_1$  and  $M_2$ . The statement " $M_2$  is a common-



**FIGURE 23:** ChatGPT believes that the gate of  $M_1$  is tied to  $X$ .

source amplifier with fixed gate voltage" is self-contradictory. Score: 2

**Q30:** Analyze the circuit shown in Figure 24.

**ChatGPT:**  $M_1$ : NMOS; acts as a cascode transistor.  $M_2$ : NMOS, with the gate tied to the input, operates as the amplifying device.

**Comments:** The answer is incorrect. Also, ChatGPT fails to see the feedback loop. Score: 0



**FIGURE 24:** ChatGPT incorrectly identifies  $M_1$  as an NMOS device.

## Overall Assessment

Adding up the scores, we obtain a total of 49 out of 120 points, i.e., 41%, as ChatGPT's performance in this evaluation. We also observe that ChatGPT exhibits a poorer performance with two-transistor circuits than with one-transistor topologies. More serious, though, is ChatGPT's inconsistent, flawed conceptual understanding as the structures begin to depart from those available in online resources. **SSC**

## EDITOR'S NOTE (continued from p. 5)

current continuity even in regions without physical charge transport. Behzad's "The Analog Mind" column [A8] begins a new series exploring whether AI tools could one day take over the field of analog design. Chris' "Shop Talk" column [A9] examines active feedback amplifiers—circuits that place active devices in the feedback path—and explains their properties and advantages. Farhana's "Circuits From a System Perspective" column [A10] explores how tiny MEMS devices make motion sensing possible in everyday technologies.

The goal of the magazine continues to be to provide Society news and information as well as a series of self-contained resources to keep SSCS members up-to-date with changes in technology while, at the same time, providing reviews of circuit design concepts. This includes contributions from experts describing the current state of affairs and the

evolution of a particular IC technology. We will also continue to feature articles focused on the contributions of luminaries and solid-state circuit techniques and directions.

We hope you enjoy reading *IEEE Solid-State Circuits Magazine*. Please send comments to me at lbelosto@ieee.org.

## Appendix: Related Articles

- [A1] A. Whitcombe, "Time-domain versus voltage-domain data conversion: Principles, opportunities, and challenges," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 28–38, Fall 2025, doi: [10.1109/MSSC.2025.3596052](https://doi.org/10.1109/MSSC.2025.3596052).
- [A2] H. Liu et al., "Harnessing memory technology innovations for on-device large language models in augmented reality SoCs: Cooptimizing system architecture with model characteristics," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 39–46, Fall 2025, doi: [10.1109/MSSC.2025.3596910](https://doi.org/10.1109/MSSC.2025.3596910).
- [A3] F. Sheikh et al., "Chiplets everywhere! Opportunities and challenges," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 47–61, Fall 2025, doi: [10.1109/MSSC.2025.3615124](https://doi.org/10.1109/MSSC.2025.3615124).
- [A4] N. Ebrahimi et al., "Toward spectrally efficient and physically reconfigurable architectures for multibeam-waveform co-
- [A5] V. B. Suresh and S. K. Mathew, "Blockchains: An overview of the technology, circuit primitives, and future opportunities," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 79–92, Fall 2025, doi: [10.1109/MSSC.2025.3595831](https://doi.org/10.1109/MSSC.2025.3595831).
- [A6] Z. Xu and N. Li, "Multibeamformer ICs for phased arrays: Enabling spatial multiplexing communication and sensing," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 93–103, Fall 2025, doi: [10.1109/MSSC.2025.3610331](https://doi.org/10.1109/MSSC.2025.3610331).
- [A7] A. Sheikholeslami, "Current without electrons [Circuit Intuitions]," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 8–10, Fall 2025, doi: [10.1109/MSSC.2025.3612805](https://doi.org/10.1109/MSSC.2025.3612805).
- [A8] B. Razavi, "Analog design experiments with AI—Part 1 [The Analog Mind]," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 11–15, Fall 2025, doi: [10.1109/MSSC.2025.3611213](https://doi.org/10.1109/MSSC.2025.3611213).
- [A9] C. Mangelsdorf, "Active feedback amps [Shop Talk: What You Didn't Learn in School]," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 16–24, Fall 2025, doi: [10.1109/MSSC.2025.3610791](https://doi.org/10.1109/MSSC.2025.3610791).
- [A10] F. Sheikh, "Microscale marvels for motion sensing [Circuits From a System Perspective]," *IEEE Solid-State Circuits Mag.*, vol. 17, no. 4, pp. 25–27, Fall 2025, doi: [10.1109/MSSC.2025.3613800](https://doi.org/10.1109/MSSC.2025.3613800).

**SSC**