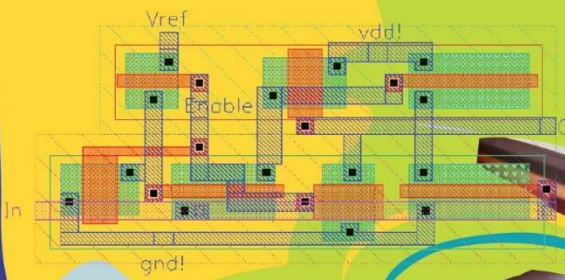
Logical Effort

Advanced Digital IC Design



Lecture

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Khosrow Ghadiri

- Logic effort is an assignment of a number to logic gate to describe the drive strength (current) of the gate relative to that of a reference inverter.
- A logic gate is characterized by:
  - Logical effort
  - Parasitic delay
- Logic effort definitions:
- ❶ Measure of how much worse the gate ability to deliver output current compare with an inverter with identical input capacitance
- ❷ The ratio of gate input capacitance to that of an inverter which deliver equal output current.
- ❸ The slope of the gate input capacitance vs. fanout curve divided by the slope of an inverter delay vs. fanout curve

- The Logical effort of an input group g_A

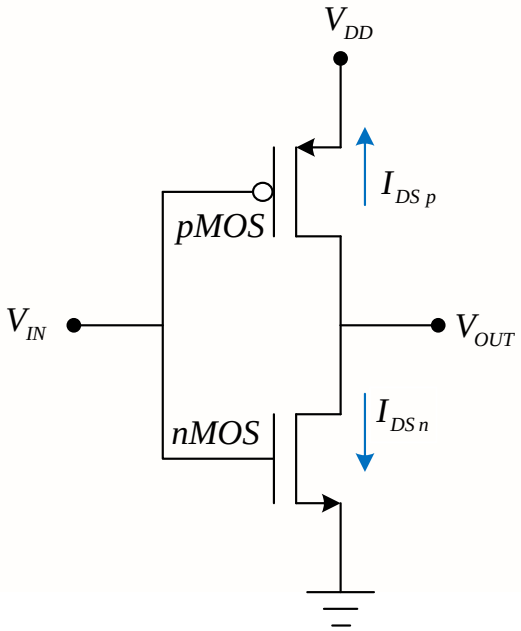
$$g_A = \frac{C_A}{C_{inv}} = \frac{\sum_i^A C_i}{C_{inv}}$$

- The capacitance C_A is combined input capacitive of every signal in the input group A.
- The capacitance C_{inv} is input capacitance of inverter designed to have the same drive capability of the digital gate.
- Assumption: mobility of pMOS is half of the nMOS

$$\gamma = \mu = \frac{\mu_n}{\mu_p}$$

- Capacitance is proportional to the width W.
- The conductance is proportional to the width W.

- The Inverter input low and output high.
- The mobility of pMOS is half of nMOS.
- Pullup input capacitance of an inverter is proportion to $2W$
- Pulldown input capacitance of an inverter is proportion to W
- Total input capacitance of an inverter is proportion to $3W$



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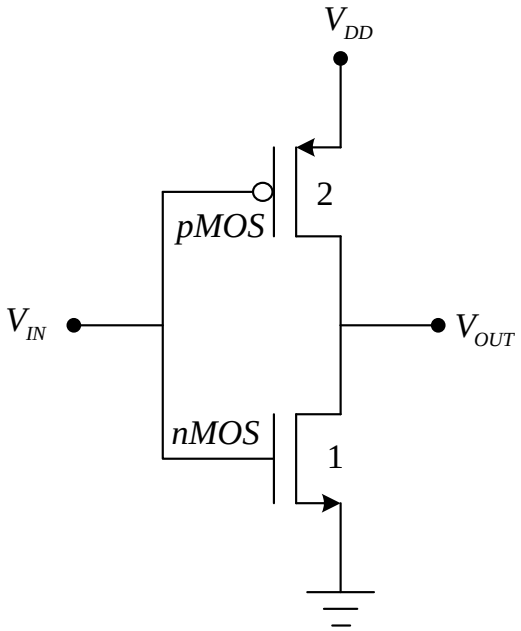
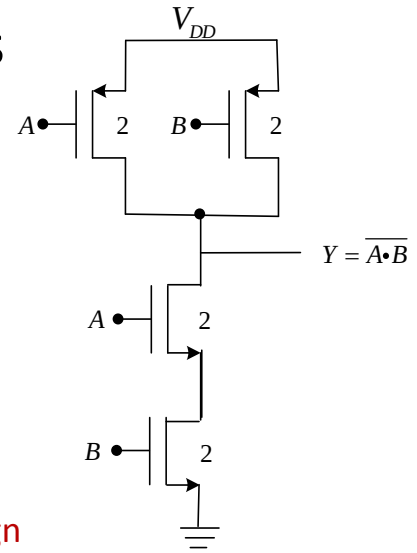


- The 2-input NAND gate with two inputs low and output high.
- The mobility of pMOS is half of nMOS.
- Pullup input capacitance of an inverter is proportion to $2W$
- Pulldown input capacitance of an inverter is proportion to $2W$
- the input capacitance of one input signal of 2-input NAND gate is proportion to the sum of the width of pullup transistors and pulldown transistors $2W + 2W = 4W$
- Total input capacitance of an inverter is proportion to $3W$
- The two pulldown transistors are in series
- The two pullup transistors are in parallel
- The logical effort $g_{NAND} = \frac{C_{NAND}}{C_{inv}} = \frac{4}{3}$



- The 2-input NOR gate with two inputs low and output high.
- The mobility of pMOS is half of nMOS.
- Pullup input capacitance of an inverter is proportion to $2W$
- Pulldown input capacitance of an inverter is proportion to $2W$
- the input capacitance of one input signal of 2-input NOR gate is proportion to the sum of the width of pullup transistors and pulldown transistors $W + 4W = 5W$
- Total input capacitance of an inverter is proportion to $3W$
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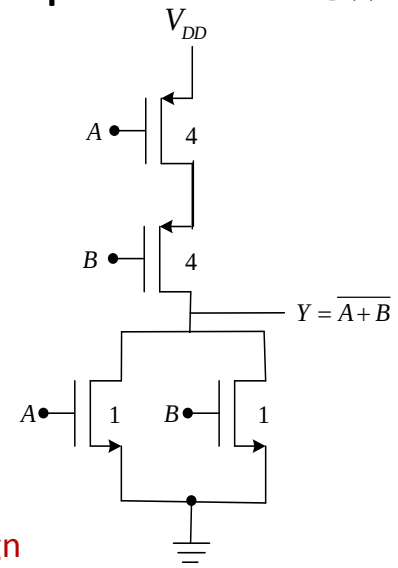

- The logical effort $g_{NOR} = \frac{C_{NOR}}{C_{inv}} = \frac{5}{3}$

- Normalized delay:

$$d = f + p$$

- Stage effort (f) depends on the load
- Intrinsic delay (p) of the logic gate
- Stage effort (f)
  - Logical effort (g)

$$g = \frac{C_{gate}}{C_{inv}}$$

  - Electrical effort (h)

$$h = \frac{C_{\text{in of load}}}{C_{\text{in of inv}}}$$

- Stage effort

$$f = gh$$

- Multistage logic network:
- Normalized path delay

$$D = NF^{\frac{1}{N}} + P$$

- Parasitic path delay P.
- Path logical effort G(the productof the individual logical effors of the gates.
- Path electrical effort H is the ratio of th load of the path to its input.

$$F = GH$$

- Path branching effort B is product of individual path effort.

$$F = GHB$$

- Minimum delay:

$$f = F^{\frac{1}{N}}$$

- Number of stage N.
- Total normalized delay of an inverter

$$d = gh + p = (1)(1) + 1 = 2$$

- Normalized parasitic delay of 2-input NAND gate

$$d = gh + p = \left(\frac{4}{3}\right)(1) + 2 = \frac{10}{3}$$

- Normalized parasitic delay of 2-input NOR gate

$$d = gh + p = \left(\frac{5}{3}\right)(1) + 2 = \frac{11}{3}$$

- Logic Gates

Gate Type	Logic Effort	Formula	$n=2$ $\gamma=2$	$n=3$ $\gamma=2$	$n=4$ $\gamma=2$
NAND	Total	$\frac{n(n+\gamma)}{1+\gamma}$	$\frac{8}{3}$	5	8
	per input	$\frac{(n+\gamma)}{1+\gamma}$	$\frac{4}{3}$	$\frac{5}{3}$	2
NOR	Total	$\frac{n(n+\gamma)}{1+\gamma}$	$\frac{10}{3}$	7	12
	per input	$\frac{(n+\gamma)}{1+\gamma}$	$\frac{5}{3}$	$\frac{7}{3}$	3

- Logic Gates

Gate Type	Logic Effort	Formula	$n=2$ $\gamma=2$	$n=3$ $\gamma=2$	$n=4$ $\gamma=2$
XOR XNOR	Total	$n^2\left(2^{n-1}\right)$	8	36	128
	per boundle	$n\left(2^{n-1}\right)$	4	12	32
MUX	Total	$4n$	8	12	16
	d, s*	2, 2	2, 2	2, 2	2, 2