University of California
College of Engineering
Department of Electrical Engineering
and Computer Sciences

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WeFr 2-3:30pm

Fr, February 19, 6:30-8:00pm

EECS 141: SPRING 10—MIDTERM 1

NAME	Last First

SID	

Problem 1 (15):

Problem 2 (12):

Problem 3 (15):

Total (42)	

[PROBLEM 1] CMOS NON-INVERTING BUFFER (15 pts)

The following circuit can be seemed as a “DIGITAL NON-INVERTING BUFFER”.

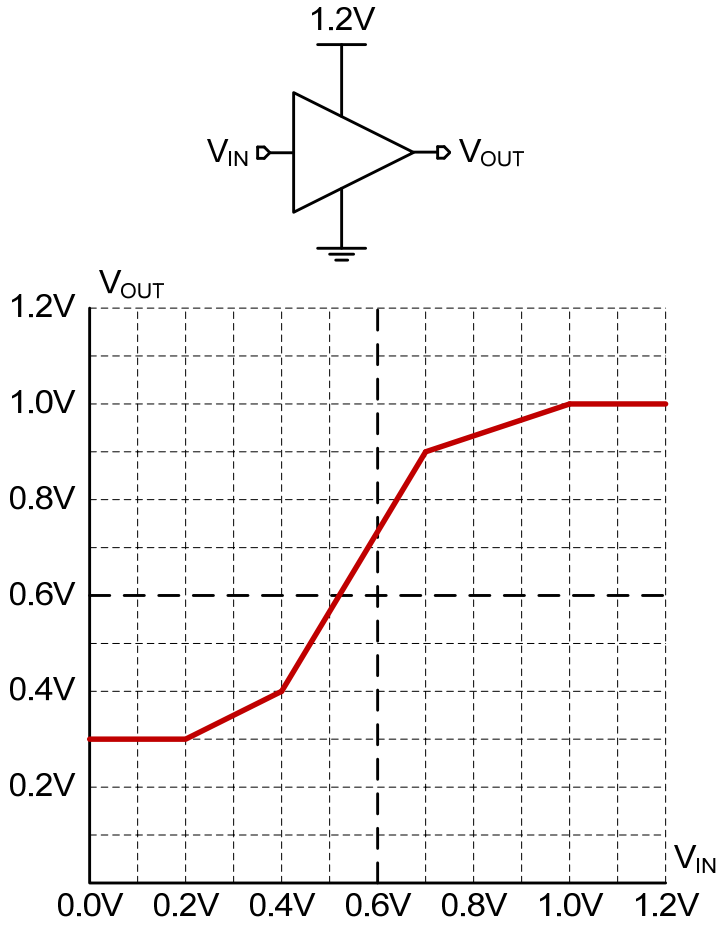


Fig.1 (a) DIGITAL BUFFER & VTC

(a) (3pts) Compute V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H.

(i) V_{IL}	**=**
(ii) V_{IH}	**=**
(iii) V_{OL}	**=**
(iv) V_{OH}	**=**
(v) NM_L	**=**
(vi) NM_H	**=**

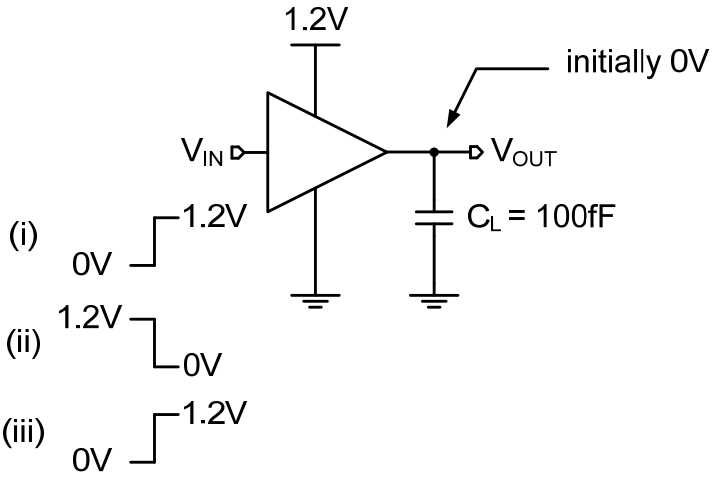


Fig.1 (b) One-stage DIGITAL BUFFER with 100fF C_L

(b) (6pts) For Fig.1.(b), the output voltage, V_{OUT}, is initially discharged, V_{OUT}=0. You may ignore the intrinsic capacitance, or diffusion capacitance, of the buffer.
Find the energy dissipated in the buffer during the first 0 to 1.2V step input (i), **First E_{DISS}**.
Then, after the output reaches its final value, a 1.2V to 0 step is applied to the input (ii). Find the energy dissipated in the buffer, **Second E_{DISS}**.
A second 0 to 1.2V step follows (iii). Find again the energy dissipated in the buffer (**Third E_{DISS}**).

(i) 1st E_{DISS} =
(ii) 2nd E_{DISS} =
(iii) 3rd E_{DISS} =

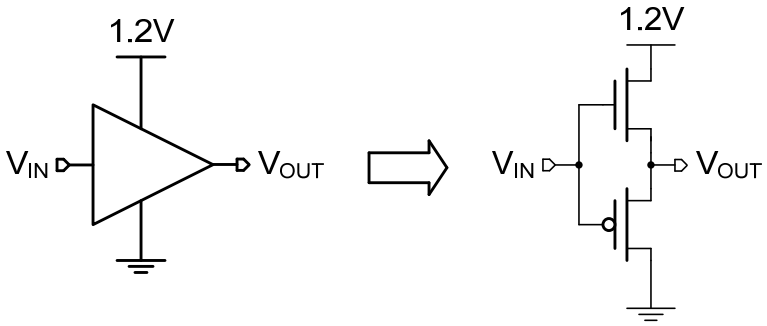
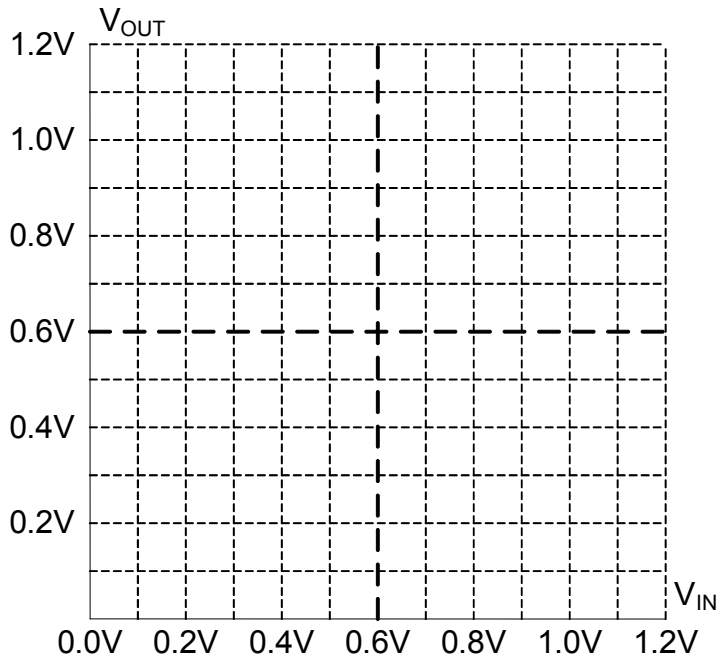


Fig.1 (c)

(c) (4 pts) One engineer tried to develop a transistor-level implementation of the buffer as shown in Fig.1(c). Draw the VTC of the circuit where VIN goes from 0V to 1.2V and then goes back to 0V. Here, the $V_{TN}=|V_{TP}|=0.2V$, R_{OFF}=inf., and no body effect, that is the threshold voltage is not dependent upon the voltage of the body.



(d) (2pts) Can the gate of Fig 1.c still be considered a digital gate (or, is it still regenerative)? Explain in a couple of words why or why not.

[PROBLEM 2] RING OSCILLATOR (12pts)

Consider the 5-stage ring oscillator shown in Fig.2a, which is used to generate a clock signal. The input gate capacitance of a minimum-sized inverter (size=1) is C_{IN}=10fF, while $R_{ON,N}$=$R_{ON,P}$=7.22kΩ, and R_{OFF}=inf. Assume that the input capacitance is proportional to its size, and R_{ON} is inversely proportional to its size. The diffusion capacitance, or intrinsic capacitance, of inverter is the same as the gate capacitance, γ=1. Ignore resistance and capacitance of the wires between the inverters.

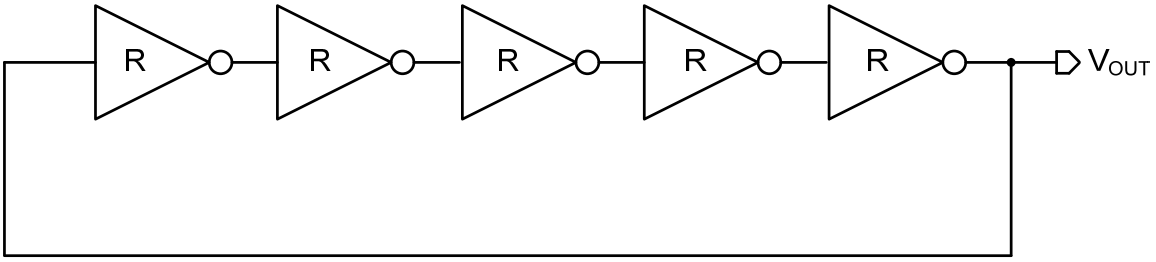
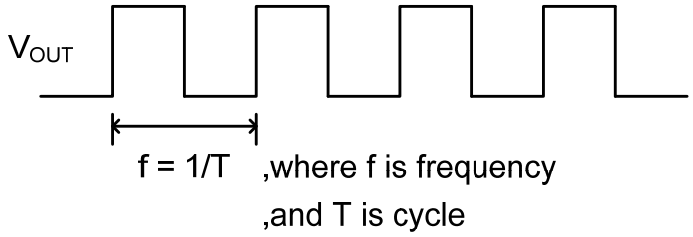


Fig.2 (a) 5-stage Ring Oscillator

(a) (6pts) Determine the oscillation frequency of this circuit at V_{OUT} for R=1 (that is, using unit inverters). Determine also the power dissipation of the circuit P_{SUPPLY} for VDD = 1.2V. You should take into account the gate and diffusion capacitances.



f =
P_{SUPPLY} =

(b) (6pt) Determine the oscillation frequency of ring oscillator and as well as the power dissipation, when the inverters are sized at R=2, R=4, and R=8, respectively. Please normalize your results with respect to $f_{R=1}$ and $P_{SUPPLY,R=1}$.

R	$f_R / f_{R=1}$	$P_{SUPPLY,R} / P_{SUPPLY,R=1}$
2		
4		
8		

[PROBLEM 3] COMPLEX LOGIC AND LOGICAL EFFORT (15 pts)

(a) (2pts) Implement the logic function $F = \overline{A \cdot B + C}$ by using a complex static CMOS Gate. Place the PMOS and NMOS driven by input A closest to the output node, F, in your transistor stacks.

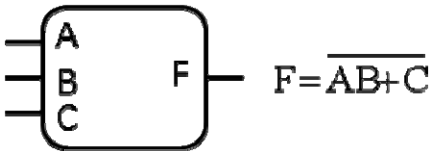


Fig.3 (a) Complex Gate

(b) (3pts) The unit inverter is shown in Fig. 3(b). Assume that C_D=C_G =2fF/μm. Size the *transistors of the complex gate in (a) such that the worst cast driving strength for all inputs is the same as a unit inverter. Give the width of all transistors in units of um. Determine the logical effort for each input?*

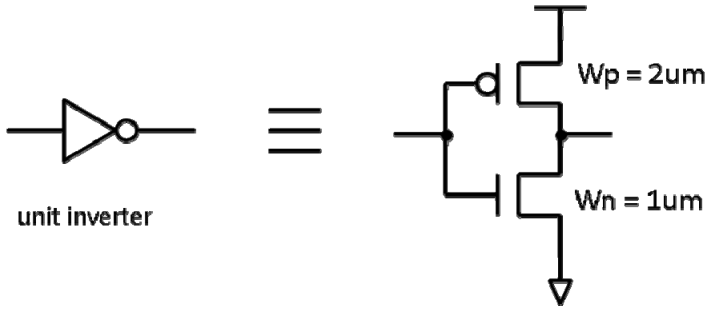


Fig.3 (b) Unit Inverter

Sizes of all transistors:
(In units of um)

LE_A=

LE_B=

LE_C=

(c) (5 pts) In Fig. 3(c), we insert two unit-sized inverters to drive input A of the complex gate. For the complex gate, use the sizes of transistors that you derived in (b). Assume that $C_D=C_G$ =2fF/μm. The delay, Td1, measured from ***In*** to ***X*** is 40ps. What is the delay, Td2, measured from ***In*** to ***Y***?

(Note: If you don't know the answer for (a) and (b), replace the complex gate with a 3-input NOR gate, $F = \overline{A + B + C}$ *. Size the transistors of 3-input NOR gate such that the worst cast driving strength for all inputs is the same as a unit inverter.)*

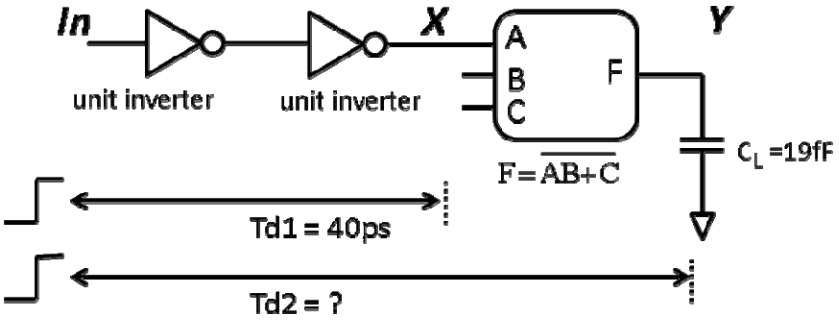


Fig.3 (c) Delay of the Complex Gate

Td2=

(d) (5pts) The complex gate that you designed in (a) is used in the critical path of the logical network shown in Fig. 3(d). Assume that C_D=C_G =2fF/μm. What is the total path effort from In to Out? In order to minimize the delay, what should the effective fan-out per stage for this chain of gates be?

(Note: If you don't know the answer in (a) and (b), replace the complex gate with a 3-input NOR gate, $F = \overline{A + B + C}$ *.)*

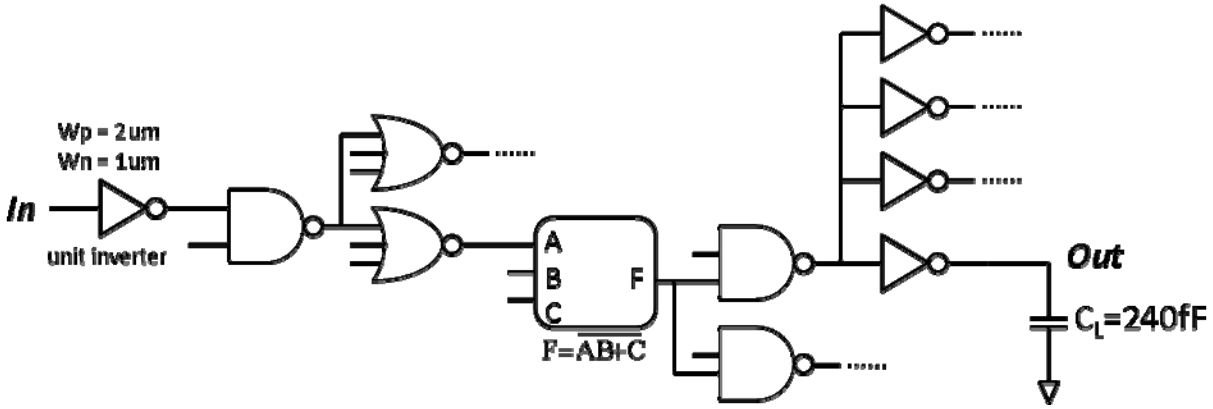


Fig.3 (d) Critical Path of Combinational Logic

PE =
EF =