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Wednesday, April 22, 2:10~3:30pm

SOLUTIONS

PROBLEM 1:

(1) When $V_X = 0.5V$

$|V_{GS}| = 1 - 0.5 = 0.5V$

$|V_{GS}| - |V_T| = 0.5 - 0.3 = 0.2V < |V_{D,VSAT}|$

$|V_{DS}| = 1 - 0.5 = 0.5V > |V_{GS}| - |V_T|$

M1 is therefore in **saturation** region.

When $V_X = 0.1V$

$|V_{GS}| = 1 - 0.1 = 0.9V$

$|V_{GS}| - |V_T| = 0.9 - 0.3 = 0.6V > |V_{D,VSAT}|$

$|V_{DS}| = 1 - 0.1 = 0.9V > |V_{D,VSAT}|$

M1 is therefore in **velocity saturation** region.

(2) Assume the voltage on M1's source (which is also M2's drain) is V_X. Apparently V_X<0.2V; otherwise M1 would be turned off. Therefore for M2:

$V_{GS} - V_T = 0.5 - 0.3 = 0.2V < V_{D,VSAT}$

$V_{DS} = V_X < V_{GS} - V_T$

M2 is therefore in **linear** region.

For M1:

$V_{GS} - V_T < 0.5 - 0.3 = 0.2V < V_{D,VSAT}$

$V_{DS} = 1 - V_X > 1 - 0.2 = 0.8V$

M1 is therefore in **saturation** region.

(3) Again assume the voltage on M1 and M2's sources is V_X. Apparently 0.3V<V_X<0.7V for both transistors to be on. For M2:

$|V_{GS}| - |V_T| < 0.7 - 0.3 = 0.4V < |V_{D,VSAT}|$

$|V_{DS}| = |V_{GS}| > |V_{GS}| - |V_T|$

Therefore M2 is in **saturation** region.

$$|I_{D2}| = \frac{2W}{L} k_p \frac{1}{2}\left(|V_{GS}| - |V_T|\right)^2 = \frac{W}{L} \times 50 \frac{\mu A}{V^2}\left(V_X - 0.3\right)^2$$

For M1:

$V_{DS} = V_{GS} > V_{GS} - V_T$

So it can be either in saturation or velocity saturation region. Assume it is in saturation,

$$I_{D1} = \frac{W}{L} k_n \frac{1}{2}\left(V_{GS} - V_T\right)^2 = \frac{W}{L} \times 50 \frac{\mu A}{V^2}\left(1 - V_X - 0.3\right)^2$$

Since the current of M1 and M2 has to be identical,

$$\frac{W}{L} \times 50 \frac{\mu A}{V^2}\left(V_X - 0.3\right)^2 = \frac{W}{L} \times 50 \frac{\mu A}{V^2}\left(0.7 - V_X\right)^2$$

$$V_X = 0.5V$$

which validates the assumption that M1 is indeed in **saturation** region.

(4) Again assume the voltage on M1's drain (or M2's source) is V_X. Apparently V_X>0.3V; otherwise M2 would be turned off. M1 is either in velocity saturation or linear region. Assume it is in the linear region:

$$V_X > 1 - \left|V_{D,VSAT}\right| = 0.5V$$

$$\left|I_{D1}\right| = \frac{2W}{L} k_p \left(\left|V_{GS}\right| - \left|V_T\right| - \frac{1}{2}\left|V_{DS}\right|\right) \times \left|V_{DS}\right| = \frac{2W}{L} k_p \left(1 - 0.3 - \frac{1 - V_X}{2}\right) \times \left(1 - V_X\right) \quad [1]$$

Now for M2, since its V_{DS}>0.5V, it is either in saturation or velocity saturation region. Further assume M2 is saturation,

$$\left|V_{GS}\right| = V_X - \left|V_T\right| = V_X - 0.3V < \left|V_{D,VSAT}\right|$$

$$V_X < 0.8V$$

$$\left|I_{D2}\right| = \frac{W}{L} k_p \times \frac{1}{2} \times \left(\left|V_{GS}\right| - \left|V_T\right|\right)^2 = \frac{W}{2L} k_p \left(V_X - 0.3\right)^2$$

Since $I_{D1}=I_{D2}$:

$$V_X = 0.87V$$

Apparently the assumption that M2 is in saturation is invalid. Alternatively let's assume it's in velocity saturation region:

$$\left|I_{D2}\right| = \frac{W}{L} k_p \left(\left|V_{GS}\right| - \left|V_T\right| - \frac{1}{2}\left|V_{D,VSAT}\right|\right) \times \left|V_{D,VSAT}\right| = \frac{W}{L} k_p \times \left(V_X - 0.3 - 0.25\right) \times 0.5 \quad [2]$$

Equating [1] and [2]

$$V_X = 0.87V$$

which validates the assumption.

Therefore: M1 is in **linear** region; M2 is in **velocity saturation** region.

PROBLEM 2

(1) Size the transistors of the first-stage dynamic CMOS gate Y such that the worst-case drive strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What is logical effort of Y for input A and B? (Freebee!) (1 pt)

m1=m2=m3=3 (0.5 pt)

m4=2

$LE_A = LE_B = 1$ (0.5 pt)

(2) Determine the logic function F of the logic network in terms of input A, B, and C. (Another freebee!) (0.5 pt)

F= $\overline{(AB+C)}$ (0.5 pt)

(3) It is reasonable to first assume that the critical path for the output F high-to-low transition is from the input A to the output F. Size the gate Y, R, and Z to minimize the propagation delay T_{HL} **from the input A to the output F**. Assume the input capacitance of the input A cannot exceed 4C, where C is the input capacitance of a unit size inverter. (3 pts)

$G = 1 \times 1 \times \frac{5}{3} = \frac{5}{3}$ (0.5 pt)

$B = 1$

$F = 75$ (0.5 pt)

$h = \sqrt[3]{GBF} = \sqrt[3]{\frac{5 \times 75}{3}} = 5$ (0.5 pt)

$f_1 = \frac{h}{g_1} = \frac{5}{1} = 5,\ f_2 = \frac{h}{g_2} = \frac{5}{1} = 5,\ f_3 = \frac{h}{g_3} = \frac{5}{\frac{5}{3}} = 3$

Sizing of gates accordingly:
(Note: I use the same definition in the lecture note. Size 2 gate has twice the input capacitance of a unit inverter)

$Y = 4$ (0.5 pt)

$R = 4f_1 = 20$ (0.5 pt)

$Z = 4f_1 f_2 = 100$ (0.5 pt)

Y=4

R=20

Z=100

(4) Use the same transistor size you find in (3) to calculate the propagation delay T_{HL} in terms of t_{p0}. Assume $\gamma = 1$ (1.5 pts)

$p = \frac{5}{3} + 1 + 2 = 4\frac{2}{3}$ (0.5 pt)

$\frac{T_{HL}}{t_{p0}} = \sum\left(p_i + \frac{f_i g_i}{\gamma}\right) = 4\frac{2}{3} + \frac{1}{\gamma}\left(5 + 5 + 5\right) = 19\frac{2}{3}$ (0.5 pt)

$T_{HL} = 19\frac{2}{3}t_{p0}$ (0.5 pt)

(5) Now let's turn to the output F low-to-high transition. Identify the critical path of the network for the output low-to-high transition and explain your choice. Calculate the propagation delay T_{LH} by using the same transistor size you find in (3). (2 pts)

The critical path is from the input C to the output (0.5 pt) because the delay from A to o2 is zero for the output low-to-high transition. (0.5 pt)

$$p = 2$$

$$\frac{T_{LH}}{t_{p0}} = \sum\left(p_i + \frac{f_i g_i}{\gamma} \right) = 2 + \frac{1}{\gamma} \cdot 5 = 7 \text{ (0.5 pt)}$$

$$T_{LH} = 7t_{p0} \text{ (0.5 pt)}$$

(6) What are the activity factors of nodes o1, o2, and F if P(A=0) = P(B=0) = P(C=0) = 0.25? (2 pts)

$$\alpha_{o1(0->1)} = p(o1 = 0) \cdot p(o1 = 1) = \frac{3}{4} \cdot \frac{3}{4} \cdot 1 = \frac{9}{16} \text{ (0.5 pt)}$$

$$\alpha_{o2(0->1)} = p(o2 = 0) \cdot p(o2 = 1) = 1 \cdot \frac{9}{16} = \frac{9}{16} \text{ (0.5 pt)}$$

$$\begin{aligned}\alpha_{F(0->1)} &= p(F = 0) \cdot p(F = 1) \\ &= (p(o2 = 0) \cdot p(C = 1) + p(o2 = 1) \cdot p(C = 0) + p(o2 = 1) \cdot p(C = 1)) \cdot \\ &\quad p(o2 = 0) \cdot p(C = 0) \\ &= (1 \cdot \frac{3}{4} + \frac{9}{16} \cdot \frac{1}{4} + \frac{9}{16} \cdot \frac{3}{4}) \cdot 1 \cdot \frac{1}{4} \text{ (0.5 pt)} \\ &= \frac{21}{64} \text{ (0.5 pt)}\end{aligned}$$

$$\alpha_{o1(0->1)} = \frac{9}{16}$$

$$\alpha_{o2(0->1)} = \frac{9}{16}$$

$$\alpha_{F(0->1)} = \frac{21}{64}$$