EE223 Analog Integrated Circuits
Fall 2018

Lecture 16: Midterm Solution and Project Description

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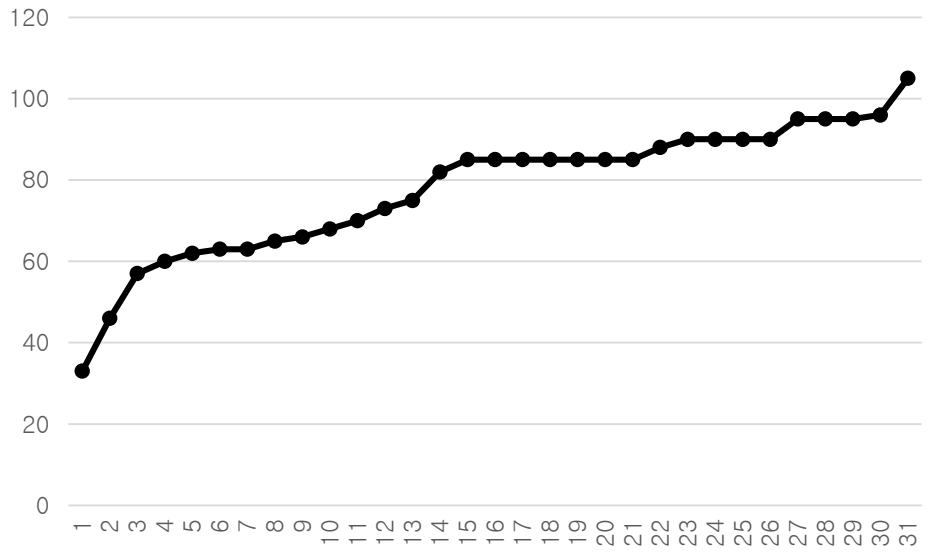
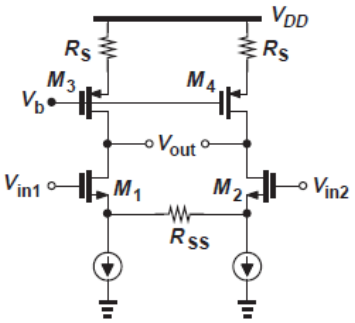
Midterm Score

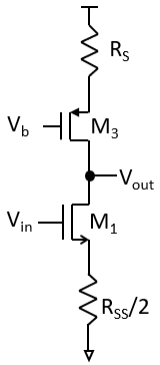


Problem #1

For the differential amplifier shown below, answer the followings.

a) Draw a half circuit on the right-hand side of the above circuit. (**5 point)**
b) From the half circuit, provide the gain expression of the circuit by inspection. Make a reasonable approximation if necessary. (**5 point)**
c) Provide the expression for the output impedance of the circuit by inspection. Make a reasonable approximation if necessary. **(5 point)?**





$$\frac{V_{out}}{V_{in}} = \frac{-(g_{m3}r_{o3})(R_S)}{\frac{1}{g_{m1}} + \frac{R_{SS}}{2}}$$

$$R_{out} = R\uparrow // R\downarrow$$

$$= (g_{m3}r_{o3})(R_S) // (g_{m1}r_{o1})(\frac{R_{SS}}{2})$$

Problem #2

For the transistor below with W/L = 10um/1um, assume VT0=0.6V, γ=0.4V1/2, 2ΦF=0.9V. Use the equations below to solve the problems.

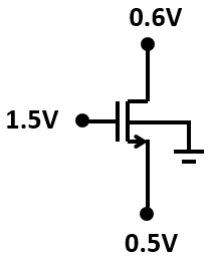
a) Calculate VT and state the transistor's region of operation (Triode or Saturation). (10 points)

b) Based on the result from a), using an appropriate IDS equation above (either Triode or Saturation), derive expressions for gm, go, gmb from its definition and sketch the low frequency small-signal model of the transistor. Use Leff=L-2LD to simplify the expression. (10 points)

$$I_{DS} = \mu_n C_{OX} \frac{W}{L-2L_D}\left(V_{GS} - V_{Tn} - 0.5V_{DS}\right)V_{DS} \quad \textbf{(Triode)}$$

$$I_{DS} = \frac{1}{2}\mu_n C_{OX} \frac{W}{L-2L_D}\left(V_{GS} - V_{Tn}\right)^2\left(1+\lambda V_{DS}\right) \quad \textbf{(Saturation)}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}\right)$$



Triode equation → $I_{DS} = \mu C_{ox} (W/L) (V_{gs}-V_T-0.5V_{ds}) V_{ds}$

$g_m = dI_{ds}/dV_{gs} = \mu C_{ox} (W/L) V_{ds}$

$g_o = dI_{ds}/dV_{ds} = \mu C_{ox} (W/L) (V_{gs}-V_T-V_{ds})$

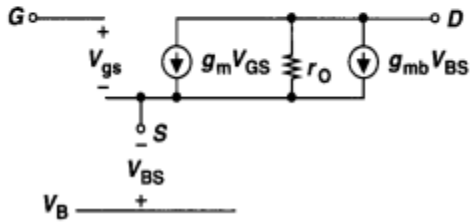
$g_{mb} = dI_{ds}/dV_{bs} = [dI_{ds}/dV_T][dV_T/dV_{bs}] = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}}$

$V_T = 0.6 + 0.4\,(\text{sqrt}(0.9 + 0.5) - \text{sqrt}(0.9)) = 0.694$

$V_{gs} - V_T = (1.5 - 0.5) - 0.694 = 0.306$

$V_{ds} = 0.6 - 0.5 = 0.1$

$V_{ds} < V_{gs}-V_T$ → Triode

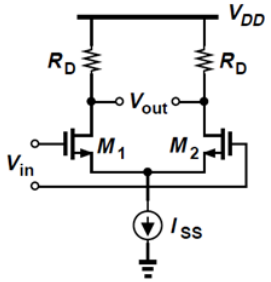


Problem #3

For the differential amplifier below with $(W/L)_1 = (W/L)_2 = 10um/1um$, assume VDD = 1.8V, Vth = 0.6 V, Vdsat1 = Vdsat2 = Vgs-Vth = 0.3V, Iss requires Vdsat of 0.3V, gds = 0.

a) What is the dc bias voltage at the output to get the maximum output voltage swing? (5 points)

b) Find the maximum achievable dc gain based on the dc operating point found in a). Final answer should be a number, not an expression. You know there are 3 gm expressions. Pick an appropriate gm expression to solve this problem. (5 points)



Vout max = 1.8V, Vout min = 0.3V + 0.3V = 0.6V

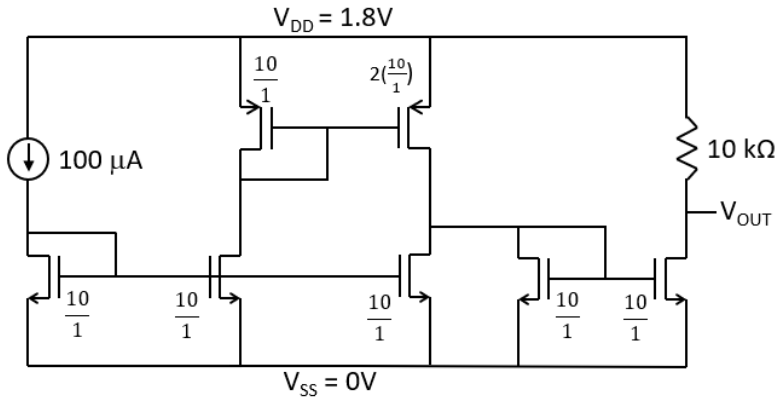
→ Peak-to-peak output signal swing = 1.2V

→ DC operating point is Vdd – 0.6V = 1.2V

DC gain = $g_m R_D = (2 I_1 / V_{dsat1}) R_D = (2 I_1 R_D) / V_{dsat1} = 2 \times 0.6 / 0.3 = 4$

Problem #4

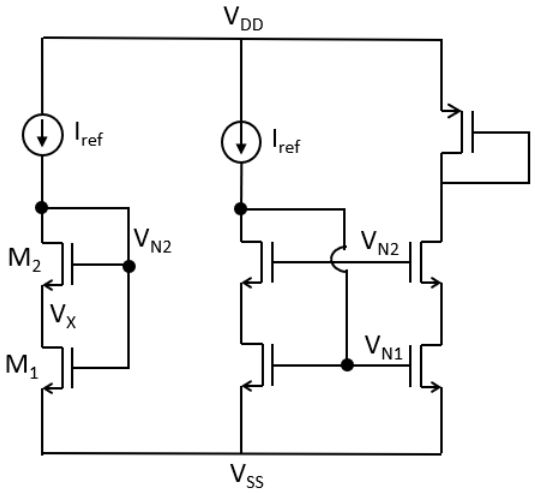
For the current mirror circuit below, neglect channel length modulation effect. What is the voltage at Vout? Show how you come up with the result.



The output current through 10kΩ resistor is 100uA.
Therefore, Vout = 1.8V – 10kΩ x 100uA = 1.8V - 1V = 0.8V.

Problem #5

For the high-swing cascode current mirror circuit below, prove why the transistors M1 and M2 are in either Triode or Saturation.



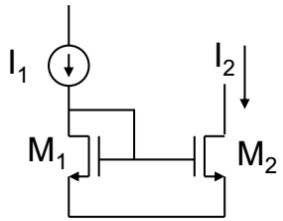
M2 is in saturation as it is diode connected.
$V_{ds2} = V_{gs2} > V_{gs2} - V_{th2}$.

M1 is in Triode region. Proof is as follows:
$V_{ds1} = V_x$
$V_{gs1} - V_{th1} = V_x + V_{gs2} - V_{th1} = V_x + V_{th2} + V_{dsat2} - V_{th1} \approx V_x + V_{dsat2}$
Therefore, $V_{ds1} < V_{gs1} - V_{th1} \rightarrow$ Triode region

Problem #6

For the simple current mirror shown below, assume I1=10μA, W=L=5μm for both M1 and M2, and VDS of M1 and M2 are the same, and Vdsat = 0.3V. Because of random mismatch introduced during the manufacturing process, threshold voltage (Vth) will not be the same. Use Pelgrom's model to solve this problem.

a) What is the Vth mismatch, ΔVth, if Avt = 3mV·μm ? (5 points)



$$\Delta V_{th} = \frac{A_{vt}}{\sqrt{WL}} = \frac{3mV \cdot um}{\sqrt{5um\ x\ 5um}} = \frac{3mV \cdot um}{5um} = 0.6\text{mV}$$

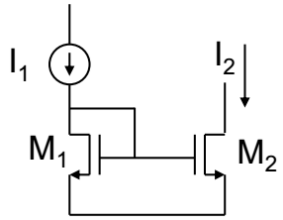
b) Assume the current mismatch (ΔI/I) is mostly due to Vth mismatch (neglect W/L mismatch) and the mismatch is 0.2% initially when W=L=5μm. Provide the new size to achieve 0.1% current mismatch while maintaining the same Vdsat. State the exact value for W and L individually. (5 points)

$$\frac{\Delta I}{I} \approx \frac{2\Delta V_{th}}{V_{gs}-V_{th}} = \frac{2\Delta V_{th}}{V_{dsat}}$$

In order to reduce the current mismatch by of factor of 2 while maintaining the same V_{dsat}, we have to reduce ΔV_{th} by a factor of 2. This means WL should be increased by a factor of 4. Since we have to maintain the same V_{dsat}, W/L ratio should not be changed. Therefore, W=L=10um.

Problem #6

c) Now I am allowed to change the dc bias point while I1 is still 10μA. So, I have changed the size of both M1 and M2 to W=25μm and L=1μm to increase the gm of the transistors. Assuming the VDS of M1 and M2 are still the same, explain what is going to happen to the mismatch characteristics ($\Delta I/I$) of the current mirror. Mismatch gets better or worse, why? (5 points)



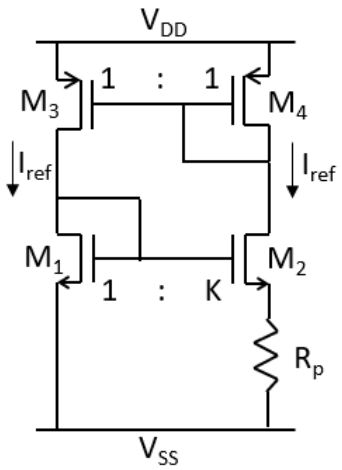
From the golden equation $I_D = ½ (\mu C_{ox}) (W/L) (V_{gs} - V_{th})^2$,
if I change (W/L) ratio from (5/5) to (25/1) while keeping the current, then $V_{gs} - V_{th}$ will be decreased. In the meantime, since the product of W and L, WL=5x5=25x1, is not changed, the V_{th} mismatch ($\Delta V_{th} = \frac{A_{vt}}{\sqrt{WL}}$) remains the same. Therefore, from the current mismatch ($\frac{\Delta I}{I} \approx \frac{2\Delta V_{th}}{V_{gs}-V_{th}} = \frac{2\Delta V_{th}}{V_{dsat}}$) expression, the mismatch will get worse as the numerator is fixed and the denominator has been decreased.

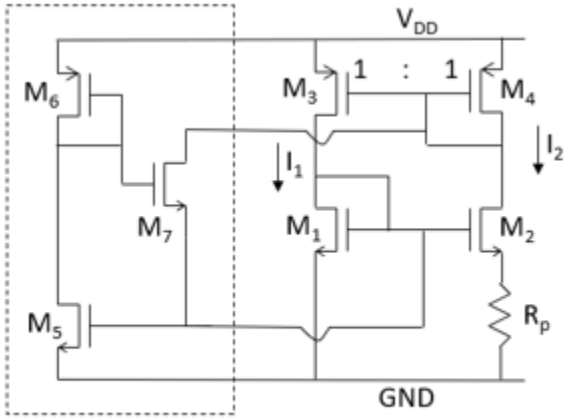
Problem #7

For the circuit shown below,

a) Add a startup circuit and suggest a size for each of the transistors in the startup circuit. (5 points)

b) Derive an expression for Iref in terms of device parameters and K-value. (5 points)

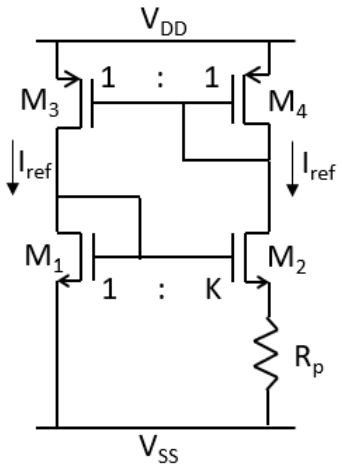




M_5 = 10um/1um, M_6 = 1um/10um, M_7 = 1um/0.18um

Problem #7

b) Derive an expression for Iref in terms of device parameters and K-value. (5 points)



$$V_{gs1} = V_{gs2} + R_p I_2$$

$$V_{th1} + \sqrt{\frac{2I_1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} = V_{th2} + \sqrt{\frac{2I_2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} + R_p I_2$$

$$\sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} = R_p I$$

$$\sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}}\left(1 - \frac{1}{\sqrt{4}}\right) = R_p I$$

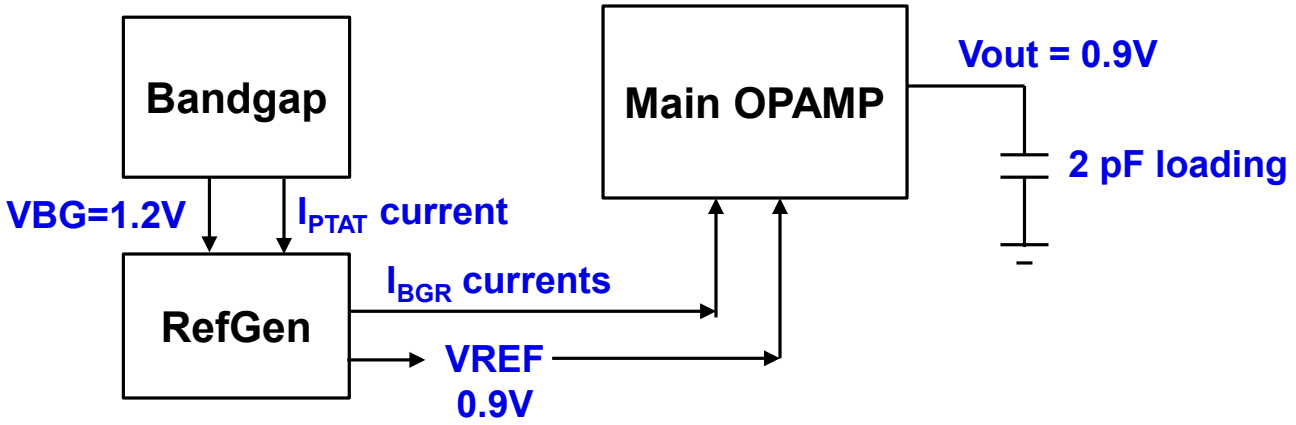
$$\sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}}\frac{1}{2} = R_p I \quad \rightarrow \quad \frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}\frac{1}{4} = R_p{}^2 I^2$$

$$\rightarrow \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}\frac{1}{2} = R_p{}^2 I \quad \rightarrow I = \frac{1}{2R_p{}^2 \mu_n C_{ox}\left(\frac{W}{L}\right)_1}$$

Project Logistics

1. A group of 3 students
2. Less number of students per group is fine
3. One Project Report per group
4. Report should be in IEEE conference paper format
5. Project Report due : 5 PM, Dec 10

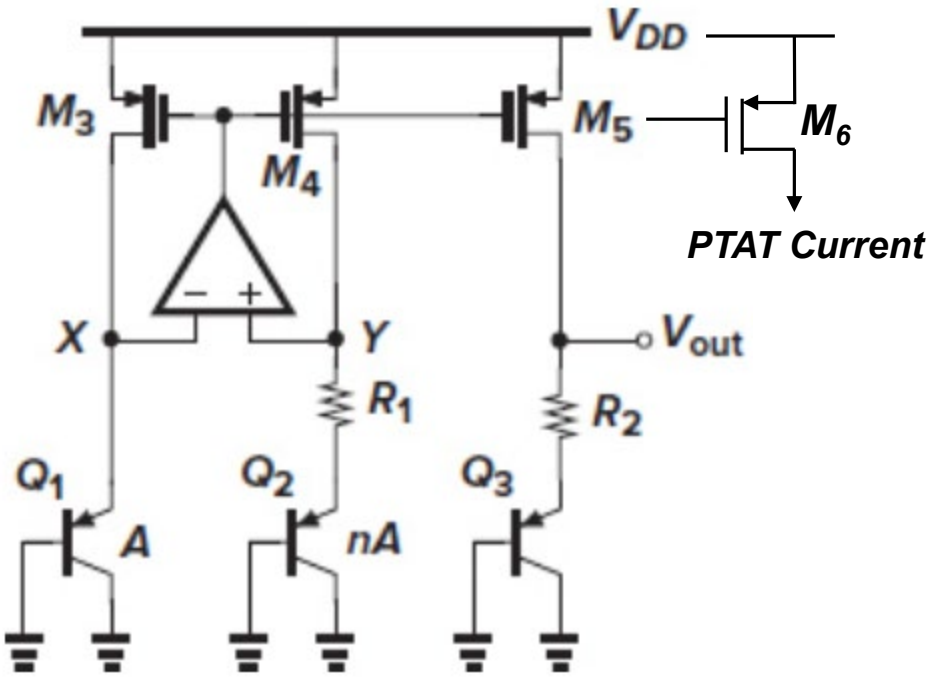
Project Description



Main Circuit – High Gain OPAMP
Auxiliary Circuits – Bandgap, RefGen

- VDD=1.8V
- Device types available for the design
  → nmos2v, pmos2v, nmos2v_nat, vpnp5, resnsppoly, Ideal cap
- Results should meet the requirement over the following PVT corners
  - TT, SS, FF
  - 1.7V, 1.8V, 1.9V
  - -40C, 0C, 40C, 80C

Bandgap



Use PMOS diff pair input
for the Folded-cascode amplifier

Key Spec

Vout should be 1.2V.
Vout variation less than ±1% over PVT
PTAT current is nominally 25uA

Design Procedure

Q1=1, Q2=8, Q3=3
Choose R1 to get the current around I=4~5uA
Then choose R2 to get around Vout=1.2V

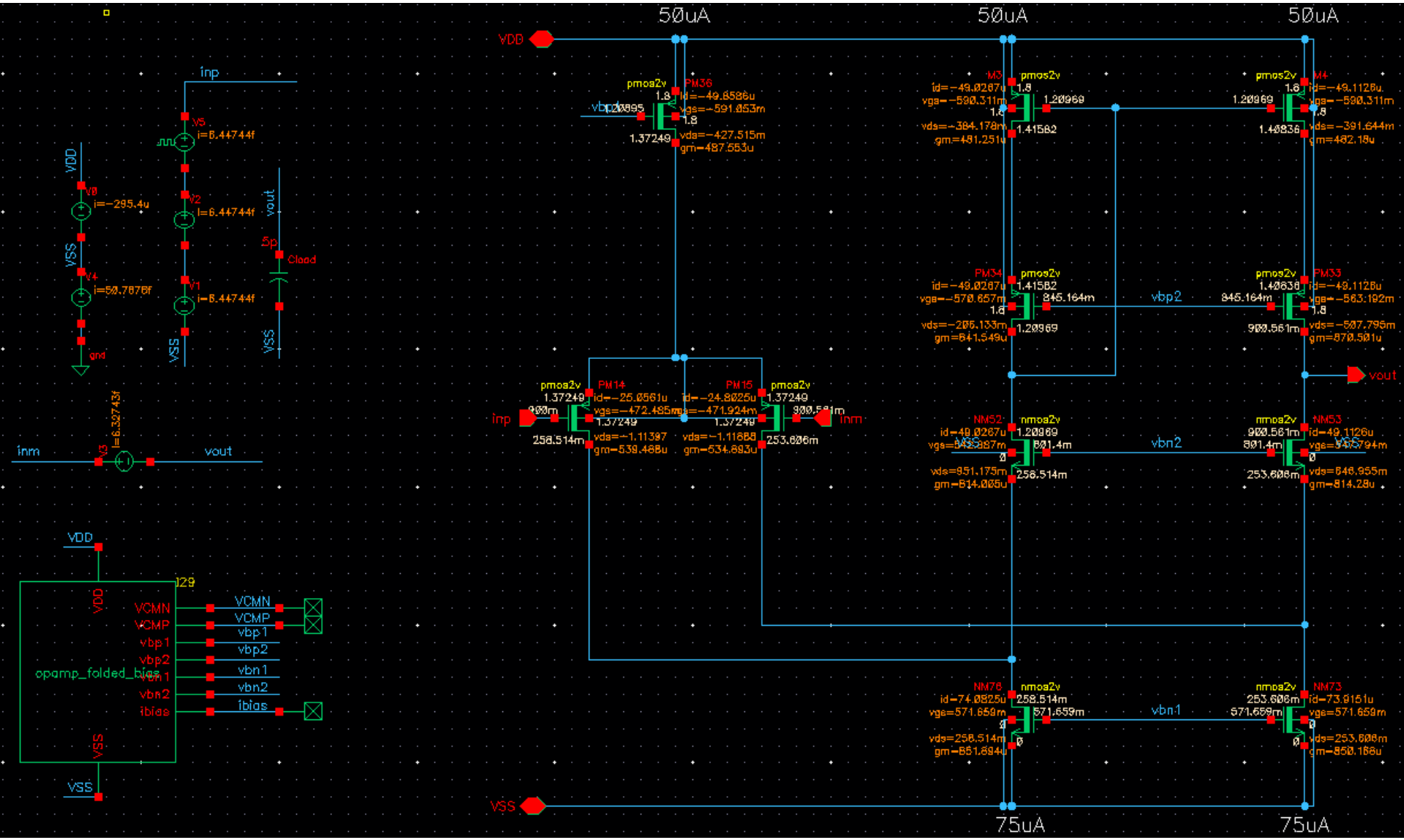
The OPAMP will force the node X and Y to be the same for the matching between M3 and M4.

M3, M4, M5 are generally sized to be the same to carry the same current.

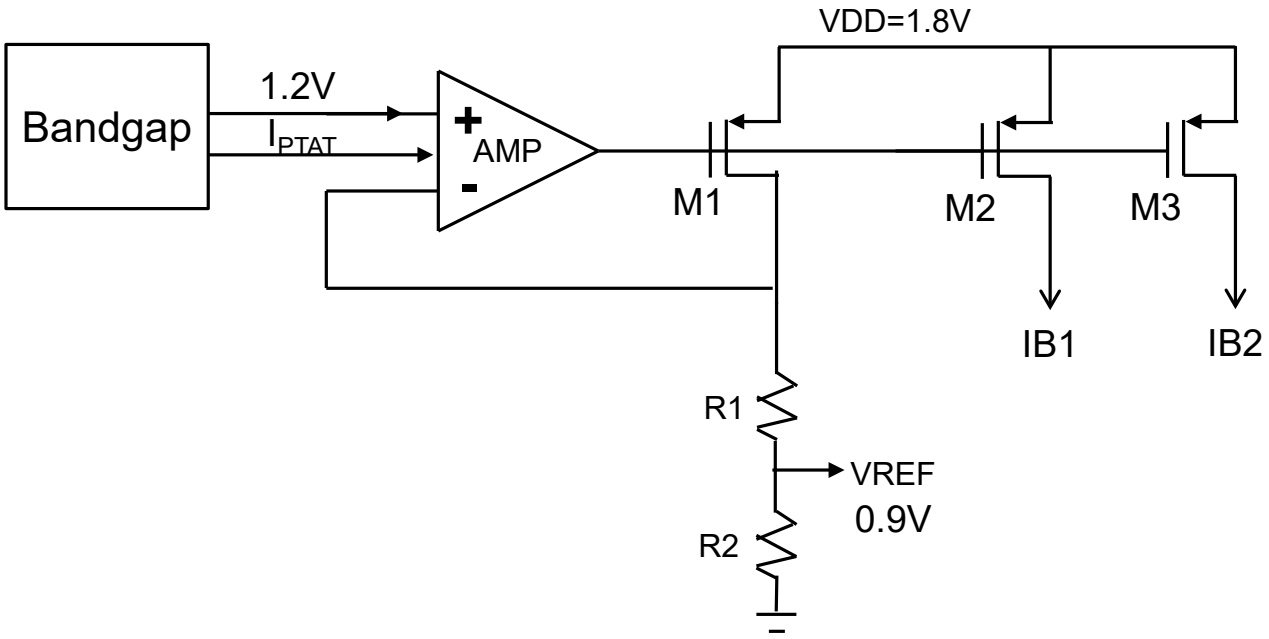
Final Vout, the bandgap voltage output, should be around 1.2V.

Choose R2 to compensate temperature variation of the bandgap voltage.

Example Folded-Cascode Amplifier Circuit



Reference Generator



Design Points

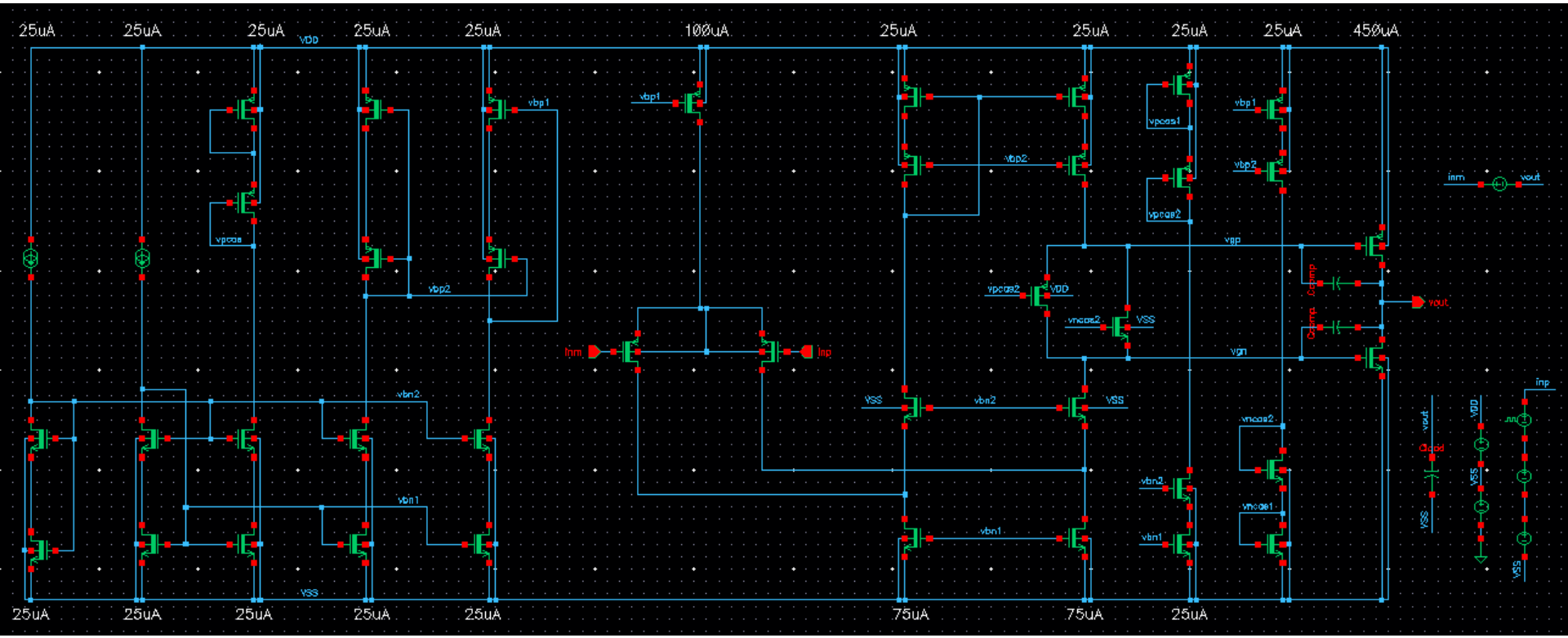
1. AMP and M1 will constitute a 2-stage RC compensated OPAMP.
2. AMP needs to be stable in unity gain configuration.
3. R1 and R2 should use multiple units of the same size.
4. VREF=0.9V will be the input voltage to the main AMP.
5. IB1 and IB2 will supply the currents required in the Main Amplifier.

Main OPAMP Spec

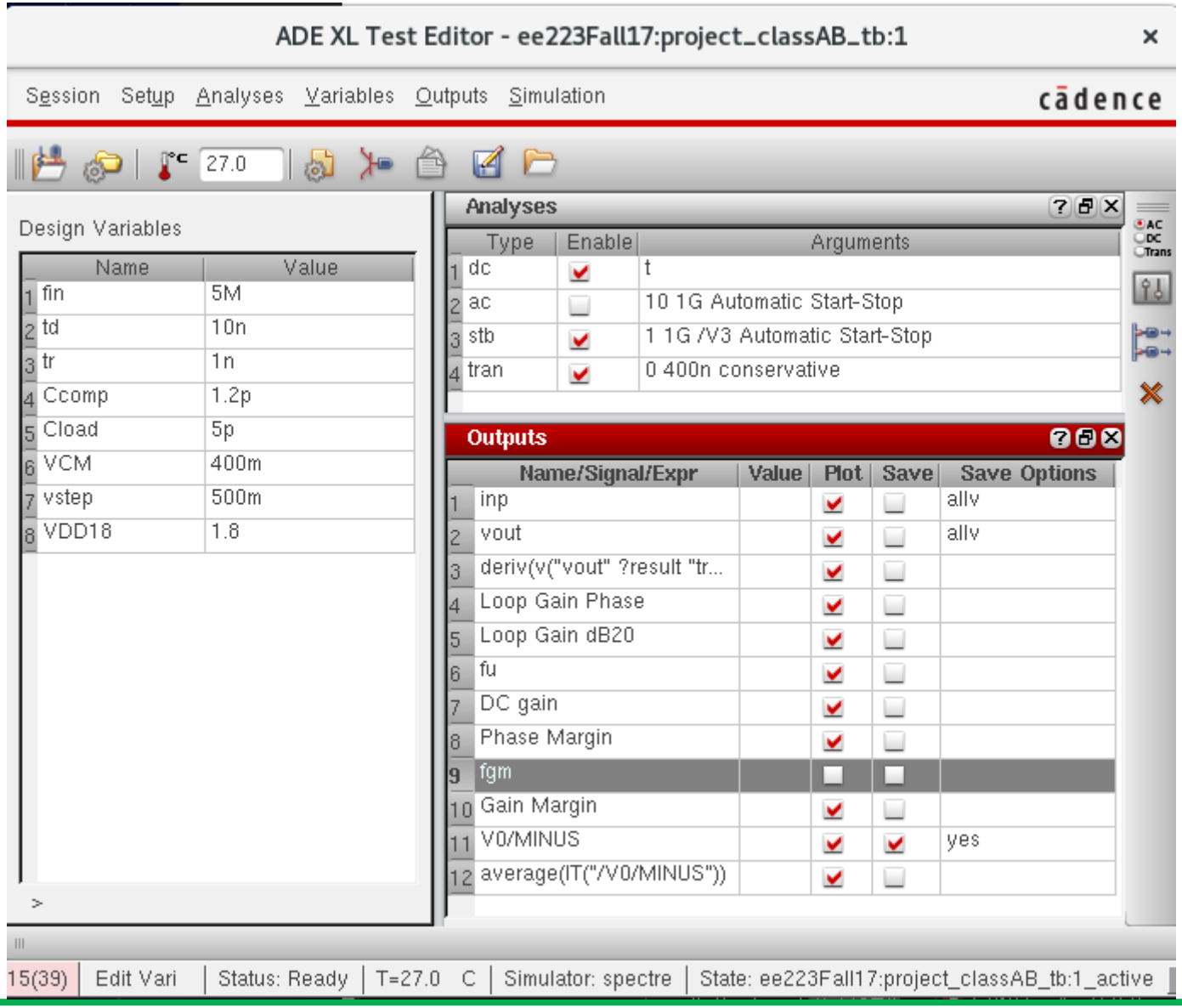
Parameter	Typical Result	PVT Result
DC Gain	80 dB	> 70 dB
Unity Gain Frequency	30 MHz	> 25 MHz
Phase Margin	60 Degree	> 55 Degree
Gain Margin	12 dB	> 9 dB
Slew Rate	15 V/us	> 10 V/us
Power	1.5 mW	< 2 mW

- Loading cap = 2 pF
- For Transient simulation, apply 5MHz input pulse and run for 400 ns.

Example Main OPAMP



ADE Test Editor for Main OPAMP



ADE output parameters of previous slide

- fu
  - To get the unity gain frequency expression in ADE
  - Run stb analysis and plot the Loop Gain and Phase
  - In the plot window, choose Loop Gain dB20 and send it to Calculator → See next page Figure (a)
  - In Calculator, take “cross” of the Loop Gain dB20 → See next page Figure (b)
  - Send buffer expression to ADE → See next page Figure (c)

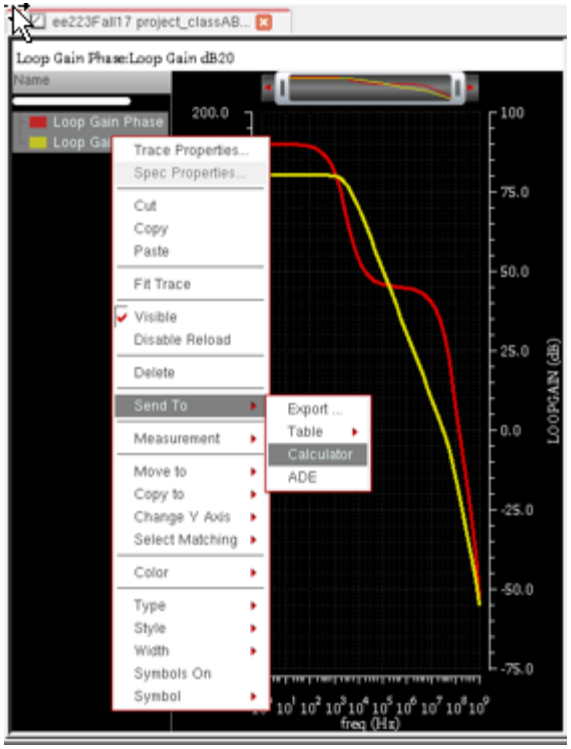
- DC gain
  - To get the DC gain in ADE
  - Send Loop Gain dB20 to Calculator
  - In Calculator, take “value” at 10 Hz of the Loop Gain 20dB → See Figure on page 12
  - Send buffer expression to ADE

- Phase Margin
  - To get Phase Margin in ADE,
  - Send Loop Gain Phase to Calculator
  - In Calculator, take “value” at fu of the Loop Gain Phase
  - Send buffer expression to ADE

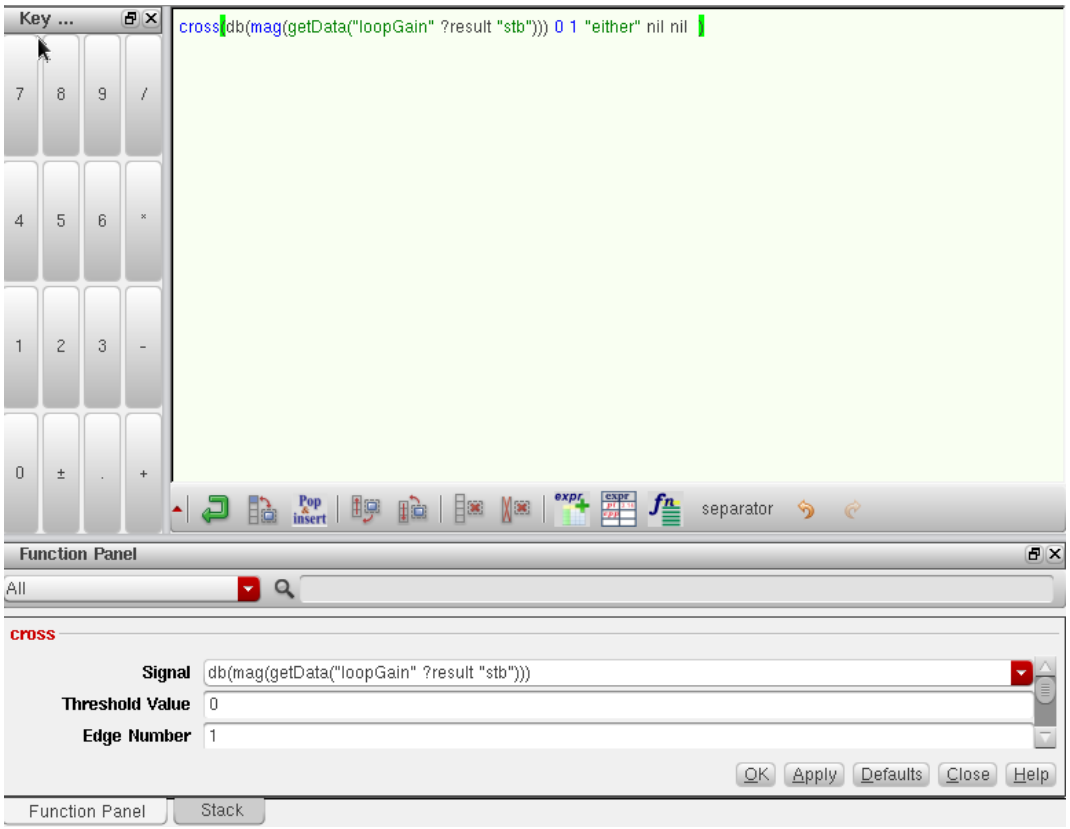
- Gain Margin
  - To get Gain Margin in ADE,
  - Send Loop Gain Phase to Calculator
  - In Calculator, take “cross” of the Loop Gain Phase
  - Send buffer expression to ADE and name it as fgm
  - Then, send Loop Gain dB20 to Calculator
  - In Calculator, take “value” at fgm of the Loop Gain 20dB
  - Send buffer expression to ADE

ADE output parameter for fu

(a)

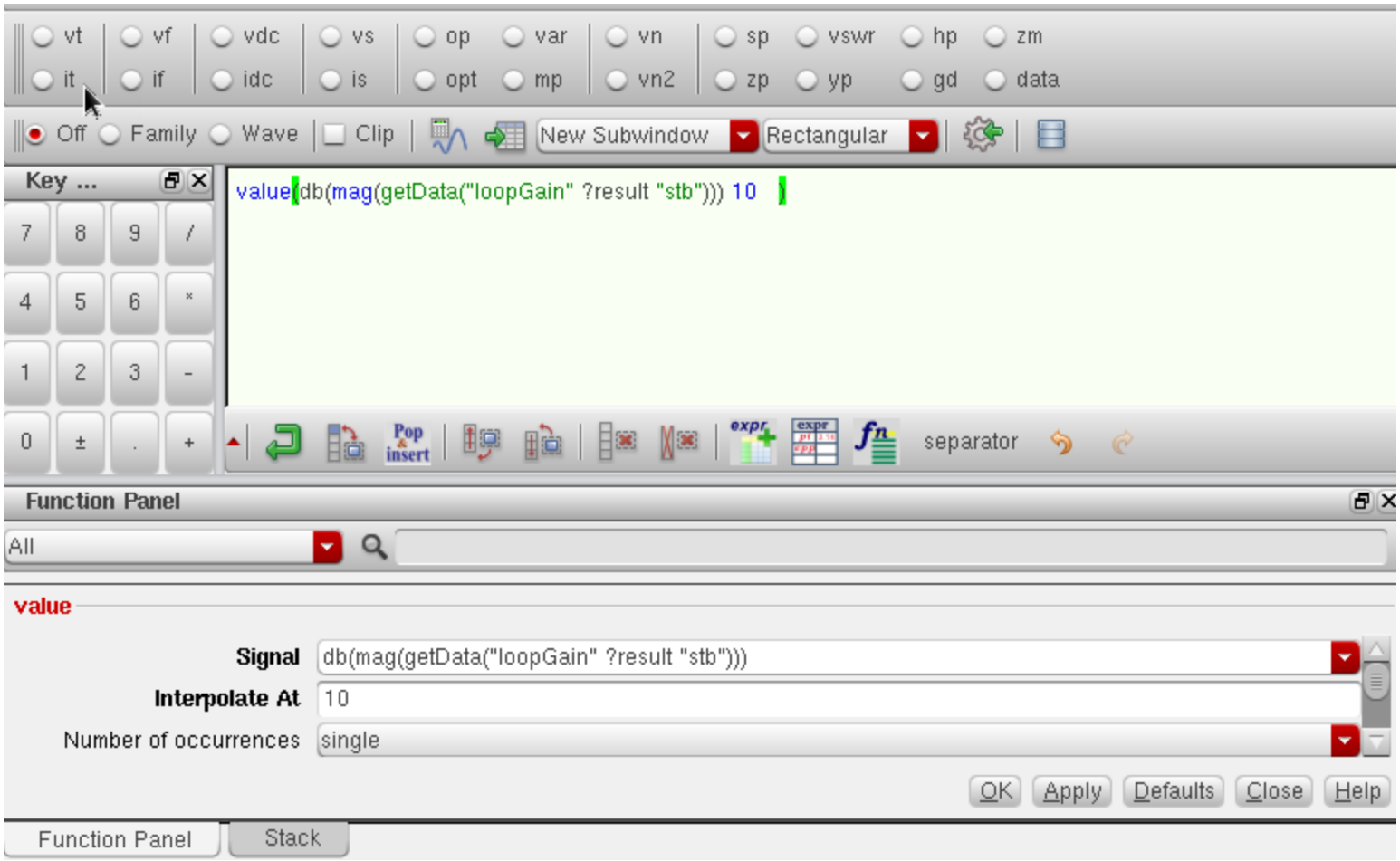


(b)



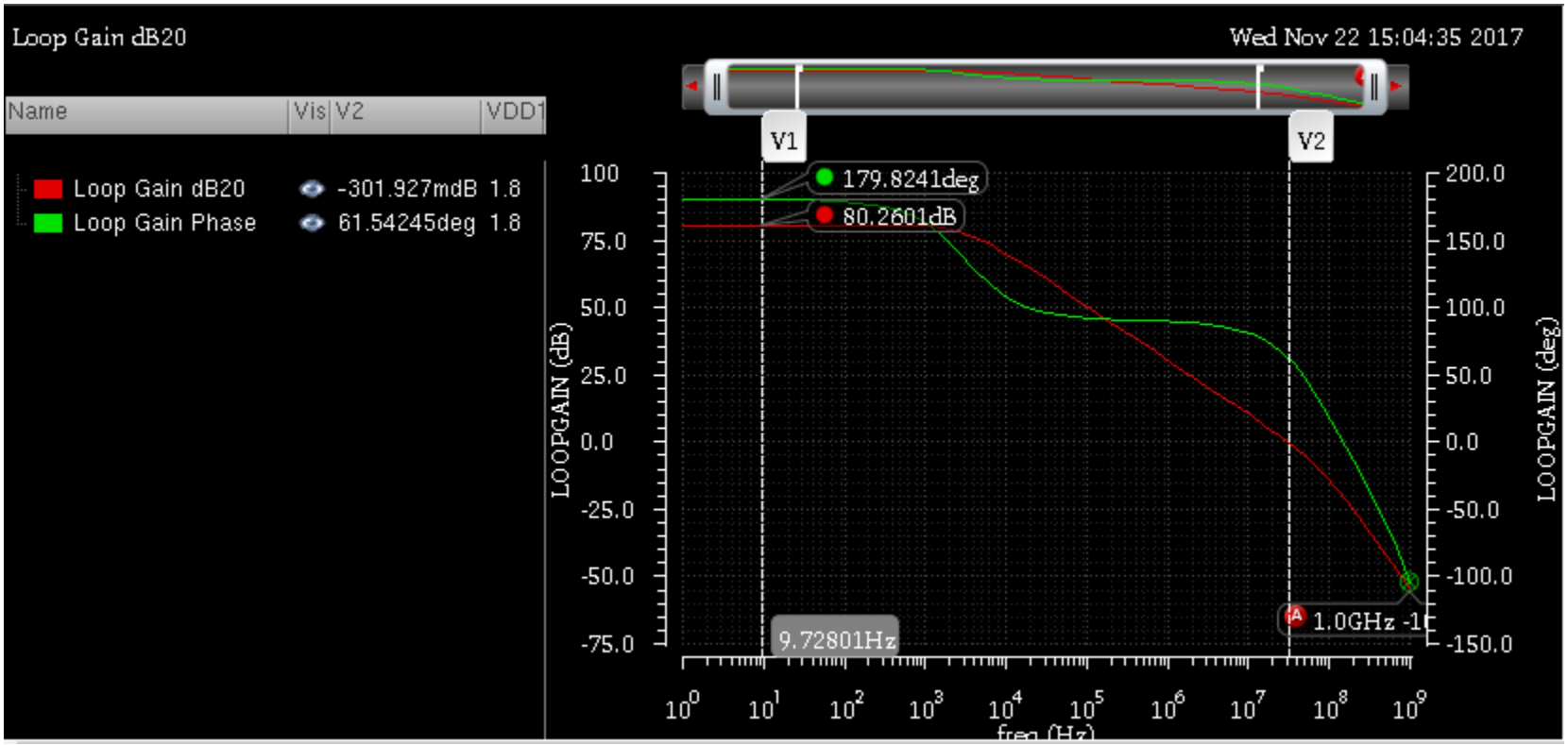
(c)

ADE output parameter for DC Gain



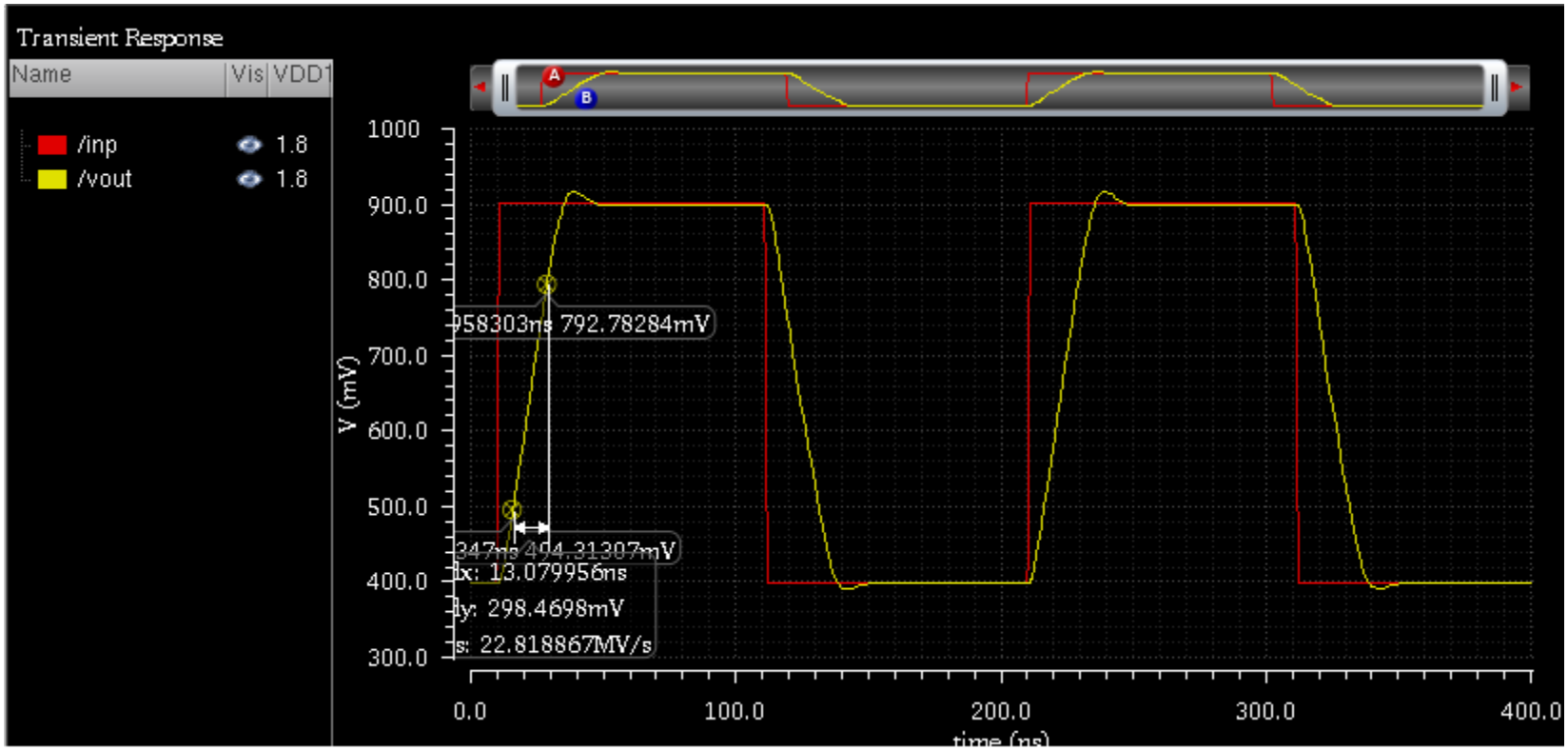
Typical Result for Main OPAMP

stb analysis



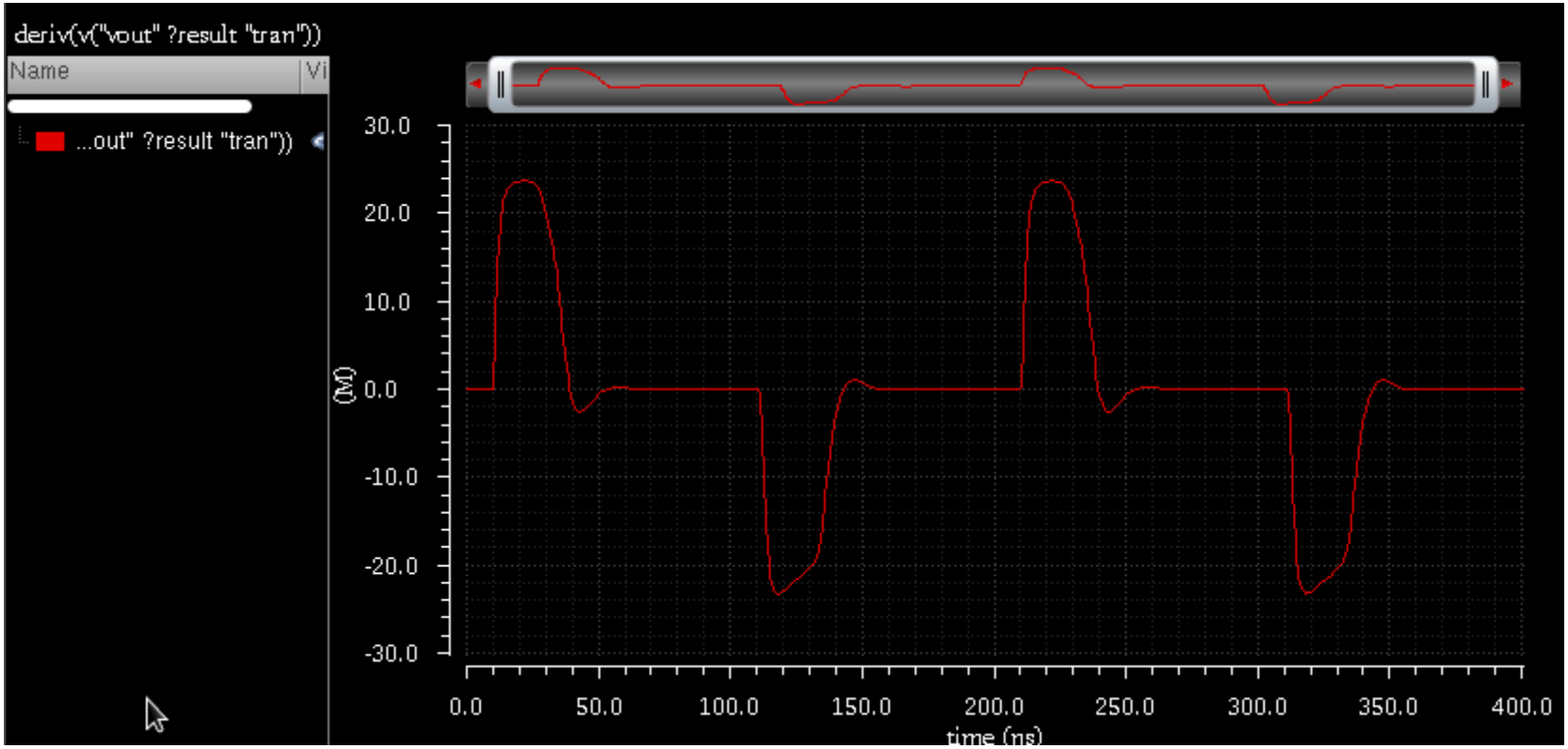
Typical Result for Main OPAMP

Transient analysis

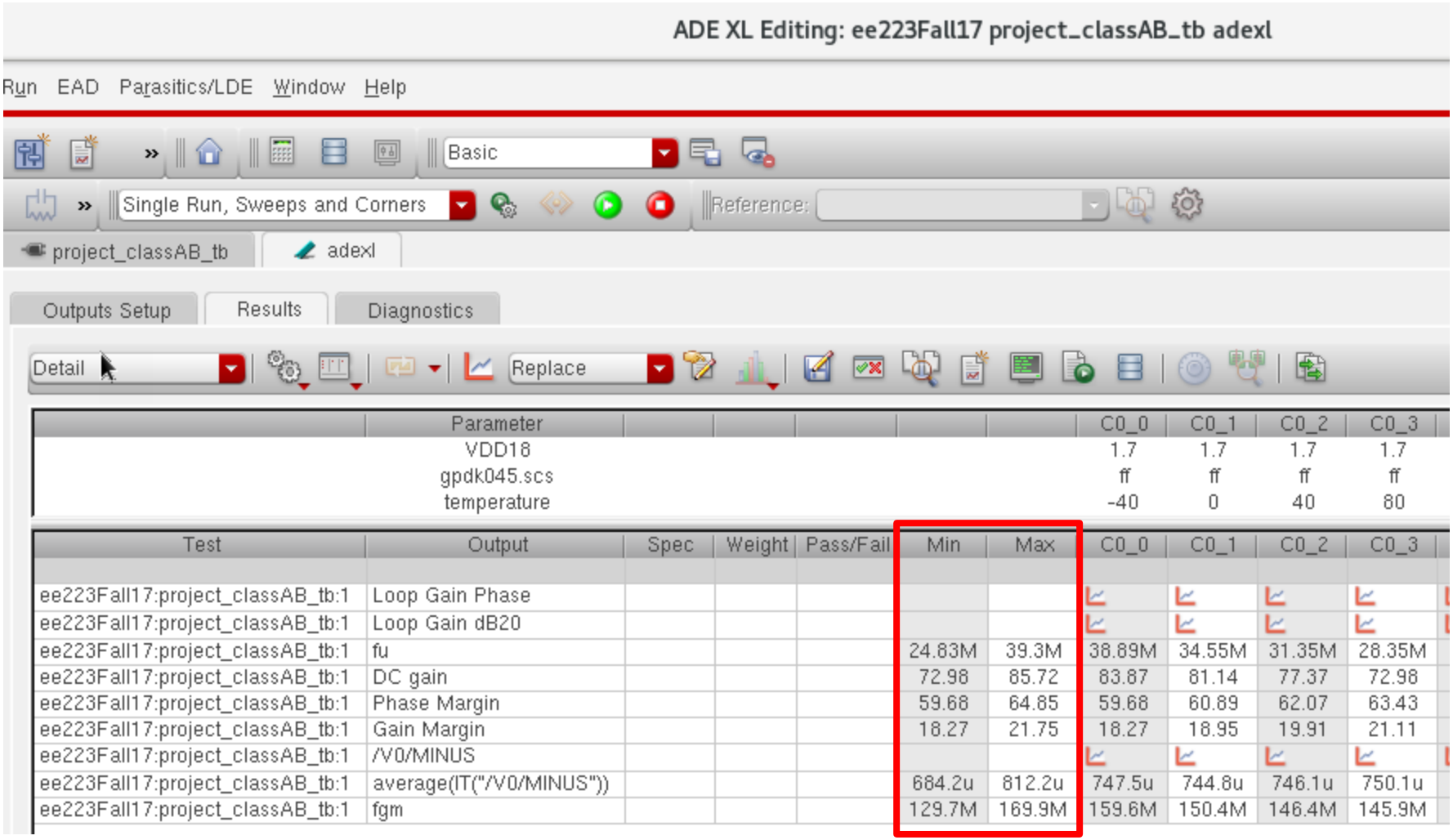


Typical Result for Main OPAMP

Slew rate by taking “deriv” of the output signal in Cadence Calculator



PVT Simulation Result for Main OPAMP using ADE-XL



Parameter						C0_0	C0_1	C0_2	C0_3
VDD18						1.7	1.7	1.7	1.7
gpdk045.scs						ff	ff	ff	ff
temperature						-40	0	40	80

Test	Output	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2	C0_3
ee223Fall17:project_classAB_tb:1	Loop Gain Phase									
ee223Fall17:project_classAB_tb:1	Loop Gain dB20									
ee223Fall17:project_classAB_tb:1	fu				24.83M	39.3M	38.89M	34.55M	31.35M	28.35M
ee223Fall17:project_classAB_tb:1	DC gain				72.98	85.72	83.87	81.14	77.37	72.98
ee223Fall17:project_classAB_tb:1	Phase Margin				59.68	64.85	59.68	60.89	62.07	63.43
ee223Fall17:project_classAB_tb:1	Gain Margin				18.27	21.75	18.27	18.95	19.91	21.11
ee223Fall17:project_classAB_tb:1	/V0/MINUS									
ee223Fall17:project_classAB_tb:1	average(IT("/V0/MINUS"))				684.2u	812.2u	747.5u	744.8u	746.1u	750.1u
ee223Fall17:project_classAB_tb:1	fgm				129.7M	169.9M	159.6M	150.4M	146.4M	145.9M

PVT conditions : TT, SS, FF, 1.7V, 1.8V, 1.9V, -40C, 0C, 40C, 80C – Total 36 corners

References

- Bandgap
  - Chapter 11 of the Textbook
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