University of California
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and Computer Sciences

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WeFr 2-3:30pm

We, April 7, 6:30-8:00pm

EECS 141: SPRING 10—MIDTERM 2

NAME	Last First

SID	

Problem 1 (10):

Problem 2 (12):

Problem 3 (12):

Total (34)	

MAKE SURE TO SHOW REASONINGS and DERIVATIONS.
A NUMERIC ANSWER ONLY DOES NOT SUFFICE!

[PROBLEM 1] COMPLEX LOGIC (10 pts)

(a) **(1 pts)** What is the logic function of the circuit shown below?

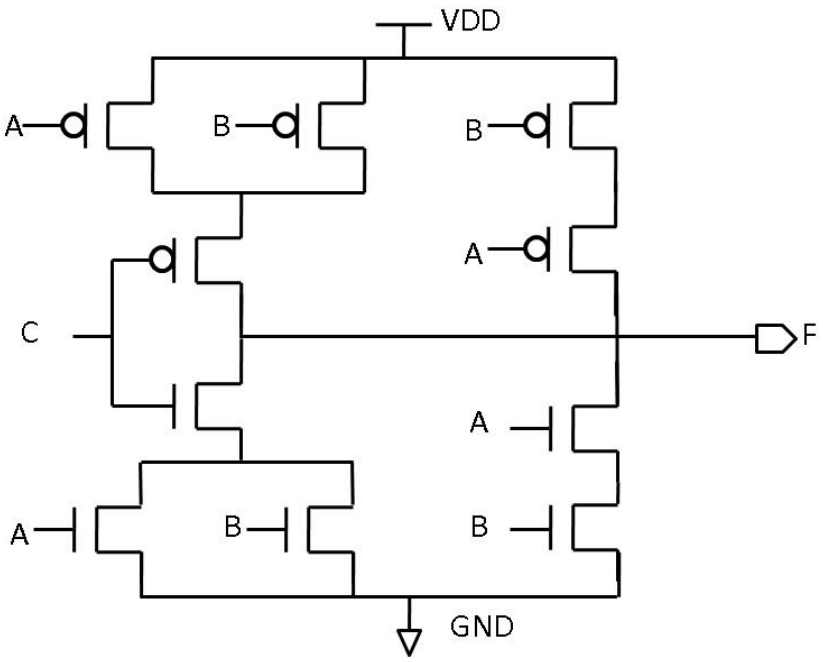

Fig.1

F=

(b) **(4 pts)** Answer the following questions regarding the circuit shown in Fig. 1.

(i) Is this a static logic gate? Why or why not?

(ii) Are the PUNs and PDNs complementary networks (that is, can I use the Euler Graph technique to drive one from the other)? Explain.

(iii) Identify the main advantage of the proposed circuit topology. Back up your answer.

(c) (2 pts) Size the transistors so that the worst-case driving strength for all inputs is the same as a unit inverter (PMOS to NMOS ratio of 2/1). What are logical efforts of the A and C inputs?

LE_A=
LE_C=

(d) **(3 pts)** Is it possible to implement this function using **single n- and p- diffusion strips**? In either case, draw the layout **stick diagram** that would lead to a small area standard cell layout.
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[PROBLEM 2] PASS TRANSISTOR LOGIC (12 pts)

Consider the pass-transistor logic network of Fig. 2. The following (transistor) parameters are given: $V_{TN}=|V_{TP}|=V_T=0.3V$ and $V_{DD}=1.2V$. You may ignore body effect**. C_L= 20fF.** L of all transistors equals 0.1um. The equivalent model of the NMOS and PMOS transistors is given in the Figure as well. The model parameters can assumed to be constant and are NOT a function of biasing conditions. The nominal values for the parameters are given as: Reqn=12kΩ/□ and Reqp=24kΩ/□ (where the □ denotes the W/L ratio); and C_G=2fF/um, C_D=1fF/um (expressed as a function of the transistor width).
Consider the unit size inverter (S=1) to have the following dimensions: Wn=0.2um and Wp=0.4um.

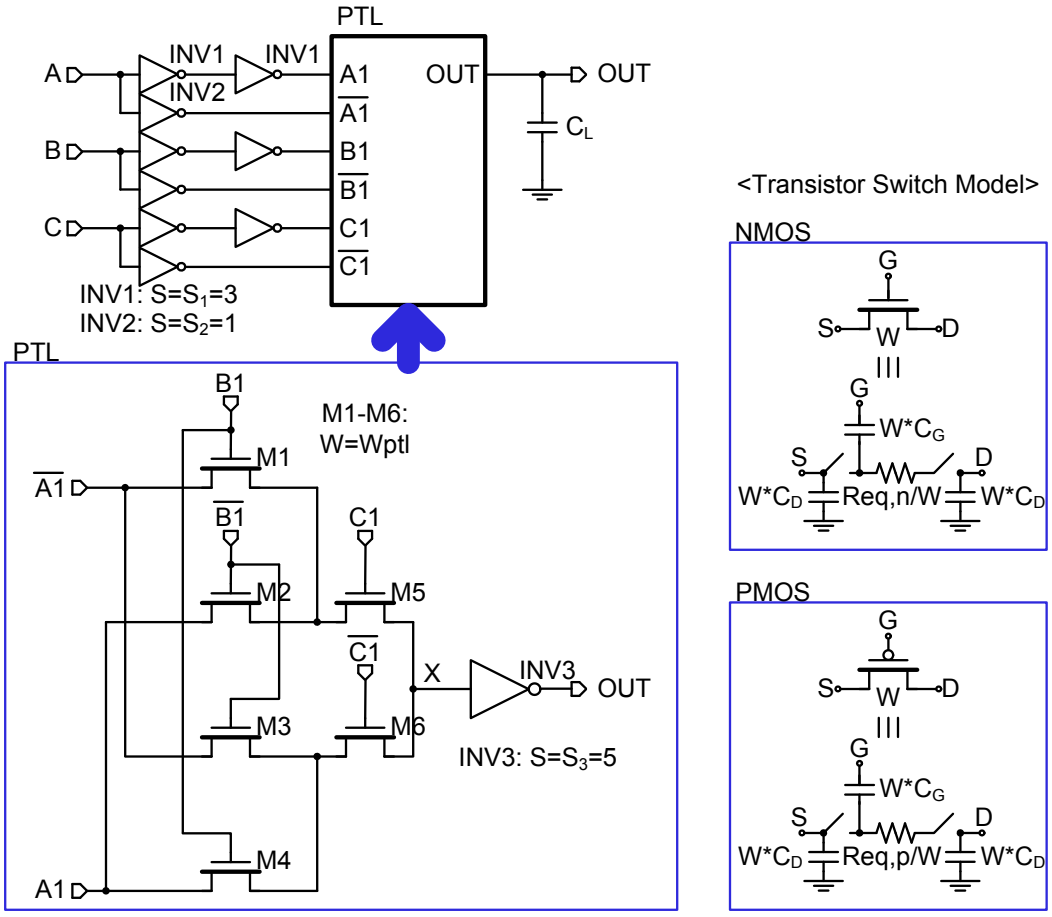

Fig.2 Pass Transistor Logic (PTL)

(a) **(1 pts)** What is function OUT of the circuit of Fig.2 as a function of the A, B, and C inputs?

OUT =

(b) **(4 pts)** Assume that the critical path of the circuit of Fig.2 is from input A to OUT. For the sake of simplicity, **we decided to make all the pass-transistors (M1-M6) equal (size: Wptl)**. We now want to size these transistors so that the delay from A to OUT for a step input from 0 to V_{DD} is minimized.
Draw a **CLEAR** diagram of the critical path of the circuit with the related capacitors annotated, and provide an expression for the value of each capacitor and resistor in your diagram.

(c) **(2 pts)** Derive an expression for the delay as a function of **Wptl** by using Elmore delay method.

(d) **(2 pts)** Determine the value of **Wptl** that minimizes the delay, and find that minimum delay.

Wptl =
Tp(Elmore) =

(e) **(3 pts)** Another approach to derive the delay of critical path and derive the optimum sizing of the pass-transistors is to use the Logical Effort approach. Explain QUALITATIVELY how you would apply this to this problem. Do you expect the result to be the same as obtained in (d)? Explain why or why not?

[PROBLEM 3] Dynamic Logic (12 pts)

In this problem, you may assume that equivalent resistances of a NMOS and PMOS are Reqn=12kΩ/□ and Reqp=24kΩ/□. C_D = C_G=2fF/um (Notice: **This is different from problem 2**). The unit inverter size is Wn=1um and Wp=2um (S=1). The L for all transistors is 0.1um .V_{TN}=|V_{TP}|=V_T=0.3V and V_{DD}=1.2V. Ignore body effect and charge sharing.

(a) (4 pts) A 2-input domino AND gate is shown below. Find the logical efforts for the first stage and second stage (LE_1 and LE_2) for both **the evaluation phase (EV) and precharge phase (PR)?** Please write down the equations of your calculation for each LE.

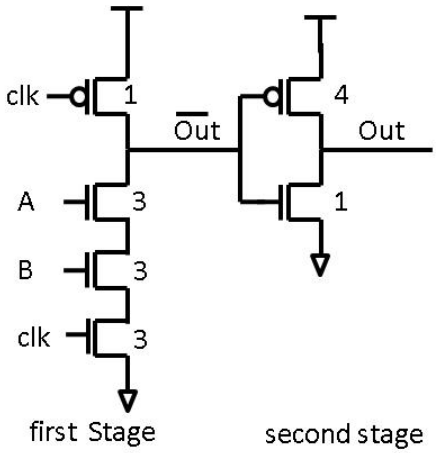

Fig.3a Domino Logic

Evaluation Phase:
$LE_{1,EV}$ =
$LE_{2,EV}$ =

Precharge Phase
$LE_{1,PR}$ =
$LE_{2,PR}$ =

(b) **(3 pts)** A 4-input AND gate can be implemented by using three 2-input domino AND gates as shown in Fig.3a. We properly size each stage in the 4-input AND gate to minimize the delay of the evaluation phase. What is the minimum delay ($\mathbf{T_{p,EV}}$) in the worst-case during the evaluation phase?

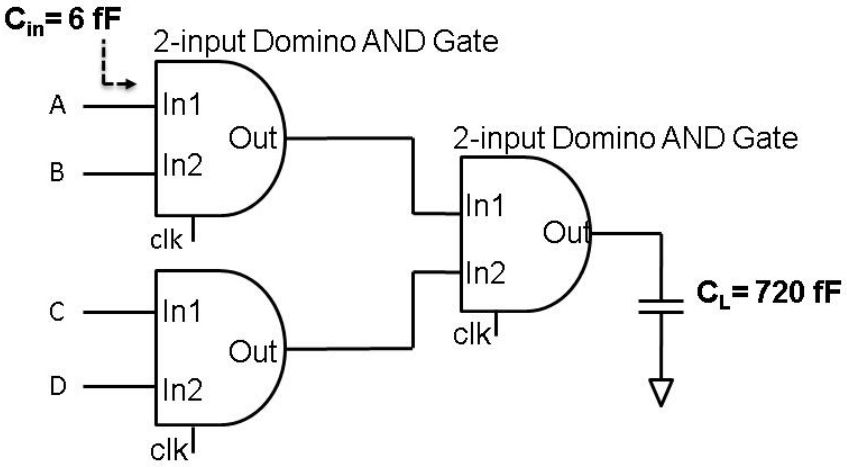

Fig.3b 4-input AND gate with domino logic in Fig.3a.

$T_{p,EV}$ =

(c) (3 pts) With the same sizing, what is the high-to-low delay ($T_{p,PR}$) during the precharge phase?

$T_{p,PR}$ =

(d) **(2 pts)** One engineer developed new domino logic as shown in Fig.3c**.** We use this new domino gate for implementing the 4-input AND gate of Fig.3b. Describe qualitatively how this change impacts the evaluation and precharge times of the gate in comparison with the results of parts (b-c).

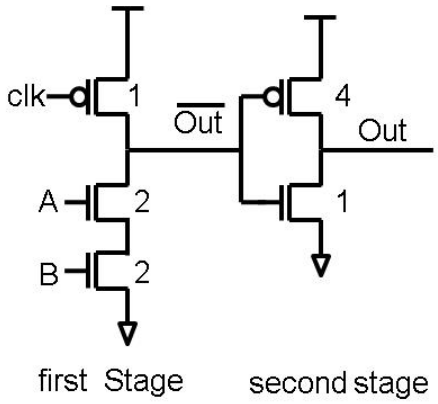

Fig.3c New domino logic for 4-input AND gate in Fig.3b