EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 20: Pipelined ADC 2

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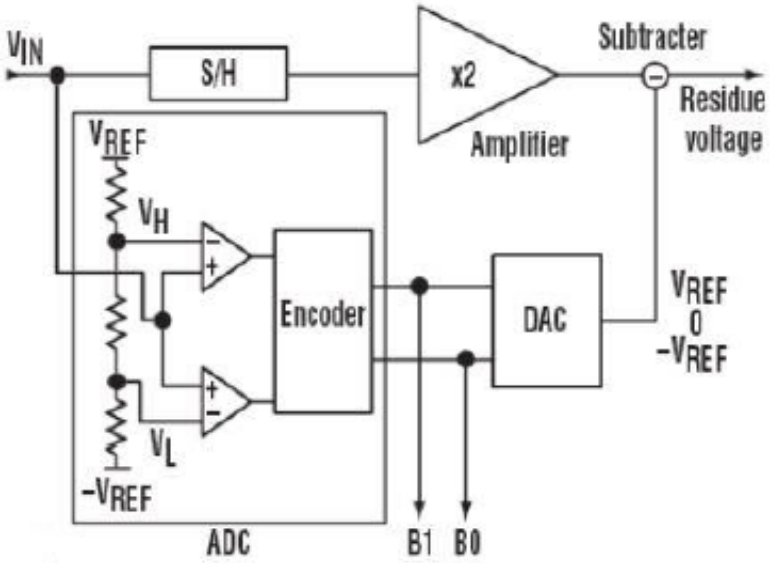
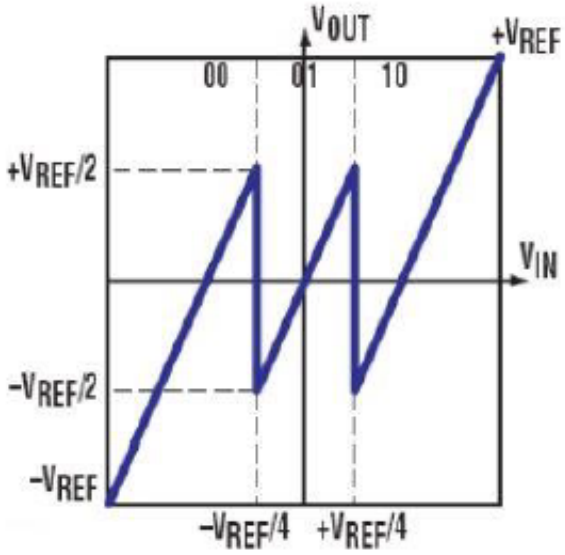
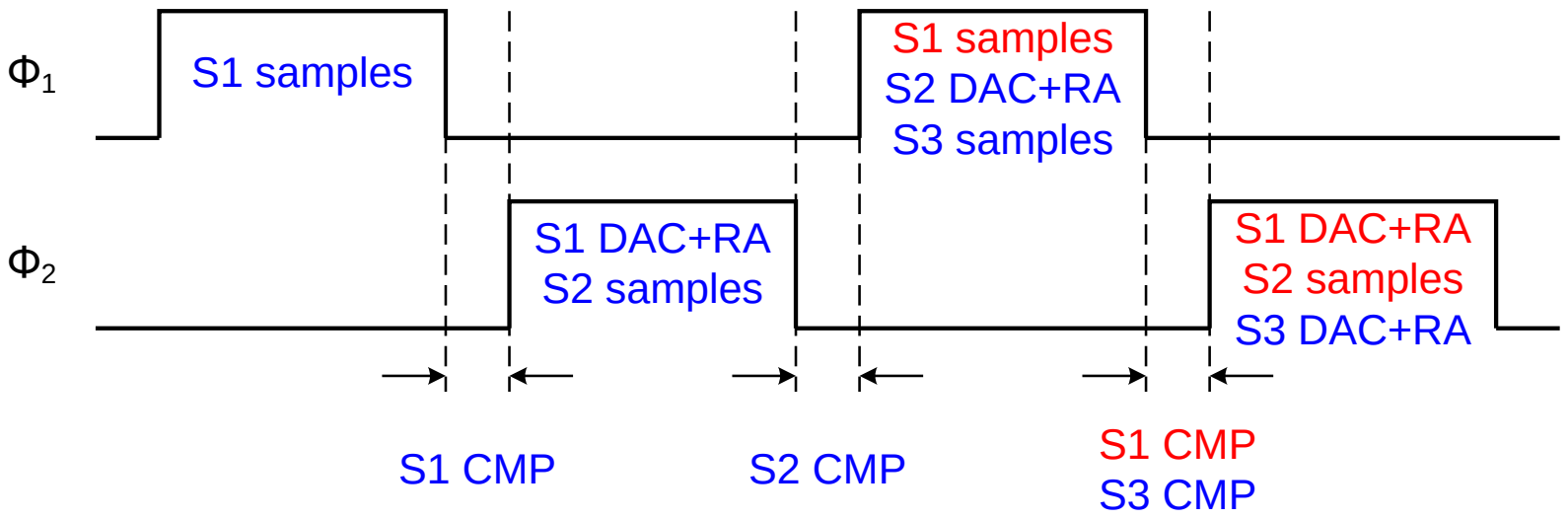
1.5-Bit Stage Architecture





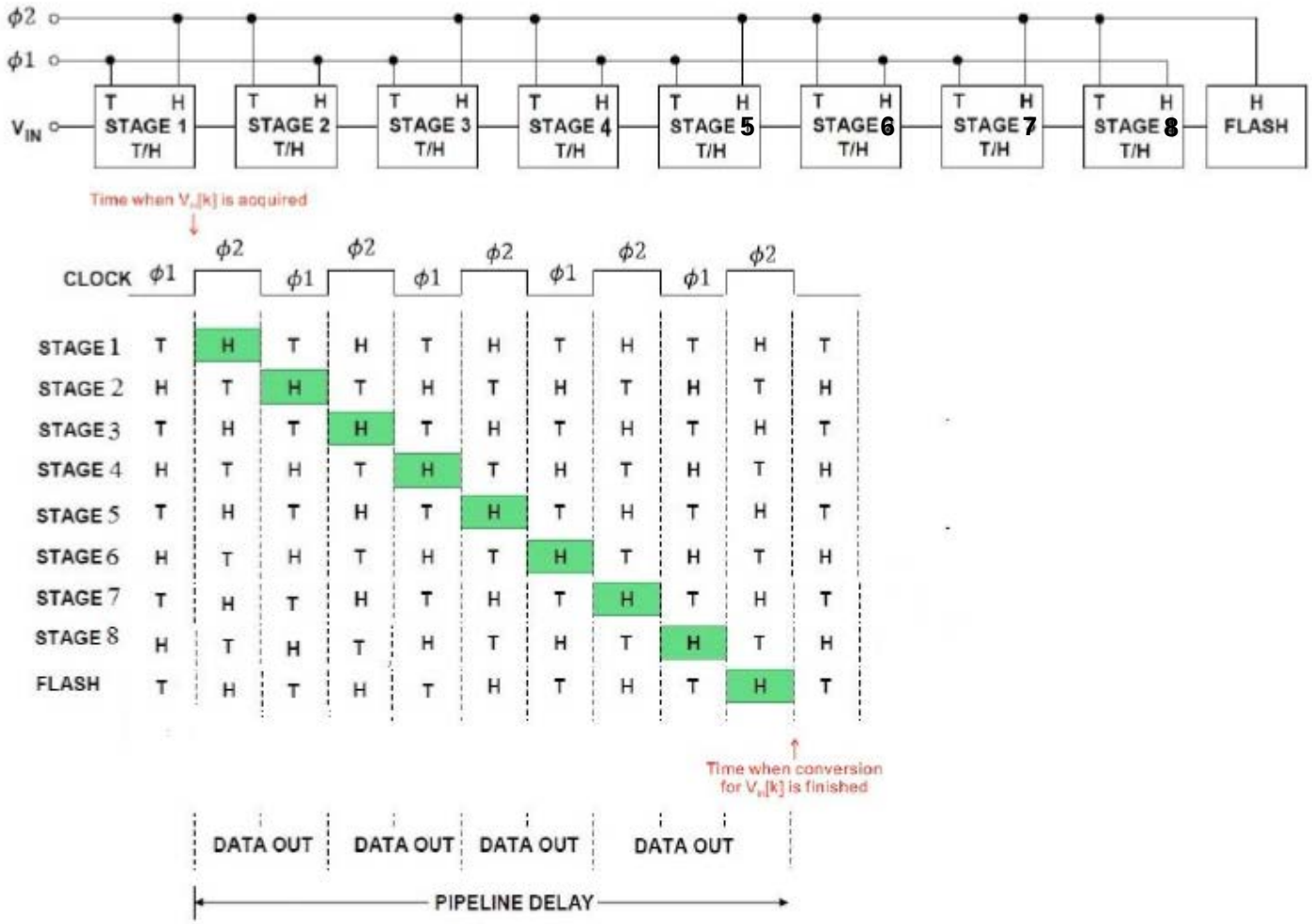
V_{IN}	Range	B1	B0	DAC O/P	Residue
$V_{IN} > V_H$	H	1	0	$+V_{REF}$	$2V_{IN} - V_{REF}$
$V_L < V_{IN} < V_H$	M	0	1	0	$2V_{IN}$
$V_H < V_L$	L	0	0	$-V_{REF}$	$2V_{IN} + V_{REF}$

Timing Diagram of Pipelining

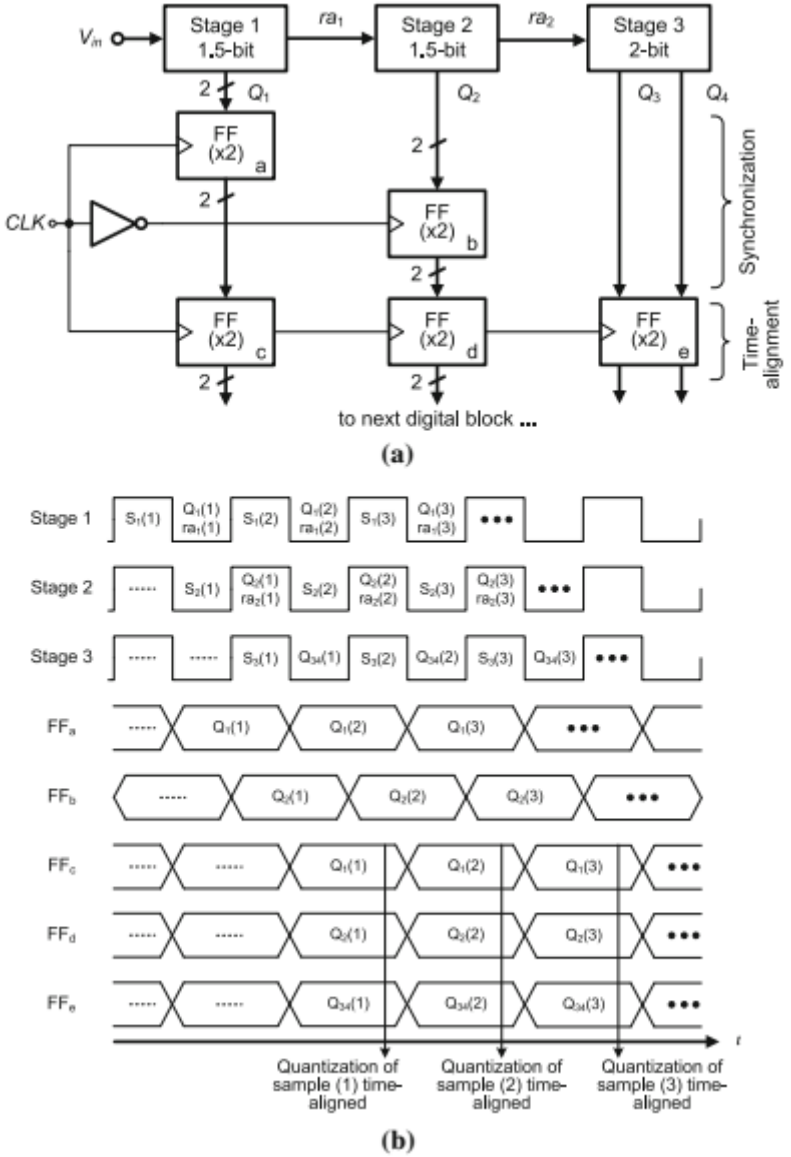


- Two-phase nonoverlapping clock is typically used, with the coarse ADCs operating within the nonoverlapping times
- All pipelined stages operate simultaneously, increasing throughput at the cost of latency

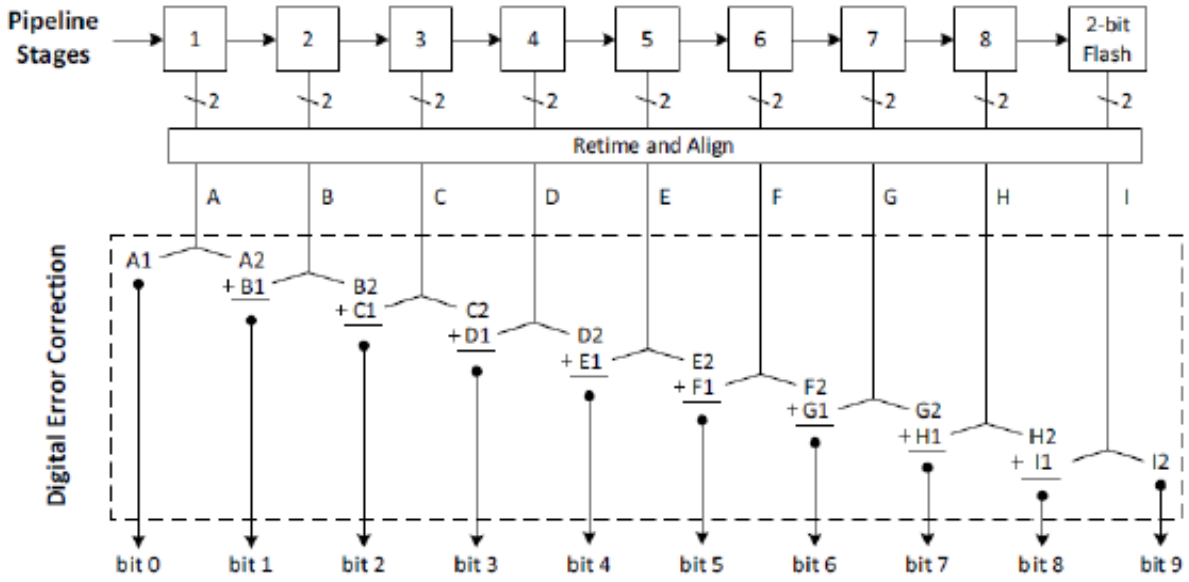
Timing of Pipeline Stages



Time-Alignment and Synchronization



Digital Error Correction



Digital Correction

$$V_o = \begin{cases} 2V_i - V_{ref} & \text{if } V_i > V_{ref}/4 \quad d = 2\,(10)_2 \\ 2V_i & \text{if } -V_{ref}/4 \le V_i \le +V_{ref}/4 \quad d = 1\,(01)_2 \\ 2V_i + V_{ref} & \text{if } V_i < -V_{ref}/4 \quad d = 0\,(00)_2 \end{cases}$$

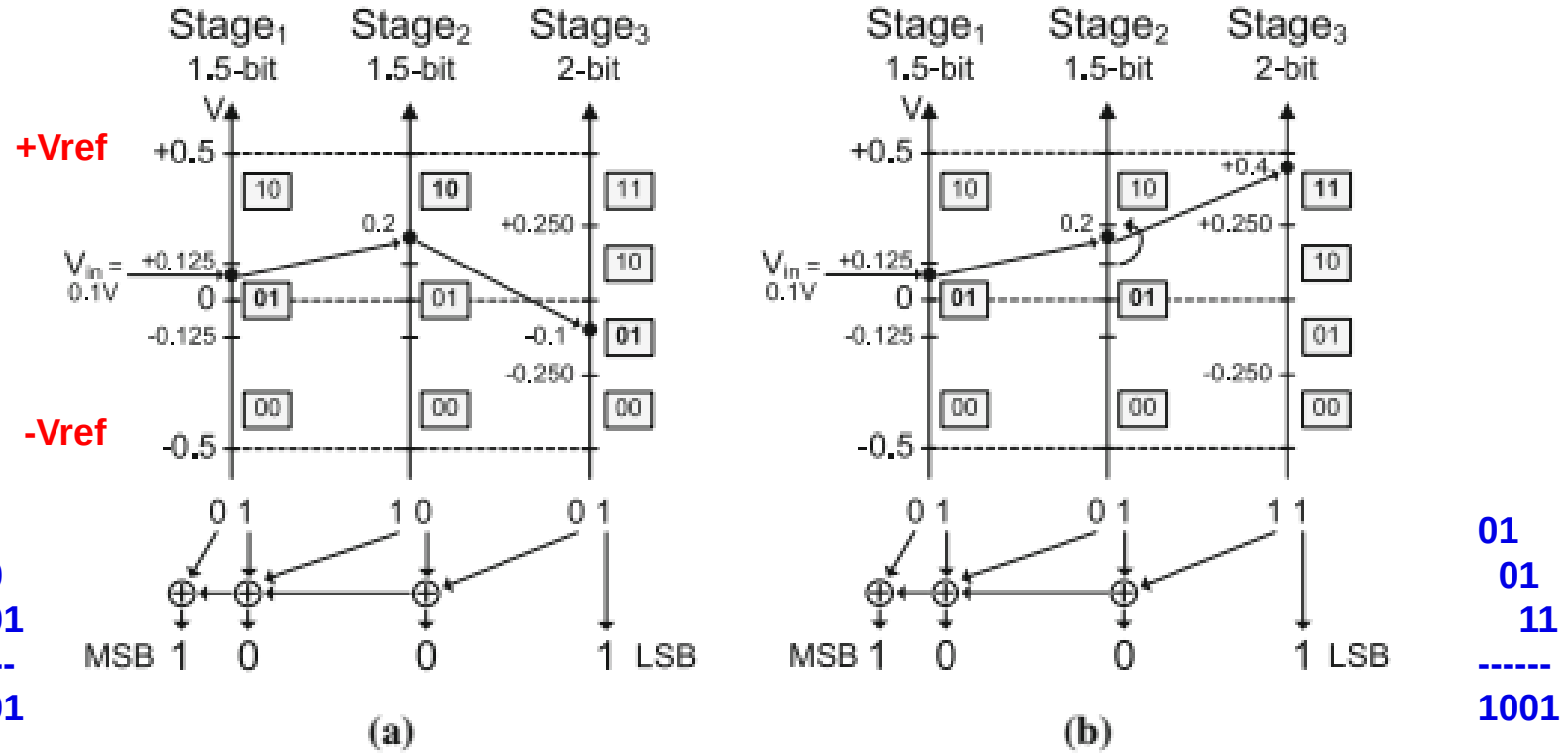


Fig. 2.15 Example of the operation of digital correction: **a** Ideal situation (and indecision corrected). **b** Offset error in stage 2: offset corrected

10-Bit ADC Example

1	0		
	0	1	
		0	0
1	0	1	0

Table 4.3: Example of digital error correction

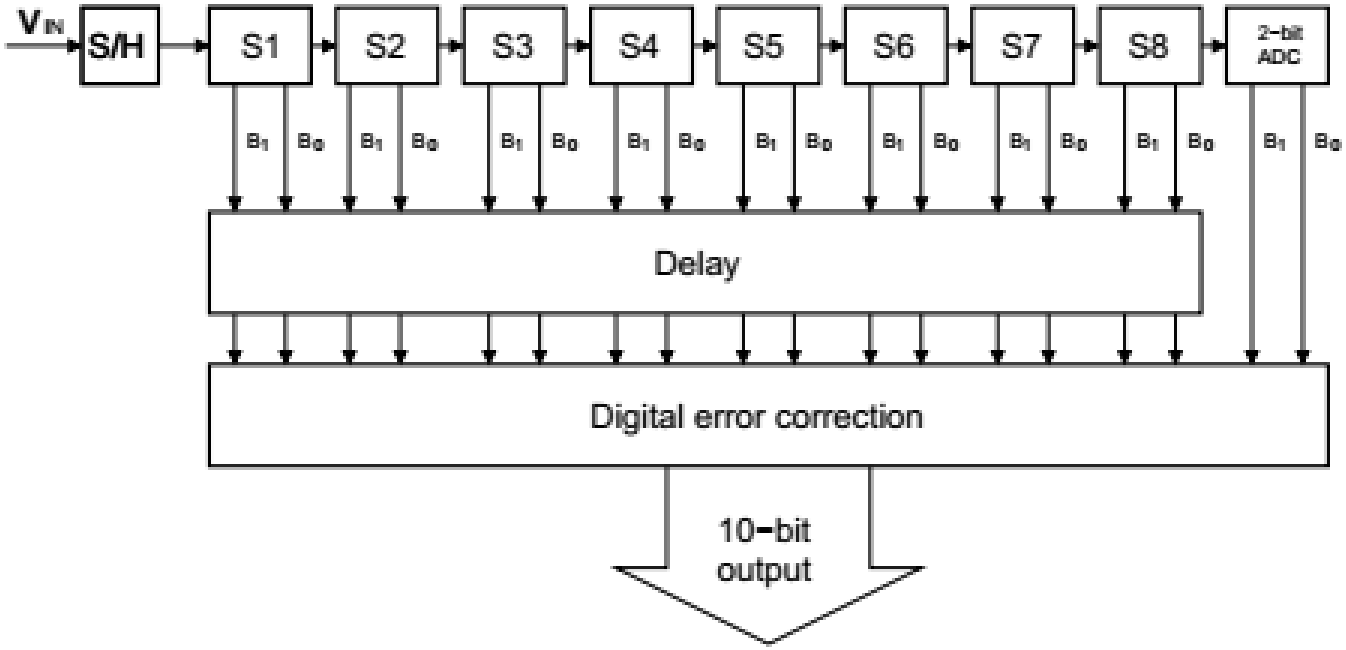


Figure 4.8: The final structure of the pipeline

Pipelined ADC Features

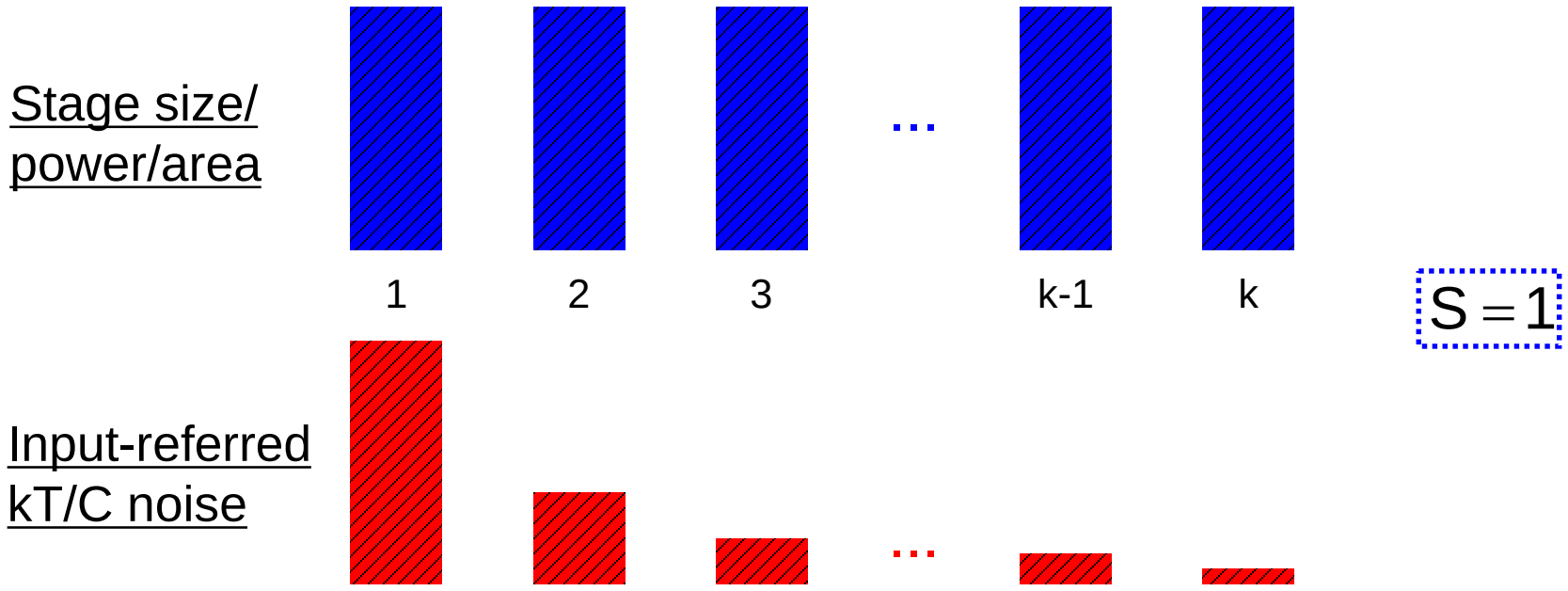
Features

- Architecture complexity is proportional to the resolution $N = \Sigma n_j$
- Throughput is significantly improved relative to algorithmic or SAR
- Digital redundancy works the same way as algorithmic
- Inter-stage gain enables stage scaling to save power and area

Limitations

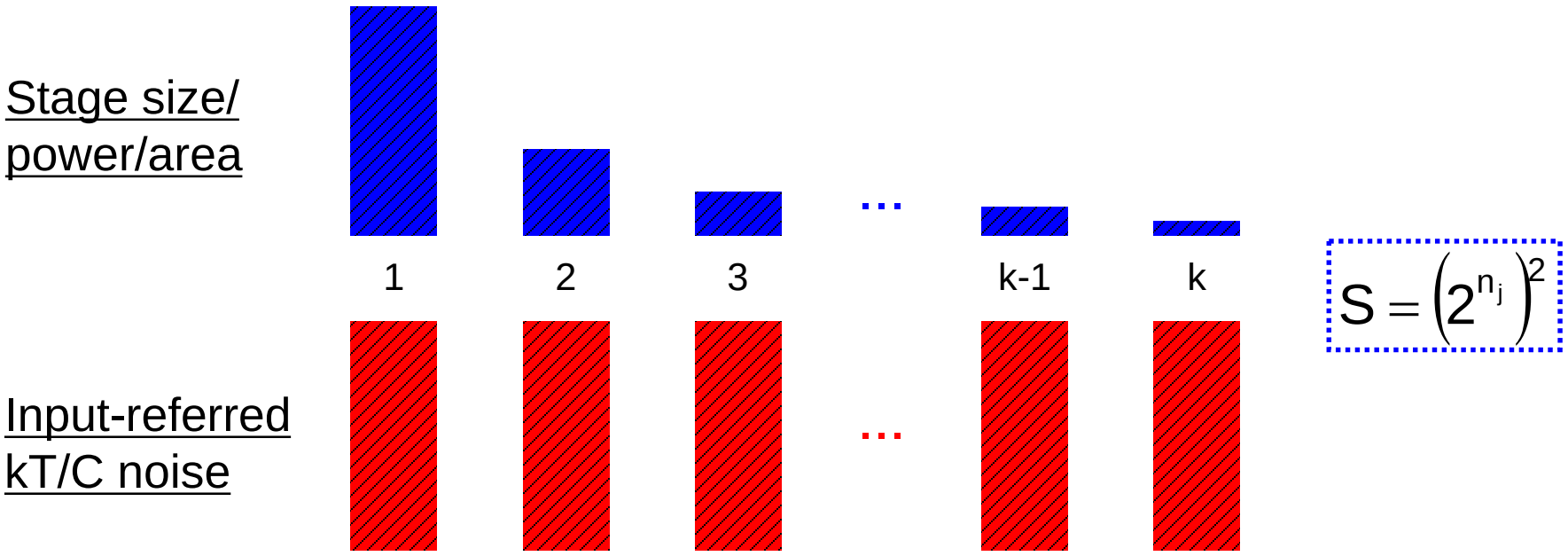
- Typically 3 conversion operations are involved
  - Sample-and-hold
  - Sub-ADC comparison
  - Sub-DAC and residue generation
- High-gain op-amps are required to produce residue signals with certain accuracy, which limits the conversion speed
- Long latency may be problematic for certain applications

No Stage Scaling



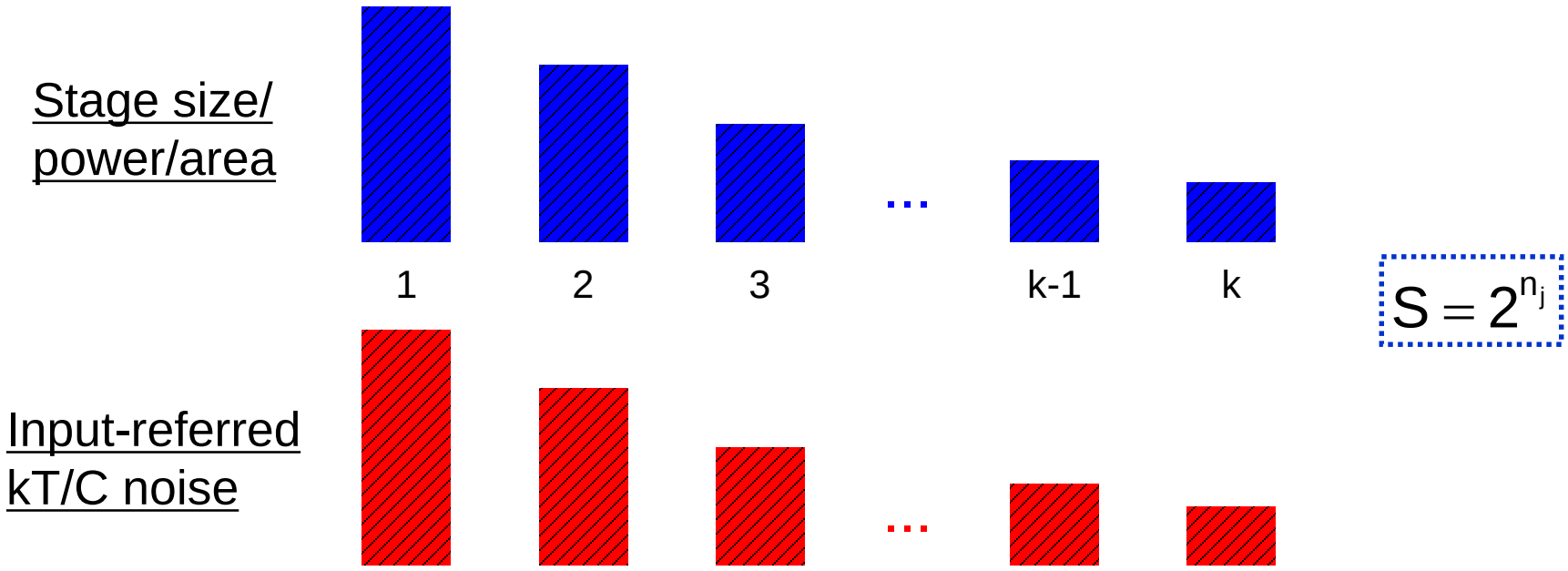
- All stages identically sized – same capacitors, op-amps, comparators
- Later stages are clearly oversized due to inter-stage gains

Aggressive Stage Scaling



- Stages sized such that the input-referred noises are identical
- Later stages are clearly downsized too aggressively

Optimum Stage Scaling



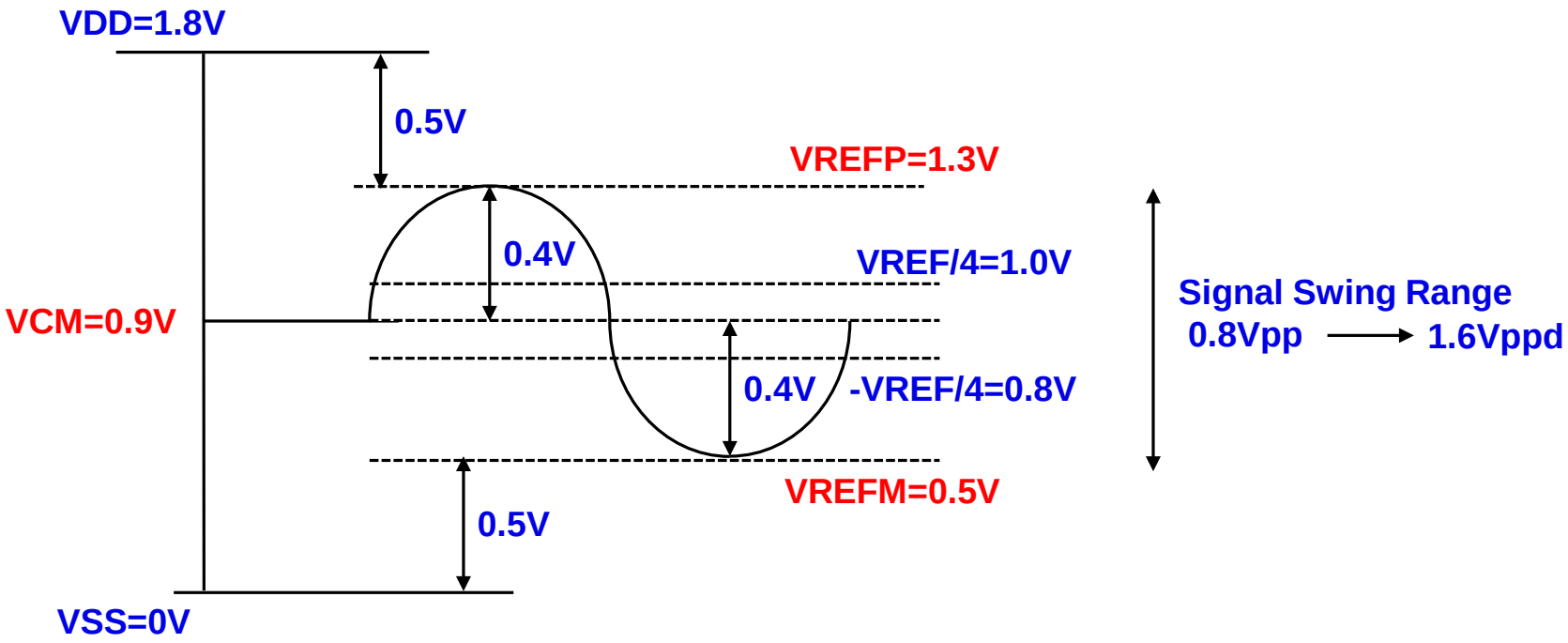
Optimum scaling lies in between the two extremes $\rightarrow S \approx 2^{n_j}$

Class Project: 10-bit Pipelined ADC

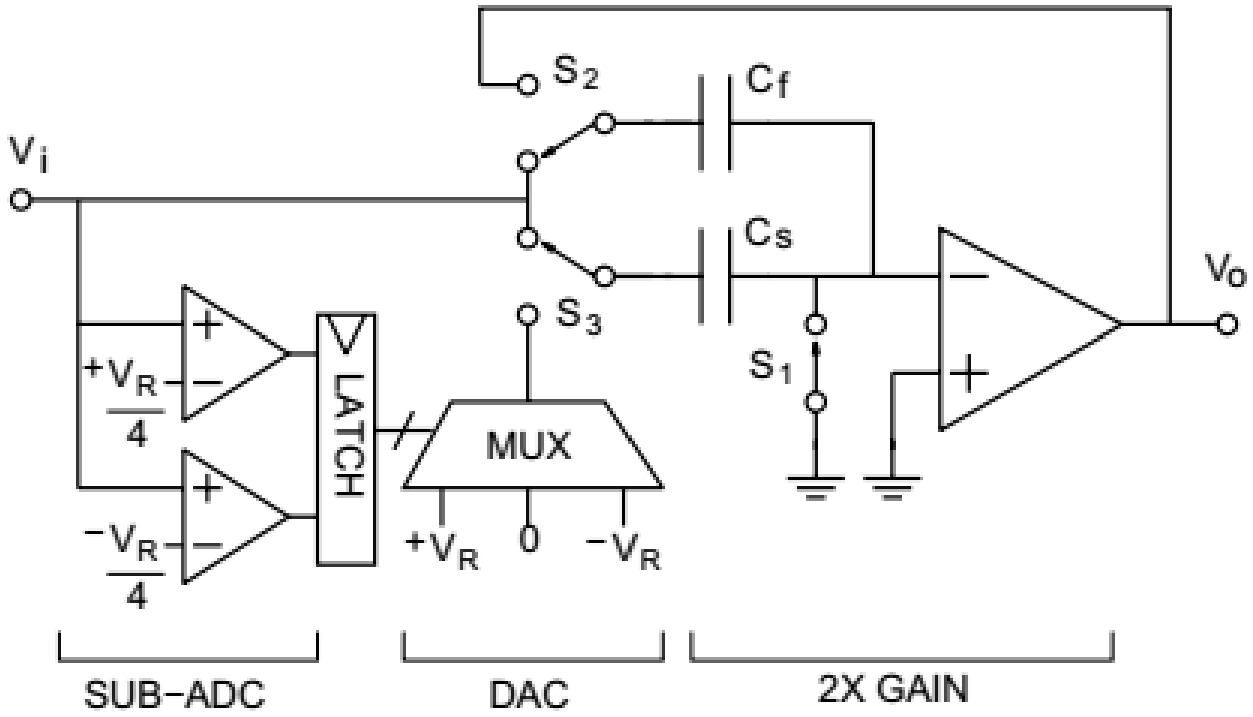
Process Technology	45nm CMOS with 0.18um I/O devices
Supply Voltage	VDD = 1.8V ± 5%
Temperature Range	0 ~ 70 ºC
Sampling Rate, Fs	100 MS/s
Input Full Scale, VFS	1.6 Vppd
Input Frequency	1 ~ 10 MHz
FoM	< 3.6 pJ/conv. step (To be confirmed)
Process Corners	TT, FF, SS

- All performance numbers to be confirmed.
- Use Ideal capacitor cell “cap” from analogLib
- Use “ideal_bias” cell in ee288lib for master current sources
- Use “ideal_clock” cell in ee288lib for 2-phase non-overlapping clocks
- Use Ideal DC voltage source for all voltage references such as VREFP, VREFM, and VCM

Signal Swing in Project



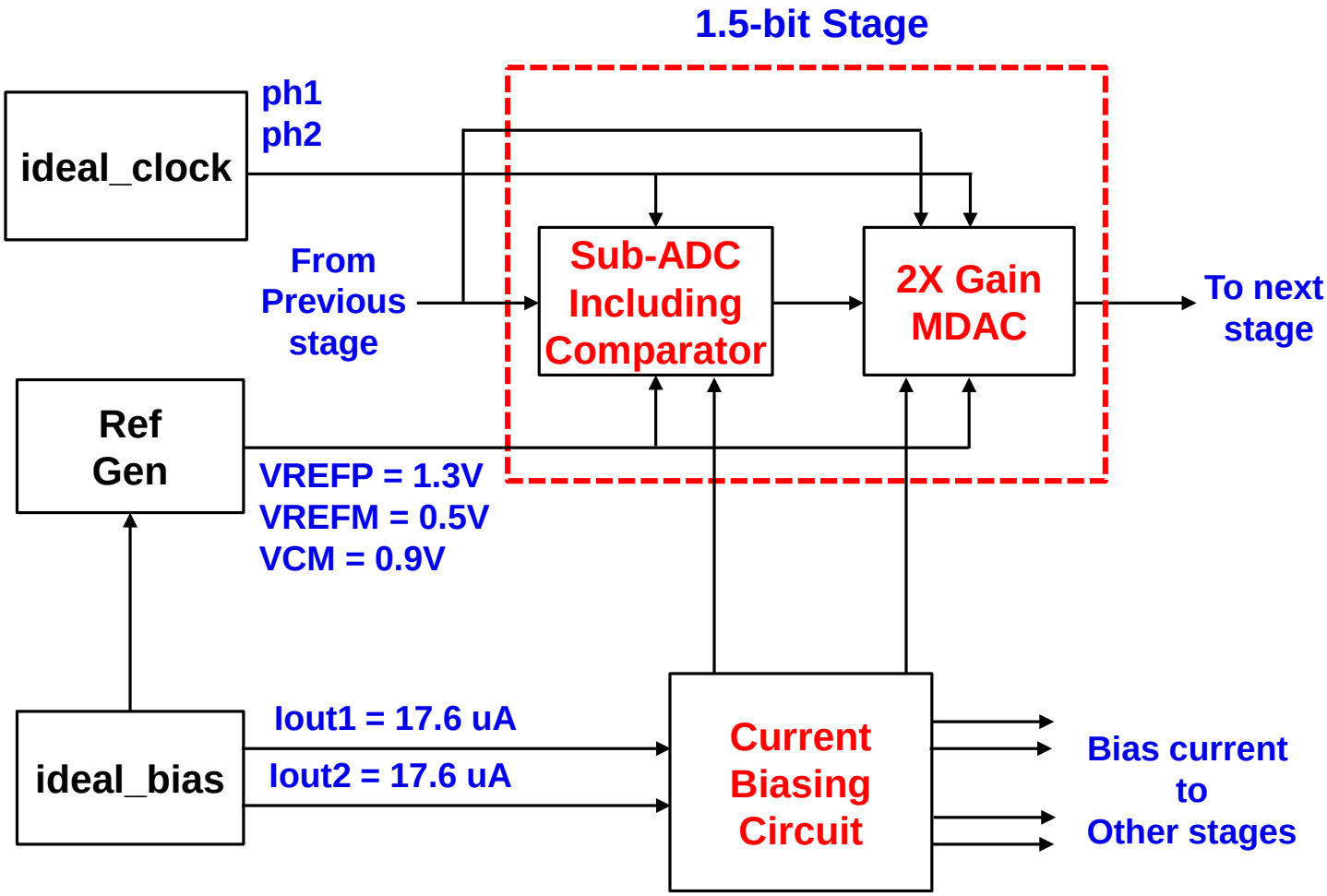
1.5-Bit Stage Architecture



Reference Paper:

A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999

Key Blocks To Design in the Project



Project Scoring Rule

Total point			**40**
Condition 1	**Functional Fully-Differential 10-bit Pipelined ADC**		**10**
		Typical corner (TT, 1.8V, 27C)	
		Vin (0.5V to 1.3V)	
		fin = (cycles/N) * fs where cycles=7 and N=64	
		Fs = 100 MSPS	
		Ideal switches	
		Ideal opamp	
Condition 2	**Condition 1 plus**	**Real switches**	**5**
Condition 3	**Condition 2 plus**	**Real opamp**	**5**
Condition 4	**Condition 3 plus**	**Meeting FoM requirement at Typical corner**	**5**
Condition 5	**Condition 4 plus**	**Meeting FoM requirement at PVT corner**	**5**
		TT, FF, SS, 1.8V +- 5%, 0-70C	
Presentation (10 min)			**5**
Project report in 4-page IEEE conference paper submission format			**5**
Extra point		**Publication level papers**	**10**

Items to prepare for project presentation

- Summary of your design
- Schematics
- Simulation Test Bench
- Simulation Results
  - OPAMP
  - Comparator
  - 1-stage operation
- FFT plot for the whole ADC

Presentation Score Breakdown

- 20% for Neatness and clearness of the presentation materials to check if the slides are done professionally or not
- 20% for block functionality to check if the individual block design is functional or not
- 10% on if you answered the questions correctly or not in the Q&A session following your presentation

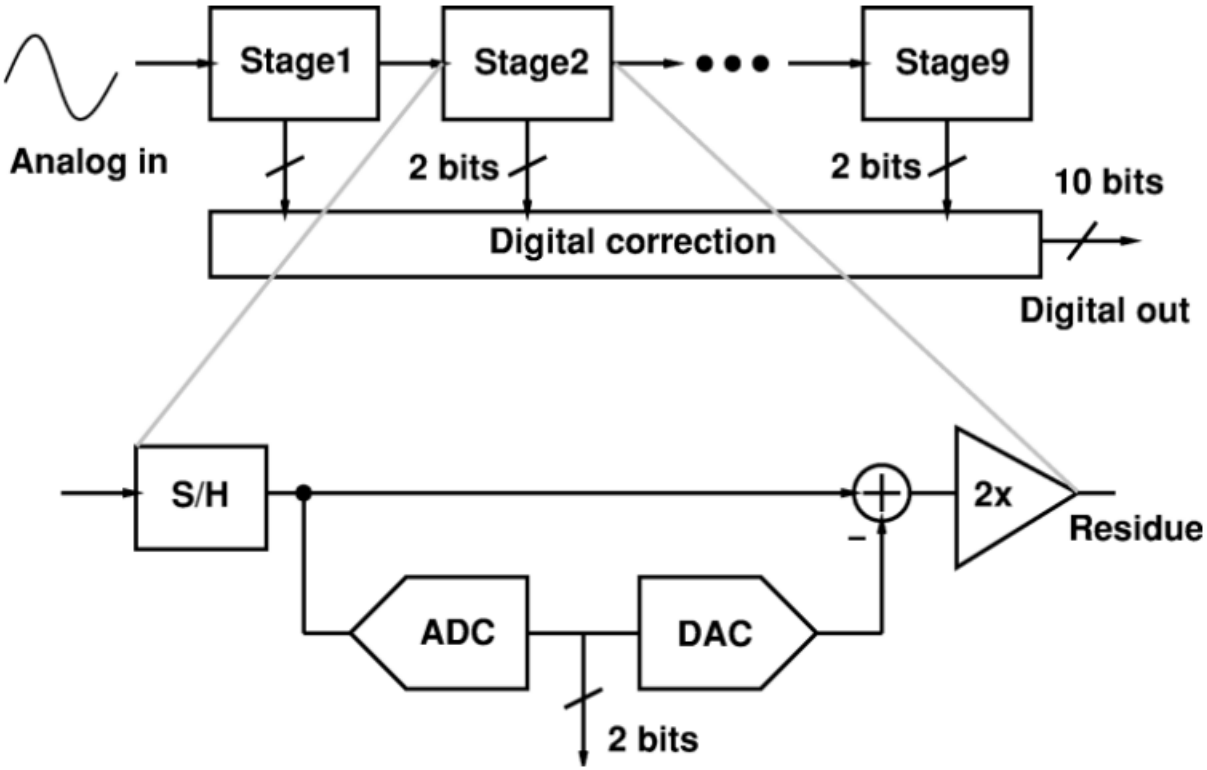
Project Report Guideline

- Use the IEEE template file uploaded in project folder in Canvas
- Total report length should be 4-pages
- Report should include the following sections
  - Abstract
  - Introduction
  - Main sections
  - Conclusion
  - References

Project Report Score Breakdown

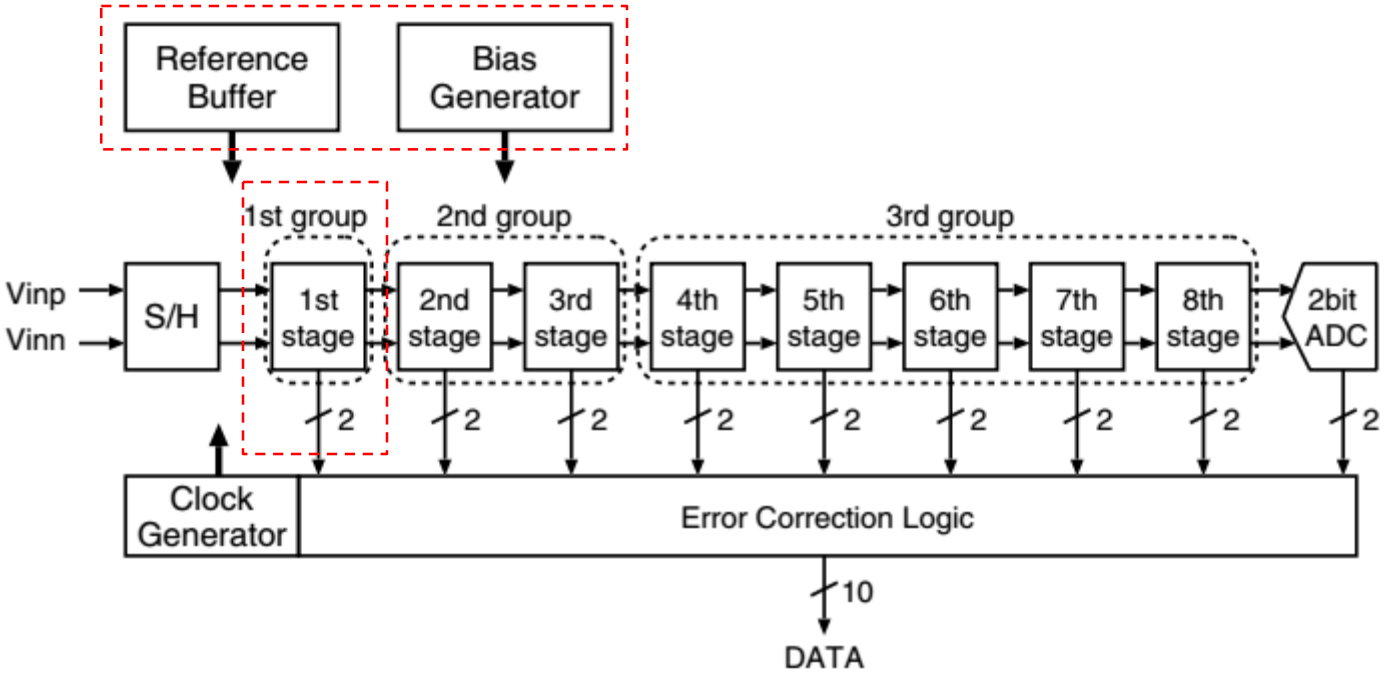
- 20% for Neatness and clearness to check if the report is done professionally and if the report follows IEEE format
- 20% for block functionality to check if the individual block design is functional or not
- 10% for full block functionality - if your team cannot show the full functionality, all of your team score will be affected.
- Extra credit for publication-level report

10-bit Pipeline ADC from [Ref. 1]



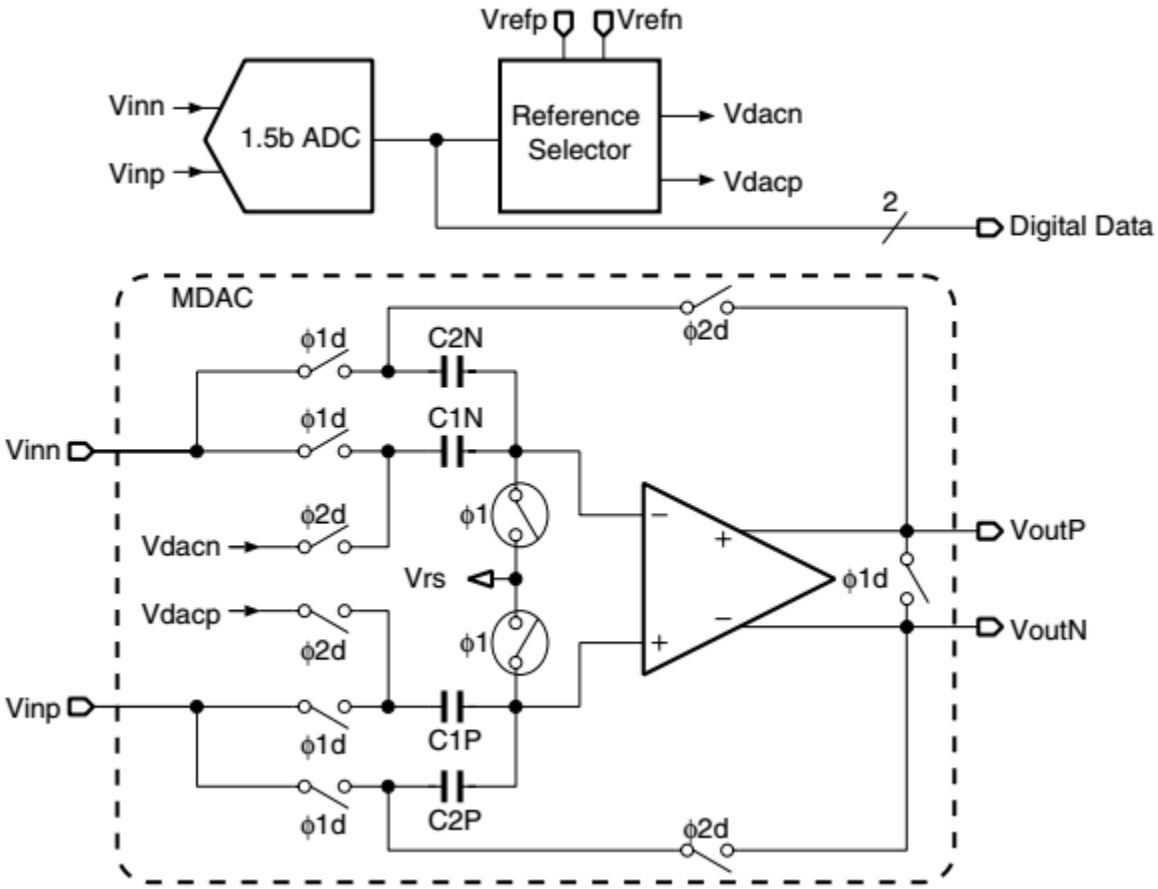
[Ref. 1] A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999.

10-bit ADC Architecture from [Ref. 2]



[Ref. 2] H. Ishii, K. Tanabe, and T. Iida, “A 1.0V 40mW 10b 100MS/s Pipeline ADC in 90nm CMOS,” *IEEE Custom Integrated Circuits Conference*, pp. 10.5.1–10.5.4, 2005.

Project : 1.5-bit Pipeline Stage [Ref. 2]



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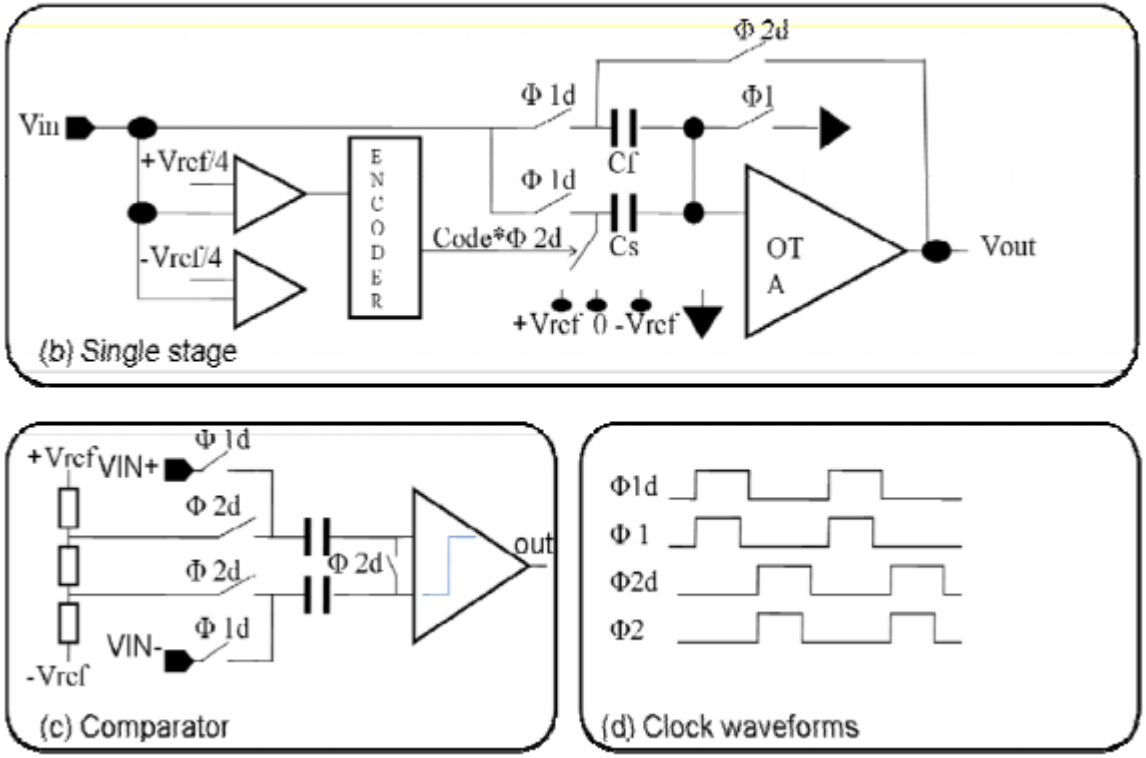
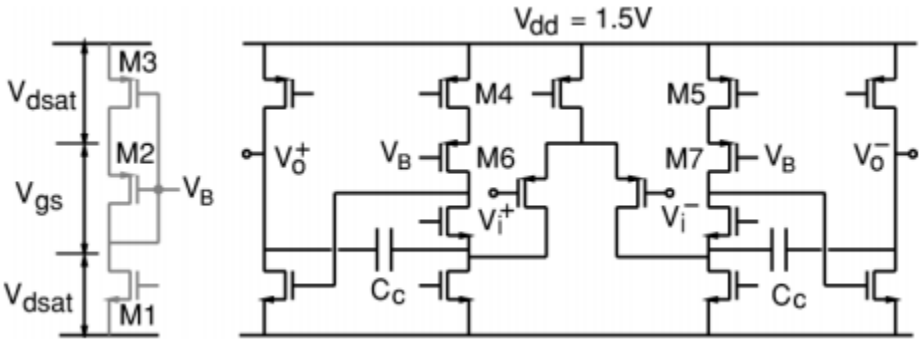
Project : 1.5-bit Pipeline Stage [Ref. 3]

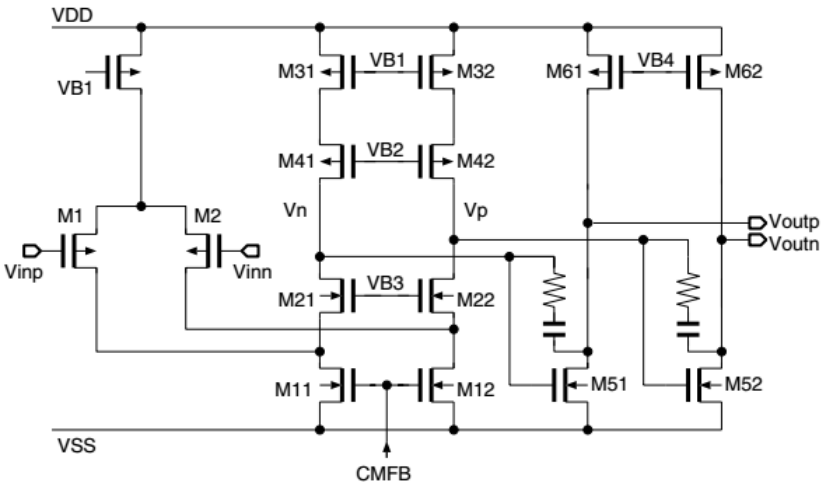


[Ref. 3] M. Boulemnakher, “A 1.2V 4.5mW 10b 100MS/s Pipeline ADC in 65nm CMOS,” *IEEE International Solid-State Circuit Conference*, pp. 250-251, 2008

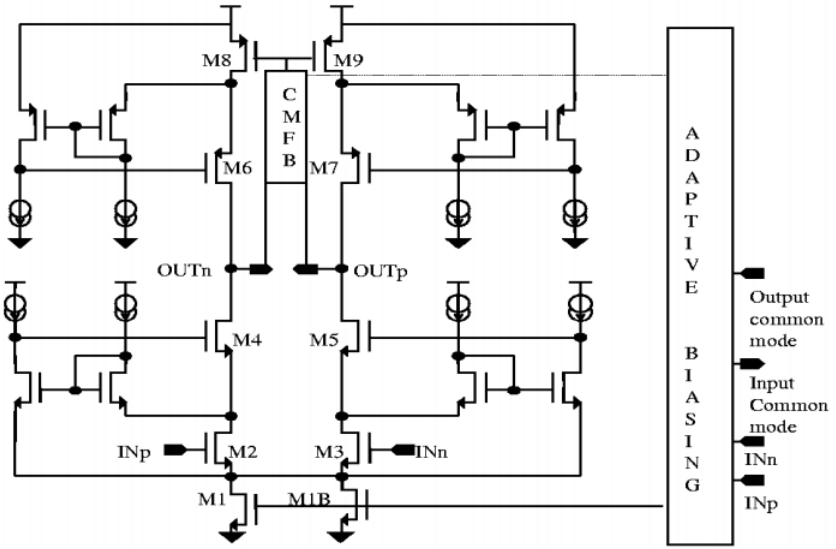
Example OPAMP Circuits



[Ref. 1]

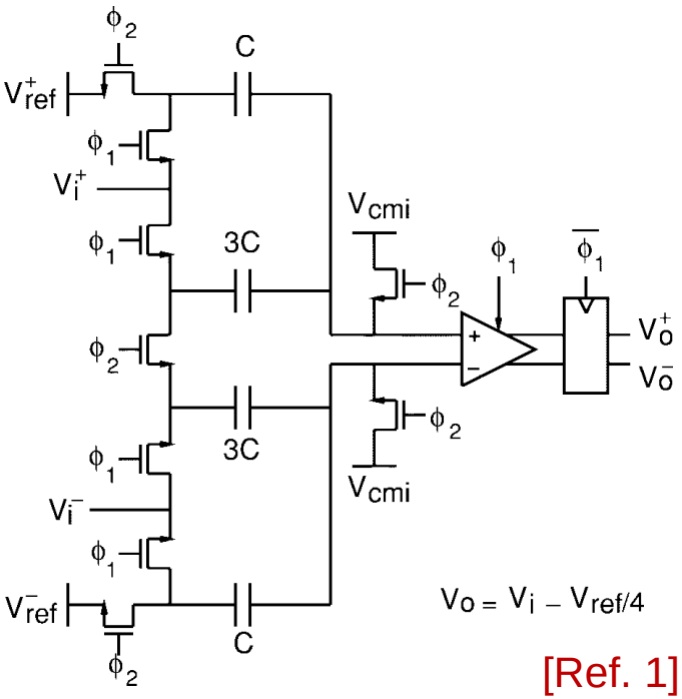


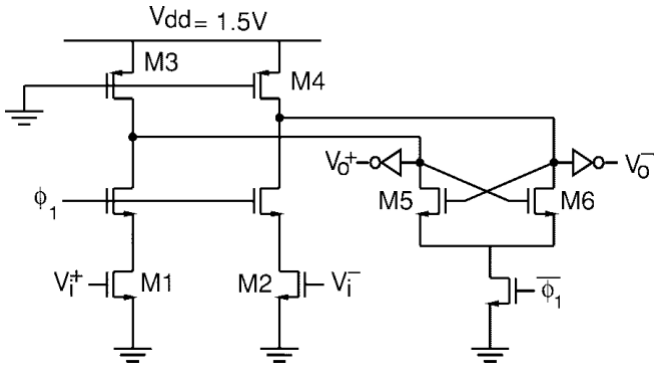
[Ref. 2]



[Ref. 3]

Comparators





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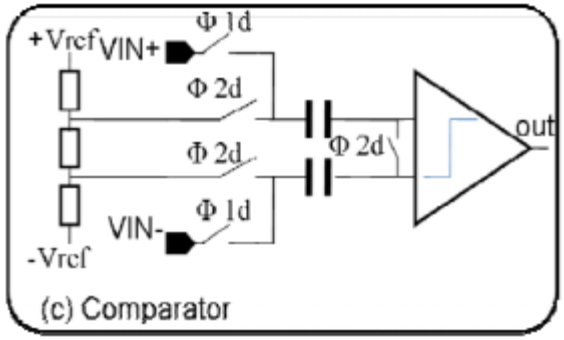


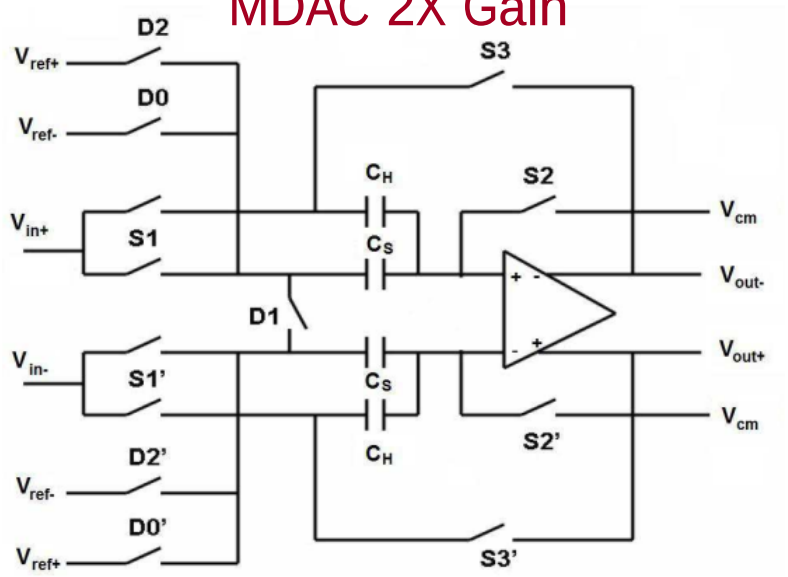
[Ref. 3]

MDAC

B_1	B_0	D_0	D_1	D_2
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	X	X	X

Sub-ADC to DAC Bit Logic

MDAC 2X Gain



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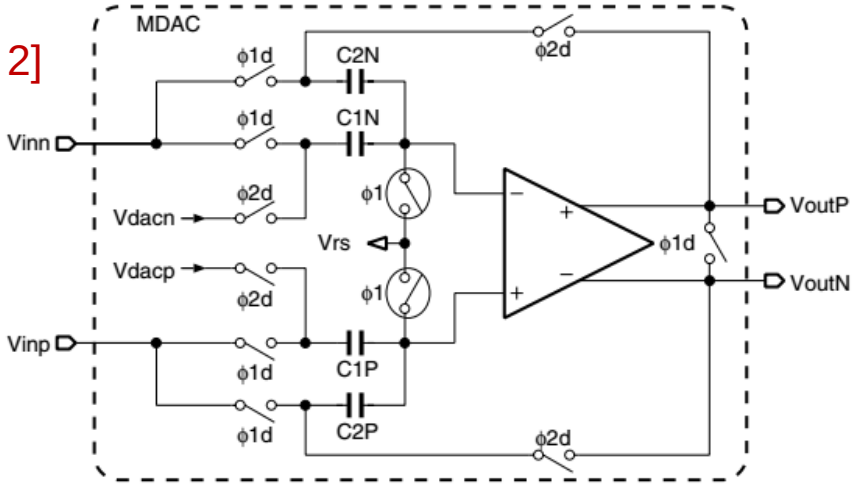

References

1. A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–606, May 1999

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3. M. Boulemnakher, “A 1.2V 4.5mW 10b 100MS/s Pipeline ADC in 65nm CMOS,” ISSCC, pp. 250-251, 2008

4. M. E. Bayoumy, *MS Thesis, University of Texas, Austin*, A Study of 10-bit, 100Msps Pipeline ADC and the Implementation of 1.5-bit Stage, 2013

5. Overview of Pipelined ADC Chapter 13 from the book by M. Figueiredo et al., Reference-Free CMOS Pipeline Analog-to-Digital Converters, 2013