I would like to summarize key takeaway points for the materials you learned from EE288 class.

1.To start-off, all data converters use comparators and/or opamps as the basic building block to implement a binary search algorithm.

2. For high-speed & lower resolution up to about 6-bit applications, Flash ADC is the best choice. High speed comparator design will be challenging, but doable. Offset cancellation either at the input capacitor or output capacitor, or combination of the two are used by using 2-phase clocks.

3. Clocked-comparator based on preamp and regenerative latch is frequently used to overcome several non-ideal effects such as offset and kickback noise of the regenerative latch. Two-phase clock is necessary.

4. The offset of the latch or differential pair in the preamp is mostly from threshold voltage variation of the matched pair transistors. The mismatch can be reduced by choosing larger size as the delta-vth will be proportional to the inverse square root of the transistor area (W*L) from Pelgrom's mismatch model. The same argument for the current mirror mismatches.

5. When you design a current mirror, try to use high-swing cascode structure. We have spent enough time on how to design the high-swing cascode circuit. This is very important as it will be used extensively in opamp design.

6. The main current mirror transistors at the bottom need to have large channel length and the cascode transistor can have minimal channel length. The cascode biasing leg will have a bottom transistor that is in Triode region. Other than this transistor, all the other transistors need to be in Saturation except the switches in Switched-Capacitor circuits.

7. Switched-Capacitor circuit consist of switches, capacitors, and opamp in negative feedback configuration. To operate the SC circuits, you need two-phase non-overlapping clocks. And the switches can be implemented by NMOS, PMOS, CMOS, and bootstrapped switches. NMOS is a good switch if the signal level to process is low. PMOS will be good if the signal level is high. CMOS will be good for all signal levels. However, the switches at the input sampling capacitors will have signal-dependent nonlinearity as the gate overdrive voltage (vgs–vth) will be signal-dependent. Therefore, you want to use bootstrapped switch in this case.

8. There are two non-ideal switch errors when the switch turns off. They are channel charge injection and clock feedthrough. When the switch turns off, the channel charge need to go either to the left or right. This will introduce charge injection error. Clock feedthrough is due the Cgs and Cgd of the transistor.

9. To mitigate these errors, we typically employ the so-called bottom plate sampling. This means you turn off the bottom plate a little early compared to the top plate of the sampling capacitor. Therefore, when you create two-phase clocks, you need to generate early or advanced clock signals.

10. There is a confusion about the bottom plate. But when you connect the capacitor around the opamp, make sure not to connect the bottom plate to the summing node of the opamp as this will reduce the feedback factor.

11. Feedback factor β is often the ratio of capacitors or ratio of resistors. It represents how much output signal you are feeding back to the input side.

12. The gain error of the SC circuit is given by 1/βA and the settling error is related to the bandwidth of the amplifier. Therefore, for a certain resolution and sampling rate of the ADC, you need to calculate the amount of opamp gain and bandwidth based on error tolerance.

13. For medium speed applications, pipelined ADC is a good choice. As the pipelined ADC

consists of a number of stages, it is important to design the Pipeline stage to meet the required spec. Typically the first stage is the most power consuming block and the subsequent stages can be scaled down with the same structure.

14. Each pipeline stage can produce multiple bits. But 1.5-bit/stage is very popular as it can achieve high-speed operation. The 1.5-bit stage requires 2-comparators, sub-ADC logic, and the MDAC with gain of 2.

15. The MDAC requires a fully-differential opamp with enough gain and speed. As the opamp is fully-differential, you need a common-mode feedback (CMFB) circuit to set the DC level correctly. In switched-capacitor circuit, it is advantageous to use switched-capacitor CMFB as there is no signal swing constraint.

16. There are many types of OPAMP you can use in SC circuit, but Folded-cascode with gain-boosting is a good choice. For this, you need to design sub-opamp that can be folded-cascode again. Don't make the sub-opamp too fast and make sure to design the high-swing cascode bias circuit correctly to use it here.

17. We have spent some time to use Matlab and VerilogA coding to use in the homework and project. Try to be hands-on on these as it will be useful, and they may ask you if you go to an interview.

18. We also used quite a lot of circuits using ideal elements. It is a good idea to build an ideal circuit before you build a real circuit as the performance of the ideal circuit will be a good reference to the real circuit performance.

19. In ADC and DAC testing, we use the FFT plot to find out the ENOB and SNR. Make sure to use coherent sampling, i.e., the input signal frequency needs to have certain relationship with the sampling clock and the FFT size. If you don't choose the correct signal frequency, you will get spectrum leakage and the FFT plot will show this. Of course, you can use windowing, but it is always a good practice to use the coherent sampling.

20. There are other ADC architectures such as SAR ADC and single-slope ADC and the Oversampling ADC we discussed in the class. The SAR ADC is becoming very popular these days as it uses comparator instead of opamp, which is the most power-hungry block in the pipelined ADC.

21. However, the SAR is slow. Therefore, the people are using many SAR ADCs in parallel in time-interleaving (TI) manner to create high-speed ADC. Another popular architecture is the so-called Pipelined SAR or SAR assisted Pipeline ADC. In this hybrid architecture, you use SAR ADC instead of Flash ADC in the pipeline stage design. This is typically done when you use multi-bit (5 or 6-bit/stage) in pipelined stage. This type of hybrid ADC are very popular these days along with time-interleaving. This class of ADC is called Time-interleaved ADC.

22. The Oversampling ADC is typically implemented along with noise shaping function to implement high resolution ADC. For this we use integrator in the forward path. Depending on the number of integrators, we can create higher order oversampling ADC. Each time you double the sampling rate, you will get 0.5-bit (3dB) improvement in ENOB. If you use noise shaping along with the oversampling, each time you double the oversampling rate on the 1-st order noise shaping ADC, you get 1.5-bit (9dB) ENOB improvement, whereas the improvement will be 2.5-bit (15dB) for 2nd order noise shaping ADC.

23. In case of DAC, a capacitor array can be used to implement charge re-distribution SAR type DAC. The capacitor array is typically binary weighted. To reduce the array size, we can use two sections of cap array connected by a coupling cap. In these cap array-based DAC architecture, dynamic power is significant when you are going through the SAR logic switching. Therefore, techniques or algorithms to reduce the switching energy is an active research area.

24. Another popular DAC architecture is current steering DAC. There are binary weighted DAC, unary or unit element DAC or combination of the two, which is segmented DAC. The binary DAC is simple as you don’t need any decoding logic, but it has large DNL at major bit (MSB) transition. The unary DAC has good DNL performance, but it needs a large decoding logic if the resolution becomes high.

25. The Segmented DAC is the compromise of the binary and unary. And it is a good choice most of the time. The MSB array will be unit element and the LSB array will be binary weighted.

26. The design of the ADC and DAC requires simulating in a proper test bench configuration. Always try to use hierarchical design and make sure to understand how to simulate ac response of single-ended and fully-differential opamp.

27. Lastly but not the least, you need to brush off the basics in analog design. This requires understanding the golden equation, gm, ro, poles and zeros, the relationship between the DC gain, dominant pole, unity gain frequency, and the phase & gain margin to ensure the stability of the amplifier.