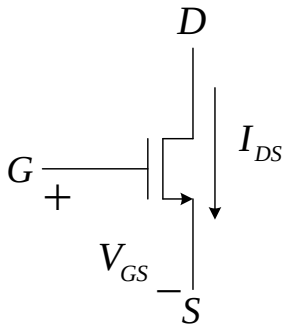
MOS CAPACITOR MODELS

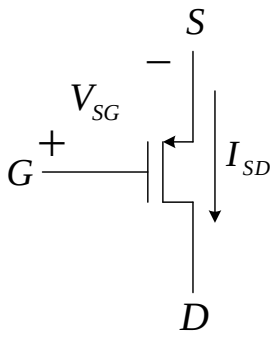
Lecture 7

- nMOSFET



Operation Regions	Voltages	Current
Cut Off	$V_{GS} \le V_{Tn}$	$I_{DS} = 0$
Saturation	$V_{GS} > V_{Tn}$ $V_{DS} > V_{GS} - V_{Tn}$	$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2\left(1+\lambda V_{DS}\right)$
Resistive	$V_{GS} > V_{Tn}$ $V_{DS} < V_{GS} - V_{Tn}$	$I_{DS} = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{GS} - V_{Tn}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$

- pMOSFET

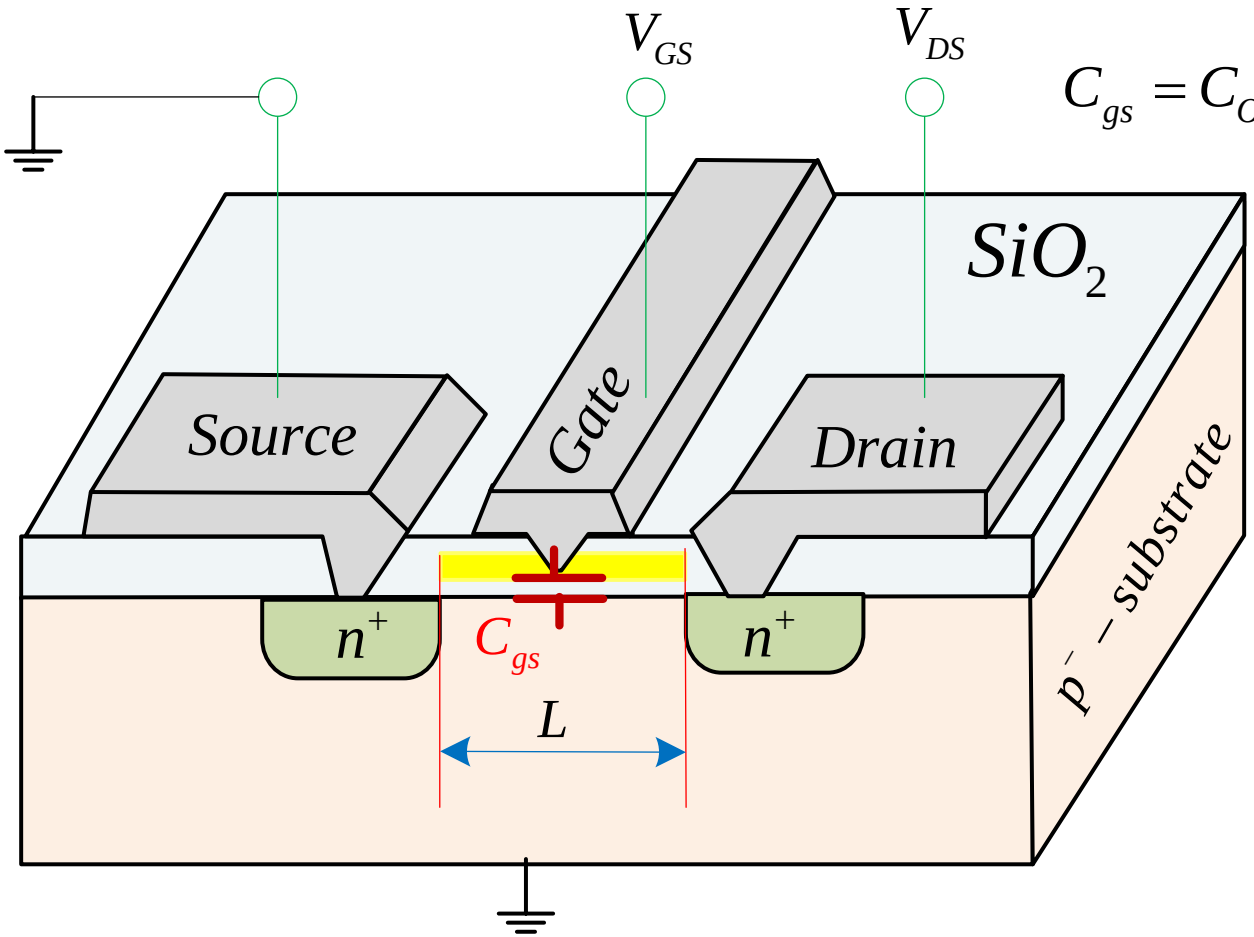


Operation Regions	Voltages	Current
Cut Off	$V_{SG} \le \lvert V_{Tp} \rvert$	$I_{SD} = 0$
Saturation	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} > V_{SG} - \lvert V_{Tp} \rvert$	$I_{SD} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG} - \lvert V_{Tp} \rvert\right)^2\left(1+\lambda V_{SD}\right)$
Resistive	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} < V_{SG} - \lvert V_{Tp} \rvert$	$I_{SD} = \mu_p C_{ox}\frac{W}{L}\left[\left(V_{SG} - \lvert V_{Tp} \rvert\right)V_{SD} - \frac{V_{SD}^2}{2}\right]$

- Enhancement mode MOSFET transistor region of operation

	Cut-off	Resistive	Saturation
nMOS	$V_{GSn} < V_{Tn}$ $V_{IN} < V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} < V_{GSn} - V_{Tn}$ $V_{OUT} < V_{IN} - V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} > V_{GSn} - V_{Tn}$ $V_{OUT} > V_{IN} - V_{Tn}$
pMOS	$V_{GSp} > V_{Tp}$ $V_{IN} > V_{Tp} + V_{DD}$	$V_{GSp} < V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{Tp}$ $V_{OUT} > V_{IN} - V_{Tp}$	$V_{GSp} = V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{Tp}$ $V_{OUT} < V_{IN} - V_{Tp}$

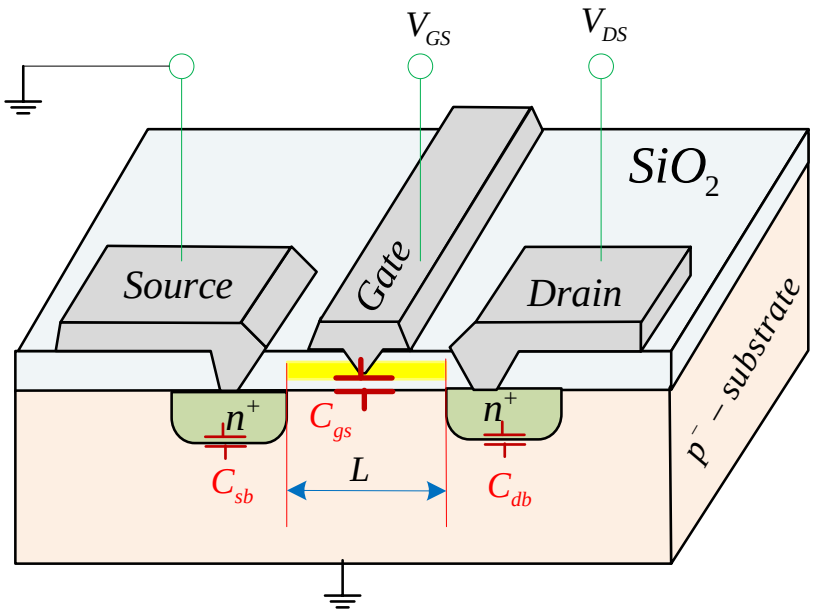
- Gate capacitance of Ideal MOSFET transistor



$$C_{gs} = C_{OX}WL = \frac{\varepsilon_{OX}WL}{t_{OX}}$$

- Approximated gate capacitance as channel connected to source

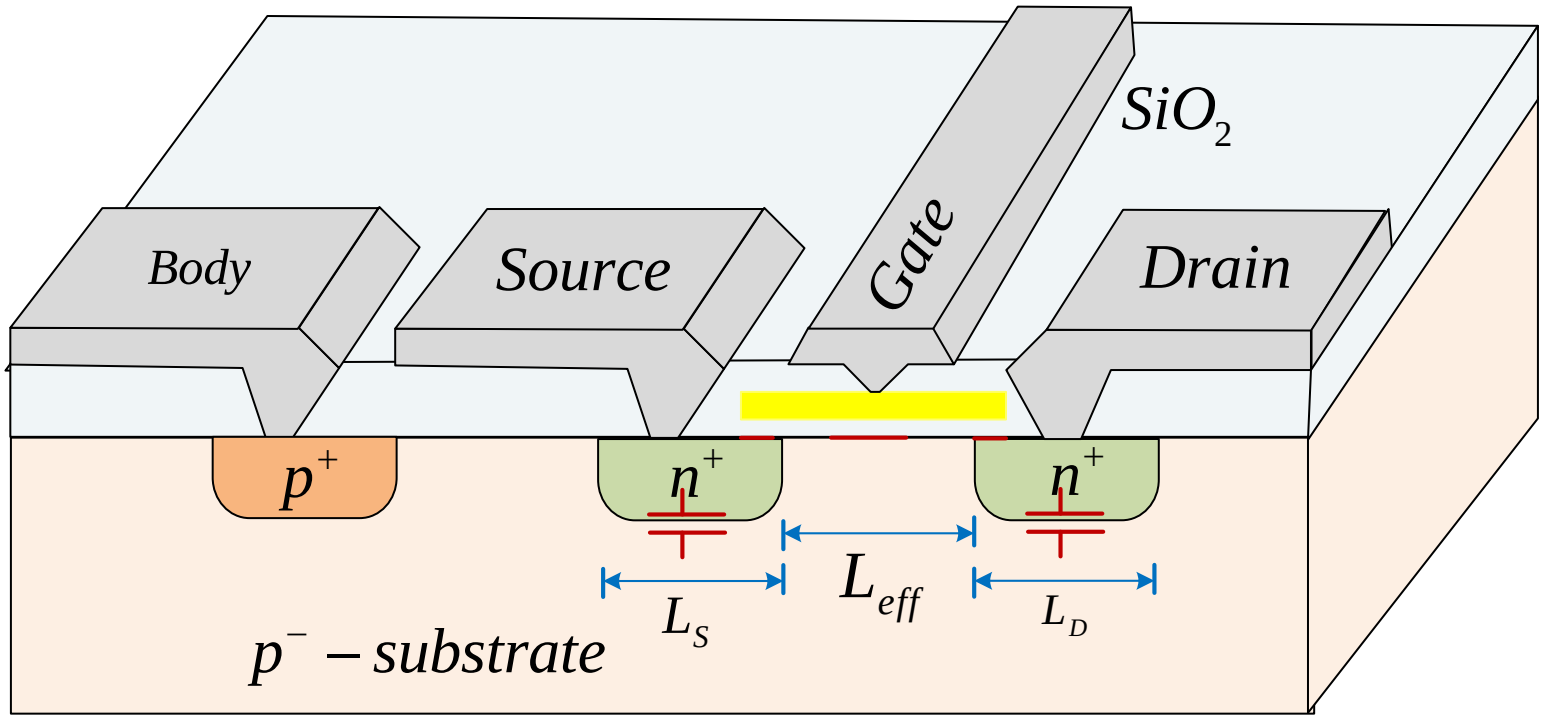
- Gate capacitance of Ideal MOSFET transistor



$$C_{gs} = C_{OX}WL = \frac{\varepsilon_{OX}WL}{t_{OX}}$$

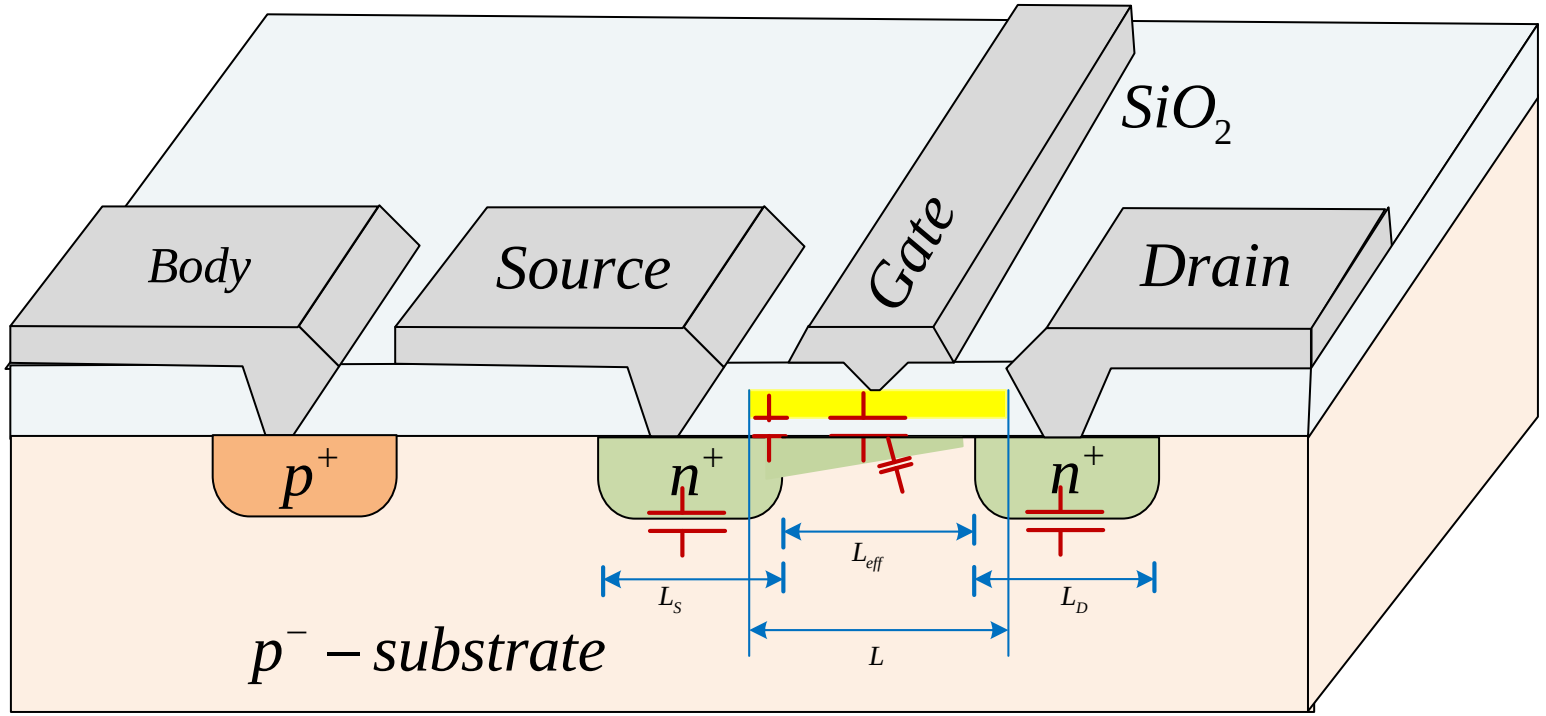
- Approximated gate capacitance as channel connected to source
- Capacitor across the reverse-biased Drain-Bulk C_{db}
- Capacitor across the reverse-biased Drain-Bulk C_{sb}

- Parasitic capacitors in the cut-off



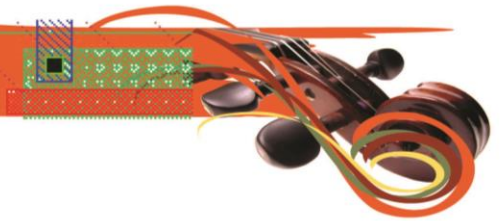
$$C_j = C_{j0}\left(1+\frac{V_{SB}}{V_0}\right)^n \qquad V_0 = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$$

- Intrinsic capacitors in the saturation $V_{GS} > V_{TN}$ & $V_{DS} > V_{GS} - V_{TN}$



$$C_{gate} = C_{gate-body} + C_{gate-source} + C_{gate-drain}$$

$$C_{gate} = 0 + \frac{2C_0}{3} + 0 = \frac{2C_0}{3}$$



- Intrinsic MOS gate capacitor

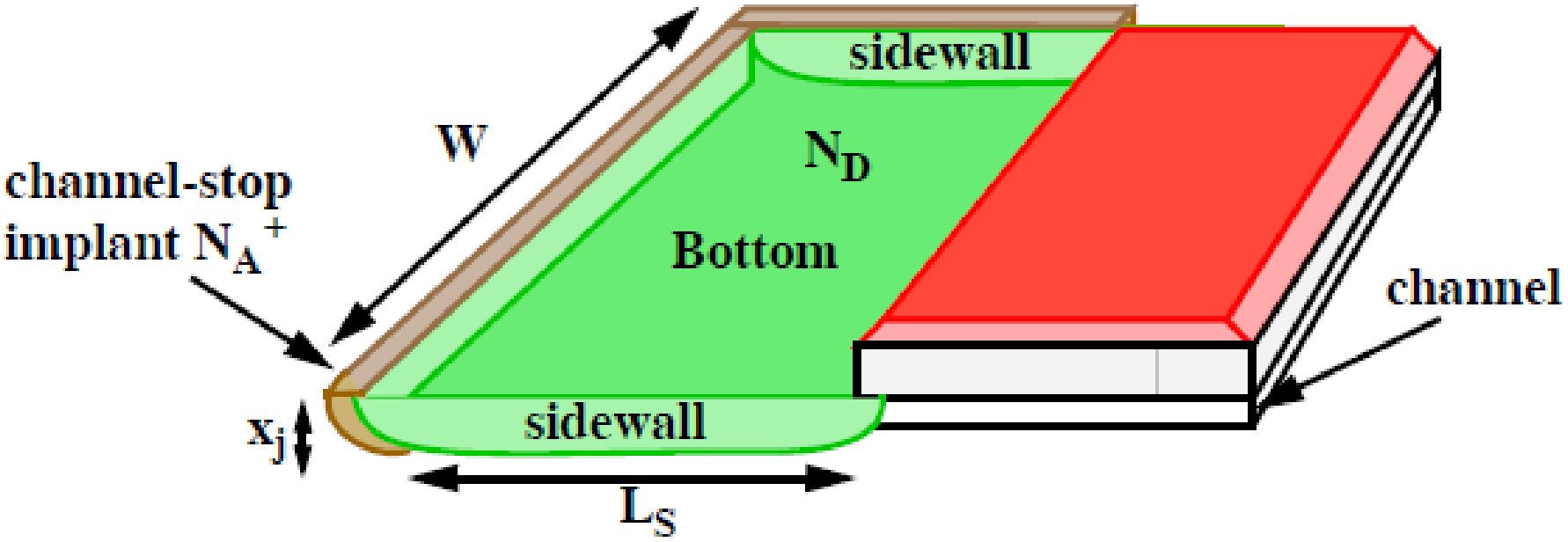
Operation	Cut-off	Saturation	Resistive
C_{gs}	0	$\frac{2}{3}C_{OX}WL_{eff}$	$\frac{1}{2}C_{OX}WL_{eff}$
C_{gd}	0	0	$\frac{1}{2}C_{OX}WL_{eff}$
C_{gb}	$C_{OX}WL_{eff}$	0	0
C_g	$C_{OX}WL_{eff}$	$\frac{2}{3}C_{OX}WL_{eff}$	$C_{OX}WL_{eff}$

- Resistive (Linear): $C_{gb} \simeq 0$ channel is shielded from the bulk by inversion
- Saturation (Active): $C_{gd} = 0$ and $C_{gb} = 0$ channel pinch-off

- Detailed gate capacitors

Operation	Cut-off	Saturation	Resistive
C_{gs}	$C_{OX}WL_D$	$\frac{2}{3}C_{OX}WL_{eff}+C_{OX}WL_D$	$\frac{1}{2}C_{OX}WL_{eff}+C_{OX}WL_D$
C_{gd}	$C_{OX}WL_D$	$C_{OX}WL_D$	$\frac{1}{2}C_{OX}WL_{eff}+C_{OX}WL_D$
C_{gb}	$C_{OX}WL_{eff}$	0	0

- Junction capacitance



$$C_{sb}\left(\text{Cut-off}\right) = C_j WL_S + C_{js}x_j\left(2W + 2L_S\right)$$

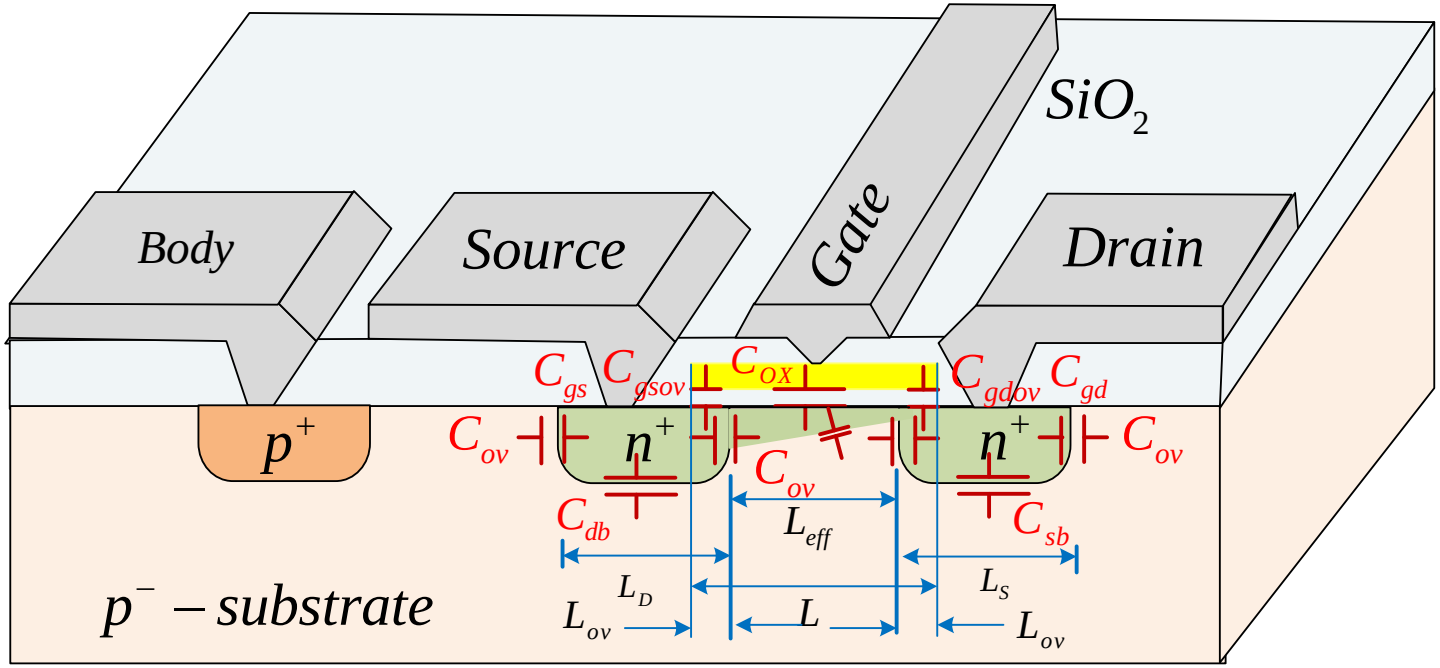
$$C_{sb}\left(\text{Saturation}\right) = C_j WL_S + C_{js}x_j\left(W + 2L_S\right)$$

$$C_{sb}\left(\text{Resistive}\right) = C_j WL_S + C_{js}x_j\left(W + 2L_S\right)$$

- Both $n^+$the drain and the source forms planar pn-junction
- ❶ Capacitance of $n^+ - p^-$ -junction between source and channel
- ❷ Capacitance of $n^+ - p^+$-junction between source and p^+ channel stop implant
- ❸ Capacitance of $n^+ - p^+$ -junction between source and p^+ channel stop implant
- ❹ Capacitance of $n^+ - p^+$ -junction between source and p^+ channel stop implant
- ❺ : Capacitance of $n^+ - p^-$ -junction between source and substrate

$$C_j = C_{j0}\left(1+\frac{V_{SB}}{V_0}\right)^n \quad C_{j0} = \sqrt{\frac{\varepsilon_{Si} q}{2}\left(\frac{N_A N_D}{N_A + N_D}\right)\left(\frac{1}{V_0 - V}\right)} \quad V_0 = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$$

- Parasitic capacitors



$$C_{sb}\left(\text{Cut-off}\right)=C_jWL_S+C_{js}x_j\left(2W+2L_S\right)$$

$$C_{sb}\left(\text{Saturation}\right)=C_jWL_S+C_{js}x_j\left(W+2L_S\right)$$

$$C_{sb}\left(\text{Resistive}\right)=C_jWL_S+C_{js}x_j\left(W+2L_S\right)$$

Operation	Cut-off	Saturation	Resistive
C_{gd}	0	0	$\frac{1}{2}C_{OX}WL_{eff}$
C_{gd}	$C_{OX}WL_{over}$	$C_{OX}WL_{over}$	$C_{OX}WL_{over}$
C_{db}	$C_jWL_S + C_{js}x_j\left(2W + 2L_D\right)$	$C_jWL_D + C_{js}x_j\left(W + 2L_D\right)$	$C_jWL_D + C_{js}x_j\left(W + 2L_D\right)$
C_{gb}	$C_{OX}WL_{eff}$	0	0
C_{gs}	0	$\frac{2}{3}C_{OX}WL_{eff}$	$\frac{1}{2}C_{OX}WL_{eff}$
C_{gs}	$C_{OX}WL_{over}$	$C_{OX}WL_{over}$	$C_{OX}WL_{eff}$
C_{sb}	0	$\frac{2}{3}C_jWL_{eff}$	$\frac{1}{2}C_jWL_{eff}$
C_{sb}	$C_jWL_S + C_{js}x_j\left(2W + 2L_S\right)$	$C_jWL_S + C_{js}x_j\left(W + 2L_S\right)$	$C_jWL_S + C_{js}x_j\left(W + 2L_S\right)$