San José State University
Department of Electrical Engineering
EE223-02, Analog Integrated Circuits, Fall 2018

Course and Contact Information

Instructor:	Sang-Soo Lee
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Office Hours:	MW 4:45 PM - 5:45 PM, Other time by appointment
Class Days/Time:	MW 6 PM - 7:15 PM
Classroom:	Dudley Moorhead Hall 149B
Prerequisites:	EE124 or equivalent

Course Description

This course studies nanoscale metal-oxide semiconductor field effect transistor (MOSFET) modeling and circuit design techniques for analog integrated circuit applications. Course topics include short channel issues, layout techniques to improve design performance, noise modeling and transformation, wide-swing current mirrors, bandgap and reference circuits, gain and bandwidth characteristics of single-stage and two-stage amplifiers. A variety of operational amplifier architectures including fully-differential structures with their slew rate, settling time, phase margin, stability will be discussed in detail. Finally, the application of the fully-differential operational amplifiers in switched-capacitor circuits is discussed for a class project.

Course Learning Outcomes (CLO)

Students will acquire the ability to: characterize and model MOS transistors, bias and operate transistors in amplifiers with different characteristics, understand high performance layout with minimum parasitic, utilize simulation tools to characterize complex analog integrated circuits, determine the trade-off among linearity, bandwidth, gain and power dissipation of amplifiers, design stable multi-stage amplifiers, apply frequency compensation techniques for amplifiers, design temperature and supply independent bandgap reference circuits, design 2-phase non-overlapping clock and clocked comparator for switched-capacitor circuits.

Upon successful completion of this course, students will be able to:

1. *Design advanced biasing circuits, operational amplifiers, comparators and switched-capacitor circuits.*
2. *Understand the concept of noise, distortion, stability, phase margin, voltage swing, slew-rate and gain-bandwidth product of amplifiers.*
3. *Use modern engineering CAD tools for computations, simulations, analysis, and design of analog and mixed-signal circuits.*
4. *Verify the theory with hands-on lab simulations.*

Required Texts/Readings

Textbook

Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill, 2001

Other Readings

- Lecture notes
- Analog *Integrated Circuit Design, 2nd Edition, by Tony Chan Carusone, David A. Johns and Ken Martin, Wiley, 2011*
- CMOS *Circuit Design, Layout, and Simulation, 3rd Edition, by R. Jacob Baker, IEEE Press, Wiley, 2010*
- Analysis *and Design of Analog Integrated Circuits, 5th Edition, by Gray, Hurst, Lewis and Meyer, Wiley, 2009*

Course Requirements and Assignments

Assignments and projects are mainly based on Cadence Spectre simulations and are closely related to topics discussed in this course. Cadence simulation tools will not be taught in this course and students are required to master this CAD tool by themselves. Each group (maximum 2 students) must write a formal project report using a word processor (i.e. Microsoft Office) and submit the original write-up including all data, images and graphs by email before deadline to be eligible to receive a credit. Students may be required to present their works like standard design reviews as conducted in industry. Non-restricted MOSFET transistor models will be provided for assignments and projects. More details on design projects will be provided as the lectures progress.

"Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practica. Other course structures will have equivalent workload expectations as described in the syllabus."

Final Examination or Evaluation

The date of the exams is shown on the course syllabus. Exams will be closed book. However, students can bring 1 page of aid sheet. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams.

Grading Information

homework	25%
midterm exam	25%
design project	25%
final exam	25%

Determination of Grades

90% and above	A
89% - 85%	A-
84% - 82%	B+
81% - 79%	B
78% - 75%	B-
74% - 72%	C+
71% - 69%	C

68% - 65%	C-
64% - 62%	D+
61% - 59%	D
58% - 55%	D-
below 55%	F

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the class and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/ Make sure to review these policies and resources.

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student's second offense in any course will result in a Department recommendation of suspension from the University.*

EE223 / Analog Integrated Circuits, Fall 2018 Course Schedule

Lecture #	Date	Topics	Book reading
1	22-Aug	Introduction to Analog IC design	Chapter 1
2	27-Aug	MOS Operation	Chapter 2
3	29-Aug	MOS IV and 2nd order Effects (**HW#1 handout, 5% grade**)	Chapter 2
4	5-Sep	MOS small-signal model	Chapter 3
5	10-Sep	MOS capacitances and layout	Chapter 3
6	12-Sep	Common-source amplifiers and Source Follower	Chapter 4
7	17-Sep	Common-Gate and Folded-Cascode (**HW#2 handout, 5% grade**)	Chapter 5
8	19-Sep	Differential Pairs and Current Mirrors	Chapter 6
9	24-Sep	Frequency Response	Chapter 6
10	26-Sep	Noise – Flicker and Thermal	Chapter 7
11	1-Oct	Noise in Amplifiers (**HW#3 handout, 5% grade**)	Chapter 7
12	3-Oct	Feedback	Chapter 8
13	8-Oct	OPAMP - Single Stage	Chapter 8
14	10-Oct	OPAMP - Two Stage, Gain Boosting	Chapter 9
15	15-Oct	Stability and Frequency Compensation **(HW#4 handout, 5% grade)**	Chapter 9
16	17-Oct	***Midterm Exam, 75 minutes, 25% grade***	Chapter 10
17	22-Oct	Fully differential OPAMP	
18	24-Oct	Common-Mode Feed-Back (CMFB)	Lecture note
19	29-Oct	Bandgap reference & Project Description	Lecture note
20	31-Oct	Switched-Capacitor Circuits (**HW#5 handout, 5% grade**)	Chapter 11
21	5-Nov	Sample & Hold and MDAC	Chapter 12
22	7-Nov	Comparators and Clock Circuits	Lecture note
23	14-Nov	Offset Cancellation	Lecture note
24	19-Nov	Mismatches and Nonlinearity	Lecture note
25	26-Nov	Analog Layout Techniques	Chapter 13
26	28-Nov	Project Presentation - Group 1-5	Chapter 18
27	3-Dec	Project Presentation - Group 6-10	
28	5-Dec	Project Presentation - Group 11-15	
29	10-Dec	Review for Final Exam	
Final	12-Dec	***Dec. 12, Wednesday, from 5:15PM — 7:00PM, 25% grade***	

- *No class on Labor Day 9/3 Mon, Veteran's Day 11/12 Mon, Thanksgiving Holiday: 11/21 Wed.*
- *Midterm Exam date is subject to change with advanced notice. Exact date will be announced in the class.*