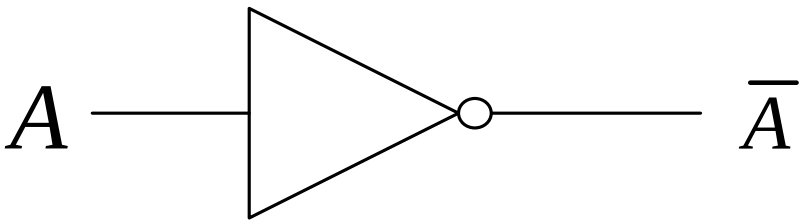
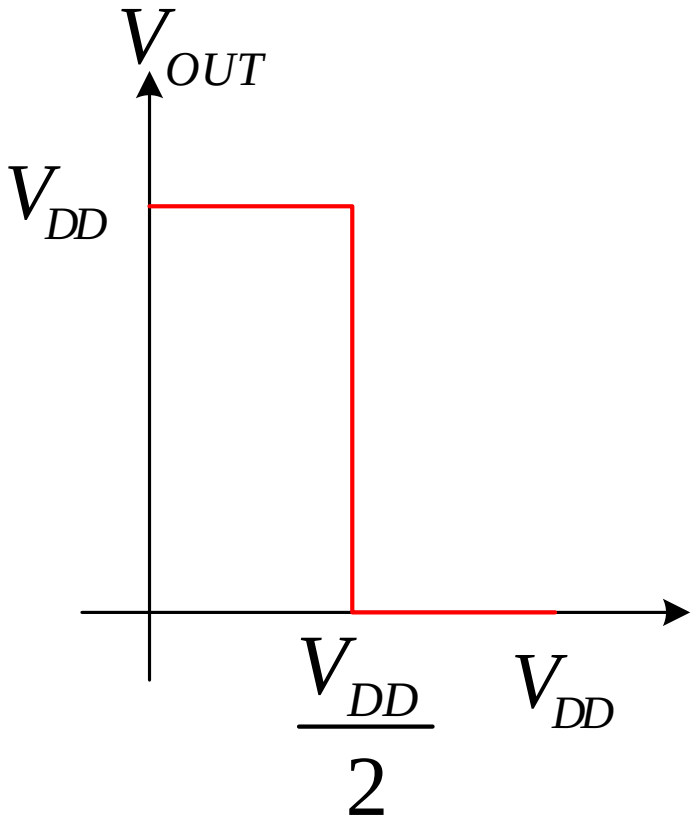
Inverter Chain

Lecture 10

- Ideal Inverter





- Switching Threshold

- The switching threshold defined as a voltage
- Where

$$V_M = V_{OUT} = V_{IN}$$

- Since

$$V_{GS} = V_{DS}$$

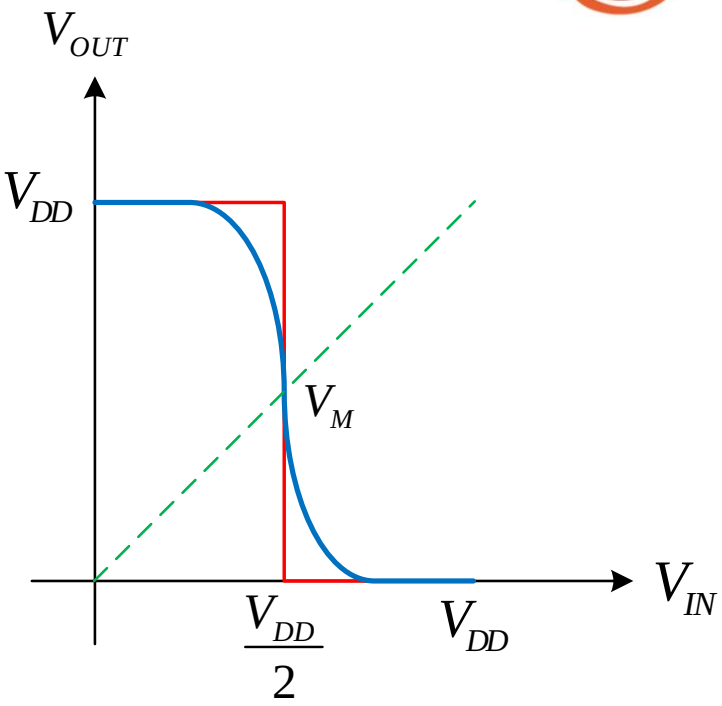
- Both pMOS and nMOS are in saturation.
- For velocity saturation

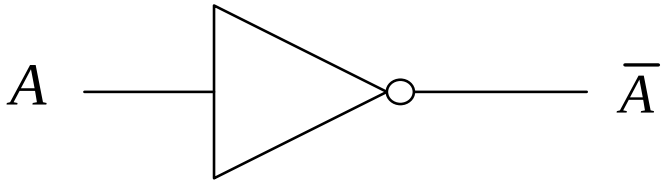
$$V_{DS}(sat) < V_M - V_T$$

- Ignoring the channel modulation $\lambda = 0$

$$k_n V_{DSn}(sat)\left(V_M - V_{Tn} - \frac{V_{DSn}(sat)}{2}\right)$$

$$+ k_p V_{DSp}(sat)\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSp}(sat)}{2}\right) = 0$$





- Switching Threshold

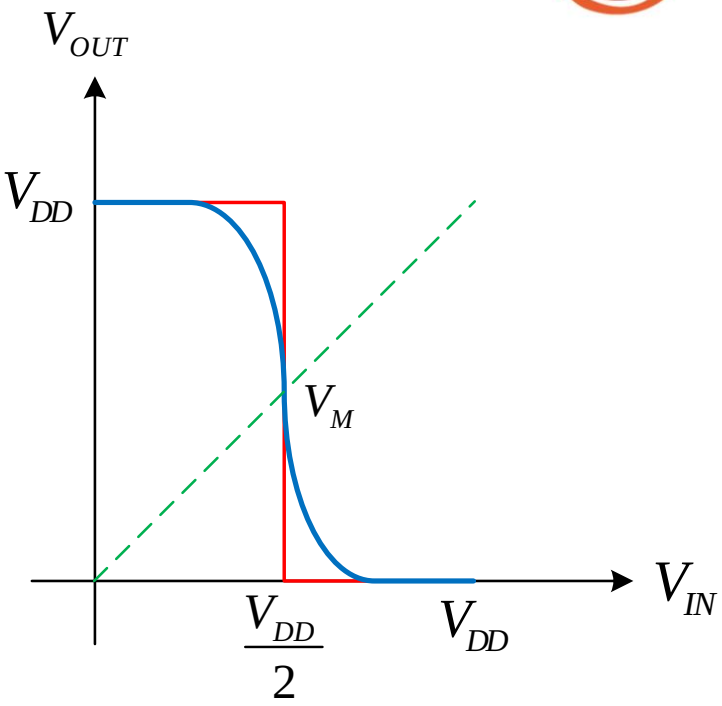
$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}$$

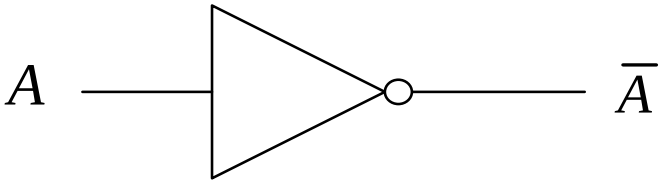
- Where r compares the relative strength of pMOS and nMOS

$$r = \frac{k_p V_{DSp}(sat)}{k_n V_{DSn}(sat)} = \frac{\upsilon_p(sat) W_p}{\upsilon_n(sat) W_n}$$

- For the $t_{ox}(pMOS) = t_{ox}(nMOS)$

$$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1+r}$$





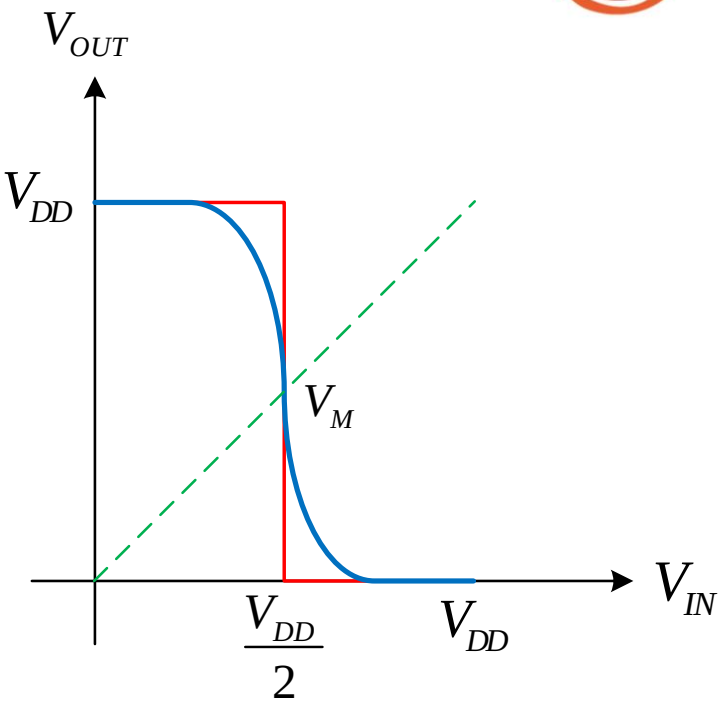
- Switching Threshold
- For comparable high and low noise margin

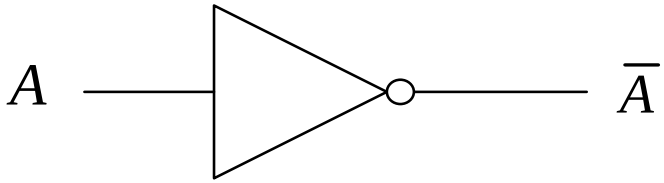
$$V_M \approx \frac{rV_{DD}}{1+r} = \frac{V_{DD}}{2}$$

- Which requires $r = 1$
- Then the pMOS device should be seized to

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSn}(sat)}{k'_p V_{DSp}(sat)}$$

- Making W_p wider results in $r > 1$ and move V_M upper than the middle closer to V_{DD} and increasing the strength of nMOS move the switching voltage V_M closer to GND.





- Switching Threshold

- For desired value of the threshold voltage V_M , the pMOS to nMOS transistor sizes to set

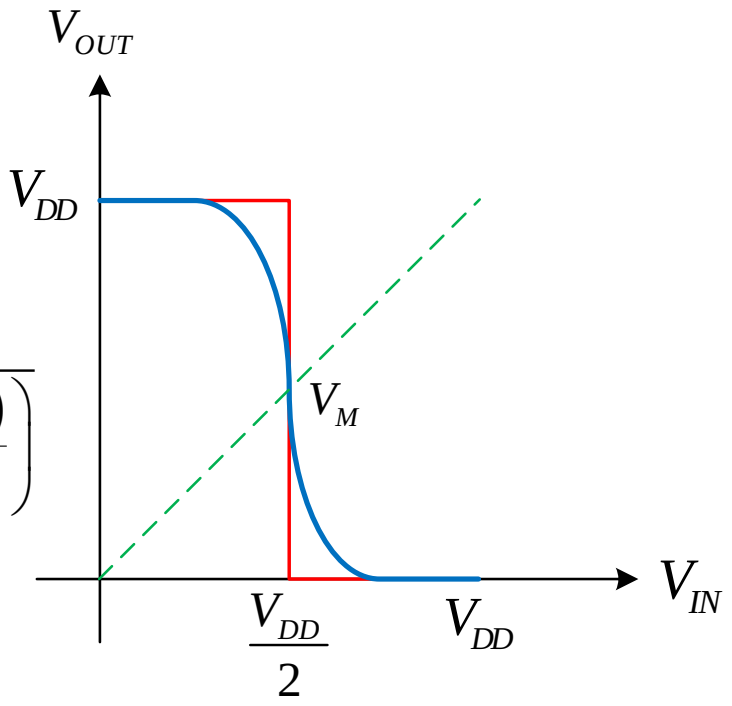
$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSn}(sat)\left(V_M - V_{Tn} - \frac{V_{DSn}(sat)}{2}\right)}{k'_p V_{DSp}(sat)\left(V_{DD} - V_M + V_{Tp} + \frac{V_{DSp}(sat)}{2}\right)}$$

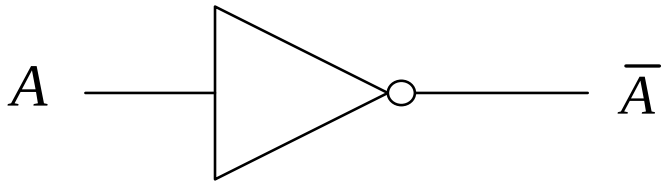
- For $V_{DS}(sat) > V_M - V_T$ where the saturation velocity is not occur, then

$$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1 + r}$$

- Where

$$r = \sqrt{\frac{-k_p}{k_n}}$$





V_{DD}

- Length Modulation
- Ignoring length modulation results in infinite gain
- Considering length modulation results in infinite gain

$$k_n V_{DSn}(sat)\left(V_{IN}-V_{Tn}-\frac{V_{DSn}(sat)}{2}\right)(1+\lambda V_{OUT})$$

$$+k_p V_{DSp}(sat)\left(V_{IN}-V_{DD}-V_{Tp}-\frac{V_{DSp}(sat)}{2}\right)(1+\lambda_p V_{OUT}-\lambda_p V_{DD})=0$$

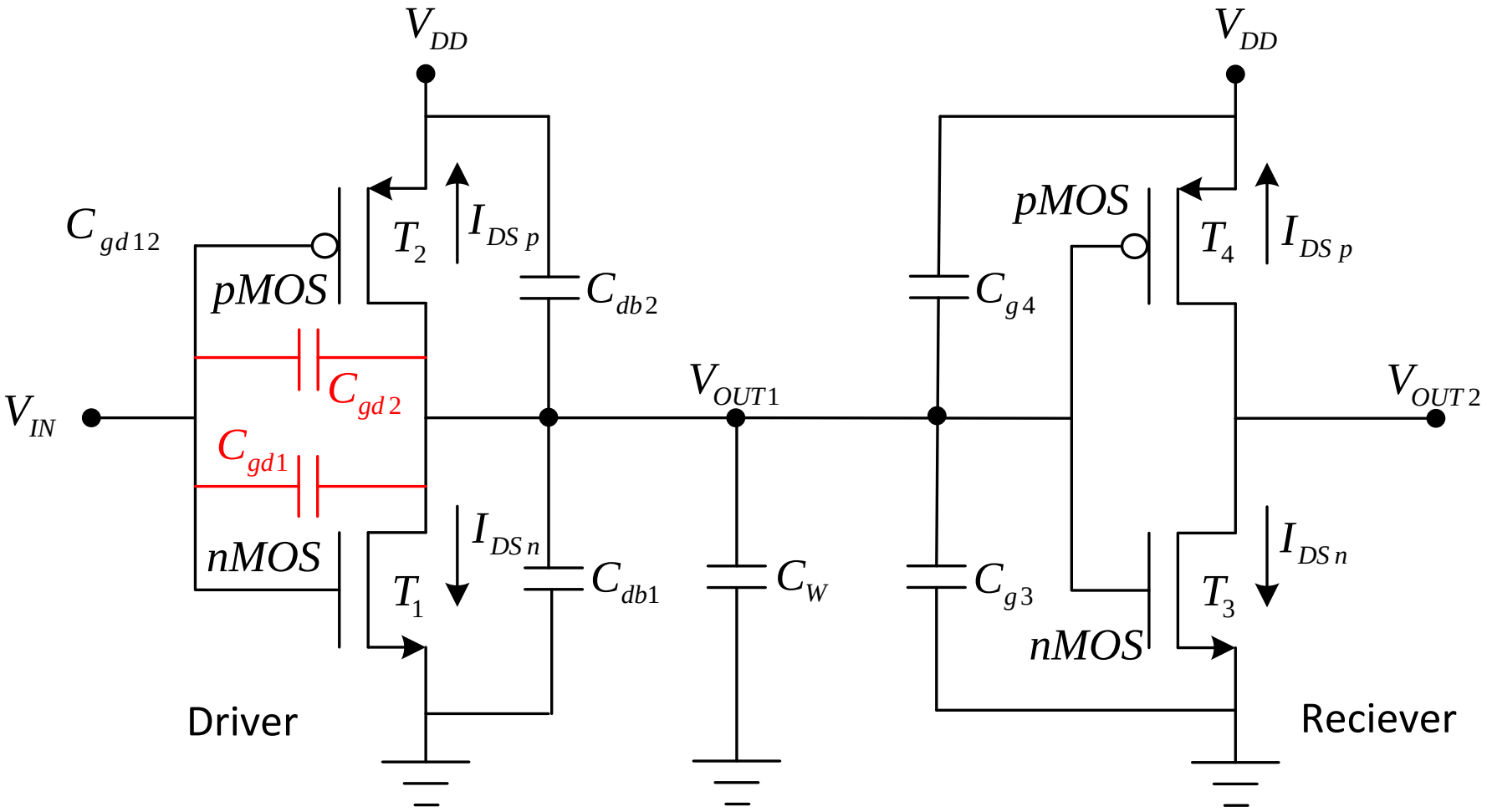
- Differentiating the output with respect to the input

$$\frac{dV_{out}}{dV_{in}}=\frac{k_n V_{DSn}(sat)(1+\lambda_n V_{OUT})+k_p V_{DSp}(sat)(1+\lambda_p V_{OUT}-\lambda_p V_{DD})}{\lambda_n k_n V_{DSn}(sat)\left(V_{IN}-V_{Tn}-\frac{V_{DSn}(sat)}{2}\right)+\lambda_p k_p V_{DSp}(sat)\left(V_{IN}-V_{DD}-V_{Tp}-\frac{V_{DSp}(sat)}{2}\right)}$$

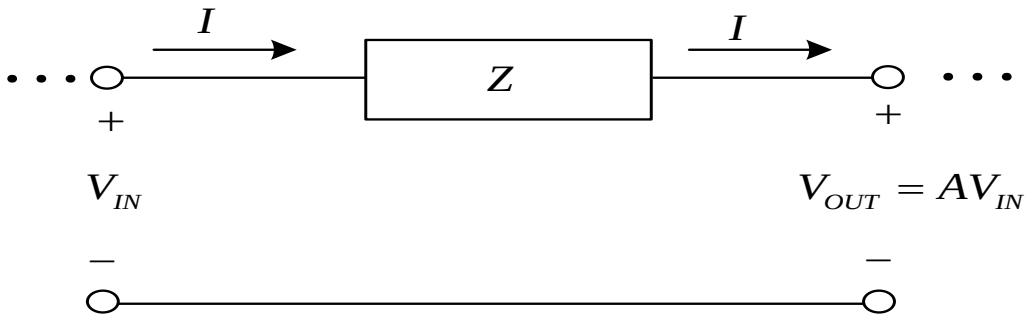
- Ignoring some second-order terms and setting $V_{IN}=V_M$ results in gain
- .

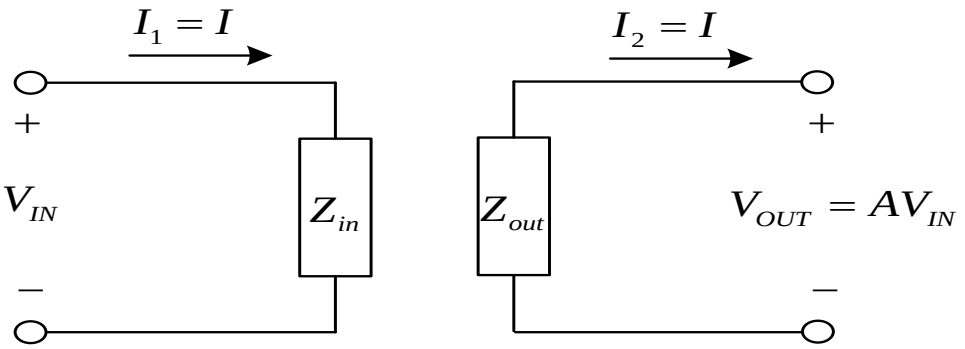
$$g=\frac{1}{I_{DS}(V_M)}\frac{k_n V_{DSn}(sat)+k_p V_{DSp}(sat)}{\lambda_n-\lambda_p}=\frac{1+r}{\left(V_M-V_{Tn}-\frac{V_{DSn}(sat)}{2}\right)(\lambda_n-\lambda_p)}$$

- Effect of Capacitance (lumped capacitor model)



- Miller effect:



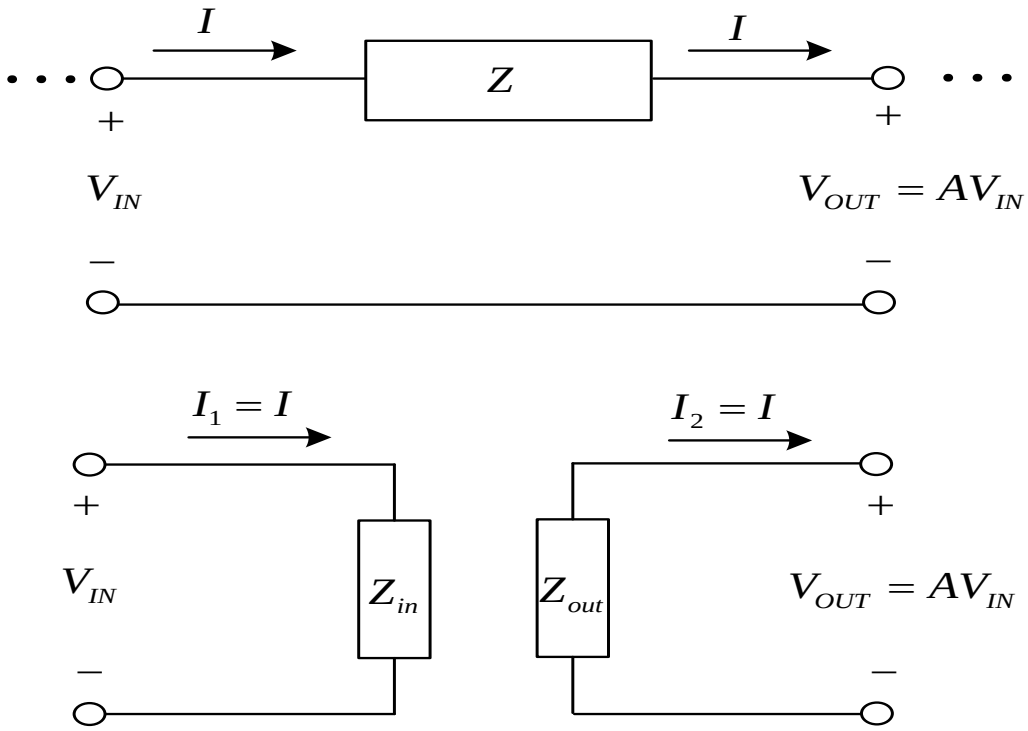


$$Z_{in} = \frac{Z}{1-A}$$

$$Z_{out} = \frac{Z}{1-\frac{1}{A}}$$

- The impedance Z can be replaced by two impedance Z_{in} connected between input node and ground and Z_{out} between the output node and ground

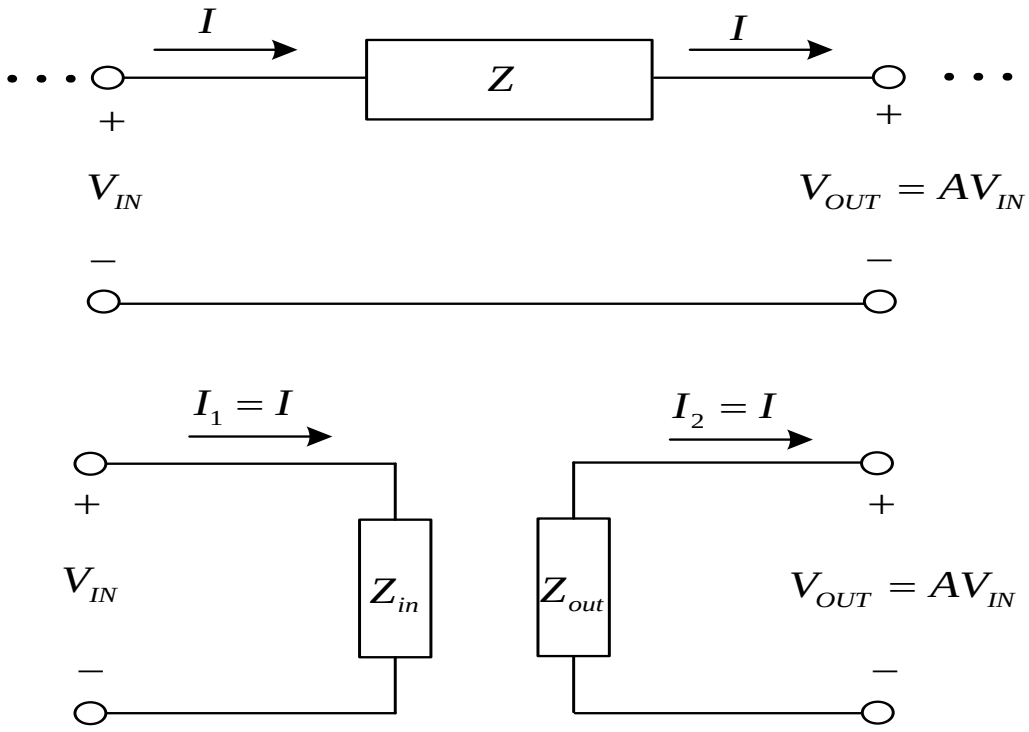
- Miller effect:



$$I_1 = \frac{V_{IN}}{Z_{in}} = I = \frac{V_{IN} - AV_{IN}}{Z} = \frac{V_{IN} - V_{OUT}}{Z}$$

$$Z_{in} = \frac{Z}{1 - A}$$

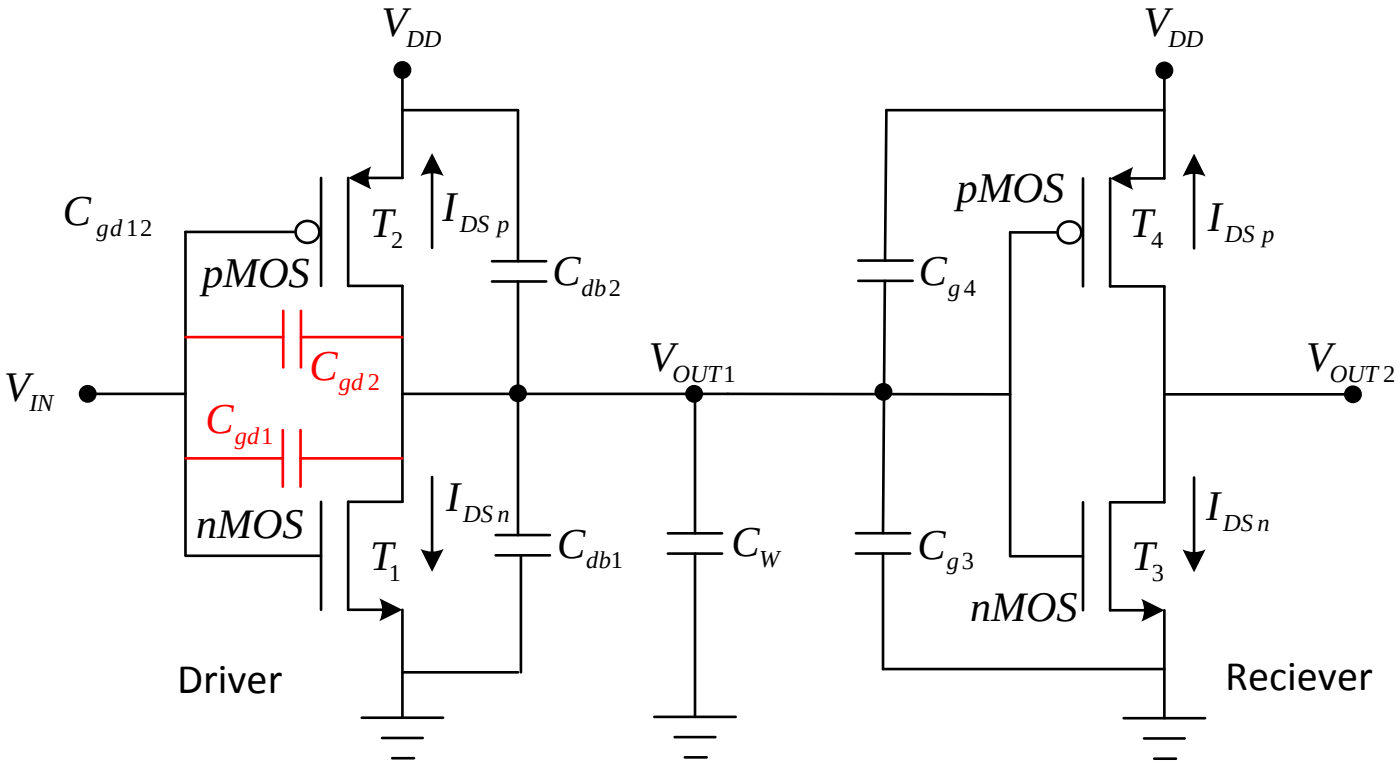
- Miller effect:



$$I_2 = \frac{0 - V_{OUT}}{Z_{OUT}} = \frac{0 - AV_{IN}}{Z_{OUT}} = I = \frac{V_{IN} - V_{OUT}}{Z} = \frac{V_{IN} - AV_{IN}}{Z}$$

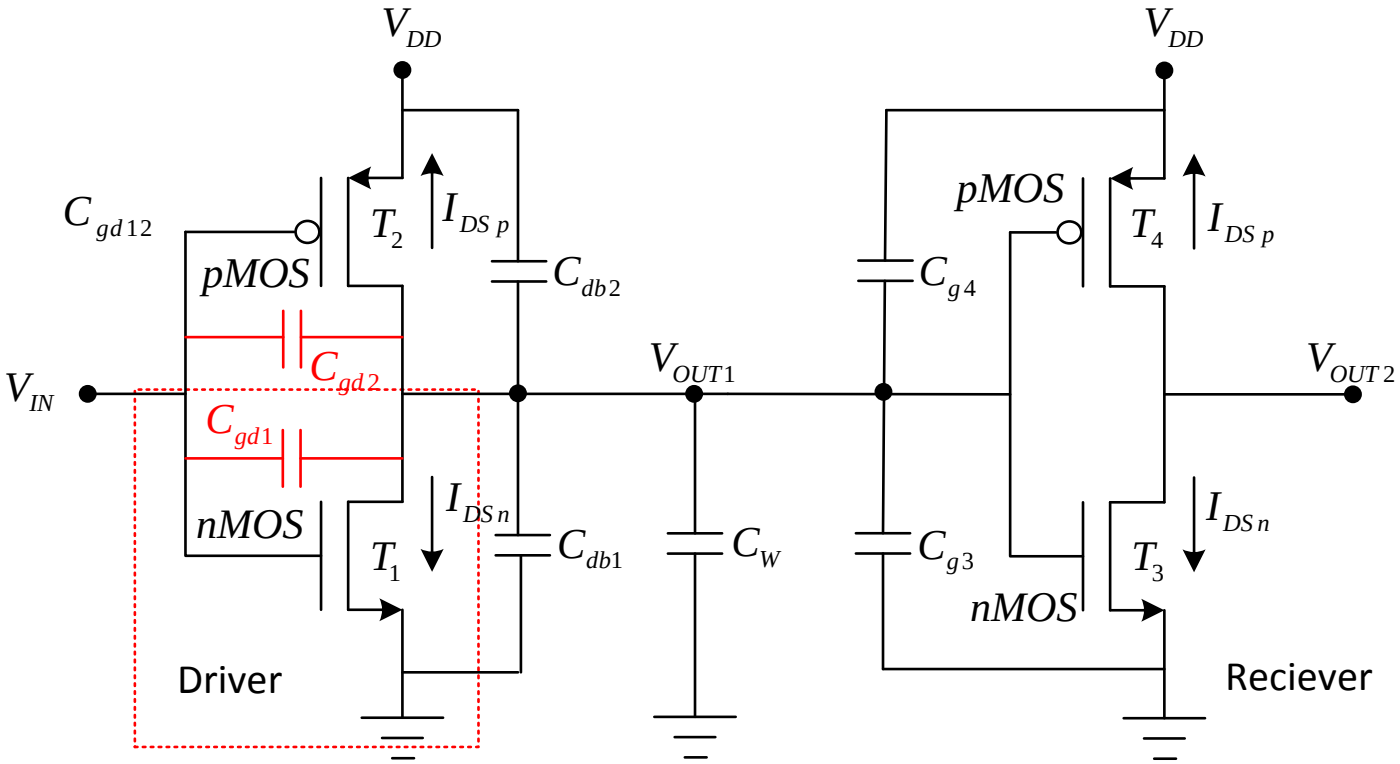
$$Z_{out} = \frac{Z}{1 - \frac{1}{A}}$$

- Modeling floating gate-drain capacitor by a capacitor from output to ground



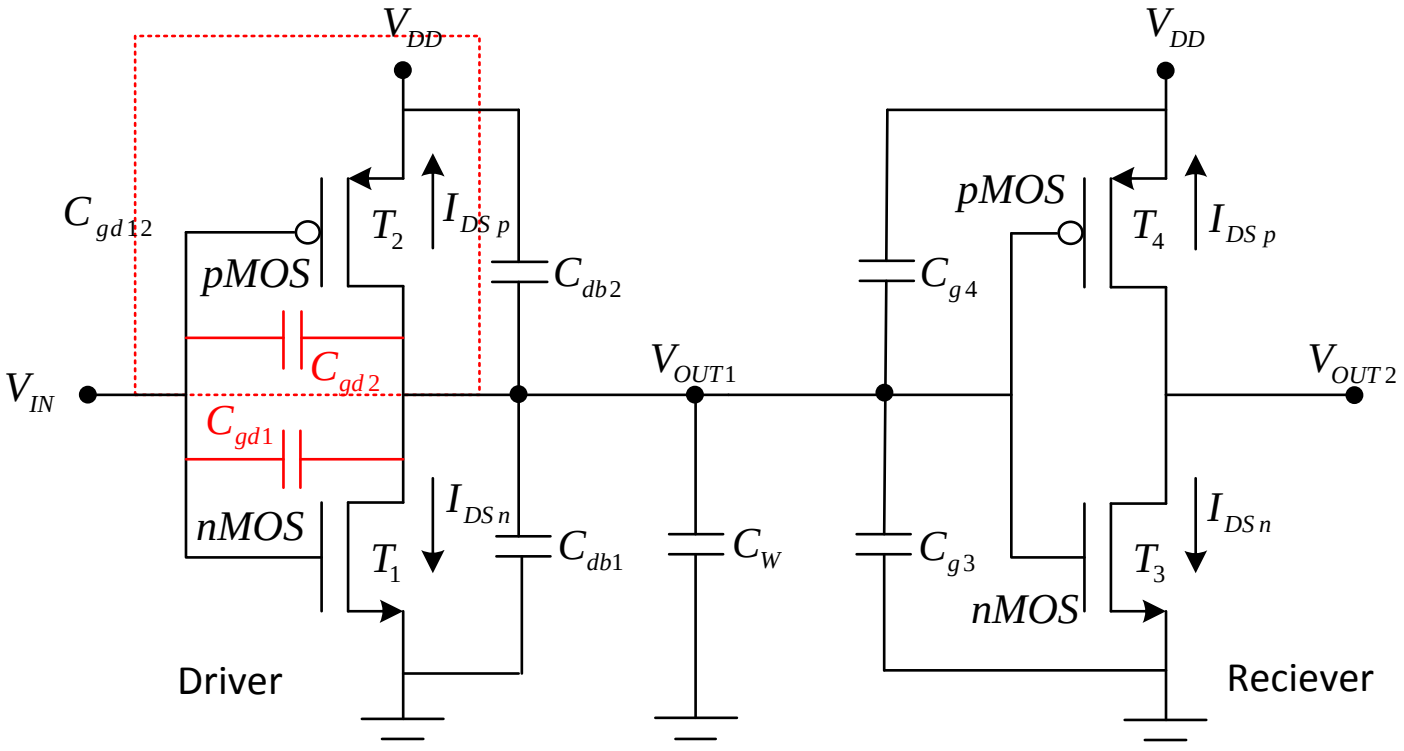
- The capacitor C_{gd1} can be replaced by an equivalent capacitor $2C_{gd1}$ between output node and ground. V_{IN} goes high and V_{OUT} goes low by the same amount. The voltage change across the capacitor C_{gd1} is twice the amount (A=2)

- Modeling floating gate-drain capacitor by a capacitor from output to ground



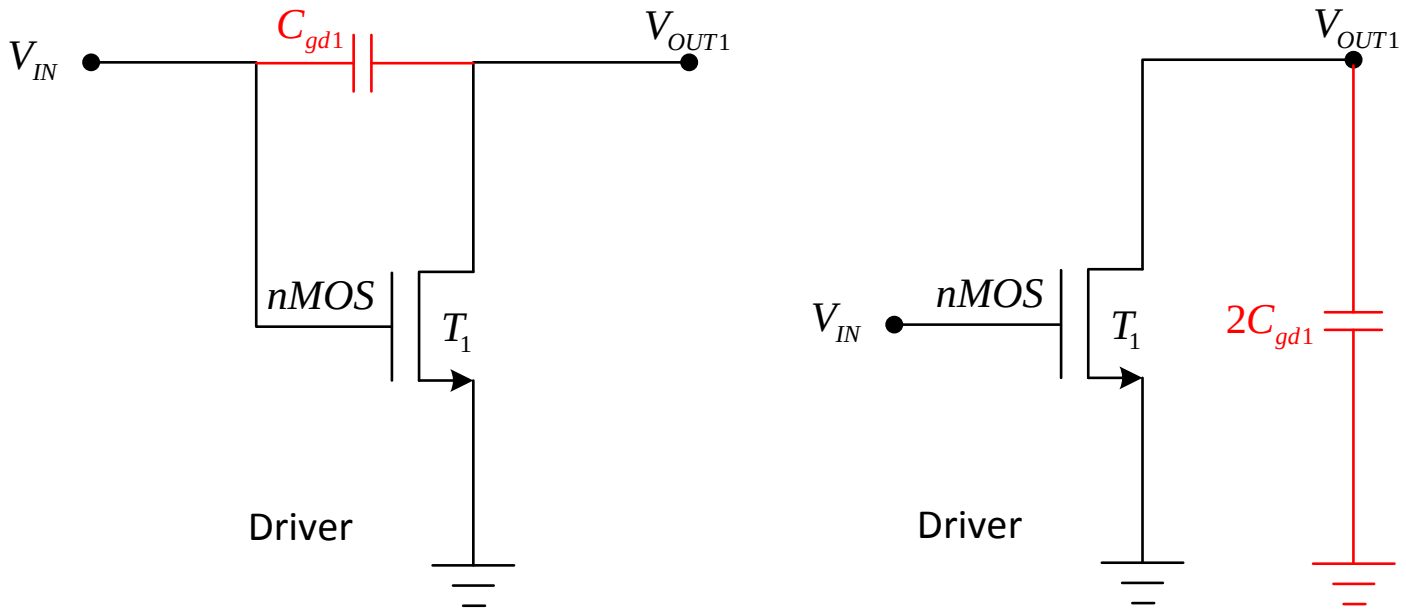
- The capacitor C_{gd1} can be replaced by an equivalent capacitor $2C_{gd1}$ between output node and ground. V_{IN} goes high and V_{OUT} goes low by the same amount. The voltage change across the capacitor C_{gd1} is twice the amount (A=2)

- Modeling floating gate-drain capacitor by a capacitor from output to ground



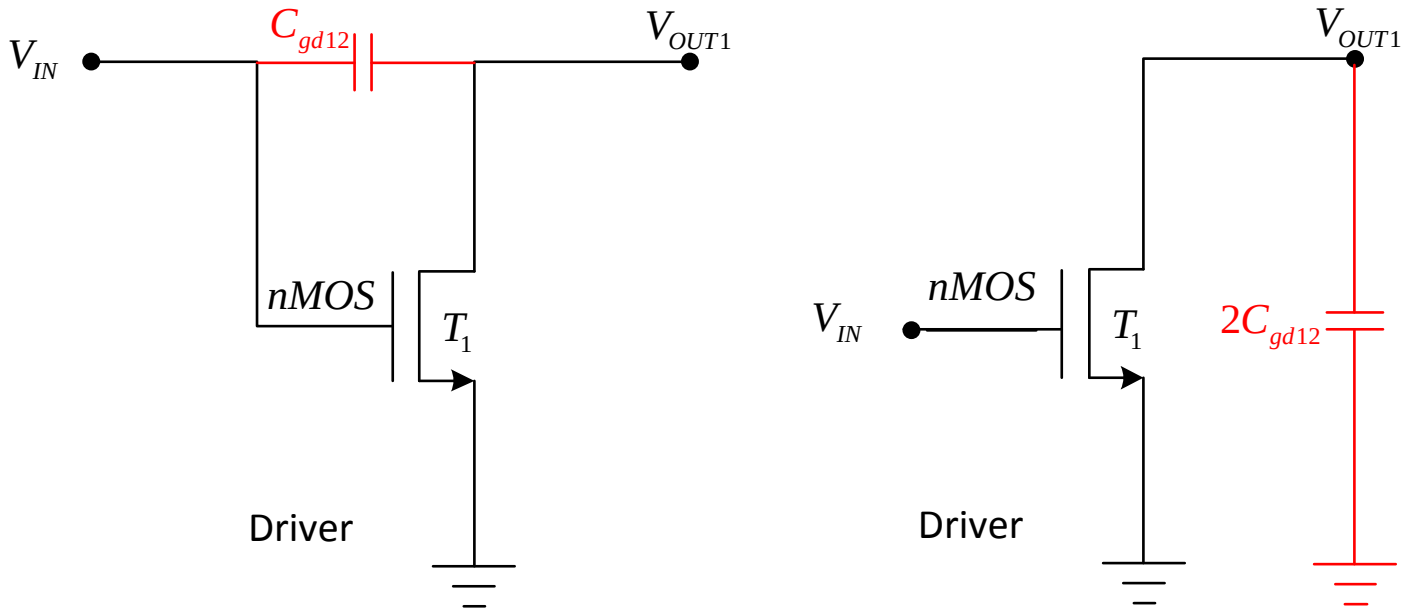
- The capacitor C_{gd2} can be replaced by an equivalent capacitor $2C_{gd2}$ between output node and ground. V_{IN} goes high and V_{OUT} goes low by the same amount. The voltage change across the capacitor C_{gd2} is twice the amount (A=2)

- Modeling floating gate-drain capacitor by a capacitor from output to ground



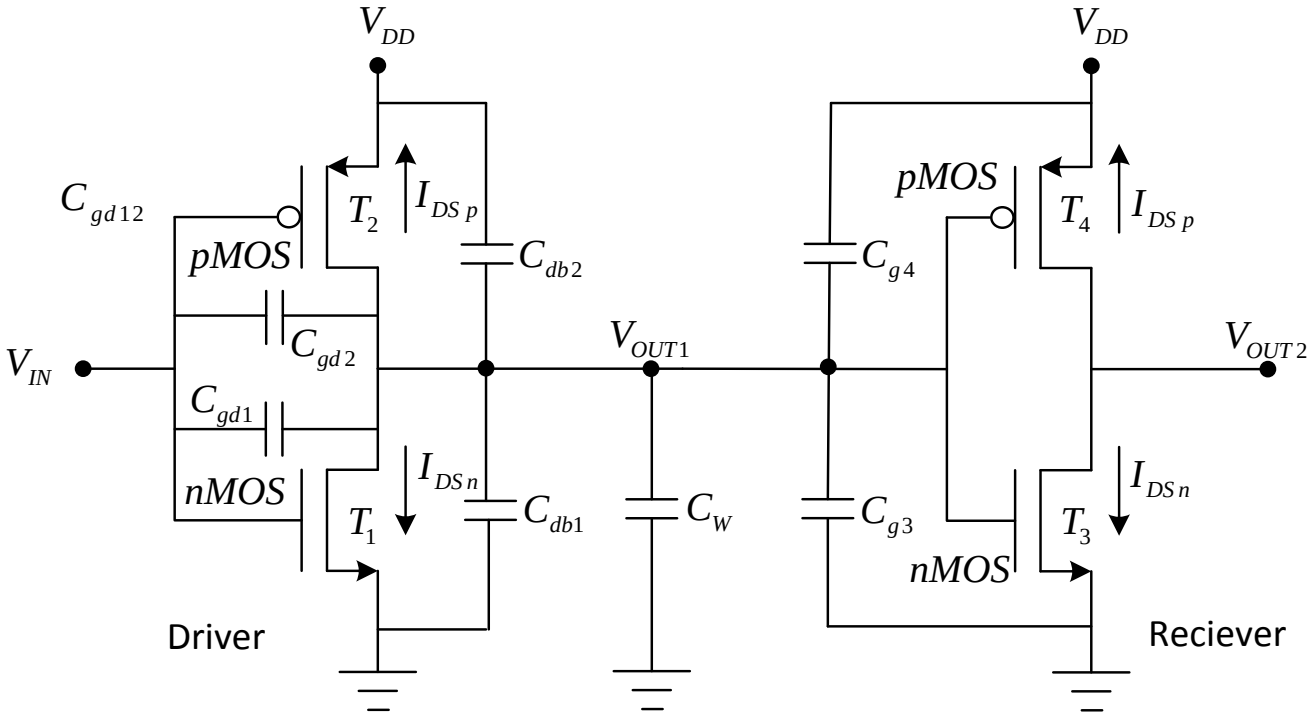
- Transistor T_1 and T_2 are either in cut-off or in saturation mode during the first half of the output transient up to 50%.
- The capacitor C_{gd1} can be replaced by an equivalent capacitor $2C_{gd1}$ between output node and ground. V_{IN} goes high and V_{OUT} goes low by the same amount. The voltage change across the capacitor C_{gd1} is twice the amount (A=2)

- Modeling floating gate-drain capacitor by a capacitor from output to ground



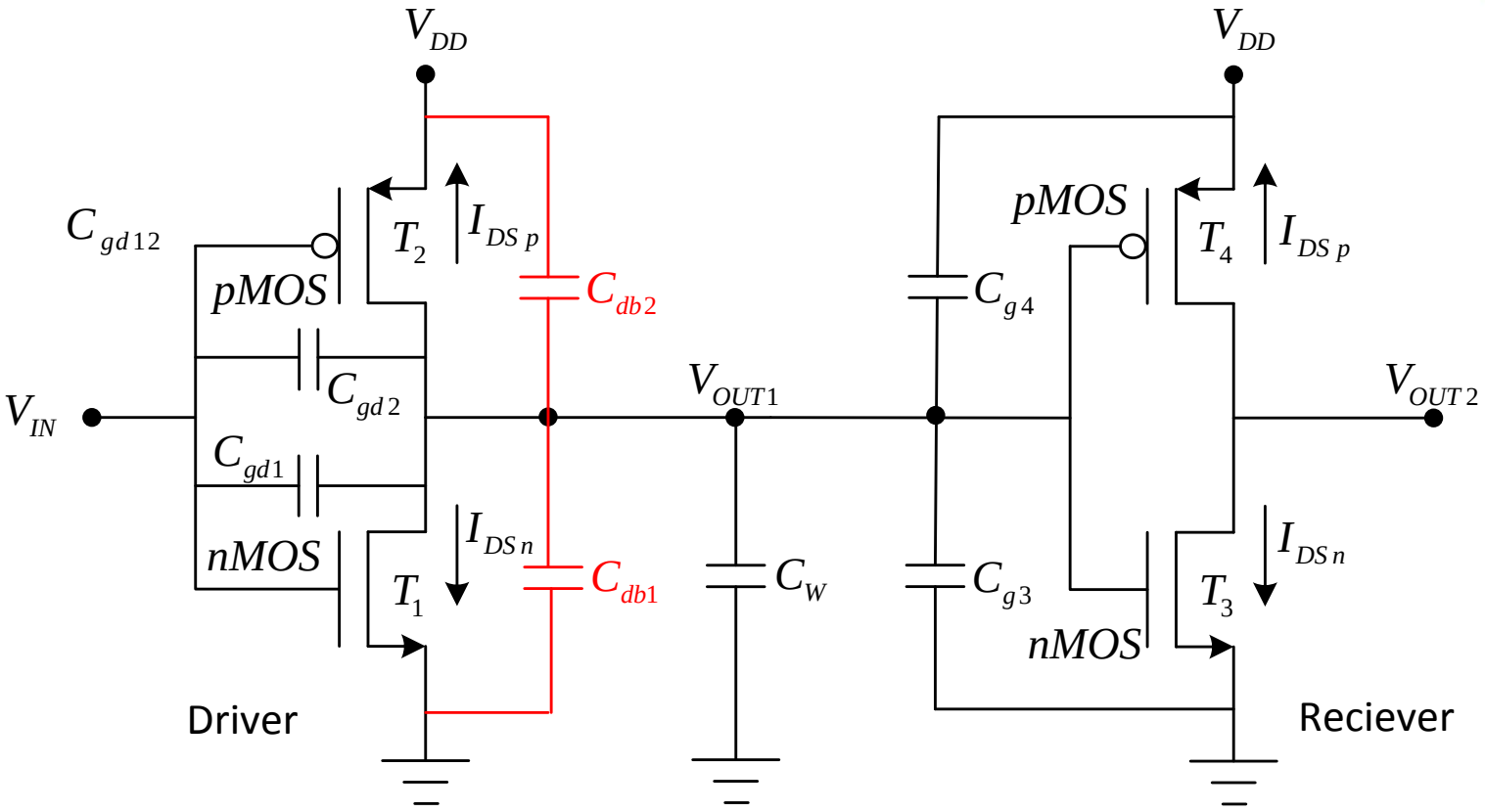
- Transistor and are either in cut-off or in saturation mode during the first half of the output transient up to 50%.
- The capacitor C_{gd12} can be replaced by an equivalent capacitor $2C_{gd12}$ between output node and ground. V_{IN} goes high and V_{OUT} goes low by the same amount. The voltage change across the capacitor C_{gd12} is twice the amount (A=2)

- Effect of Capacitance (lumped capacitor model)



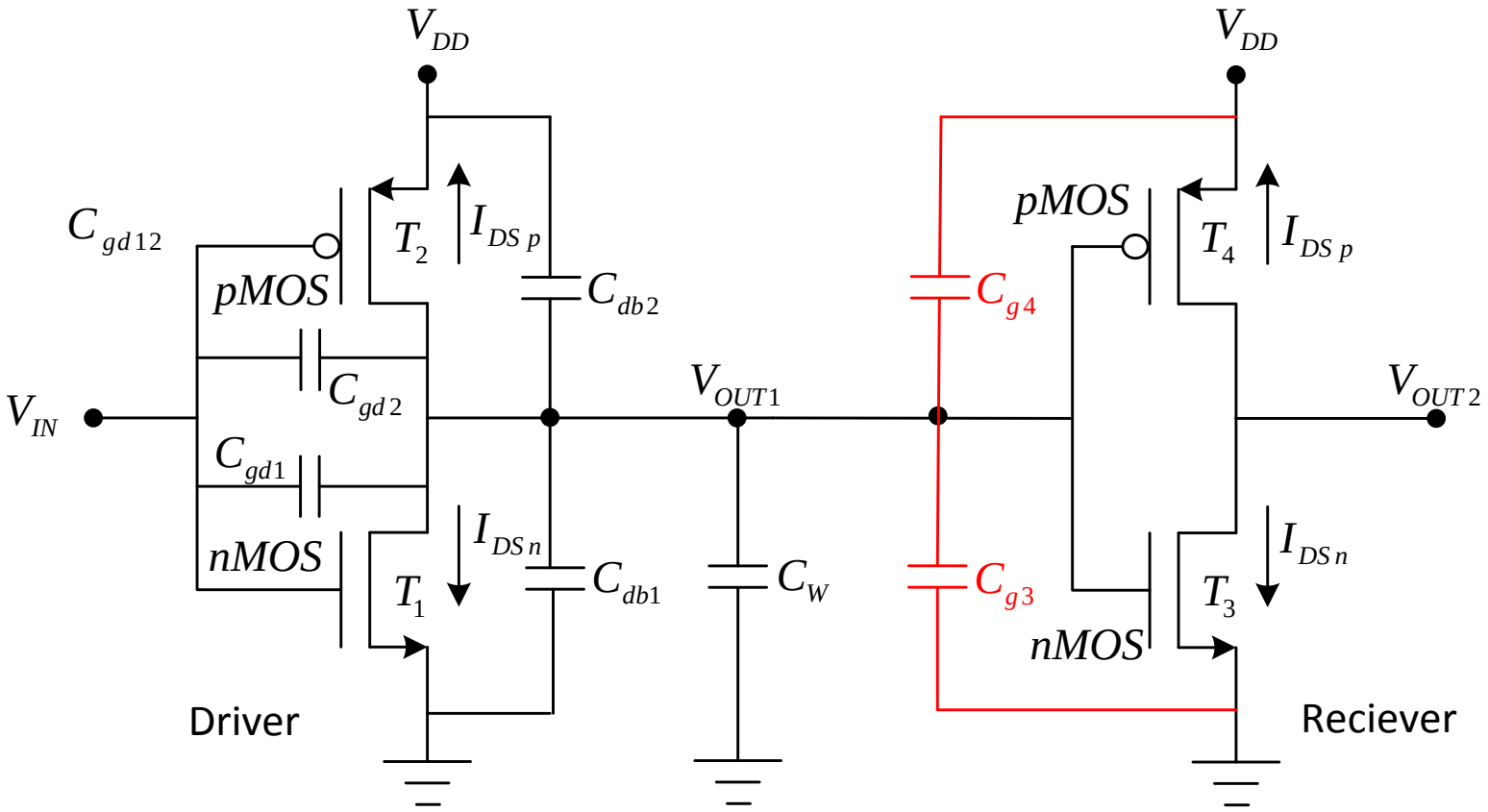
- The capacitor C_{gd12} can be replaced by an equivalent capacitor $2C_{gd12}$ between output node and ground. V_{IN} goes high and V_{OUT} goes low by the same amount. The voltage change across the capacitor C_{gd12} is twice the amount (A=2)

- Effect of Capacitance (lumped capacitor model)



- Capacitor $C_{db1}$and C_{db2} has a terminal capacitor at a constant voltage.
- $C_{db1}$and C_{db2}can be replaced with equal capacitance from output node to ground.

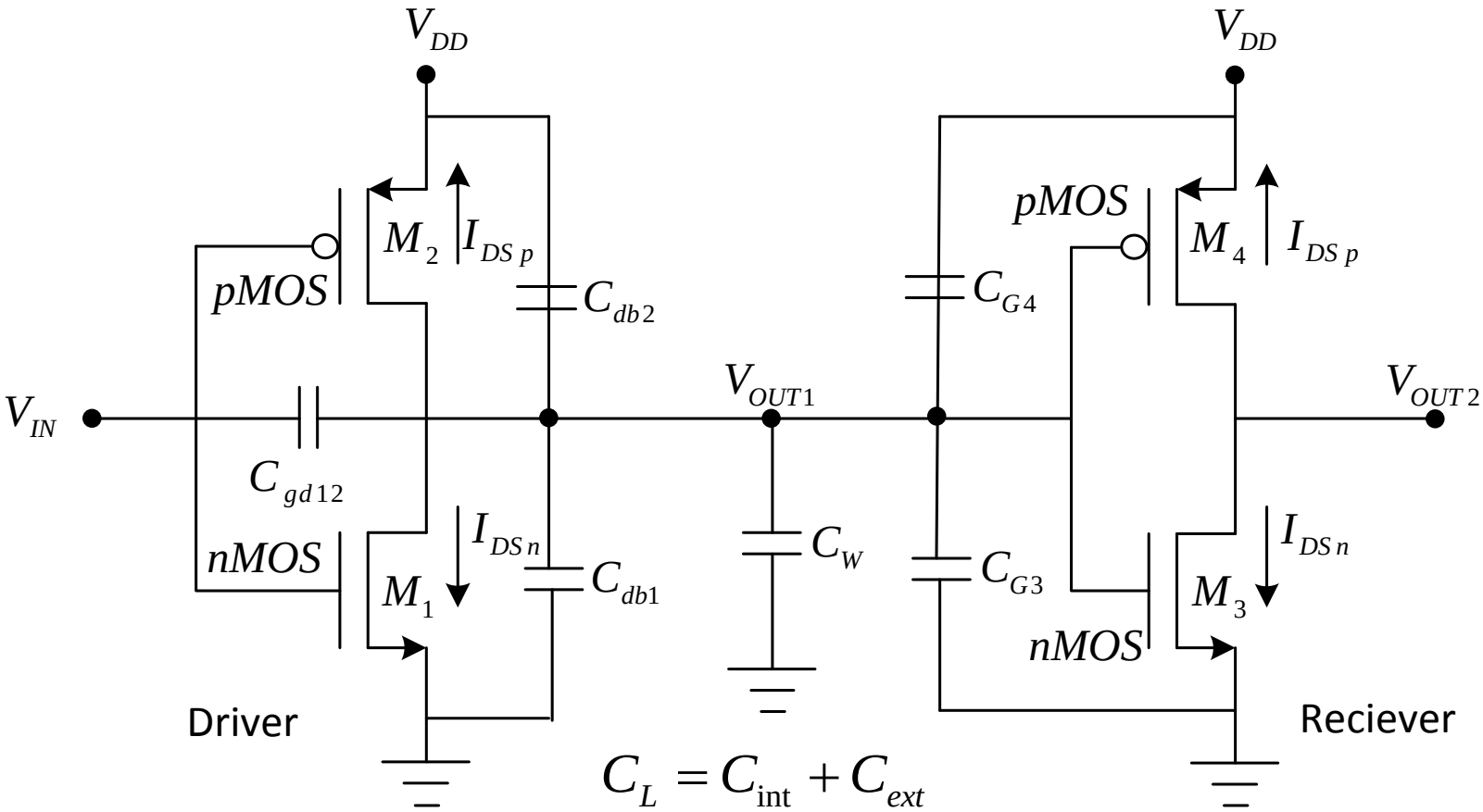
- Effect of Capacitance (lumped capacitor model)



- The second inverter does not switch state. Input capacitors remain constant.

$$C_{g3} + C_{g4} = (WL)_3 C_{OX} + (WL)_4 C_{OX} + C_{gsov3} + C_{gdov3} + C_{gsov4} + C_{gdov4}$$

- Effect of Capacitance (lumped capacitor model)

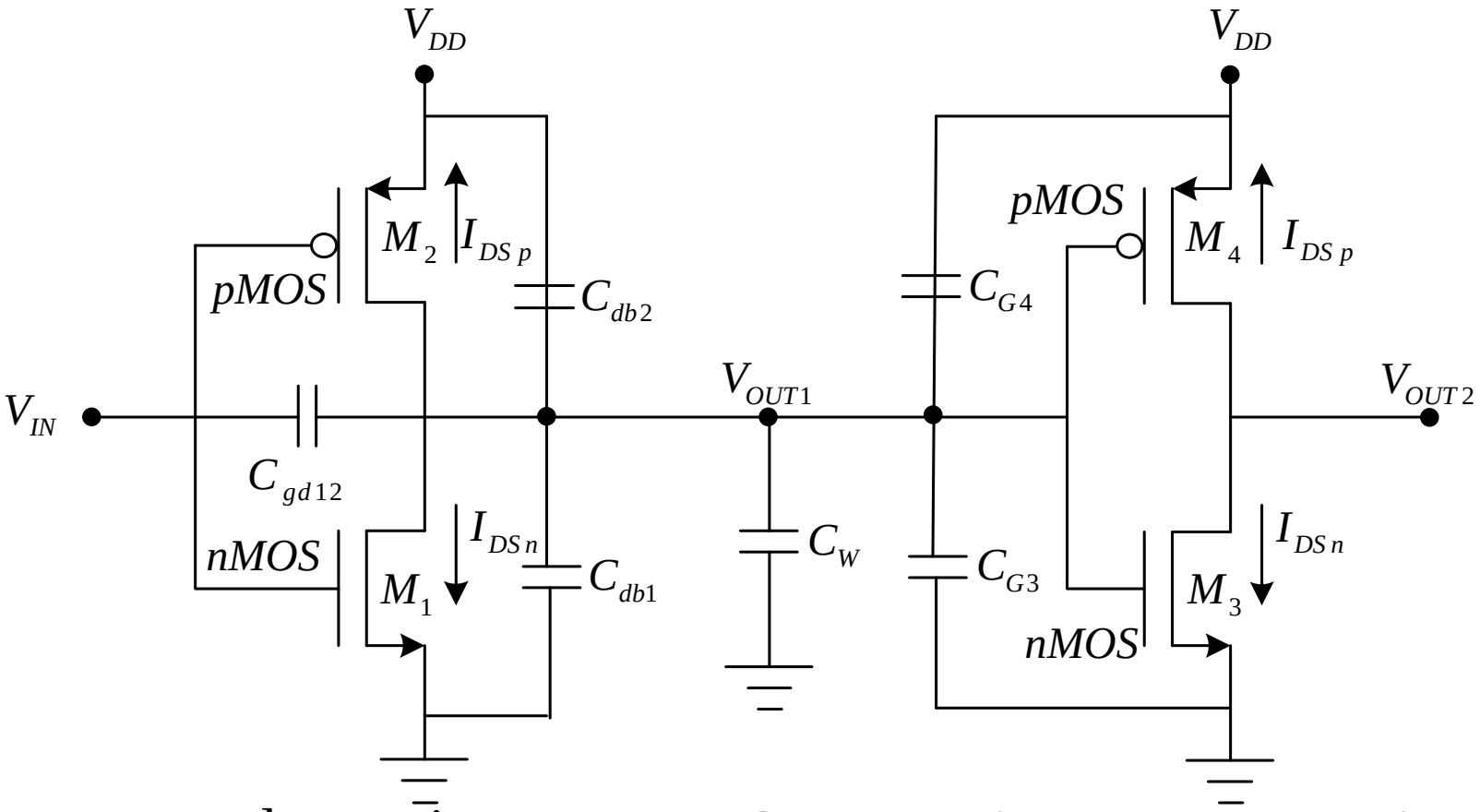


$$C_L = C_{\text{int}} + C_{ext}$$

C_{int} = internal capacitance of driver $\quad C_{db,12}$ = junction capacitance

$C_{gd,12}$ = gate capacitance (including Miller capacitance) $\quad C_{\text{int}} = C_{db,12} + C_{gd,12}$

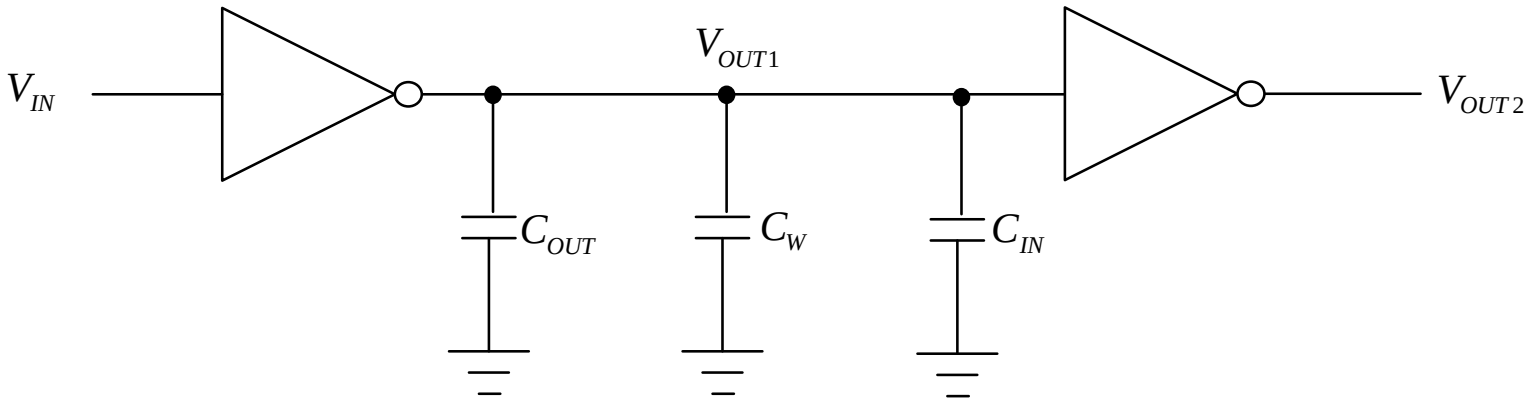
- Effect of Capacitance (lumped capacitor model)



C_{ext} = external capacitance $C_{g,43}$ = reciever gate capacitance

C_W = interconnect capcitance(wire) $C_{ext} = C_W + C_{g,43}$

- Inverter Chain

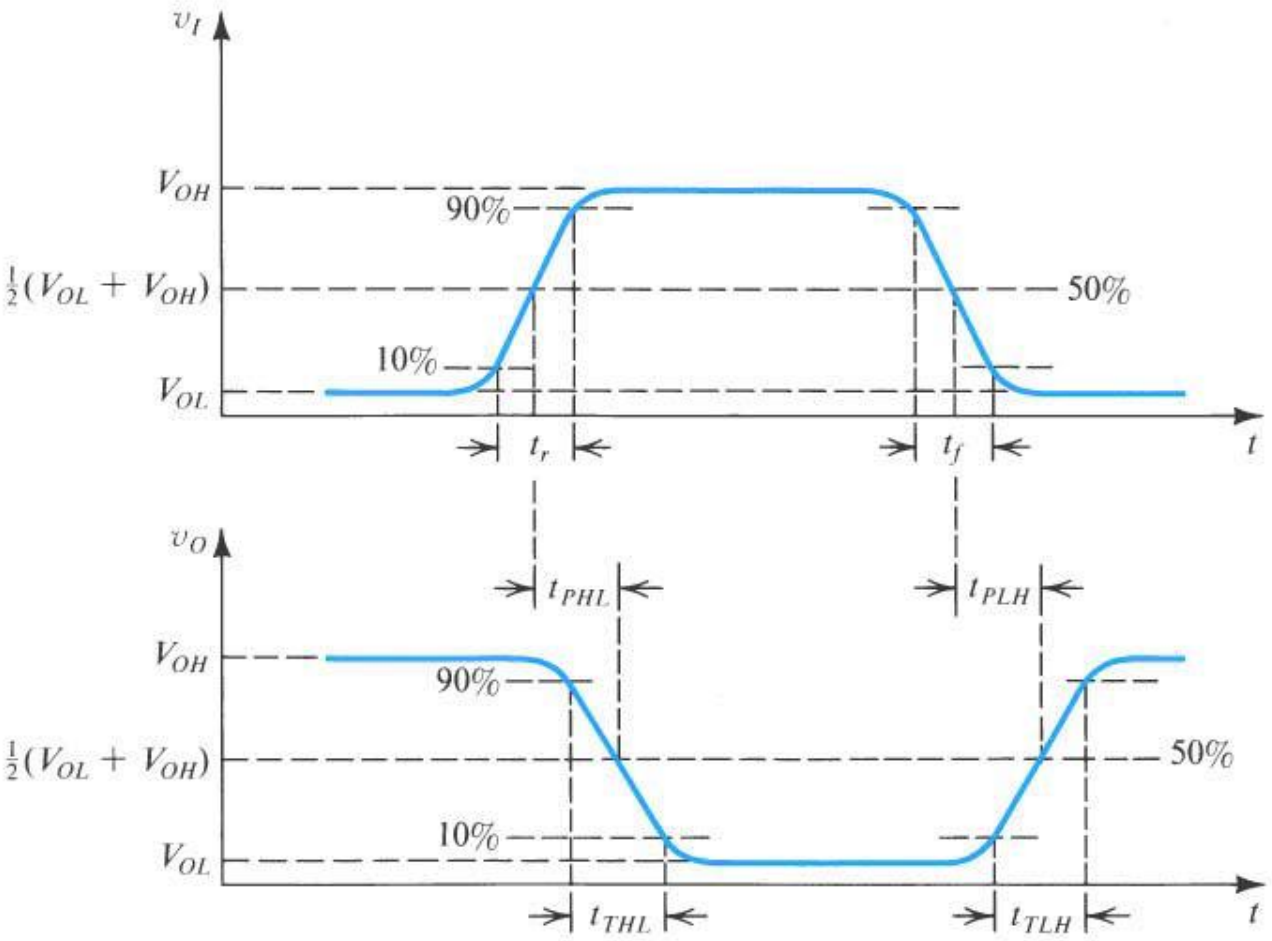


$$C_L = C_{OUT} + C_W + C_{IN}$$

$$C_{OUT} = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2}$$

$$C_{IN} = C_{g3} + C_{g4}$$

- Inverter Chain



- The dynamic of performance of a logic circuit is characterized by the propagation delay of its basic inverter.
- The inverter propagation delay τ_p is defined as the average of the low-to-high and the high-to-low propagation delay.

$$\tau_p = \frac{\tau_{pLH} + \tau_{pHL}}{2}$$

- The propagation delay τ_{pLH} and τ_{pHL} are defined as the time required for output voltage to reach between the low and high levels (%50 of V_{DD} in CMOS logic).
- The intrinsic propagation delay of the CMOS inverter that is loaded only by its own output capacitance C_{OUT}.

$$\tau_{p0} = \frac{\tau_{pLH0} + \tau_{pHL0}}{2}$$

- The pMOS and nMOS transistors can be replaced by equivalent resistance R_{eqp} and R_{eqn} when charging and discharging the capacitor C_{OUT} in simplified analysis.
- The pMOS acts as a resistor R_{eqp} when C_{OUT} is charged to and output switches from low-to-high. The intrinsic V_{DD} propagation delay is

$$\tau_{pLH0} = 0.69 R_{eqp} C_{OUT}$$

- The nMOS acts as a resistor R_{eqn} when C_{OUT} is discharged when output switches from high-to-low. The intrinsic propagation delay is

$$\tau_{pHL0} = 0.69 R_{eqn} C_{OUT}$$

$$\tau_{p0} = \frac{0.69 R_{eqp} C_{OUT} + 0.69 R_{eqn} C_{OUT}}{2}$$

$$\tau_{p0} = \frac{0.69R_{eqp}C_{OUT} + 0.69R_{eqn}C_{OUT}}{2}$$

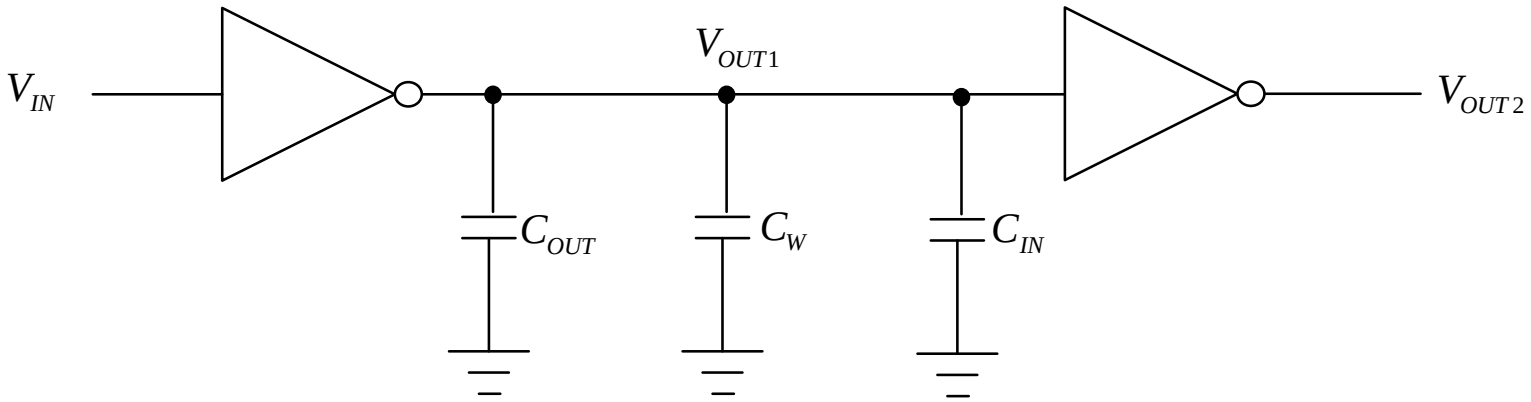
$$\tau_{p0} = \frac{0.69\left(R_{eqp} + R_{eqn}\right)C_{OUT}}{2} = \frac{0.69\left(R_{eq}\right)C_{OUT}}{2}$$

$$R_{eq} = R_{eqp} + R_{eqn}$$

$$C_L = C_{\text{int}} + C_{ext}$$

$$C_{\text{int}} = C_{OUT} + C_W$$

$$C_{ext} = C_{IN}$$



$$C_L = C_{\text{int}} + C_{ext}$$

$$C_{\text{int}} = C_{OUT} + C_W$$

$$C_{ext} = C_{IN}$$

$$C_L = C_{\text{int}}\left(1+\alpha\right)$$

- Intrinsic delay of CMOS inverter

$$\tau_p = 0.69 R_{eq} C_L$$

$$C_L = C_{\text{int}} + C_{ext}$$

$$\tau_p = 0.69 R_{eq} (C_{\text{int}} + C_{ext})$$

$$\tau_p = 0.69 R_{eq} C_{\text{int}} \left(1 + \frac{C_{ext}}{C_{\text{int}}}\right)$$

$$\tau_p = t_{po} \left(1 + \frac{C_{ext}}{C_{\text{int}}}\right)$$

$$\tau_{po} = \text{ the intrinsic delay}$$

- Impact of sizing on gate delay

- S= sizing factor
- R_{ref} = The resistance of reference inverter (Usually a minimum size inverter)
- Reference gate=minimum size gate
- C_{iref} = The internal capacitance of the reference gate

$$C_{\text{int}} = SC_{iref}$$

$$R_{eq} = \frac{R_{ef}}{S}$$

$$t_p = 0.69\left(\frac{R_{ef}}{S}\right)(C_{iref})\left(1+\frac{C_{ext}}{SC_{iref}}\right)$$

$$t_p = 0.69\left(R_{ref}\right)(C_{iref})\left(1+\frac{C_{ext}}{SC_{iref}}\right)$$

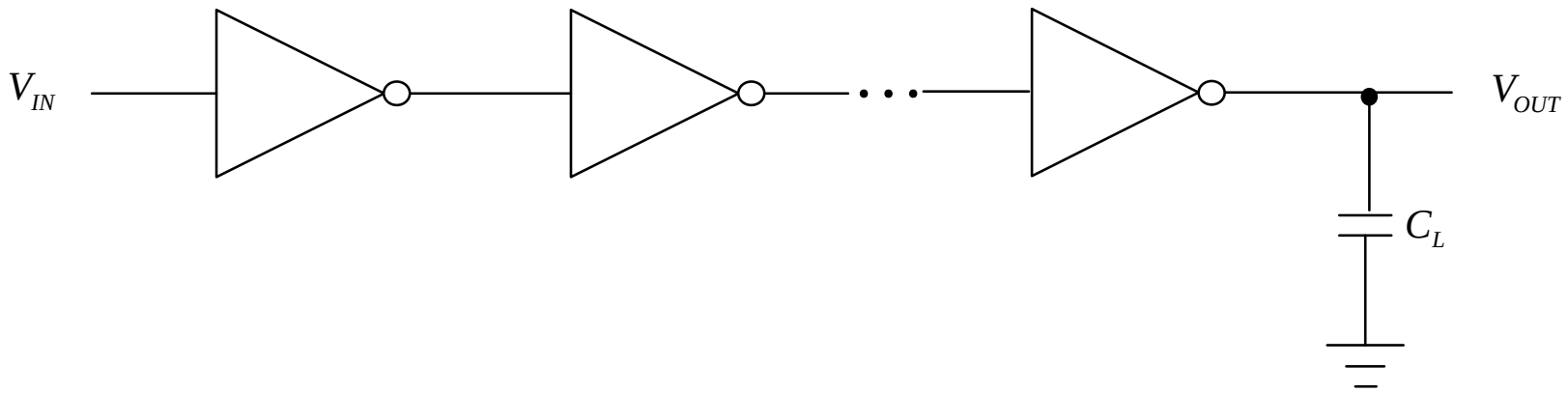
$$t_p = t_{po}\left(1+\frac{C_{ext}}{SC_{iref}}\right)$$

- Impact of sizing on gate delay

$$t_p = t_{po}\left(1 + \frac{C_{ext}}{SC_{iref}}\right)$$

- 1) Intrinsic delay is independent of gate sizing and determined only by technology and inverter layout
- 2) If S is made very large, gate delay approaches the intrinsic value but increases the area significantly.

- Inverter Chain



- Given C_L
- 1) How many stages of inverter are needed to minimize the delay?
- 2) How to size the inverter?

- Inverter delay
- Minimum length devices, $L = 0.25\mu m$
- Assumption : for example $W_p = 2W_N = 2W$
  a) Same pull up and pull down currents
  b) $R_N = R_P$: approximately equal resistance
  c) $t_{pHL} = t_{pLH}$: equal rise and fall delay
- Analyze as an RC network
- Delay (D)

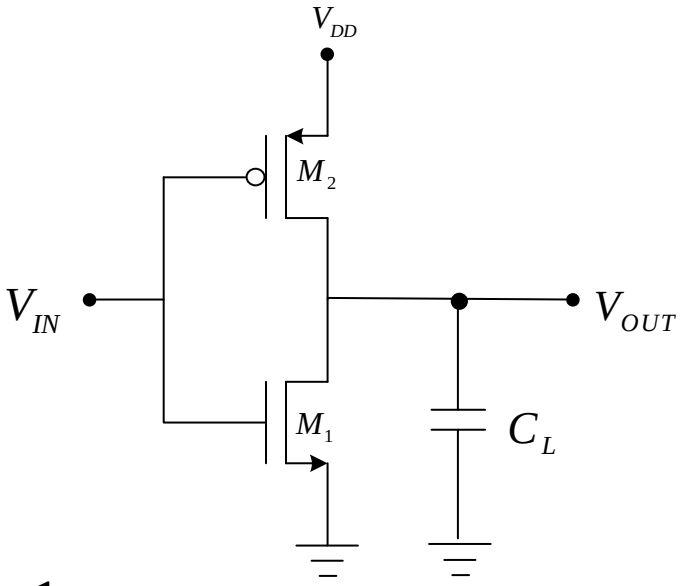
$$t_{pHL} = \ln 2 R_N C_N$$

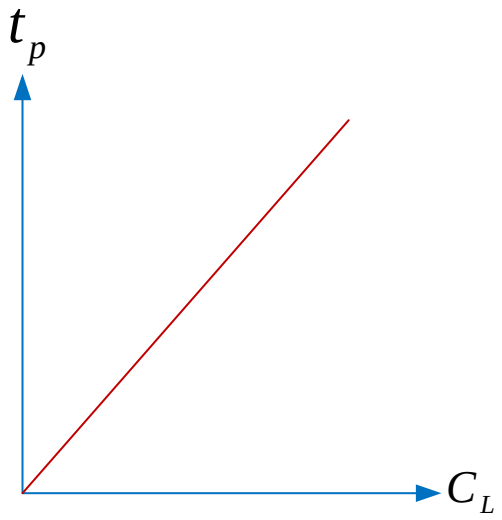
$$t_{pLH} = \ln 2 R_p C_p$$

- Load for the next stage

$$C_{g,in} = 3\frac{W}{W_{unit}} C_{unit}$$

- Voltage supply scaling





$$W_{unit} = 1$$

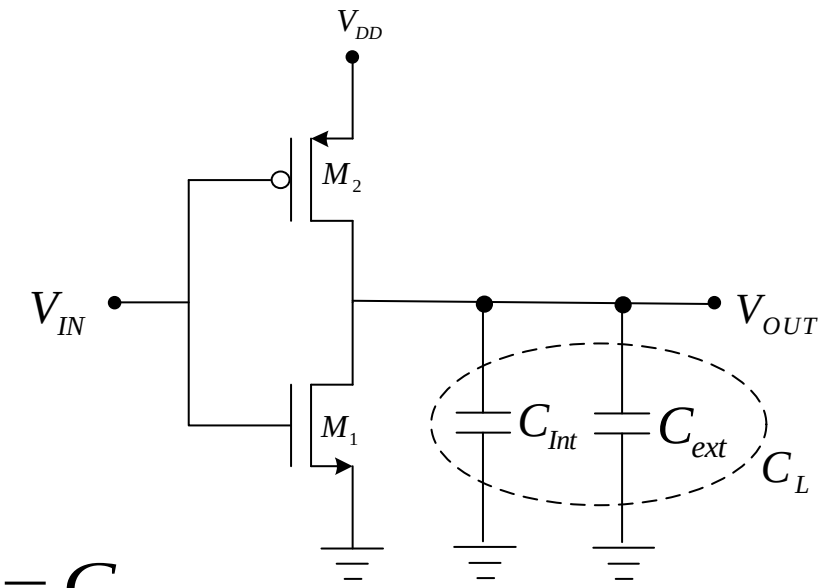
$$t_p = kR_W C_L$$

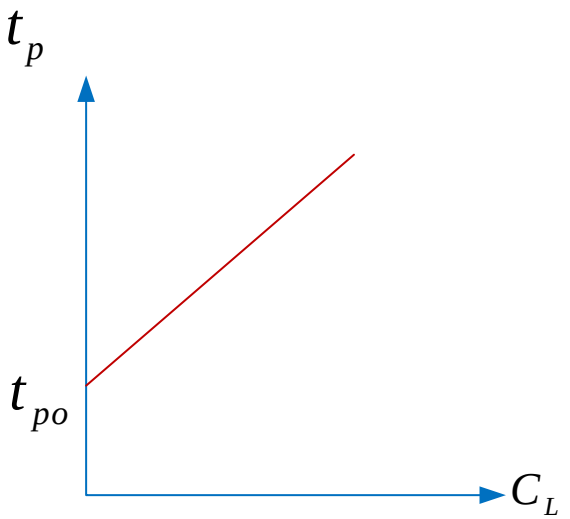
$$K = 0.69 = \text{constant}$$

- Assumption:

$$\text{no load} \rightarrow \text{zero delay}$$

- Inverter with load





$$C_N = C_{unit}$$

$$delay(t_p) = kR_W(C_{\text{int}} + C_{ext}) = kR_W C_{\text{int}} + kR_W C_{ext}$$

$$= kR_W C_{\text{int}}\left(1 + \frac{C_{ext}}{C_{\text{int}}}\right) = t_{po}\left(1 + \frac{C_{ext}}{C_{\text{int}}}\right)$$

$$t_{po} = kR_W C_W$$

- Delay formula: inverter chain

$$C_{\text{int}} = \gamma C_{gin}$$

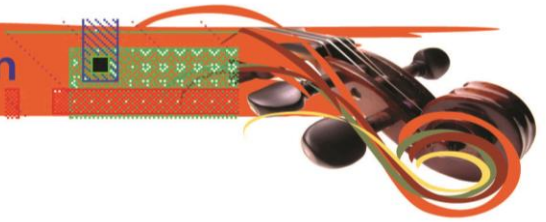
$$\gamma \simeq 1$$

$$f = \frac{C_{ext}}{C_{gin}} = effective\ \ fanout$$

$$t_{po} = 0.69 R_{eq} C_{\text{int}}$$

$$delay \simeq R_{eq}(C_{\text{int}} + C_{ext})$$

$$t_p = 0.69 R_{eq} C_{\text{int}} \left(1 + \frac{C_{ext}}{C_{\text{int}}}\right) = t_{po}\left(1 + \frac{f}{\gamma}\right)$$



- Apply to inverter Chain

$$t_p = t_{p1} + t_{p2} + \ldots\ldots\ldots + t_{pN}$$

$$t_{p,j} = t_{po}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right)$$

$$t_{p,j} = \sum_{j=1}^{N} t_{p,j} = t_{po}\sum_{i=1}^{N}\left(1 + \frac{C_{gin,j+1}}{\gamma C_{gin,j}}\right)$$

$$C_{gin,N+1} = C_L$$

- Optimal tapering for given N
- Delay equation has N-1 unknowns, $C_{g,2}, \ldots\ldots\ldots\ldots C_{g,N}$
- Minimize the delay, find N-1 partial derivatives
- Results:

$$\frac{C_{g,j+1}}{C_{g,j}} = \frac{C_{g,j}}{C_{g,j-1}} \quad for\ j = 2,\ldots\ldots,N$$

- Size of each stage is the geometric mean of two neighbours

$$C_{g,j} = \sqrt{C_{g,j-1}, (C_{g,j+1})}$$

- Each stage has the same effective fanout $= f_j = f = \frac{C_{ext}}{C_{g,j}}$
- each stage has the same delay

$$t_p = t_{po}\left(1 + \frac{f}{\gamma}\right)$$

- Optimum delay and number of stages f

$$\frac{C_L}{C_{g,N}} = \frac{C_{g,N}}{C_{g,N-1}} = \cdots\cdots = \frac{C_{g,2}}{C_{g,1}} = f$$

$$f^N = \frac{C_L}{C_{g,1}} = F$$

$$f = \sqrt[N]{F}$$

$$t_p = Nt_{po}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)$$

- If N is too large, intrinsic delay of stages dominate, while if N is small, effective fanout of each stage(f) is large and the second term dominates.

- Example: How to choose N?

- $\frac{C_L}{C_1}$ has to be evenly distributed across N=3 stages

$$\frac{C_L}{C_{\text{int}}} = \frac{8C_1}{C_1} = 8$$

$$f = \sqrt[3]{8} = 2$$

- For a given load C_L and given input capacitance C_{in} find optimal sizing f.

$$C_L = FC_{in} = f^N C_{in}$$

$$N = \frac{\ln F}{\ln f}$$

$$t_p = Nt_{po}\left(\frac{\sqrt[N]{F}}{\gamma+1}\right) = \frac{t_{po}\ln F}{\gamma}\left(\frac{f}{\ln f}+\frac{\gamma}{\ln f}\right)$$

$$\frac{\partial t_p}{\partial f} = \frac{t_{po}\ln F}{\gamma}\bullet\frac{\ln f - 1 - \frac{\gamma}{f}}{\ln^2 f} = 0$$

- If self loading is ignored
- For $\gamma = 0, f = e, N = \ln F$

$$f = e^{1+\frac{\gamma}{f}}$$

- Optimum f for given process defined by γ optimum tapering factor

$$f_{opt} = 3.6$$
$$for\ \gamma = 1$$

- Impact of self loading on t_p
- No self loading for $\gamma = 0$
- Optimal # of stages
- $N = \ln F$

$$t_p(normalized) = \frac{t_p}{t_{po}}$$

- With self loading $\gamma = 1$
- If $f < f_{opt}$ (too many stages) will result in delay to increase
- Normalized delay function of F

$$t_p = Nt_{po}\left(1 + \frac{\sqrt[N]{F}}{\gamma}\right)$$

$$\frac{t_p(opt)}{t_{po}} \; for \; \gamma = 1$$

- Buffer design
- N f t_p

  1 64 65

  2 8 18

  3 4 15

  4 2.8 15.