Characteristic Curves of Silicon Nanowire Surrounding Gate Field Effect Transistors

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***Abstract*—The main purpose of this assignment is to develop an understanding for the basic tools used in the Cadence Virtuoso Analog-Design Environment (ADE) essential for designing & analyzing any analog circuit. In addition to that, the characteristics of the NMOS & PMOS transistors in the novel technology of the 10nm silicon nanowire surrounding gate field effect transistor (SGFET) are studied for future use in the design of larger integrated circuits.**

***Index Terms*— Cadence virtuoso, I-V curves, SGFET, Field-effect transistors**

I. Introduction

THE behavior of transistors differ from one technology to another, so it is essential to study the characteristics of the technology being used before employing it in designing integrated circuits. One way to do that is by observing the IV curves of the transistors which explain how the drain current, I_D, behaves as the terminal voltages change.[1]

In this assignment, a novel technology, namely the "silicon nanowire SGFET", is studied. The intrinsic part of the transistor device in this technology consists mainly of a channel, 10nm in length & 2nm in radius, completely surrounded by the gate. This structure gives full control to the gate on the channel eliminating some crucial short-channel effects like drain-induce barrier lowering (DIBL). This technology shows very promising potential for Analog & RF applications.[2]

II. Test bench setup

The test bench setups for the NMOS transistor & the PMOS transistor are shown in Fig. 1 & 2, respectively. The gate & drain terminal voltages are swept with respect to the source terminal voltage using DC sources connected to the gate & the drain.

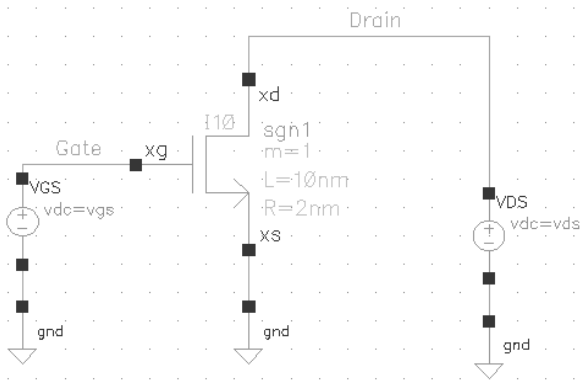


Fig. 1. NMOS transistor test bench setup

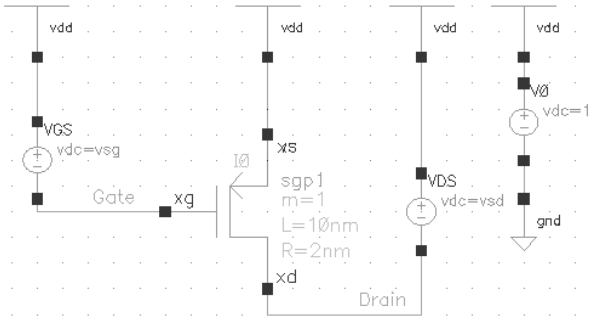


Fig. 2. PMOS transistor test bench setup

III. DC Analysis & Results

A. Drain Current while changing Gate Voltage

For the NMOS transistor, to get the I_D-V_{GS} curve, the V_{DS} is fixed at a certain value (1V in our setup) while sweeping V_{GS} with an increment of 10mV. In case of the PMOS transistor, the same procedure is conducted with the slight difference of changing the voltage difference polarity, so the I_D-V_{SG} is obtained while keeping V_{SD} fixed at 1V. The curves for the NMOS & PMOS transistors are shown in Fig. 3 & 4, respectively.

It is worth to mention that I_D increases dramatically after the V_{GS} (or V_{SG} in case of the PMOS) reaches a certain voltage value called the "Threshold voltage" or "V_{TH}", which is about 0.26V in NMOS & -0.28V in PMOS.

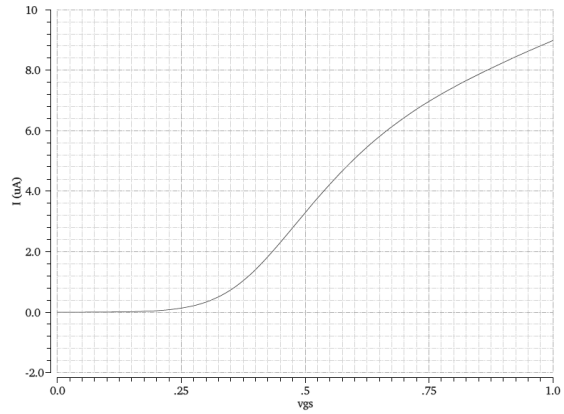


Fig. 3. I_D-V_{GS} curve for the NMOS transistor

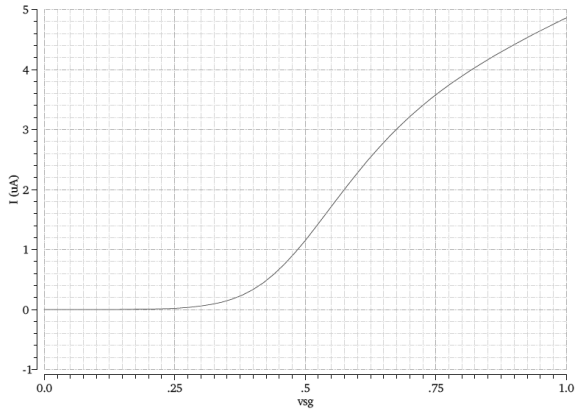


Fig. 4. I_D-V_{SG} curve for the PMOS transistor

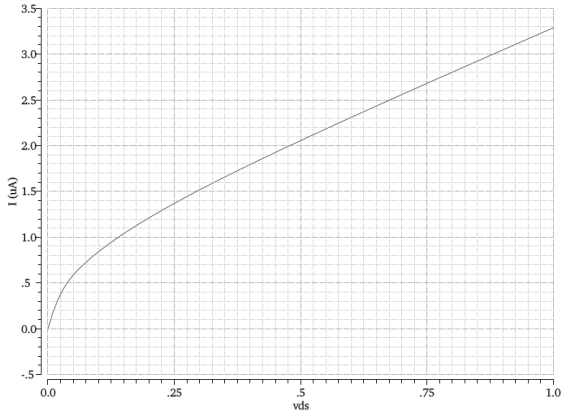


Fig. 5. I_D-V_{DS} curve for the NMOS transistor

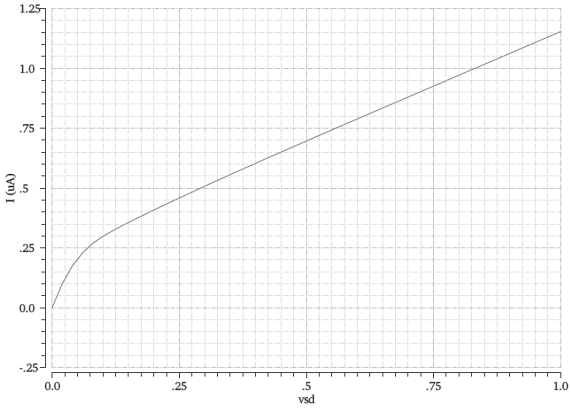


Fig. 6. I_D-V_{SD} curve for the PMOS transistor

B. Drain Current while changing Drain Voltage

To get the I_D-V_{DS} curve in the case of the NMOS transistor, the V_{GS} is now kept fixed at a certain value (0.5V in our setup) while sweeping V_{DS} with an increment of 10mV. In case of the PMOS transistor, V_{SG} & V_{SD} are used instead of V_{GS} & V_{DS}, respectively. The output characteristic curves are shown in Fig. 5 & 6.

C. Output Resistance r_{ds}

The resistance of the MOSFET transistor can be calculated as the inverse of the derivative of the drain current I_D with respect to the drain-source voltage V_{DS}. This relationship can be shown in equation (1).

$$r_{ds} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} \quad (1)$$

The curves for the resistance r_{ds} can be obtained using the calculator function in the ADE while sweeping the value of V_{DS} at a fixed value of V_{GS}. Using the same tool, the second & third derivatives can also be obtained. These curves are shown in Fig. 7(a), (b), & (c) for the NMOS, and Fig. 8(a), (b), & (c) for the PMOS.

D. Transconductance g_m

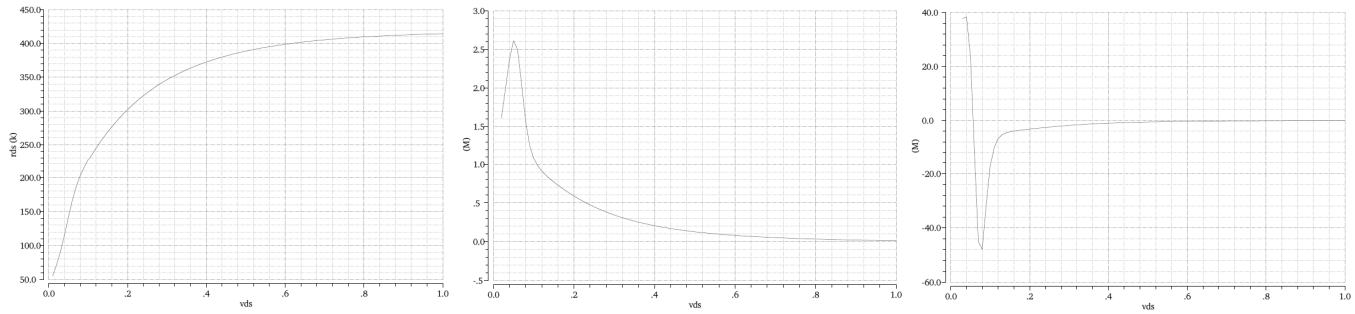
The transconductance of the MOSFET transistor is calculated by taking the derivative of the drain current I_D with respect to the gate-source voltage V_{GS} as expressed in equation (2).

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right) \quad (2)$$

Similar to what was done for r_{ds}, using the calculator function in the ADE while sweeping the value of V_{GS} at a fixed value of V_{DS}, the curve for g_m, the second & the third derivatives can be obtained. These curves are shown in Fig. 9(a), (b), & (c) for the NMOS, and Fig. 10(a), (b), & (c) for the PMOS.

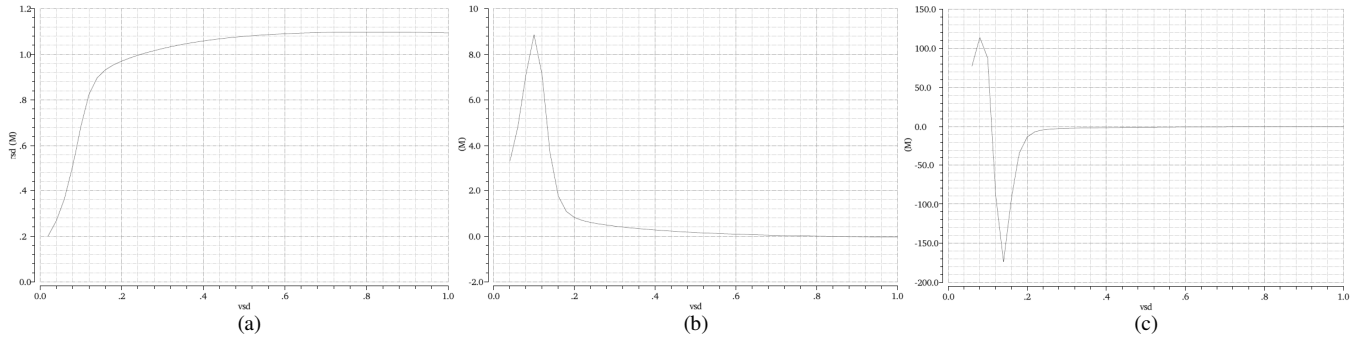
It is noticed that g_m increases with the increase of V_{GS} till it reaches a peak value, then starts to drop as V_{GS} continues to increase. This is because g_m is the slope of the I_D-V_{GS} curve, and as shown in Fig. 3 & 4, the increase of I_D starts to fall at high values of V_{GS}, as if I_D is reaching a saturation point after which the effect of increasing V_{GS} is not as strong. As a result, g_m starts to fall after a peak value as V_{GS} further increases.

The maximum g_m value for the NMOS transistor is 19.74 uS & it occurs at V_{GS}=488.57mV, while for the PMOS transistor, it is 11.48 uS at V_{SG}=558.15mV.



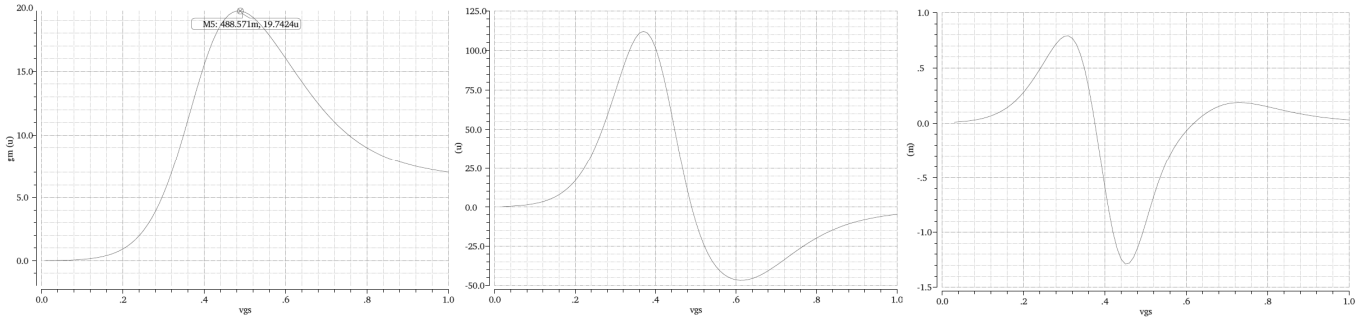
(a) (b) (c)

Fig. 7. (a) r_{ds}, (b) its 2nd derivative, & (c) its 3rd derivative curves for the NMOS transistor



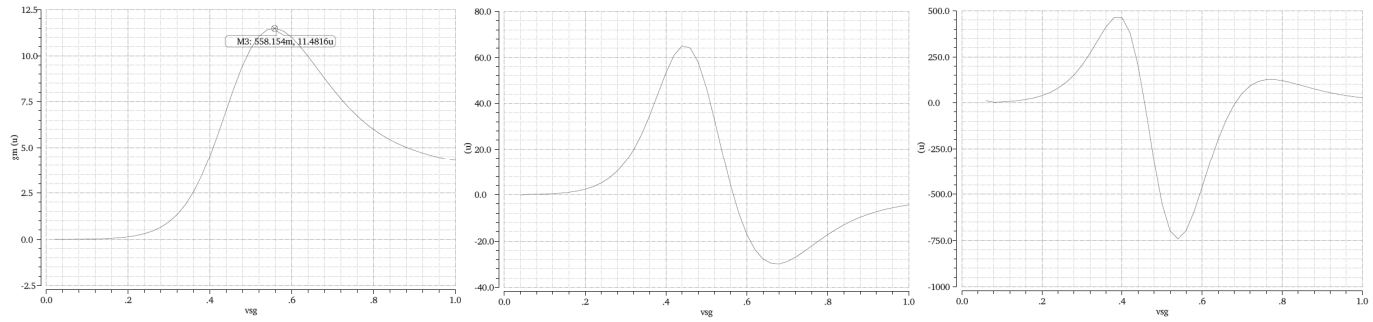
(a) (b) (c)

Fig. 8. (a) r_{sd}, (b) its 2nd derivative, & (c) its 3rd derivative curves for the PMOS transistor



(a) (b) (c)

Fig. 9. (a) g_m, (b) its 2nd derivative, & (c) its 3rd derivative curves for the NMOS transistor



(a) (b) (c)

Fig. 10. (a) g_m, (b) its 2nd derivative, & (c) its 3rd derivative curves for the PMOS transistor

IV. Parametric Analysis

The parametric analysis is a useful tool to observe the characteristic curves while changing two variables at the same time. Almost the same steps are conducted as before but at different values of a second variable.

The results will be similar curves to the ones obtained before in the DC analysis, but now there is a curve for each value of the second variable, all appended to the same graph window for the purpose of comparison & observation.

In the following subsections, a variable that was fixed in one of the previous analyses will be swept over a number of values. The number of steps is chosen such that the simulation would not consume a lot of time.

A. Drain Current curves

The I_D-V_{GS} curve is obtained as before, but with also sweeping V_{DS} with an increment of 100mV, as shown in Fig. 11 & 12. It is shown that the I_D-V_{GS} curve is raised as the value of V_{DS} increases, which means a higher V_{DS} results in greater I_D to flow at any V_{DS}.

The same goes for the I_D-V_{DS} curve, but this time V_{GS} is swept with an increment of 100mV, as shown in Fig. 13 & 14. The I_D-V_{DS} curves are raised as the value of V_{GS} increases, because V_{GS} is responsible for the channel formation, so higher V_{GS} gives greater channel.

B. Output Resistance r_{ds}

Using equation (1) in the ADE calculator, the r_{ds} curve is obtained for different values of V_{GS} with a step of 100mV, as shown in Fig. 15(a) for NMOS & Fig. 16(a) for PMOS. The curves of the second & the third derivatives of I_D with respect to V_{DS} are also obtained at these V_{GS} values.

The curves for r_{ds} are drawn on a semi-log scale because the values of r_{ds} could vary from a few Kilo-ohms to Mega-ohms. That's because when the values of the V_{GS} are very low, the transistor is in the cutoff region or near it, where there is almost no channel for the current to flow. As V_{GS} increases, a channel starts to form, allowing the flow of current, thus represented by lower values of r_{ds}.

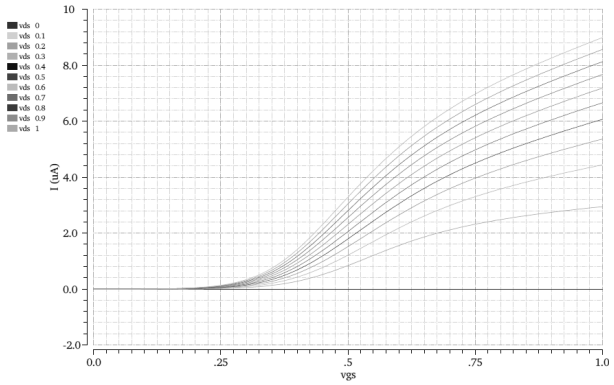


Fig. 11. I_D-V_{GS} curves at different V_{DS} values for the NMOS transistor

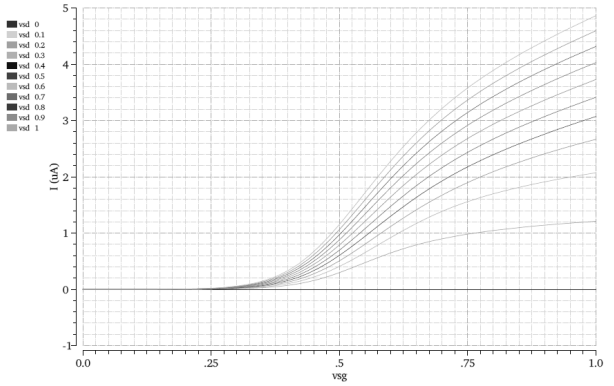


Fig. 12. I_D-V_{SG} curves at different V_{SD} values for the PMOS transistor

C. Transconductance g_m

Similar to what was done for the r_{ds} curves, the curves for g_m, the second & the third derivatives of I_D with respect to V_{GS} are obtained at the different values of V_{DS}. The curves are shown in Fig. 17(a), (b), & (c) for NMOS, and 18(a) (b), & (c) for PMOS.

As seen in Fig. 11 & 12, having a greater V_{DS} results in a greater I_D flowing in the channel for the whole V_{GS} range. So, when observing the curves of g_m in 17(a) for NMOS & 18(a) for PMOS, increasing the V_{DS} causes an increase for g_m at any V_{GS}.

V. CONCLUSION

This document presented the behavior of the drain current, I_D, with respect to the terminal voltages, V_{GS} & V_{DS}, for the Nanowire SGFET transistors. The curves for the drain-source resistance, r_{ds}, & the transconductance, g_m, are also presented, along with the second & third derivatives of I_D with respect to V_{GS} & V_{DS}.

These curves & parameters are essential for the building, the designing & the analysis of any analog integrated circuit that will utilize the Nanowire SGFET technology.

The steps of how these curves were obtained using the Cadence Virtuoso Analog Design Environment & its different tools were also explicitly explained so they would be the basis for future circuit design work.

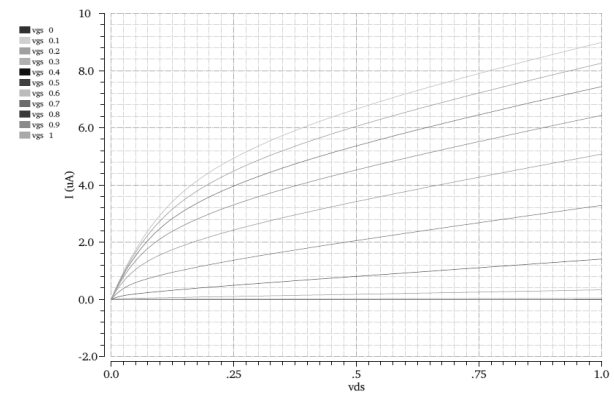


Fig. 13. I_D-V_{DS} curves at different V_{GS} values for the NMOS transistor

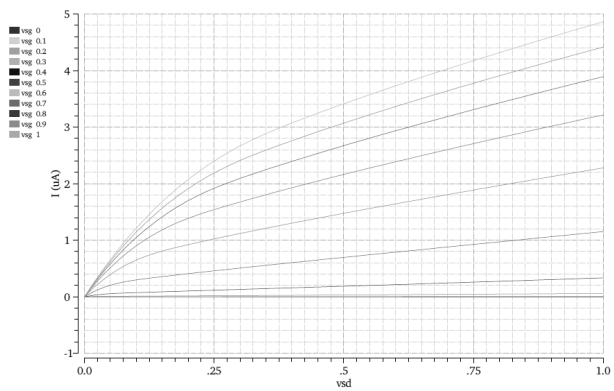


Fig. 14. I_D-V_{SD} curves at different V_{SG} values for the PMOS transistor

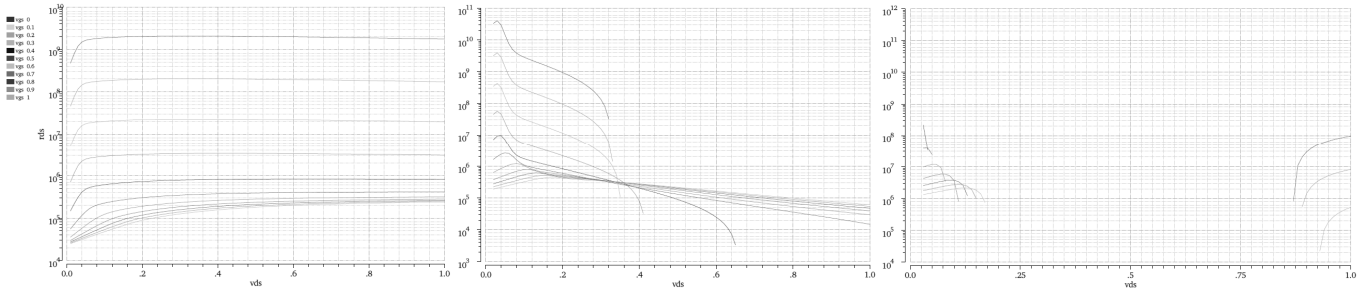


Fig. 15. (a) r_{ds}, (b) its 2nd derivative, & (c) its 3rd derivative curves at different V_{GS} values for the NMOS transistor

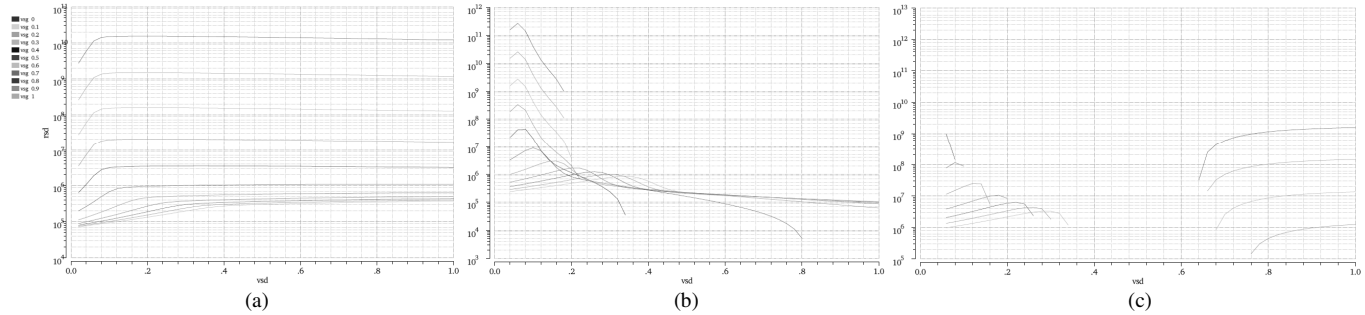


Fig. 16. (a) r_{sd}, (b) its 2nd derivative, & (c) its 3rd derivative curves at different V_{SG} values for the PMOS transistor

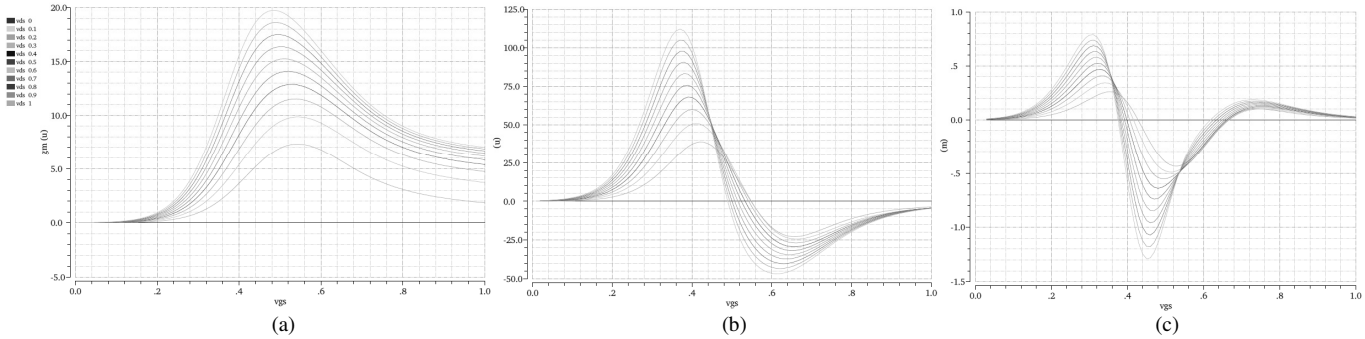


Fig. 17. (a) g_m, (b) its 2nd derivative, & (c) its 3rd derivative curves at different V_{DS} values for the NMOS transistor

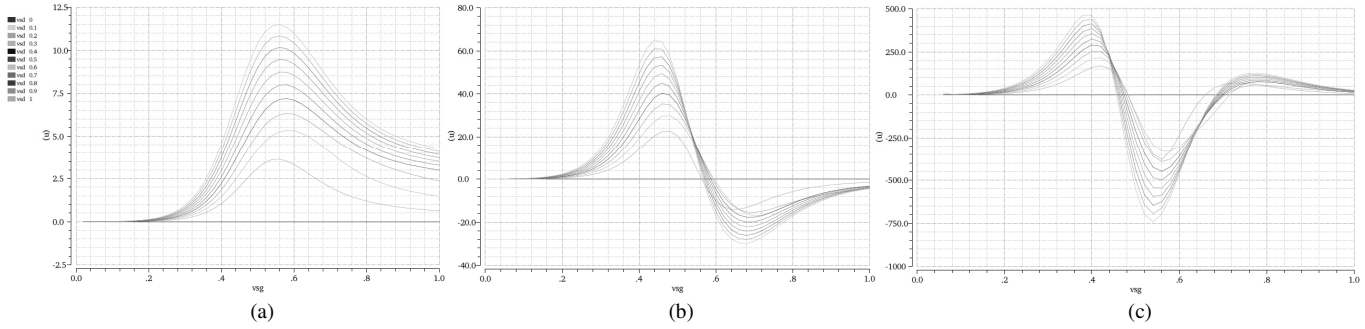


Fig. 18. (a) g_m, (b) its 2nd derivative, & (c) its 3rd derivative curves at different V_{SD} values for the PMOS transistor

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