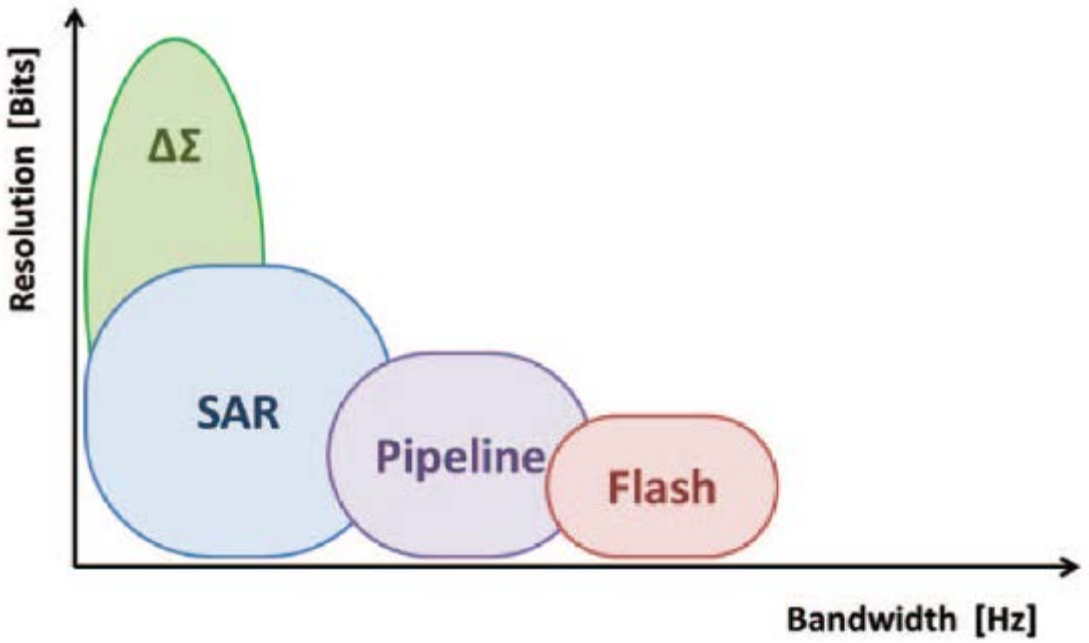
EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 25: ADC Trends

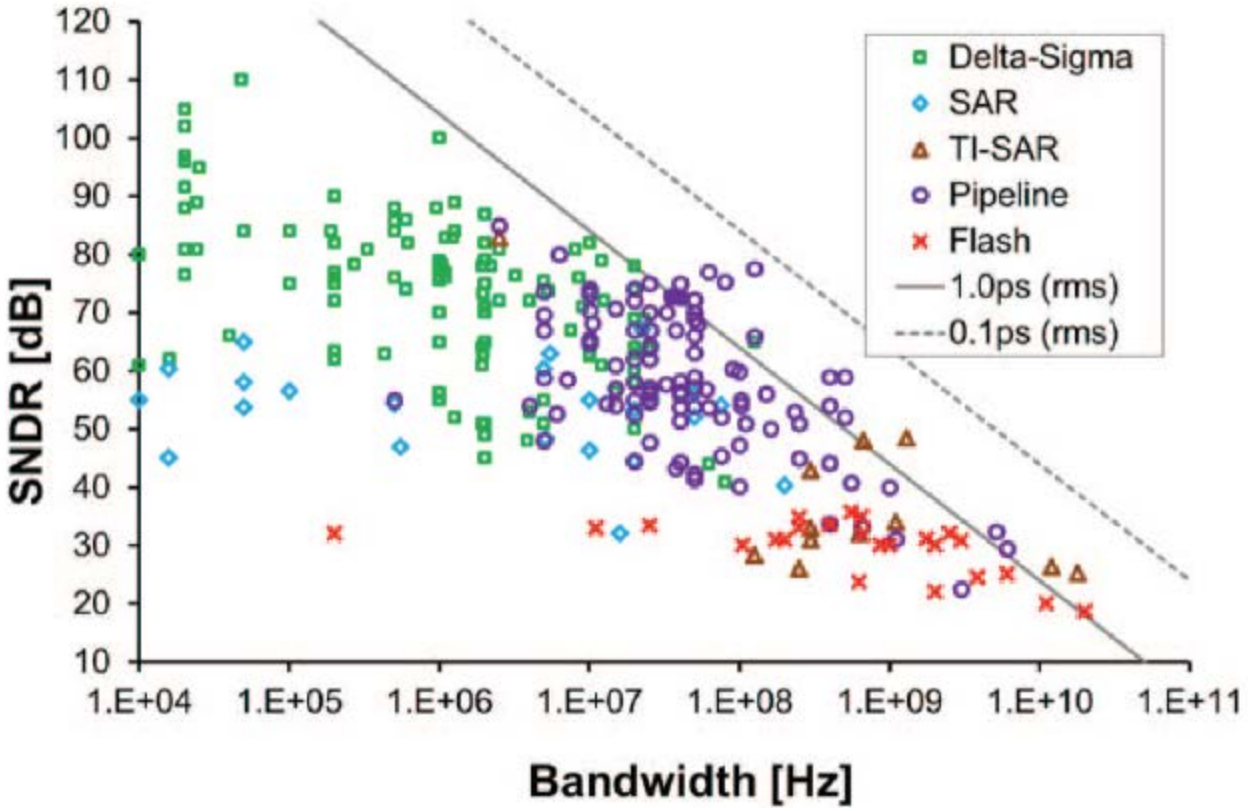
Prof. Sang-Soo Lee
sang-soo.lee@sjsu.edu
ENG-259

ADC Architectures

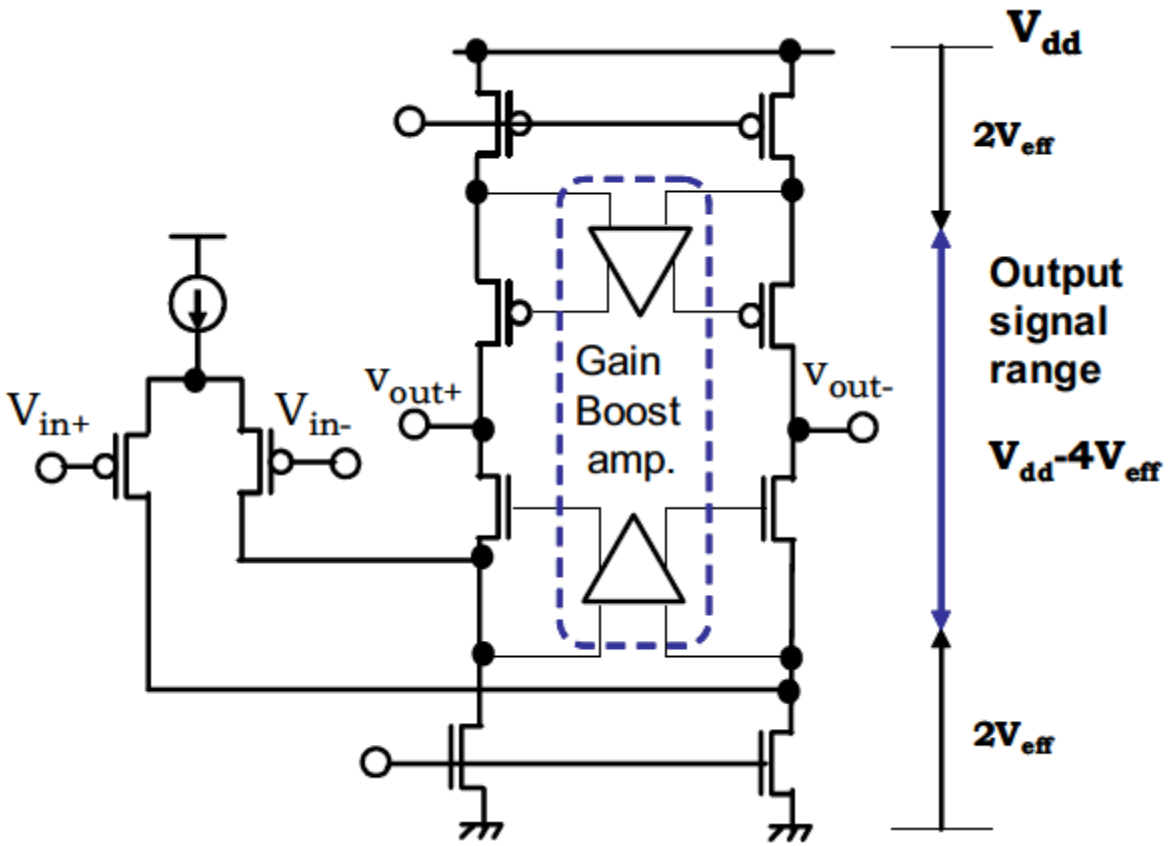


Resolution vs. Bandwidth

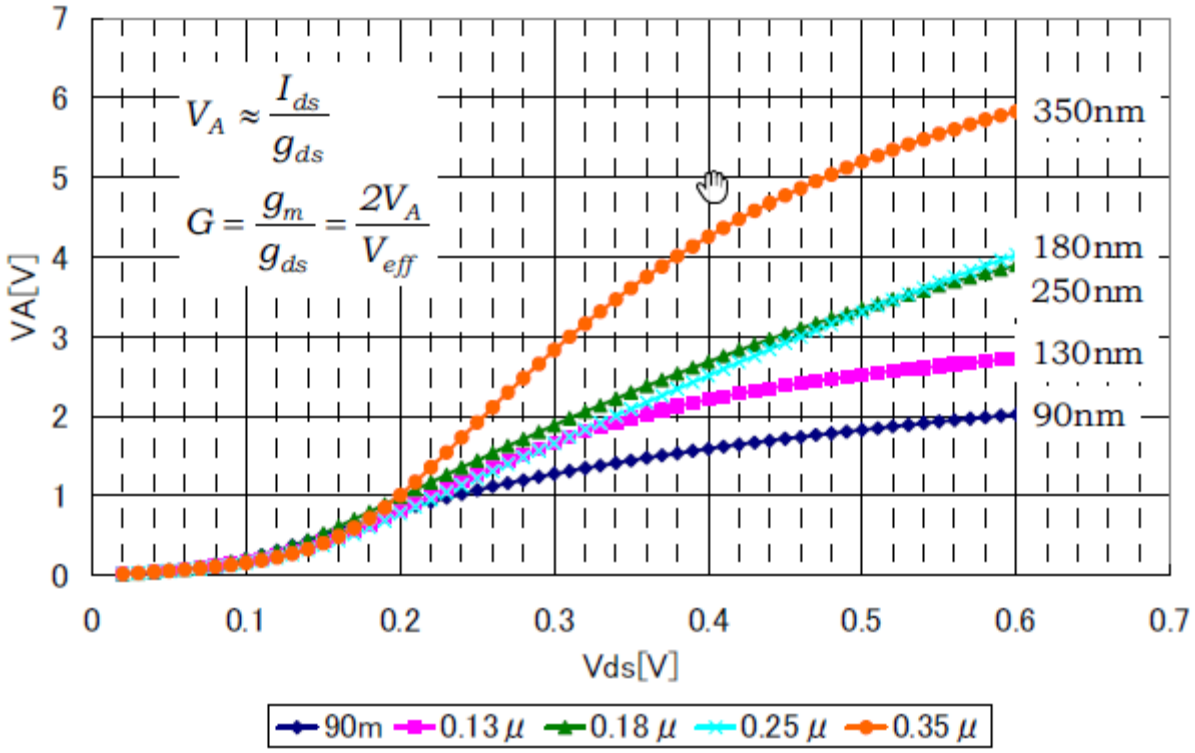
B. Murmann. ADC performance survey 1997–2015. [Online]. Mar. 2015. Available: http://web.stanford.edu/~murmann/adcsurvey.html



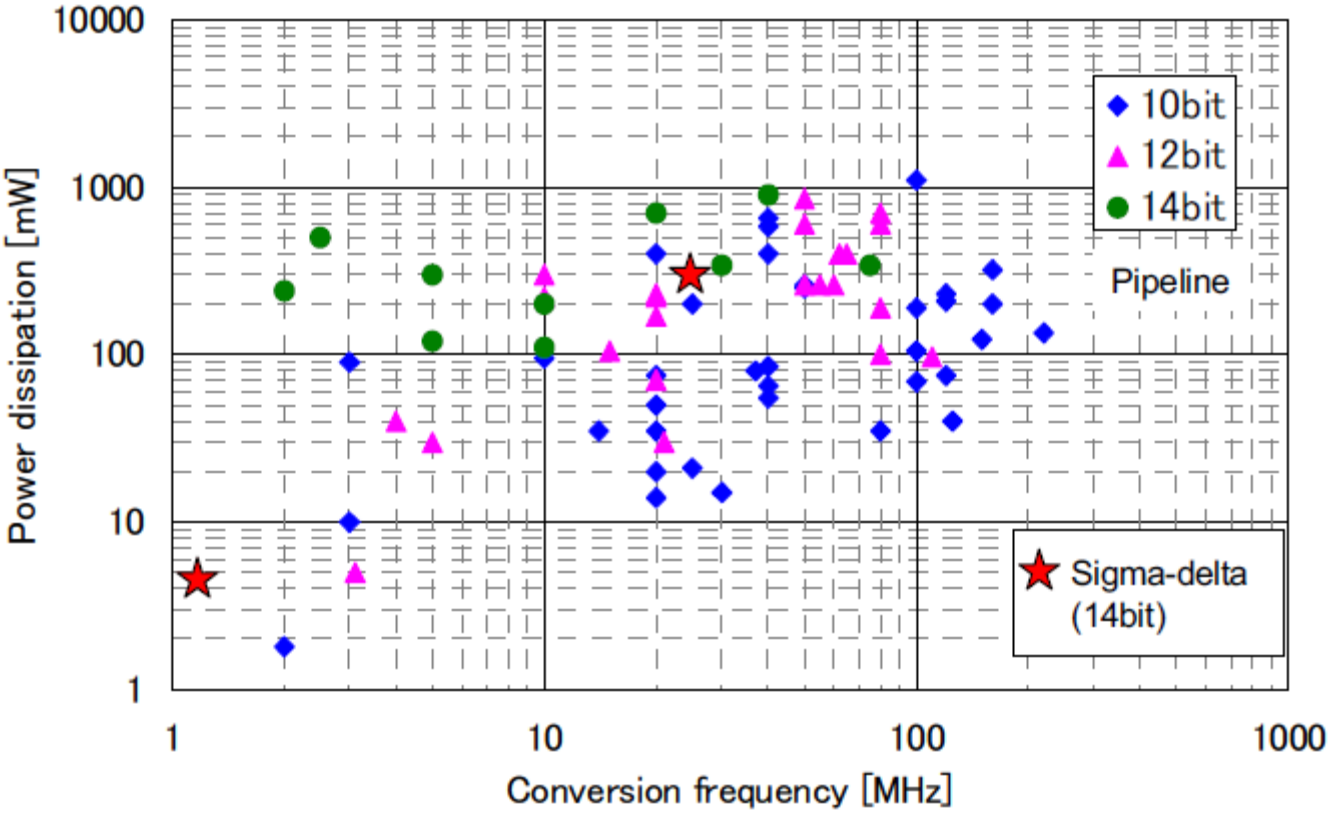
OPAMP for Pipelined ADC



V_A vs V_{ds}


$V_A \approx \frac{I_{ds}}{g_{ds}}$
$G = \frac{g_m}{g_{ds}} = \frac{2V_A}{V_{eff}}$
350nm
180nm
250nm
130nm
90nm
VA[V]
Vds[V]
0
1
2
3
4
5
6
7
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
90m
0.13 μ
0.18 μ
0.25 μ
0.35 μ

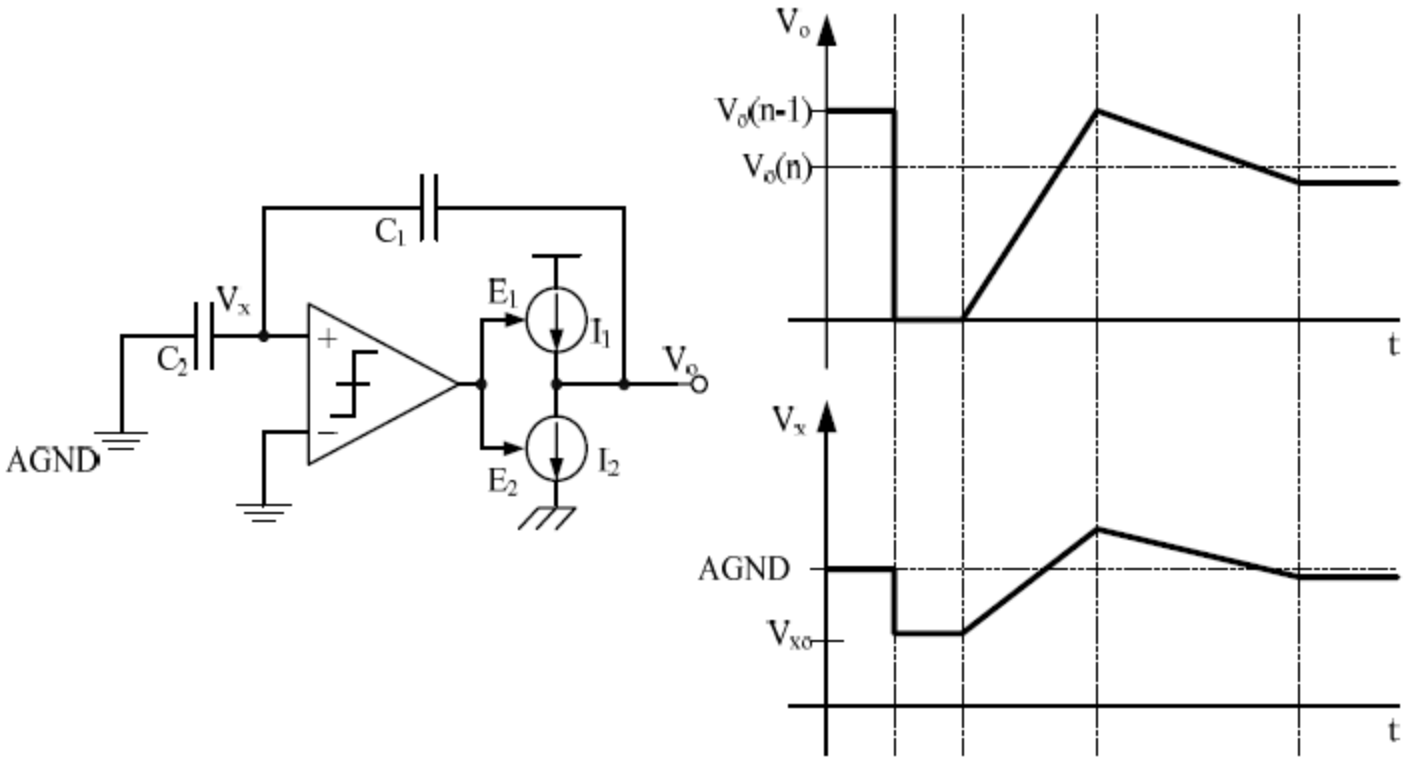
Power vs. Conversion Speed



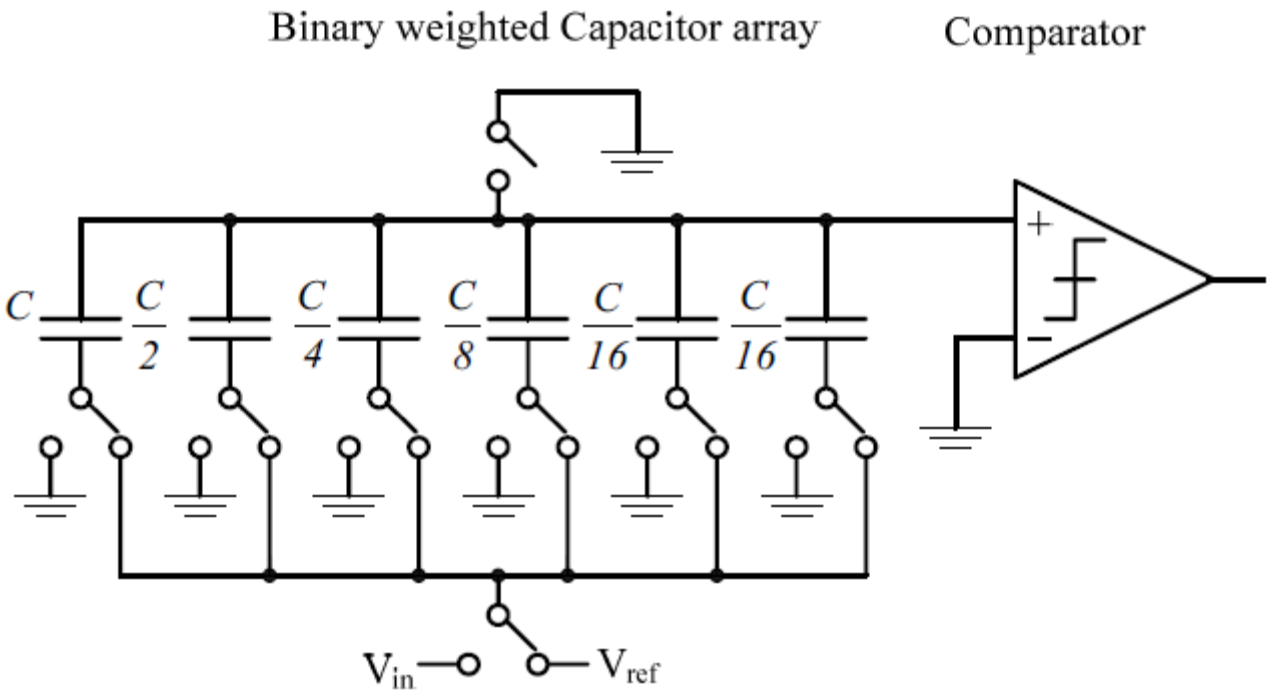
High-Speed ADC Architecture Trends

- ADC without OPAMP
  - Comparator based Architecture
  - SAR ADC
- Time-interleaved ADC
- Hybrids ADC
  - Pipelined SAR ADC
- Digitally Assisted ADC

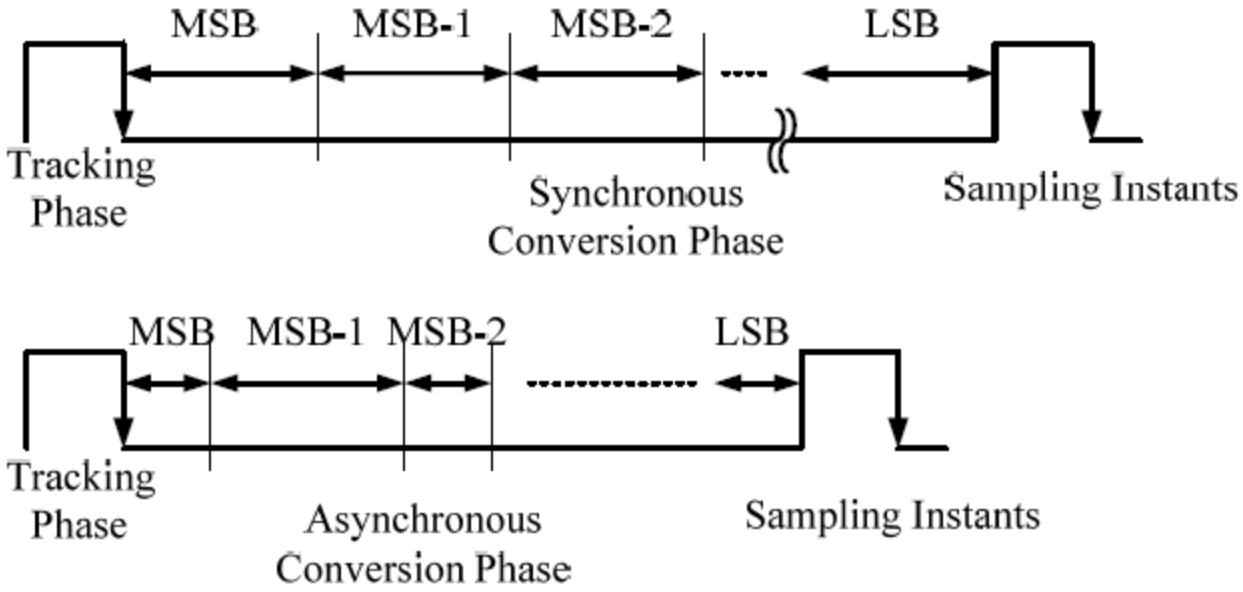
Comparator controlled current source



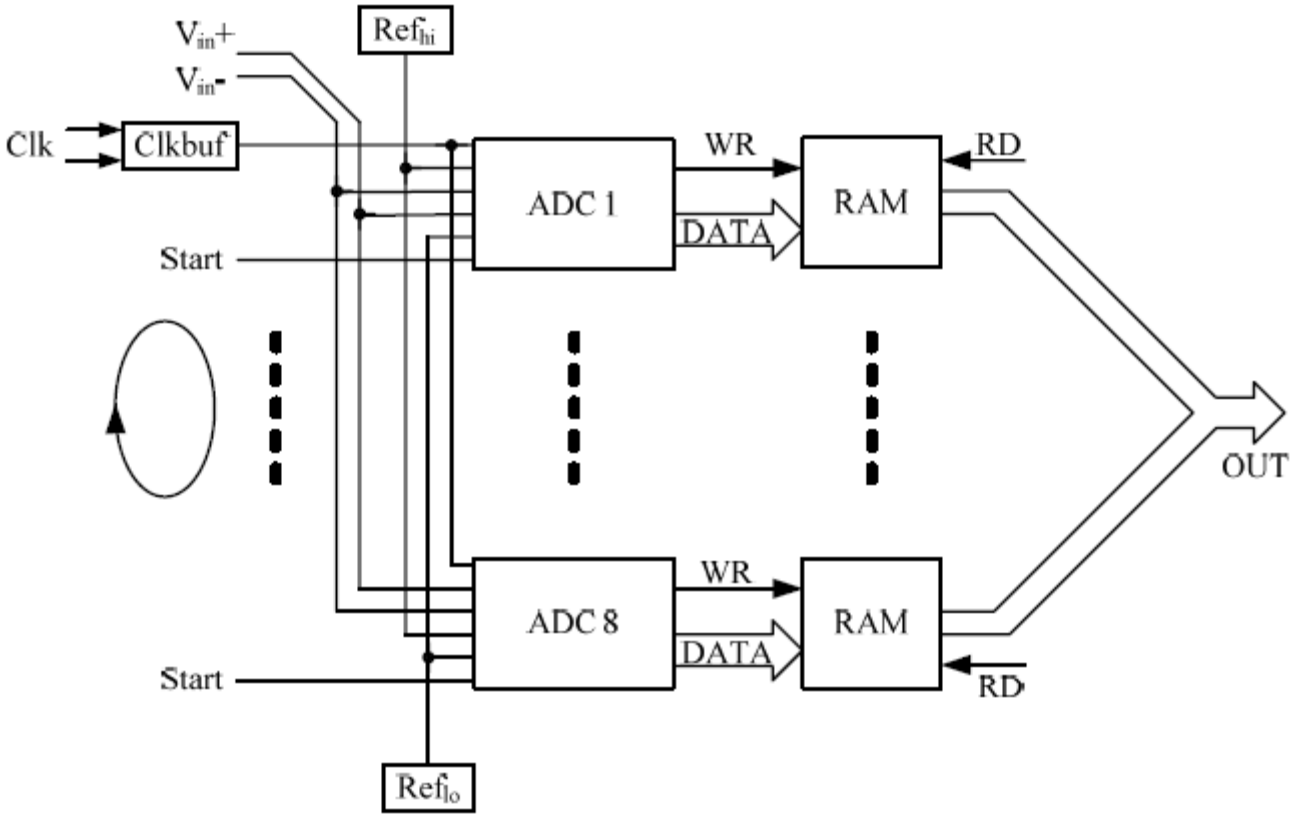
SAR ADC


Binary weighted Capacitor array
Comparator
C
C/2
C/4
C/8
C/16
C/16
+
−
Vin
Vref

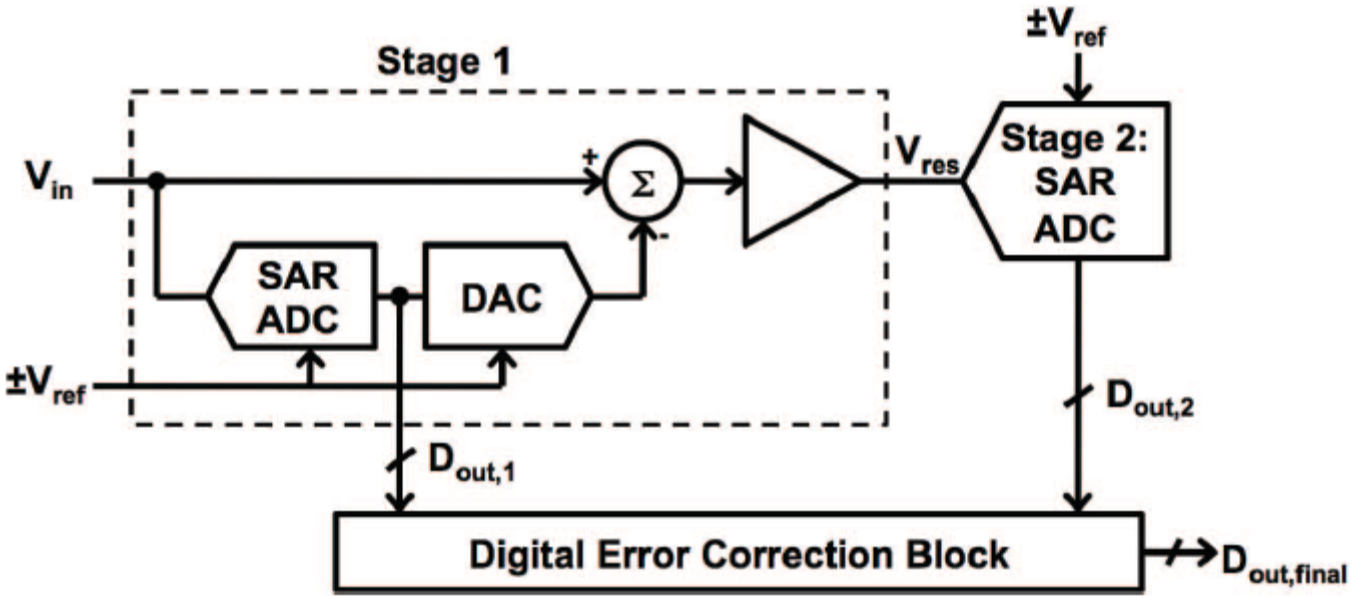
Asynchronous SAR ADC



Time-interleaved SAR ADC

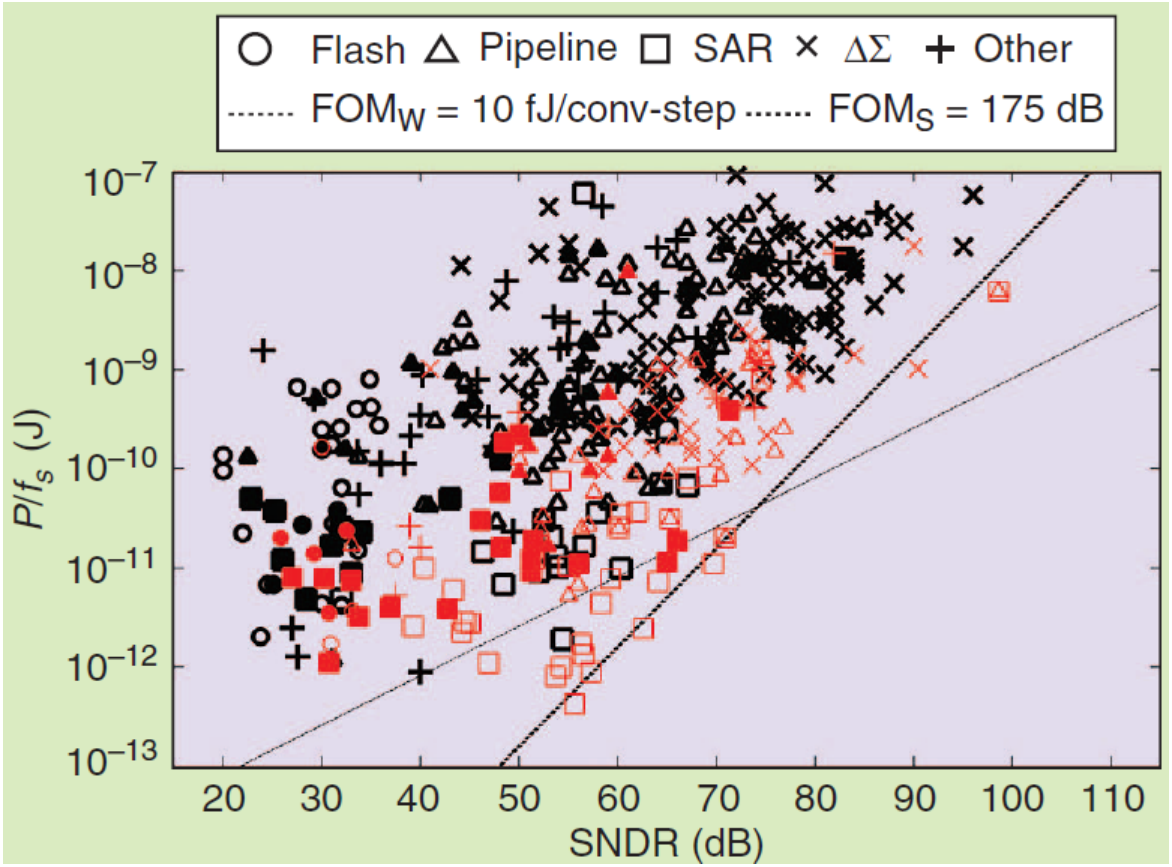


SAR-Assisted Pipelined ADC

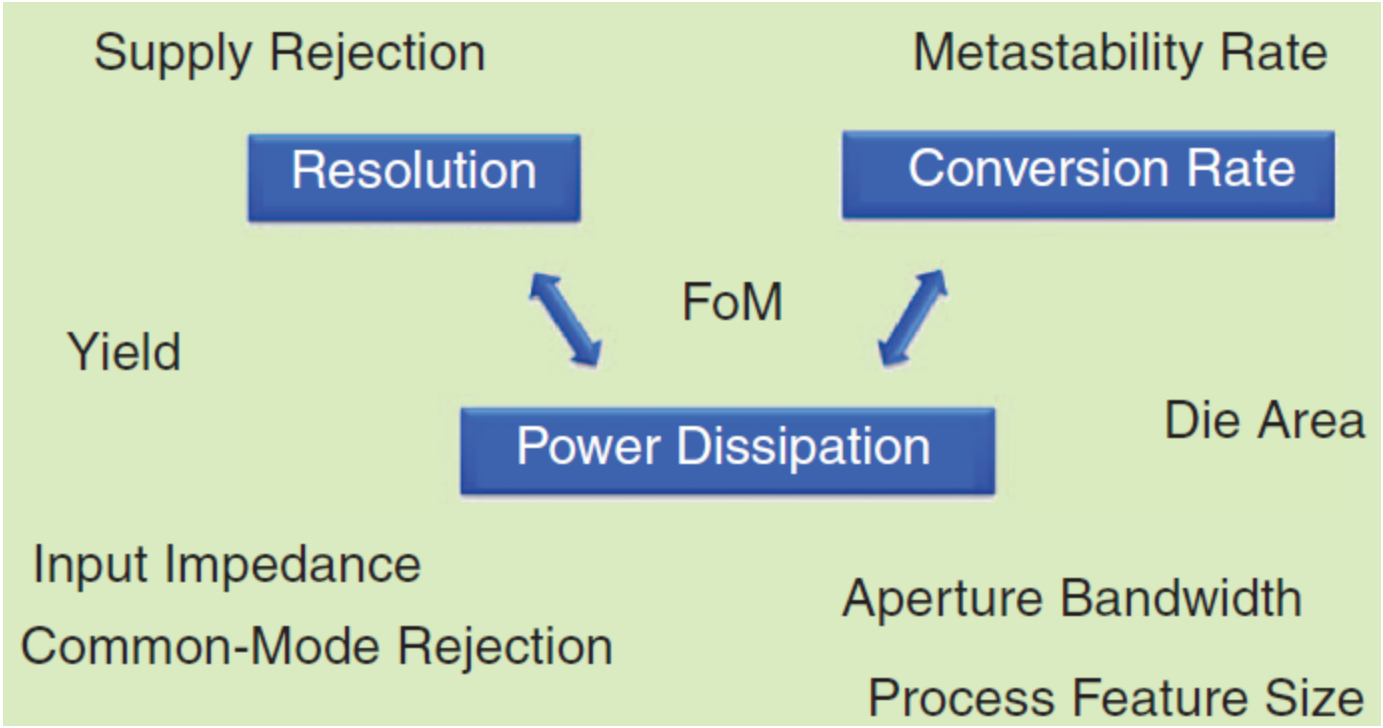


ADC Conversion Energy vs SNDR

From "Boris Murmann, The race for the extra decibel, IEEE Solid-State Circuits Magazine, Summer 2015
ISSCC 1997-2015 and VLSI Ciruits Symposium 1997-2014
The red markers indicate data reported after 2010.
Points with solid fill mark time-interleaved designs.

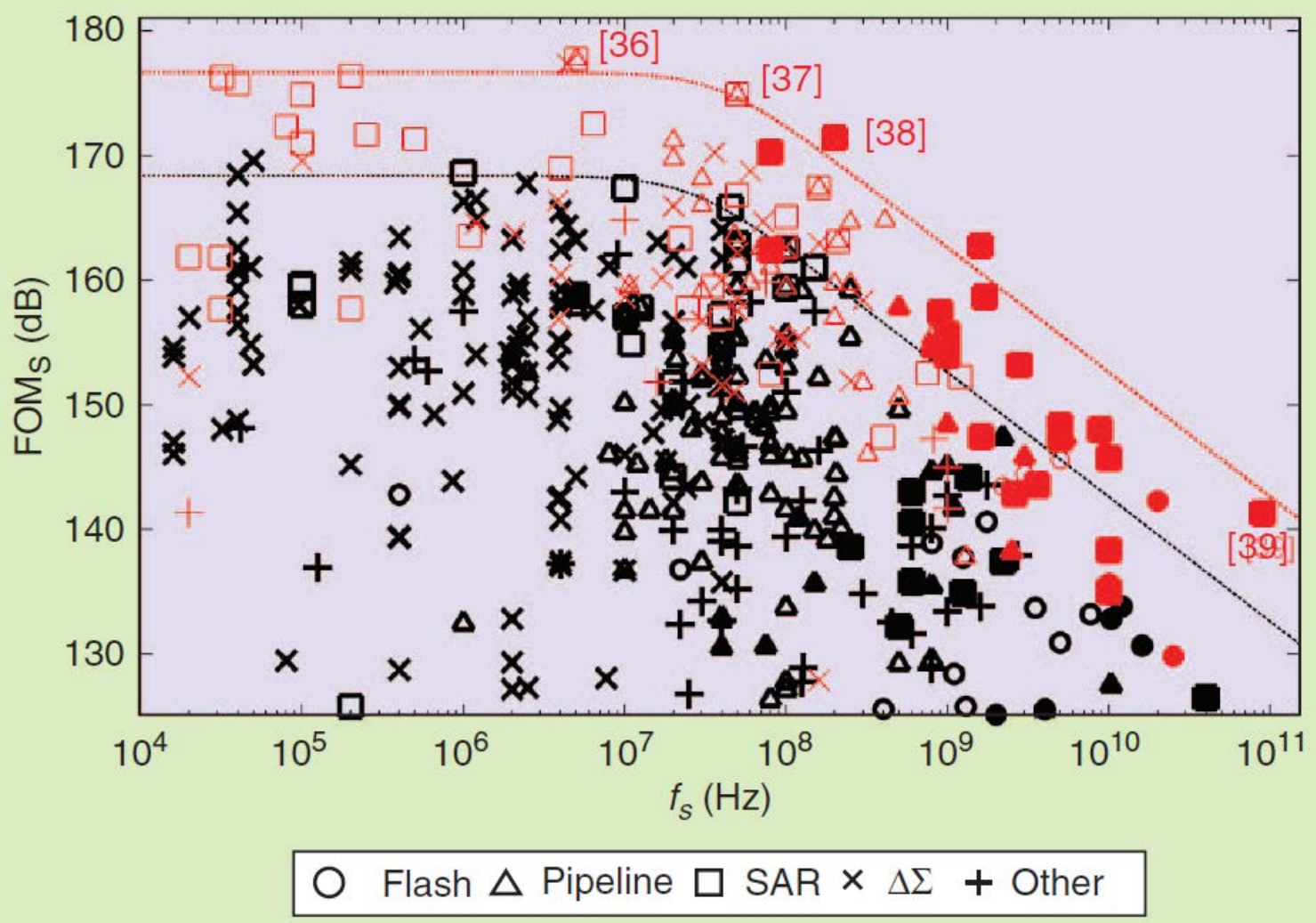


ADC Figure of Merit

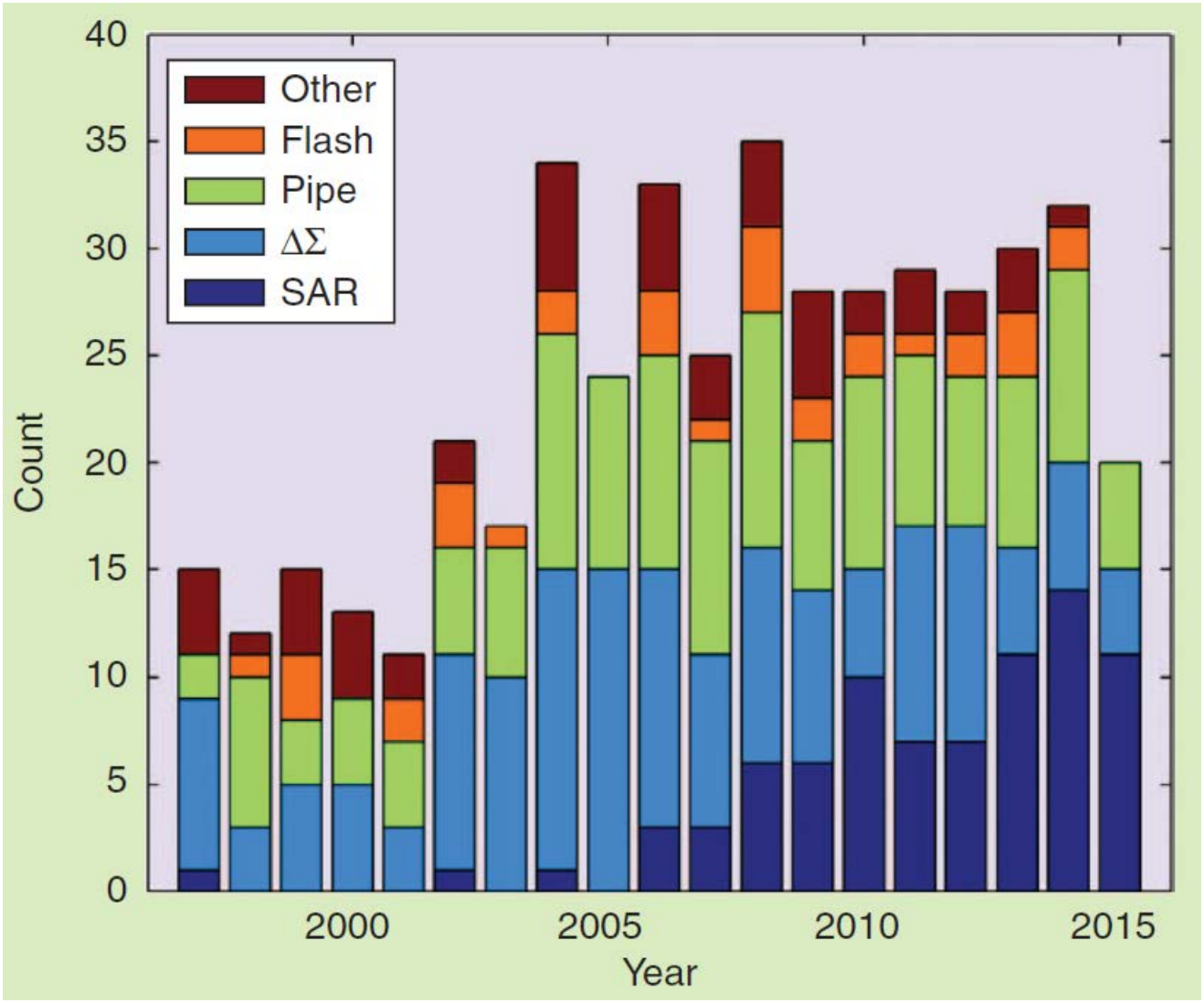


WALDEN FoM [1]	SCHREIER FoM (DR) [22]	SCHREIER FoM (SNDR) [23]
$\mathrm{FoM_W} = \frac{P}{f_s \cdot 2^{\mathrm{ENOB}}}$ $\mathrm{ENOB} = \frac{\mathrm{SNDR\,(dB)} - 1.76}{6.02}$	$\mathrm{FoM}_{s,\mathrm{DR}} = \mathrm{DR\,(dB)} + 10\log\left(\frac{BW}{P}\right)$	$\mathrm{FoM_S} = \mathrm{SNDR\,(dB)} + 10\log\left(\frac{f_s/2}{P}\right)$

FoM_S vs Conversion Rate



ADC Architecture Trends



Time-interleaved ADC papers