EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 11: Bootstrapped Clock Circuits
Comparator

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ENG-259

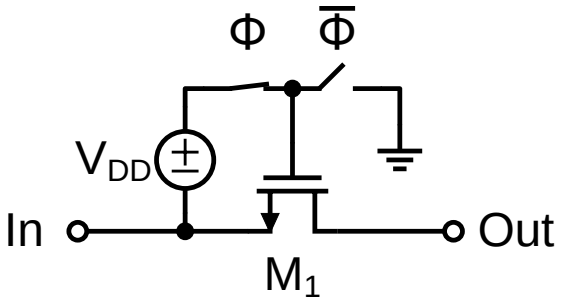
Course Schedule – Subject to Change

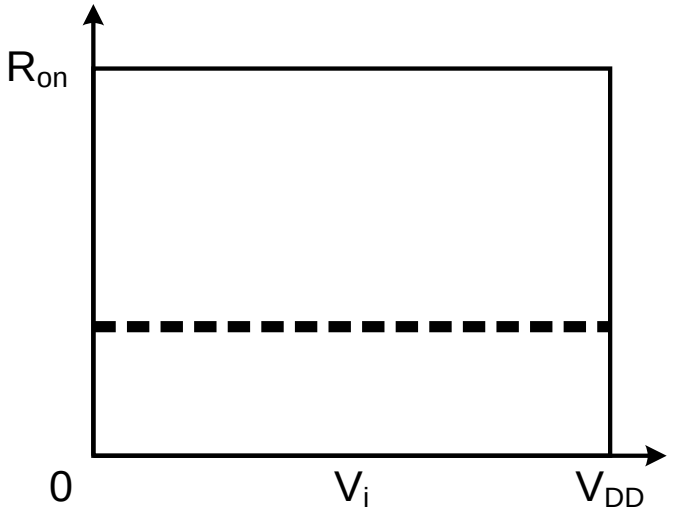
Date	Topics
24-Jan	Course introduction and ADC architectures
29-Jan	Converter basics: AAF, Sampling, Quantization, Reconstruction
31-Jan	ADC dynamic performance metrics, Spectrum analysis using FFT
5-Feb	ADC & DAC static performance metrics, INL and DNL
7-Feb	OPAMP and bias circuits review
12-Feb	SC circuits review
14-Feb	Sample and Hold Amplifier - Reading materials
19-Feb	Flash ADC and Comparators: Regenerative Latch
21-Feb	Comparators: Latch offset, preamp, auto-zero
26-Feb	~~Finish Flash ADC~~
28-Feb	DAC Architectures - Resistor, R-2R
5-Mar	DAC Architectures - Current steering, Segmented
7-Mar	DAC Architectures - Capacitor-based
12-Mar	SAR ADC with bottom plate sampling
14-Mar	SAR ADC with top plate sampling
19-Mar	Midterm Review
21-Mar	Midterm exam
26-Mar	Spring break
28-Mar	Spring break
2-Apr	Pipelined ADC stage - comparator, MDAC, x2 gain
4-Apr	Pipelined ADC bit sync and alignment using Full adders
9-Apr	Pipelined ADC 1.5bit vs multi-bit structures
11-Apr	Fully-differential OPAMP and Switched-capacitor CMFB
16-Apr	Single-slope ADC
18-Apr	Oversampling & Delta-Sigma ADCs
23-Apr	Second- and higher-order Delta-Sigma Modulator.
25-Apr	Hybrid ADC - Pipelined SAR
30-Apr	Hybrid ADC - Time-Interleaving
2-May	ADC testing and FoM
7-May	Project presentation 1
8-May	Project presentation 2
14-May	Final Review
20-May	Project Report Due by 6 PM

Bootstrap circuits
Comparator

***Midterm Exam dates are approximate and subject to change with reasonable notice.**

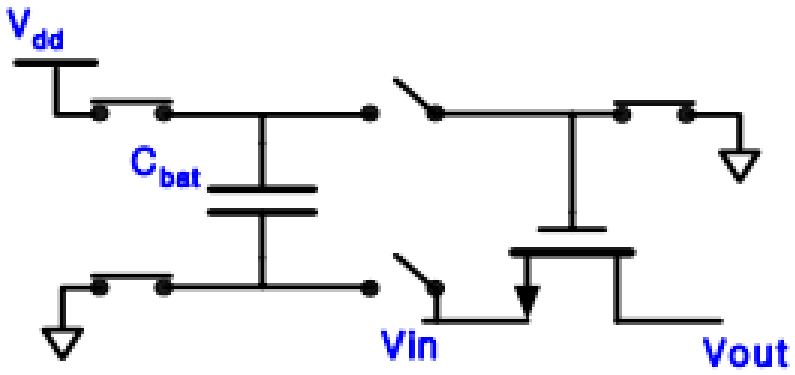
Clock Bootstrapping



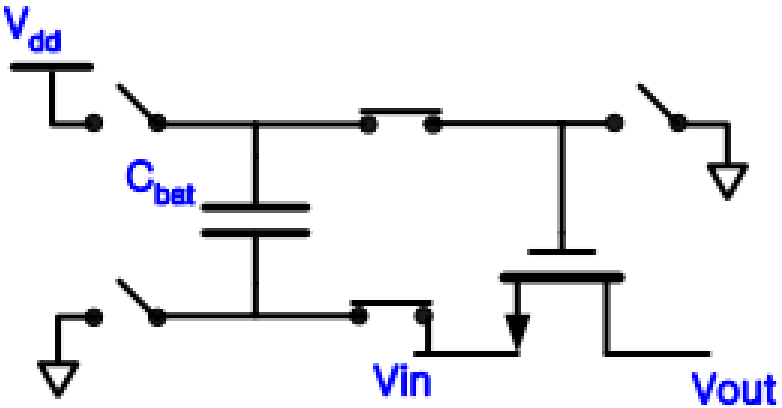


- Constant gate overdrive voltage $V_{GS} = V_{DD}$ for the switch
- R_{on} is not dependent on V_{in} to the first order (body effect?)
- NMOS device only with less parasitic capacitance

Clock Bootstrapping



(a)

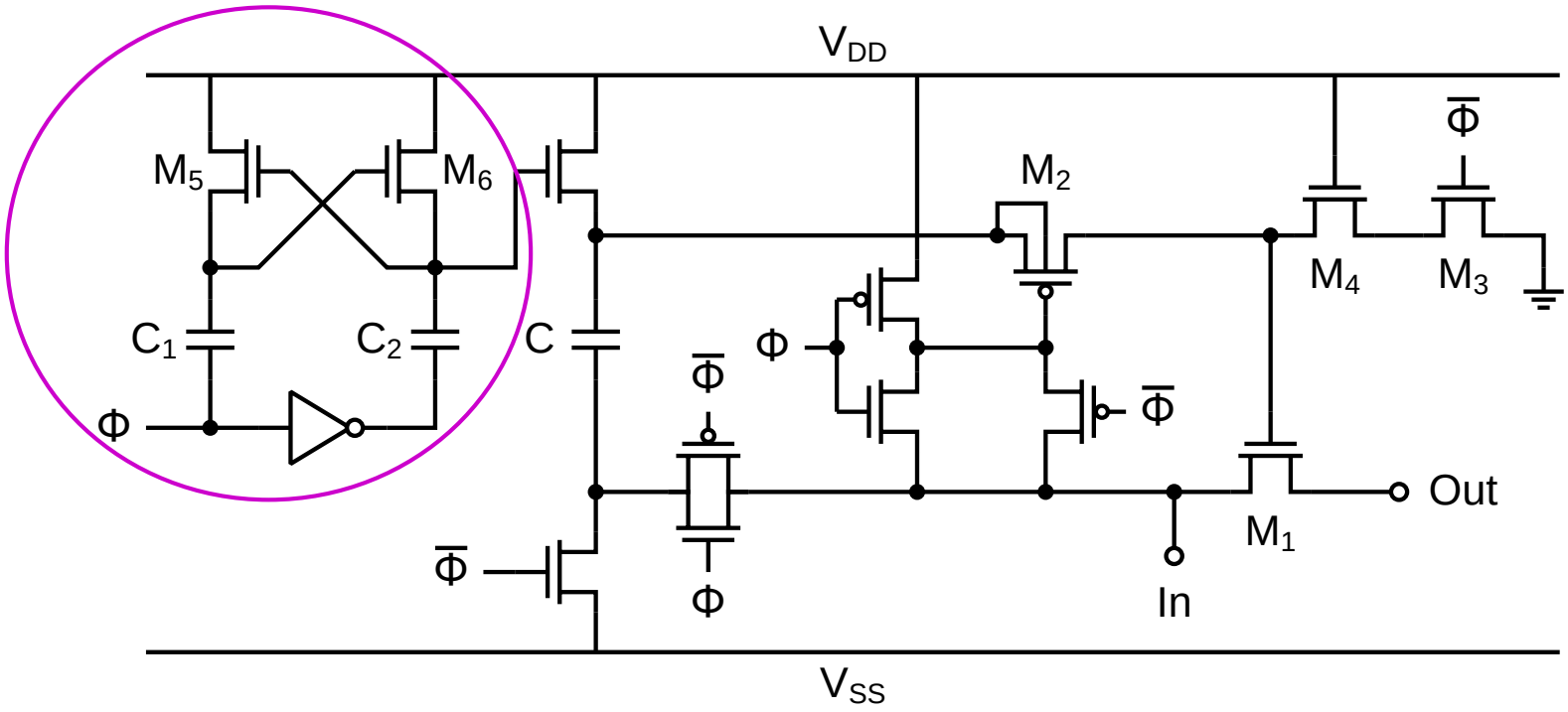


(b)

Clock Bootstrapping

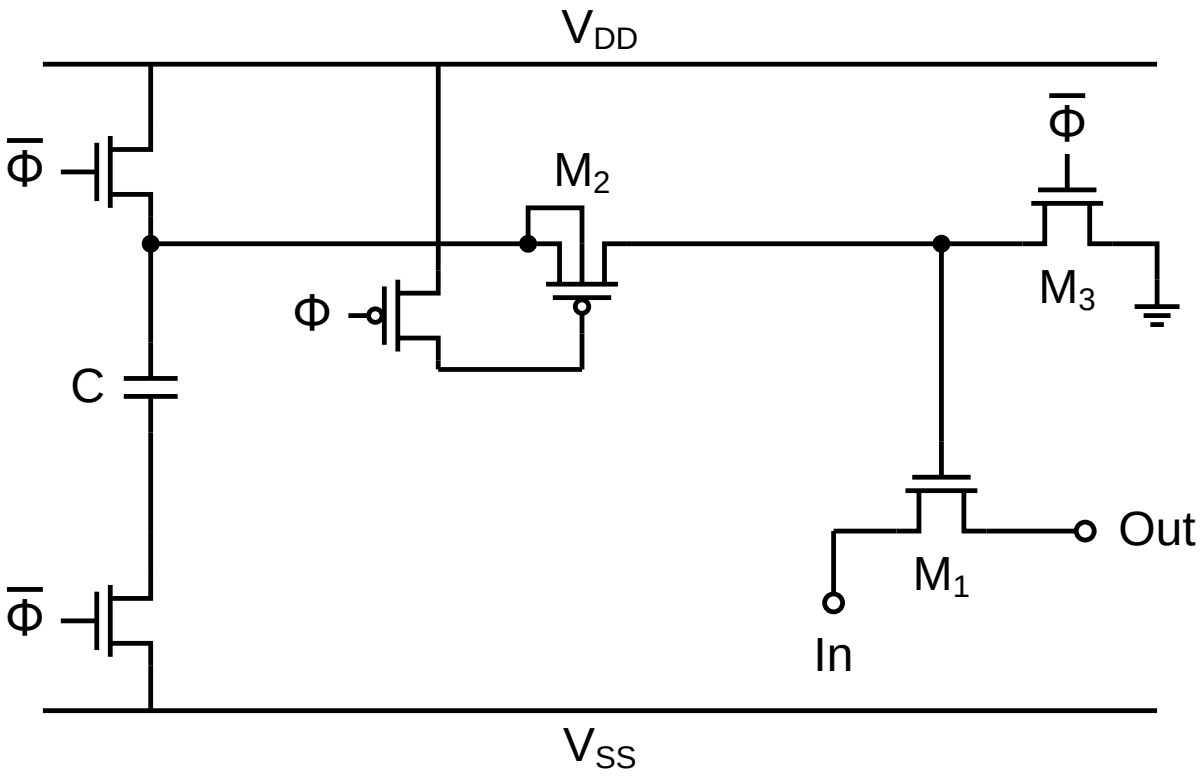
Nakagome Charge Pump

Y. Nakagome et al., “An experimental 1.5 V 64 Mb dram,”
IEEE J. Solid-State Circuits, vol. 26, pp. 465–472, Apr. 1991

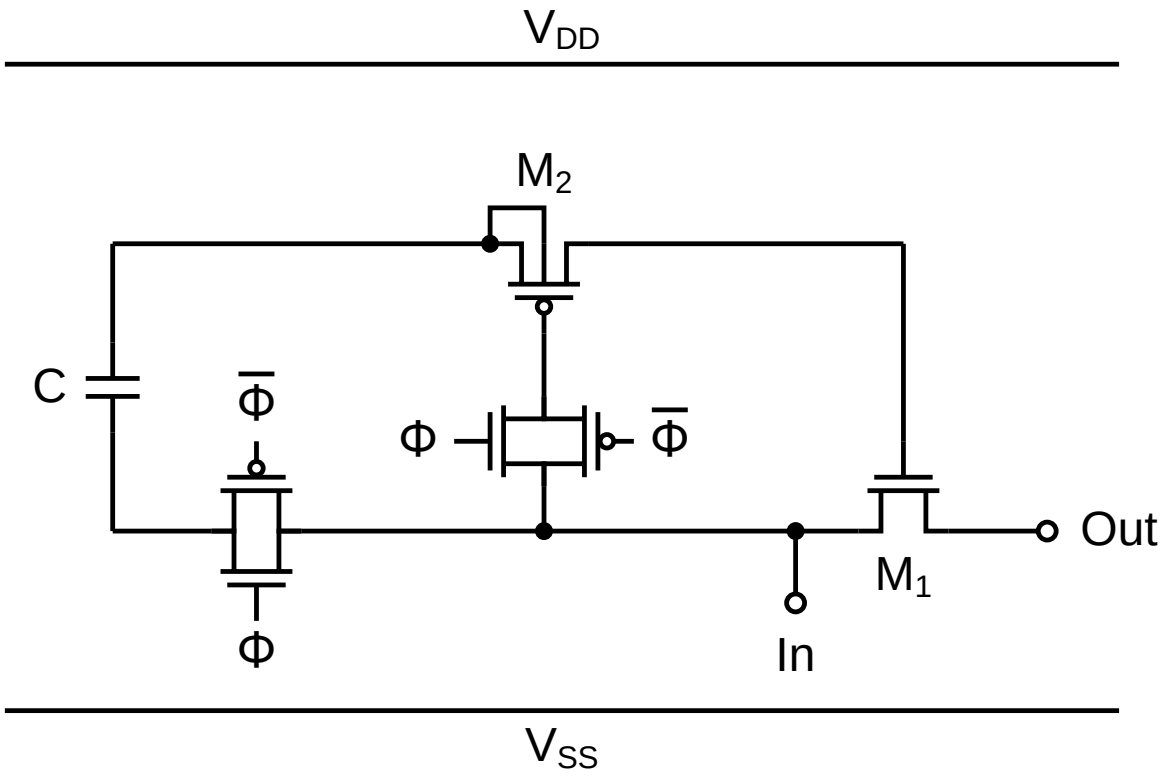


Ref: A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline ADC,”
IEEE Journal of Solid-State Circuits, vol. 34, issue 5, pp. 599-606, 1999.

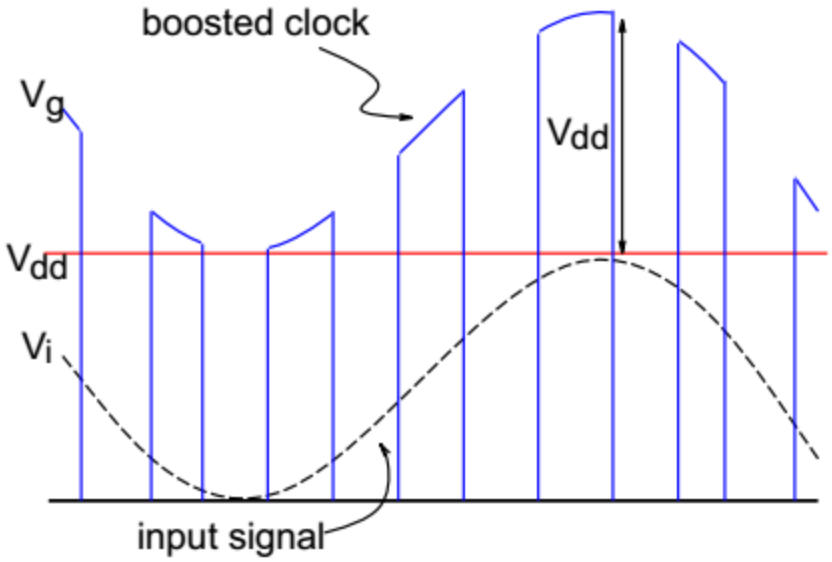
Clock Bootstrapping (Φ=0)



Clock Bootstrapping (Φ=1)

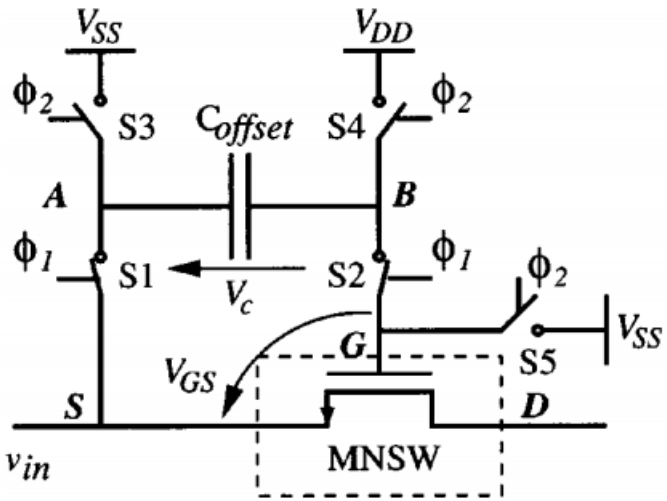


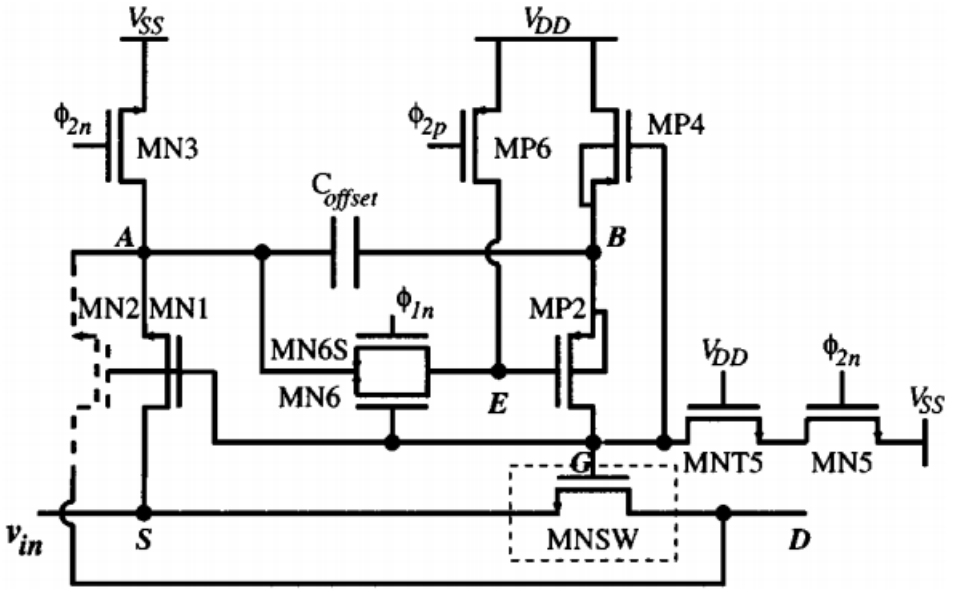
Clock Bootstrapping



Another Clock Bootstrap Circuit

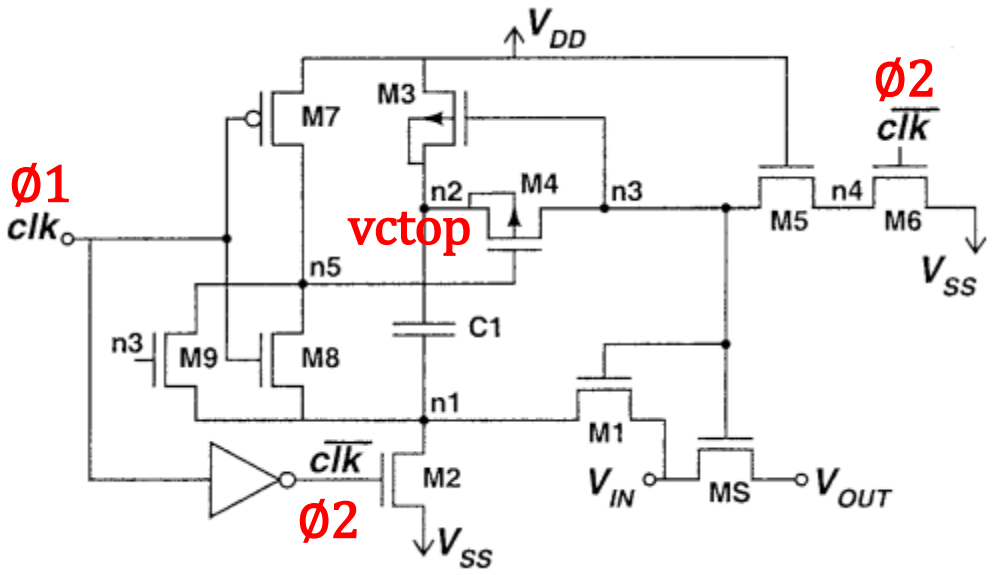
Mohamed Dessouky and Andreas Kaiser, “Very Low-Voltage Digital-Audio ΔΣ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping,”
IEEE J. Solid-State Circuits, vol. 36, pp. 349–355, Mar. 2001



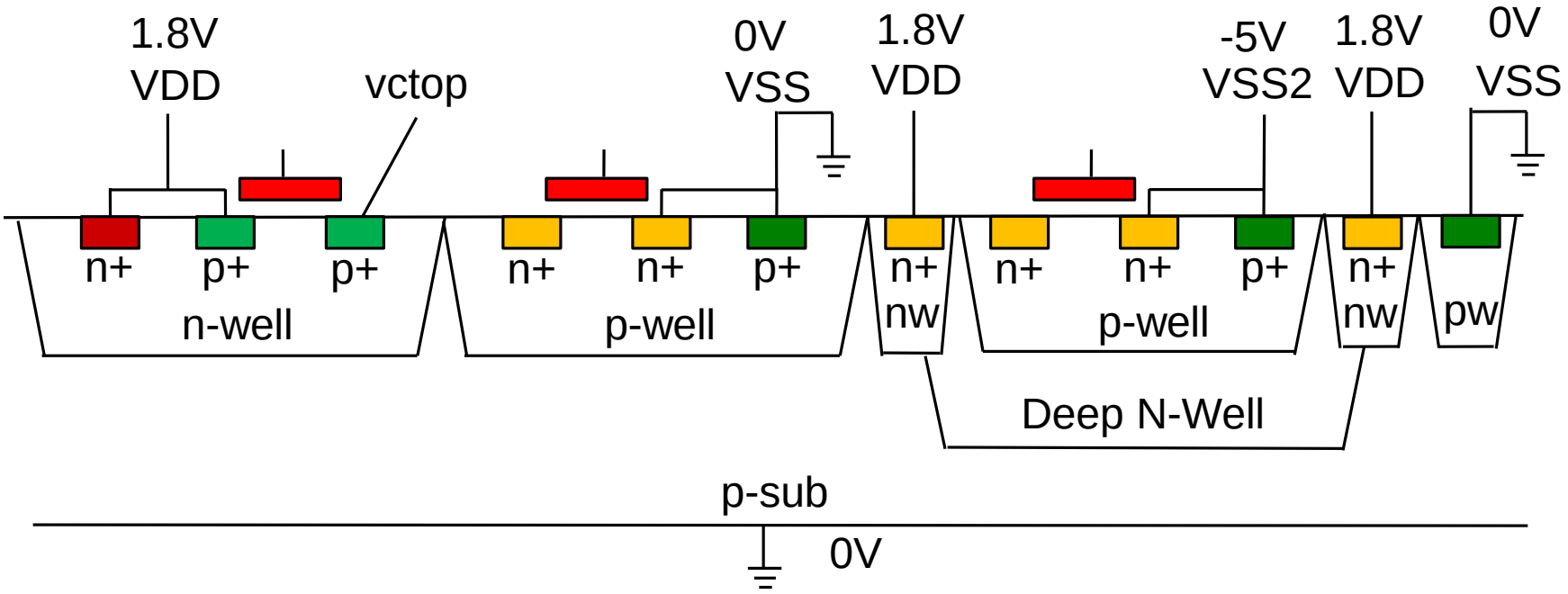


Another Clock Bootstrap Circuit

M. Waltari, et.al., “A Self-Calibrated Pipeline ADC with 200 MHz IF-Sampling Frontend,” *Analog Integrated Circuits and Signal Processing*, vol. 37, pp. 201–213, 2003

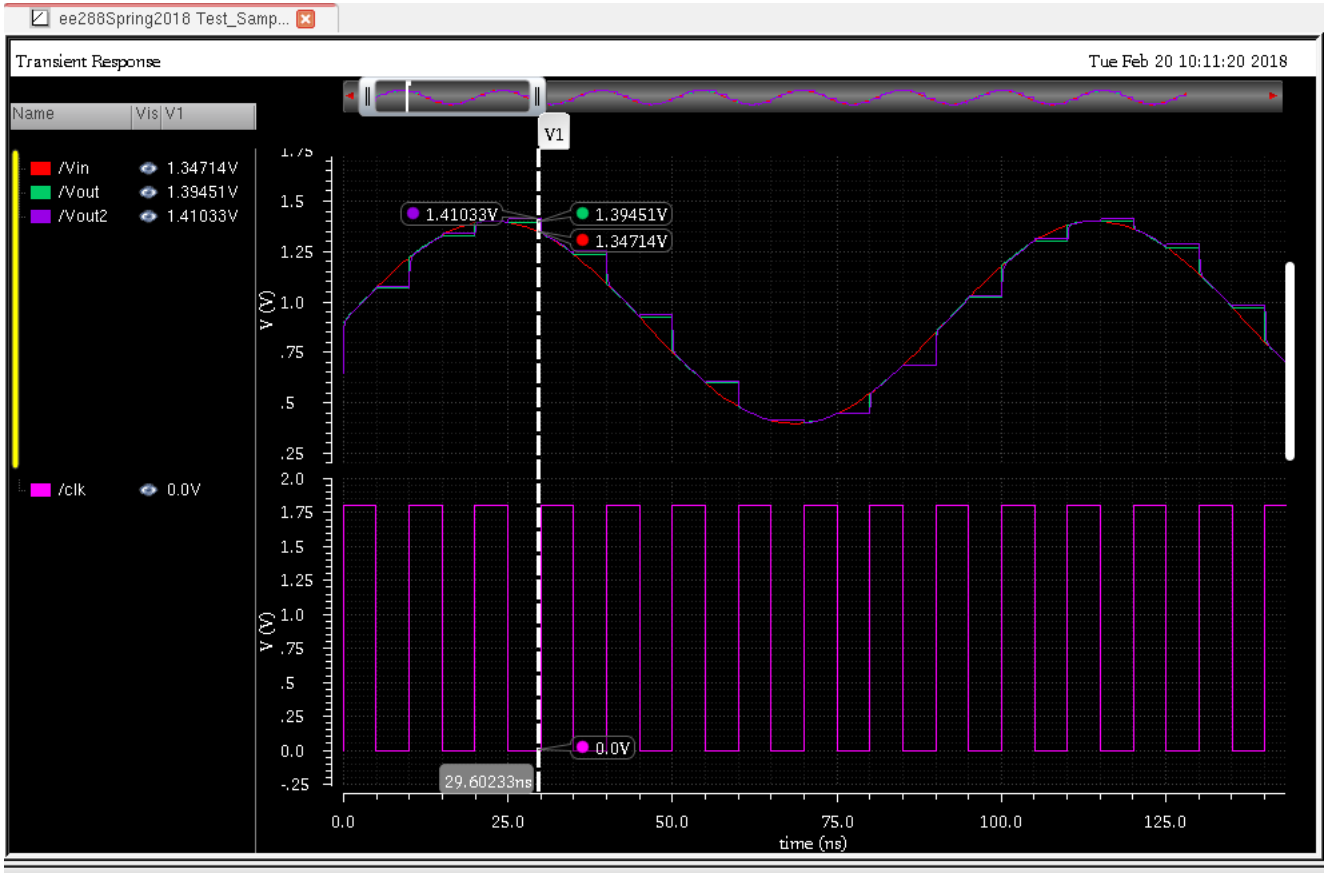


Cross-section of MOS Transistors

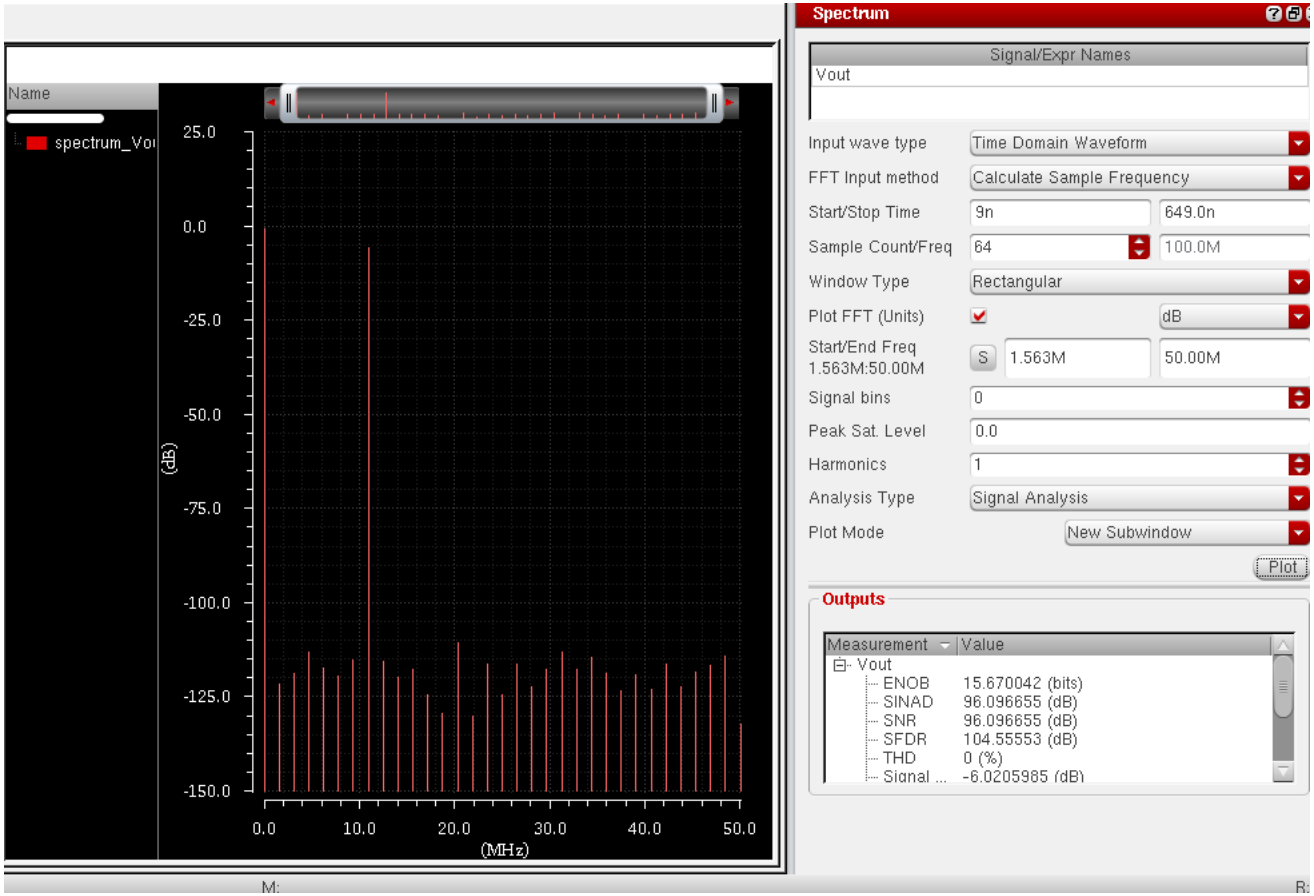


All pn junctions must be reverse-biased at all times.
If vctop > VDD, the n-well tab should be connected to vctop.

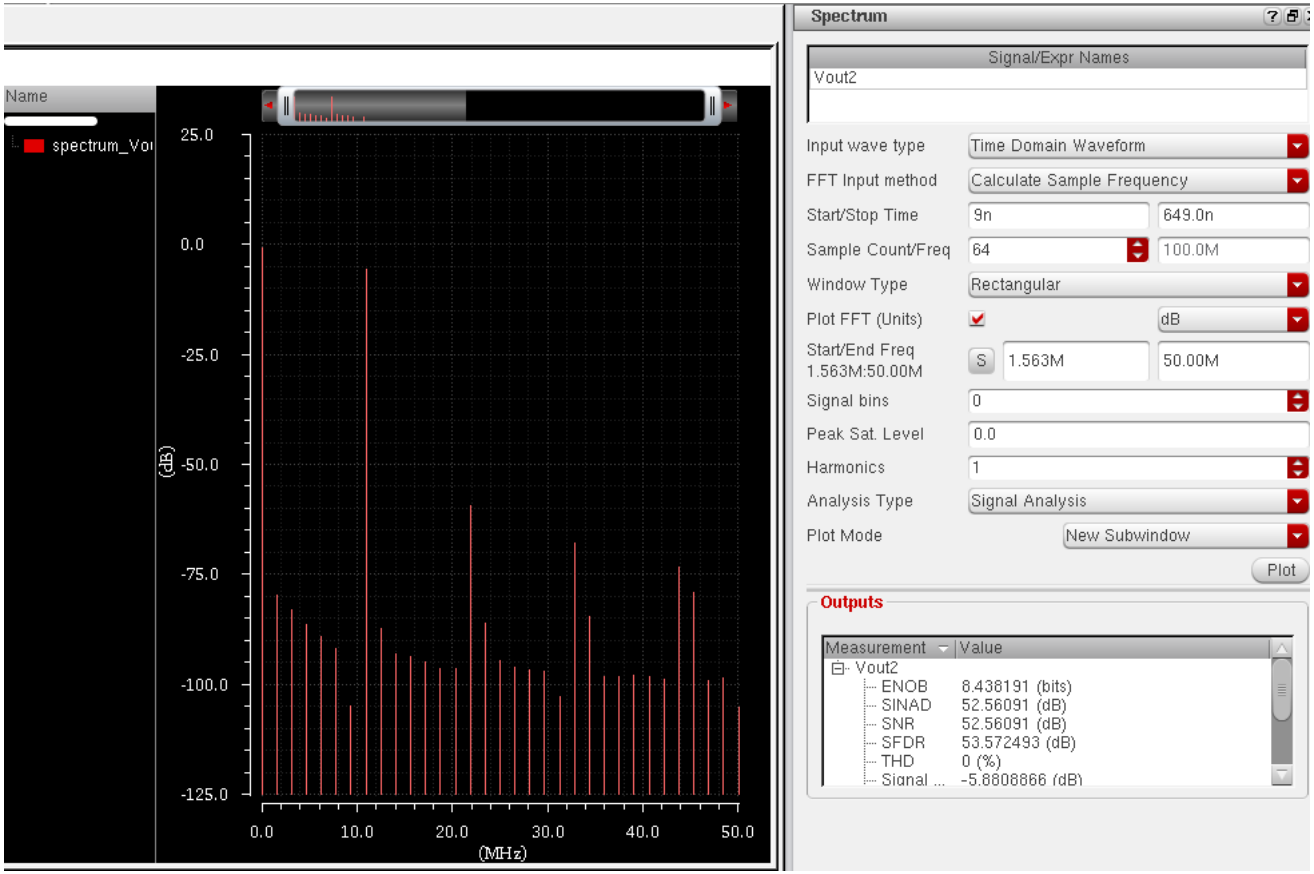
Test_Sample_Hold



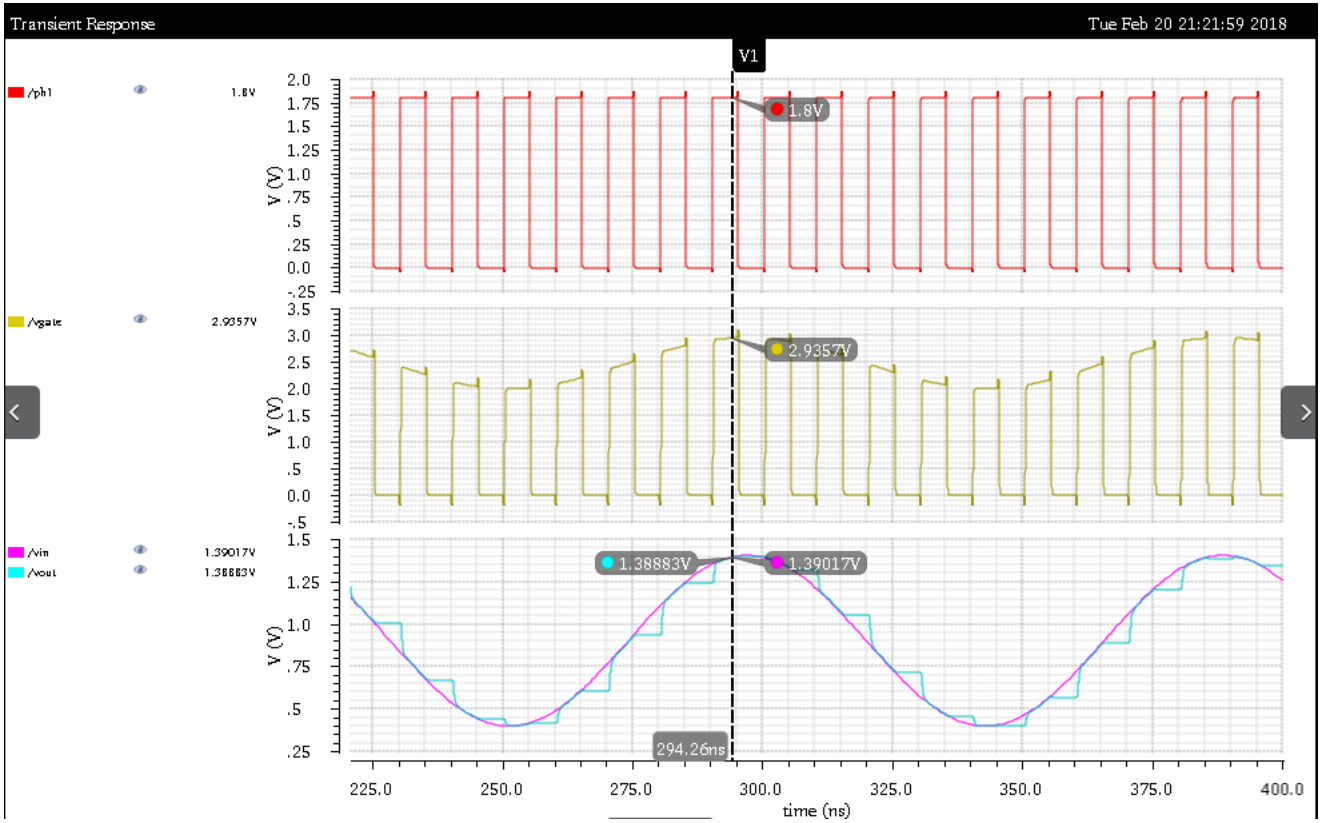
Ideal Switch Spectrum



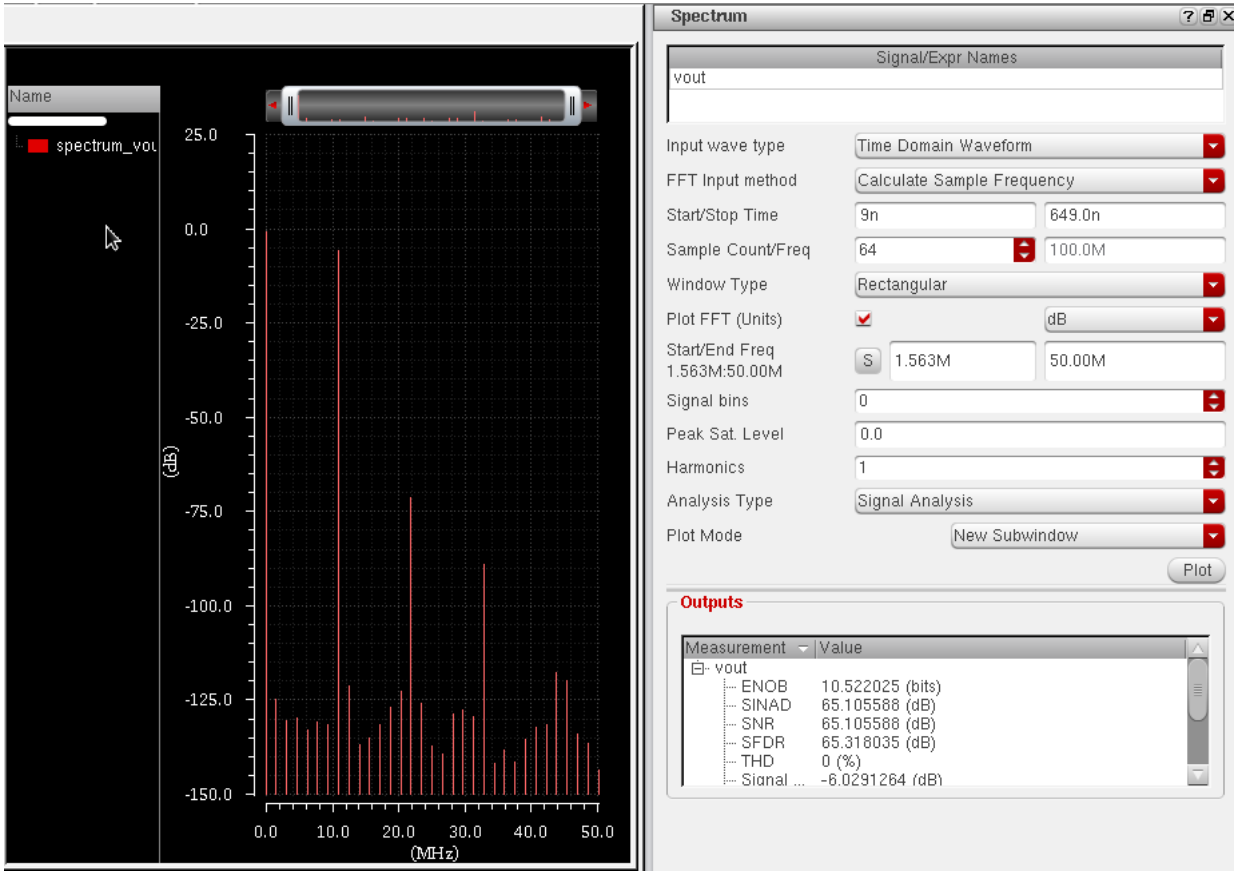
CMOS TG Spectrum



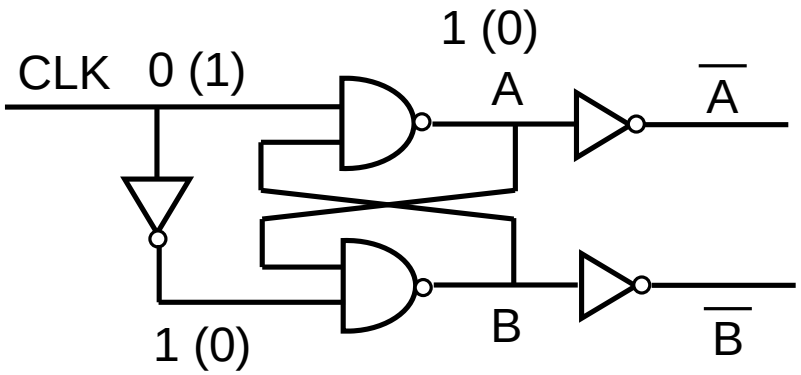
bootstrap_tb

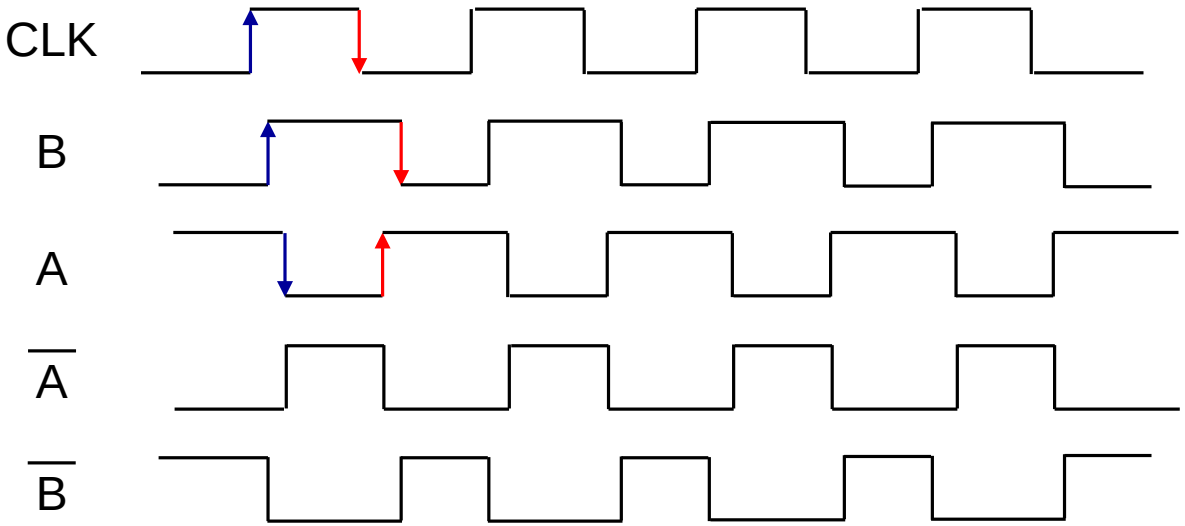


Spectrum of Bootstrap Switch

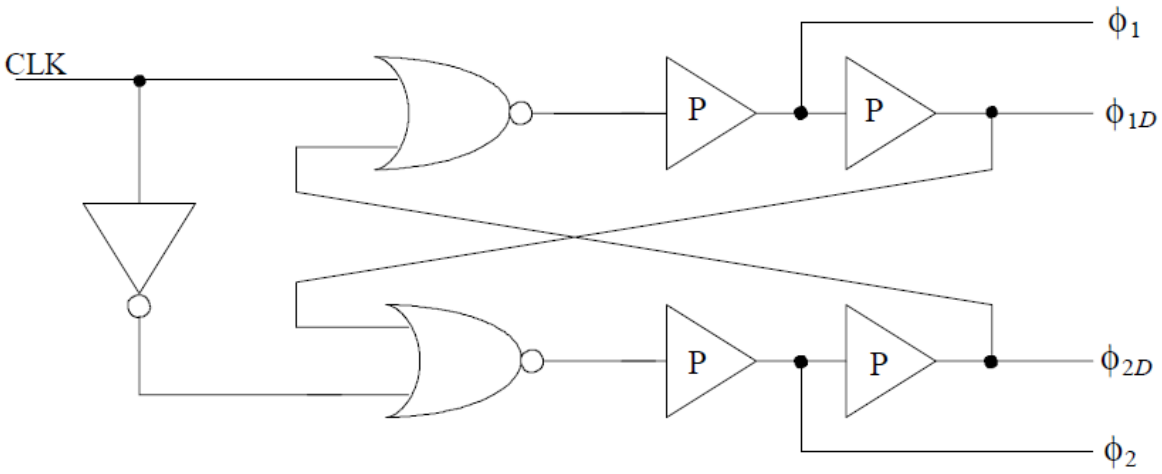


Non-overlapping clock

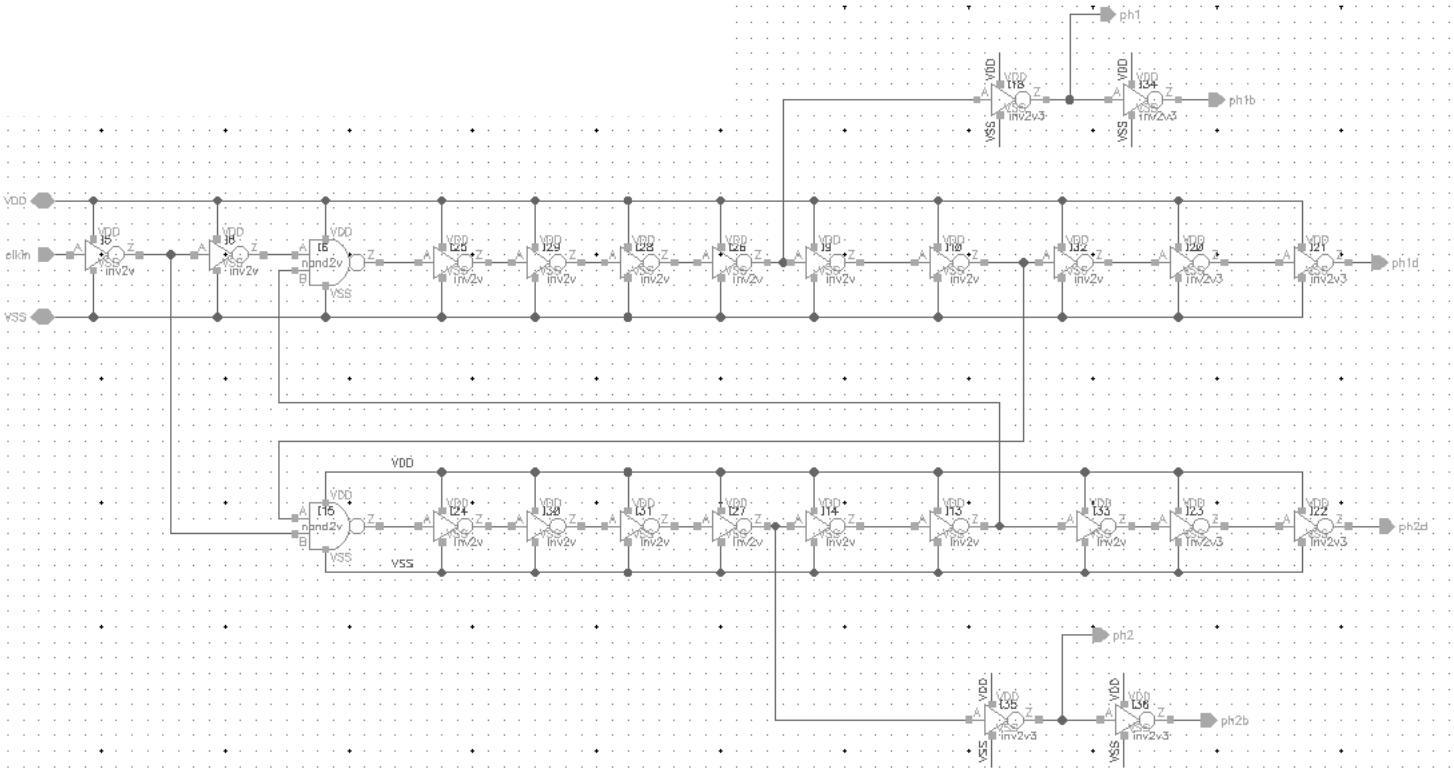




Non-overlapping clock

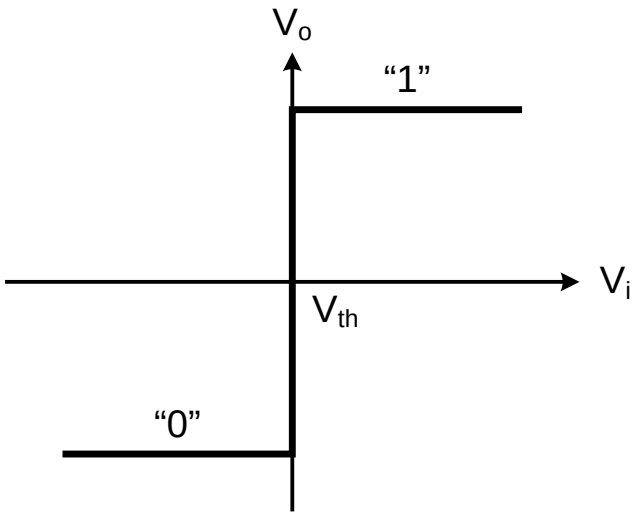


2phase_clk

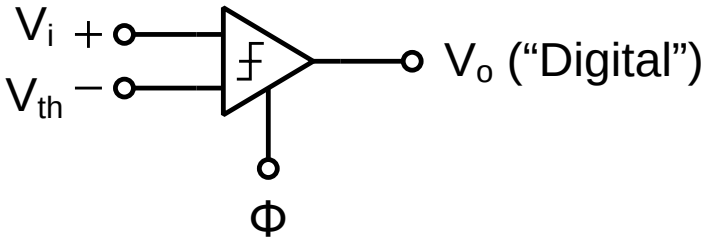

VDD
clkin
VSS
ph1
ph1b
ph1d
ph2
ph2b
ph2d
inv2v
inv2v3
nand2v

Comparator

Comparator Definition



Transfer characteristic (ideal)



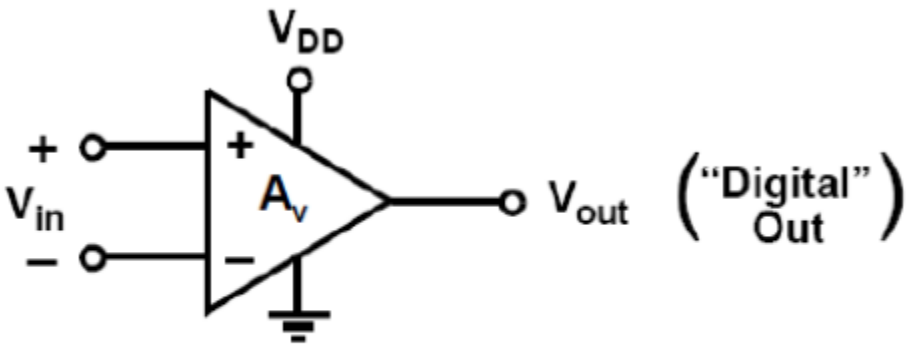
Circuit symbol

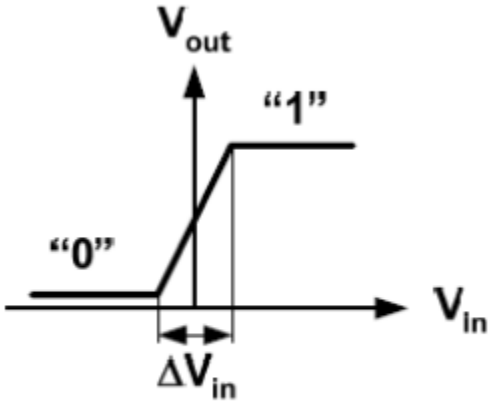
Detects the polarity of the analog input signal and produces a digital output (1 or 0) accordingly – threshold-crossing detector

Design Considerations

- Accuracy
  - Gain (resolution)
  - Offset
- Speed
  - Small-signal bandwidth
  - Settling time or delay time, slew rate
  - Overdrive recovery
- Power dissipation
- Input properties
  - Sampled data versus continuous time
  - Common-mode rejection
  - Input capacitance and linearity of input capacitance
  - Kickback noise

Gain Requirement





For 10-bit ADC, VDD=1.8V, FS=1V, LSB=1V/1024≈1mV

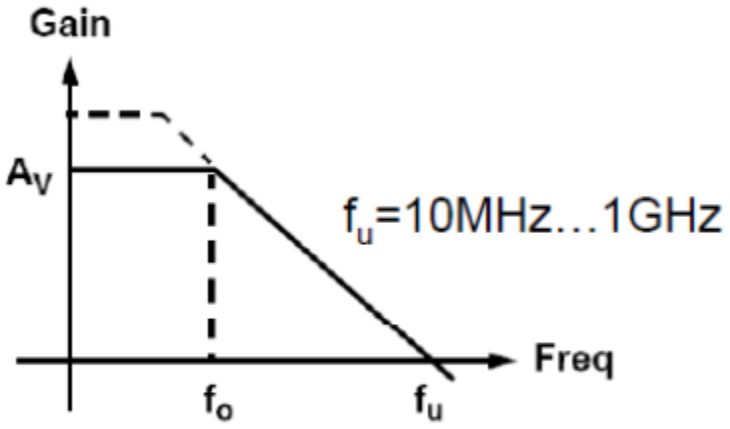
For ½ LSB precision, we need

$$A_v = \frac{1.8V}{0.5 \cdot 1mV} \approx 3686 = 71\text{dB}$$

Implementation Options

- Considerations
  - Amplification need not be linear
  - Amplification need not be continuous in time, if comparator is used in a sampled data system
    - Clock signal will tell comparator when to make a decision
- Implementation options to be looked at
  - Single stage amplification
    - E.g. OTA or OpAmp in open loop configuration
  - Multi-stage amplification
    - E.g. cascade of resistively loaded differential pairs
  - Regenerative latch using positive feedback
    - E.g. cross coupled inverters

Using an OPAMP or OTA

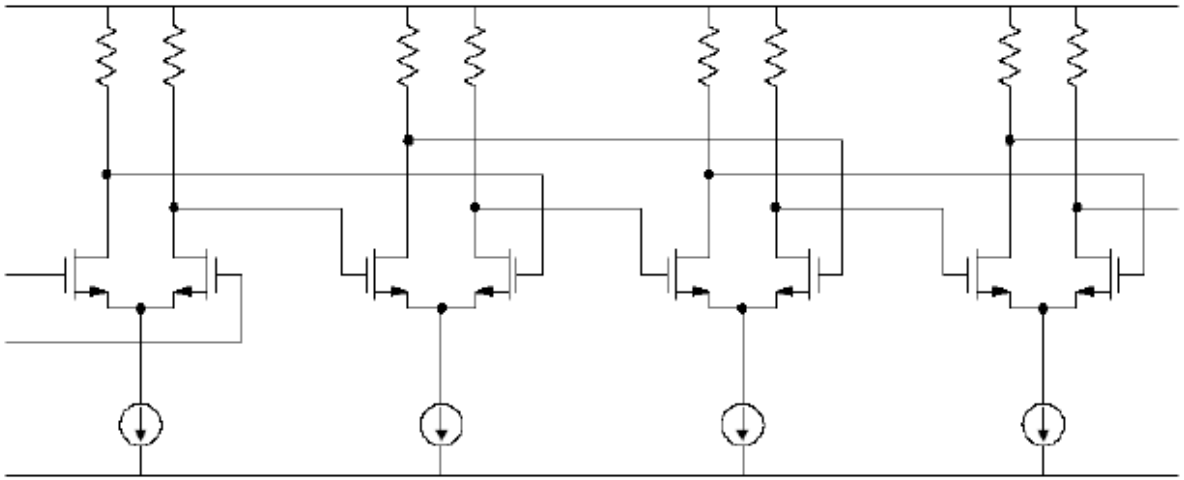


f_u = unity gain frequency, f_o = – 3dB frequency

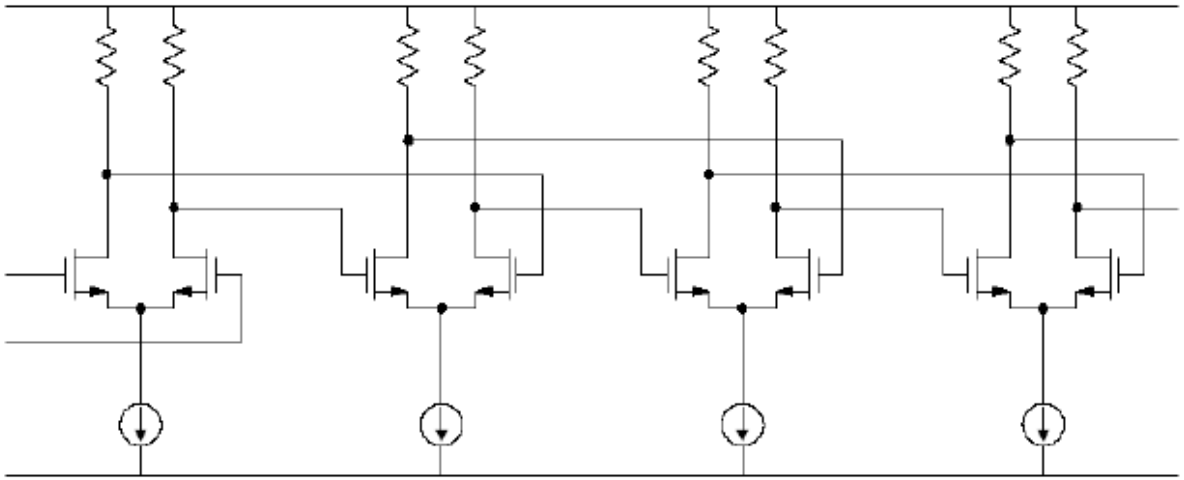
$$f_0 = \frac{f_u}{A_v} = \frac{1GHz}{3686} = 271kHz$$

$$\tau_0 = \frac{1}{2\pi f_0} = 0.59\mu S \longrightarrow \textbf{Too slow!}$$

Cascade of Open Loop Amplifiers



Cascade of Open Loop Amplifiers



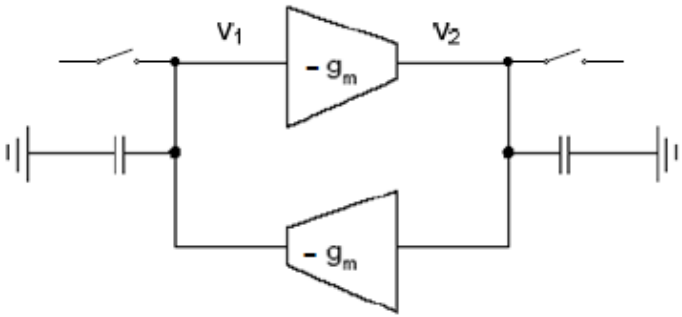
In each stage: $\omega_u = \frac{g_m}{C_{gs}} \cong \text{const.}$ $A_0 = g_m R = \frac{\omega_u}{\omega_0}$ $\omega_0 = \frac{1}{RC} = \frac{\omega_u}{A_0}$

- Possible choices for a given, constant overall gain objective
  - Lots of stages with low gain
  - Only a few stages with moderate gain

Regenerative Latch

$t < 0$ setup initial condition $v_{10} - v_{20} = v_{d0}$

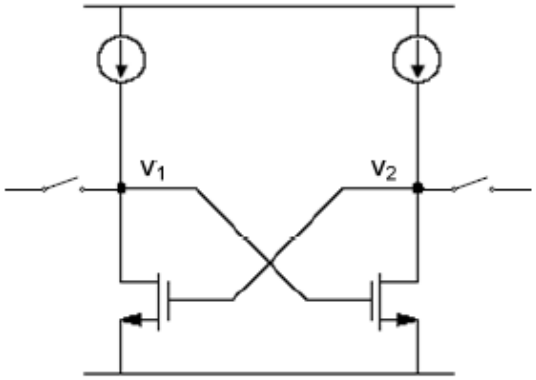
$t \geq 0$ enable positive feedback



$$\frac{dv_1}{dt} = \frac{i_1(t)}{C} = \frac{-g_m v_2(t)}{C}$$

$$\frac{dv_2}{dt} = \frac{i_2(t)}{C} = \frac{-g_m v_1(t)}{C}$$

$$\tau_u = \frac{C}{g_m}$$



$$\Rightarrow v_1(t) - v_2(t) = v_d(t) = v_{d0} \cdot e^{t/\tau_u}$$

$$\Rightarrow A(t) = \frac{v_d(t)}{v_{d0}} = e^{t/\tau_u}$$

Latch Gain

$A(\tau_d)$	τ_d/τ_u
10	2.3
100	4.6
1,000	6.9
10,000	9.2

For 10-bit, you need about 7τ