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6:00-7:30pm

EECS 141: FALL 2002—MIDTERM 1

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

NMOS:

$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$

PMOS:

$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last **SOLUTION** First

GRAD/UNDERGRAD	

Problem 1: __12_/ 12

Problem 2: __20_/ 20

Problem 3: __10_/ 10

Total: __42_/ 42

PROBLEM 1. (10 pts) MOS transistor as a switch

a) (4 pts) Find the final value of the voltage V_o, as a response to a LH transition at the input as shown in Figures 1.a – 1.d. Assume $V_{TN} = |V_{TP}| = 0.5V$. Assume that the capacitor is initially discharged, and ignore subthreshold conduction and body effect.

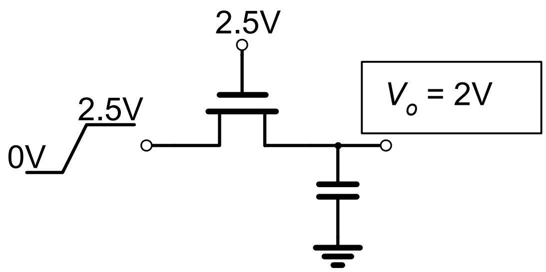

Figure 1.a.

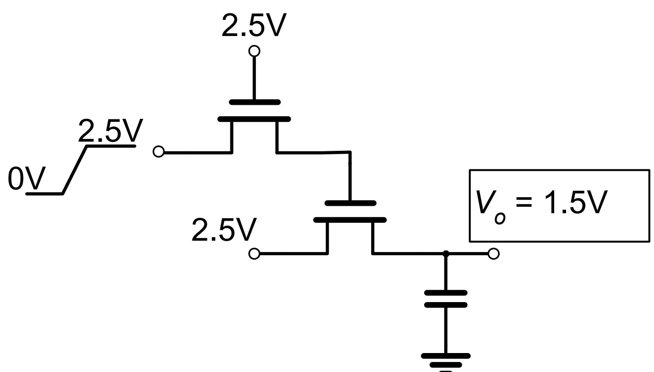

Figure 1.b.

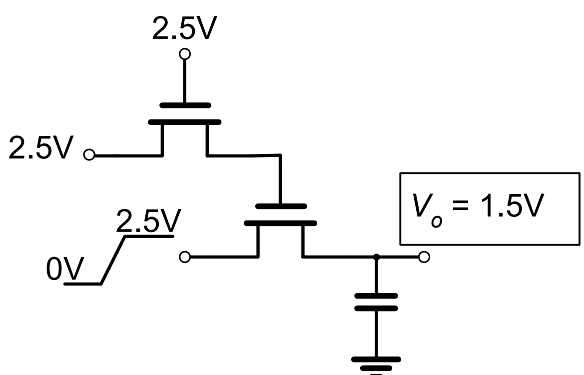

Figure 1.c.

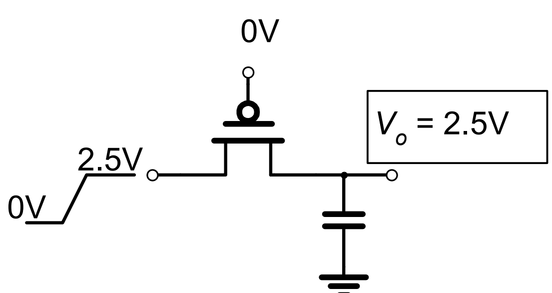

Figure 1.d.

b) (2pts) When the output reaches its final value, a 2.5V to 0 step is applied to the input. Determine the energy consumed in the transistors from Figure 1.c. during the transition (in symbolic terms).

$$E_{dis} = \frac{1}{2}C(V - 2V_T)^2$$

$$\boxed{E_{1\to 0} = \frac{1}{2}C(V - 2V_T)^2}$$

c) (6pts) For Figure 1.d, find the energy dissipated in the transistor during the first 0$\rightarrow$ 1 transition. Then, when the output reaches its final value, a 2.5V to 0 step is applied to the input, followed by the second 0 to 2.5V step. Find the energy dissipated in the transistor in the first 1 $\rightarrow$ 0 transition, and the second 0$\rightarrow$ 1 transition (in symbolic terms).

First $E_{0\rightarrow 1} = \frac{1}{2} C V^2$

First $E_{1\rightarrow 0} = \frac{1}{2} C\left(V^2 - V_T{}^2\right)$

Second $E_{0\rightarrow 1} = \frac{1}{2} C(V - V_T)^2$

PROBLEM 2. (20pts) Transistor sizing.

An inverter chain is shown in Figure 2. The first and the third inverter are supplied from V_{DD1} = 2.5V, while the second inverter is supplied from V_{DD2} = 1.5V. The input to the inverter chain swings between 0 and 2.5V. All transistors are minimum length, L = 0.25μm.

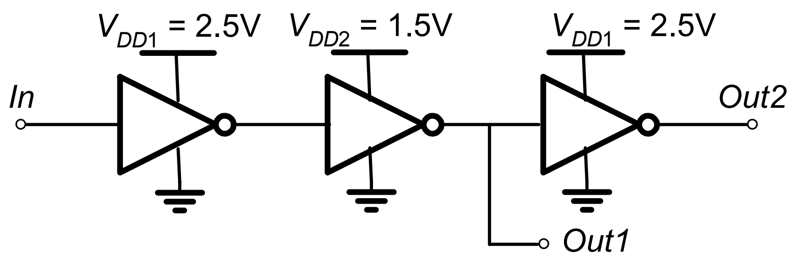

Figure 2.

Wn = 1μm	Wn = 1μm	Wn = 1μm
Wp = 2μm		Wp = 2μm

a) (8pts) If the width of the NMOS transistor in the second stage is Wn = 1μ, find the size of the PMOS transistor, such that the second inverter exhibits the same LH and HL propagation delays (output *Out1*).

The 50% point at the output of the second inverter is $V_{DD2}/2$ = 0.75V.
Need $R_{eqp} = R_{eqn}$.

$$R_{eqn} = \frac{3}{4}\frac{V_{DD2}}{k_n\frac{W_n}{L}\left[(V_{DD1}-V_{Tn})V_{DSATn}-\frac{V_{DSATn}^2}{2}\right]}$$

$$R_{eqp} = \frac{1}{2}\left(\frac{V_{DD2}}{I_D(V_{DD}2)}+\frac{V_{DD2}/2}{I_D(V_{DD2}/2)}\right)$$

$$R_{eqp} = \frac{1}{2}\left(\frac{V_{DD2}}{k_p\frac{W_p}{L}\left[\left(V_{DD2}-|V_{Tp}|\right)|V_{DSATp}|-\frac{V_{DSATp}^2}{2}\right]}+\frac{V_{DD2}/2}{k_p\frac{W_p}{L}\left[\left(V_{DD2}-|V_{Tp}|\right)\frac{V_{DD2}}{2}-\frac{V_{DD2}^2}{8}\right]}\right)$$

$$\boxed{W_p = 7.14\mu m}$$

b) (8pts) Determine the high and low output levels at the node *Out2*. Hint: You can make a reasonable assumption on the operating modes of transistors, but you have to prove that these assumptions are correct when you find the solution.

$V_{OH} = 2.5\text{V}$
V_{OL}: If output is low enough, PMOS is velocity saturated and NMOS is linear.
$|I_p| = I_n$

$$\frac{k_p}{2}\frac{Wp}{L}\left(V_{DD1} - V_{DD2} - |V_{Tp}|\right)^2 = k_n \frac{Wn}{L}\left[\left(V_{DD2} - V_{Tn}\right)V_{OL} - \frac{V_{OL}^{\ 2}}{2}\right]$$

$V_{OL} = 0.09\text{V}$

Check assumptions: PMOS V_{GS}, V_{DS}, V_{DSAT} – saturation, NMOS linear.

$V_{OH} = 2.5\text{V}$

$V_{OL} = 0.09\text{V}$

c) (4pts) How would you resize the third inverter to improve the noise margins?

Increase Wn, or decrease Wp/Wn ratio. This also decreases V_M.

3. CMOS Scaling (10pts)

A microprocessor consumes 0.3mW/MHz when fabricated using a 0.13 μm process. The area of the processor is 0.7 mm^2. Assume a 200 MHz clock frequency, and 1.2 V power supply. Its leakage power is 0.1mW. Assume short channel devices, but ignore second order effects like mobility degradation, series resistance, etc.

a) (5pts) If the supply voltage of the microprocessor scaled to 90 nm is reduced to 1.0 V, what will the area, frequency, power consumption, and power density be?

Full scaling, since voltage and gate length change by different factors. Referring to table 3.8 (page 119 of the reader) we get:

$$S = \frac{L_{old}}{L_{new}} = \frac{0.13}{0.09} = 1.444$$

$$U = \frac{V_{old}}{V_{new}} = \frac{1.2}{1.0} = 1.2$$

<u>Area:</u>

$$A_{new} = \frac{1}{S^2} A_{old} = \frac{0.7mm^2}{1.444^2} = 0.336mm^2$$

<u>Frequency:</u>

$$f_{new} = Sf_{old} = 1.444 \times 200MHz = 288.8MHz$$

<u>Power:</u>

$$P_{old} = (200MHz) \times 0.3mW / MHz = 60mW$$

$$P_{new} = \frac{1}{U^2} P_{old} = \frac{60mW}{1.2^2} = 41.67mW$$

<u>Power density:</u>

$$PD_{new} = \frac{P_{new}}{A_{new}} = \frac{41.67mW}{0.336mm^2} = 124.0mW / mm^2$$

b) (5pts) If the threshold voltage in the 0.13 μm process is 0.35V, what should be the threshold voltage in 90nm? Assuming 80mV/dec subthreshold slope, what would be the leakage power of the new processor?

Same scaling as in problem a, so:
$S = 1.444$, $U = 1.2$

Hence, the new value of the threshold voltage is:

$$V_{Tnew} = \frac{1}{U} V_{Told} = \frac{0.35V}{1.2} = 0.292V$$

Hence,

$$\Delta V_T = V_{Told} - V_{Tnew} = 58mV$$

We know that (see pages 96 and 212-214 of the reader):

$$P_{leak,old} = aV_{old} I_{leak,old} \tag{1}$$

$$P_{leak,new} = aV_{new} I_{leak,new} \tag{2}$$

where a is a constant.

Dividing (2) by (1) we get:

$$\frac{P_{leak,new}}{P_{leak,old}} = \frac{V_{new}}{V_{old}} \frac{I_{leak,new}}{I_{leak,old}} = \frac{1}{U} 10^{\Delta V_T / 80mV} \Rightarrow P_{leak,new} = 0.1mW \frac{1}{1.2} 10^{58/80} = 441\mu W$$