EE141-Spring 2010 Digital Integrated Circuits

Lecture 5
Switch Logic - Optimization

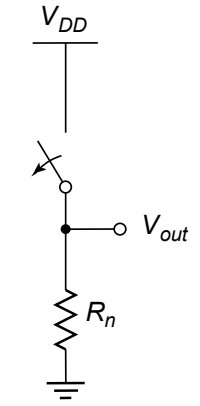
Administrativia

- Homework #2 posted
- First lab this week

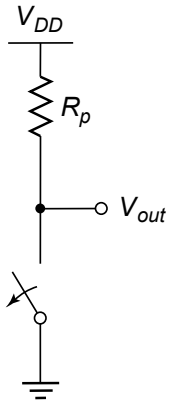
Class Material

- Last lecture
  - Design Rules
  - Introduction to switch logic
- Today's lecture
  - Optimization of inverter logic
- Reading (5.4-5.5)

CMOS Inverter at First Glance



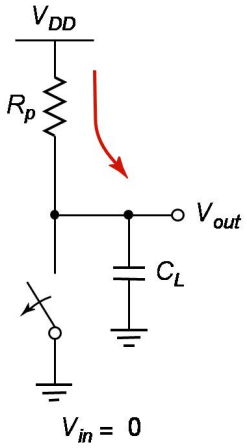
$V_{in} = V_{DD}$



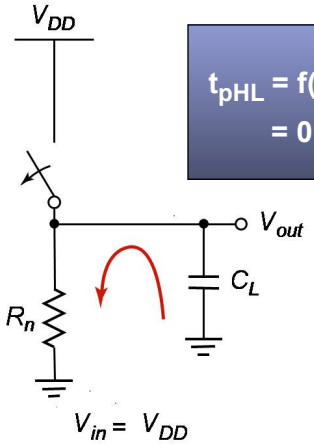
$V_{in} = 0$

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

CMOS Inverter: Transient Response



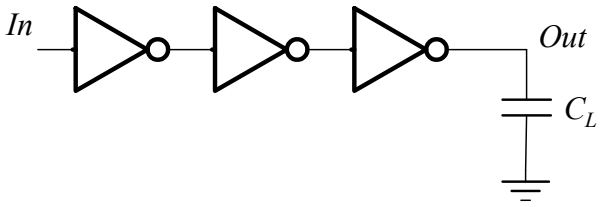
(a) Low-to-high



(b) High-to-low

$t_{pHL} = f(R_{on}C_L)$
$= 0.69\ R_n C_L$

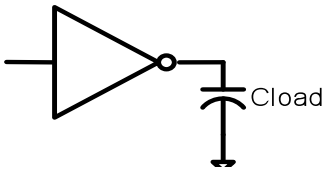
The Next Question: Inverter Chain



- For some given C_L:
  - How many stages are needed to minimize delay?
  - How to size the inverters?
- Anyone want to guess the solution?

Careful about Optimization Problems

- Get fastest delay if build one **very** big inverter
  - So big that delay is set only by self-loading



- Likely not the problem you're interested in
  - Someone has to drive this inverter…

Engineering Optimization Problems in General

- Need to have a set of constraints
- Constraints key to:
  - Making the result useful
  - Making the problem have a 'clean' solution
- For sizing problem:
  - Need to constrain size of first inverter

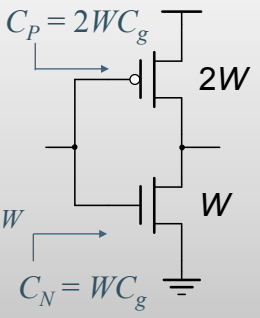
Delay Optimization Problem #1

- You are given:
  - A fixed number of inverters
  - The size of the first inverter
  - The size of the load that needs to be driven
- Your goal:
  - Minimize the delay of the inverter chain
- Need model for inverter delay vs. size

Inverter Delay

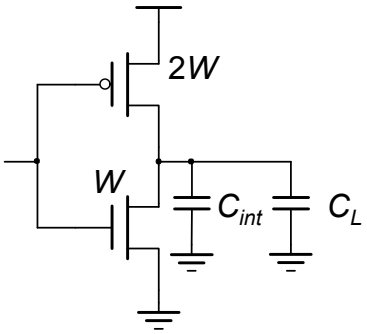
Delay: $t_{pHL} = (\ln 2)\, R_N C_L$ $t_{pLH} = (\ln 2)\, R_p C_L$

- Assume we want equal rise/fall delays
  $t_{pHL} = t_{pLH}$
  - Need approximately equal resistances, $R_N = R_P$
  - PMOS approximately 2 times larger resistance for same size;
  - Must make PMOS 2 times wider, $W_P = 2W_N = 2W$
  - $t_p = (\ln 2)\,(R_{inv}/W)\, C_L$ with R_{inv} resistance of minimum size NMOS



Loading on the previous stage: $C_{in} = WC_{ginv} = W(3C_G)$

Inverter Delay Model



$R = R_{inv}/W$

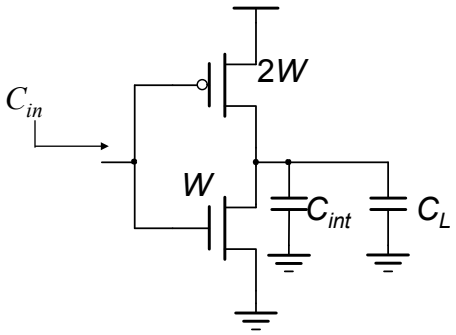
$C_{int} = W(3C_d) = WC_{dinv}$

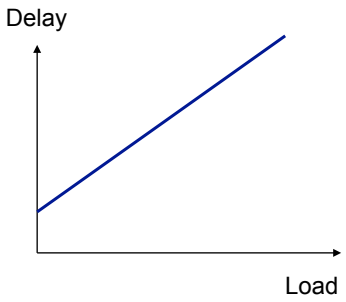
Replace ln(2) with k (a constant):

Delay = $kR(C_{int} + C_{L)}$

Delay = $k(R_{min}/W)(WC_{dinv} + C_L)$

Inverter with Load





Delay = $\boldsymbol{kR\,C_{in}(C_{int}/C_{in} + C_L/C_{in})}$

$\boldsymbol{= kR_{min}C_{ginv}[C_{dinv}/C_{ginv} + C_L/(WC_{ginv})]}$

= Delay (Internal) + Delay (Load)

$\boldsymbol{C_{dinv}/C_{ginv} = \gamma =}$ **Constant independent of size**

Delay Formula

$$Delay \sim R_W \left(C_{int} + C_L\right)$$

$$t_p = kR_W C_{\text{in}} \left(C_{\text{int}}/C_{in} + C_L / C_{in}\right) = t_{inv}\left(\gamma + f\right)$$

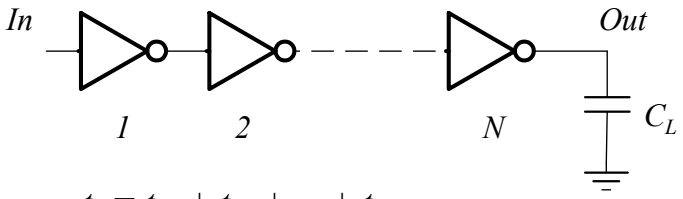
$C_{int} = \gamma\, C_{in}$ ($\gamma \approx 1$ for CMOS inverter)

$f = C_L/C_{in}$ – electrical fanout

$t_{\text{inv}} = kR_{min}C_{ginv}$

t_{inv} is independent of sizing of the gate!!!

Apply to Inverter Chain



$$t_p = t_{p1} + t_{p2} + \ldots + t_{pN}$$

$$t_{pj} = t_{inv}\left(\gamma + \frac{C_{in,j+1}}{C_{in,j}}\right)$$

$$t_p = \sum_{j=1}^{N} t_{p,j} = t_{inv}\sum_{i=1}^{N}\left(\gamma + \frac{C_{in,j+1}}{C_{in,j}}\right), \quad C_{in,N+1} = C_L$$

Optimal Tapering for Given N

- Delay equation has N-1 unknowns, $C_{in,2} \ldots C_{in,N}$
- **To minimize the delay,** find N-1 partial derivatives:

$$t_p = \ldots + t_{inv}\frac{C_{in,j}}{C_{in,j-1}} + t_{inv}\frac{C_{in,j+1}}{C_{in,j}} + \ldots$$

$$\frac{dt_p}{dC_{in,j}} = t_{inv}\frac{1}{C_{in,j-1}} - t_{inv}\frac{C_{in,j+1}}{C_{in,j}^2} = 0$$

Optimal Tapering for Given N (cont'd)

- Result: every stage has **equal fanout**:

$$\boxed{\frac{C_{in,j}}{C_{in,j-1}} = \frac{C_{in,j+1}}{C_{in,j}}}$$

- In other words, size of each stage is geometric mean of two neighbors:

$$\boxed{C_{in,j} = \sqrt{C_{in,j-1}C_{in,j+1}}}$$

- Equal fanout → every stage will have same delay

Optimum Delay and Number of Stages

- When each stage has same fanout f:

$$f^N = F = C_L / C_{in,1}$$

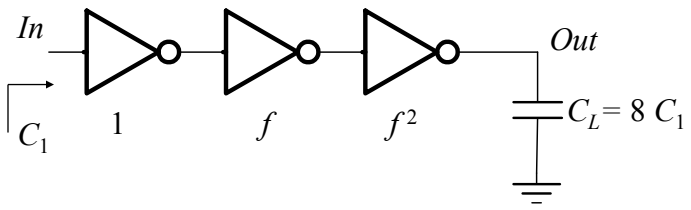
- Effective fanout of each stage:

$$f = \sqrt[N]{F}$$

- Minimum path delay:

$$t_p = N t_{inv} \left(\gamma + \sqrt[N]{F} \right)$$

Example



C_L/C_1 has to be evenly distributed across $N = 3$ stages:

$$f = \sqrt[3]{8} = 2$$

Delay Optimization Problem #2

- You are given:
  - The size of the first inverter
  - The size of the load that needs to be driven
- Your goal:
  - Minimize delay by finding optimal number and sizes of gates
- So, need to find N that minimizes:

$$t_p = N t_{inv}\left(\gamma + \sqrt[N]{C_L/C_{in}}\right)$$

Solving the Optimization

- Rewrite N in terms of fanout/stage f:

$$f^N = C_L/C_{in} \rightarrow \boxed{N = \frac{\ln\left(C_L/C_{in}\right)}{\ln f}}$$

$$t_p = N t_{inv}\left(\left(C_L/C_{in}\right)^{1/N} + \gamma\right) = t_{inv}\ln\left(C_L/C_{in}\right)\left(\frac{f+\gamma}{\ln f}\right)$$

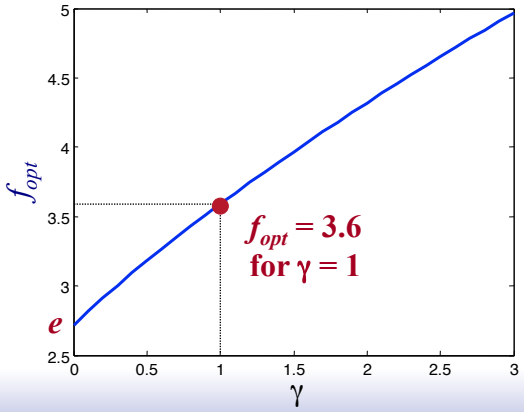
$$\frac{\partial t_p}{\partial f} = t_{inv}\ln\left(C_L/C_{in}\right)\cdot\frac{\ln f - 1 - \gamma/f}{\ln^2 f} = 0$$

$$f = \exp\left(1+\gamma/f\right) \qquad \boxed{\text{For } \gamma = 0, f = \text{e}, N = \ln\left(C_L/C_{in}\right)}$$

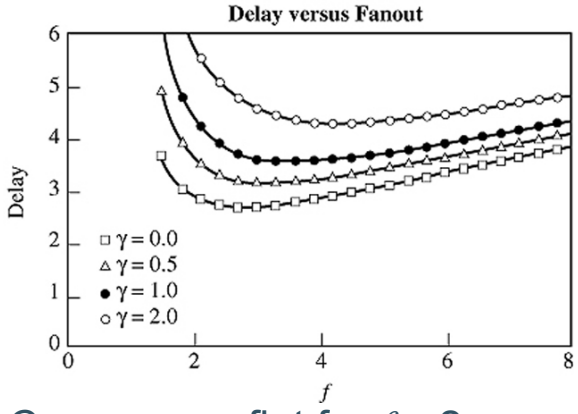
Optimum Effective Fanout *f*

- Optimum f for given process defined by γ

$$f = \exp(1 + \gamma / f)$$



In Practice: Plot of Total Delay



[Hodges, p.281]

- Curves very flat for $f > 2$
  - Simplest/most common choice: $f = 4$

Normalized Delay As a Function of F

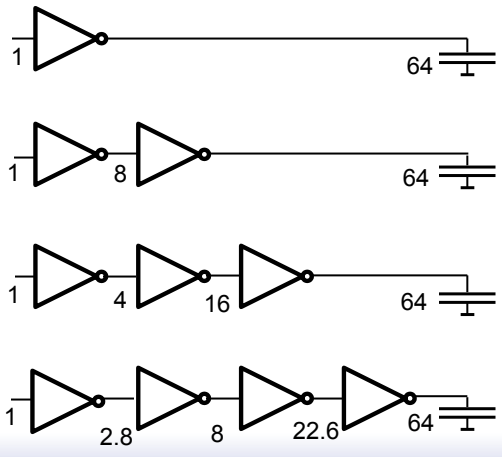
$$t_p = N t_{inv}\left(\gamma + \sqrt[N]{F}\right), \quad F = C_L / C_{in}$$

F	Unbuffered	Two Stage	Inverter Chain
10	11	8.3	8.3
100	101	22	16.5
1000	1001	65	24.8
10,000	10,001	202	33.1

($\gamma = 1$)

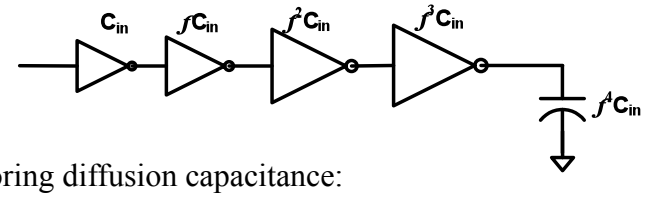
Textbook: page 210

Buffer Design



N	f	t_p
1	64	65
2	8	18
3	4	15
4	2.8	15.3

What About Energy (and Area)?



Ignoring diffusion capacitance:

$$C_{tot} = C_{in} + f \cdot C_{in} + \ldots + f^N \cdot C_{in}$$
$$= C_{in} \cdot (1 + f + \ldots + f^N)$$
$$= C_{in} + C_{in} \cdot f^N + C_{in} \cdot \underbrace{f \cdot (1 + f + \ldots + f^{N-2})}$$

Overhead !!! $f(f^{N-1}-1) / (f-1)$

Example (γ=0): C_L = 20pF; C_i = 50fF → N = 6

Fixed: 20pF

Overhead: 11.66pF !!!

Example Overhead Numbers

Example: C_L = 20pF; C_{in} = 50fF