Tunneling Transistor based 6T SRAM Bitcell Circuit Design in Sub-10nm Domain

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Abstract—The Static Random Access Memory (SRAM) directly impacts the performance of the modern multi-core processor. Hence, the power, performance and area metrics are very crucial for SRAM design. In this article, we have successfully designed 10 nm TFET based 6T SRAM circuit at reduced supply voltage of 0.5 V. We also have optimized the circuit for high density, high performance, intermediate (trade-off between high density, high performance) 6T SRAM application. Later, we have estimated the dynamic "Read" power, "Read" energy, "Write" power, "Write" energy. The performance metrics: "Read" delay and "Write delay" are also analyzed precisely. These power, energy, delay metrics are also compared against the existing 10nm FinFET.

Index Terms – Tunneling, TFET, 6T SRAM, Dynamic Read and Write Power.

I. INTRODUCTION

Nonstop scaling of silicon CMOS device has led to a record increase in multi-core performance of latest microprocessors. Because of the exponentially growing transistor count, the total power consumption and energy efficiency are important matrix for today's multi-core microprocessors. Therefore, nanoelectronics enabled energy efficiency at the device, circuit and system level are crucial. The dynamic power depends on the square supply voltage. Supply voltage cut while upholding device performance is an efficient method to decrease the power consumption because it decreases the dynamic power quadratically and the leakage power linearly. The fall of the threshold voltage leads to I_{OFF} rise exponentially for MOSFET The fundamental limit of MOSFET threshold voltage scaling blocks the supply voltage scaling. Hence, the supply voltage restricts the I_{ON} and I_{ON}/I_{OFF} ratio. In MOSFETs, the theoretical restriction of 60 mV/decade sub-threshold swing at room temperature leads to limit the threshold voltage scaling and low power operation [1].

The organization of the paper is as follows. Section I illustrates the limitation of the existing Silicon based MOSFET technology. Section II provides benchmarking for emerging devices. It also illustrates benchmarking of exiting TFET technology. Section III represents the simulation, result and analysis. Section IV shows the benchmarking between TFET and FinFET. Finally, Section V concludes the paper with a brief of future work.

II. EXISTING TFETs

A. Why Tunnel FET?

Numerous novel transistors have been explored to reduce power consumption for emerging circuit and architecture application. Benchmarking on post-CMOS logic transistors are summarized in [4]-[5].

Table 1: Performance Benchmarking for Emerging Devices [4].

Device Name	Area	Delay	Energy	Power	Throughput	Thr@<10W/cm2
units	µm2	ps	fJ	w/cm2	Pops/s/cm2	Pops/s/cm2
CMOS HP	40.8	84	2.48	71.8	29	4.04
CMOS LP	40.8	31331	0.42	0	0.08	0.08
III-IV TFET	54.4	1378	0.15	0.2	1.33	1.33
HJTFET	54.4	461	0.33	1.3	3.98	3.98
GNR TFET	54.4	861	0.04	0.1	2.13	2.13
GpnJ	26.2	143	10.03	268	26.73	1
SpinFET	40.8	282	3.2	27.8	8.68	3.13
STT/DW	6.8	112820	50	6.5	0.13	0.13
STMG	5.9	38094	0.4	0.2	0.44	0.44
STTtraid	17.7	228580	3.64	0.1	0.02	0.02
STOlogic	5.9	69760	51	12.3	0.24	0.2
ASLD	3.9	52522	20.78	10	0.48	0.48
SWD	2	12404	0.13	0.5	4.1	4.1
NML	11.8	57600	3.47	0.5	0.15	0.15

B. State of Art of Tunnel FET

The device performance of n-type III-V Tunnel FET is summarized in Table 2.

Table 2: Performance Comparison for fabricated III-V TFETs [3], [5].

Reference	Source-Channel Material	EOT [nm]	I_{ON} [uA/um]	V_{DS} [V]	V_{ON}-V_{OFF} [V]	I_{ON}/I_{OFF}	S_{MIN} [mV/dec]	S_{EFF} [mV/dec]
Zhou [7]	GaSb-InAs	1.3	180	0.5	1.5	6000	200	400
Zhou [8]	InP-InGaAs	1.3	20	0.5	1.75	450000	93	310
Mohata [9]	GaAsSb-InGaAs	1.75	135	0.5	1.5	17000	230	350
Zhao [10]	$In_{0.7}Ga_{0.3}As$	1.2	40	0.5	2	200000	84	380
Li [11]	AlGaSb-InAs	1.6	78	0.5	1.5	1600	125	470
Dewey [12]	$In_{0.53}Ga_{0.47}As$	1.1	5	0.3	0.9	70000	58	190

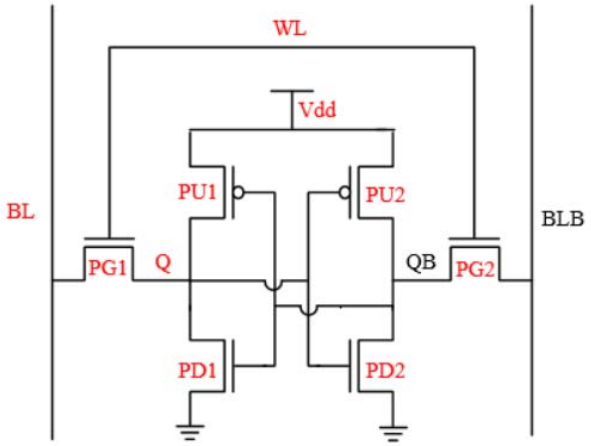
III. RESULT AND ANALYSIS

A. Simulation Setup

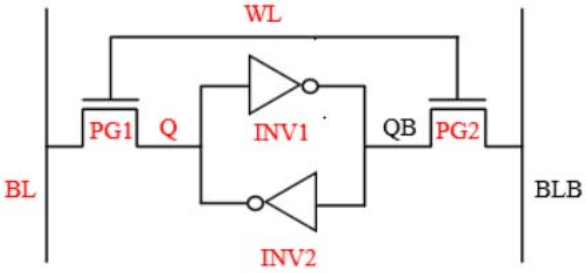
A Verilog-A lookup table based 10nm TFET transistor model [1]-[2] is used for the simulation. This model is not optimized and affects the "Write" operation significantly. But this is the best TFET model available to design circuit. This 6T SRAM circuit is designed and simulated by HSPICE.

B. 6T SRAM

Figure 1 shows TFET based 6T SRAM, which is most popular high density SRAM circuit. The operation of 6T SRAM is available in [6]-[7] for interested readers.



(a) Complete Circuit View



(b) Simplified Inverter View
Figure 1. TFET based 6T SRAM circuit.

C. Read Operation

Figure 2 shows the "Read" operation of TFET based 6T SRAM.

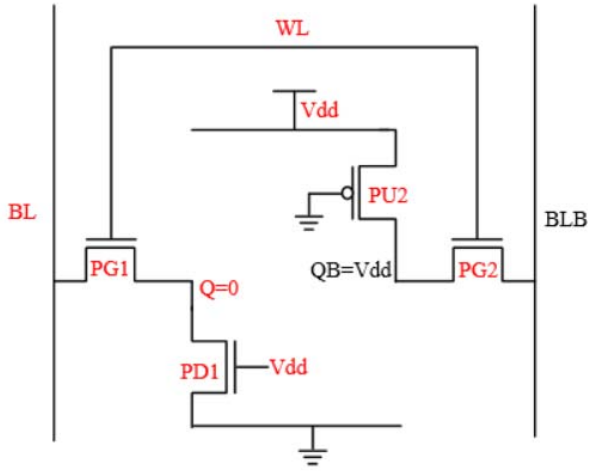


Figure 2. "Read" operation of TFET based 6T SRAM.

Figure 3 shows the "Read" operation output of 10nm TFET based 6T SRAM when PU:PD:PG ratio is 1:1:1, initial condition and final condition.

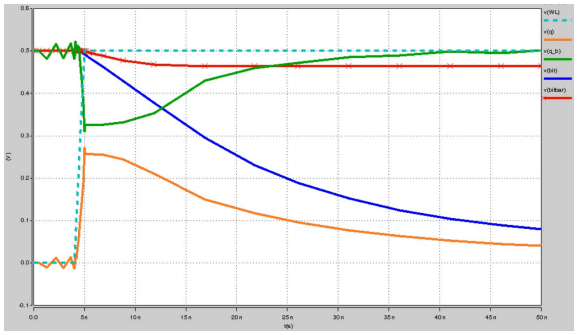


Figure 3: The "Read" Operation waveform of 10nm TFET based 6T SRAM (PU:PD:PG=1:1:1). Initial Condition: WL=0, Q=0, Q_b=1, BL=1, BL_b=1. Final Condition: WL=1, Q=0, Q_b=1, BL=0, BL_b=1.

Figure 4 shows the "Read" operation output of 10nm TFET based 6T SRAM when PU:PD:PG ratio is 1:5:2, initial condition and final condition.

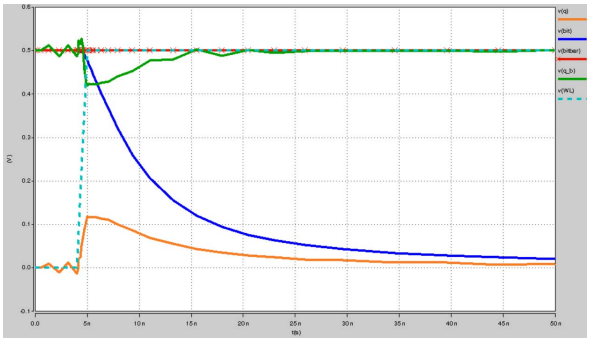


Figure 4: The "Read" Operation waveform of 10nm TFET based 6T SRAM (PU:PD:PG=1:5:2). Initial Condition: WL=0, Q=0, Q_b=1, BL=1, BL_b=1. Final Condition: WL=1, Q=0, Q_b=1, BL=0, BL_b=1.

Figure 5 shows the "Read" operation output of 10nm TFET based 6T SRAM when PU:PD:PG ratio is 2:5:2, initial condition and final condition.

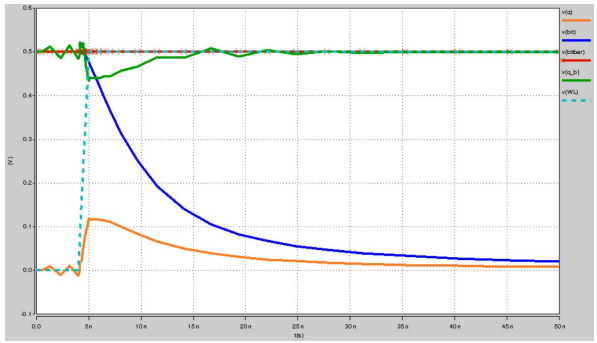


Figure 5: The "Read" Operation waveform of 10nm TFET 6T based SRAM (PU:PD:PG=2:5:2). Initial Condition: WL=0, Q=0, Q_b=1, BL=1, BL_b=1. Final Condition: WL=1, Q=0, Q_b=1, BL=0, BL_b=1.

D. Write Operation

Figure 6 shows the "Write" operation of TFET based 6T SRAM. This Verilog-A lookup table based 10nm TFET transistor model [2] has couple of limitations: (i) it

give huge nose to Q and QB after "Write" operation for any circuit combination; (ii) it does n't allow 6T SRAM circuit design for most of the sizing. We have optimized our 6T SRAM circuit to minimize these unwanted glitch from the TFET.

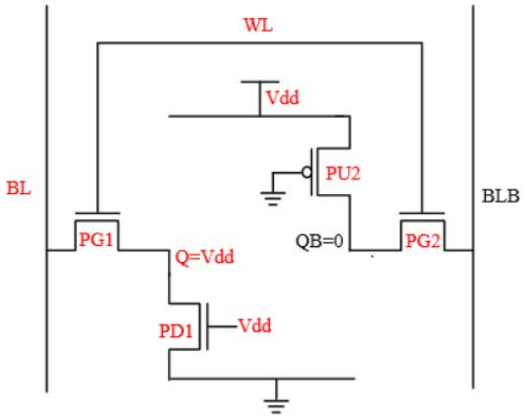


Figure 6: "Write" operation of TFET based 6T SRAM.

Figure 7 shows the "Write" operation output of 10nm TFET based 6T SRAM when PU:PD:PG ratio is 1:1:1, initial condition and final condition.

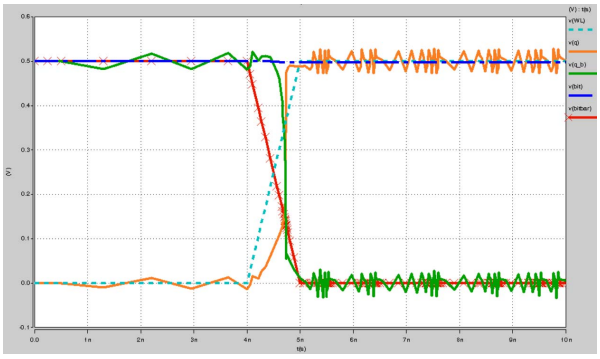


Figure 7: The "Write" operation waveform of 10nm TFET based 6T SRAM (PU:PD:PG=1:1:1). Initial Condition: WL=0, Q=0, Q_b=1, BL=1, BL_b=1. Final Condition: WL=1, Q=1, Q_b=0, BL=1, BL_b=0.

Figure 8 shows the "Write" operation output of 10nm TFET based 6T SRAM when PU:PD:PG ratio is 1:5:2, initial condition and final condition.

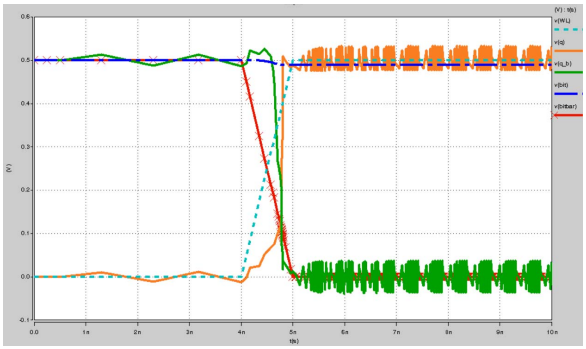


Figure 8: The "Write" operation waveform of 10nm TFET based 6T SRAM (PU: PD: PG=1:5:2). Initial Condition: WL=0, Q=0, Q_b=1, BL=1, BL_b=1. Final Condition: WL=1, Q=1, Q_b=0, BL=1, BL_b=0.

Figure 9 shows the "Write" operation output of 10nm TFET based 6T SRAM when PU:PD:PG ratio is 2:5:2, initial condition and final condition.

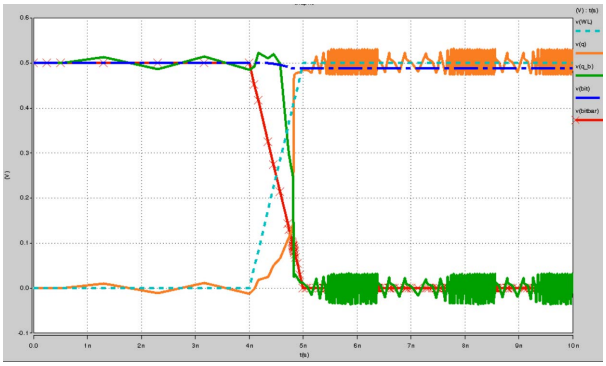


Figure 9: The "Write" operation waveform of 10nm TFET based 6T SRAM (PU:PD:PG=2:5:2). Initial Condition: WL=0, Q=0, Q_b=1, BL=1, BL_b=1. Final Condition: WL=1, Q=1, Q_b=0, BL=1, BL_b=0.

IV. BENCHMARKING OF TFET VS. FINFET

The comparison between 10 nm Tunnel FET 6T SRAM and 10 nm FinFET 6T SRAM is summarized in Table 3. The physical significances of the benchmarking between are discussed below.

- The dynamic write power of TFET is 4.55E+06 times more than FinFET based SRAM. This a drawback of TFET device 6T SRAM.
- The dynamic write energy of TFET based 6T SRAM is 4.09E+06 times more than FinFET based 6T SRAM.
- TFET based 6T SRAM writes 11% faster than FinFET based 6T SRAM.
- The dynamic Read power of TFET based 6T SRAM is 8.29 E+06 times more than FinFET based 6T SRAM. This a drawback of TFET device 6T SRAM.
- TFET based 6T SRAM reads 21% slower than FinFET based 6T SRAM.
- The dynamic Read energy of TFET based 6T SRAM is 1.01E+08 times more than FinFET based 6T SRAM.

Table 3: Benchmarking between 10 nm TFET based 6T SRAM and 10 nm FinFET based 6T SRAM.

Transistor	Tunnel FET			FinFET		
Technology Node (n,m)	10	10	10	10	10	10
Vdd	0.5	0.5	0.5	0.5	0.5	0.5
Density	High	Intermediate	Low	High	Intermediate	Low
Performance	Low	Intermediate	High	Low	Intermediate	High
PU:PD:PG ratio	1:1:1	1:5:2	2:5:2	1:1:1	1:5:2	2:5:2

Dynamic Write Power (W)	5.82 E-09	1.58E-08	3.37 E-08	1.28 E-15	1.28E-15	1.28 E-15
Write Delay (S)	9.90 E-10	9.90E-10	9.90 E-10	1.10 E-09	1.10E-09	1.10 E-09
Dynamic Write Energy (J)	5.76 E-18	1.56E-17	3.34 E-17	1.41 E-24	1.41E-24	1.41 E-24
Dynamic Read Power (W)	1.06 E-08	2.77E-09	3.32 E-09	1.27 E-15	1.27E-15	1.27 E-15
Read Delay (S)	4.26 E-08	2.69E-08	1.42 E-08	3.51 E-09	3.48E-09	3.49 E-09
Dynamic Read Energy (J)	4.50 E-16	7.44E-17	4.70 E-17	4.47 E-24	4.41E-24	4.43 E-24

V. CONCLUSION AND FUTURE WORK

We have successfully optimized our 6T SRAM circuit to minimize these unwanted glitch from the TFET model. The read and write operation are ensured with enough glitch margin. The only bright side is TFET based SRAM writes 11% faster than FinFET based SRAM. TFET based 6T SRAM reads 21% slower than FinFET based 6T SRAM. So, the speed matrix of TFET SRAM is ok. But the dynamic "Write" power, dynamic "Write" energy, dynamic Read power and dynamic Read energy of TFET based SRAM are more than FinFET based SRAM. So, TFET based 6T SRAM is more power hunger than FinFET based 6T SRAM. Our future work will involve the detailed analysis of TFET based SRAM.

VI. ACKNOWLEDGMENT

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