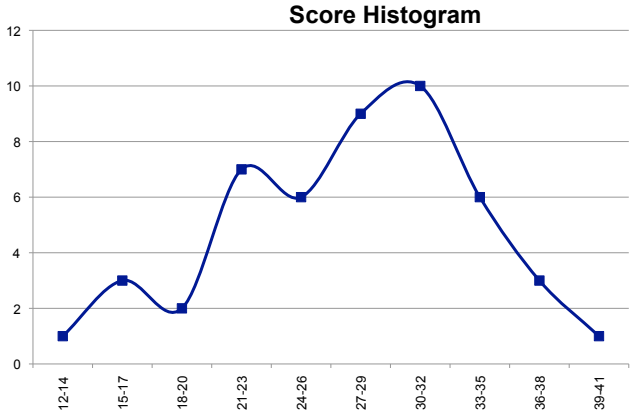
EE141-Spring 2010 Digital Integrated Circuits

Lecture 11
Transistor Capacitors

Administrativia

- HW 4 due on Friday
- No re-grades on MT1 after next Wednesday
- Project to be launched in week 7 – stay tuned

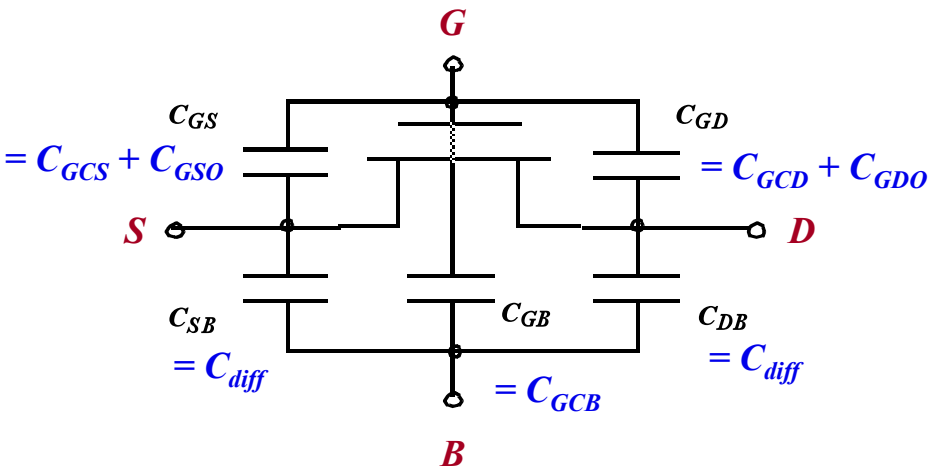
Midterm 1



Max: 40
Mean: 27.9
Median: 28.1
Stdev: 5.97

MOS Capacitance

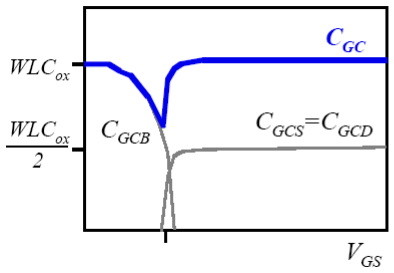
MOS Capacitances



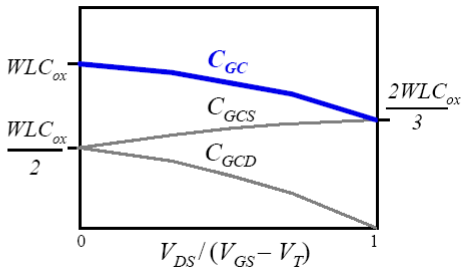
Gate Capacitance

- Capacitance (per area) from gate across the oxide is $W \cdot L \cdot C_{ox}$, where $C_{ox}=\varepsilon_{ox}/t_{ox}$

Gate Capacitance

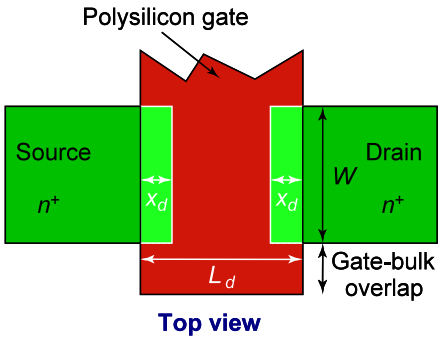


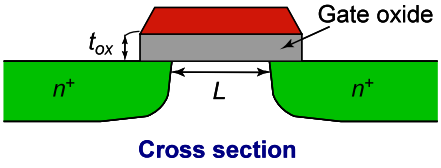
C_{gate} vs. V_{GS} (with V_{DS} = 0)



C_{gate} vs. operating region

Gate Overlap Capacitance

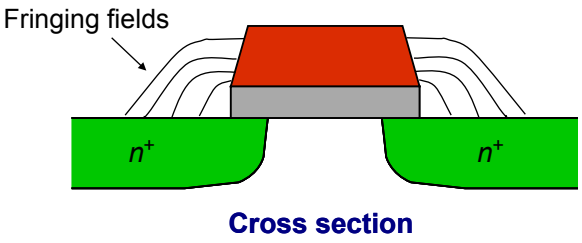




$$C_O = C_{ox} \cdot x_d$$

Off/Lin/Sat → $C_{GSO} = C_{GDO} = C_O \cdot W$

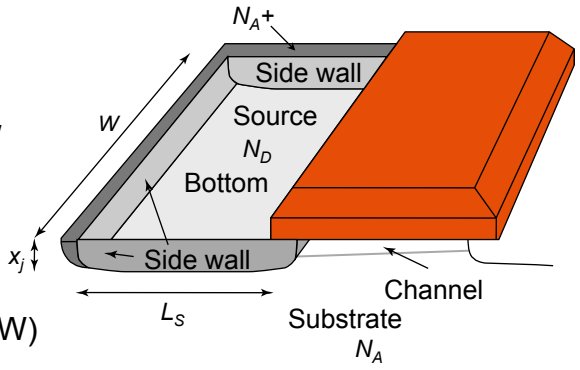
Gate Fringe Capacitance



- C_{OV} not just from metallurgic overlap – get fringing fields too
- Typical value: ~0.2fF·W(in μm)/edge

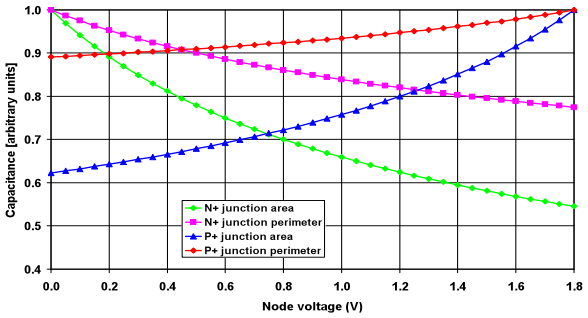
Diffusion Capacitance

- Bottom
  - Area cap
  - $C_{bottom} = C_j \cdot L_S \cdot W$
- Sidewalls
  - Perimeter cap
  - $C_{sw} = C_{jsw} \cdot (2L_S + W)$
- GateEdge
  - $C_{ge} = C_{jgate} \cdot W$
  - Usually automatically included in the SPICE model



Junction Capacitance (2)

- Junction caps are nonlinear
  - C_J is a function of junction bias



- SPICE model equations:
  - Area C_J = area × C_{J0} / (1+ $|V_{DB}|/\phi_B)^{mj}$
  - Perimeter C_J = perim × C_{JSW} / (1 + $|V_{DB}|/\phi_B)^{mjsw}$
  - Gate edge C_J = W × C_{Jgate} / (1 + $|V_{DB}|/\phi_B)^{mjswg}$
- How do we deal with nonlinear capacitance?

Linearizing the Junction Capacitance

Replace non-linear capacitance by
large-signal equivalent linear capacitance
which displaces equal charge over voltage swing of interest

$$C_{eq} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(V_{high}) - Q_j(V_{low})}{V_{high} - V_{low}} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

Capacitance Model Summary

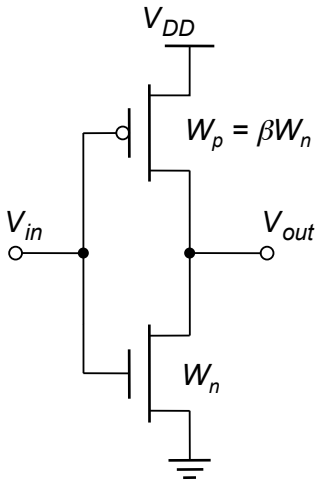
- **Gate-Channel Capacitance**
  - $C_{GC} \approx 0$ ($|V_{GS}| < |V_T|$)
  - $C_{GC} = C_{ox} \cdot W \cdot L_{eff}$ (Linear)
    - 50% G to S, 50% G to D
  - $C_{GC} = (2/3) \cdot C_{ox} \cdot W \cdot L_{eff}$ (Saturation)
    - 100% G to S
- **Gate Overlap Capacitance**
  - $C_{GSO} = C_{GDO} = C_O \cdot W$ (Always)
- **Junction/Diffusion Capacitance**
  - $C_{diff} = C_j \cdot L_S \cdot W + C_{jsw} \cdot (2L_S + W) + C_{jg}W$ (Always)

Capacitances in 0.25 μm CMOS Process

	C_{ox} (fF/μm^2)	C_O (fF/μm)	C_j (fF/μm^2)	m_j	ϕ_b (V)	C_{jsw} (fF/μm)	m_{jsw}	ϕ_{bsw} (V)
NMOS	6	0.31	2	0.5	0.9	0.28	0.44	0.9
PMOS	6	0.27	1.9	0.48	0.9	0.22	0.32	0.9

CMOS Inverter VTC

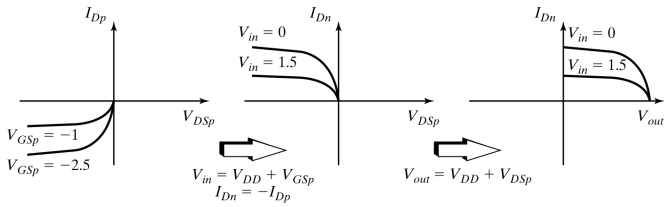
The CMOS Inverter



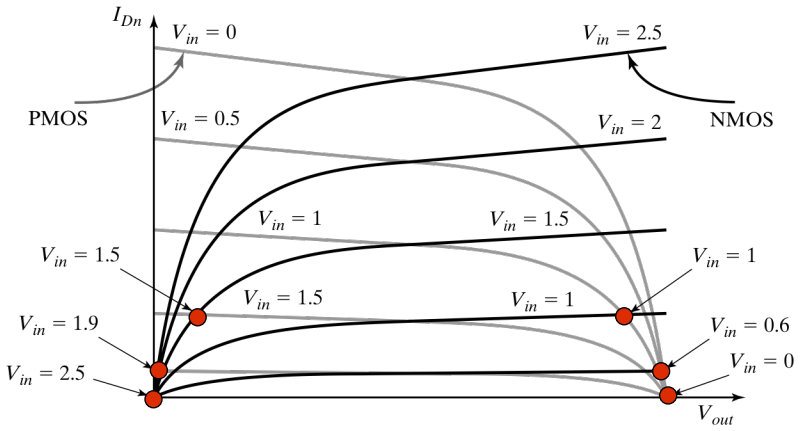
PMOS Load Lines

PMOS Load Lines

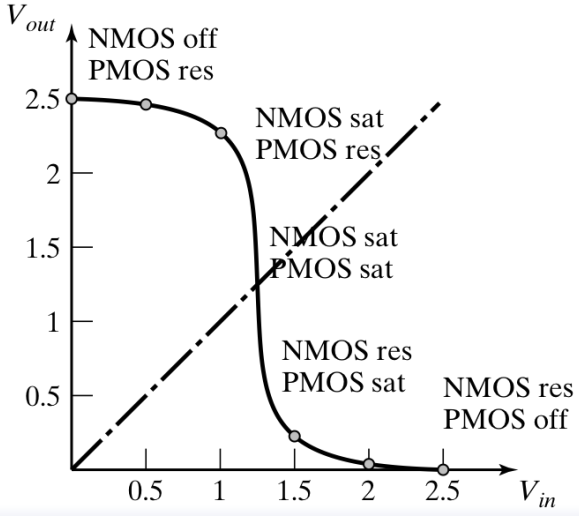
- For DC VTC, $I_{Dn} = I_{Dp}$
  - Graphically, looking for intersections of NMOS and PMOS IV characteristics
- To put IV curves on the same plot, PMOS IV is "flipped" since $|V_{DSp}| = V_{DD} - V_{out}$
  - Also, $|V_{GSp}| = V_{dd} - V_{in}$



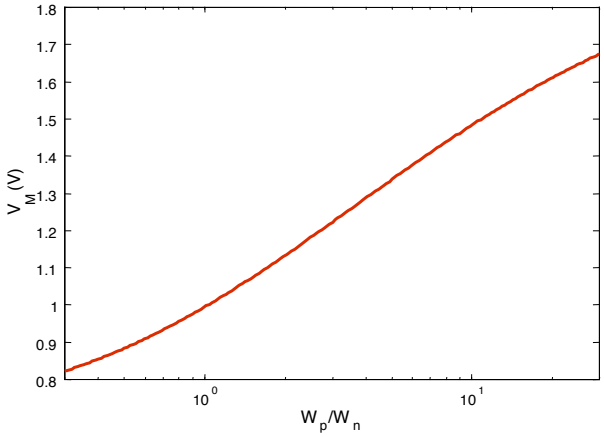
CMOS Inverter Load Characteristics



CMOS Inverter VTC

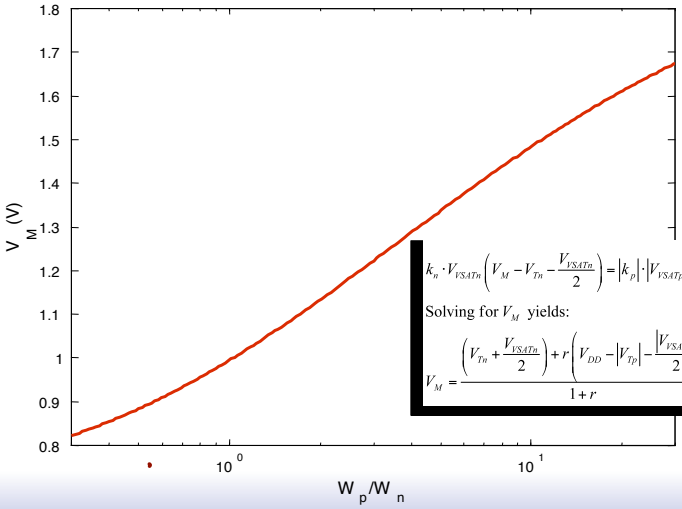


Switching Threshold as a Function of Transistor Ratio



$$I_{dn}(V_M) = I_{dp}(V_M)$$

Switching Threshold as a Function of Transistor Ratio



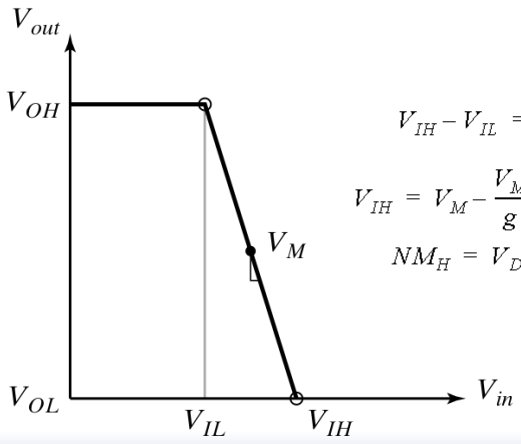
$$k_n \cdot V_{VSATn}\left(V_M - V_{Tn} - \frac{V_{VSATn}}{2}\right) = |k_p| \cdot |V_{VSATp}|\left(V_{DD} - V_M - |V_{Tp}| - \frac{|V_{VSATp}|}{2}\right)$$

Solving for V_M yields:

$$V_M = \frac{\left(V_{Tn} + \frac{V_{VSATn}}{2}\right) + r\left(V_{DD} - |V_{Tp}| - \frac{|V_{VSATp}|}{2}\right)}{1+r} \quad \text{with } r = \frac{|k_p| \cdot |V_{VSATp}|}{k_n \cdot V_{VSATn}} = \frac{W_p v_{satp}}{W_n v_{satn}}$$

Determining V_{IH} and V_{IL}

A simplified approach

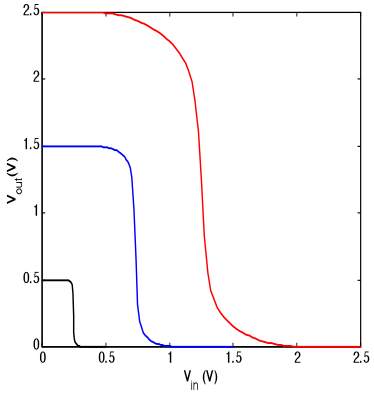


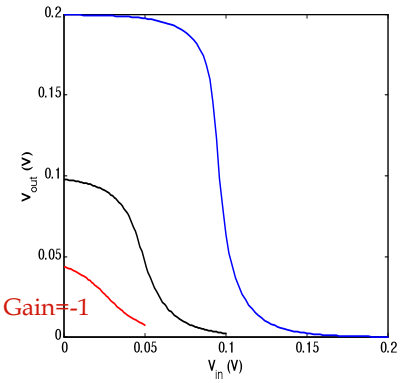
$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

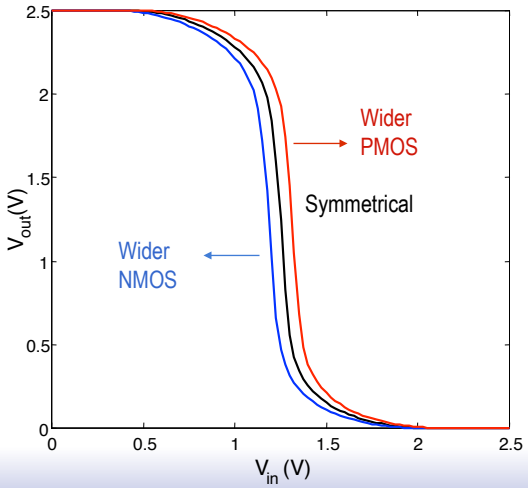
$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

Gain as a function of VDD

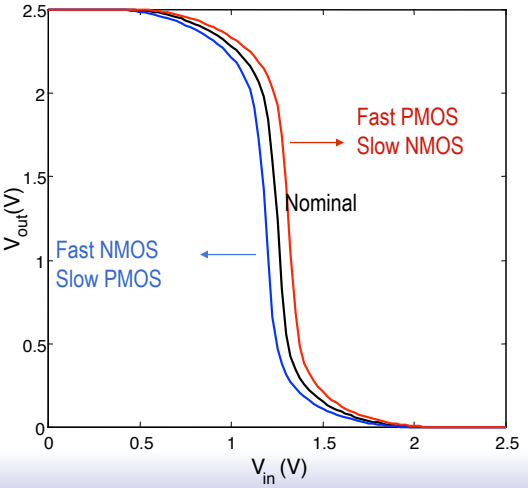




Impact of Sizing

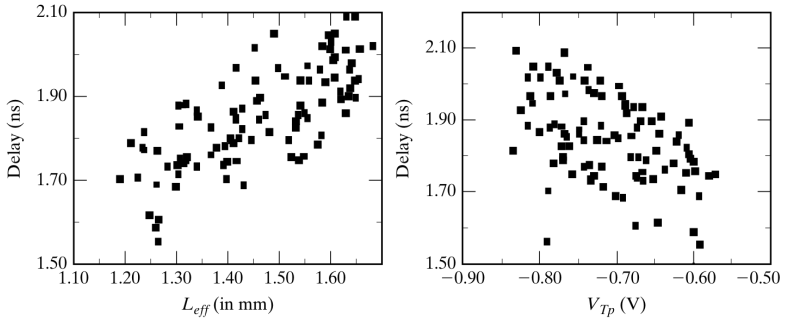


Impact of Process Variations



Process Variations

Not all transistors are alike
Impacts parameters such as reliability and performance

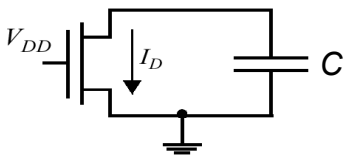


Define process corners: SS, FF, SF, FS

CMOS Switching Delay

MOS Transistor as a Switch

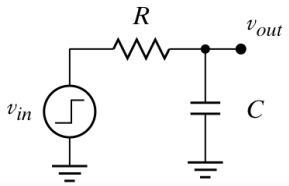
• Discharging a capacitor



$$i_D = i_D(v_{DS})$$

$$i_D = C\frac{dV_{DS}}{dt}$$

• We modeled this with:



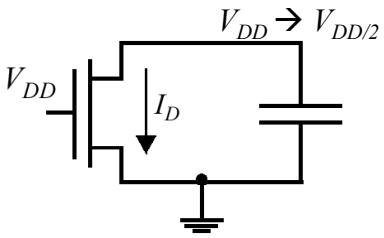
$t_p = \ln(2)\,RC$

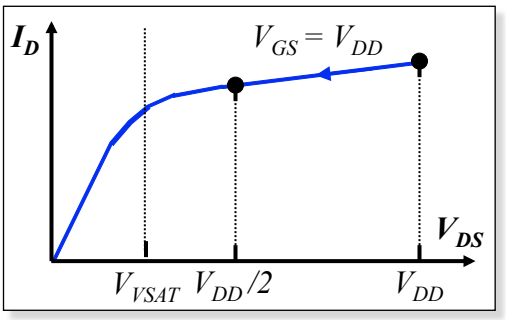
MOS Transistor as a Switch

- Real transistors aren't exactly resistors
  - Look more like current sources in saturation
- Two questions:
  - Which region of IV curve determines delay?
  - How can that match up with the RC model?

Transistor Discharging a Capacitor

- With a step input:

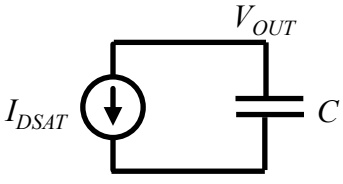


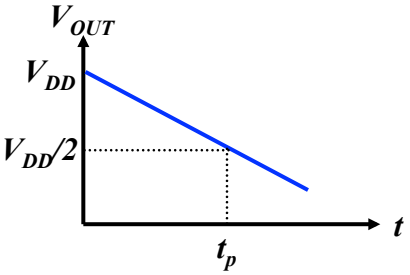


- Transistor is in (velocity) saturation during entire transition from V_{DD} to $V_{DD}/2$

Switching Delay

- In saturation, transistor basically acts like a current source:



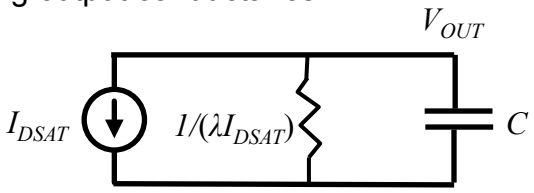


$$V_{OUT} = V_{DD} - (I_{DSAT}/C)t \longrightarrow \boxed{t_p = C(V_{DD}/2)/I_{DSAT}}$$

Defining IDSAT

Switching Delay (with Output Conductance)

- Including output conductance:



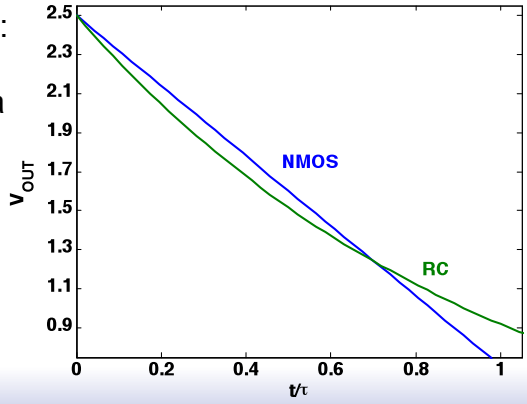
$$V_{OUT} = \left(V_{DD} + \lambda^{-1}\right) e^{-t/(C/\lambda I_{DSAT})} - \lambda^{-1}$$

- For "small" λ:

$$t_p \approx \frac{C\left(V_{DD}/2\right)}{\left(1+\lambda V_{DD}\right) I_{DSAT}}$$

RC Model

- Transistor current not linear on V_{OUT} – how is the RC model going to work?
- Look at waveforms:
- Voltage looks like a ramp for RC too



Finding Req

- Match the delay of the RC model with the actual delay:

$$t_p = t_{p,RC}$$

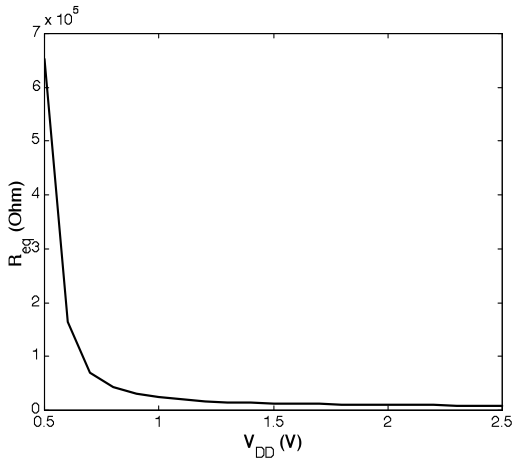
$$\frac{C(V_{DD}/2)}{(1+\lambda V_{DD})I_{DSAT}} = \ln(2) R_{eq} C \longrightarrow \boxed{R_{eq} = \frac{(V_{DD}/2)}{\ln(2)(1+\lambda V_{DD})I_{DSAT}}}$$

- Often just: $\boxed{R_{eq} \approx \frac{1}{2 \cdot \ln(2)} \frac{V_{DD}}{I_{DSAT}}}$

- Note that the book uses a different method and gets $0.75 \cdot V_{DD}/I_{DSAT}$ instead of ~$0.72 \cdot V_{DD}/I_{DSAT}$.

The Book's Method

The Transistor as a Switch



The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31