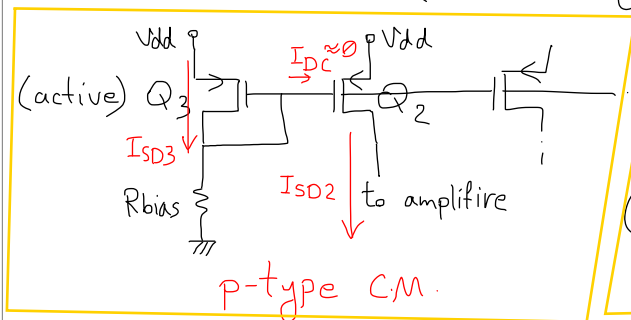
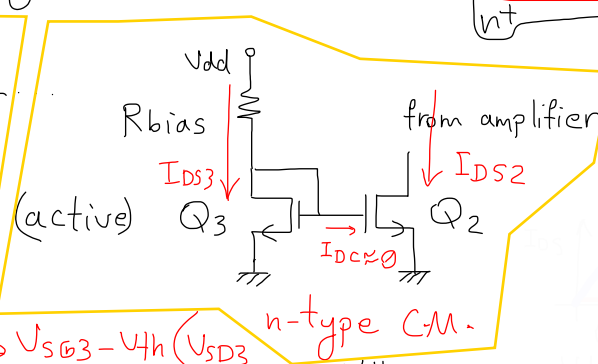


* Current Mirrors (DC Analysis):



p-type CM.



n-type CM.

$$V_{G3} = V_{D3} \Rightarrow V_{SG3} = V_{SD3} \Rightarrow V_{SG3} - V_{th} \left(V_{SD3} \right)$$

for pmos Q3 : $I_{SD3} = \frac{1}{2} \mu_p C_{ox} \frac{W_3}{L_3} (V_{SG3} - V_{th})^2 [1 + \lambda (V_{SD3} - (V_{SG3} - V_{th}))]$ \Rightarrow find $\begin{cases} V_{SG3} \\ I_{SD3} \end{cases}$

KVL: $V_{DD} = V_{SG3} + R_{bias} \cdot I_{SD3}$

Q2 operate in active: $\frac{I_{SD2}}{I_{SD3}} = \frac{\frac{1}{2} \mu_p C_{ox} \frac{W_2}{L_2} (V_{SG2} - V_{th})^2 [1 + \lambda (V_{SD2} - (V_{SG2} - V_{th}))]}{\frac{1}{2} \mu_p C_{ox} \frac{W_3}{L_3} (V_{SG3} - V_{th})^2 [1 + \lambda V_{th}]}$

$$\frac{I_{SD2}}{I_{SD3}} = \frac{\frac{W_2}{L_2}}{\frac{W_3}{L_3}} \times \frac{1 + \lambda (V_{SD2} - (V_{SG2} - V_{th}))}{1 + \lambda V_{th}}$$

$V_{DD} = 3V, V_{SD2} \approx 1.5V, V_{th} = 0.5V, V_{SG2} = 1V$
 $\lambda = 0.01 \left[\frac{1}{V} \right]$

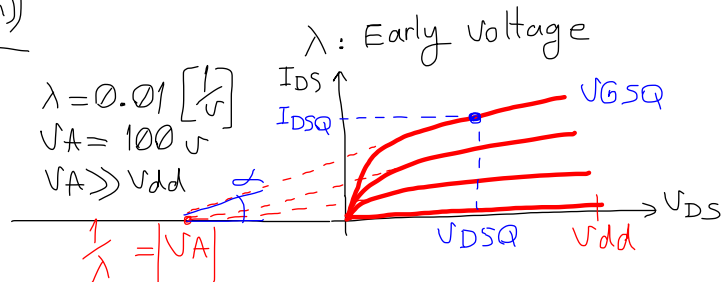
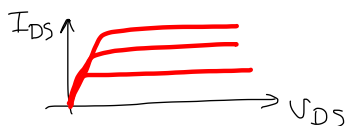
$$r_{ds} = \frac{1}{\lambda \cdot I_{DS}}$$

this term generate some error in mapping the current and for $\lambda \approx 0$ disappears

for nmos Q3 : $I_{DS3} = \frac{1}{2} \mu_n C_{ox} \frac{W_3}{L_3} (V_{GS3} - V_{th})^2 [1 + \lambda V_{th}]$ \Rightarrow find $\begin{cases} V_{GS3} \\ I_{DS3} \end{cases}$

KVL: $V_{DD} = R_{bias} \cdot I_{DS3} + V_{GS3}$

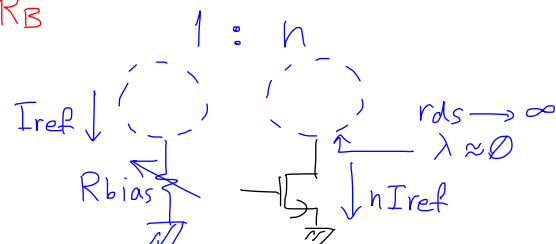
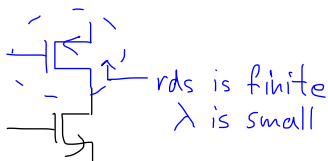
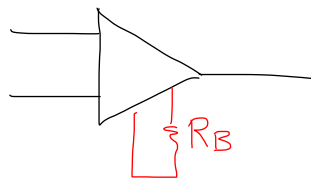
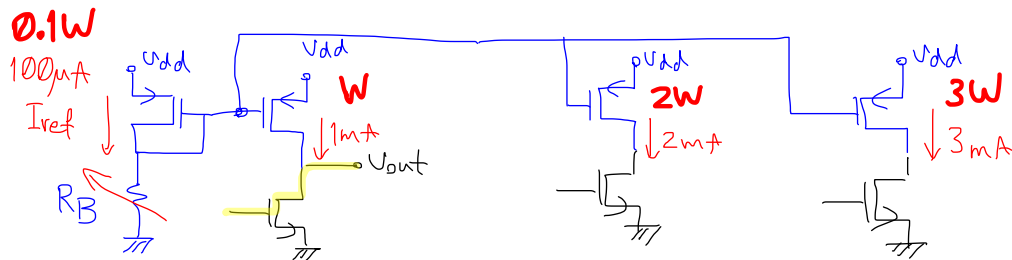
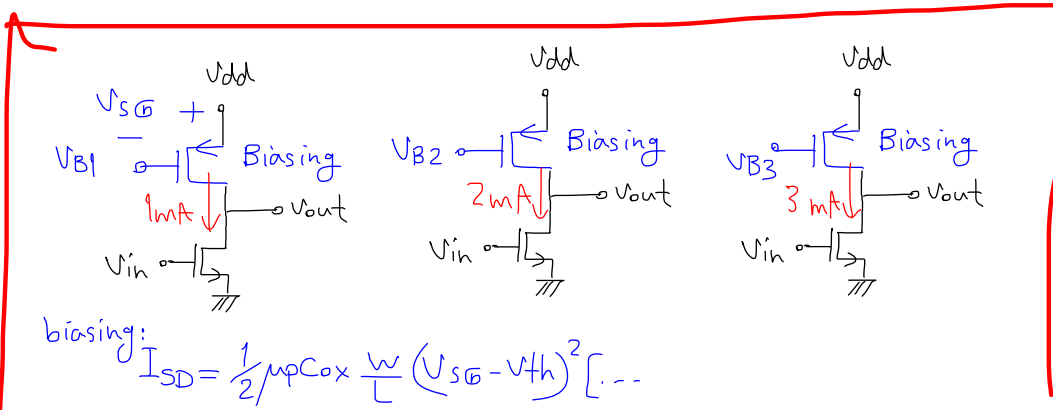
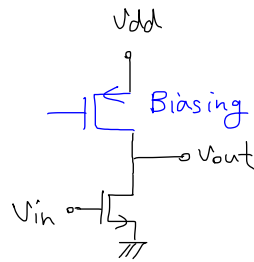
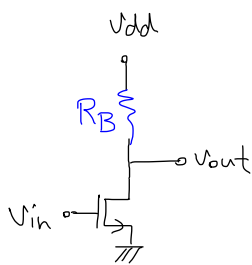
$$\frac{I_{DS2}}{I_{DS3}} = \frac{\frac{W_2}{L_2}}{\frac{W_3}{L_3}} \times \frac{1 + \lambda (V_{DS2} - (V_{GS2} - V_{th}))}{1 + \lambda V_{th}}$$



$$r_{and} = \frac{I_{DSQ}}{V_A + V_{DSQ}}, \quad \begin{cases} V_A \gg V_{DD} \\ V_{DSQ} < V_{DD} \end{cases}$$

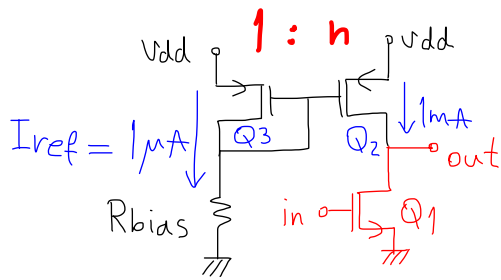
ignore

$$\frac{I_{DSQ}}{V_A} = \frac{1}{r_{ds}} = \lambda \cdot I_{DSQ} \Rightarrow \lambda = \frac{1}{V_A}$$



* Current Mirror (AC analysis) :

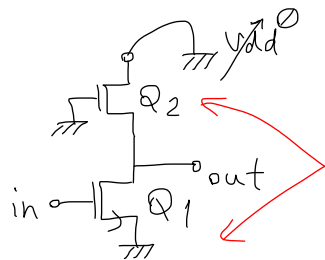
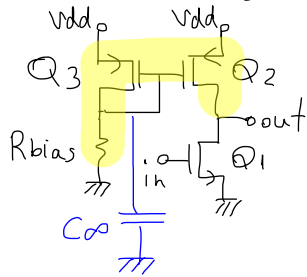
$$L_2 = L_3 = 45 \text{ nm}$$



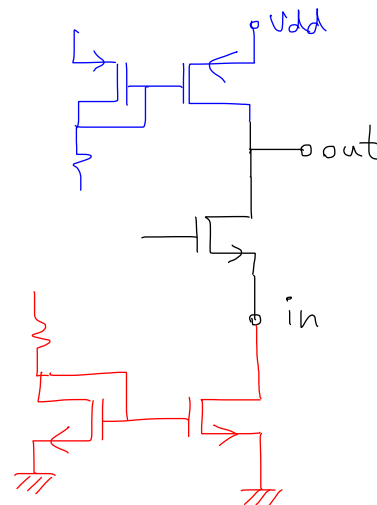
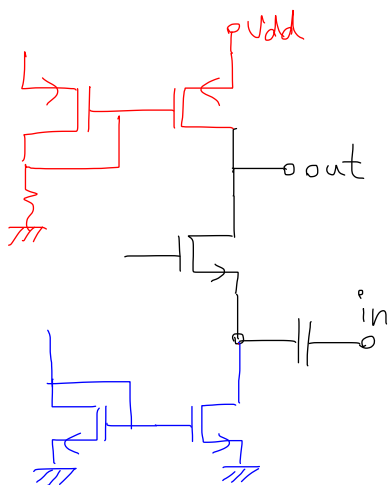
$$\frac{I_{SD2}}{I_{SD3}} \approx \frac{\frac{W_2}{L_2}}{\frac{W_3}{L_3}} \Rightarrow \frac{1\mu\text{A}}{1\mu\text{A}} = \frac{W_2}{W_3}$$

* Gate of Q_2 mainly has a DC voltage and during AC analysis is considered as ground

→ AC analysis

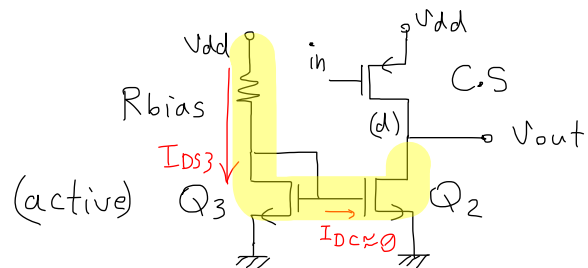
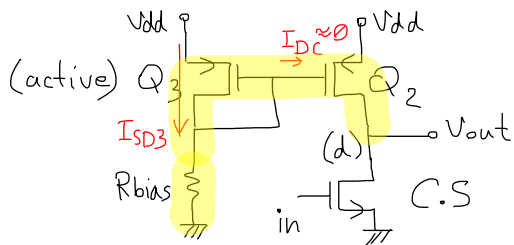


replace Q_1 and Q_2 with small-signal model

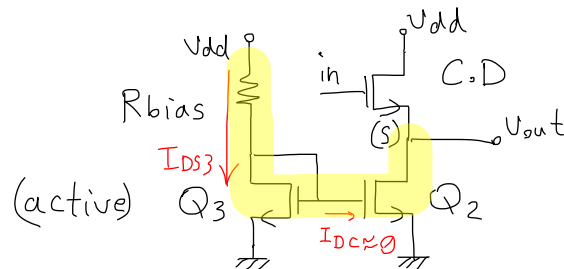
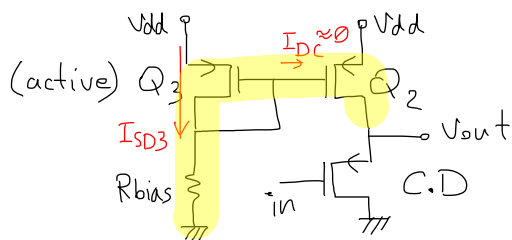


* Current Mirrors (in Circuit):

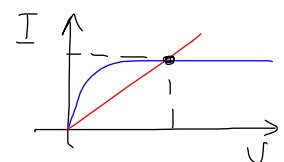
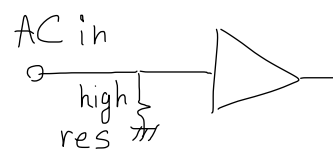
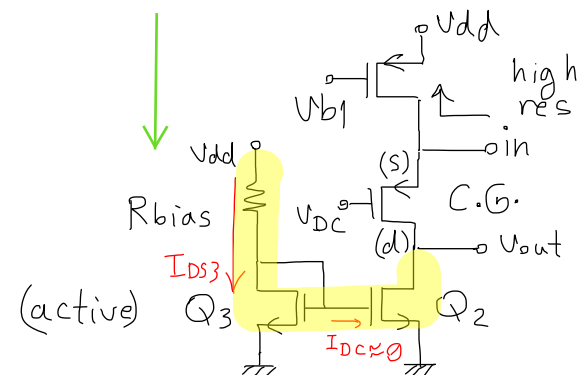
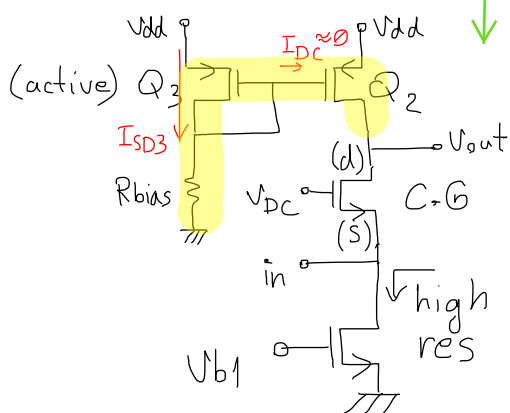
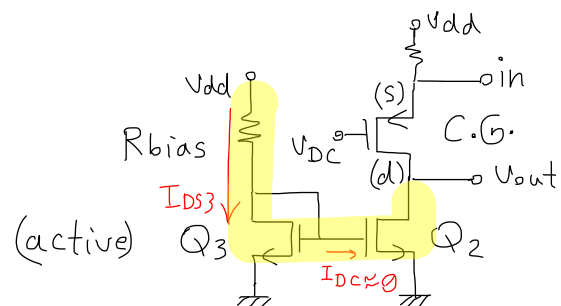
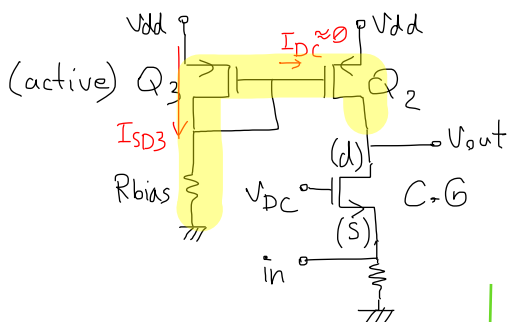
Common Source



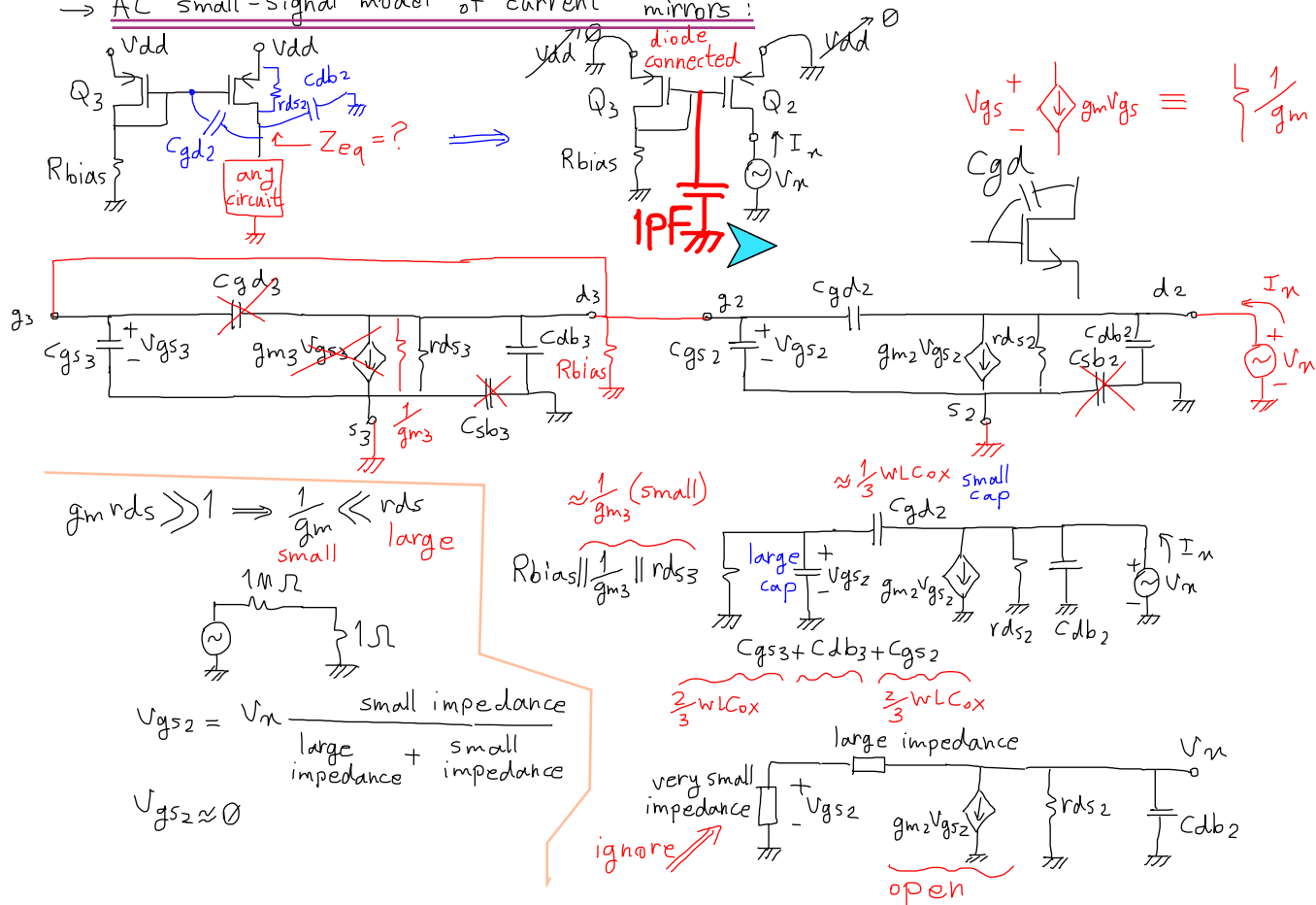
Common Drain



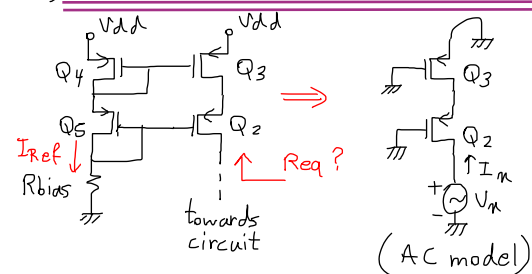
Common Gate



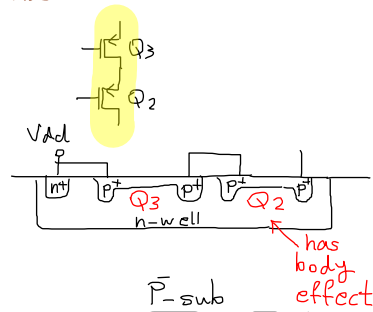
→ AC small-signal model of current mirrors:



→ how to increase resistance of a current mirror:



use one n-well



Handwritten notes and equations:

- $(g_{m2} + g_{b2})V_{s2} + g_{ds3}V_{s2} + g_{ds2}(V_{s2} - V_n) = 0$
- $i_n = g_{ds3}V_{s2}$
- $\Rightarrow V_{s2} [g_{m2} + g_{b2} + g_{ds3} + g_{ds2}] = V_n [g_{ds2}]$
- $\Rightarrow \frac{V_n}{i_n} = \frac{g_{ds3} + g_{ds2} + g_{m2} + g_{b2}}{g_{ds2} g_{ds3}} \approx g_{m2} r_{ds2} r_{ds3}$