

## *EE141-Spring 2010 Digital Integrated Circuits*

### Lecture 2 Design Metrics

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## *Administrative Stuff*

- ❑ Discussions start next week
- ❑ Labs start in week 3
- ❑ Homework #1 is due next Friday
  - Everyone should have an EECS instructional account
  - Use cory, quasar, pulsar

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## SPICE “Deck” Syntax (hidden)

### CMOS LEAKAGE CHARACTERIZATION

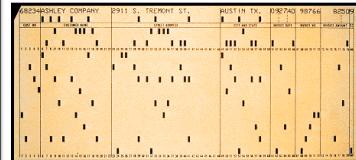
```
X1 0 1 nvdd1 INVERTER
X2 nvdd 2 nvdd2 INVERTER

VDDS nvdd 0 1.2
VDDN nvdd nvdd1 0
VDDP nvdd nvdd2 0

.subckt INVERTER nin nout nsupply

X1 nout nin 0 0 nsvt W=0.15 L=0.1
X2 nout nin nsupply nsupply psvt W=0.3 L=0.1
.ends INVERTER

* Commands
.dc VDDS 0.6 1.2 0.05
.print i(VDDN), i(VDDP)
.options brief
.lib '..\..\Models\65nmCMOS.lib' svt_TT
.END
```



Born in the days of punched cards

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## Last Lecture

### ❑ Last lecture

- Introduction, Moore’s law, future of ICs

### ❑ Today’s lecture

- Introduces basic metrics for design of integrated circuits
- How to measure cost?
- Intro to IC manufacturing

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## *Design Metrics*

- How to evaluate performance of a digital circuit (gate, block, ...)?
  - Cost
  - Reliability
  - Speed/Performance (delay, frequency)
  - Power

## *Cost of Integrated Circuits*

- NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.
- Recurrent costs - variable
  - proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these proportional to chip area



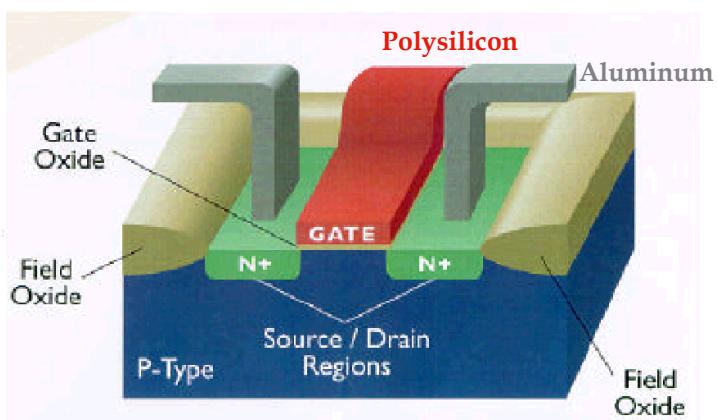
## In Intro to CMOS IC Manufacturing

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## The MOS Transistor

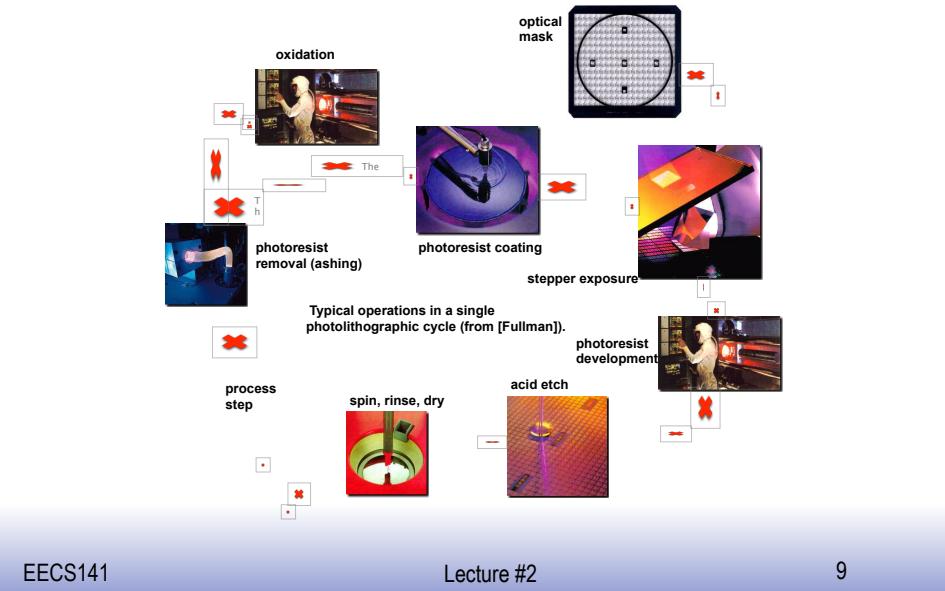


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## Review: Photo-Lithographic Process

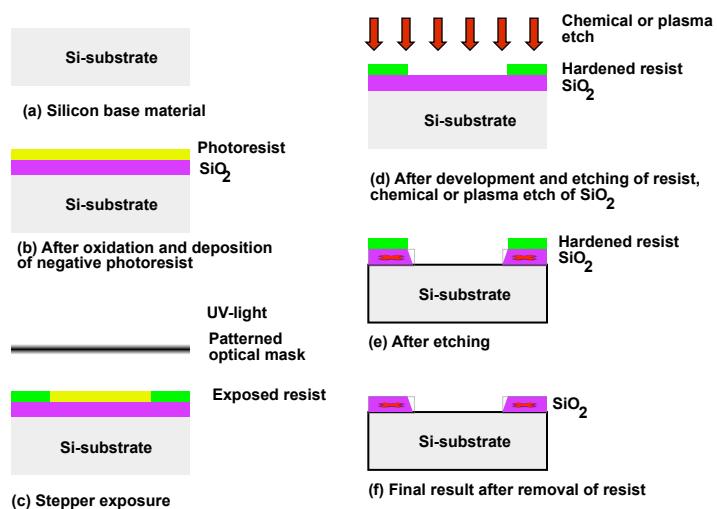


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## Patterning of $\text{SiO}_2$

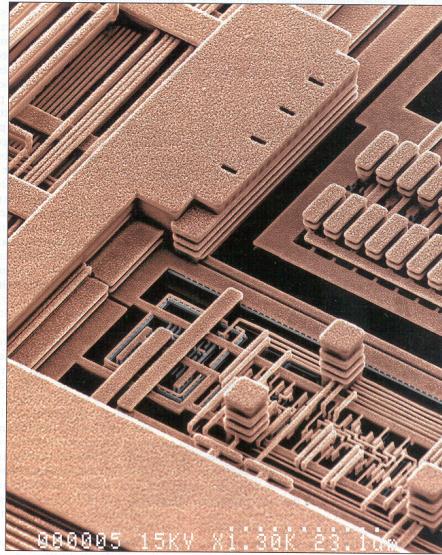
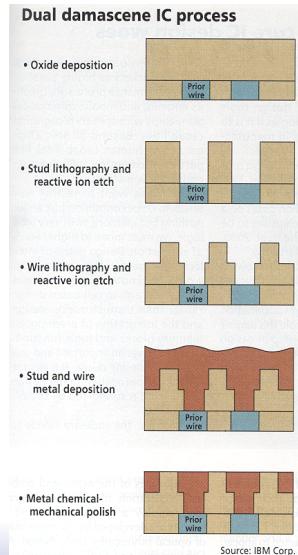


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## Advanced Metallization

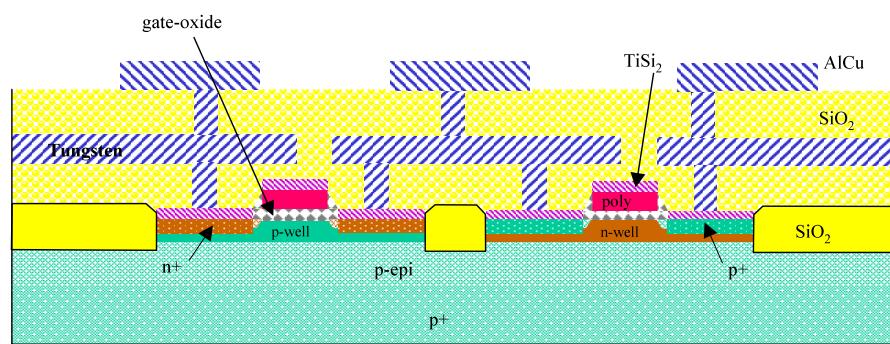


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## A Modern CMOS Process



Dual-Well Shallow-Trench-Isolated CMOS Process

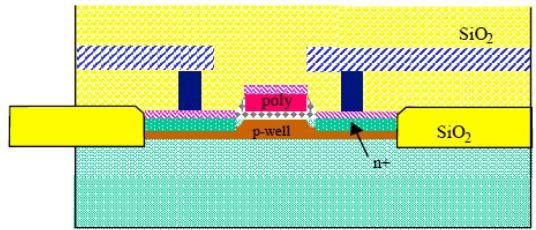
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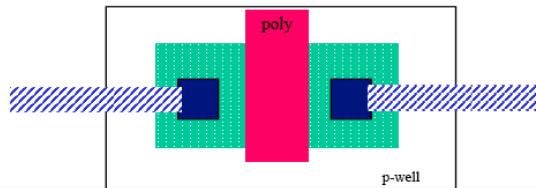
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## Transistor Layout

Cross-Sectional View



Layout View



## Back to Cost

- ❑ NRE (non-recurrent engineering) costs - fixed
  - Independent of volume (i.e., number of units made/sold)
  - Examples: design time and effort, mask generation, equipment, etc.
  
- ❑ Recurrent costs - variable
  - proportional to volume
  - Examples: silicon processing, packaging, test
  - Most of these proportional to chip area

## NRE Cost is Increasing

**Exploding NRE / Mask Costs**

"The club of people who can afford an extreme sub-micron ASIC or COTS design is getting pretty exclusive."  
Ron Wilson, EE Times (May 2000)

70nm ASICs will have \$4M NRE

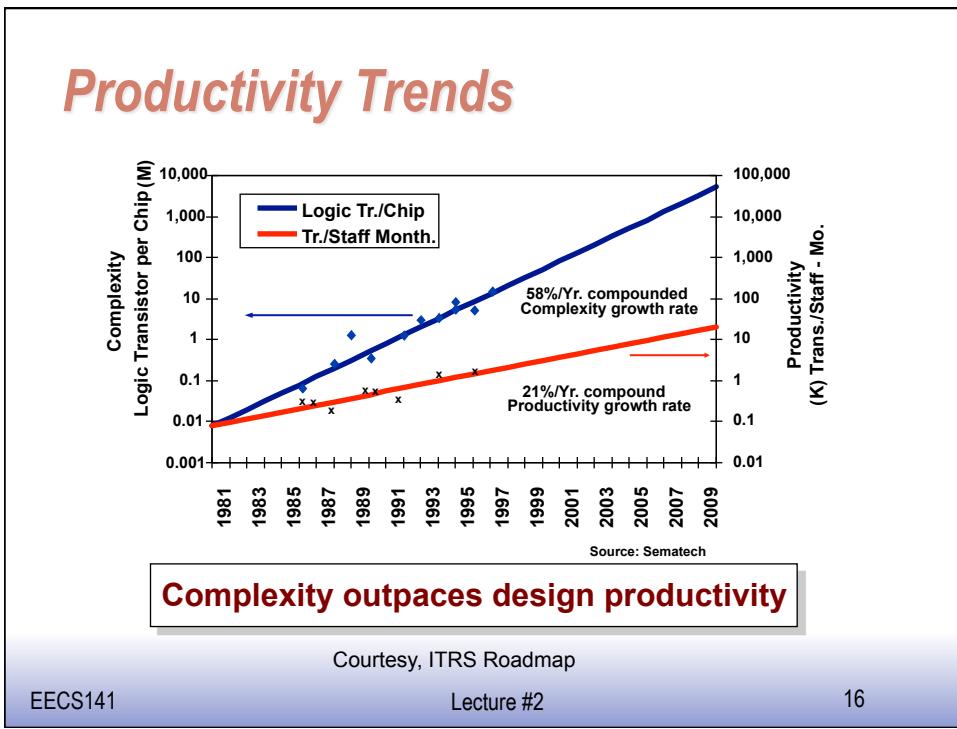
www.InnovationRevolution.com

ATI, Mentor, XILINX

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## Total Cost

### ❑ Cost per IC

$$\text{cost per IC} = \underbrace{\text{variable cost per IC}}_{\downarrow} + \frac{\text{fixed cost}}{\text{volume}}$$

### ❑ Variable cost

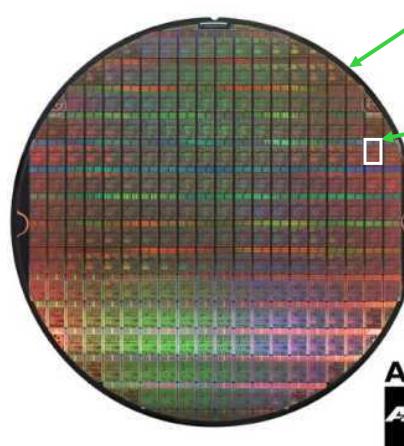
$$\text{variable cost} = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}$$

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## Die Cost



$$\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} * \text{die yield}}$$



From: <http://www.amd.com>

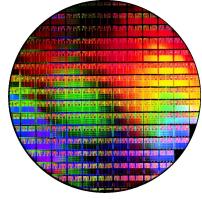
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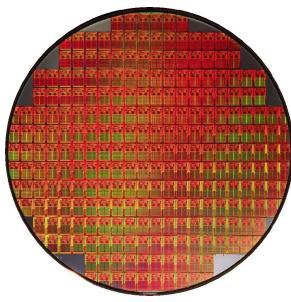
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## Wafer size

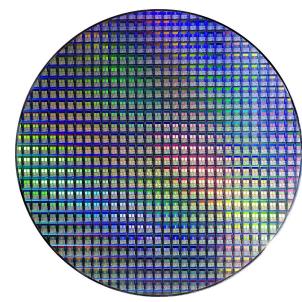
AMD Athlon



8" (200mm)  
90nm CMOS



12" (300mm)  
90nm CMOS



12" (300mm)  
65nm CMOS

Next: 18" Wafers?

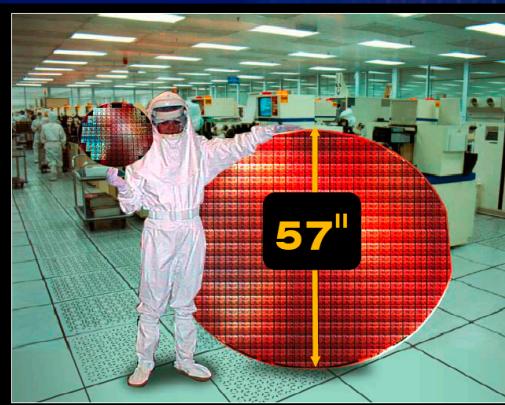
From: <http://www.sandpile.org>

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## Projected 2000 Wafer, circa 1975



Moore was not always accurate

G. Moore, Keynote Address ISSCC 2003

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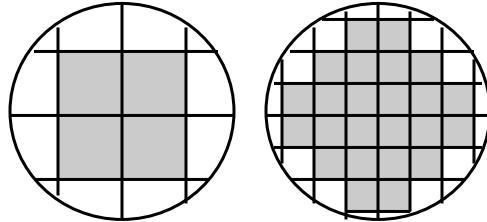
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## Yield

$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}$$



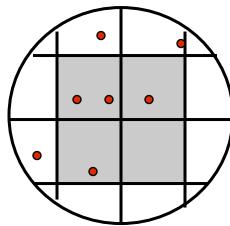
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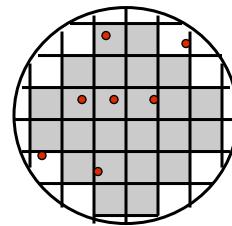
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## Defects

$$\text{Yield} = 1/4$$



$$\text{Yield} = 19/24$$



$$\text{die yield} = \left( 1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}, \text{ where } \alpha \text{ is approximately 3}$$



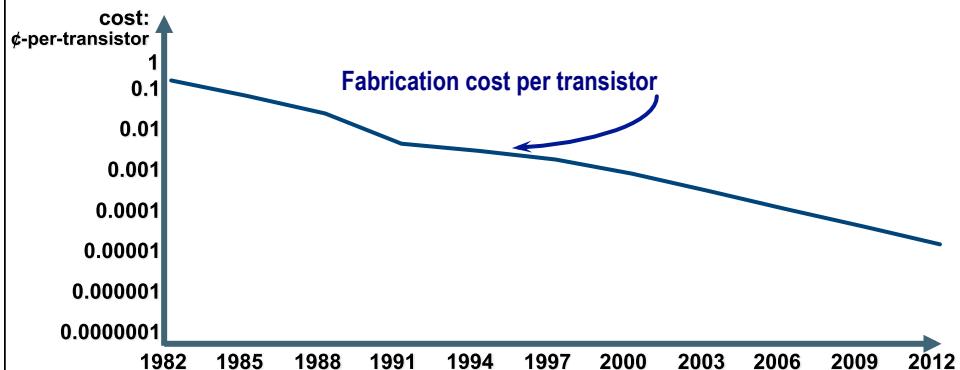
$$\text{die cost} \propto \frac{1}{[(\text{die/wafer} \propto \text{die area}^{-1})(\text{yield} \propto \text{die area}^{-3})]} \propto \text{die area}^4$$

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## Cost per Transistor



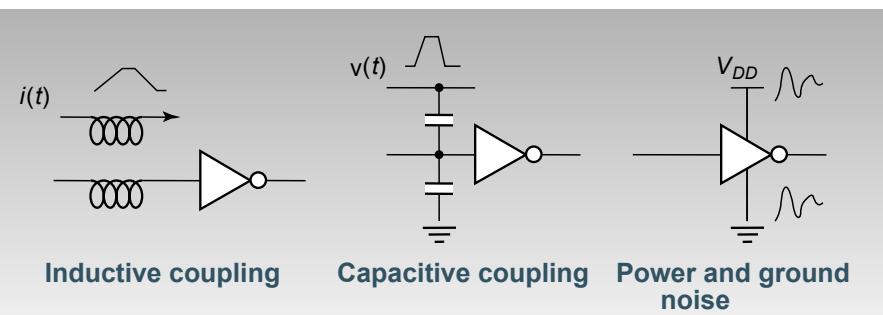
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## Reliability

- The real world is analog
  - All physical quantities you deal with as a circuit designer are actually continuous
- Thus, even a “digital” signal can be noisy:



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## Noise and Digital Systems

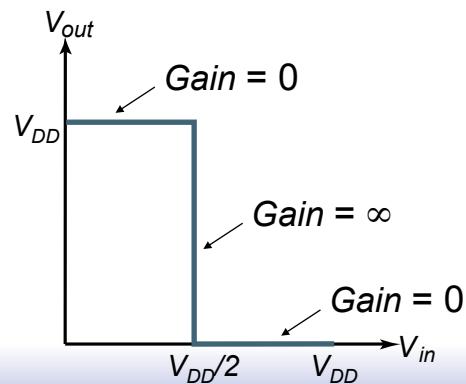
- Circuit needs to work despite “analog” noise
  - Digital gates can reject noise
  - This is actually how digital systems are defined
  
- Digital system is one where:
  - Discrete values mapped to analog levels and back
  - All the elements (gates) can reject noise
    - For “small” amounts of noise, output noise is less than input noise
  - Thus, for sufficiently “small” noise, the system acts as if it was noiseless

## Noise Rejection

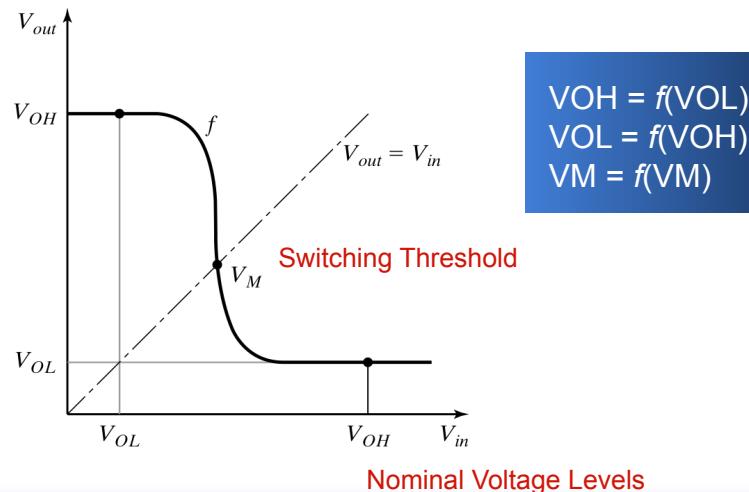
- To see if a gate rejects noise
  - Look at its DC voltage transfer characteristic (VTC)
  - See what happens when input is not exactly 1 or 0

- Ideal digital gate:

- Noise needs to be larger than  $V_{DD}/2$  to have any effect on gate output



## More Realistic VTC

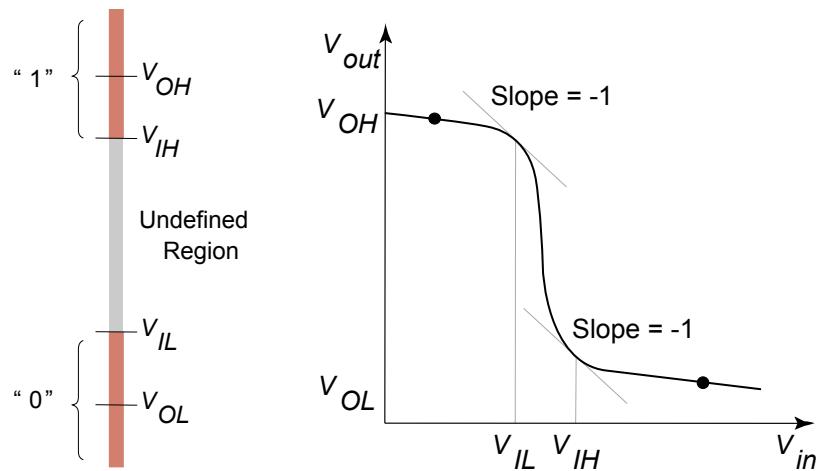


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## Voltage Mapping

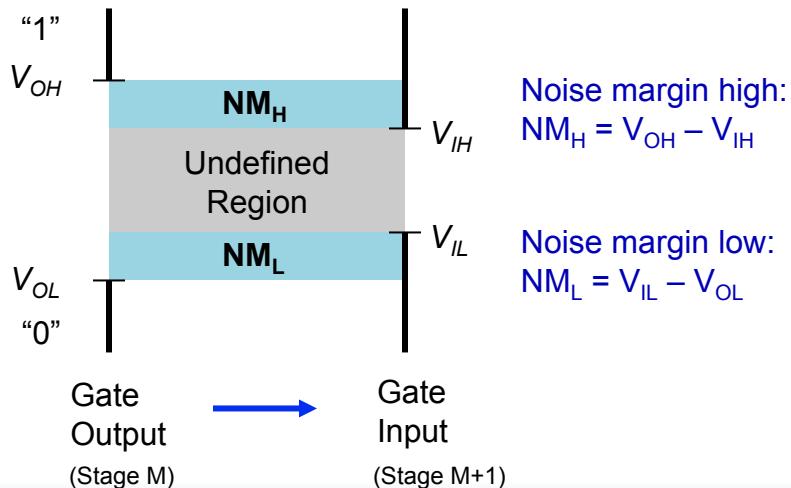


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## Definition of Noise Margins

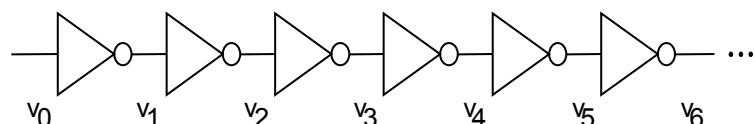


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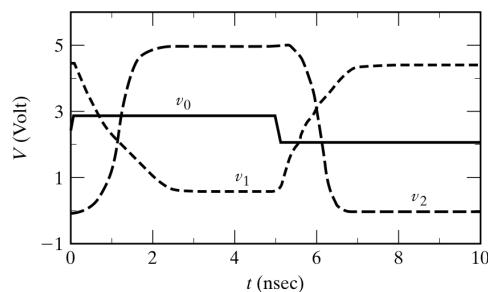
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## Digital Gate Noise Reduction: Regenerative Property



A chain of inverters



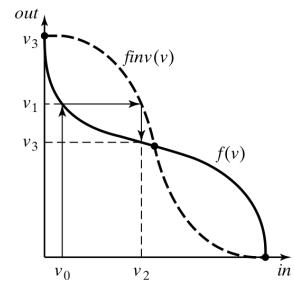
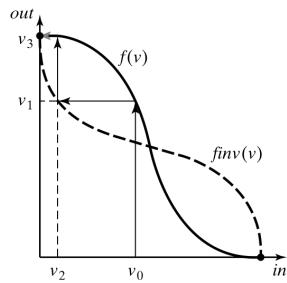
Simulated response

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## Regenerative Property (Another View)

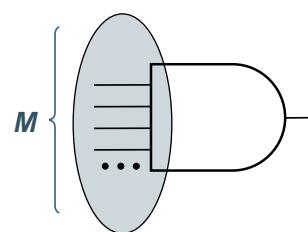
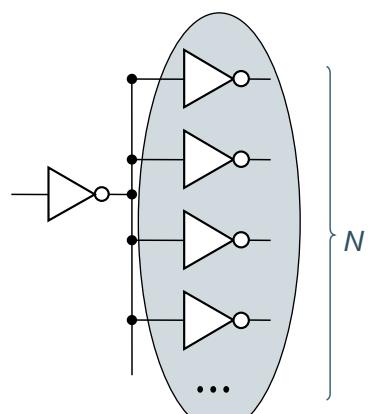


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## Fan-in and Fan-out



*There is a modified definition of fan-out for CMOS logic*

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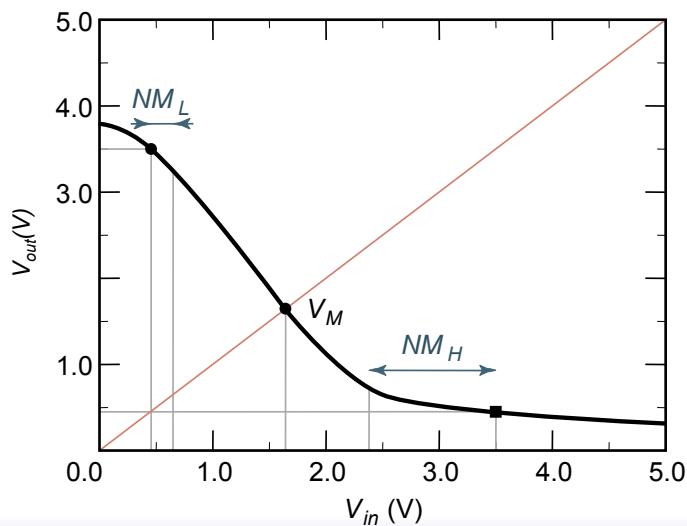
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## Key Reliability Properties

- ❑ Absolute noise margin values are not the only things that matter
  - e.g., floating (high impedance) nodes are more easily disturbed than low impedance nodes (in terms of voltage)
- ❑ Noise immunity (i.e., how well the gate suppresses noise sources) needs to be considered too
- ❑ Summary of some key reliability metrics:
  - Noise transfer functions & margin (ideal: gain =  $\infty$ , margin =  $V_{dd}/2$ )
  - Output impedance (ideal:  $R_o = 0$ )
  - Input impedance (ideal:  $R_i = \infty$ )

## Example: An Old-time Inverter



## ***Example: An Old-time Inverter***

- ❑  $V_{OH} = 3.6V$
- ❑  $V_{OL} = 0.4V$
- ❑  $V_{IL} = 0.6V$
- ❑  $V_{IH} = 2.3V$
- ❑  $NM_H = V_{OH} - V_{IH} = 1.3V$
- ❑  $NM_L = V_{IL} - V_{OL} = 0.2V$

## ***Summary***

- ❑ Understanding the design metrics that govern digital design is crucial
  - We discussed cost and reliability so far
- ❑ Key design messages so far:
  - Keep chip area as small as possible
  - Pick design styles and parameters so that noise margins are reasonable

## ***Next Lecture***

- ❑ Performance and energy
- ❑ A first glance at an inverter