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6:30-8:00pm

EECS 141: FALL 2001—MIDTERM 1

For all problems, you can assume the following transistor parameters (unless otherwise mentioned):
NMOS:
$V_{Tn} = 0.4$, $k'_n = 115\ \mu A/V^2$, $V_{DSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$
PMOS:
$V_{Tp} = -0.4V$, $k'_p = -30\ \mu A/V^2$, $V_{DSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\Phi_F = 0.6V$

NAME	Last First

GRAD/UNDERGRAD	

Problem 1: _____/ 8

Problem 2: _____/12

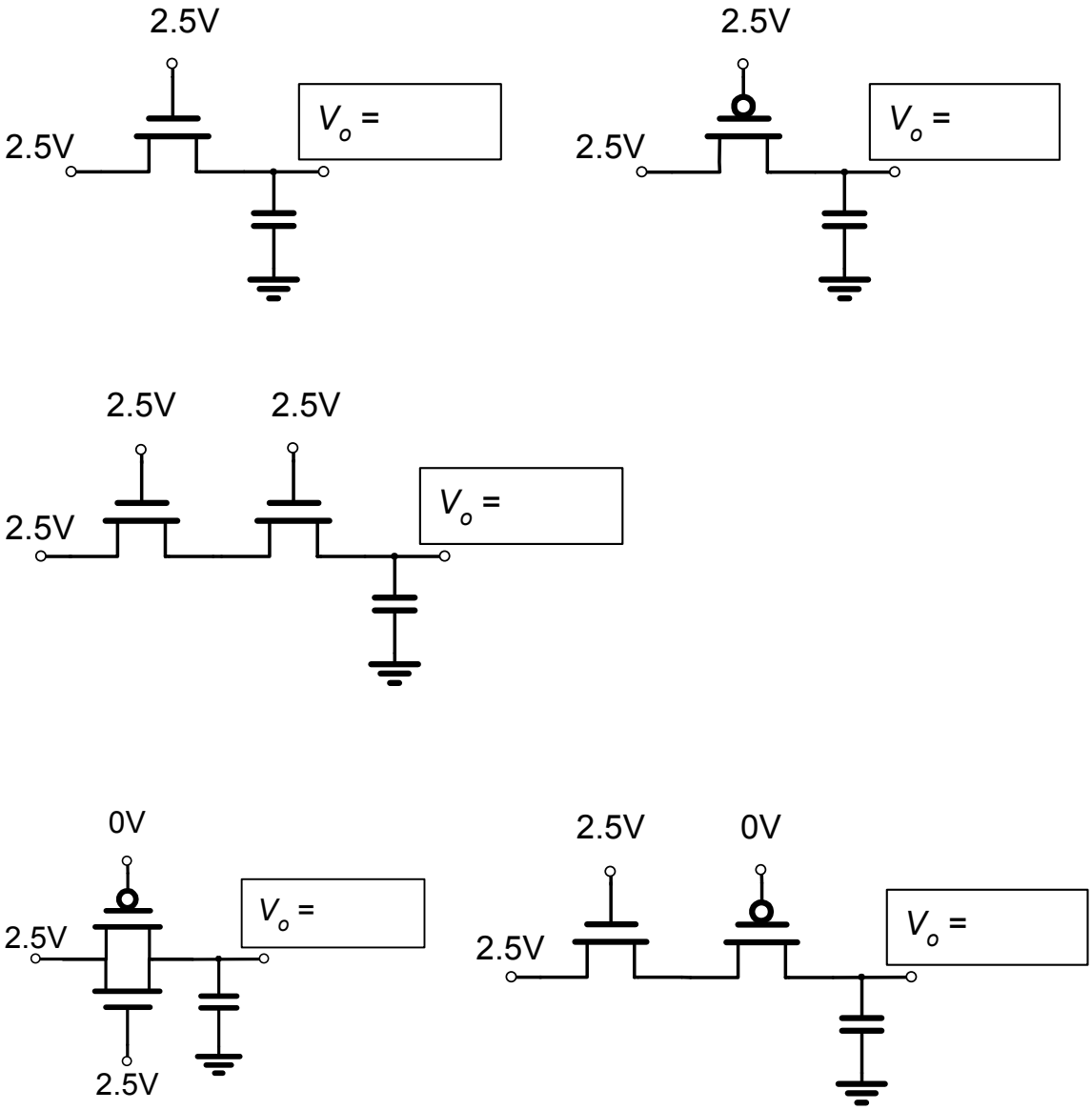
Problem 3: _____/12

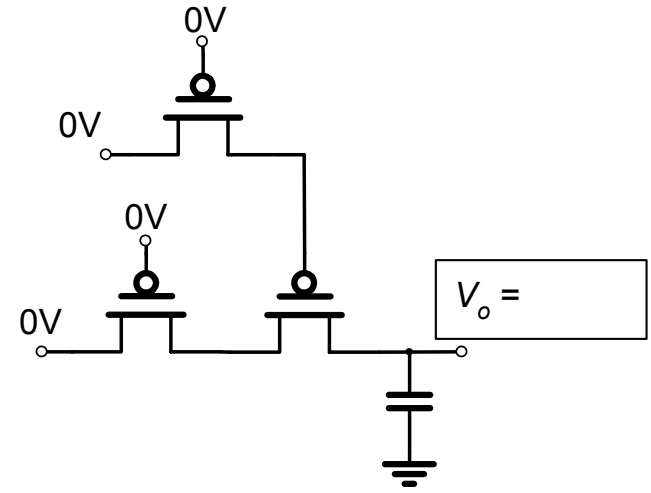
Problem 4: _____/12

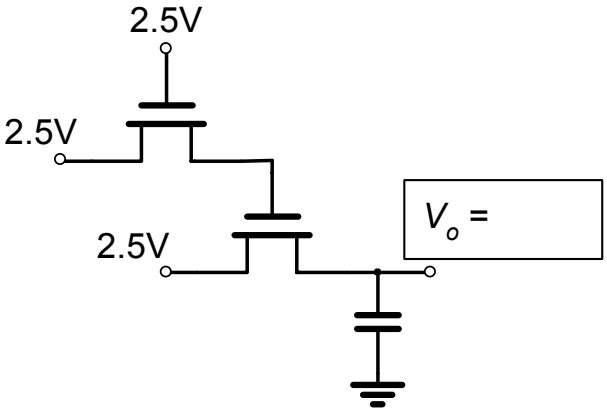
Total: _____/44

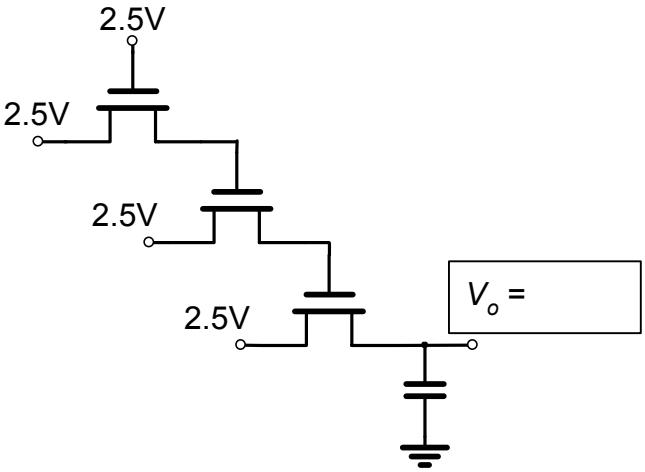
PROBLEM 1. MOS transistor as a switch

Find the final value of the voltage V_o. Assume $V_{TN} = |V_{TP}| = 0.5$V. Assume that the capacitor is initially discharged, and ignore subthreshold conduction and body effect.




0V
0V
0V
0V
V_o =


2.5V
2.5V
2.5V
V_o =


2.5V
2.5V
2.5V
2.5V
V_o =

PROBLEM 2. Equivalent RC models.
In class we modeled the inverter delay by finding its equivalent resistance and capacitance. You are asked to find the equivalent resistance and input capacitance of a capacitively loaded symmetrically sized inverter.

a) Draw a schematic of how you would measure the equivalent resistance and briefly explain how would you do this.

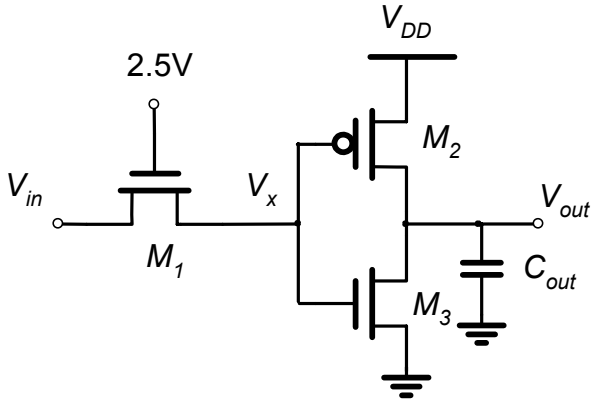
b) Draw a schematic of how you would measure the equivalent input capacitance of this inverter. Explain the measurement procedure.

c) Does the input capacitance of this inverter depend on its loading? Explain your answer.

d) Does the input capacitance of this inverter depend on the type of transition (H-L or L-H transition)? If the answer is yes, which one is larger? Explain your answer.

PROBLEM 3. Gate delays.

Consider a three-transistor circuit as shown in the figure below. V_{DD} = 2.5V and input signal switches between 0 and V_{DD} with sharp rise and fall times. Use the transistor parameters indicated on the first page of the midterm. Ignore body effect. All transistors are minimum length, L = 0.25µm. Transistor widths: W_2 = 2µm, W_1 = 1µm.



a) Find the M_3 transistor width such that the switching point of the inverter (V_M) is placed in the middle of the V_X signal swing.

b) Find the t_{pLH} delay of this circuit. C_{ox} = 6fF/μm^2. Overlap capacitances are C_o = 0.3 fF/μ. Bottom-plate PN junction capacitances are 2fF/μ (drain lengths are included). Ignore the sidewall capacitances. Ignore the impact of rise/afll times on propagation delay. C_{out} = 10fF.

PROBLEM 4. Wire modeling.
Consider an isolated 2mm long and 1um wide M1 wire over a silicon substrate driven by an inverter with zero output resistance and capacitance.

a) If the wire width is doubled, the delay of this wire will be (circle one):

More than 2x shorter / Exactly 2x shorter / Shorter, but less than 2x /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation:

b) If the wire length is halved, the delay of this wire will be (circle one):

More than 2x shorter / Exactly 2x shorter / Shorter, but less than 2x /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation:

c) If the wire thickness is doubled, the delay of this wire will be (circle one):

More than 2x shorter / Exactly 2x shorter / Shorter, but less than 2x /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation:

d) If the oxide thickness (between the wire and the substrate) is doubled, the wire delay will be (circle one):

More than 2x shorter / Exactly 2x shorter / Shorter, but less than 2x /
Unchanged /
Less than doubled / Exactly doubled / More than doubled

Explanation: