SAN JOSE STATE UNIVERSITY
Electrical Engineering Department

EE288 Data Conversions/Analog Mixed-Signal ICs

Spring 2018

Midterm Exam

Instructor: Sang-Soo Lee

Problem	Score	Max Score
1		5
2		5
3		5
4		5
5		5
6		5
Total		**30**

Name: _____

ID: _____

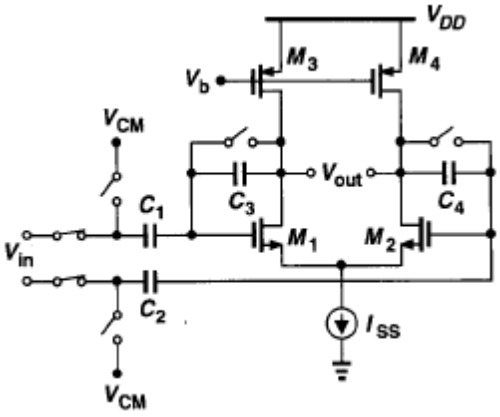
Problem 1 (5 points)

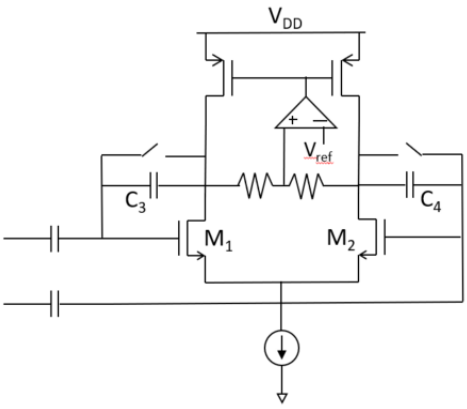
Consider the switched-capacitor circuit below, where the CMFB is not shown. Assume $(W/L)_{1\text{-}4}$ = 50/0.5. I_{ss} = 1mA., $C_1 = C_2$ = 2pF, $C_3 = C_4$ = 0.5pF, and the output common-mode level is 1.5V. Neglect the transistor capacitances. Assume $\lambda = 0.1\ V^{-1}$ and V_{dsat} = 0.2V for all transistors.

(a) Draw a common-mode feedback circuit that can work with the main amplifier on the right side of the circuit and explain the operation of the CMFB loop.

(b) Calculate the open loop gain of the amplifier.

(c) Calculate the gain error of the closed-loop SC amplifier.





Open loop gain

$A = g_{m1}\, r_{out}$

$= g_{m1}\, (r_{o1} \,//\, r_{o3})$

$= (2I / V_{dsat})\, [1 / (\lambda_n I + \lambda_p I)]$

$= (2 / V_{dsat})\, [1 / (\lambda_n + \lambda_p)]$

$= (2 / 0.2)\, (1 / 0.2) = 50$

Gain error of the switched-capacitor circuit is $1/\beta A$

$\beta = C_3 / (C_1 + C_3)$

$= 0.5 / (2 + 0.5)$

$= 1/5$

$1/\beta A = 5/50 = 0.1$

Problem 2 (5 points)

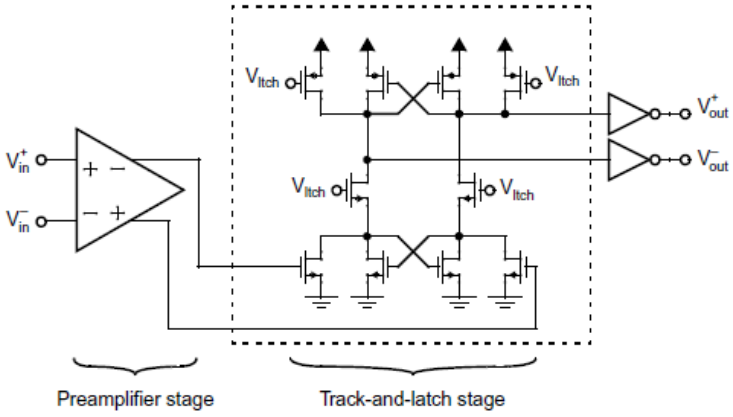
The following latched comparator has been designed for a 10-bit ADC running at 100MHz sampling rate. The preamp has a differential pair with W/L = 2(1.6um/0.2um). Assume there is 10mV latch offset and the offset of the preamp is dominated by the differential pair mismatch.

(a) Calculate the offset of the preamp using Pelgrom's model. Assume A_{vt} = 2.4mV·um.

(b) Determine the gain of the preamp to achieve 5mV overall input referred offset.

(c) Suggest a preamplifier circuit to achieve the gain you calculated in (b). Clearly show the size for the appropriate transistors in the suggested circuit. Assume $\mu_n = 200\mu A/V^2$ and $\mu_p = 100\mu A/V^2$.

(d) What is the gain you can achieve with the regenerative latch if V_{latch} is high during 80% of the half clock period for the latch regeneration? Assume the latch regeneration time constant is 0.5ns.



Offset of the preamp caused by the differential pair mismatch

V_{os} = A_{vt} / sqrt(WL)
= 2.4mV / sqrt(2x1.6x0.2)
= 2.4mV / 0.8
= 3 mV

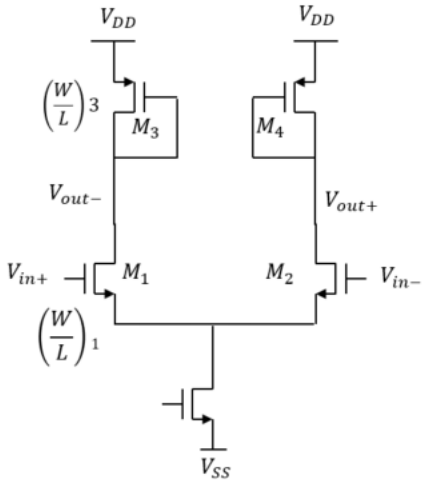
Overall input referred offset

$V_{os}^2 = V_{os\_preamp}^2 + (V_{os\_latch}/A)^2$
$5mV^2 = 3mV^2 + (10mV/A)^2$
A = 2.5

Gain of the regenerative latch

80% of the half clock = 0.8 x 5ns = 4ns
Time constant τ = 0.5ns
Gain = exp(t/τ) = exp(4ns/0.5ns) = exp(8) = 2981

Preamplifier circuit and the size calculation



$$Gain = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}_{M1} I_{D1}}}{\sqrt{2\mu_p C_{ox}\frac{W}{L}_{M3} I_{D3}}} = \frac{\sqrt{200\frac{W}{L}_{M1}}}{\sqrt{100\frac{W}{L}_{M3}}} = \frac{\sqrt{2\frac{W}{L}_{M1}}}{\sqrt{\frac{W}{L}_{M3}}} = 2.5$$

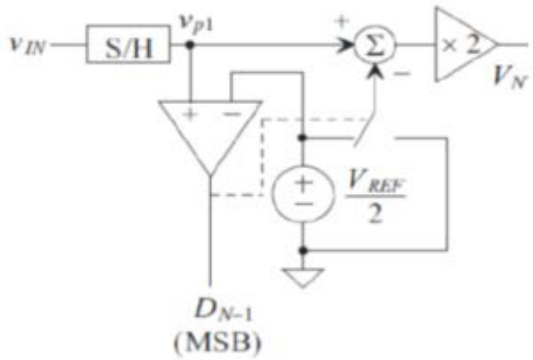
$$2\frac{W}{L}_{M1} = \frac{W}{L}_{M3}(2.5)^2$$

$$\frac{W}{L}_{M1} = 3.125\,\frac{W}{L}_{M3}$$

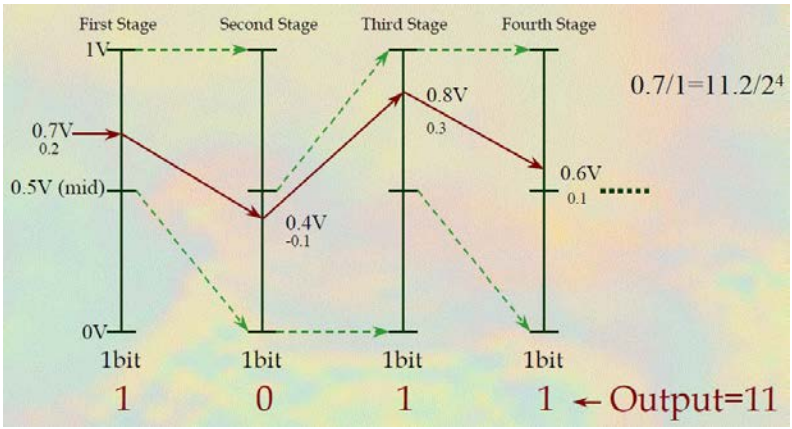
Problem 3 (5 points)

You are building a 4-bit pipelined ADC based on 1-bit per stage architecture. Assume the Full-scale input signal range is 0 ~ 1V, and Vrefp=1V and Vrefm=0V.

(a) Sketch the 1-bit/stage circuit using ideal components and describe how the pipeline stage works.



(b) Assume an input signal of 0.7V. Provide analog and digital output values for each and every stage for the 4-bit ADC. Analog values should be between 0V and 1V, and the digital values should be either 0 or 1.



Problem 4 (5 points)

Spectral testing has been performed on a 12-bit ADC by using a 3MHz full-scale sinusoidal input, sampling frequency of 10MHz, and 1024-point FFT. Use below spectral plot to answer the followings.

(a) Draw the input signal tone on the spectral plot below assuming no windowing required.
(b) Compute the ideal SQNR for this ADC.
(c) By raising the chip temperature and re-measuring the SNR, the effect of thermal noise is estimated as 5dB extra SNR degradation at the ambient temperature. Find the overall SNR at the ambient temperature.
(d) Using the SNR result found in c), find the value for the noise floor level shown as Y[dB] on the spectral test graph.
(e) Due to sampling without an antialiasing filter, aliased second and third harmonics showed up in the plot. Assuming the aliased second harmonic is -79dBFS and the third harmonic is -72dBFS, plot the aliased tones in the graph.

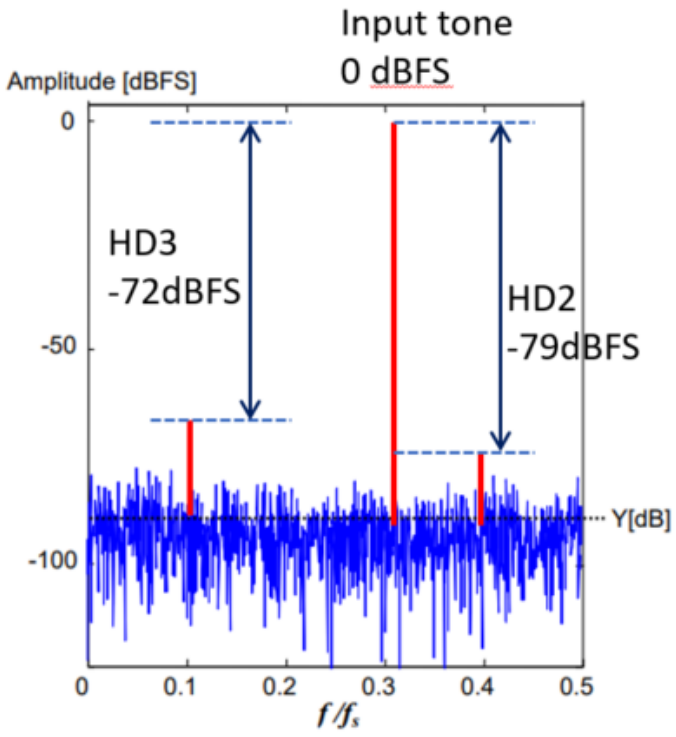
Input freq = 3MHz, Sampling freq = 10MHz $\rightarrow$ $f_{in}/f_s = 3/10 = 0.3$

SQNR = 6.02 N + 1.76 = 6.02 x 12 + 1.76 = 74 dB

SNR = 74 – 5 = 69 dB

Noise floor

Y[dB] = –69 – 10 log $[2^N/2]$ = –69 – 10 log(1024/2) = –69 – 27 = –96 dB



Problem 5 (5 points)

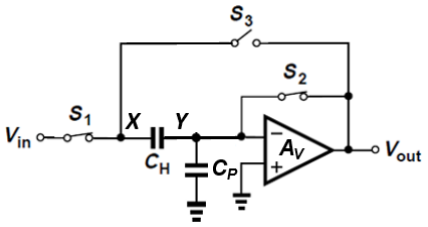
For the flip-around S/H circuit shown below,

(a) Explain where the bottom plate of the capacitor C_H should be connected to. X or Y?

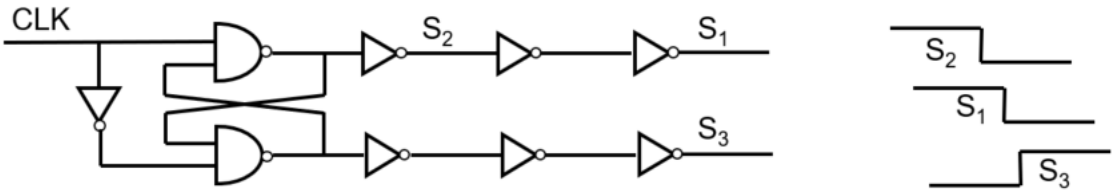
(b) Provide a clock generation circuit to control the switches S_1, S_2, and S_3 based on bottom plate sampling scheme.

(c) What is the feedback factor during the hold mode?

(d) Derive the closed-loop gain expression (V_{out}/V_{in}) using the charge conservation method.



Bottom plate usually has higher parasitic capacitance. Therefore, we should connect the bottom plate to X to reduce the summing node capacitance. This will increase the feedback factor of the Switched-Capacitor circuit.



$\beta = C_H / (C_H + C_P)$

Charge conservation during Ø1 and Ø2

During Ø1, total charge at summing node is $Q1 = C_H(0-V_{in})$

During Ø2, total charge at summing node is $Q2 = C_pV_Y + C_H(V_Y-V_{out})$

Let Q1 = Q2

$-V_{in}C_H = C_pV_Y + C_H(V_Y-V_{out}) = (C_p + C_H)V_Y - C_HV_{out}$

$V_Y(-A_{v1}) = V_{out}$

$-V_{in}C_H = (C_p + C_H)(-V_{out}/A_{v1}) - C_HV_{out}$

$V_{in}C_H = (C_p + C_H)(V_{out}/A_{v1}) + C_HV_{out}$

$V_{in}C_H = [(C_p + C_H)/A_{v1} + C_H]V_{out}$

$V_{in} = [(C_p + C_H) / (C_HA_{v1}) + 1]V_{out}$

$V_{out}/V_{in} = 1 / [(C_p + C_H) / (C_HA_{v1}) + 1] = 1 / [1 + 1/(\beta A_{v1})]$

Problem 6 (5 points)

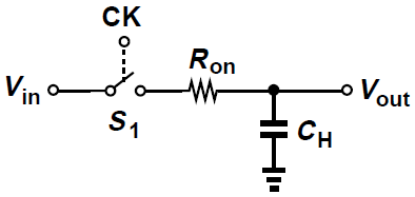
Consider the following sampling circuit with an ideal switch S_1, where R_{on}=400 Ω . The circuit has been designed for a 10-bit system with Full Scale = 1V.

(a) How large should we choose the value of the sampling capacitance C_H so that the rms noise from the sampler is equal to 0.25LSB of the ADC at T = 27°C? K=1.38x10^{-23}.

(b) Compared to the case where only quantization noise is present, how much is the overall SNR degraded by the kT/C noise?

(c) If the clock CK has a 50% duty cycle, calculate the maximum clock frequency at which inputs between 0~1V can be sampled to within 1/2 LSB accuracy at 10-bit resolution? Assume the sampling capacitance C_H =1pF.

(d) The switch has been implemented with an NMOS. What are the other factors affecting the accuracy of this sampling circuit?



(a) rms noise variance is KT/C

1 LSB = $V_{FS}/2^N = 1/2^{10} = 1/1024 = \Delta$

sqrt(KT/C) = Δ / 4 = 1 / (4 x 1024)

C = KT / (1/ (4x1024))^2 = 1.38 x 10^{-23} x 300 x 16 x 1024^2 = 69.5 fF

(b) Original SNR = 10 log (Signal Power / Quantization Noise)

New SNR = 10 log [Signal Power / (Quantization Noise + KT/C)]

Original SNR – New SNR

= 10 log (Quantization Noise + KT/C) / Quantization Noise)

= 10 log [(Δ^2/12 + (Δ/4)^2) / (Δ^2/12)]

= 10 log [(1/12 + 1/16) / (1/12)]

= 10 log (1 + 12/16)

= 2.43 dB

(c)Error = V_{FS} exp(-t/ τ) = Δ/2 = (V_{FS} /2^N)/2 → t = τ ln (2^{N+1})

τ = RC = 400Ω x 1pF = 4 x 10^{-10}

t = τ ln (2^{11}) = 7.62 τ = T_{max} / 2 = 1/(2 x f_{max})

f_{max} = 1/(2 x 7.62 x 4 x 10^{-10}) = 164 MHz

(d)NMOS sampling circuit will have signal dependent nonlinearity, charge injection and clock feedthrough error.