Transistor Sizing

Lecture 5

- Rule: Select W/L ratio to provide the gate with same current-driving capability in both directions equal to that of basic inverter
- Basic inverter

$$\begin{cases} \left(\frac{W}{L}\right)_n = n \quad \text{typically} \quad n = 1 \\ \left(\frac{W}{L}\right)_p = p \quad \text{typically} \quad p = 1.5 \end{cases}$$

- For match design $\frac{p}{n} = \frac{\mu_n}{\mu_p}$ typical $p = 2n$ and for minimum area $p = n$

- Network Equivalent W/L ratio:
- Rational :

$$R_{on} = \frac{\text{Constant}}{\frac{W}{L}}$$

- Transistor Series Connection

$$R_{series} = R_{on1} + R_{on2} + ... = \frac{\text{Constant}}{\left(\frac{W}{L}\right)_1} + \frac{\text{Constant}}{\left(\frac{W}{L}\right)_2} + \cdots$$

$$R_{series} = \text{Constant}\left[\frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2} + ...\right] = \frac{\text{Constant}}{\left(\frac{W}{L}\right)_{eq}}$$

- Network Equivalent W/L ratio:

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2} + \ldots\ldots\ldots\ldots}$$

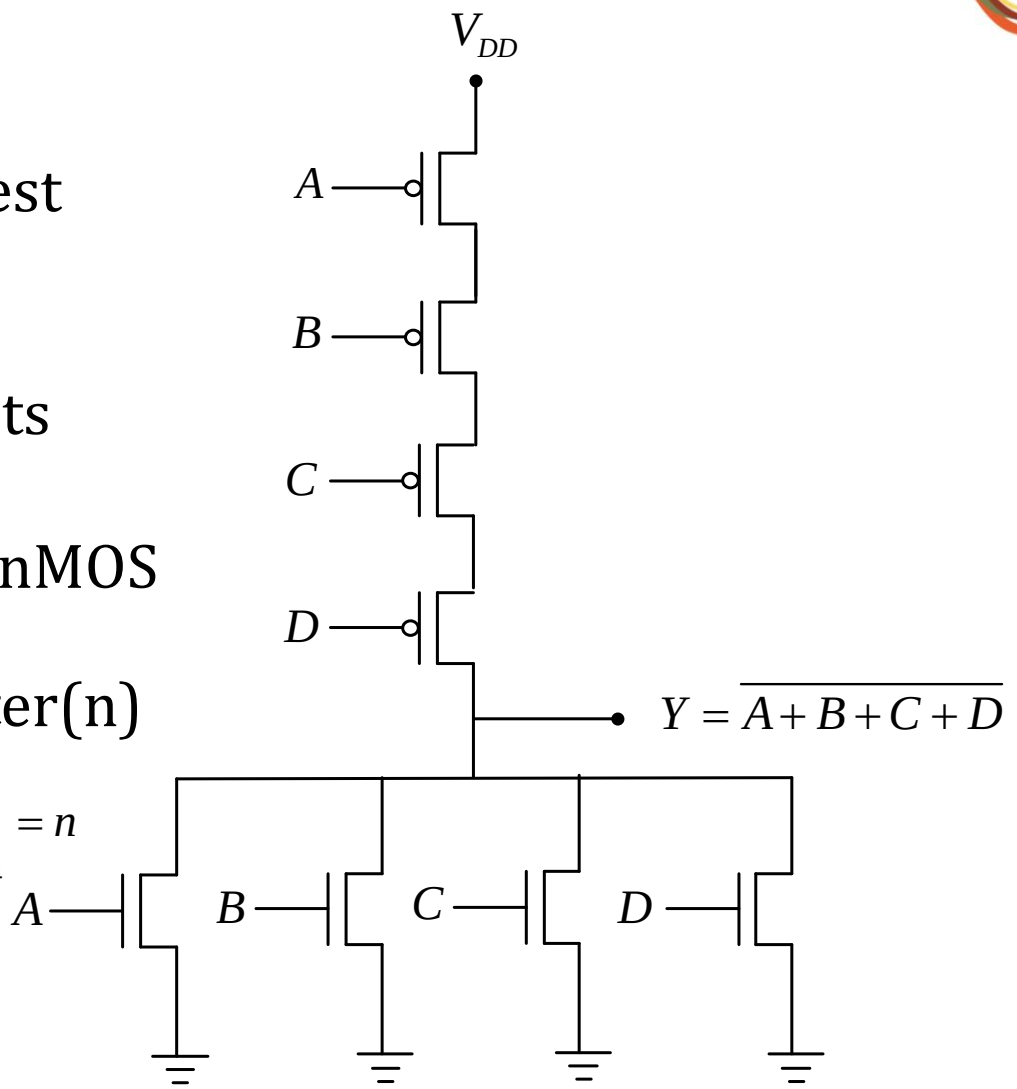
Transistor series connection

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + \ldots\ldots\ldots\ldots$$

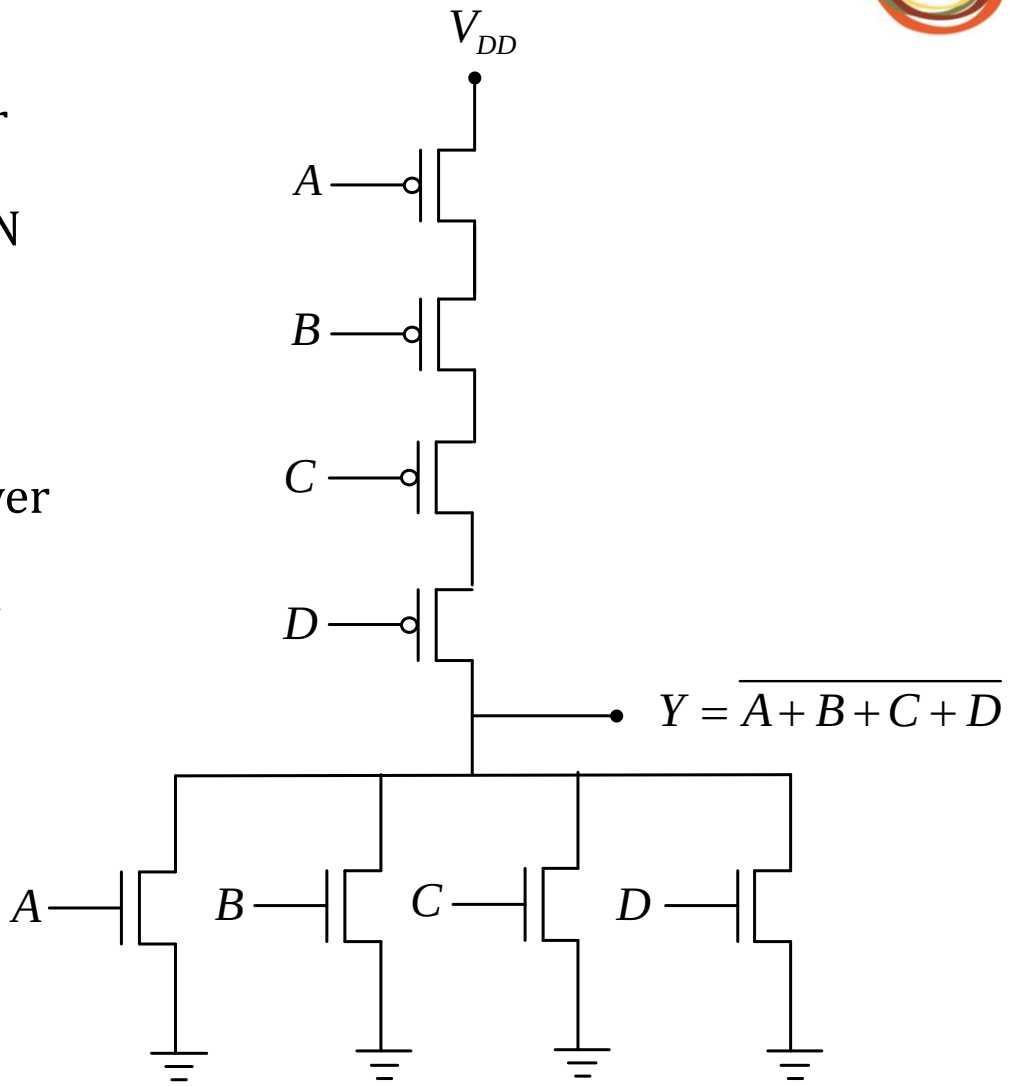
Transistor parallel connection

- Example
- Four-input Nor Gate
- Worst case(The lowest current) for PDN
- Only one of nMOS transistor is on(inputs high)
- Select the $\frac{W}{L}$ of each nMOS equal to that of the nMOS of basic inverter(n)

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = n$$



- Example
- Four-input Nor Gate
- Worst Case (stacked pMOS) for PUN
- Four series pMOS transistor ON (inputs low)
- Select the $\frac{W}{L}$ of each pMOS transistor equal to 4 times of pMOS of basic inverter(4p)
- Note: pMOS devices have a lower mobility relative to nMOS devices. Stacking pMOS should be avoided.
- (NAND implementation preferred over a NOR implementation for implementing generic logic.)



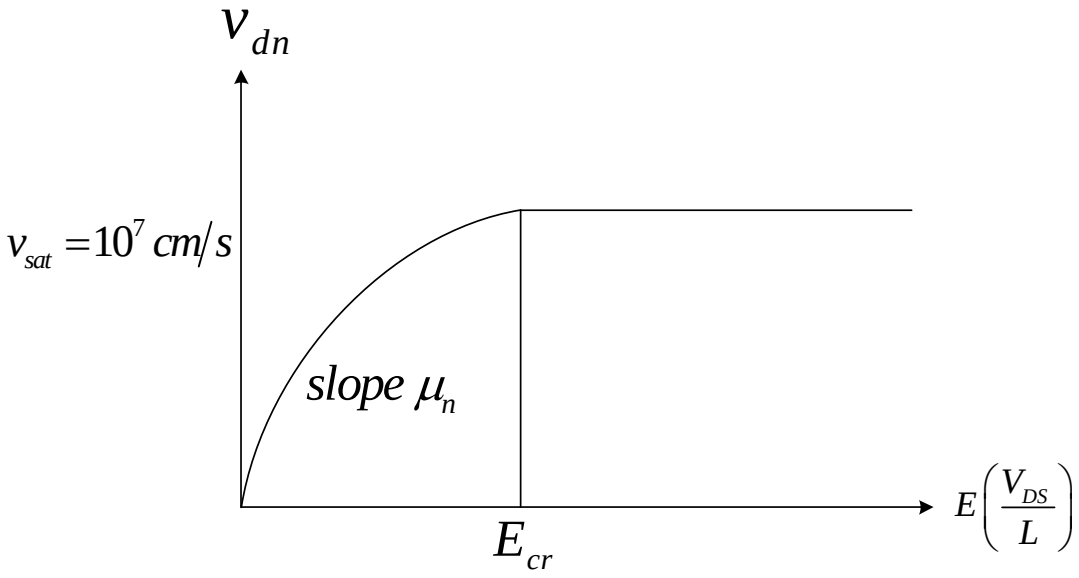
- Short channel velocity saturation

$$1\frac{V}{\mu m} < \text{typical } E_{cr} < 5\frac{V}{\mu m}$$

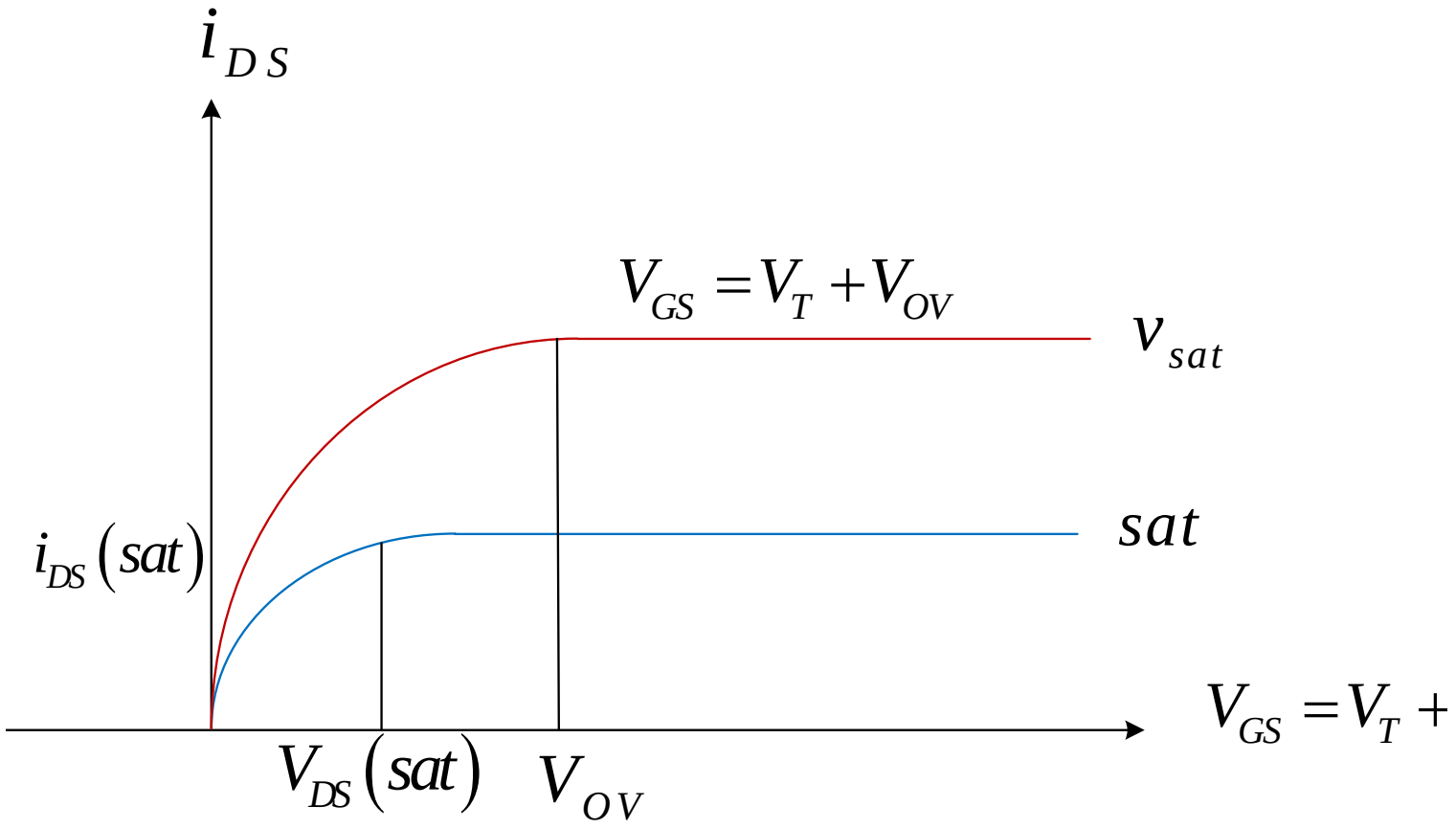
$$E_{cr} = \frac{V_{DS}(v_{sat})}{L}$$

$$v_{sat} = \mu_n \frac{V_{DS}(v_{sat})}{L}$$

$$V_{DS}(v_{sat}) = \frac{L}{\mu_n} v_{sat}$$



- Ids vs. Vds Characterstic



- Ids vs. Vds Characterstic

$$I_{DS}(resistive) = \mu_n C_{ox} \frac{W}{L} \nu_{DS} \left[(V_{GS} - V_T) - \frac{1}{2} V_{DS} \right]$$

$$V_{DS} = V_{OV} = V_{GS} - V_T \quad for\ I_{DS}(sat)$$

$$I_{DS}(\text{Edge of Sat}) = \mu_n C_{ox} \frac{W}{L} V_{DS}(sat) \left[V_{GS} - V_T - \frac{1}{2} V_{DS}(sat) \right]$$

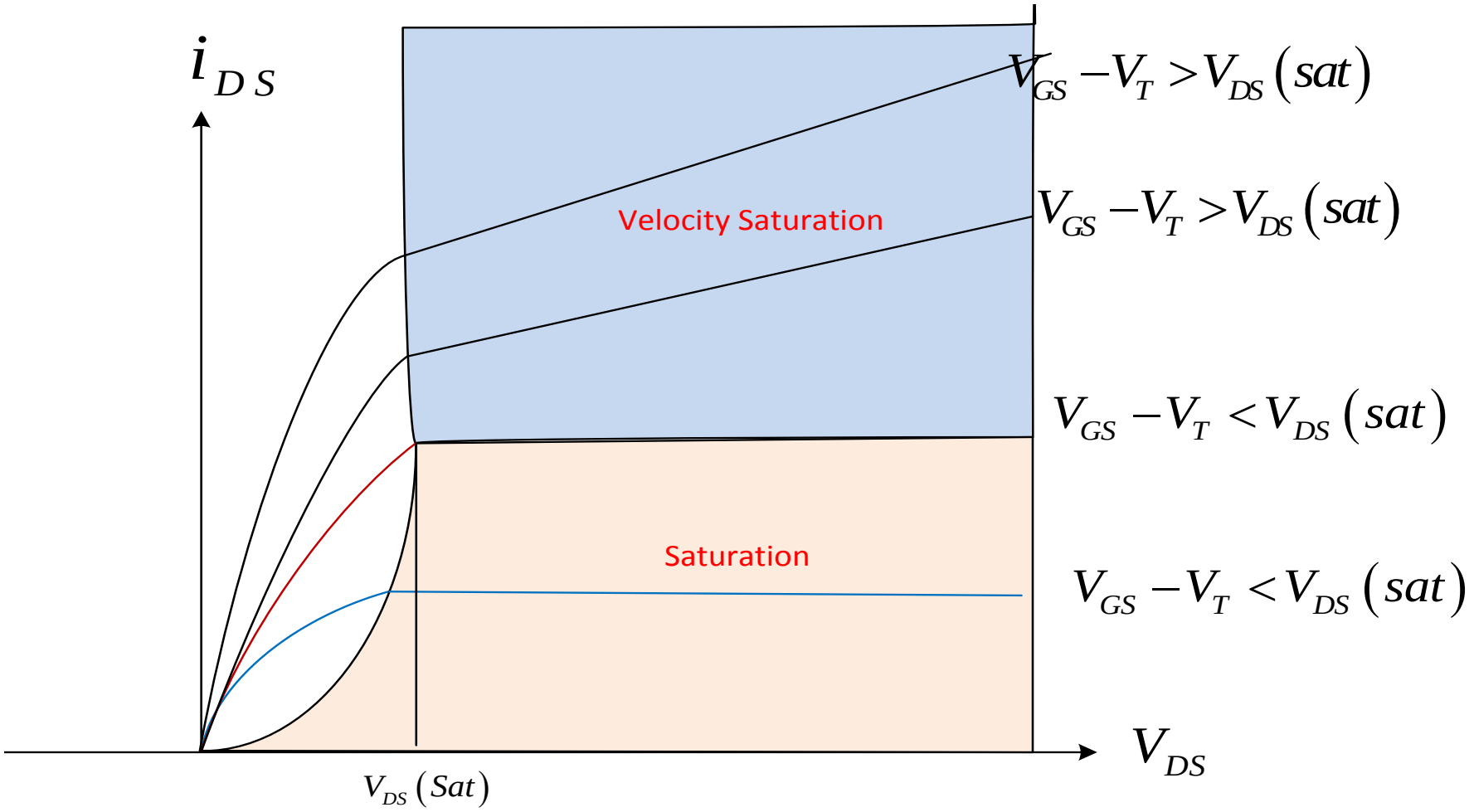
$$V_{ov} > V_{DS}(sat)$$

$$I_{DS}(\text{Edge of Sat}) = \mu_n C_{ox} \frac{W}{L} V_{DS}(sat) \left[V_{GS} - V_T - \frac{1}{2} V_{DS}(sat) \right]$$

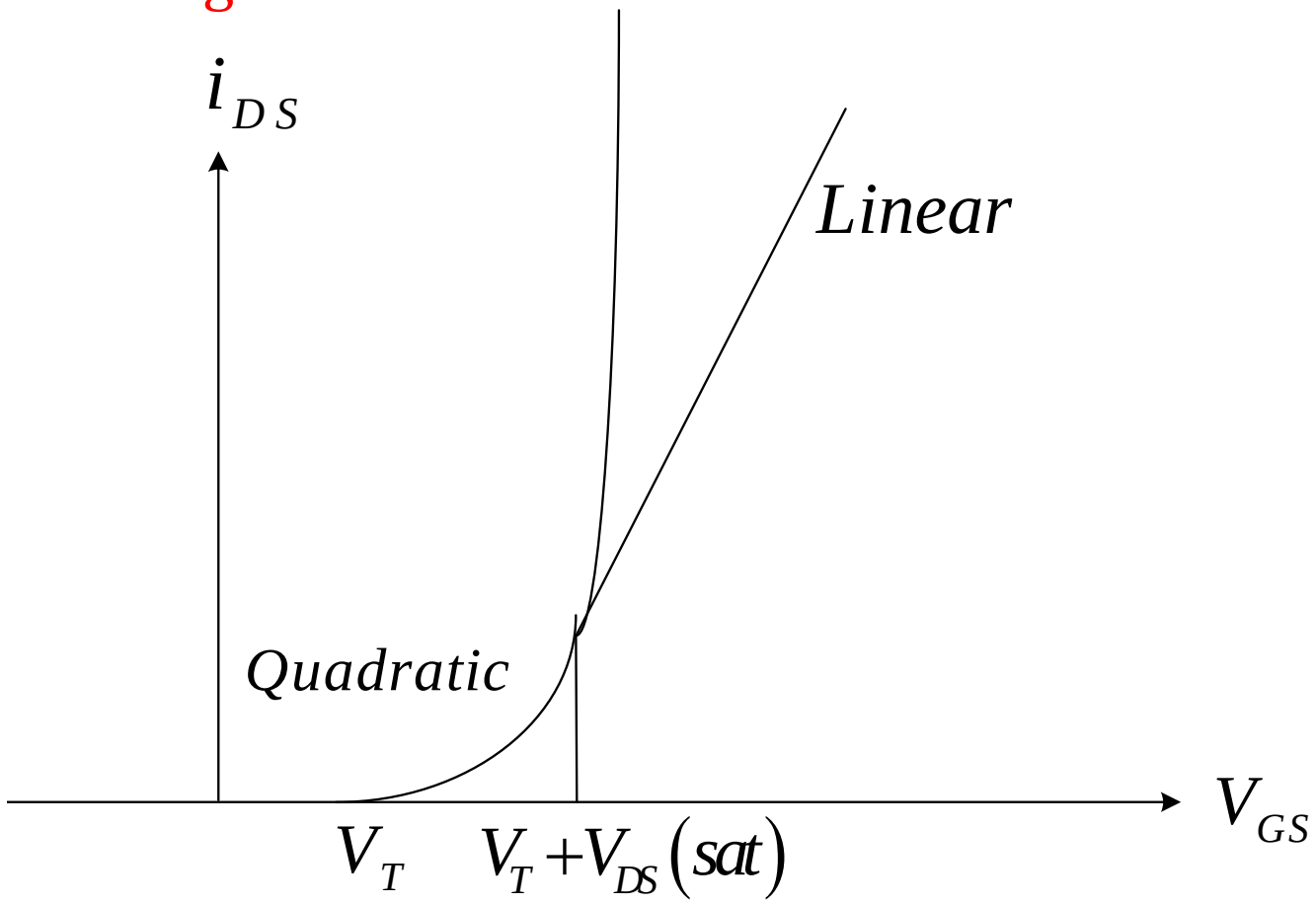
$$I_{DS}(\text{Edge of Sat}) = C_{ox} W \nu_{sat} \left[V_{GS} - V_T - \frac{1}{2} V_{DS}(\nu sat) \right]$$

$$I_{DS}(\text{Sat}) = \mu_n C_{ox} \frac{W}{L} \nu_D(sat) \left[V_{GS} - V_T - \frac{1}{2} V_{DS}(\nu sat) \right] (1 + \lambda V_{DS})$$

- Ids vs. Vds Characterstic



- Ids vs. Vgs Characterstic



- Effects of Fan-in and Fan-out on propagation delay.
- Observation: Each additional input to CMOS gate requires two additional transistor, one nMOS and one pMOS.
  - Increase chip area
  - Increase the total effective capacitance per gate
  - Increase propagation delay
- Fan-in limited to 4

- Special need Alternatives
- ❶ Pseudo – nMOS logic
- Replace PUN in a CMOS by a single permanently on pMOS transistor
- Advantage: Reduction in transistor count(area)
- Disadvantage: static power dissipation V_{OL} dependence on the $\frac{W}{L}$ ratio.
- ❷ Pass transistor logic(PTL)
- MOS transistor as switch in the series path from input to output.
- Disadvantage: Signal level degradation.

- Special need Alternatives
- ❸ ECL Emitter Coupled Transistor
- Bipolar logic circuit.

V_{OL}

$\frac{W}{L}$

- Summary of the implication of scaling the device dimension by a factor $\frac{1}{s}$ where s>1

Parameters	Scaling	Parameters
W, L, t_{ox}	$1/s$	
V_{DD}, V_T	$1/s$	
$Area$	$1/s^2$	WL
C_{ox}	s	ε_{OX}/t_{OX}
k_n', k_p'	s	$k_n' = \mu_n C_{OX}, k_p' = \mu_p C_{OX}$
C_{gate}	$1/s$	WLC_{OX}
t_p(intrinsic)	s	$\alpha C/k'V_{DD}$
$Energy$	$1/s$	CV_{DD}^2
P_{dyn}	$1/s^2$	$f_{\max} CV_{DD}^2 = CV_{DD}^2/2t_p$
$Power\ density$	1	$P_{dyn}/device\ area$

- Note: V_{DD} may not follow the scaling factor

$$V_{DD} = 5V \quad 0.5\mu m \ process$$

$$V_{DD} = 1.2V \quad 0.13\mu m \ process$$

- Note: V_T is not decreased with the same factor.