EE288 Data Conversions/Analog Mixed-Signal ICs
Spring 2018

Lecture 24: Oversampled ADC 2

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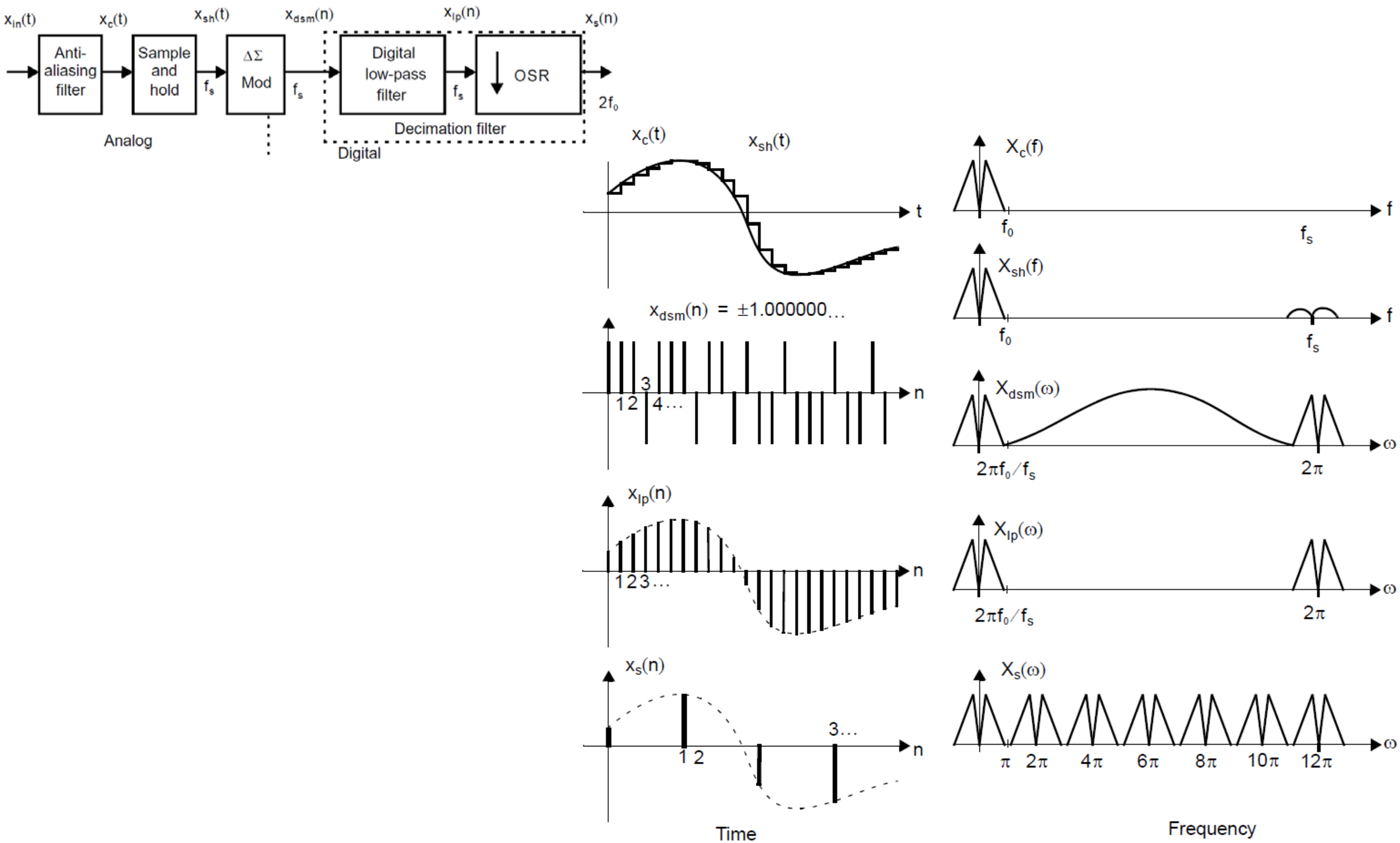
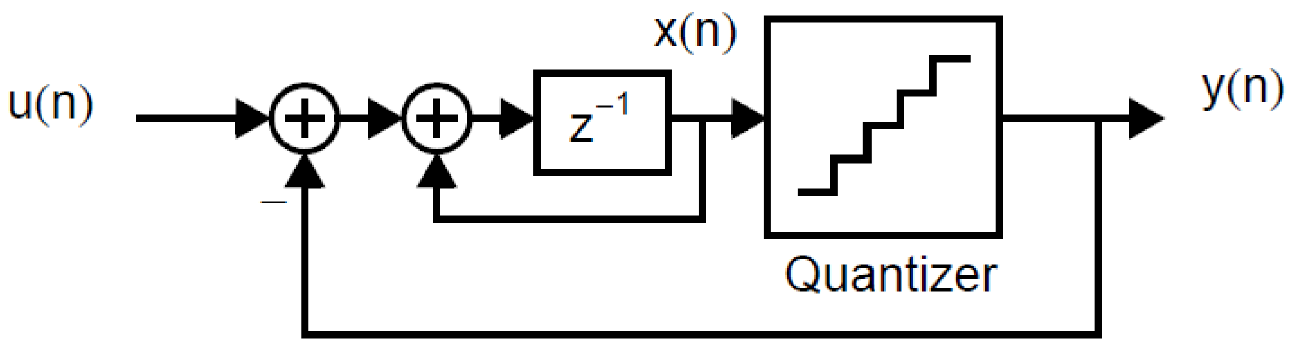
ENG-259

Signals and Spectra in Oversampling ADC



First-Order Noise Shaping

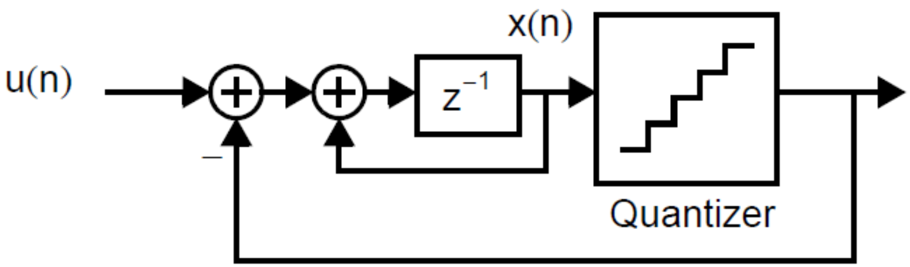


$$H(z) = \frac{1}{z-1}$$

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1}$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+1/(z-1)} = (1-z^{-1})$$

First-Order Noise Shaping



$$H(z) = \frac{1}{z-1}$$

$$z = e^{j\omega T} = e^{j2\pi f/f_s}$$

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1}$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+1/(z-1)} = (1-z^{-1})$$

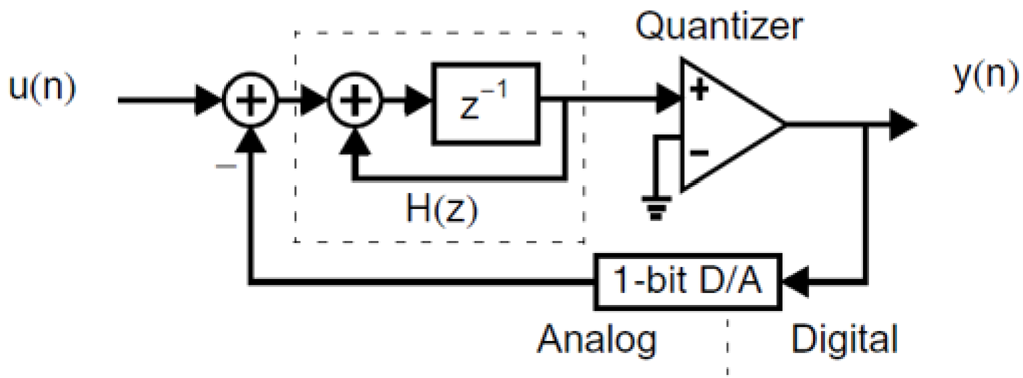
$$N_{TF}(f) = 1 - e^{-j2\pi f/f_s} = \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \times 2j \times e^{-j\pi f/f_s} = \sin\left(\frac{\pi f}{f_s}\right) \times 2j \times e^{-j\pi f/f_s} \longrightarrow |N_{TF}(f)| = 2\sin\left(\frac{\pi f}{f_s}\right)$$

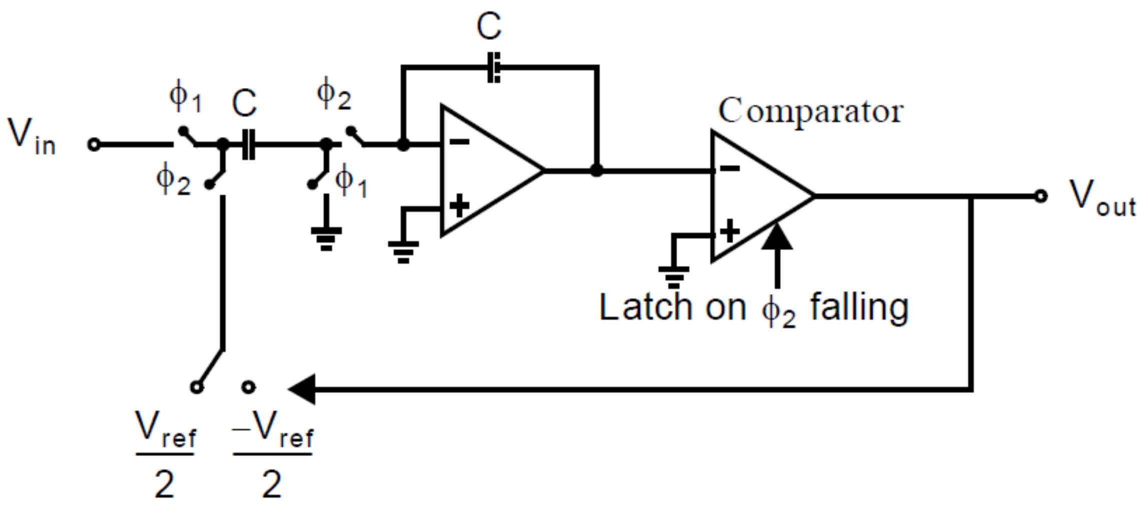
$$P_e = \int_{-f_0}^{f_0} S_e^2(f)|N_{TF}(f)|^2\,df = \int_{-f_0}^{f_0}\left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3$$

$$SQNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{3}{\pi^2}(OSR)^3\right]$$

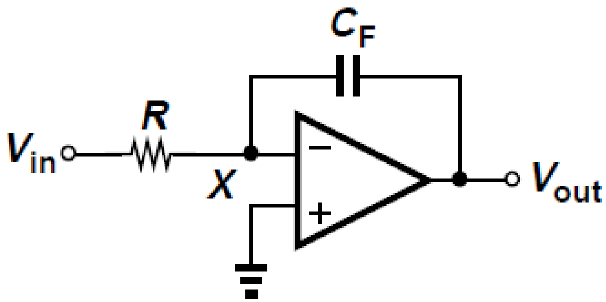
$$= 6.02N + 1.76 - 5.17 + 30\log(OSR)$$

First-Order Modulator SC Implementation



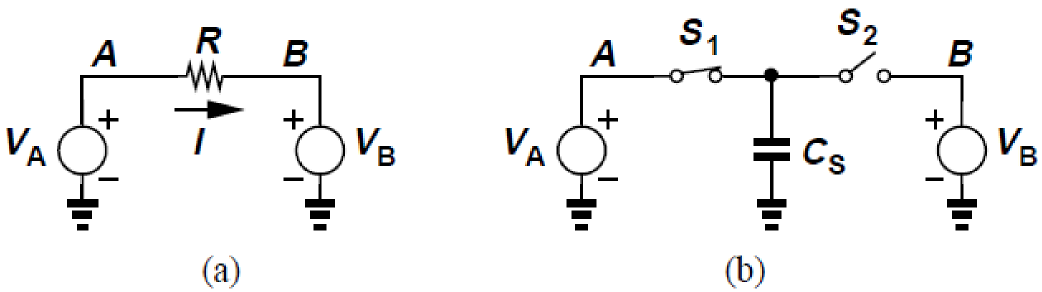


Switched-Capacitor Integrator



- Output of a continuous-time integrator can be expressed as

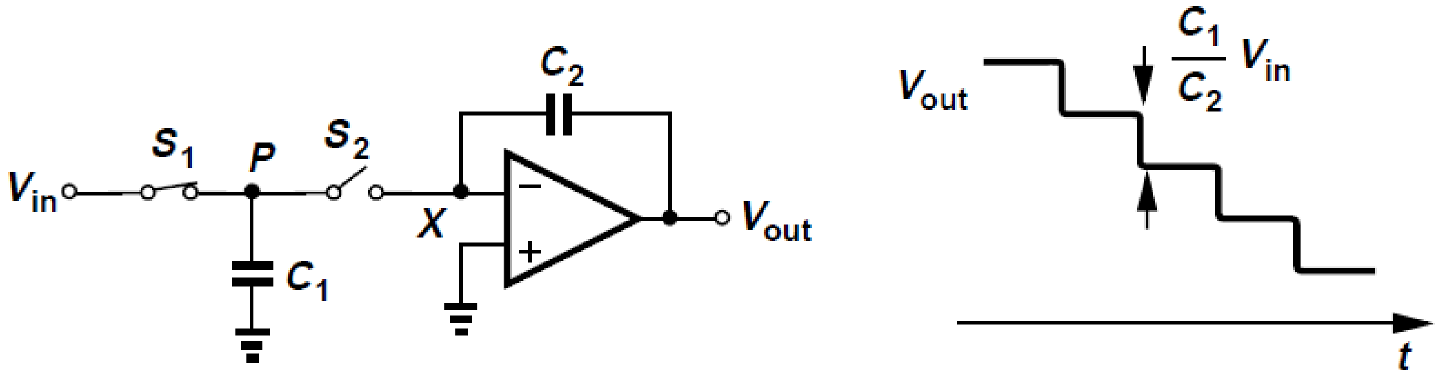
$$V_{out} = -\frac{1}{RC_F}\int V_{in}dt$$



- In Fig. (a), resistor *R* carries a current of $(V_A - V_B)/R$
- In Fig. (b), C_S is alternately connected to *A* and *B* at a clock rate f_{CK}
- Average current flowing from *A* to *B* is the charge moved in one clock period
- Can be viewed as a resistor of value $(C_S f_{CK})^{-1}$

$$\begin{aligned}\overline{I_{AB}} &= \frac{C_S(V_A - V_B)}{f_{CK}^{-1}} \\ &= C_S f_{CK}(V_A - V_B)\end{aligned}$$

Switched-Capacitor Integrator



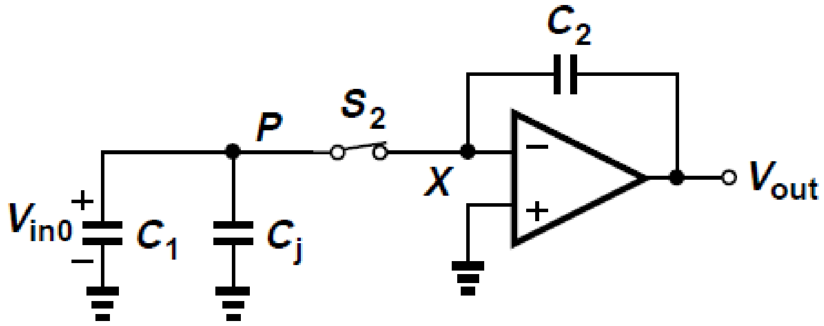
(a) (b)

- Fig. (a) shows discrete-time integrator
- In every clock cycle, C_1 absorbs a charge equal to C_1V_{in} when S_1 is on and deposits it on C_2 when S_2 is on
- If V_{in} is constant, output changes by $V_{in}C_1/C_2$ every clock cycle [Fig. (b)]
- Final value of V_{out} after clock cycle can be written as

$$V_{out}(kT_{CK}) = V_{out}[(k-1)T_{CK}] - V_{in}[(k-1)T_{CK}] \cdot \frac{C_1}{C_2}$$

Switched-Capacitor Integrator

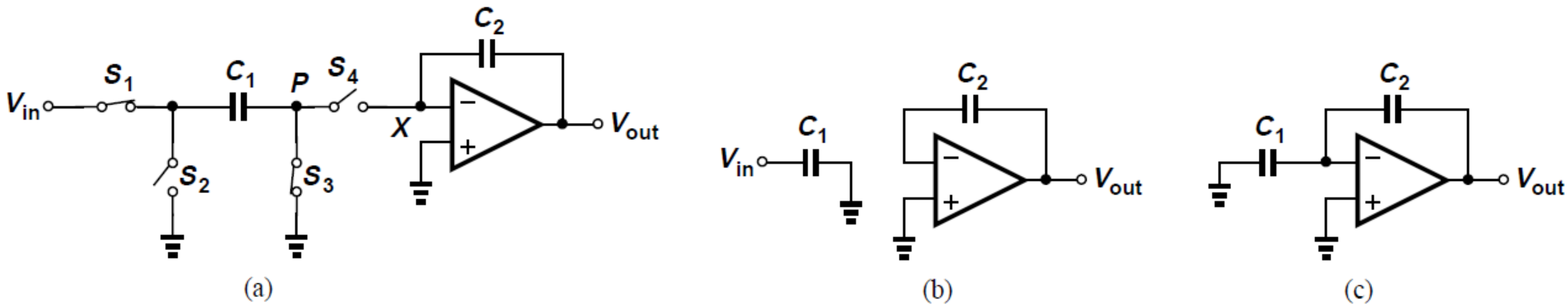
- Input-dependent charge injection of S_1 introduces nonlinearity in output voltage
- Nonlinear capacitance at node P resulting from source/drain junctions of S_1 and S_2 leads to a nonlinear charge-to-voltage conversion when C_1 is switched to X



- Charge stored on the total junction capacitance, C_j is not equal to $V_{in0}C_j$, but rather equal to

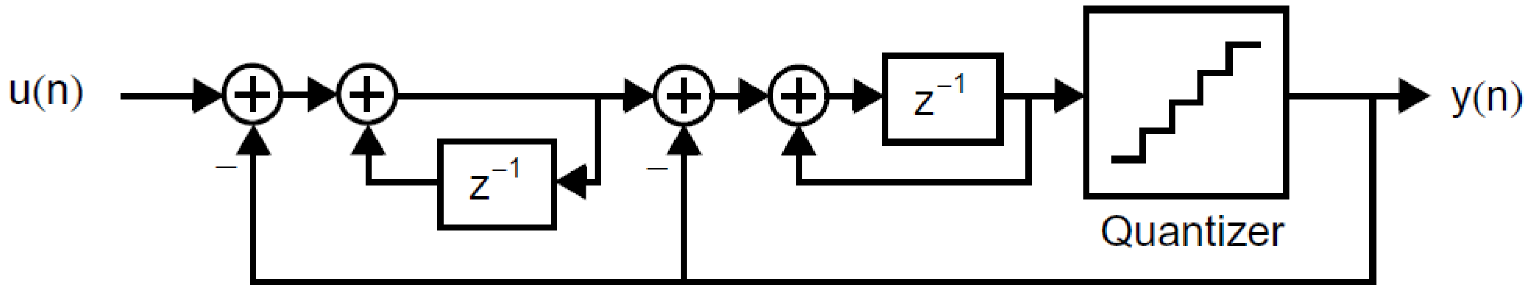
$$q_{cj} = \int_0^{Vin0} C_j dV.$$

Switched-Capacitor Integrator



- Circuit of Fig. (a) resolves the issues in the simple integrator
- In sampling mode [Fig. (b)], S_1 and S_3 are on, S_2 and S_4 are off, allowing voltage across C_1 to track V_{in} while op amp and C_2 hold previous value
- In the transition to integration mode, S_3 turns off first, injecting a constant charge onto C_1, S_1 turns off next, and subsequently S_2 and S_4 turn on
- Charge stored on C_1 is transferred to C_2 through the virtual ground node

Second-Order ΔΣ Modulator



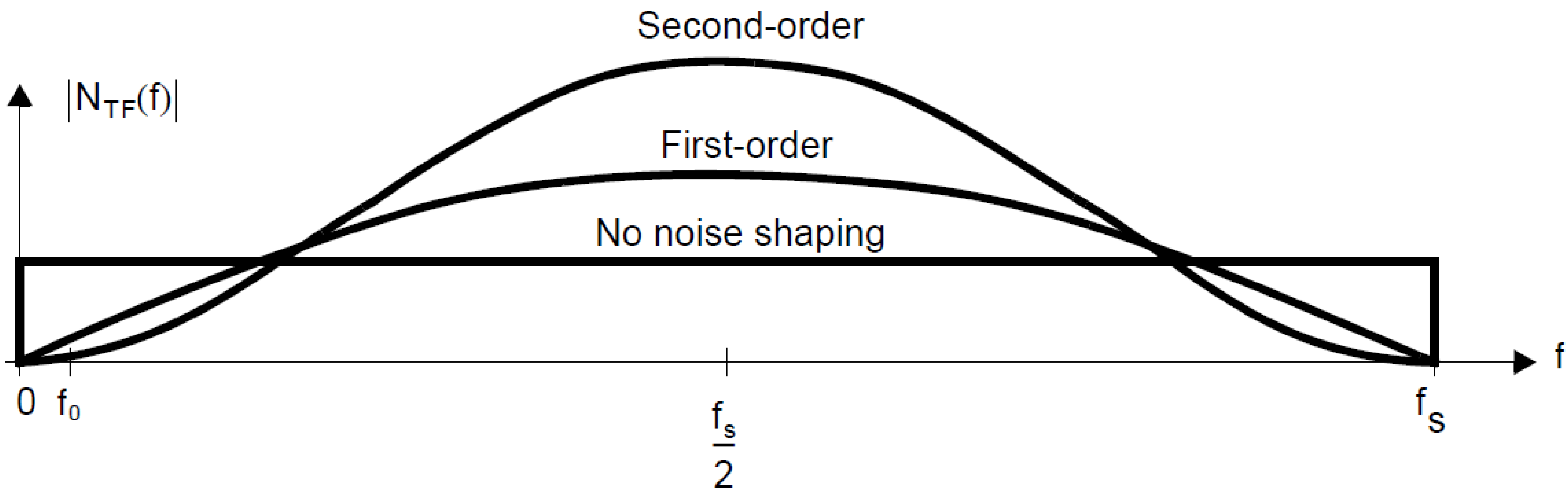
$$N_{TF}(f) = (1 - z^{-1})^2 \qquad |N_{TF}(f)| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2$$

$$P_e \cong \frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5$$

$$SQNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

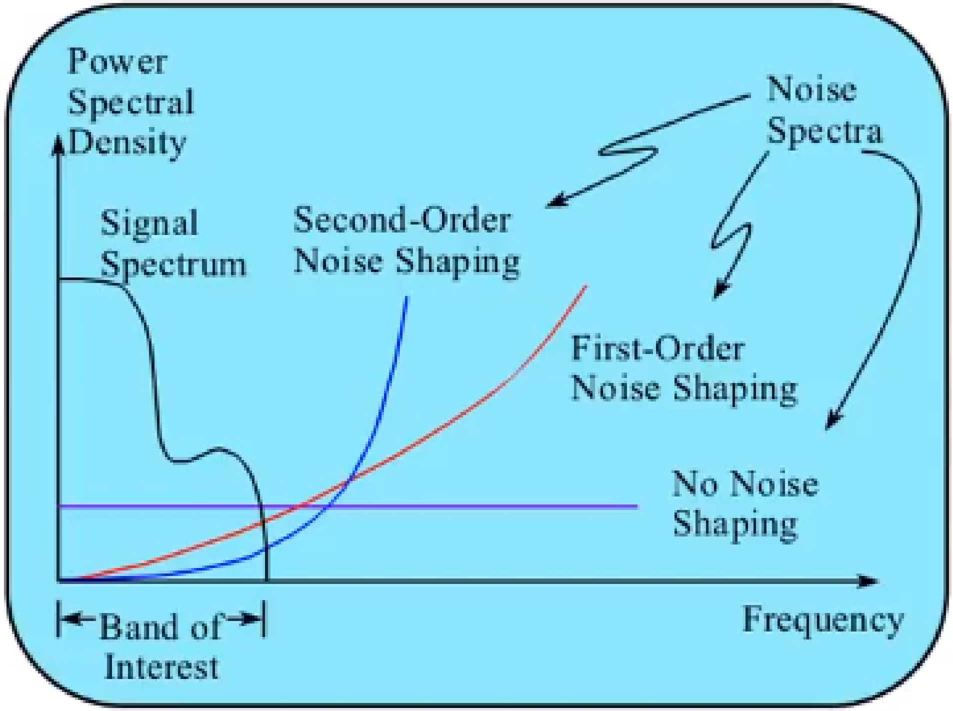
$$= 6.02N + 1.76 - 12.9 + 50\log(OSR)$$

Shaped Quantization Noise



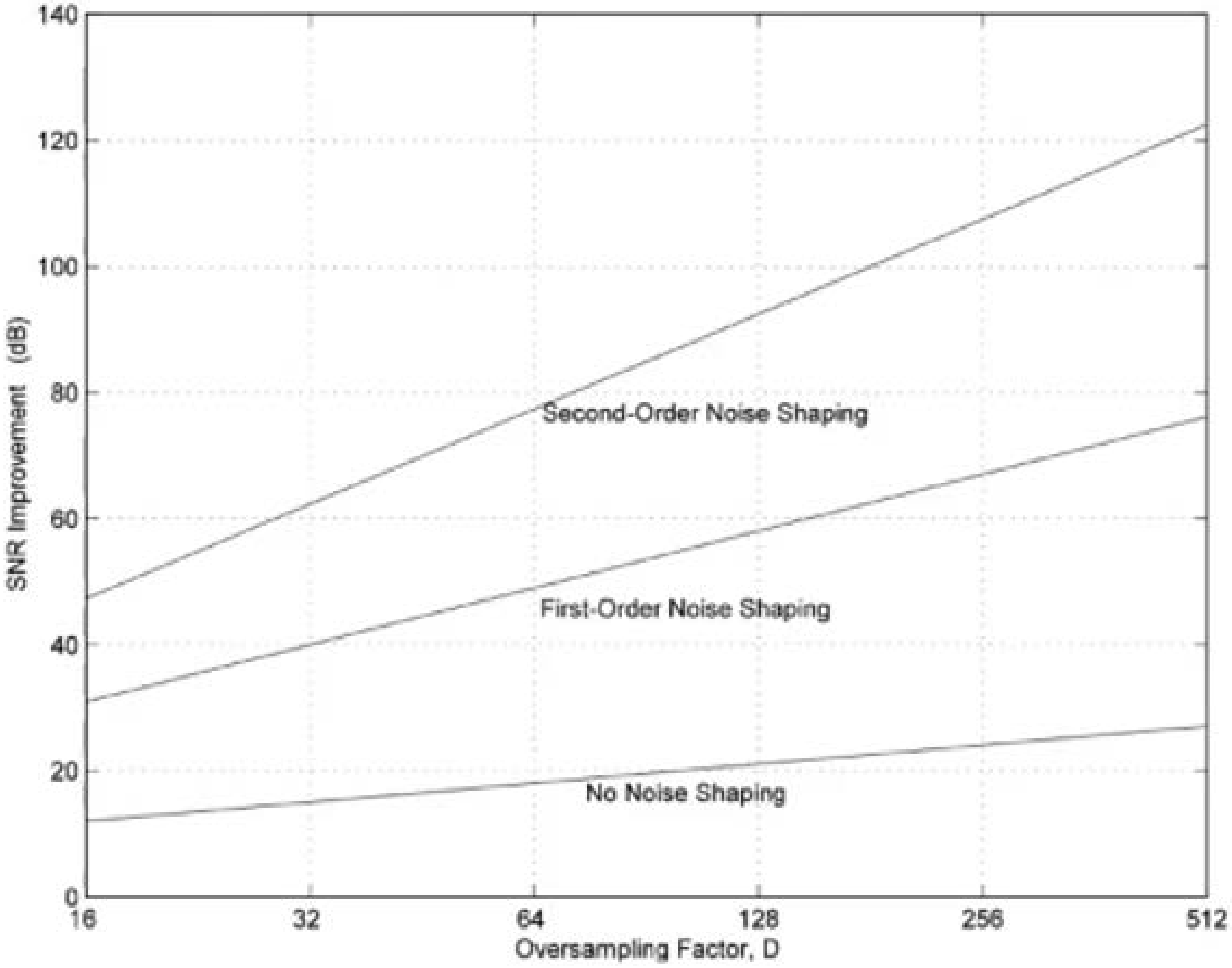
Noise Shaping Rate

- Two Main Factors Impact Performance:
  - Oversampling Rate *D*
  - Order of the Noise Shaping (1st, 2nd, 3rd, etc.)

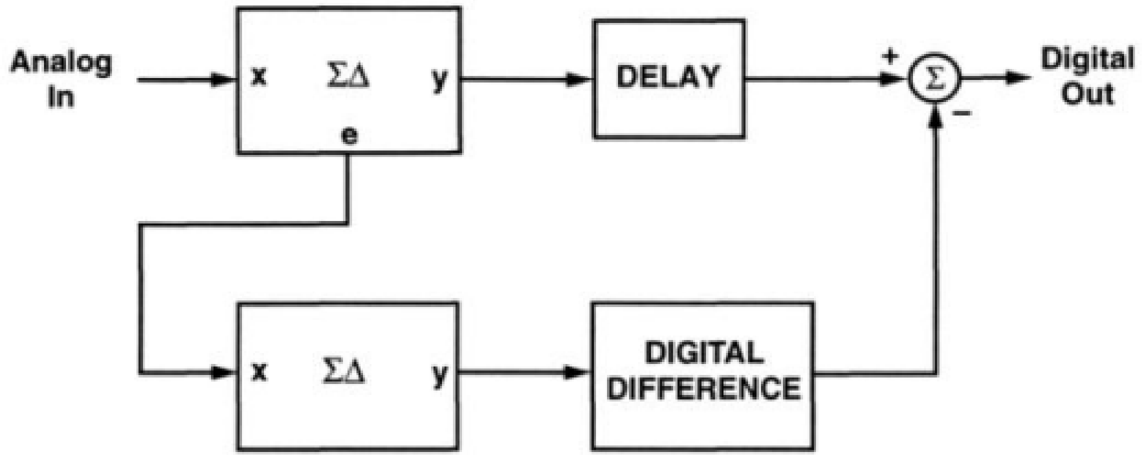


Noise Shaping	Trade Rate
None	0.5 Bits/Octave
1st Order	1.5 Bits/Octave
2nd Order	2.5 Bits/Octave

SQNR Improvement

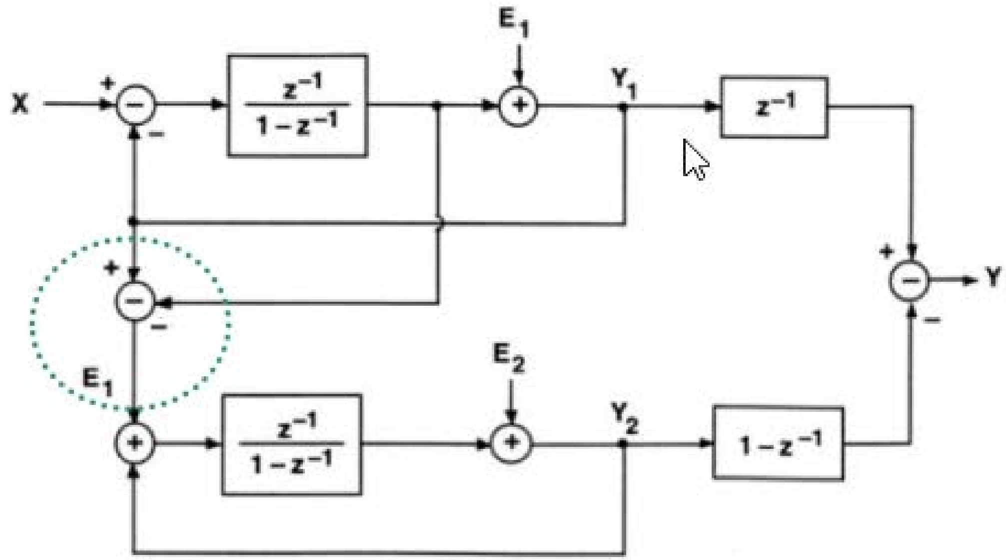


Higher Order Modulator using Cascade of 2-stages



- Main ΣΔ quantizes the signal
- The 1st stage quantization error is then quantized by the 2nd quantizer
- The quantized error is then subtracted from the results in the digital domain

2^{nd}-Order (1-1) Cascaded $\Delta\Sigma$ Modulator



$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

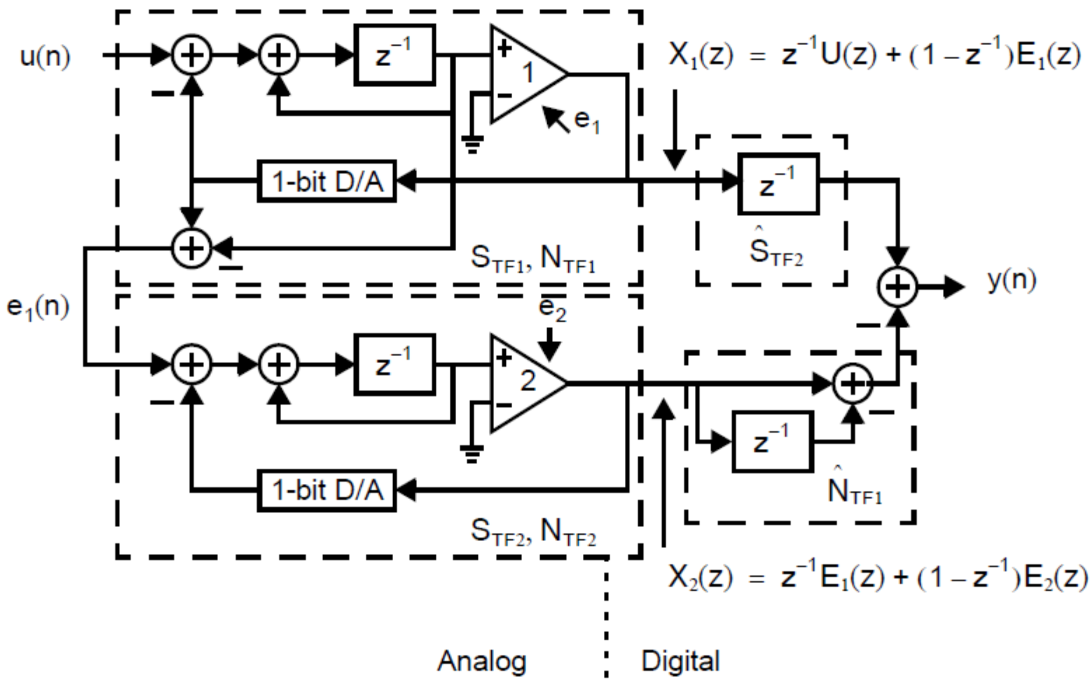
$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})Y_2(z)$$

$$= z^{-2}X(z) + z^{-1}(1 - z^{-1})E_1(z) - z^{-1}(1 - z^{-1})E_1(z) - (1 - z^{-1})^2E_2(z)$$

$$\boxed{Y(z) = z^{-2}X(z) - (1 - z^{-1})^2E_2(z)}$$

2^{nd} order noise shaping

MASH (Multi-stAge noise SHaping) structure



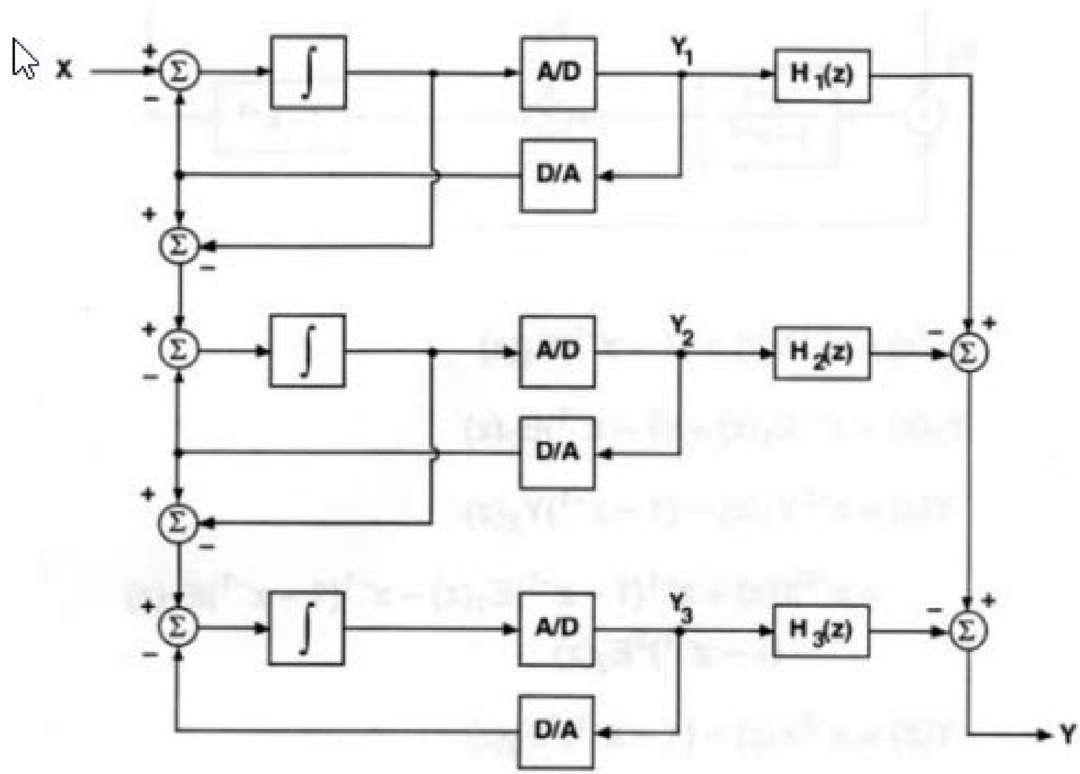
$$X_1(z) = S_{TF1}(z)U(z) + N_{TF1}(z)E_1(z)$$
$$= z^{-1}U(z) + (1 - z^{-1})E_1(z)$$

$$X_2(z) = S_{TF2}(z)E_1(z) + N_{TF2}(z)E_2(z)$$
$$= z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = \hat{S}_{TF2}(z)X_1(z) - \hat{N}_{TF1}(z)X_2(z)$$
$$= \hat{S}_{TF2}(z)S_{TF1}(z)U(z) + [\hat{S}_{TF2}(z)N_{TF1}(z) - \hat{N}_{TF1}(z)S_{TF2}(z)]E_1(z) - \hat{N}_{TF1}(z)N_{TF2}(z)E_2(z)$$
$$= \hat{S}_{TF2}(z)S_{TF1}(z)U(z) - \hat{N}_{TF1}(z)N_{TF2}(z)E_2(z) \quad \textit{if} \quad \hat{N}_{TF1}(z) = N_{TF1}(z) \text{ and } \hat{S}_{TF2}(z) = S_{TF2}(z)$$
$$= z^{-2}U(z) - (1 - z^{-1})^2E_2(z)$$

3rd-Order (1-1-1) Cascaded ΔΣ Modulator

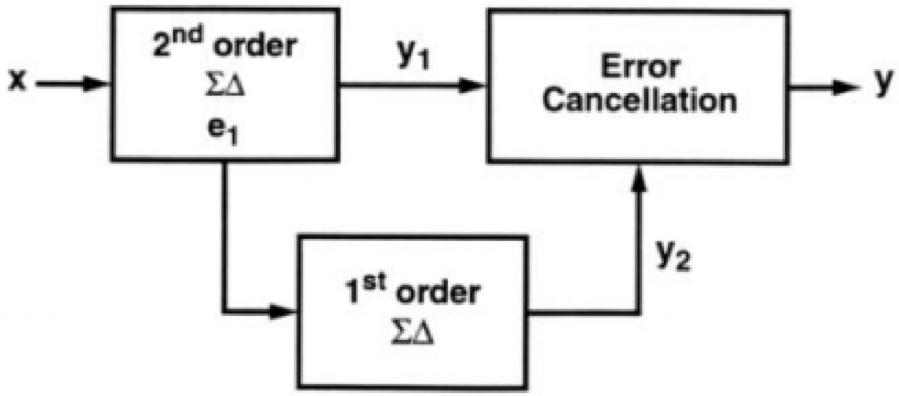
- Can implement 3rd order noise shaping with 1-1-1
- This is also called MASH (multi-stage noise shaping)



3rd-Order (2-1) Cascaded ΔΣ Modulator

Advantages of 2-1 cascade compared to 1-1-1-:

- Low sensitivity to matching precision of analog/digital paths
- Low spurious limit cycle tone levels
- No potential instability



$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$\begin{aligned} Y(z) &= z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z) \\ &= z^{-3}X(z) + z^{-1}(1 - z^{-1})^2 E_1(z) - z^{-1}(1 - z^{-1})^2 E_1(z) \\ &\quad - (1 - z^{-1})^3 E_2(z) \end{aligned}$$

3rd order noise shaping

$$\boxed{Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z)}$$

Summary of ΔΣ ADC

- Advantages of Sigma-Delta ADCs is Three-Fold:
  - Oversampling makes the Anti-Alias Filter Easy!
  - Noise Shaping Pushes ADC Noise Outside Signal Band
  - Low-Bit ADCs can be Made Closer to Ideal than High-Bit ADCs
- Disadvantage
  - Hard to get Extremely Wide Processing BW
  - But progress is being made…