SAN JOSÉ STATE UNIVERSITY

EE178 Spring 2017
Lecture Module 1

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Goals

- I am here because I enjoy sharing information on how to use Xilinx silicon, software, and solutions

- You are here to earn elective credits, but more importantly, to gain marketable experience

Syllabus Review

- No paper handouts – print your own
- Class format is lecture with practical exercises and project assignments
  - Substantial effort is required of you
  - There is no dedicated “lab” meeting

Academic Integrity

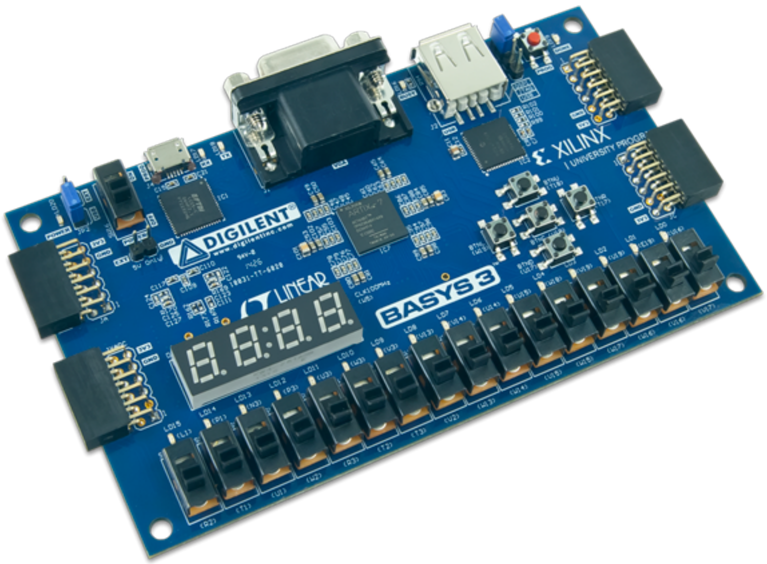
- All work is expected to be your own
  - It is okay to talk to each other and share ideas
  - It is not okay to cut and paste or share files
  - See policy on academic dishonesty

- If you are worried about “contamination” then ask an instructor for help

Required Equipment

- Immediately order and obtain a Digilent Basys3 board (Xilinx Artix 7 FPGA)
  - http://www.digilentinc.com
  - Request academic pricing
  - No “optional” items

- Labs may require access to additional equipment (monitor)



Required Equipment

- Provide your own development system
  - Laptop or desktop PC with a USB port
  - Windows 10 (64-bit) is the required O/S

- Immediately download and install Xilinx Vivado 2016.2 Webpack Edition
  - Described in first lab assignment
  - Pay attention to version / edition

Discussion Group

- Immediately go to the class website and follow the instructions to join the class discussion group
  - Class announcements, questions forum
  - Ensures “everyone is in the know”

- Email me directly with personal /confidential questions or assignment submissions

Prior Knowledge

- You should already be familiar with digital logic design from a class such as EE118
  - Electrical / Logical Basics
  - Combinational Logic
  - Sequential Logic
  - Verilog-HDL

- Let's quickly review what this means to me
  - This is not a crash course, it is a summary list
  - Items in gray are less important for this class

Electrical Basics

- Simple logic circuit implementation with transistors -- basic gates, etc...
- Transmission gates and three-state buffers
- Concepts of switching thresholds, noise margin, and electrical characteristics
- Digital abstraction of underlying analog circuits

Logical Basics

- Boolean algebra (all those rules…)
- Number systems and representation
  - Binary / Hexadecimal / Decimal
  - Conversions
  - Arithmetic

Combinational Logic

- Simple gates and their truth tables
- More complex functions and their truth tables
  - Multiplexers
  - Encoders, decoders
- Arithmetic circuits
  - Half Adder/Subtractors, Full Adder/Subtractors
  - Ripple Adders/Subtractors (n-bit)
  - Magnitude and Identity Comparators

Combinational Logic

- Combinational circuit analysis
- Random logic design
- SOP and POS canonical forms
- Use of KMAP to generate canonical forms
- Use of “Don’t Cares” in logic design
- Static and dynamic hazards

Sequential Logic

- Analysis of feedback sequential circuits
- Design of feedback sequential circuits
- Use of feedback sequential circuits
  - Flip flops
  - Latches
- Analysis of synchronous sequential circuits
- Design of synchronous sequential circuits

Sequential Logic

- Application of common synchronous circuits
  - Registers (various types)
  - Counters
- Models of synchronous sequential circuits
  - Mealy
  - Moore
- Finite state machine design techniques
- State assignment / encoding options

Verilog-HDL

- Notion of a hardware description language
- Use of Verilog-HDL for describing digital circuits and simulating their behavior
- Different ways to describe digital circuits
  - Behavioral
  - Register Transfer Level
  - Primitive or Gate Level

Why Use FPGAs?

- You would use an FPGA if it is the best choice given some metric for optimal
  - Do we know what an FPGA is?

- What are viable alternatives?
  - Custom ASIC
  - Structured ASIC (Gate Array)
  - Microcontroller
  - Processor system
  - Application specific standard product
  - Random components (e.g. SSI, MSI)

Some Metrics for Optimal

- Size, weight, and power
- Total design cost
  - Direct component cost
  - Board complexity / cost
  - NRE and amortization
- Time to design
  - Observability, debug
  - Availability of IP
- Time to market
  - Component mfg. time
- Lifetime
  - Component availability
- Performance
  - Clock frequency
  - Throughput / parallelism
  - Latency
- Reliability
  - Hard failure rates
  - Soft failure rates
- Field upgradability
  - Product before specification
  - Extend product lifespan
  - Risk reduction

Commercial Applications of Programmable Logic

Wired Communications
- Wired infrastructure
- Data center, storage

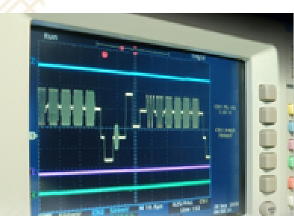
Wireless Communications
- Wireless infrastructure

Industrial, Scientific, Medical
- Ultrasound systems
- Motor controllers

Audio, Video, Broadcast
- 3D cameras
- Video transport

Automotive
- Infotainment
- Driver assistance

Consumer
- 3D television
- eReaders



Test & Measurement
- Communications instruments
- Semiconductor test equipment

Source: Xilinx, Inc.

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