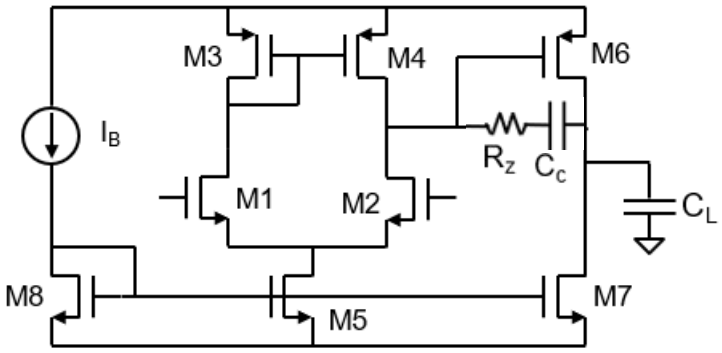
EE223 Homework #5 **Nov. 5, 2018**

Due: Nov. 28, 2018, 6 PM. 20% / day will be deducted if you miss the 6 PM deadline.

Design of a 2-stage OPAMP Circuit

In this homework, you will design a Two-Stage OPAMP with RC compensation. Use nmos2v and pmos2v for all circuits based on VDD=1.8V at TT, 27C. Your simulation results on dc operating point should show that all the transistors are in saturation region.



Key spec for the opamp is as follows:
- Av = 60 dB
- GBW = 100 MHz
- PM > 60°
- GM > 12dB
- SR > 60V/us
- Power < 2.5mW
- C_L = 5 pF

1. Draw a schematic shown above and design the circuit to meet the key spec parameters. Choose the value of Rz to cancel the zero with the second pole. See the homework#5 hint file. Provide the assumption and procedure you have used to size all the transistors in your design. Use the following parameters for the hand calculation. (**10 points**)
   - $KP_n = \mu_n C_{ox} = 300\ uA/V^2$
   - $KP_p = \mu_p C_{ox} = 160\ uA/V^2$
   - Vdsat = 0.2 V
   - I_B = 100 uA

2. Set the opamp in unity gain configuration and run a dc simulation with the input voltage of 0.9V, VDD=1.8V, Temperature=27C in Typical corner. Provide the dc operating point information as well as the node voltage information in the schematic you have designed. Create a screenshot with white background in monochrome. The screenshot should show transistor sizes as well as operating point information (drain current and operating region). Explain if your design meets the requirement or not. Report the total power dissipation of the circuit as well. (**5 points**)

3. Run a stb analysis from 10 Hz to 1 GHz to get the ac response of the opamp. Create an AC simulation plot like Fig. 1 below. From the ac plot, report the DC gain (A_0), -3dB bandwidth (ω_{-3db}), and the unity gain bandwidth (ω_u). Calculate the gain bandwidth product ($A_0 \times \omega_{-3db}$) and compare it with the unity gain bandwidth (ω_u). Explain if there is any difference. (**5 points**)

4. Run a transient simulation in unity gain configuration to get a plot like below. Input signal should be 10MHz pulse with 500mV step from 0.9V to 1.4V. Calculate the slew rate of the response and create a plot similar to Fig. 2 below. (**5 points**)

5. Now replace Rz with a PMOS transistor and add an appropriate bias circuit. Optimize the design to meet the spec and repeat the problem 2-4. (2**5 points**)

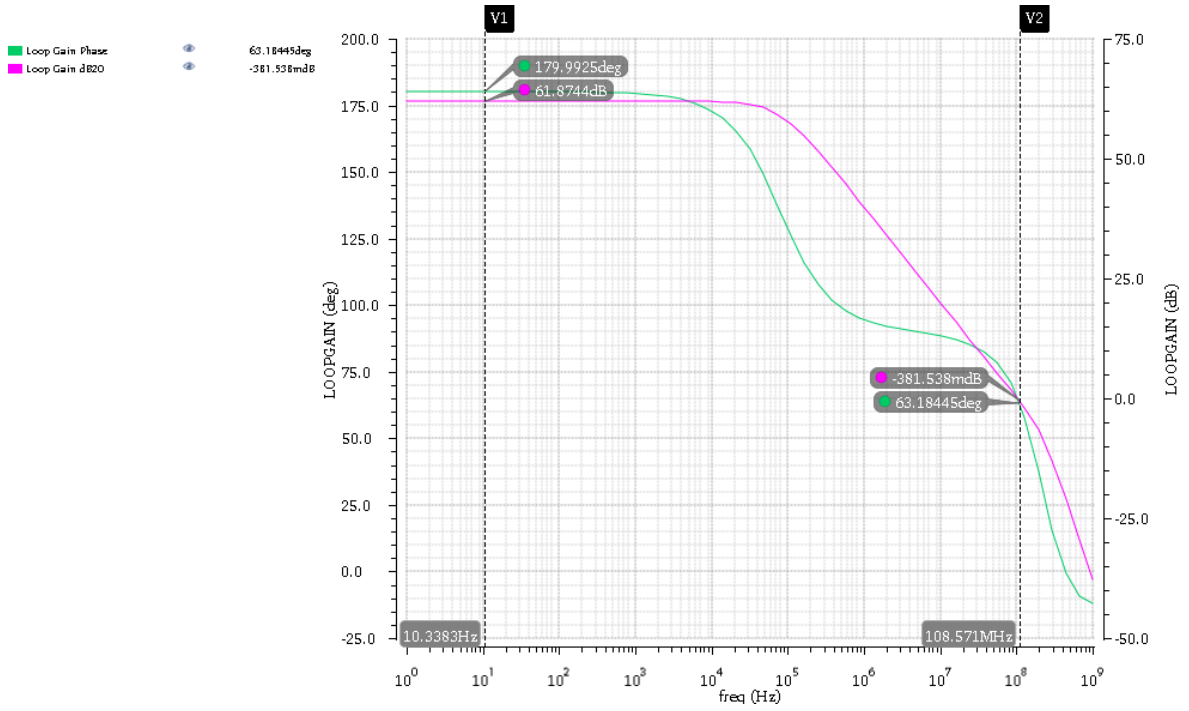


Fig. 1 An example AC simulation plot

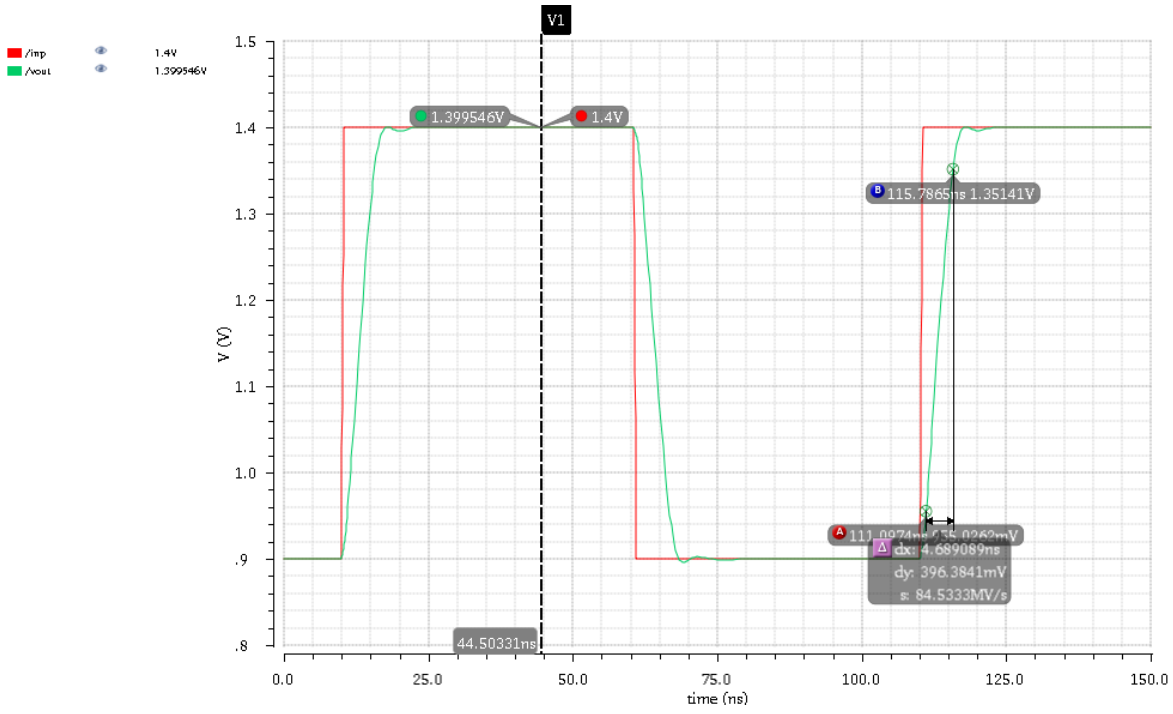


Fig. 2 An example transient simulation plot