SAN JOSÉ STATE UNIVERSITY

EE178 Spring 2017
Lecture Module 3

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Goals

- Introduction to static timing analysis
  - Circuit elements and their delays / requirements
  - Synchronous, single clock design questions:
    - Can this circuit work at all?
    - What is the maximum frequency of operation?

- Typical timing constraints for a synchronous, single clock design and reading timing reports

Reference

- Xilinx Vivado Design Suite User Guide: Using Constraints, UG903
  - Available in DocNav where you installed Vivado
  - Available on the Xilinx website

Static Timing Analysis

- Even though a digital circuit may be logically correct, you need to know how it will perform in its physical implementation
  - To meet a performance specification
  - To evaluate how your design operates

Static Timing Analysis

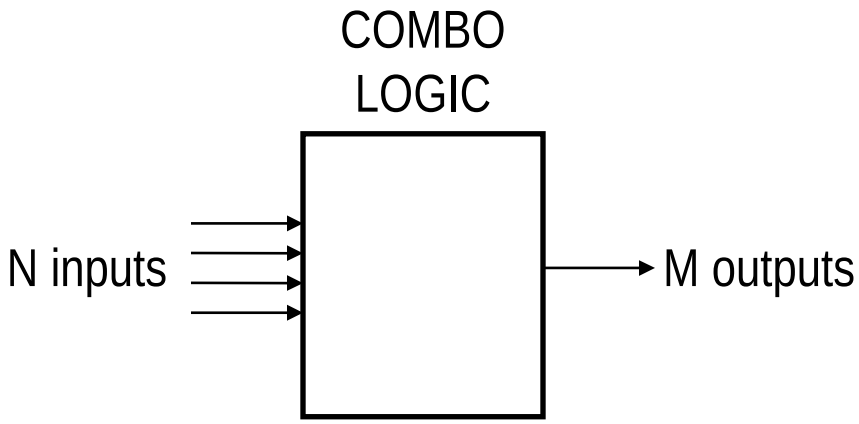
- Items of interest for analysis include:
  - Requirements for input signals to the circuit
  - Internal performance, maximum clock frequency
  - Behavior of output signals from the circuit
- If there are design specs, this information is important to determine compliance
- Also important simply to document circuit behavior

Static Timing Analysis

- To analyze the circuit, you need to know many parameters of the components used
  - Combinational logic propagation delays
  - Signal propagation delays through wire
  - Sequential logic input requirements and output delays

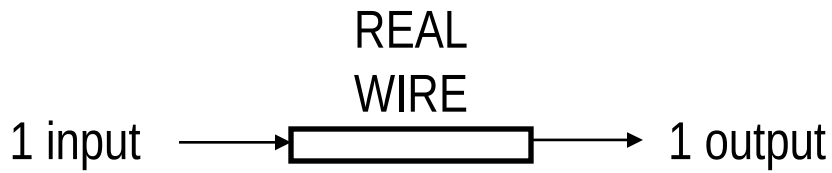
Combinational Logic

- Combinational logic propagation delays
  - Input to output propagation delays
  - Always non-zero, because we live in reality
  - Signal rising versus falling delays can be different
  - Worst case and best case delays (max/min)



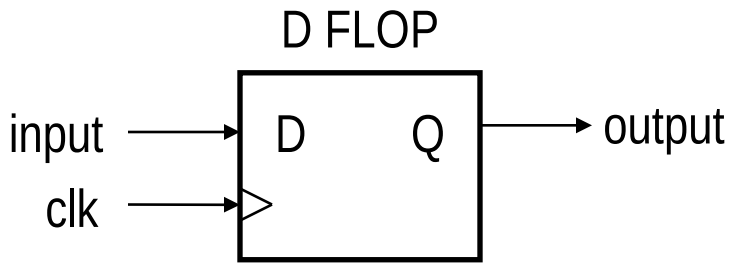
Wires

- Signal propagation delays through wire
  - Delays due to the physical nature of real wires such as resistance, capacitance, inductance
  - Always non-zero, because we live in reality
  - Worst case and best case delays (max/min)



State Elements

- Sequential logic input requirements and output valid delays
  - Clock to output valid delays
  - Relation of sampled input signal to clock
  - Signal rising versus falling delays can be different
  - Worst case and best case delays (max/min)

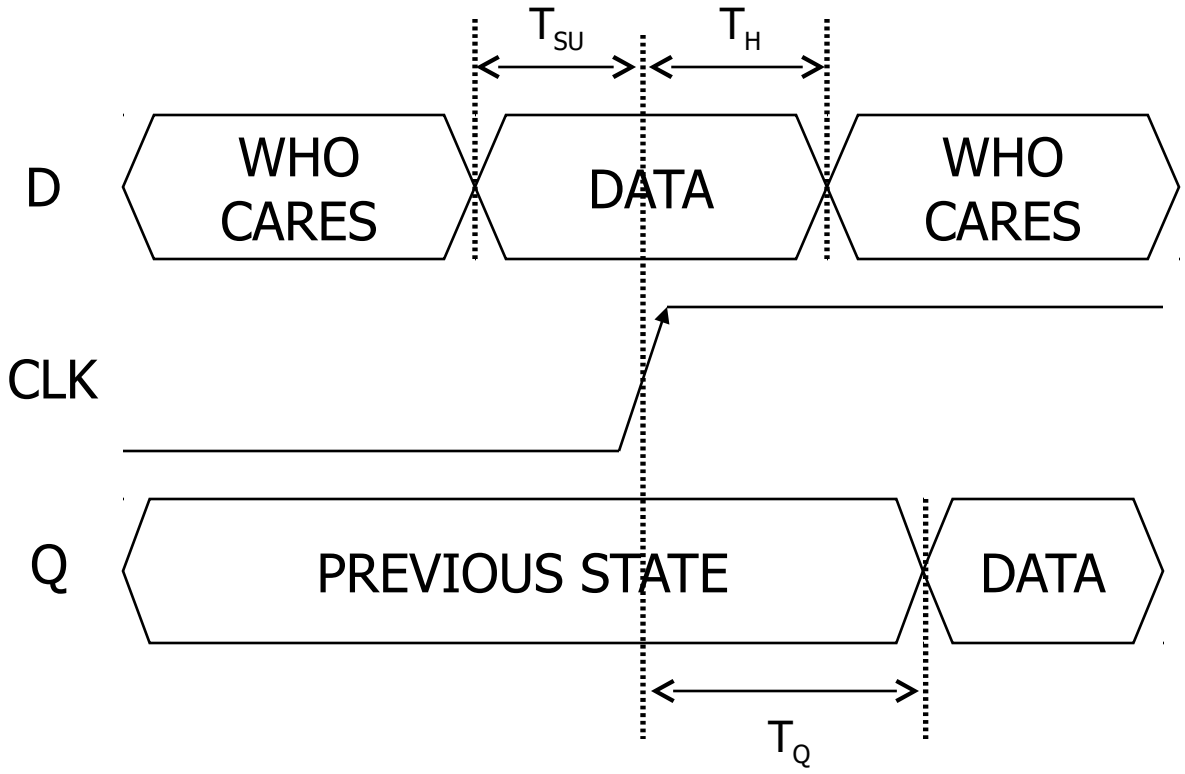


State Elements

- What is the behavior of a D flip flop?
  - Analogy to Polaroid camera...
  - Active clock edge like pressing the button
  - Data must be at rest during sampling window:
    - For a short time before (input setup)
    - For a short time after (input hold)
  - Some time after sampling event takes place, the sampled result is available (clock to out)
  - Requirements must be met for proper operation

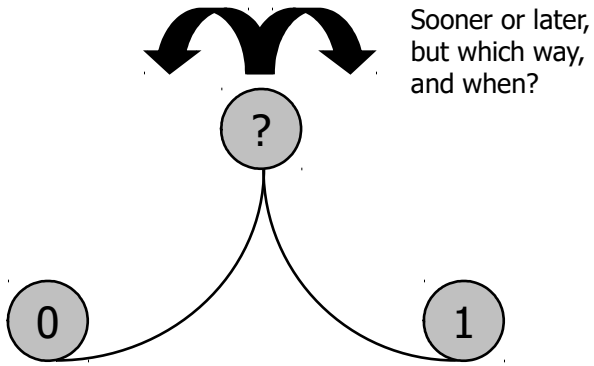
State Elements

- Synchronous designs rely on this behavior



State Elements

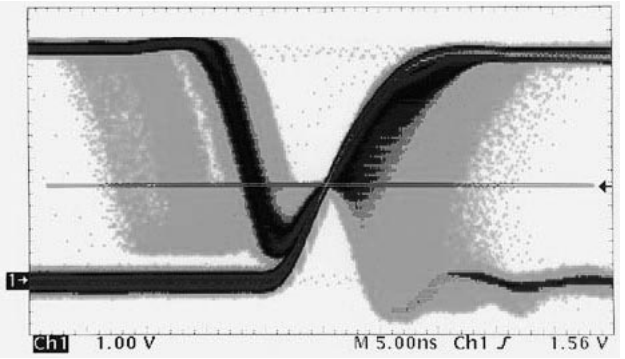
- If the input requirements are violated, the flip flop may fail to correctly sample the input
- Even worse, the it may become metastable
  - Observable as an increase in the clock to out time
  - The probability of remaining in a metastable state decreases exponentially with time
- This causes designs to fail



State Elements

Subject: Thinking out loud about metastability...

By: Philip Freidin



Flip flops may go metastable when input signals do not meet the setup and hold specifications with regard to the clock signal. These inputs include D, CE, CLR, PRE, S, R, T, J, K.

There is no cure for metastability. What you can do is trade latency of your system for higher MTBF. People that have found a cure are wrong.

Circuits that purport to solve metastability through hysteresis fail because the hysteresis circuit itself can go metastable.

Circuits that purport to solve metastability with injected noise fail because the noise is as likely to push a non-metastable event into being a metastable event as it is to helping to resolve such an event.

State Elements

Nothing improves the MTBF of a metastable synchronizer better than just waiting longer. Not clocking the intermediate signal on the negative clock edge. Not voting. Not threshold testing. Not adding noise. Not fancy SPICE simulations. Not predicting circuits. Not circuits designed to bias the outcome to either 1 or 0. Not clocking it twice as fast through twice as many flip flops. Nothing.

Just because current flip flops are better than stuff of a few years ago, and the probability and resolution time of metastable events is better, does not mean you can ignore this stuff. If someone says that things are so good now that "you almost don't have to worry about this anymore", what it means is that you absolutely need to understand it and design for it. If you don't, you will have unreliable systems.

From Thomas Cheney, October 1979:

"In closing, there is a great deal of theoretical and experimental evidence that a region of anomalous behavior exists for every device that has two stable states. The maturity of this topic is now such that papers making contrary claims without theoretical or experimental support should not be accepted for publication".

Real World Effects

- All parameters vary based on PVT
  - Higher voltage often speeds things up
  - Higher temperature often slows things down
  - Process variation is more challenging to predict
- Most datasheets specify maximum delays
- More challenging to specify minimum delays

Synchronous Design

- Every clock cycle, flip flops in a design will sample their inputs, store the value, and provide it at their outputs
  - This happens at all flip flops, on all clock edges
  - At the input side of the flip flops, the input setup and input hold requirements must be observed in order to guarantee predictable behavior
  - This applies on-chip, and between chips, as long as they are synchronous - a common clock

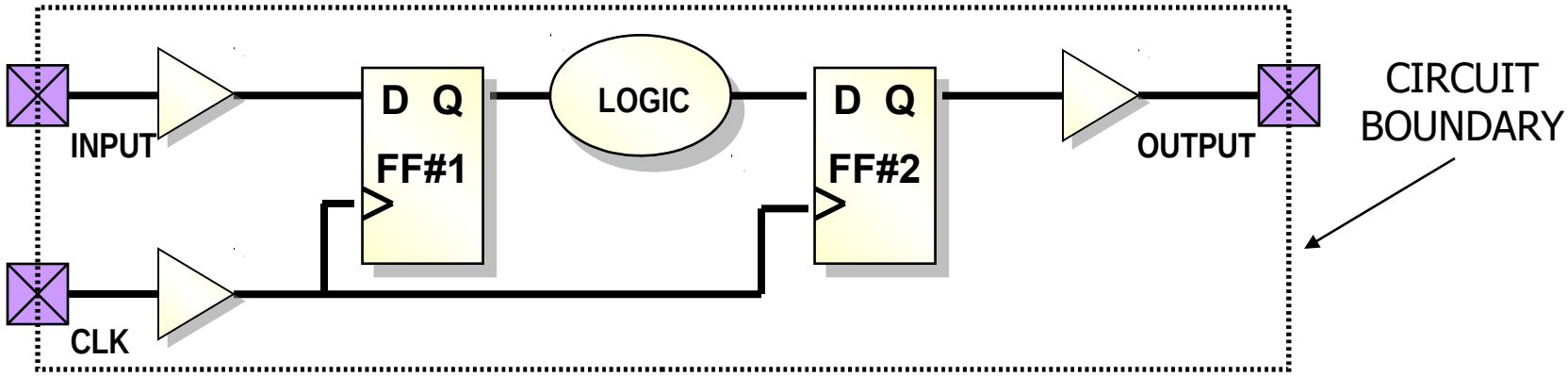
Paper Analysis Example

- Items of interest for analysis include:
  - Requirements for input signals to the circuit
  - Internal performance, maximum clock frequency
  - Behavior of output signals from the circuit
  - Timing from inputs to outputs (less common)

- Maximum clock frequency tells us how fast the circuit will operate
- Input and output behavior tells us how the circuit interacts with other circuits, presumed to be synchronous

Paper Analysis Example

- Items of interest for analysis include:
  - Internal performance, maximum clock frequency
  - Behavior of output signals from the circuit
  - Requirements for input signals to the circuit
- Evaluate how this circuit behaves, assuming an academic clock (no skew, no delay)

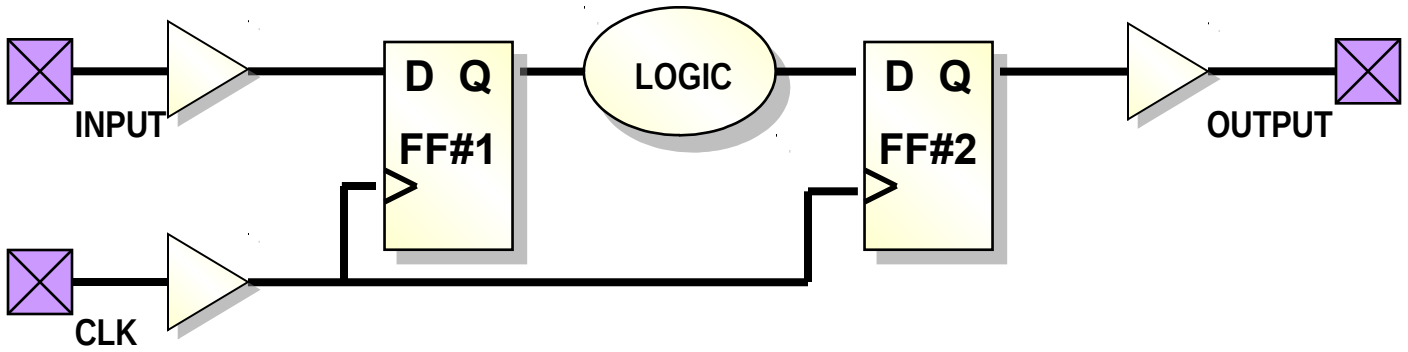


Paper Analysis Example

- Assume wire delays are $T_W = 0$ ns
- Buffers have delay of $T_B = 1$ ns
- Logic has delay of $T_L = 7$ ns
- Flip flops are identical with parameters:
  - Clock to out is $T_Q = 1$ ns
  - Input setup requirement is $T_{SU} = 2$ ns
  - Input hold requirement is $T_H = 0$ ns

Paper Analysis Example

- Clock period behavior of circuit.
  - Clock event at FF#1 launches new data into logic
  - Result sampled at FF#2 at next clock event
  - Max delay sets min period = 1/(max frequency)
  - $T_{QFF1} + T_L + T_{SUFF2} = 10$ ns min $\Rightarrow$ 100 MHz max



Paper Analysis Example

- Clock period behavior of circuit
  - This is really a check to see if the setup requirement of FF#2 is satisfied
  - If you have min/max delay parameters, use the maximum parameters for this analysis
  - What about the hold requirement?
  - Let's check to see if it is satisfied...

Paper Analysis Example

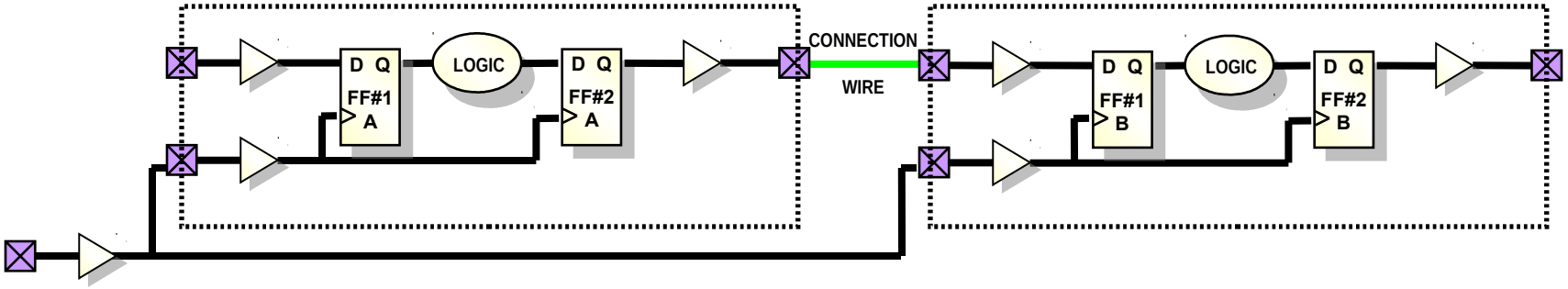
- Clock period behavior of circuit
  - Clock event at FF#1 launches new data into logic
  - Result must propagate slow enough to observe hold requirement at FF#2 for the old data
  - $T_{QFF1} + T_L \geq T_{HFF2}$?
  - If you have min/max delay parameters, use the minimum parameters for this analysis
  - If you use flip flops with zero hold requirement, this is always satisfied (no need to check)

Paper Analysis Example

- Clock period behavior of circuit
  - If the hold requirement is not met, the circuit will fail, no matter what clock frequency!
  - Real designs have multiple paths, and more than two flip flops…
    - Maximum frequency set by slowest path in design
    - Large designs have enormous numbers of paths
    - Most static timing analysis done by software

Paper Analysis Example

- Input and output behavior tells us how the circuit interacts with other circuits
- If device A and device B are synchronous, any place an output drives an input, a new path must be considered in period analysis



Paper Analysis Example

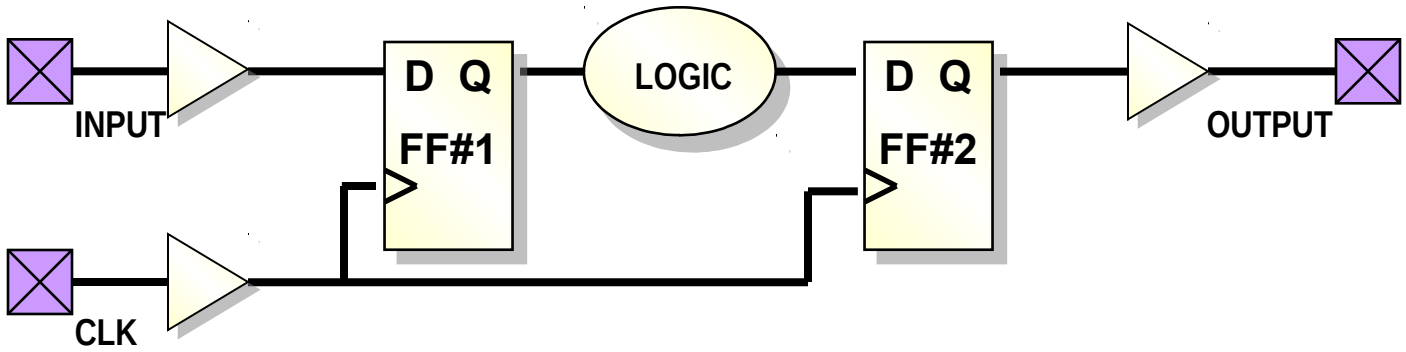
- The manufacturer of device A does not know anything about your specific design:
  - What is device B delay behavior?
  - What is the delay behavior of wiring?

- Given data on the input and output behaviors...
  - Minimum and maximum clock to output
  - Input setup and hold requirements

  …you can complete the analysis!

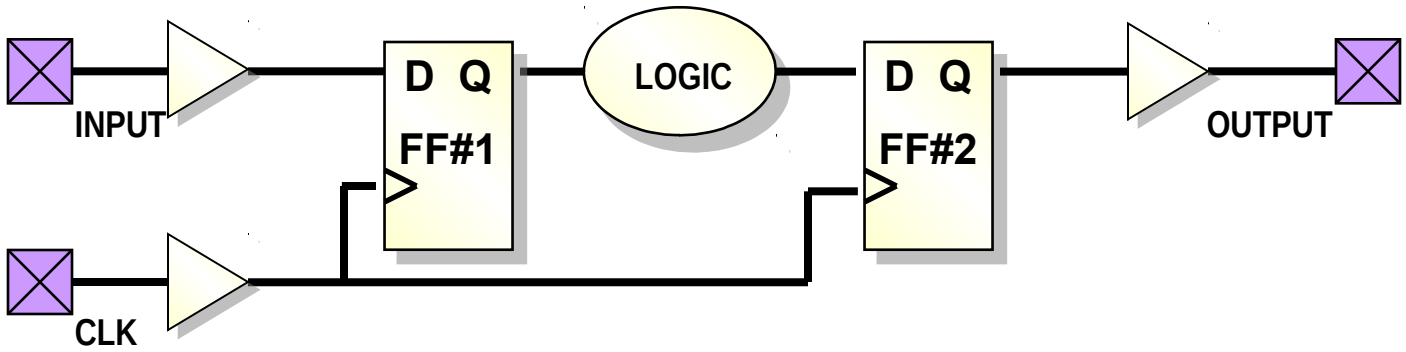
Paper Analysis Example

- Clock to output behavior of a circuit
  - Start at CLK pin, trace to OUTPUT pin
  - What is the total pin-to-pin delay?
  - $T_{BCLK} + T_{QFF2} + T_{BOUTPUT} = 3$ ns
  - If you have min/max parameters, what's worse?



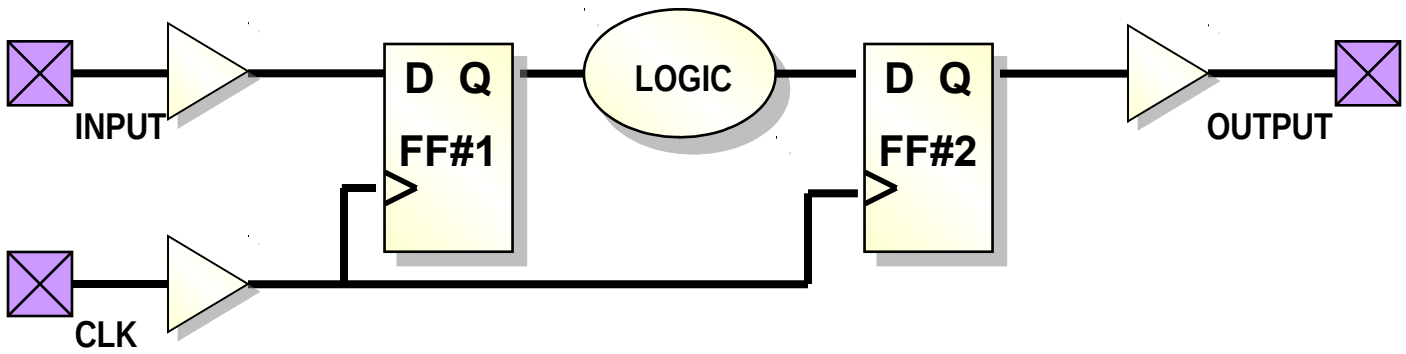
Paper Analysis Example

- Input setup behavior of a circuit
  - Start at CLK pin and INPUT pins, race to flip flop
  - What is the pin-to-pin input setup requirement?
  - $T_{SUFF1} + T_{BINPUT} - T_{BCLK} = 2$ ns
  - If you have min/max parameters, what's worse?



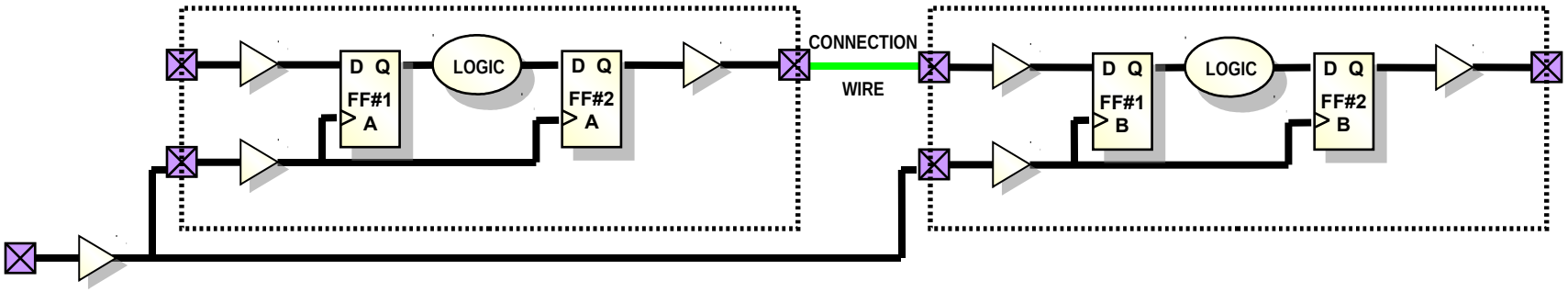
Paper Analysis Example

- Input hold behavior of a circuit
  - Start at CLK pin and INPUT pins, race to flip flop
  - What is the pin-to-pin input hold requirement?
  - $T_{HFF1} - T_{BINPUT} + T_{BCLK} = 0$ ns
  - If you have min/max parameters, what's worse?



Paper Analysis Example

- Clock period behavior at an interface
  - $T_{OUTA} + T_W + T_{SUB} = 5$ ns
  - $T_{OUTA} + T_W > T_{HB}$?
  - What is maximum frequency of complete circuit?



Some Questions

- For a designer, flip flops with zero hold requirement are wonderful – why?
- As a manufacturer, how do you design a flip flop with a zero hold requirement?
  - The benefit is ease of use
  - What is the hidden cost?
- As combinational logic and wire delays approach zero, what sets the maximum frequency?

Timing Constraints

- When doing designs with Xilinx FPGA devices, you need a mechanism to specify how you want the circuit to perform
  - To meet a performance specification
  - To evaluate how your design operates

- Let's look at the design we constrained in a lab assignment (see Verilog FSM lecture) and practice reading some Vivado timing reports

Timing Constraints

- When implementation completes, Vivado will let you know if your timing constraints failed
- Vivado is cognizant of process variation and performs analysis with min and max delays across range of voltage and temperature
- The lab assignment covers how to generate reports, let's look at the report detail…

Timing Constraints

```
create_clock -period 10.000 -name my_only_clock
             -waveform {0.000 5.000} [get_ports clk]

set_input_delay -clock [get_clocks my_only_clock] 5.000
            [get_ports {pause restart}]

set_output_delay -clock [get_clocks my_only_clock] 5.000
            [get_ports {even odd state[0] state[1] terminal}]

set_max_delay -from [get_ports {pause restart}]
            -to [get_ports terminal] 10.000
```

Timing Report Detail: Timer Settings

```
Copyright 1986-1999, 2001-2013 Xilinx, Inc. All Rights Reserved.
------------------------------------------------------------------------------------------------
| Tool Version : Vivado v.2013.4 (win32) Build 353583 Mon Dec  9 17:38:55 MST 2013
| Date         : Mon Feb 17 23:20:17 2014
| Host         : Lenovo running 32-bit Service Pack 1  (build 7601)
| Command      : report_timing_summary -delay_type min_max -report_unconstrained
|                -check_timing_verbose -max_paths 500 -nworst 500 -input_pins
|                -name timing_1 -file timing_report.txt
| Design       : fsm
| Device       : 7a100t-csg324
| Speed File   : -1  PRODUCTION 1.11 2013-11-22
------------------------------------------------------------------------------------------------

Timing Summary Report

------------------------------------------------------------------------------------------------
| Timer Settings
| --------------
------------------------------------------------------------------------------------------------

  Enable Multi Corner Analysis               :  Yes
  Enable Pessimism Removal                   :  Yes
  Pessimism Removal Resolution               :  Nearest Common Node
  Enable Input Delay Default Clock           :  No
  Enable Preset / Clear Arcs                 :  No
  Disable Flight Delays                      :  No

  Corner  Analyze    Analyze
  Name    Max Paths  Min Paths
  ------  ---------  ---------
  Slow    Yes        Yes
  Fast    Yes        Yes
```

Timing Report Detail: Create Clock (Setup - Max / Slow)

```
Slack (MET) :             8.574ns  (required time - arrival time)
  Source:                 state_reg[1]/C (rising edge-triggered cell FDPE clocked by my_only_clock  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            state_reg[1]/D (rising edge-triggered cell FDPE clocked by my_only_clock  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             my_only_clock
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (my_only_clock rise@10.000ns - my_only_clock rise@0.000ns)
  Data Path Delay:        1.466ns  (logic 0.743ns (50.681%)  route 0.723ns (49.319%))
  Logic Levels:           1  (LUT4=1)
  Clock Path Skew:        0.000ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.102ns = ( 14.102 - 10.000 )
    Source Clock Delay      (SCD):    4.456ns
    Clock Pessimism Removal (CPR):    0.354ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock my_only_clock rise edge)
                                                      0.000     0.000 r
    E3                                                0.000     0.000 r  clk
                         net (fo=0)                   0.000     0.000    clk
    E3                                                               r  clk_IBUF_inst/I
    E3                   IBUF (Prop_ibuf_I_O)         0.967     0.967 r  clk_IBUF_inst/O
                         net (fo=1, routed)           1.780     2.747    clk_IBUF
    BUFGCTRL_X0Y16                                                   r  clk_IBUF_BUFG_inst/I
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)         0.096     2.843 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.612     4.456    clk_IBUF_BUFG
    SLICE_X63Y75                                                     r  state_reg[1]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X63Y75         FDPE (Prop_fdpe_C_Q)         0.419     4.875 r  state_reg[1]/Q
                         net (fo=6, routed)           0.723     5.598    n_0_state_reg[1]
    SLICE_X63Y75                                                     r  state[1]_i_1/I2
    SLICE_X63Y75         LUT4 (Prop_lut4_I2_O)        0.324     5.922 r  state[1]_i_1/O
                         net (fo=1, routed)           0.000     5.922    n_0_state[1]_i_1
    SLICE_X63Y75         FDPE                                        r  state_reg[1]/D
  -------------------------------------------------------------------    -------------------
                         (clock my_only_clock rise edge)
                                                     10.000    10.000 r
    E3                                                0.000    10.000 r  clk
                         net (fo=0)                   0.000    10.000    clk
    E3                                                               r  clk_IBUF_inst/I
    E3                   IBUF (Prop_ibuf_I_O)         0.833    10.833 r  clk_IBUF_inst/O
                         net (fo=1, routed)           1.683    12.516    clk_IBUF
    BUFGCTRL_X0Y16                                                   r  clk_IBUF_BUFG_inst/I
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)         0.091    12.607 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.494    14.102    clk_IBUF_BUFG
    SLICE_X63Y75                                                     r  state_reg[1]/C
                         clock pessimism              0.354    14.456
                         clock uncertainty           -0.035    14.420
    SLICE_X63Y75         FDPE (Setup_fdpe_C_D)        0.075    14.495    state_reg[1]
  -------------------------------------------------------------------
                         required time                         14.495
                         arrival time                          -5.922
  -------------------------------------------------------------------
                         slack                                  8.574
```

Timing Report Detail: Create Clock (Hold - Min / Fast)

```
Slack (MET) :             0.395ns  (arrival time - required time)
  Source:                 state_reg[1]/C (rising edge-triggered cell FDPE clocked by my_only_clock  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            state_reg[1]/D (rising edge-triggered cell FDPE clocked by my_only_clock  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             my_only_clock
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (my_only_clock rise@0.000ns - my_only_clock rise@0.000ns)
  Data Path Delay:        0.502ns  (logic 0.226ns (45.017%)  route 0.276ns (54.983%))
  Logic Levels:           1  (LUT4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.839ns
    Source Clock Delay      (SCD):    1.334ns
    Clock Pessimism Removal (CPR):    0.504ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock my_only_clock rise edge)
                                                      0.000     0.000 r
    E3                                                0.000     0.000 r  clk
                         net (fo=0)                   0.000     0.000    clk
    E3                                                          r  clk_IBUF_inst/I
    E3                   IBUF (Prop_ibuf_I_O)         0.196     0.196 r  clk_IBUF_inst/O
                         net (fo=1, routed)           0.558     0.754    clk_IBUF
    BUFGCTRL_X0Y16                                              r  clk_IBUF_BUFG_inst/I
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)         0.026     0.780 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           0.555     1.334    clk_IBUF_BUFG
    SLICE_X63Y75                                                r  state_reg[1]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X63Y75         FDPE (Prop_fdpe_C_Q)         0.128     1.462 r  state_reg[1]/Q
                         net (fo=6, routed)           0.276     1.738    n_0_state_reg[1]
    SLICE_X63Y75                                                r  state[1]_i_1/I2
    SLICE_X63Y75         LUT4 (Prop_lut4_I2_O)        0.098     1.836 r  state[1]_i_1/O
                         net (fo=1, routed)           0.000     1.836    n_0_state[1]_i_1
    SLICE_X63Y75         FDPE                                   r  state_reg[1]/D
  -------------------------------------------------------------------    -------------------
                         (clock my_only_clock rise edge)
                                                      0.000     0.000 r
    E3                                                0.000     0.000 r  clk
                         net (fo=0)                   0.000     0.000    clk
    E3                                                          r  clk_IBUF_inst/I
    E3                   IBUF (Prop_ibuf_I_O)         0.385     0.385 r  clk_IBUF_inst/O
                         net (fo=1, routed)           0.603     0.987    clk_IBUF
    BUFGCTRL_X0Y16                                              r  clk_IBUF_BUFG_inst/I
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)         0.029     1.016 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           0.823     1.839    clk_IBUF_BUFG
    SLICE_X63Y75                                                r  state_reg[1]/C
                         clock pessimism             -0.504     1.334
    SLICE_X63Y75         FDPE (Hold_fdpe_C_D)         0.107     1.441    state_reg[1]
  -------------------------------------------------------------------
                         required time                         -1.441
                         arrival time                           1.836
  -------------------------------------------------------------------
                         slack                                  0.395
```

Timing Report Detail: Unconstrained (Rec - Max / Slow)

```
Slack:                    inf
  Source:                 rst (input port)
  Destination:            state_reg[0]/PRE
  (recovery check against rising-edge clock my_only_clock  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             (none)
  Path Type:              Recovery (Max at Slow Process Corner)
  Data Path Delay:        5.092ns  (logic 0.989ns (19.422%)  route 4.103ns (80.578%))
  Logic Levels:           1  (IBUF=1)
  Clock Path Skew:        4.102ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.102ns
    Source Clock Delay      (SCD):    0.000ns
    Clock Pessimism Removal (CPR):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    A18                                               0.000     0.000 f  rst
                         net (fo=0)                   0.000     0.000    rst
    A18                                                         f  rst_IBUF_inst/I
    A18                  IBUF (Prop_ibuf_I_O)         0.989     0.989 f  rst_IBUF_inst/O
                         net (fo=2, routed)           4.103     5.092    rst_IBUF
    SLICE_X63Y75         FDPE                                        f  state_reg[0]/PRE
  -------------------------------------------------------------------    -------------------
                         (clock my_only_clock rise edge)
                                                      0.000     0.000 r
    E3                                                0.000     0.000 r  clk
                         net (fo=0)                   0.000     0.000    clk
    E3                                                          r  clk_IBUF_inst/I
    E3                   IBUF (Prop_ibuf_I_O)         0.833     0.833 r  clk_IBUF_inst/O
                         net (fo=1, routed)           1.683     2.516    clk_IBUF
    BUFGCTRL_X0Y16                                              r  clk_IBUF_BUFG_inst/I
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)         0.091     2.607 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)           1.494     4.102    clk_IBUF_BUFG
    SLICE_X63Y75                                                r  state_reg[0]/C
```

Timing Report Detail: Unconstrained (Rem - Min / Fast)

```
Slack:                    inf
  Source:                 rst (input port)
  Destination:            state_reg[0]/PRE
  (removal check against rising-edge clock my_only_clock  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             (none)
  Path Type:              Removal (Min at Fast Process Corner)
  Data Path Delay:        2.024ns  (logic 0.218ns (10.746%)  route 1.807ns (89.254%))
  Logic Levels:           1  (IBUF=1)
  Clock Path Skew:        1.839ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.839ns
    Source Clock Delay      (SCD):    0.000ns
    Clock Pessimism Removal (CPR):    -0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    A18                                                  0.000     0.000 f  rst
                         net (fo=0)                      0.000     0.000    rst
    A18                                                                f  rst_IBUF_inst/I
    A18                  IBUF (Prop_ibuf_I_O)            0.218     0.218 f  rst_IBUF_inst/O
                         net (fo=2, routed)              1.807     2.024    rst_IBUF
    SLICE_X63Y75         FDPE                                           f  state_reg[0]/PRE
  -------------------------------------------------------------------    -------------------
                         (clock my_only_clock rise edge)
                                                         0.000     0.000 r
    E3                                                   0.000     0.000 r  clk
                         net (fo=0)                      0.000     0.000    clk
    E3                                                                 r  clk_IBUF_inst/I
    E3                   IBUF (Prop_ibuf_I_O)            0.385     0.385 r  clk_IBUF_inst/O
                         net (fo=1, routed)              0.603     0.987    clk_IBUF
    BUFGCTRL_X0Y16                                                     r  clk_IBUF_BUFG_inst/I
    BUFGCTRL_X0Y16       BUFG (Prop_bufg_I_O)            0.029     1.016 r  clk_IBUF_BUFG_inst/O
                         net (fo=2, routed)              0.823     1.839    clk_IBUF_BUFG
    SLICE_X63Y75                                                       r  state_reg[0]/C
```

Timing Report Detail: Pulse Width Checks

Pulse Width Checks

Clock Name: my_only_clock
Waveform: { 0 5 }
Period: 10.000
Sources: { clk }

Check Type	Corner	Lib Pin	Reference Pin	Required	Actual	Slack	Location	Pin
Min Period	n/a	BUFG/I	n/a	2.155	10.000	7.845	BUFGCTRL_X0Y16	clk_IBUF_BUFG_inst/I
Min Period	n/a	FDPE/C	n/a	1.000	10.000	9.000	SLICE_X63Y75	state_reg[0]/C
Min Period	n/a	FDPE/C	n/a	1.000	10.000	9.000	SLICE_X63Y75	state_reg[1]/C
Low Pulse Width	Fast	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[0]/C
Low Pulse Width	Fast	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[1]/C
Low Pulse Width	Slow	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[0]/C
Low Pulse Width	Slow	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[1]/C
High Pulse Width	Slow	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[0]/C
High Pulse Width	Slow	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[1]/C
High Pulse Width	Fast	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[0]/C
High Pulse Width	Fast	FDPE/C	n/a	0.500	5.000	4.500	SLICE_X63Y75	state_reg[1]/C

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