San José State University
Department of Electrical Engineering
EE223, Analog Integrated Circuits
Number 22911, Section 01, Fall 2016

Instructor:	Prof. Hamedi-Hagh
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Office Hours:	Tuesdays 10:15 to 11:30 and 15:30 to 16:30
Class Schedule:	Tuesdays/Thursdays 16:30-17:45
Classroom:	HGH122
Prerequisites:	Graduate Standing

Course Description:

This course studies nanoscale metal-oxide semiconductor field effect transistor (MOSFET) modeling and circuit design techniques for analog integrated circuit applications. Course topics include short channel issues, layout techniques to improve design performance, noise modeling and transformation, wide-swing current mirrors, gain, bandwidth and voltage swing characteristics of single-stage and two-stage amplifiers. A variety of opamp architectures with their slew rate, settling time, phase margin, stability, gain and bandwidth will be discussed in details.

Required Textbook:

- Analog Integrated Circuit Design, 2nd Edition, by Tony Chan Carusone, David A. Johns and Ken Martin, Wiley, 2011. http://analogicdesign.com

Other Reference Materials:

- Analysis and Design of Analog Integrated Circuits, 5th Edition, by Gray, Hurst, Lewis and Meyer, Wiley, 2009.
- Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill, 2001.

Grading:

assignments	10%
midterm exam	20%
design project	30%
final exam	40%

Grading Percentage Breakdown:

90% and above	A
89% - 85%	A-
84% - 82%	B+
81% - 79%	B
78% - 75%	B-
74% - 72%	C+
71% - 69%	C
68% - 65%	C-
64% - 62%	D+
61% - 59%	D
58% - 55%	D-
below 55%	F

Exams:

The date of the exams is shown on the course syllabus. Exams will be closed book. However, students are allowed to bring 1 page of aid sheet. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams.

Projects:

Assignments and projects are mainly based on Cadence and are closely relate to topics discussed in this course. Cadence will not be taught in this course and students are required to master this CAD tool by themselves. Each group (maximum 4 students) must write a formal project report using a word processor (i.e. Microsoft Office) and submit the original write-up including all data, images and graphs in a CD and by email before deadline to be eligible to receive a credit. Students may be required to present their works similar to standard design reviews as conducted in industry. Non restricted MOSFET transistor models will be provided for assignments and projects. More details on design projects will be provided as the lectures progress. **Please look under the EE223 course menu in http://www.ics.sjsu.edu to download the related materials**.

Academic Integrity Statement:

Your own commitment to learning, as evidenced by your enrollment at San Jose State University, and the University's Academic Integrity Policy requires you to be honest in all your academic course work. Faculty members are required to report all infraction to the Office of Student Conduct and Ethical Development. The policy on academic integrity can be found at http://sa.sjsu.edu/student_conduct

Students in this course are expected to maintain high ethical standards in all matters pertaining to the course, including, but not limited to, examinations, homework, course assignments, presentations, writing, laboratory work, team work, treatment of class members, and behavior in class. Cheating and plagiarism are violations of the SJSU Policy on Academic Dishonesty (S98-1) and will not be tolerated in the class. Students are expected to have read the Policy, which is available at http://www2.sjsu.edu/senate/S014-12.pdf

Campus Policy in Compliance with the Americans with Disabilities Act:

If you need course adaptations or accommodations because of a disability, if you have emergency medical information to share or if you need to make special arrangements in case the building must be evacuated, please make an appointment with your course instructor or see him/her during office hours as soon as possible.

Course Goals:

1. Students will be able to design advanced biasing circuits, opamps, comparators and switch-capacitor circuits.

2. Students will be able to understand the concept of noise, distortion, stability, phase margin, voltage swing, slew-rate and gain-bandwidth product.

3. Students will be able to use modern engineering CAD tools for computations, simulations, analysis, and design.

4. Students will be able to verify the theory with hands-on lab simulations.

Course Learning Objectives:

- The ability to characterize and model transistors
- The ability to biasing and operate transistors as amplifiers
- The ability to design amplifiers with different characteristics
- The ability to design high performance layout with minimum parasitic
- The ability to utilize simulation tools to characterize complex Analog integrated circuits
- The ability to determine the trade-off among linearity, bandwidth, gain and power dissipation of amplifiers
- The ability to design stable multi-stage amplifiers
- The ability to apply frequency compensation techniques for amplifiers

Tentative Course Syllabus and Schedule

Date	Topics
08/25	Introduction to Analog Integrated Circuit Design
08/30	Operation and Biasing of Short-Channel MOSFETs
09/01	Intrinsic and Extrinsic MOSFET Models
09/06	Small-Signal Parameters of MOSFETs
09/08	Process Variation and Layout Techniques
09/13	DC and AC Analyses
09/15	Effective Resistance at Source and Drain Terminals **(*the first assignment is due during this lecture, 5% grade*)**
09/20	Current Mirrors
09/22	DC Error and High Frequency Modeling of Current Mirrors
09/27	Common Gate Biasing
09/29	Common Gate A_{v0}, ω_{p1}, ω_{p2}
10/04	Common Gate R_{in}, R_{out}
10/06	Calculating Gain and Bandwidth by Indirect Approaches **(*the second assignment is due during this lecture, 5% grade)***
10/11	Common Source Biasing, R_{in} and R_{out}
10/13	Common Source A_{v0}, ω_{p1}, ω_{p2} and ω_z
10/18	Common Drain Biasing, R_{in} and R_{out}
10/20	Common Drain A_{v0}, ω_{p1}, ω_{p2} and ω_z
10/25	***Midterm Exam, 75 minutes, 20% grade***
10/27	Left and Right Hand Poles and Zeros
11/01	Estimating Resistance and Capacitance (gain and bandwidth) at any Node **(*project proposal is due during this lecture, 5% grade)***
11/03	Cascode Amplifiers
11/08	Folded Cascode Amplifiers
11/10	Source Degeneration Amplifiers
11/15	Diff-Pair Amplifiers and Common Mode Rejection Ratio
11/17	Single-Ended and Fully Differential Amplifiers
11/22	Opamp Frequency Compensation and Pole Splitting
11/29	Opamp Voltage Swing and Slew Rate
12/01	Design of Common Mode Feedbacks
12/06	Projects A, B, C, D, E and F Review ***(5% grade)***
12/08	Projects G, H, I, J, K and L Review ***(5% grade)***
12/13	Study/Conference Day ***(online project submission due by noon, 20% grade)***
12/19	***Final Exam, from 14:45 — 17:00, 40% grade***

Holidays: 09/05 and 11/24