UNIVERSITY OF CALIFORNIA, BERKELEY

College of Engineering
Department of Electrical Engineering and Computer Sciences

Jan M. Rabaey **Homework #5** **EECS 141 (SP10)**

Due Friday, March 5, 5pm, box in 240 Cory

[PROBLEM 1] Elmore Delay (30pts)

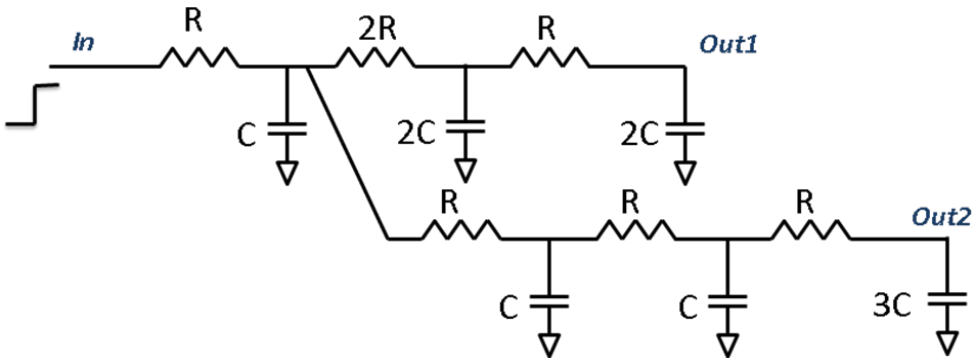


Fig. 1(a) RC Network

(a) A RC network is shown in Fig. 1(a). Calculate the Elmore delay from ***In*** to ***Out1*** and from ***In*** to ***Out2***. Which one is critical path? (10 pts)

Solution:

(1) From ***In*** to ***Out1***:

$$\tau_{in\_out1} = [RC + (R+2R)\cdot 2C + (R+2R+R)\cdot 2C] + [R\cdot(C+C+3C)] = 20RC$$

From ***In*** to ***Out2***:

$$\tau_{in\_out2} = [R\cdot C + (R+R)C + (R+R+R)\cdot C + (R+R+R+R)\cdot 3C] + [R\cdot(C+2C+2C)] = 22RC$$

The Elmore delay from ***In*** to ***Out1***is 20RC and the Elmore delay from ***In*** to ***Out2***is 22RC. So the critical path is from ***In*** to ***Out2***.

Note: Elmore Delay is just a time constant for this network. If you want to calculate the propagation delay:

$$Td_{in\_out1} = 0.69 * \tau_{in\_out1}$$
$$Td_{in\_out2} = 0.69 * \tau_{in\_out2}$$

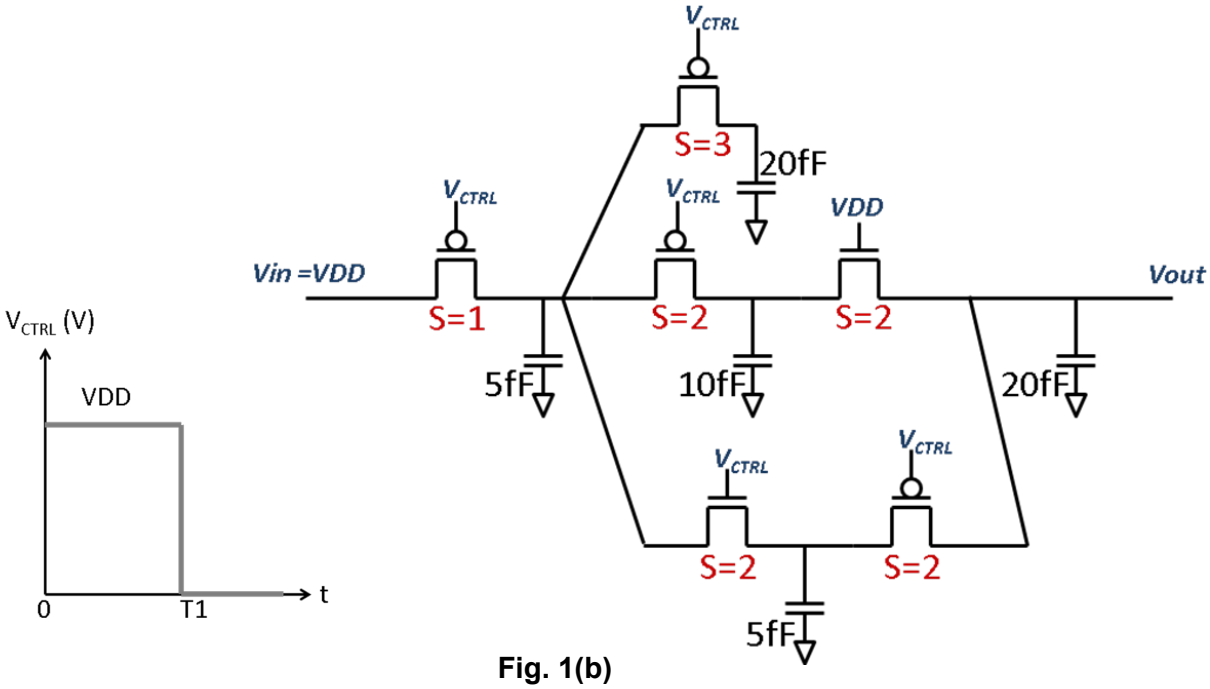


Fig. 1(b)

Consider the circuit in Fig.1(b), we will use an equivalent resistor-capacitor model and Elmore delay to estimate propagation delay of the circuit.

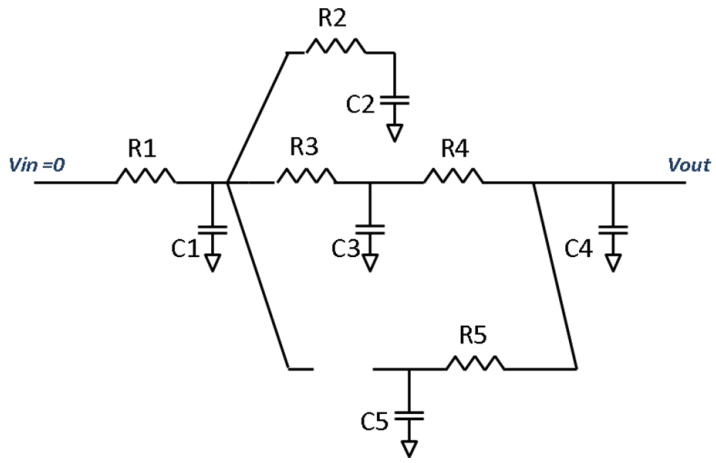
The size of the transistors is indicated as S. (S=1 means the minimum size, $W=W_{min}$; S=2 means $W=2xW_{min}$, etc.) Assume the following parameters for the minimum-size NMOS and PMOS transistors, S=1: $R_{eqNMOS}=10k\Omega$, $R_{eqPMOS}=20k\Omega$, $C_{gs}=C_{gd}=0.5fF$; $C_{db}=C_{sb}=1fF$. Ignore overlap capacitances and feed-through from the gates of the switching transistors to the circuit nodes.

Assume all nodes (except Vin) are initially at 0V. A voltage waveform V_{CTRL} shown in Fig.1(b) is applied to the circuit.

(b) Draw the equivalent R-C circuit after t=T1 including all relevant resistors and capacitors and indicate their values. (10 pts)

Solution:

(1) After t=T1, the equivalent R-C circuit is :



Component values:

R1=R_{eqPMOS}=20kΩ
C1=5fF+6C_{gs}+8C_{db}=5fF+3fF+8fF=16fF
R2=R_{eqPMOS}/3=6.67kΩ
C2=20fF+3C_{gs}+3C_{db}=20fF+1.5fF+3fF=24.5fF
R3=R_{eqPMOS}/2=10kΩ
C3=10fF+4C_{gs}+4C_{db}=16fF
R4=R_{eqNMOS}/2=5kΩ
C4=20fF+4C_{gs}+4C_{db}=20fF+2fF+4fF=26fF
R5=R_{eqPMOS}/2=10kΩ
C5=5fF+2C_{gs}+4C_{db}=10fF

(c) From the equivalent model, calculate the delay between t=T1 and the time when Vout=VDD/2 (Assume VDD is much larger than V_T, i.e. VDD>>V_T). (10 pts)

Solution:

The equivalent circuit satisfies the conditions for an RC tree (see pg. 153). Therefore we can use Eq. 4.13 to find the equivalent time-constant:

$$\tau_{vout} = R1 \cdot C1 + R1 \cdot C2 + (R1 + R3) \cdot C3 + (R1 + R3 + R4) \cdot C4 + (R1 + R3 + R4) \cdot C5 = 2.55ns$$

The propagation delay is:

$$T_{pLH} = 0.69 \cdot \tau_{vout} = 1.76ns$$

[PROBLEM 2] MOS Capacitance and Delay (40 pts)

In this problem, you are going to learn how to calculate various capacitances of an inverter and use this information to estimate propagation delay.

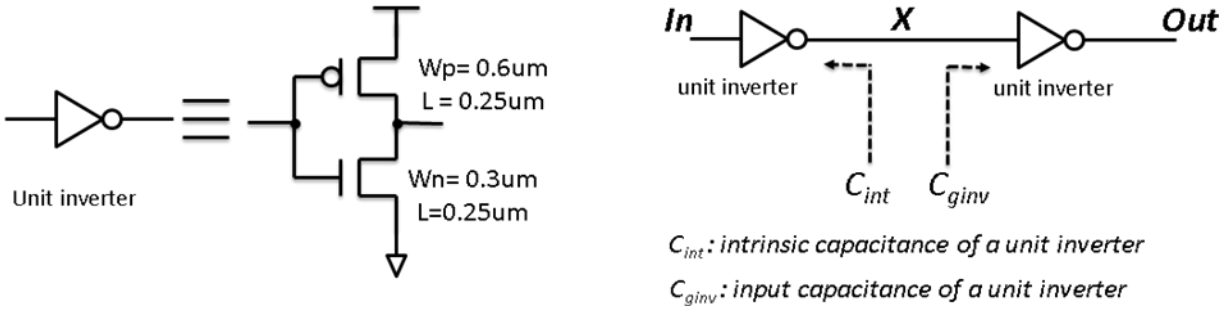


Fig. 2(a)

(a) Use the following technology parameters from the textbook to calculate the equivalent C_{int_LH}, C_{int_HL}, C_{ginv_LH}, and C_{ginv_HL} (at node X) of a unit size inverter in shown in Fig. 2(a). (Example: C_{int_LH} means the intrinsic capacitance in Low->High transition) Assume the supply is 2.5V and the inverter switches at VDD/2. Also assume for a unit-size inverter: AS_n= AD_n=0.25μm^2, PS_n= PD_n=1.5μm, AS_p= AD_p=0.3μm^2, PS_p= PD_p=3μm. (20 pts)

	NMOS	PMOS
Cox	6 fF/um^2	6 fF/um^2
Co	0.31 fF/um	0.27 fF/um
Cj	2 fF/um^2	1.9 fF/um^2
mj	0.5	0.48
Cjsw	0.28 fF/μm	0.22 fF/um
mjsw	0.44	0.32
Φ0	0.9	0.9

Solution:

$$C_{ginvLH} = C_{ginv} = C_{gn} + C_{gp} = W_n L_n C_{ox} + W_p L_p C_{ox} + 2W_n C_o + 2W_p C_o = 1.86\,fF$$
$$C_{ginvHL} = C_{ginvLH} = 1.86\,fF$$

For the junction capacitance, let's first calculate K_{eq} using the following equation:

$$K_{eq} = \frac{-\phi_0^{\,m}}{(V_{high} - V_{low})(1-m)}[(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}] \Rightarrow$$

$$K_{eqnHL} = \frac{-0.9^{0.5}}{(-2.5+1.25)(1-0.5)}[(0.9+2.5)^{1-0.5} - (0.9+1.25)^{1-0.5}] = 0.57$$

$$K_{eqnLH} = \frac{-0.9^{0.5}}{(-1.25+0)(1-0.5)}[(0.9+1.25)^{1-0.5} - (0.9+0)^{1-0.5}] = 0.79$$

$$K_{eqpHL} = \frac{-0.9^{0.48}}{(-1.25+0)(1-0.48)}[(0.9+1.25)^{1-0.48} - (0.9+0)^{1-0.48}] = 0.79$$

$$K_{eqpLH} = \frac{-0.9^{0.48}}{(-2.5+1.25)(1-0.48)}[(0.9+2.5)^{1-0.48} - (0.9+1.25)^{1-0.48}] = 0.59$$

$$K_{eqswnHL} = \frac{-0.9^{0.44}}{(-2.5+1.25)(1-0.44)}[(0.9+2.5)^{1-0.44} - (0.9+1.25)^{1-0.44}] = 0.61$$

$$K_{eqswnLH} = \frac{-0.9^{0.44}}{(-1.25+0)(1-0.44)}[(0.9+1.25)^{1-0.44} - (0.9+0)^{1-0.44}] = 0.81$$

$$K_{eqswpHL} = \frac{-0.9^{0.32}}{(-1.25+0)(1-0.32)}[(0.9+1.25)^{1-0.32} - (0.9+0)^{1-0.32}] = 0.86$$

$$K_{eqswpLH} = \frac{-0.9^{0.32}}{(-2.5+1.25)(1-0.32)}[(0.9+2.5)^{1-0.32} - (0.9+1.25)^{1-0.32}] = 0.70$$

We can therefore calculate junction capacitances:

$$C_{dbnLH} = AD_n \cdot K_{eqnLH} \cdot C_{jn} + PD_n \cdot K_{eqswnLH} \cdot C_{jswn} = 0.72\,fF$$
$$C_{dbnHL} = AD_n \cdot K_{eqnHL} \cdot C_{jn} + PD_n \cdot K_{eqswnHL} \cdot C_{jswn} = 0.54\,fF$$
$$C_{dbpLH} = AD_p \cdot K_{eqpLH} \cdot C_{jp} + PD_p \cdot K_{eqswpLH} \cdot C_{jswp} = 1\,fF$$
$$C_{dbpHL} = AD_p \cdot K_{eqpHL} \cdot C_{jp} + PD_p \cdot K_{eqswpHL} \cdot C_{jswp} = 0.79\,fF$$

$$\Rightarrow C_{\text{int}\,LH} = 2W_nC_o + 2W_pC_o + C_{dbnLH} + C_{dbpLH} = 2.23\,fF$$
$$\Rightarrow C_{\text{int}\,HL} = 2W_nC_o + 2W_pC_o + C_{dbnHL} + C_{dbpHL} = 1.84\,fF$$

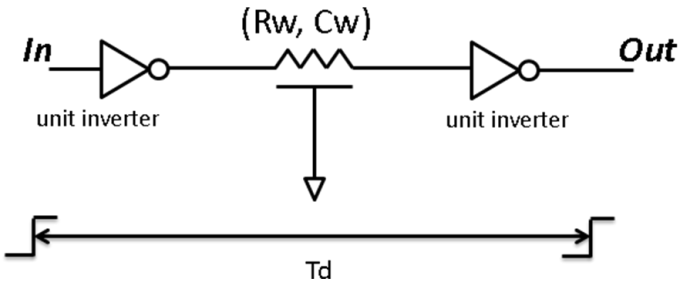


Fig. 2(b)

(b) As shown in Fig. 2(b), the first stage and the second stage are connected by a 80um long, 0.25um wide poly wire. Assume Rw = 150 Ω/□, Cw =0.09 fF/um^2 and the distributed model for the poly wire; R_{eqNMOS} = 10 kΩ and R_{eqPMOS} = 12 kΩ for NMOS and PMOS in a unit size inverter. Use the equivalent capacitances you found in part (a) to calculate propagation delay T_{d_LH} and T_{d_HL}. (20 pts)

Solution:

The capacitance and resistance from the poly wire:

$$C_W = C_w \cdot l \cdot W = 0.09 * 80 * 0.25 = 1.8 fF$$

$$R_W = R_w \cdot (l / W) = 150 * 80 / 0.25 = 48 K\Omega$$

$$\Rightarrow T_{d\_LH} = 0.38 R_W C_W + 0.69(R_{eqNMOS} C_{\text{int}\,HL} + R_{eqNMOS} C_W + R_{eqNMOS} C_{ginv\_LH} + R_W C_{ginv\_LH} + R_{eqPMOS} C_{\text{int}\,LH}) = 163.16 pS$$

$$\Rightarrow T_{d\_HL} = 0.38 R_W C_W + 0.69(R_{eqPMOS} C_{\text{int}\,LH} + R_{eqPMOS} C_W + R_{eqPMOS} C_{ginv\_HL} + R_W C_{ginv\_HL} + R_{eqNMOS} C_{\text{int}\,HL}) = 188.41 pS$$

[PROBLEM 3] MOS Capacitance and VTC revisited (30 pts)

A three-transistor circuit is shown in Fig.3. Assume VDD = 2.5V and input signal switches between 0 and VDD with sharp rise and fall times. Use the transistor parameters below and ignore body effect. All transistors have minimum length, L = 0.25 um. The widths of transistor M2 and M1: W_{M2} = 2um, W_{M1} = 1um.

NMOS:
$V_{Tn} = 0.4$, k'n = 115 uA/V^2, $V_{D,VSAT} = 0.6V$, $\lambda = 0$, $\gamma = 0.4\ V^{1/2}$, $2\phi_f = -0.6V$

PMOS:
$V_{Tp} = -0.4V$, k'p = –30 uA/V^2, $V_{D,VSAT} = -1V$, $\lambda = 0$, $\gamma = -0.4\ V^{1/2}$, $2\phi_f = 0.6V$

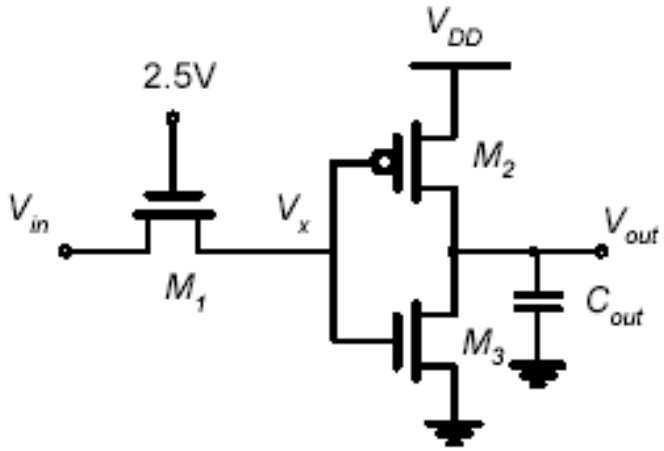


Fig. 3

(a) Find the width of transistor M3, W_{M3}, such that the switching threshold of the inverter (V_M) is placed in the middle of the V_X signal swing. (10 pts) Hint: find out the signal swing at Vx first.

Solution:

Since we ignore body effect, the highest voltage at Vx=V_{DD}-V_{Tn}=2.5-0.4=2.1;
The lowest voltage at Vx=0. We want to make V_M=(2.1-0)/2=1.05 which is in the middle of Vx signal swing.

Equating the short channel current equations for both NMOS(M3) and PMOS(M2)

$$\frac{W_3}{L}\cdot 115\left[(1.05-0.4)\cdot 0.6-\frac{0.6^2}{2}\right]=\frac{W_2}{L}\cdot 30\left[(2.5-1.05-0.4)\cdot 1-\frac{1^2}{2}\right]$$

W_2/W_3=(115/30)*[(1.05-0.4)*0.6-0.36/2]/[(2.5-1.05-0.4)*1-1/2]=1.46
$W_3=W_2$/1.46=1.37um

(b) If we increase the width of transistor M3 (leaving the width of transistor M2 fixed), in which direction will the VTC shift? Explain how the resizing of M3 affects the VTC. (5 pts)

Solution:

The VTC will shift to the left side because the NMOS with increased width has stronger pull-down strength.

(c) Find the t_{pLH} delay of this circuit. Cox = 6fF/um^2. Overlap capacitances are Co = 0.3 fF/um. Bottom-plate PN junction capacitances are 2fF/um of device width. Ignore the sidewall capacitances. Ignore the impact of rise/fall times on propagation delay. Cout = 10fF. (15 pts)

Solution:

We can divide the delay into two parts: from Vin to Vx and from Vx to Vout.

Part 1: From Vin to Vx

To estimate the delay in this part, we calculate the Req of M1 using this approximation: $R_{eqM1}=(R_{eqM1,begin}+R_{eqM1,end})/2$.

$R_{eqM1,\ begin}$: Vx=2.5-0.4=2.1(V)
Ix = $Kn(W/L)_1$[(2.5-0.4)*0.6-0.36/2] = 0.497 mA
$R_{eqM1,\ begin}$ = 4.225 KΩ

$R_{eqM1,\ end}$: Vx=1.05(V)
Ix = $Kn(W/L)_1$[(2.5-0.4)*0.6-0.36/2] = 0.497 mA
$R_{eq1,\ end}$ = 2.113 KΩ

$R_{eqM1} = (R_{eqM1,begin} + R_{eqM1,end})/2$ = 3.169 KΩ

$C_{eq,vx} = (C_{ox}LW_2+2C_oW_2)+ (C_{ox}LW_3+2C_oW_3)+C_{db1}+ C_oW_1$
=(6*0.25*2+2*0.3*2)+(6*0.25*1.37+2*0.3*1.37)+2*1+0.3*1=9.377fF

$t_{pHL,1}$ =0.69*$R_{eq,M1}C_{eq,vx}$ = 20.50 ps

Part 2: From Vx to Vout

R_{eqM2} = ¾*V_{DD}/I_{DSAT} = ¾*2.5/[Kp(W/L)(2.5-0.4)*1-0.5] = 4.883 KΩ

$C_{eq,vout} = C_{db2}+C_{db3}+2*(C_oW_2+ C_oW_3)+Cout$
=2*2+2*1.37+2*(0.3*2+0.3*1.37)+10 = 18.76 fF

$t_{pLH,2}$ = 0.69$R_{eq,M2}C_{eq,vout}$ = 63.2 ps

$t_{pLH,total}$ = 20.50+63.2= 83.7 ps