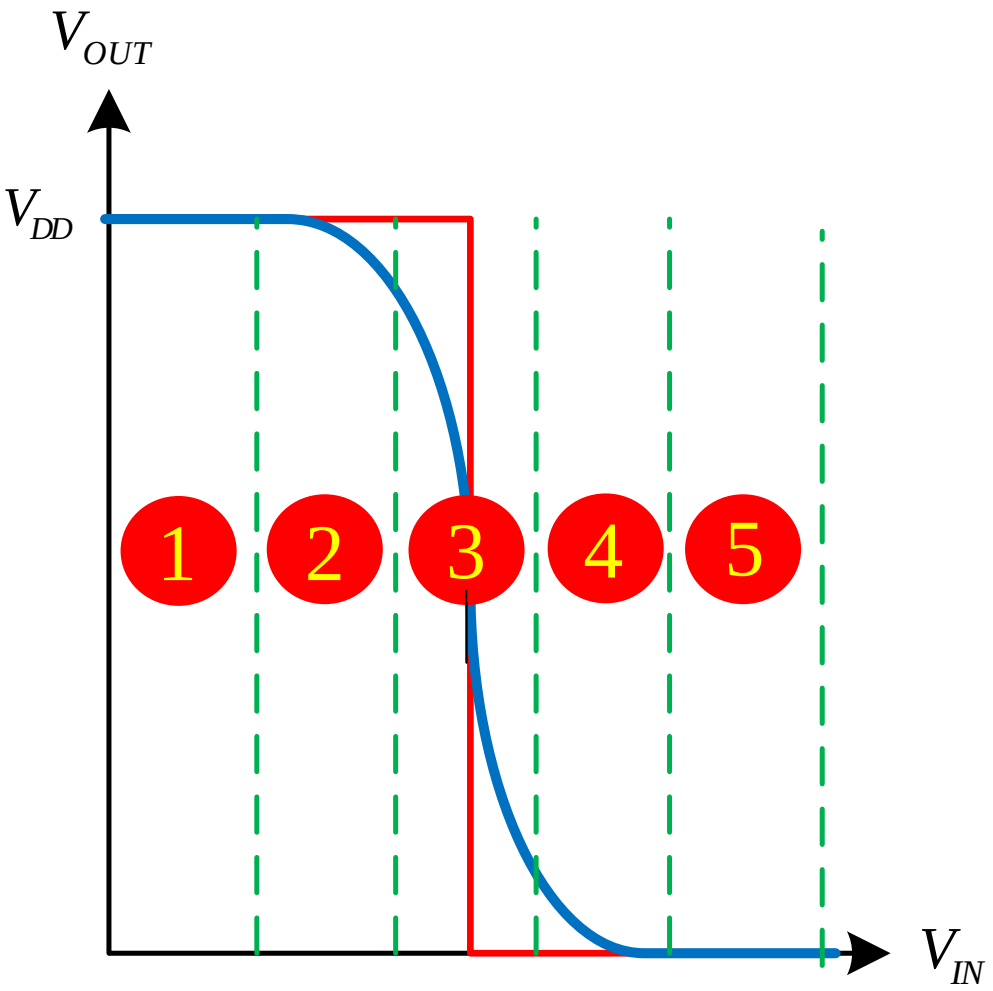
Inverter

Lecture 4

- Enhancement mode MOSFET transistor region of operation

	Cut-off	Resistive	Saturation
nMOS	$V_{GSn} < V_{Tn}$ $V_{IN} < V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} < V_{GSn} - V_{Tn}$ $V_{OUT} < V_{IN} - V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} > V_{GSn} - V_{Tn}$ $V_{OUT} > V_{IN} - V_{Tn}$
pMOS	$V_{GSp} > V_{Tp}$ $V_{IN} > V_{Tp} + V_{DD}$	$V_{GSp} < V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{Tp}$ $V_{OUT} > V_{IN} - V_{Tp}$	$V_{GSp} = V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{Tp}$ $V_{OUT} < V_{IN} - V_{Tp}$

- Inverter operating regions
- 1 nMOS Off
  pMOS Res.
- 2 nMOS Sat.
  pMOS Res.
- 3 nMOS Sat.
  pMOS Sat.
- 4 nMOS Res.
  pMOS Sat
- 5 nMOS Res.
  pMOS off



- Inverter operating regions
- 1 nMOS Off
  pMOS Res.
- 2 nMOS Sat.
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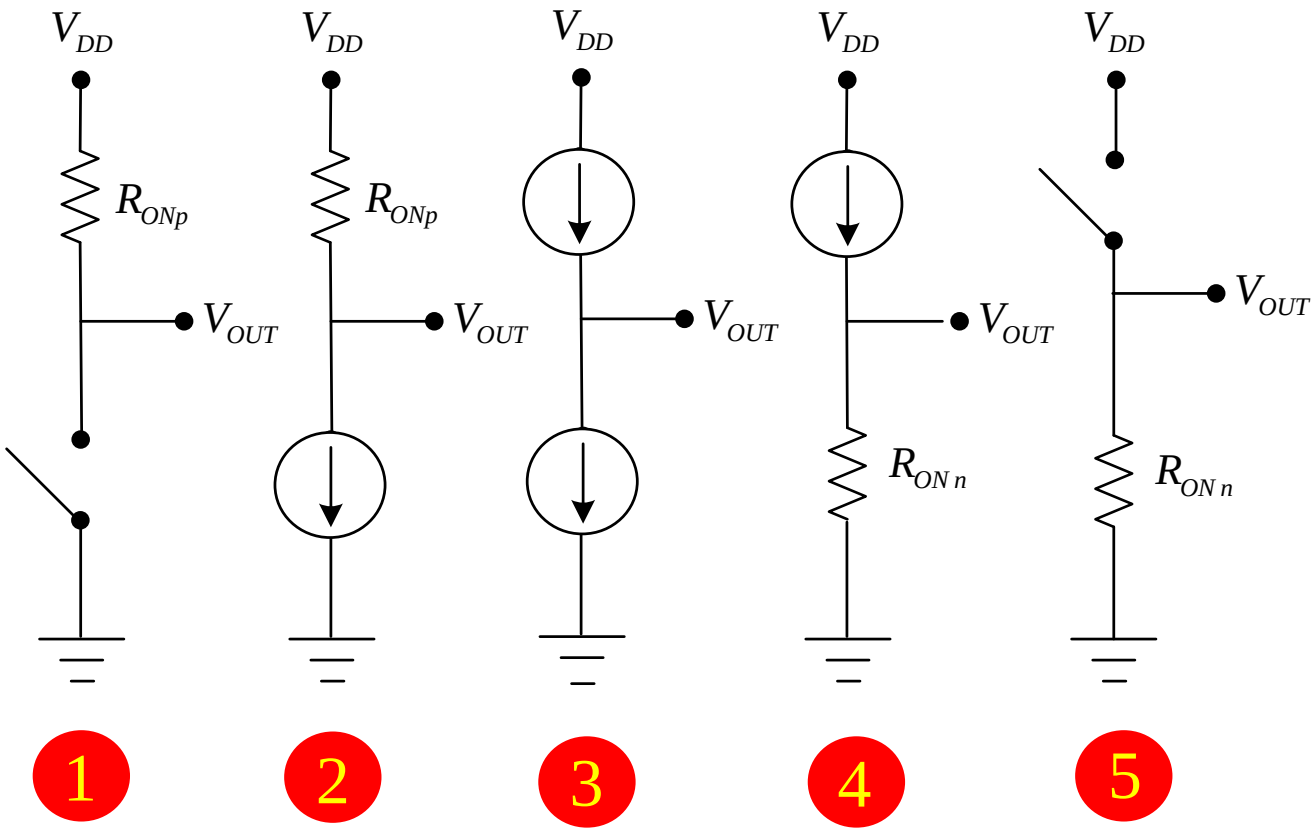
- 3 nMOS Sat.
  pMOS Sat.
- 4 nMOS Res.
  pMOS Sat
- 5 nMOS Res.
  pMOS off



- Inverter operating regions
- ❶ nMOS Off

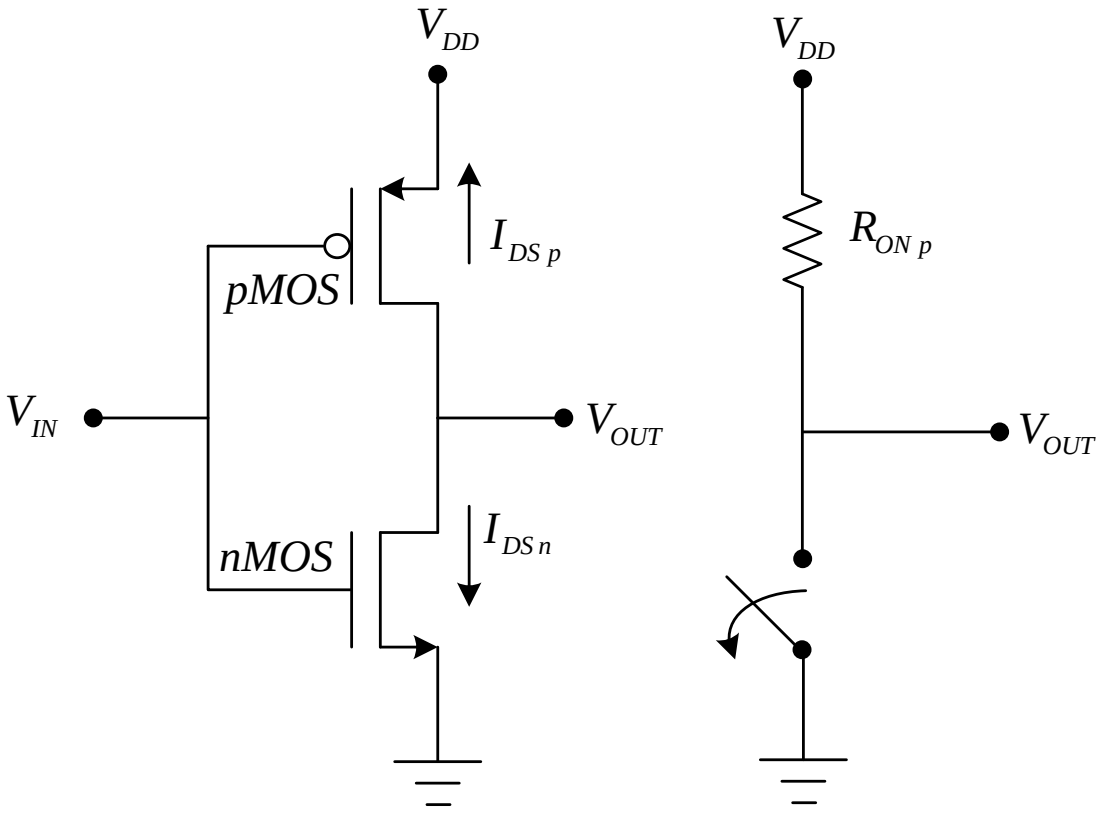
  pMOS Res.

$$I_{DSn} = -I_{DSp} = 0$$

$$V_{DSp} = V_{OUT} - V_{DD}$$

$$V_{DSp} = 0$$

$$V_{OUT} = V_{DD}$$



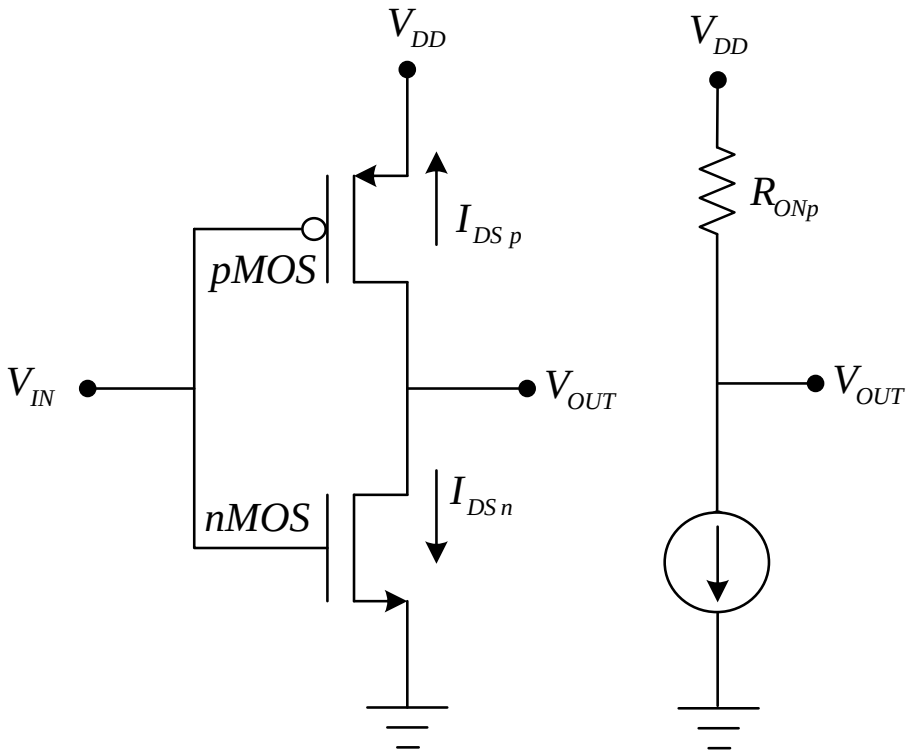
- Inverter operating regions
- ❷ nMOS Sat.
  pMOS Res.

$$V_{IN} \le V_{OUT} \le \frac{V_{DD}}{2}$$

$$I_{DSn} = k_n \frac{(V_{IN} - V_{Tn})^2}{2}$$

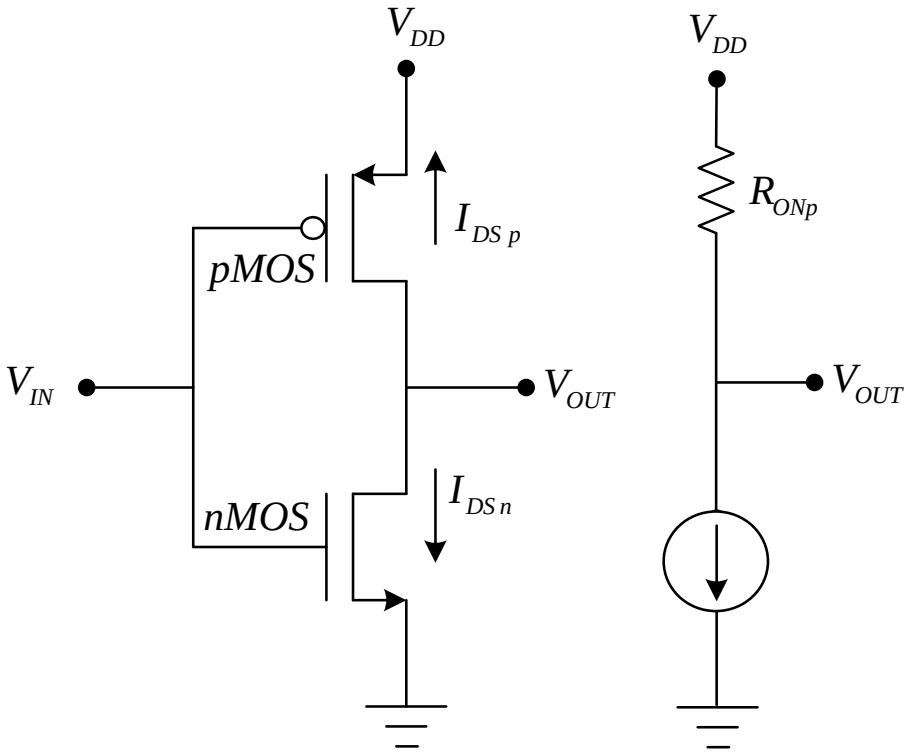
$$V_{GSp} = V_{IN} - V_{Tn}$$

$$V_{DSp} = V_{OUT} - V_{DD}$$



$$I_{DSp} = -k_p \left[(V_{IN} - V_{DD} - V_{Tp})(V_{OUT} - V_{DD}) - \frac{(V_{OUT} - V_{DD})^2}{2} \right]$$

- Inverter operating regions
- 2 nMOS Sat.
  pMOS Res.



$$I_{DSn} = -I_{DSp}$$

$$V_{OUT} = \left(V_{IN} - V_{Tp}\right) + \sqrt{\left(V_{IN} - V_{Tp}\right)^2 - 2\left(V_{IN} - \frac{V_{DD}}{2} - V_{Tp}\right)V_{DD} - \frac{k_n}{k_p}\left(V_{IN} - V_{Tp}\right)^2}$$

- Inverter operating regions
- ❸ nMOS Sat.

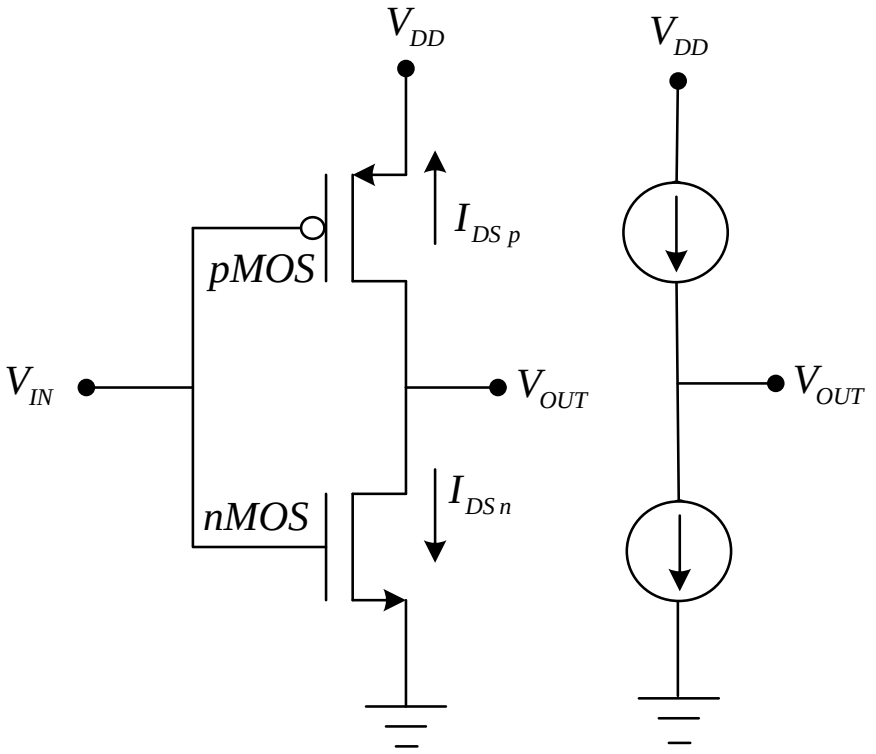
  pMOS Sat.

$$I_{DSn} = k_n \frac{(V_{IN} - V_{Tn})^2}{2}$$

$$I_{DSp} = -k_p \frac{(V_{IN} - V_{DD} - V_{Tp})^2}{2}$$

$$I_{DSn} = -I_{DSp}$$

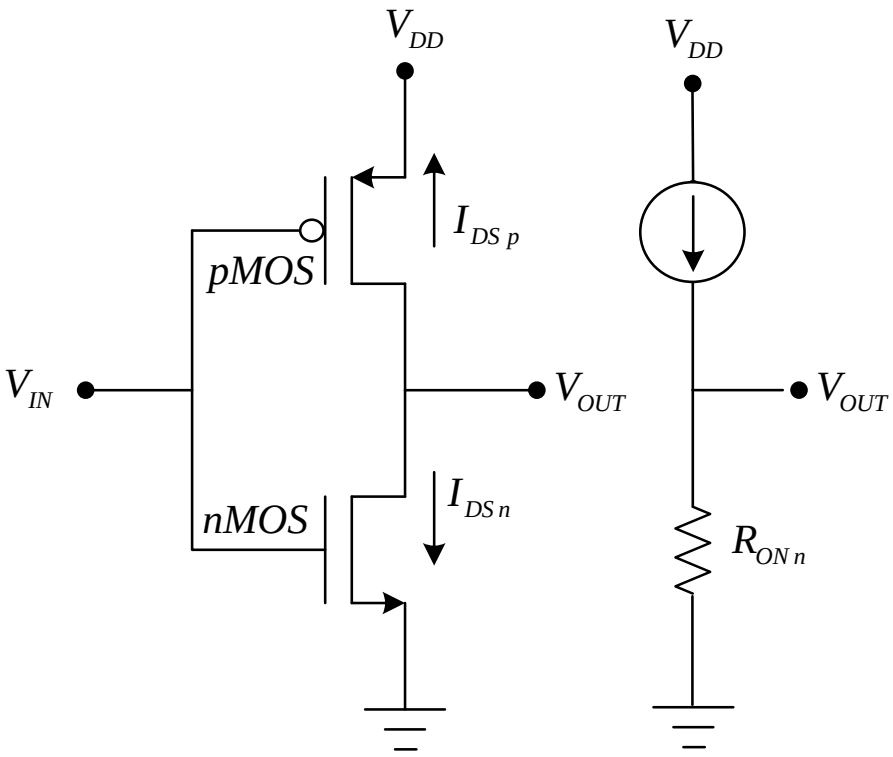
$$V_{IN} = \frac{V_{DD} + V_{Tp} + V_{IN}\sqrt{\frac{k_n}{k_p}}}{1 + \sqrt{\frac{k_n}{k_p}}}$$



- Inverter operating regions
- 4 nMOS Res.
  pMOS Sat

$$I_{DSn} = k_n\left[\left(V_{IN} - V_{Tn}\right)V_{OUT} - \frac{V_{OUT}^2}{2}\right]$$

$$I_{DSp} = -k_p\frac{\left(V_{IN} - V_{DD} - V_{Tn}\right)^2}{2}$$



$$I_{DSn} = -I_{DSp}$$

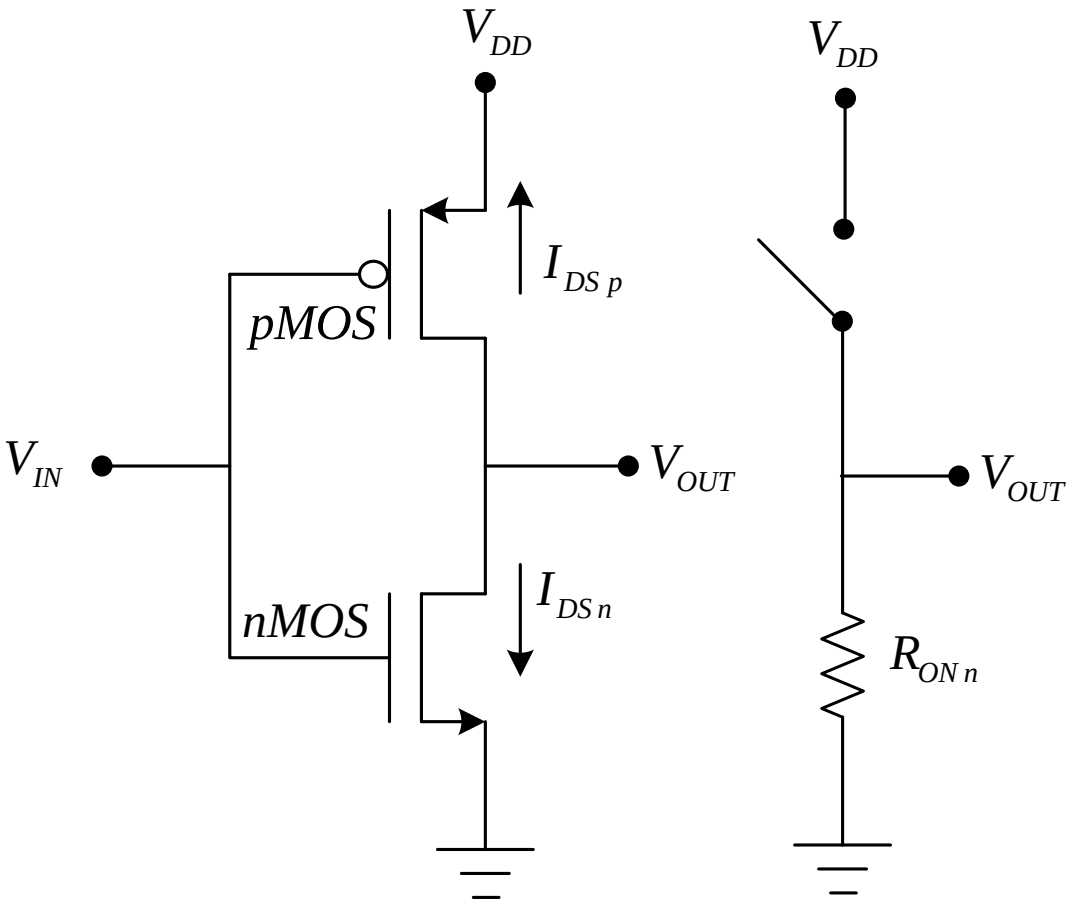
$$V_{OUT} = \left(V_{IN} - V_{Tn}\right) + \sqrt{\left(V_{IN} - V_{Tn}\right)^2 - \frac{k_p}{k_n}\left(V_{IN} - \frac{V_{DD}}{2} - V_{Tp}\right)^2}$$

- Inverter operating regions
- 5 nMOS Res.
  pMOS off

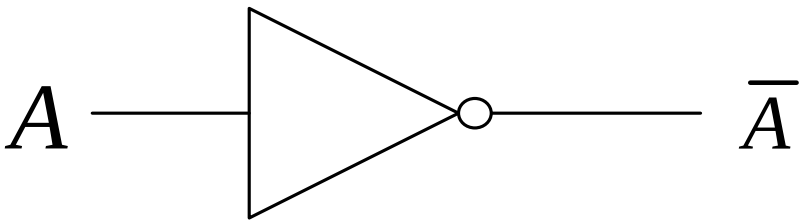
$$I_{DSp} = 0$$

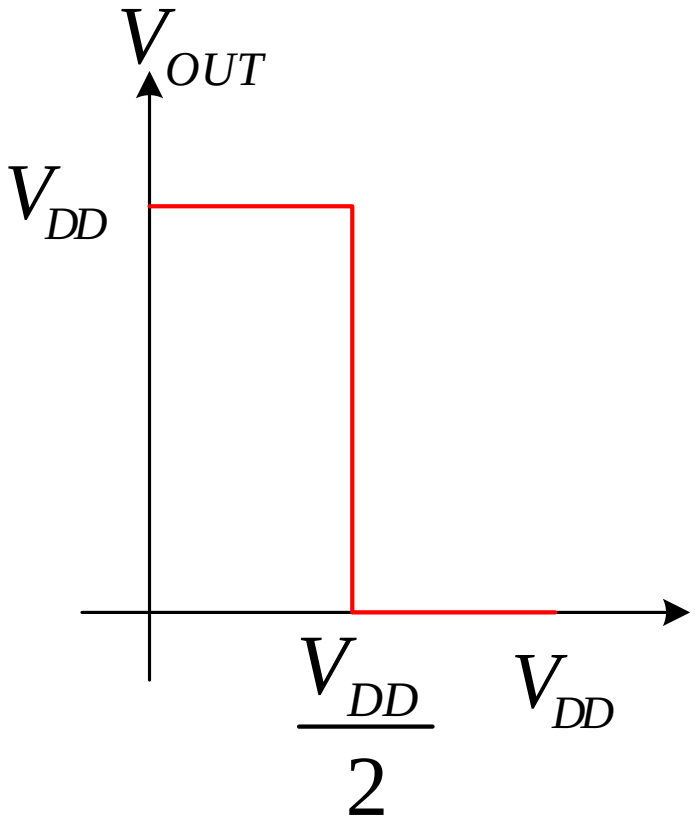
$$V_{GSp} = V_{IN} - V_{DD}$$

$$V_{OUT} = 0$$



- Ideal Inverter





- Switching Threshold

- The switching threshold defined as a voltage
- Where

$$V_M = V_{OUT} = V_{IN}$$

- Since

$$V_{GS} = V_{DS}$$

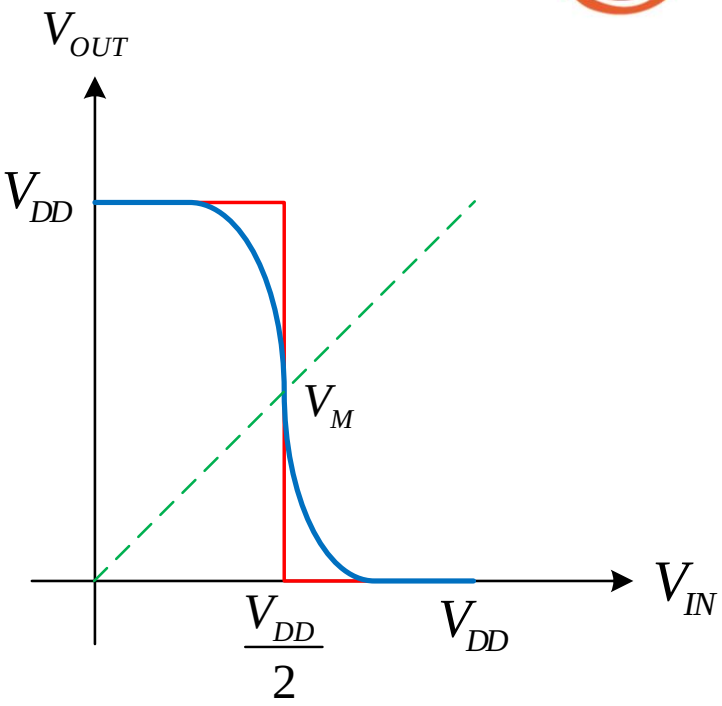
- Both pMOS and nMOS are in saturation.
- For velocity saturation

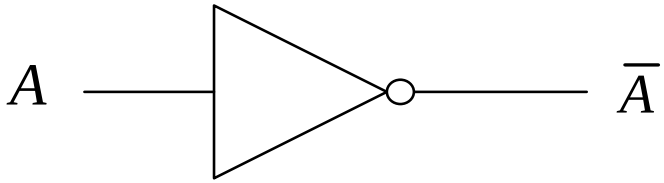
$$V_{DS}(sat) < V_M - V_T$$

- Ignoring the channel modulation $\lambda = 0$

$$k_n V_{DSn}(sat)\left(V_M - V_{Tn} - \frac{V_{DSn}(sat)}{2}\right)$$

$$+ k_p V_{DSp}(sat)\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSp}(sat)}{2}\right) = 0$$





- Switching Threshold

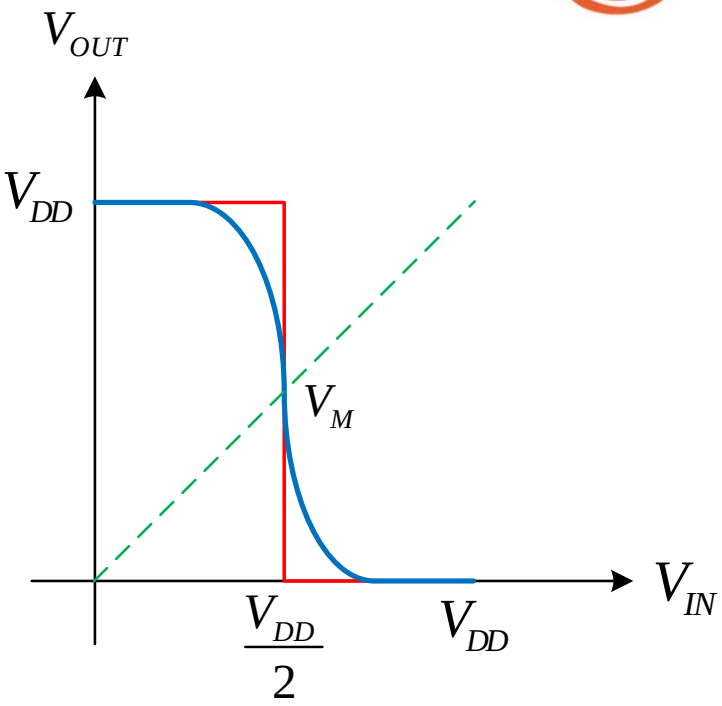
$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r}$$

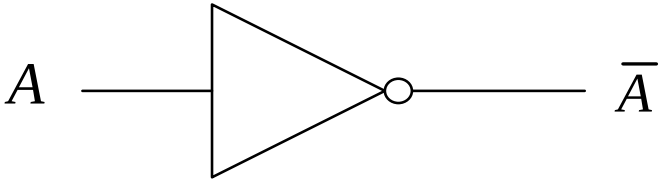
- Where r compares the relative strength of pMOS and nMOS

$$r = \frac{k_p V_{DSp}(sat)}{k_n V_{DSn}(sat)} = \frac{\upsilon_p(sat) W_p}{\upsilon_n(sat) W_n}$$

- For the $t_{ox}(pMOS) = t_{ox}(nMOS)$

$$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1+r}$$





- Switching Threshold

- For comparable high and low noise margin

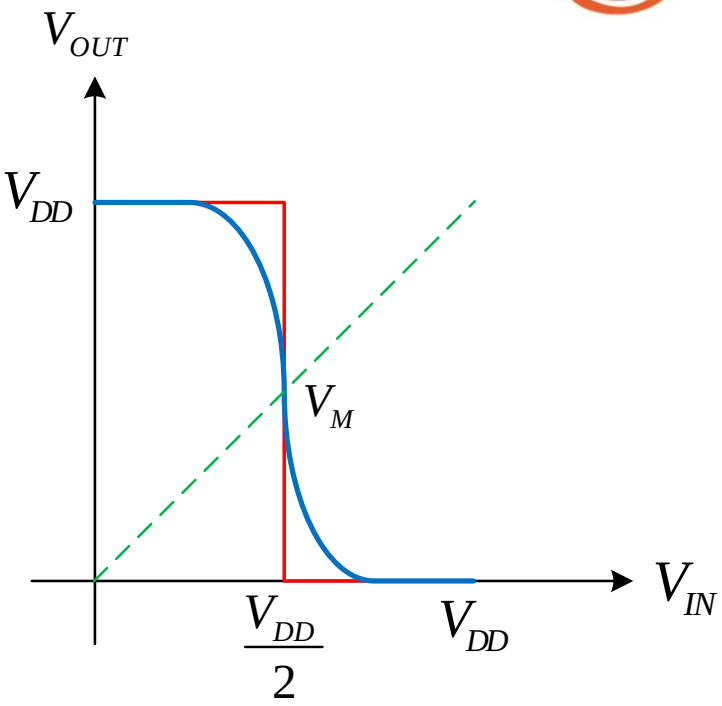
$$V_M \approx \frac{rV_{DD}}{1+r} = \frac{V_{DD}}{2}$$

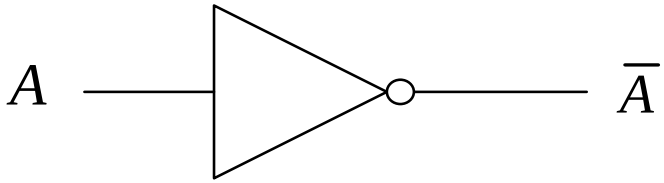
- Which requires $r = 1$

- Then the pMOS device should be seized to

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSn}(sat)}{k'_p V_{DSp}(sat)}$$

- Making W_p wider results in $r > 1$ and move V_M upper than the middle closer to V_{DD} and increasing the strength of nMOS move the switching voltage V_M closer to GND.





- Switching Threshold

- For desired value of the threshold voltage V_M , the pMOS to nMOS transistor sizes to set

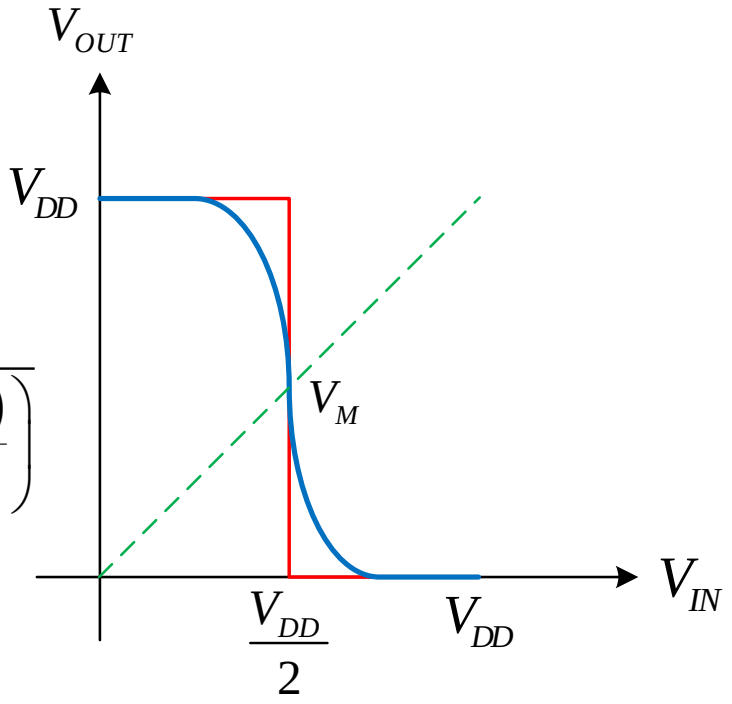
$$\frac{(W/L)_p}{(W/L)_n} = \frac{k'_n V_{DSn}(sat)\left(V_M - V_{Tn} - \frac{V_{DSn}(sat)}{2}\right)}{k'_p V_{DSp}(sat)\left(V_{DD} - V_M + V_{Tp} + \frac{V_{DSp}(sat)}{2}\right)}$$

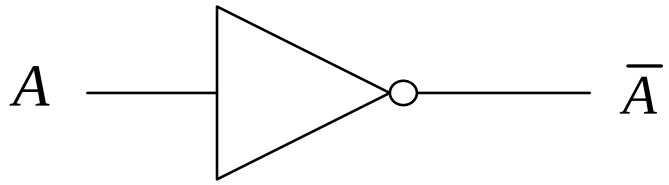
- For $V_{DS}(sat) > V_M - V_T$ where the saturation velocity is not occur, then

$$V_M = \frac{V_{Tn} + r(V_{DD} + V_{Tp})}{1 + r}$$

- Where

$$r = \sqrt{\frac{-k_p}{k_n}}$$





V_{DD}

- Noise Margin
- The input voltage high V_{IH} and out put voltage low is V_{IL} defined as

$$g = \frac{dV_{out}}{dV_{in}} = -1$$

- The piecewise linear approximation for VTC

$$V_{IH} - V_{IL} = -\frac{\left(V_{OH} - V_{OH}\right)}{g} = \frac{-V_{DD}}{g}$$

- Then the V_{IH} is

$$V_{IH} = V_M - \frac{V_M}{g}$$

- The V_{IL}

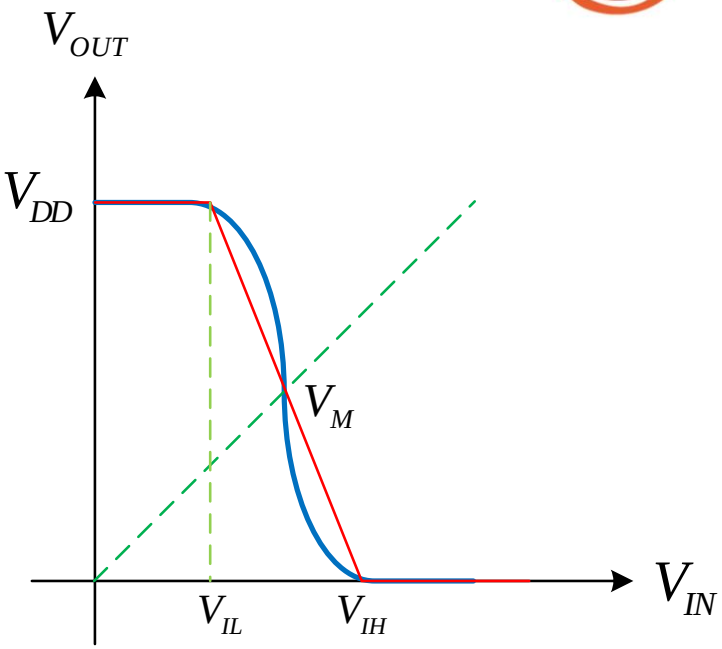
$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

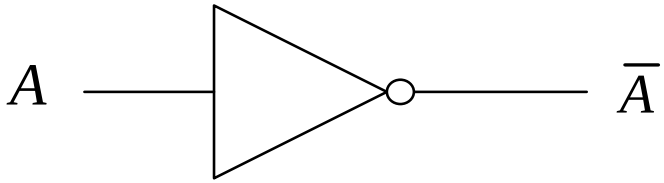
- and the high noise margin is

$$NM_H = V_{DD} - V_{IH}$$

- And the low noise margin is
- .

$$NM_L = V_{IL}$$





- Length Modulation
- Ignoring length modulation results in infinite gain
- Considering length modulation results in infinite gain

$$k_n V_{DSn}(sat)\left(V_{IN}-V_{Tn}-\frac{V_{DSn}(sat)}{2}\right)(1+\lambda V_{OUT})$$

$$+k_p V_{DSp}(sat)\left(V_{IN}-V_{DD}-V_{Tp}-\frac{V_{DSp}(sat)}{2}\right)(1+\lambda_p V_{OUT}-\lambda_p V_{DD})=0$$

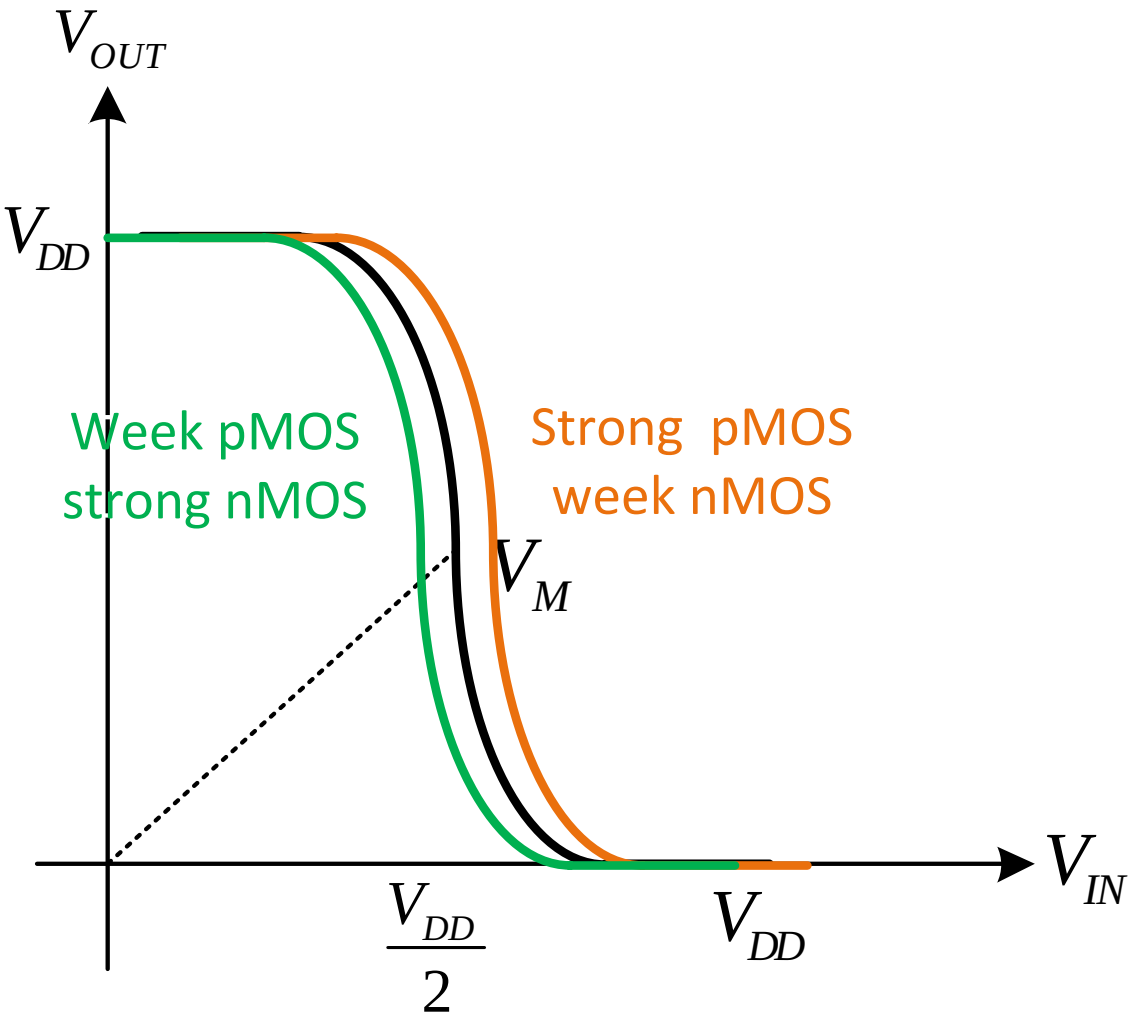
- Differentiating the output with respect to the input

$$\frac{dV_{out}}{dV_{in}}=\frac{k_n V_{DSn}(sat)(1+\lambda_n V_{OUT})+k_p V_{DSp}(sat)(1+\lambda_p V_{OUT}-\lambda_p V_{DD})}{\lambda_n k_n V_{DSn}(sat)\left(V_{IN}-V_{Tn}-\frac{V_{DSn}(sat)}{2}\right)+\lambda_p k_p V_{DSp}(sat)\left(V_{IN}-V_{DD}-V_{Tp}-\frac{V_{DSp}(sat)}{2}\right)}$$

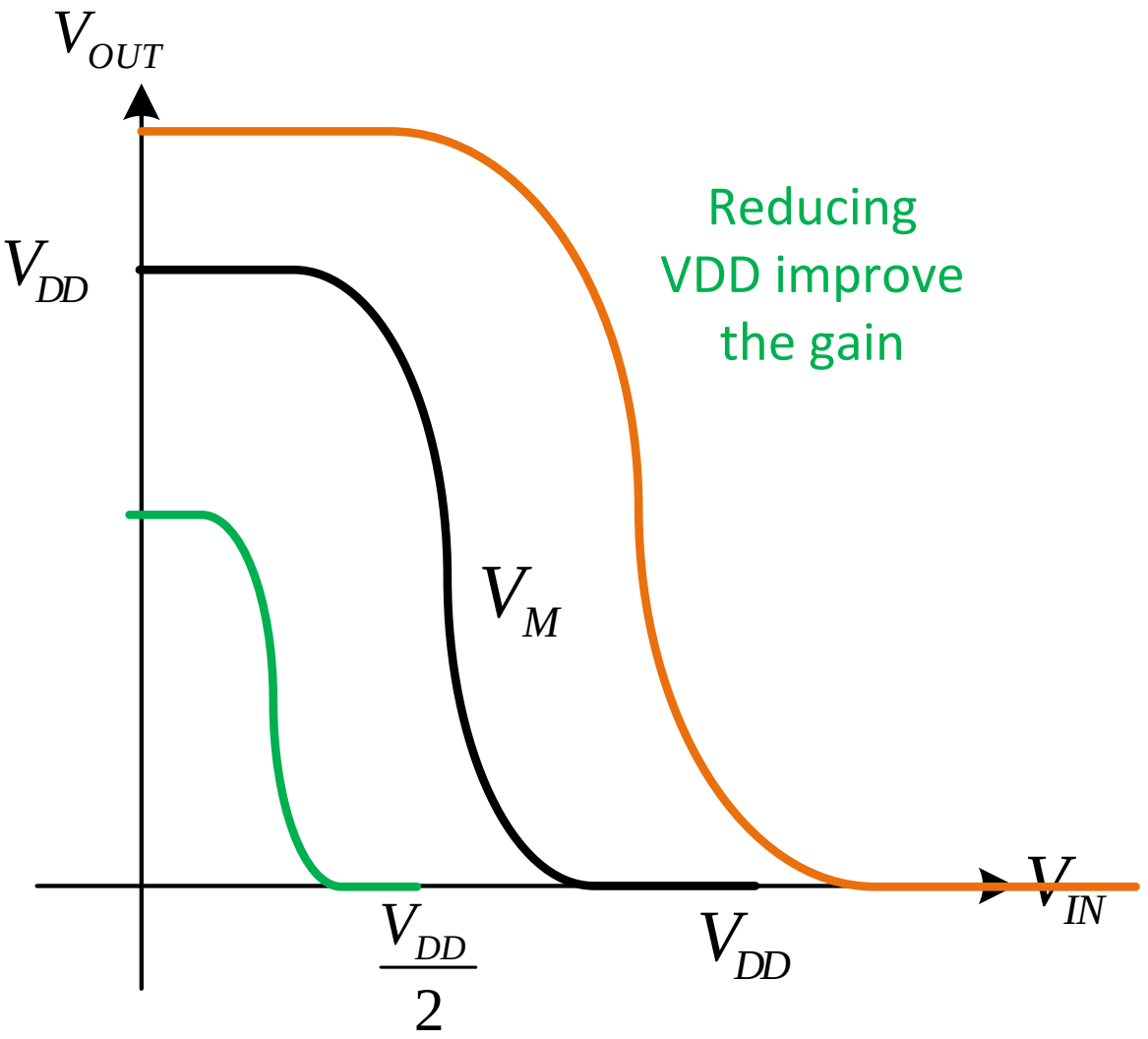
- Ignoring some second-order terms and setting $V_{IN}=V_M$ results in gain
- .

$$g=\frac{1}{I_{DS}(V_M)}\frac{k_n V_{DSn}(sat)+k_p V_{DSp}(sat)}{\lambda_n-\lambda_p}=\frac{1+r}{\left(V_M-V_{Tn}-\frac{V_{DSn}(sat)}{2}\right)(\lambda_n-\lambda_p)}$$

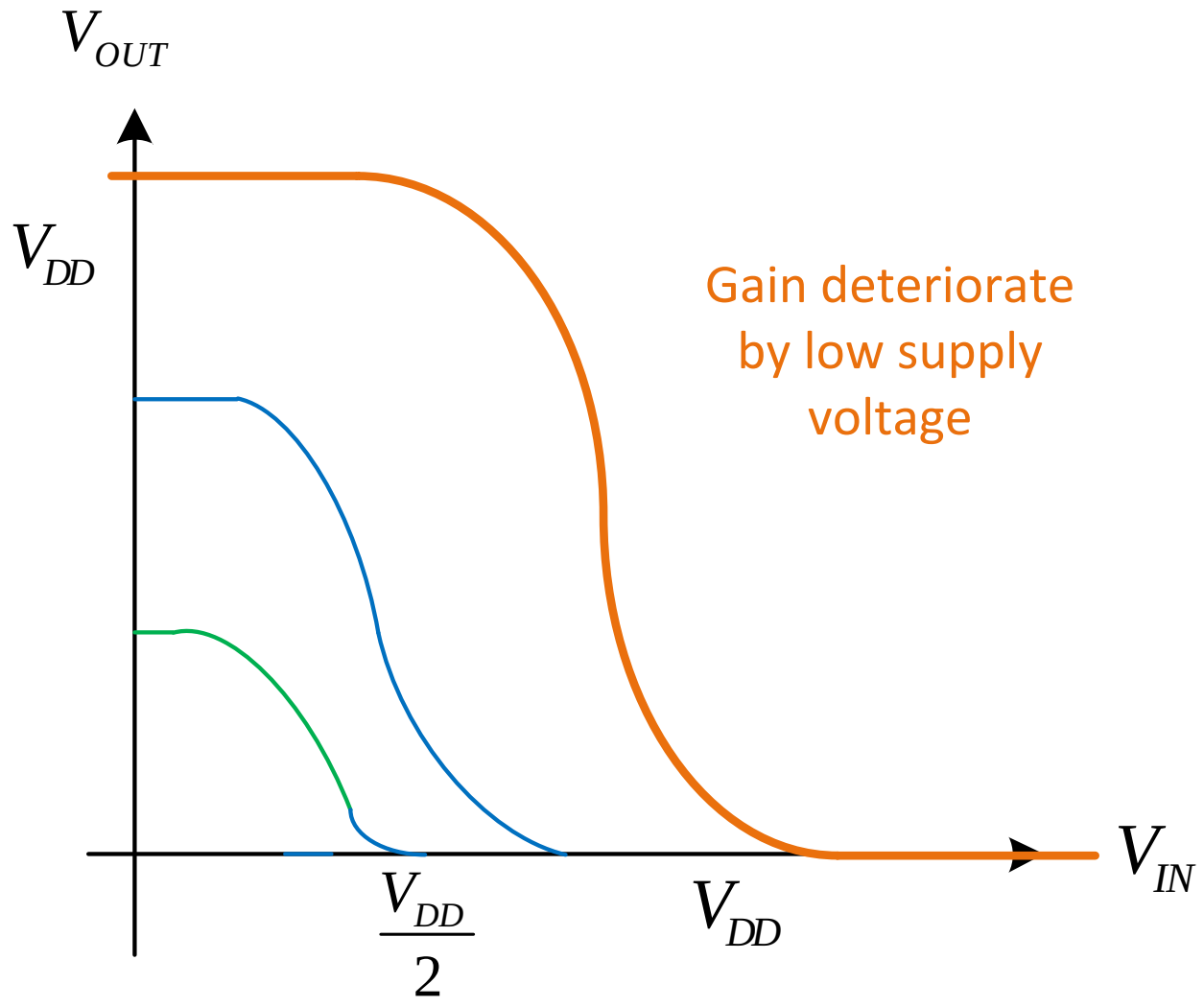
- Device variation



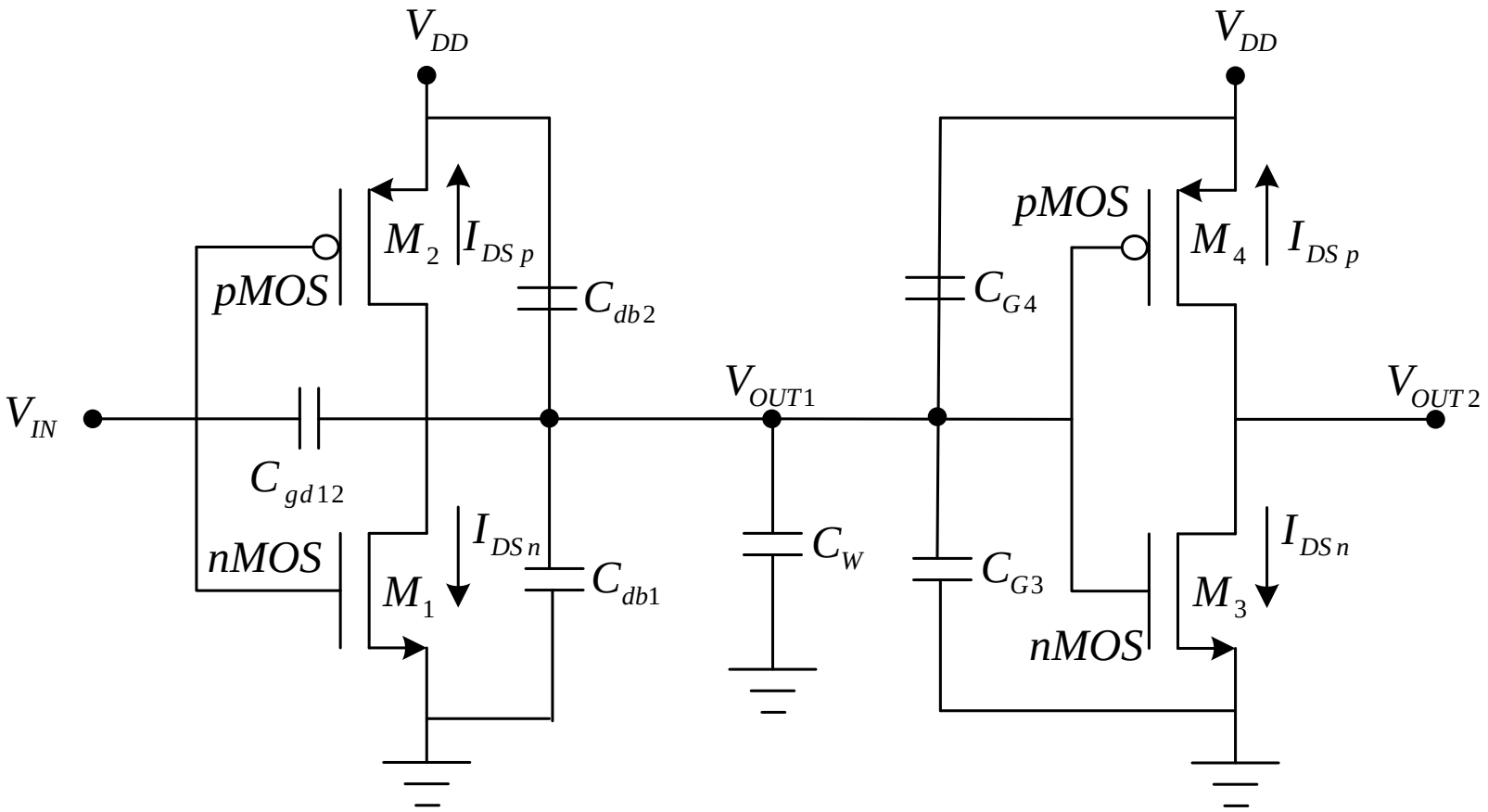
- Voltage supply scaling



- Device variation



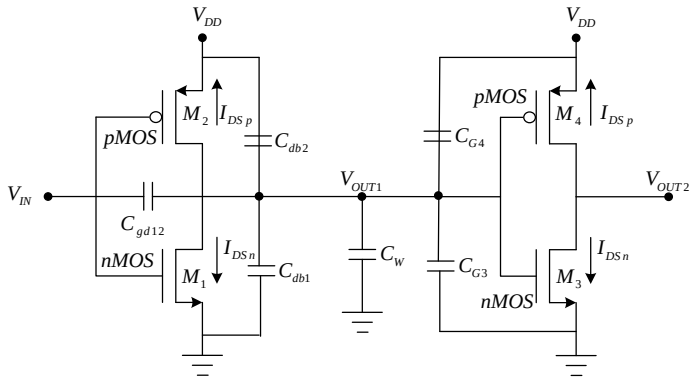
- Effect of Capacitance (lumped capacitor model)



- Gate-Drain Capacitance
- The capacitance between the gate and drain C_{gd12} of the first inverter is overlap capacitance of M1 and M2.
- M1 and M2 are either in cut-off or in saturation mode during the first half of output transient.
- The gate-drain capacitance C_{gd12} with respect to ground in lumped circuit model.

$$C_{gd12} = 2C_{GD0}W$$

- The factor of two is due to the Miller effect. The C_{GD0} is the overlapped capacitor
- .



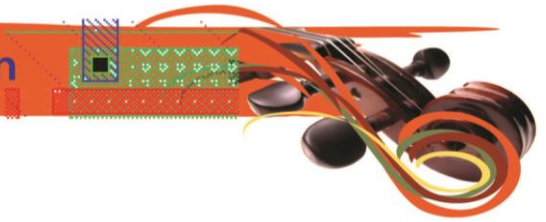
- Diffusion Capacitances

- The nonlinear voltage dependent diffusion capacitances C_{db1} and C_{db2} is due to the reversed bias pn-junction.
- The diffusion capacitor linearized over the voltage range of interest

$$C_{eq} = k_{eq} C_{jo}$$

- The C_{jo} is the junction capacitor per unit area under zero-bias condition.
- The bottom plate and sidewall zero bias value as can be obtained from the SPICE model CJ and CJSW.
- The k_{eq} is

$$k_{eq} = \frac{-V_0^m}{(V_{high} - V_{low})(1-m)} \left[(V_0 - V_{high})^{1-m} - (V_0 - V_{low})^{1-m} \right]$$



- Wire Capacitance
- The wire capacitance. C_W Depends on length and width of interconnecting wire

- Gate Capacitances
- The gate capacitances C_{g3} and C_{g4} includes both overlap and gate capacitance of each transistor.

$$C_{fan-out} = C_{gate}(nMOS) + C_{gate}(pMOS)$$
$$= (C_{GSOn} + C_{GDOn} + W_n L_n C_{OX}) + (C_{GSOp} + C_{GDOp} + W_p L_p C_{OX})$$