EE141-Spring 2010 Digital Integrated Circuits

Lecture 16
Ratioed Logic
Dynamic Logic

Administrativia

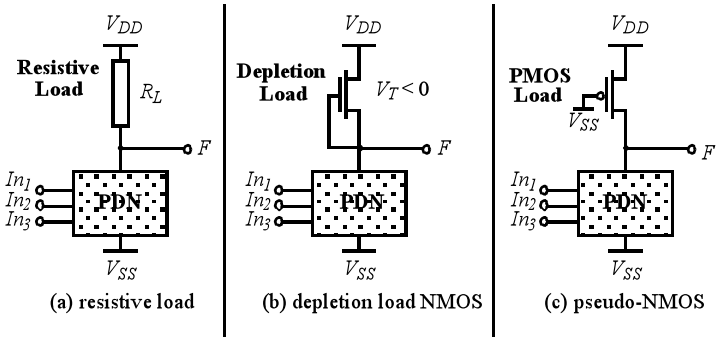
- Project Phase 1 Done – Thanks for the timely response.
- Phase 2 to be announced We – Launched on Fr.
- Hw 6 due on Fr.

Class Material

- Last lecture
  - Pass transistor logic
  - CMOS Layout
- Today's lecture
  - Ratioed Logic
  - Dynamic Logic
- Reading (Ch 6)

Ratioed Logic

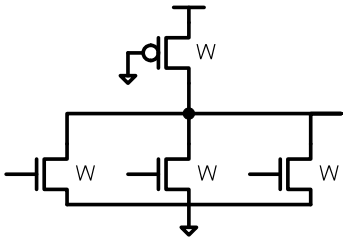
Ratioed Logic

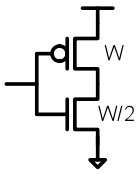


Goal: build gates faster/smaller than static complementary CMOS

Ratioed Logic LE

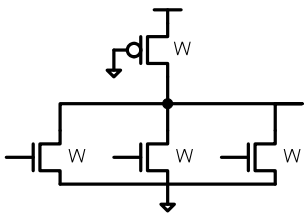
- Rising and falling delays aren't the same
  - Calculate LE for the two edges separately

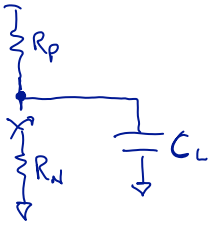




- For tpLH:
  - $C_{gate} = WC_G$ $C_{inv} = (3/2)WC_G$ $LE_{LH} =$

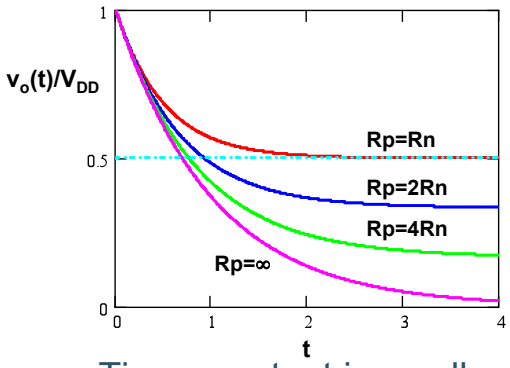
Ratioed Logic LE (pull-down edge)

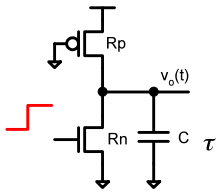




- What is LE for t_{pHL}?
- Switch model would predict $R_{eff} = R_n||R_p$
  - Would that give the right answer for LE?

Response on Falling Edge





$$\tau = \frac{Rn \cdot Rp}{Rn + Rp} \cdot C$$

$$\frac{v_o(t)}{V_{DD}} = \frac{Rn}{Rn + Rp} + \left(1 - \frac{Rn}{Rn + Rp}\right) e^{-t/\tau}$$

- Time constant is smaller, but it takes more time to complete 50% V_{DD} transient (arguably)
  - Rp actually takes some current away from discharging C

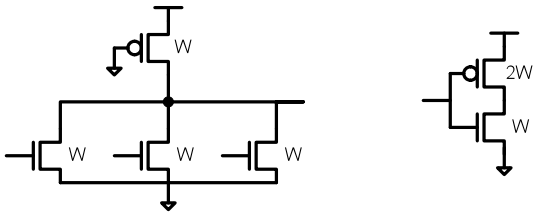
Ratioed Logic Pull-down Delay

- Think in terms of the current driving C_{load}
- When you have a conflict between currents
  - Available current is the difference between the two
  - In pseudo-nMOS case:

$$R_{drive} = \frac{1}{1/Rn - 1/Rp} \longrightarrow R_{drive} = \frac{Rn}{1 - (Rn/Rp)}$$

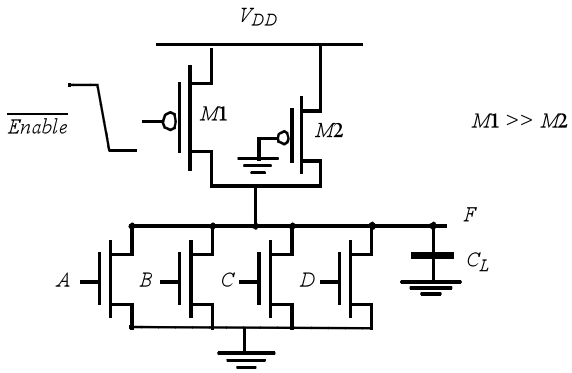
  - (Works because Rp >> Rn for good noise margin)

Ratioed Logic LE (pull-down edge)



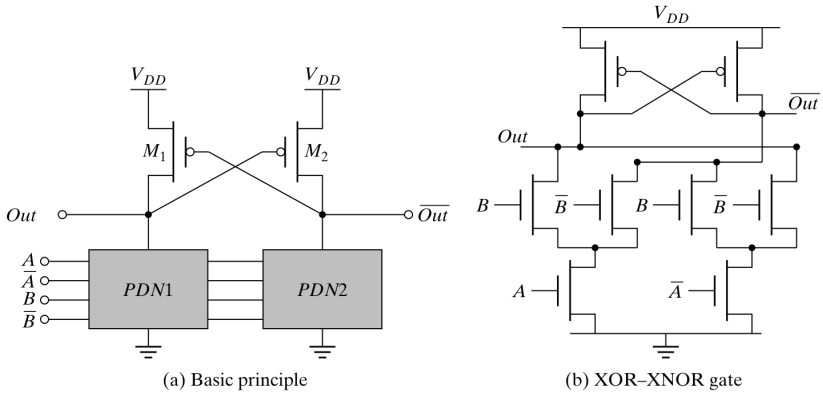
- For t_{pHL} (assuming $R_{sqp} = 2R_{sqn}$):
  - $R_{gate} = R_n/(1\text{-}Rn/Rp) = 2Rn$ $\quad R_{inv} = R_n$
  - $C_{gate} = WC_G$ $\quad C_{inv} = 3WC_G$
  - LE_{HL} =
- LE is lower than an inverter!
  - But have static power dissipation…

Improved Loads



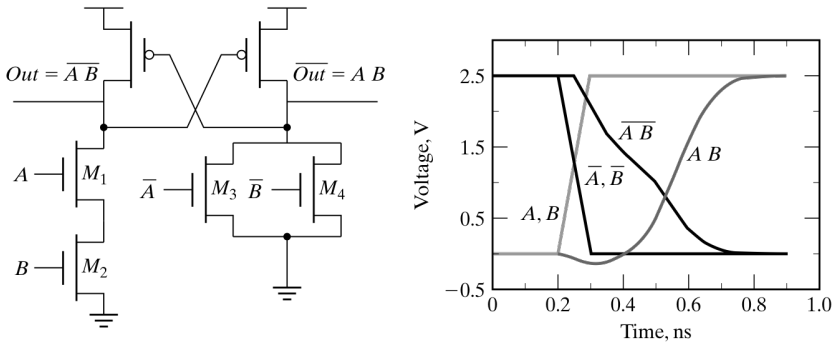
Adaptive Load

Improved Loads (2)



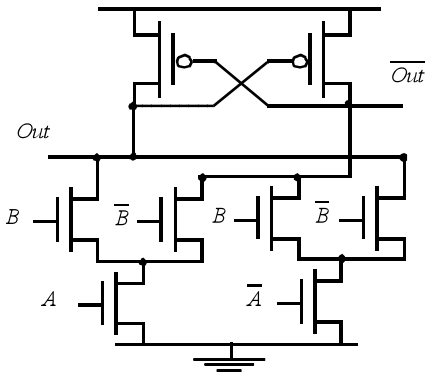
Differential Cascode Voltage Switch Logic (DCVSL)

DCVSL Transient Response



DCVSL Example1: AND

DCVSL Example2



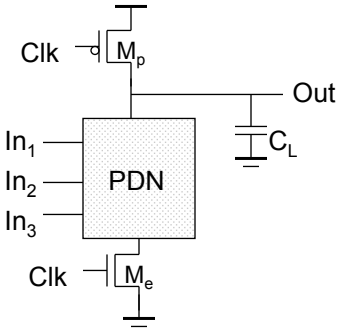
XOR/XNOR gate

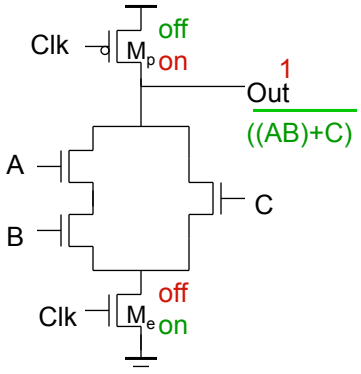
Dynamic Logic

Dynamic CMOS

- In static circuits, at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - only requires *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate





Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

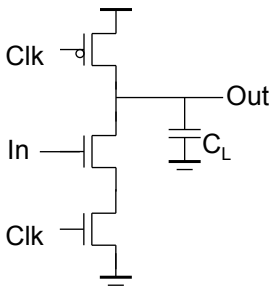
Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

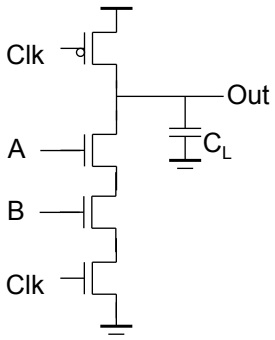
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced capacitance due to lower input capacitance (C_{in})
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

LE of Dynamic Gates



C_{gate} =
LE =

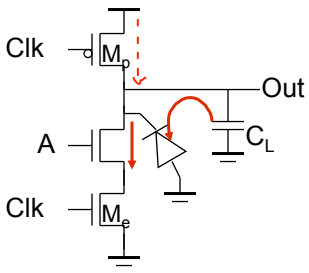


C_{gate} =
LE =

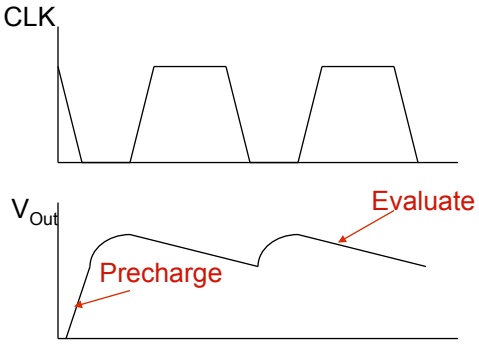
Properties of Dynamic Gates

- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
- Needs a precharge/evaluate clock

Issues in Dynamic Design 1: Charge Leakage

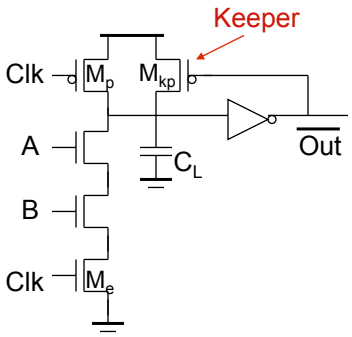


Leakage sources



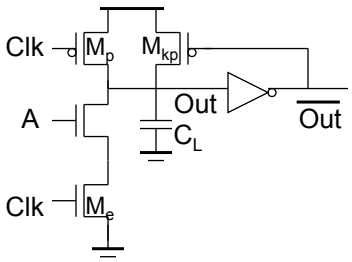
Dominant component is subthreshold current

Solution to Charge Leakage



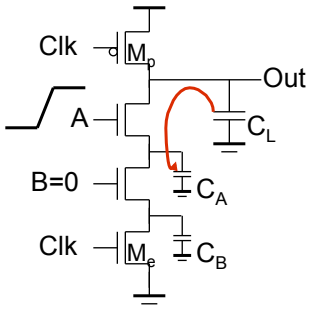
Same approach as level restorer for pass-transistor logic

Dynamic Gate VTC



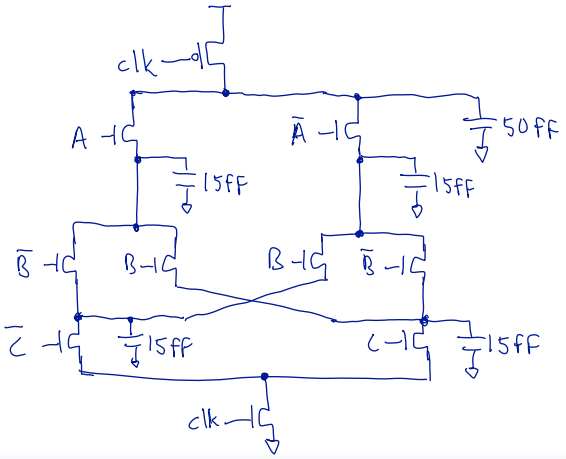
Issues in Dynamic Design 2: Charge Sharing

- Charge initially stored on C_L
  - C_A previously discharged

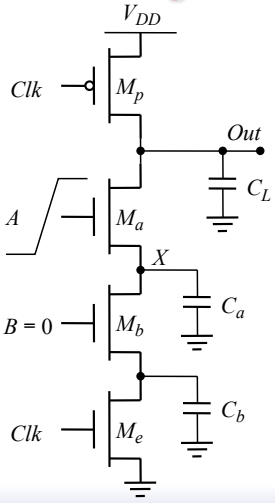


- When A rises, this charge is redistributed (shared) between C_L and C_A
- Makes Out drop below V_{DD}

Charge Sharing Example



Charge Sharing



- Two cases:
  - M_a stays on – complete charge share
  - M_a turns off – incomplete charge share

•Complete charge share:

- $Q_{Ca} = V_{Out}C_a$
  $\Delta Q_{CL} = -V_{Out}C_a$

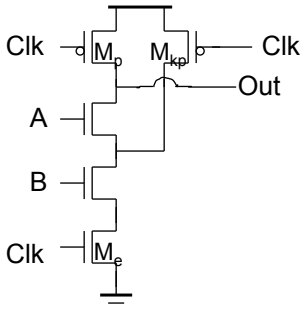
→ $\boxed{\Delta V_{Out} = -V_{DD}C_a/(C_a+C_L)}$

•Incomplete charge share:

- $Q_{Ca} = (V_{DD}-V_{TN}^*)C_a$
  $\Delta Q_{CL} = -(V_{DD}-V_{TN}^*)C_a$

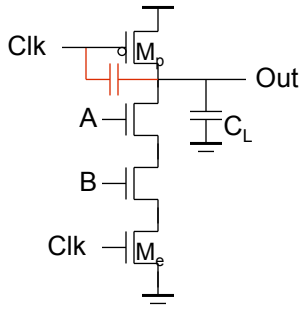
→ $\boxed{\Delta V_{Out} = -(V_{DD}-V_{TN}^*)C_a/C_L}$

Solution to Charge Sharing



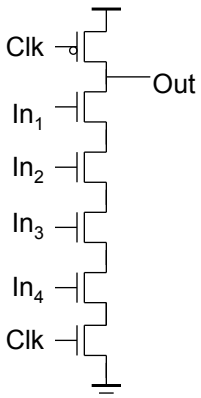
- Keeper helps a lot
  - Can still get failures if Out drops below inverter V_{sw}
- Another option: precharge internal nodes
  - Increases power and area

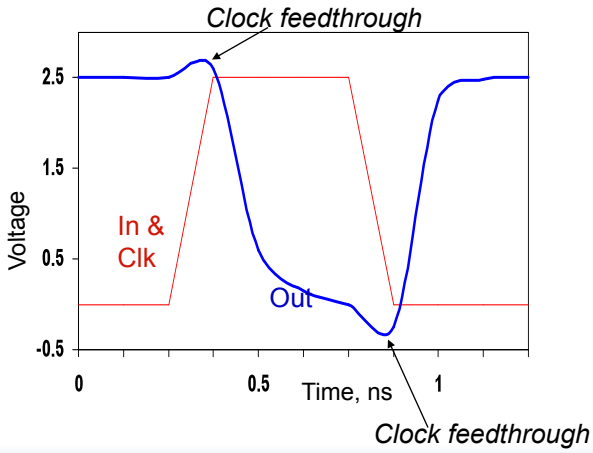
Issues in Dynamic Design 3: Clock Feedthrough



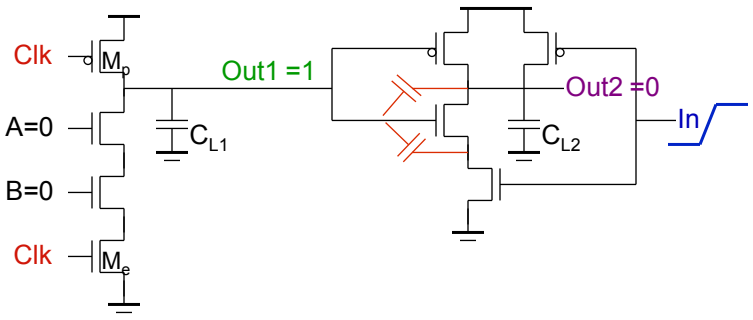
Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

Clock Feedthrough



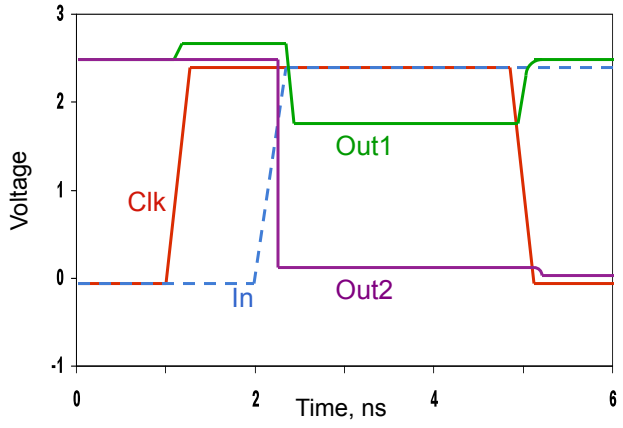


Issues in Dynamic Design 4: Backgate Coupling



Dynamic NAND Static NAND

Backgate Coupling Effect

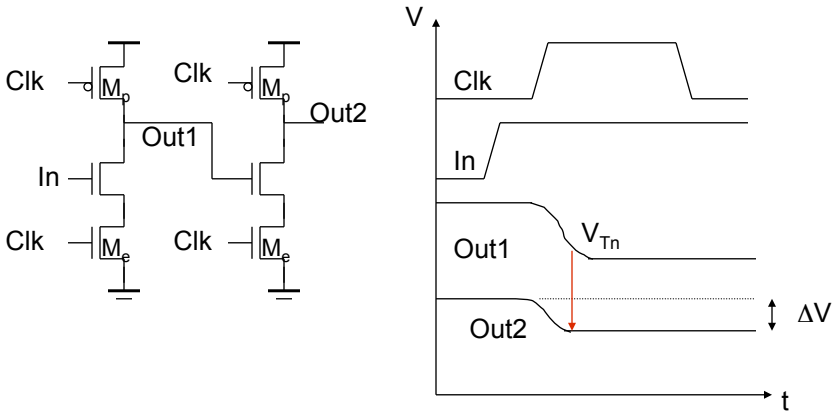


Other Effects

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)

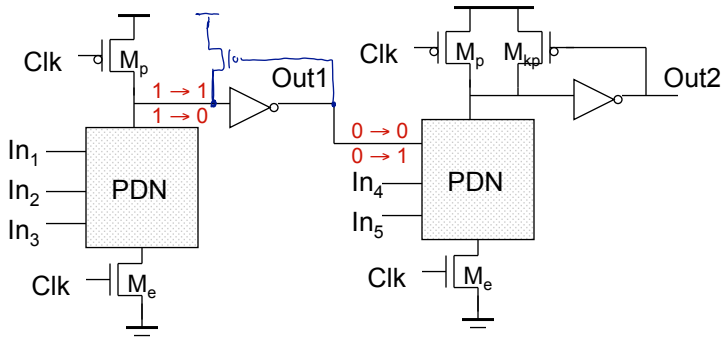
Domino Logic

Cascading Dynamic Gates

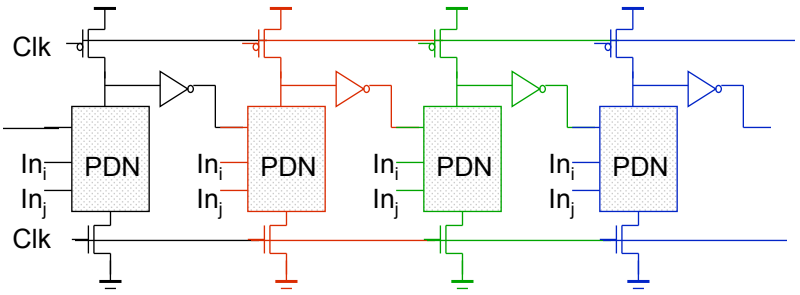


Only 0 → 1 transitions allowed at inputs!

Domino Logic



Why Named Domino?

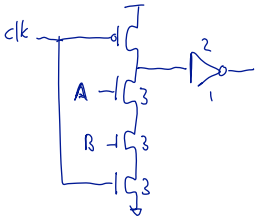


Like falling dominos!

Properties of Domino Logic

- Only non-inverting logic can be implemented
- Very high speed
  - static inverter can be skewed, only L-H transition critical
  - Input capacitance reduced – smaller logical effort

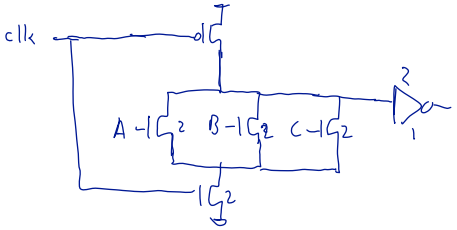
Domino Logic LE



$LE_{dyn} =$

$LE_{inv} = 1$

$\pi LE =$



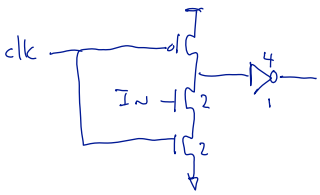
$LE_{dyn} =$

$LE_{inv} = 1$

$\pi LE =$

$LE_{static} = \frac{7}{3}$

Domino Logic LE (skewed static gate)

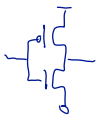


$LE_{dyn} =$

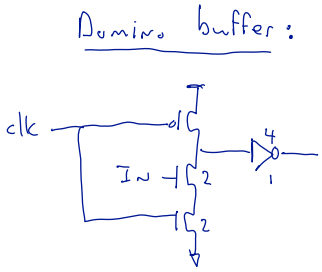
$LE_{inv} =$

$\pi LE =$

reference inverter:



Buffer "Average" LE



$LE_{dinv} = \frac{2}{3}$

$LE_{sinv} = \frac{5}{6}$

$\Pi LE = \frac{10}{18}$

"Average" $LE = \sqrt{10/18} \approx \frac{3}{4}$

Designing with Domino Logic