Elmore

Lecture 17

- Elmore Delay Approximation
- Rational:
- Delay Calculation.
- Static Timing Analysis.
- Logic Synthesis

- Output response:
- Network structure & state
  - Natural response (zero-input response)- (Homogenous,-Math-)
- Input waveform & zero states
  - Forced response (zero-state response) (Particular,-Math-)
- Linear circuits :

$$v_{Total}(t) = v_{Natural}(t) + v_{Forced}(t)$$

- Basic Waveforms
- Impulse input

$$\delta(t) = \begin{cases} 0 & t = 0 \\ 1 & otherwise \end{cases}$$

- Step input

$$u(t) = \begin{cases} 0 & t < 0 \\ 1 & t \geq 0 \end{cases}$$

- Pulse input

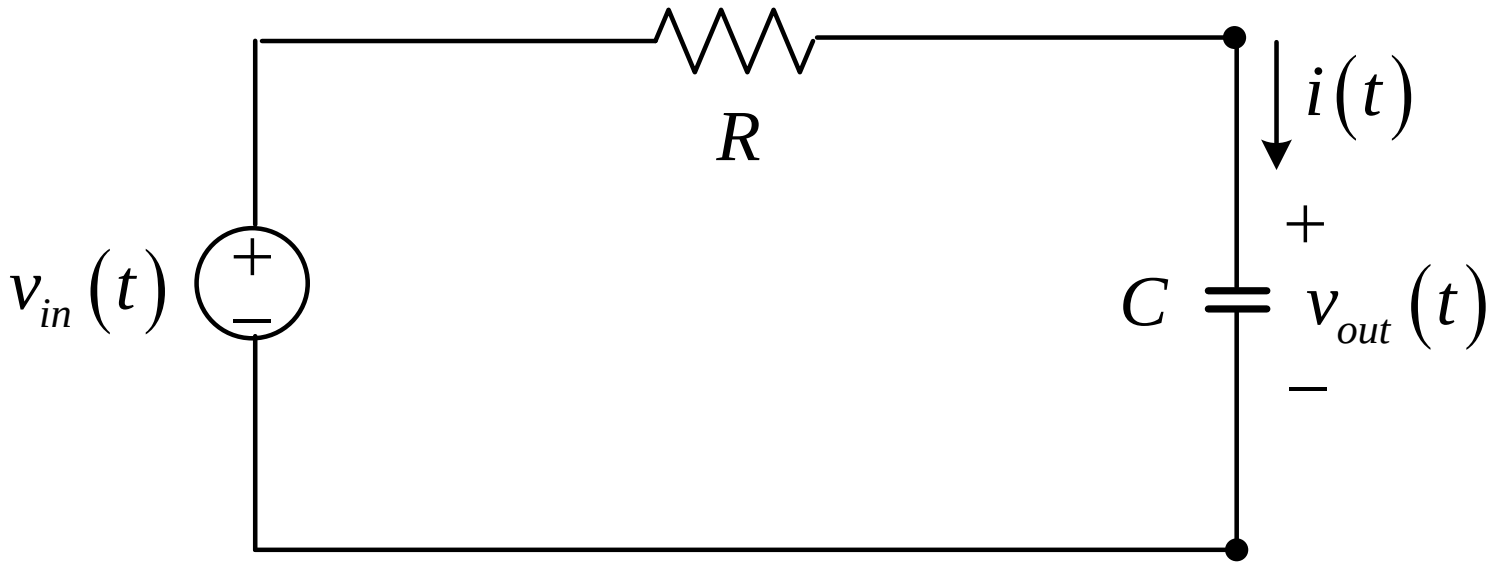
$$P_T(t) = \frac{1}{T}\left[u\left(t + \frac{T}{2}\right) - u\left(t - \frac{T}{2}\right)\right]$$

- Sinusoidal input

$$x(t) = A\sin\left(\omega t + \theta\right)$$

- Apply simple input waveforms to insight of the network design.

- Analysis of Simple RC Circuit

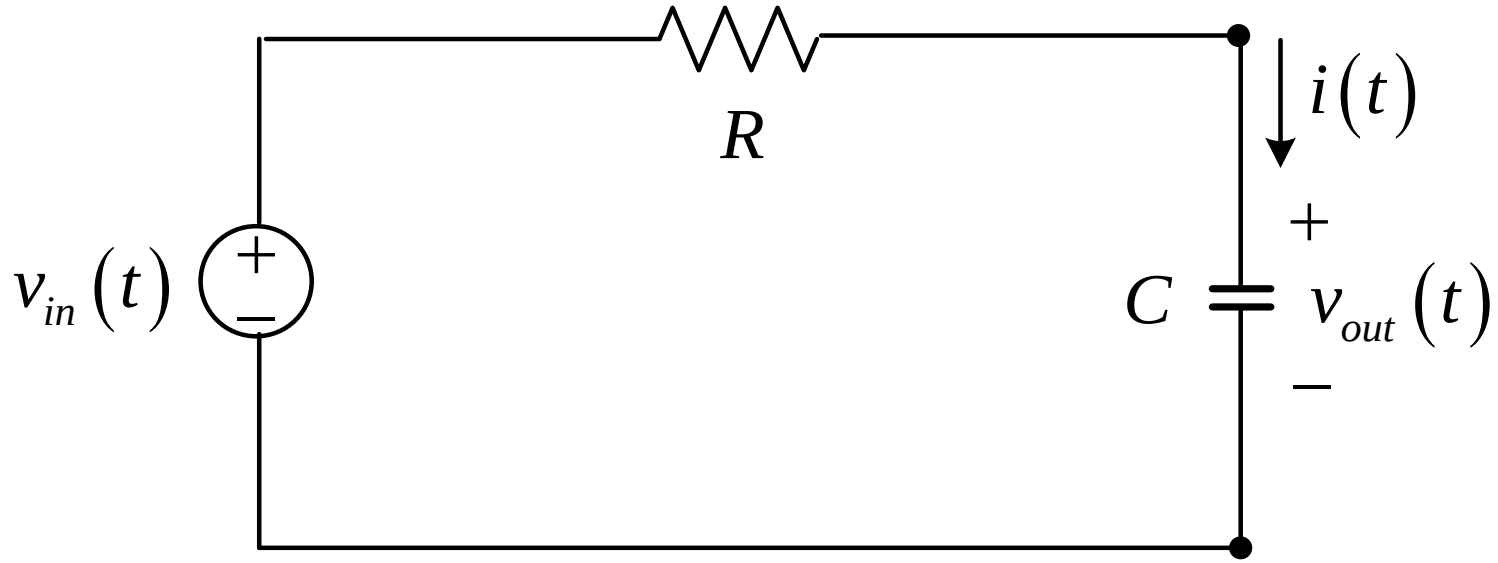


- Loop equation:

$$Ri(t) + v(t) = v_{in}(t)$$

$$i(t) = \frac{d(Cv(t))}{dt} = C\frac{dv(t)}{dt}$$

- Analysis of Simple RC Circuit



$$RC\frac{dv(t)}{dt}+v(t)=v_{in}(t)$$

- First order linear differential equation with constant coefficient

$v_{in}(t)=$ Input Signal $\qquad$ $v(t)=$ State Variable

- Analysis of Simple RC Circuit:
- Zero input response:
- $$RC\frac{dv(t)}{dt}+v(t)=0$$
- Natural response.

$$\frac{1}{v(t)}\frac{dv(t)}{dt}=-\frac{1}{RC} \qquad v_{Natural}(t)=Ce^{-t/RC}$$

- Step input response:

$$RC\frac{dv(t)}{dt}+v(t)=v_0u(t) \quad v_{Forced}(t)=v_0u(t) \quad \Rightarrow \quad v(t)=Ce^{-t/RC}+v_0u(t)$$

- Match initial state:

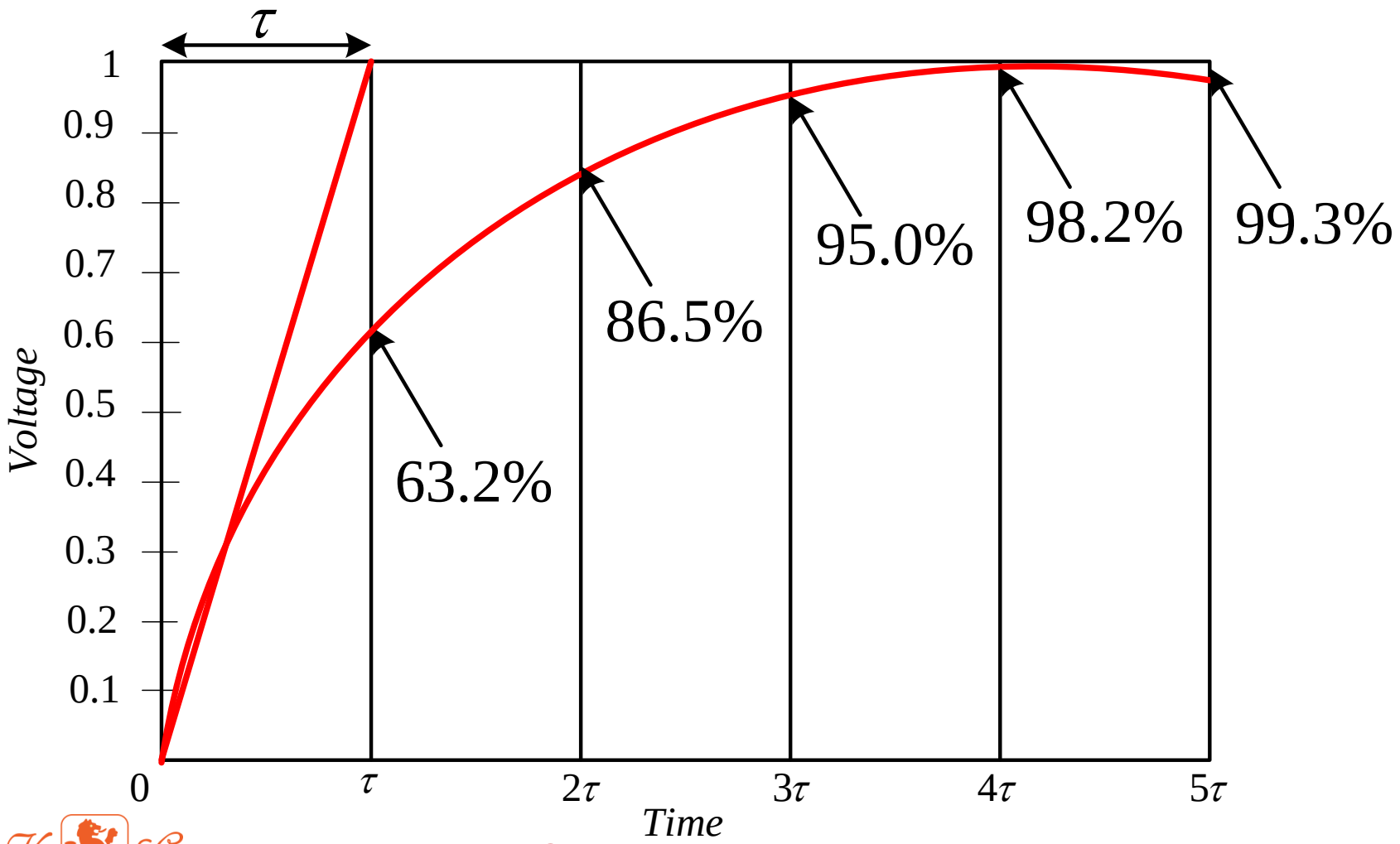
$$v(t)=0 \quad \Rightarrow \quad C+v_0u(t)=0$$

- Output response for step input:

$$v(t)=v_0(1-e^{-t/RC})u(t)$$

$$v(t)=0.9v_0 \Rightarrow t=2.3RC \qquad v(t)=0.5v_0 \Rightarrow t=0.69RC$$

- The resulting voltage $v_{out}(t)$ across the capacitor over time is shown for the normalized voltage of $1V$.



- The Elmore delay:

$$\tau_D = RC$$

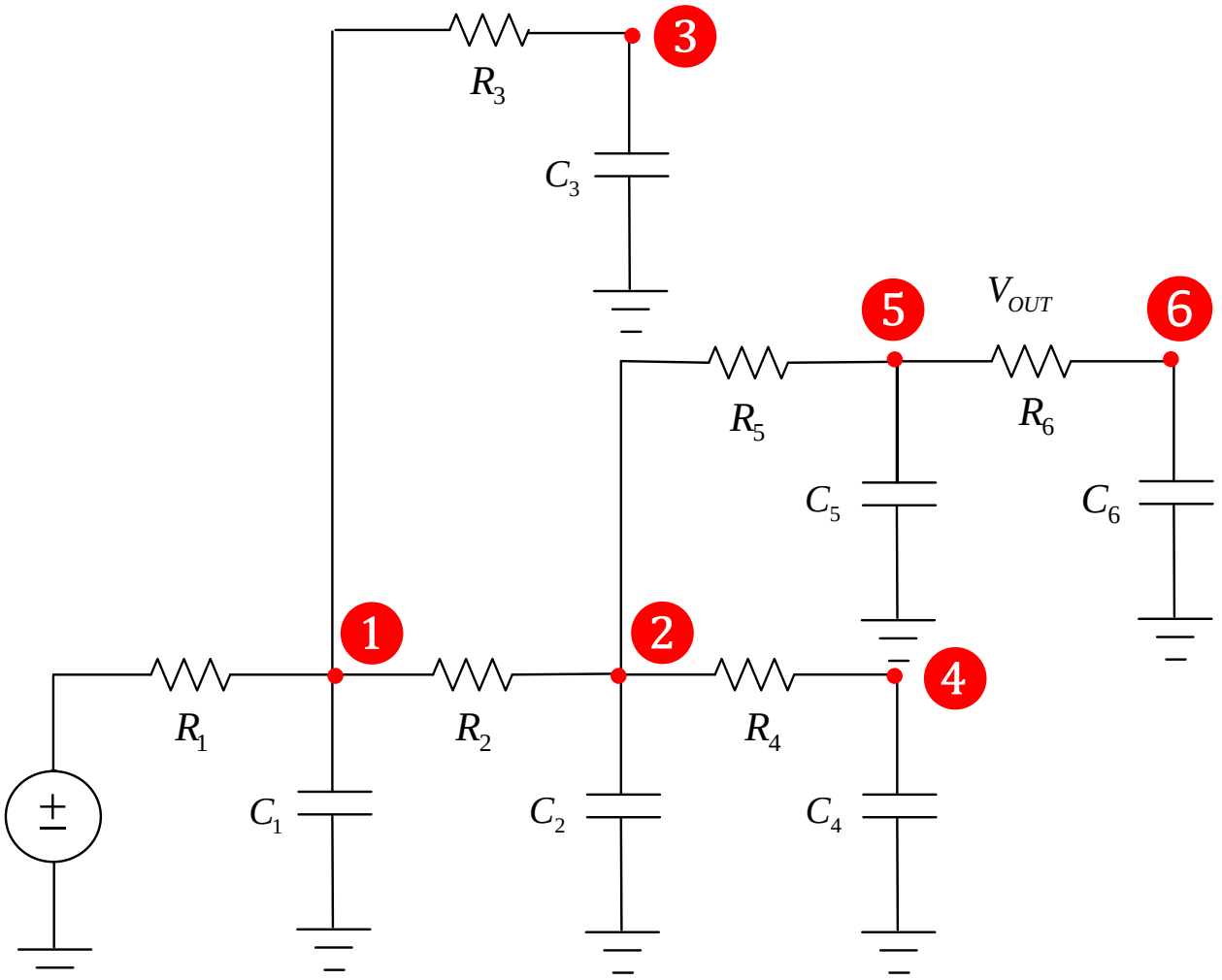
- Sink Delay :

$$\tau_d = RC$$

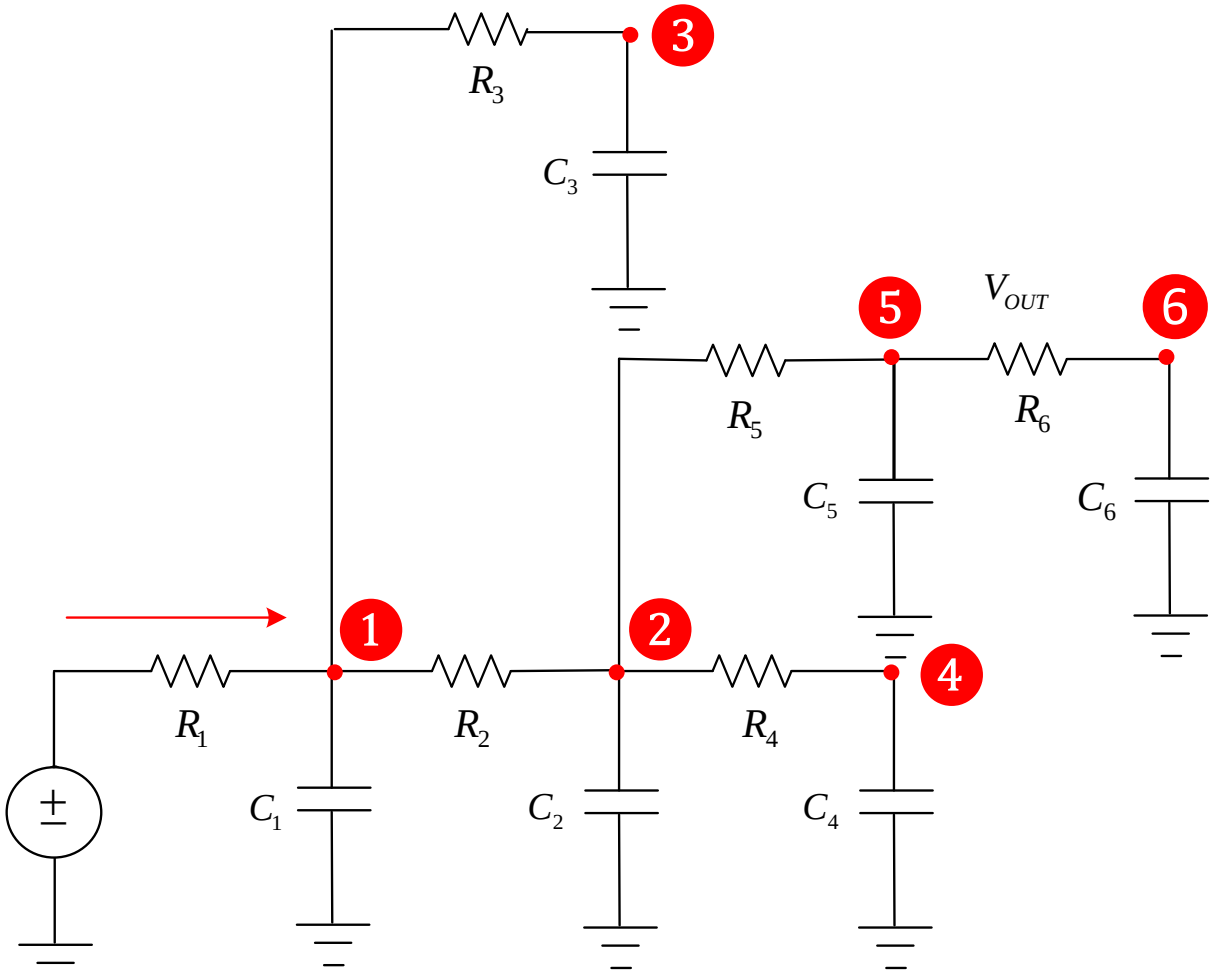
- Driver resistance: R
- Total interconnected capacitance+ loading capacitance: C
- 50% delay under step input :

$$\tau = 0.69RC$$

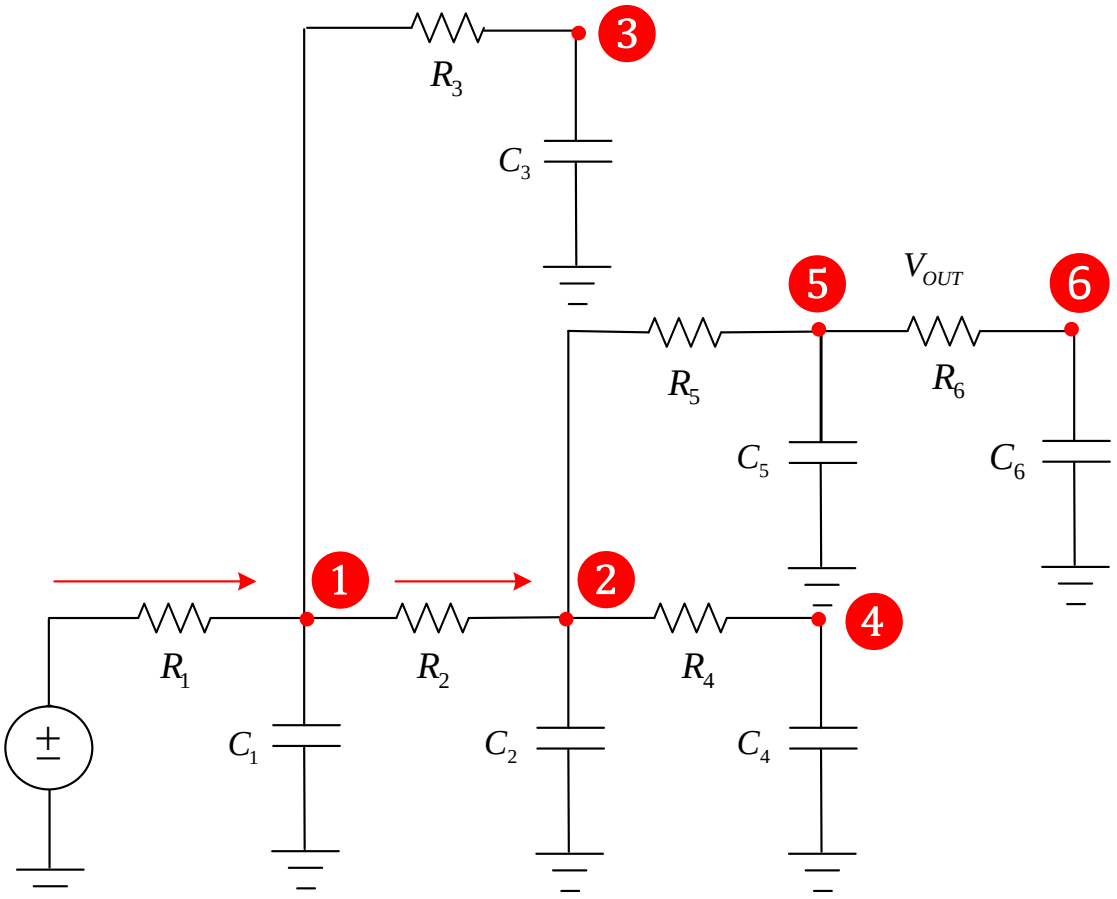
- Find the Time constant at all nodes.



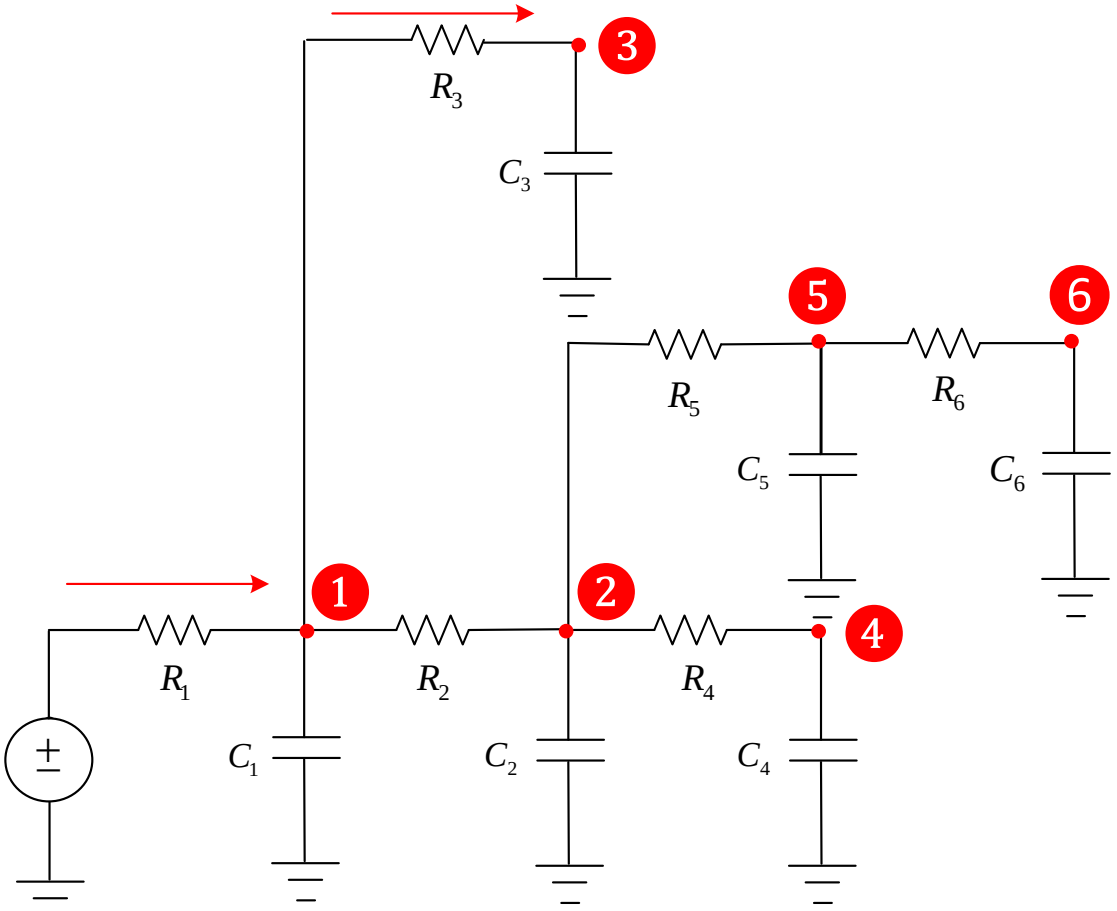
- 1 $\tau_{V_{in}-V_{out1}} = R_1\left(C_1 + C_2 + C_3 + C_4 + C_5 + C_6\right)$



- 2 $\tau_{V_{in}-V_{out\,2}} = R_1\left(C_1+C_2+C_3+C_4+C_5+C_6\right)$
$+R_2\left(C_2+C_4+C_5+C_6\right)$

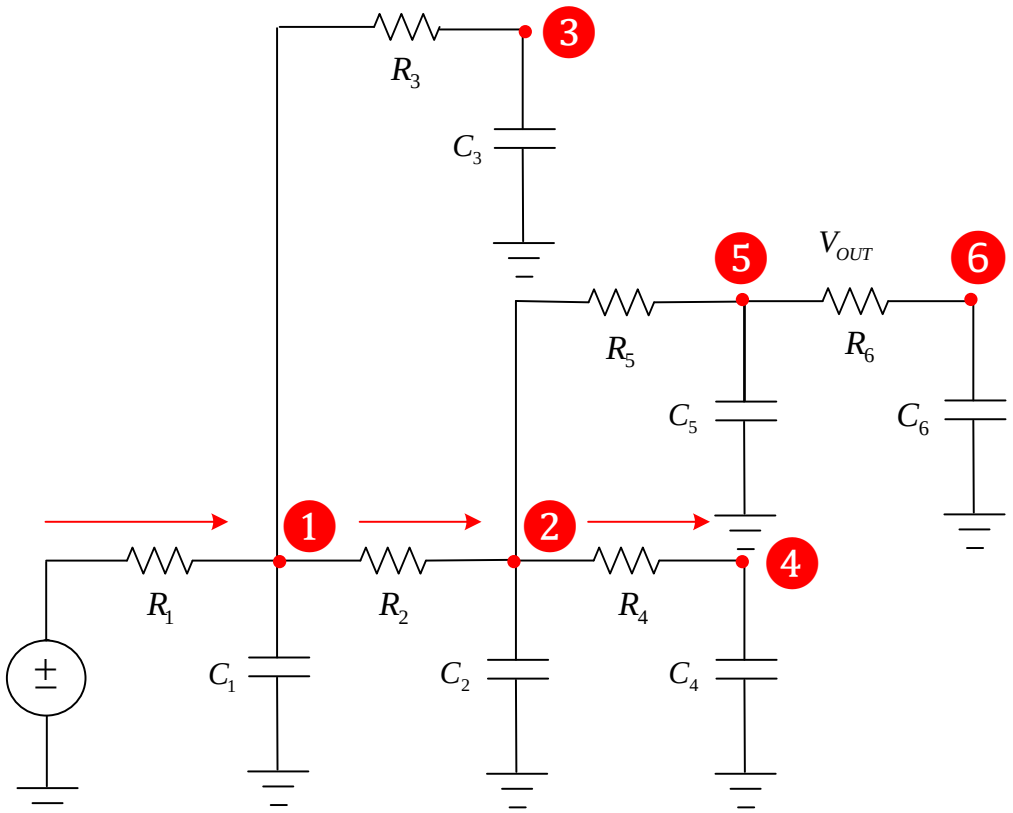


- 3 $\tau_{V_{in}-V_{out\,3}} = R_1\left(C_1+C_2+C_3+C_4+C_5+C_6\right) + R_3C_3$

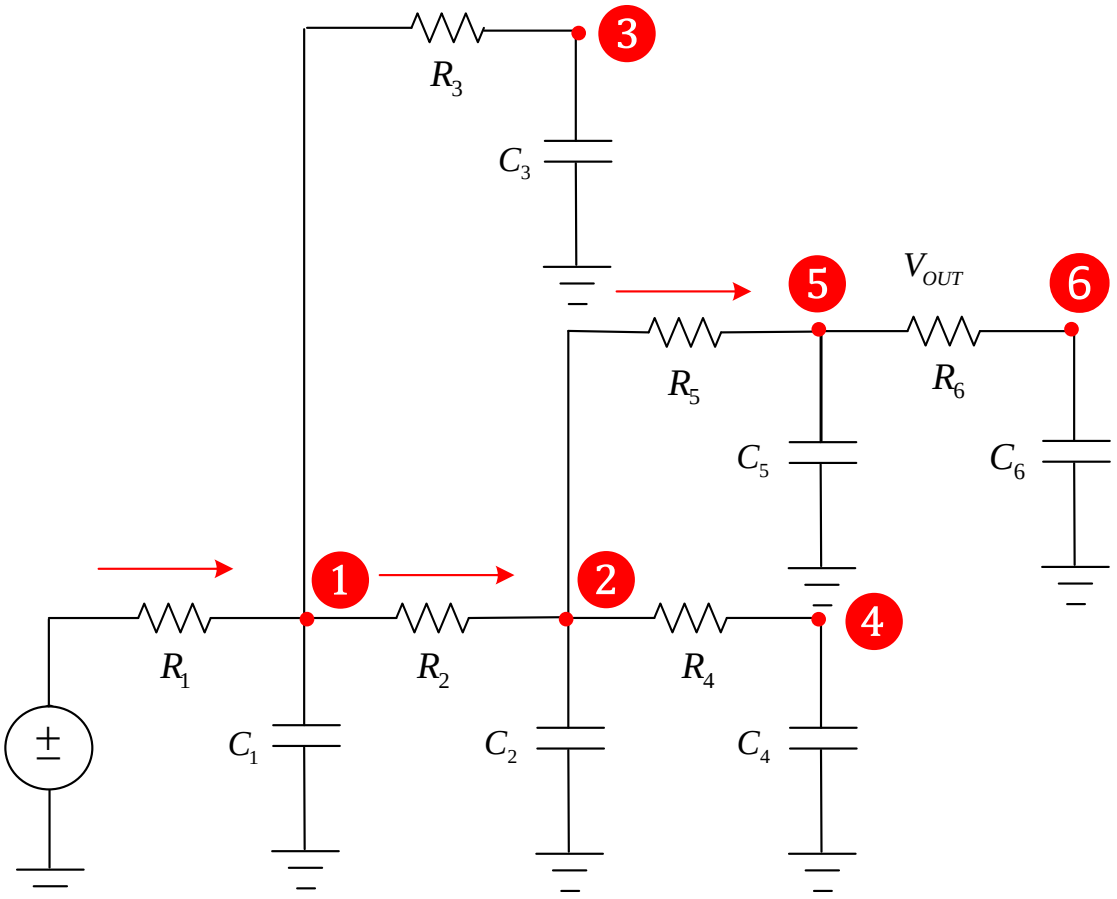


- 4

$$\tau_{V_{in}-V_{out\,4}} = R_1\left(C_1+C_2+C_3+C_4+C_5+C_6\right) + R_2\left(C_2+C_4+C_5+C_6\right)+R_4C_4$$

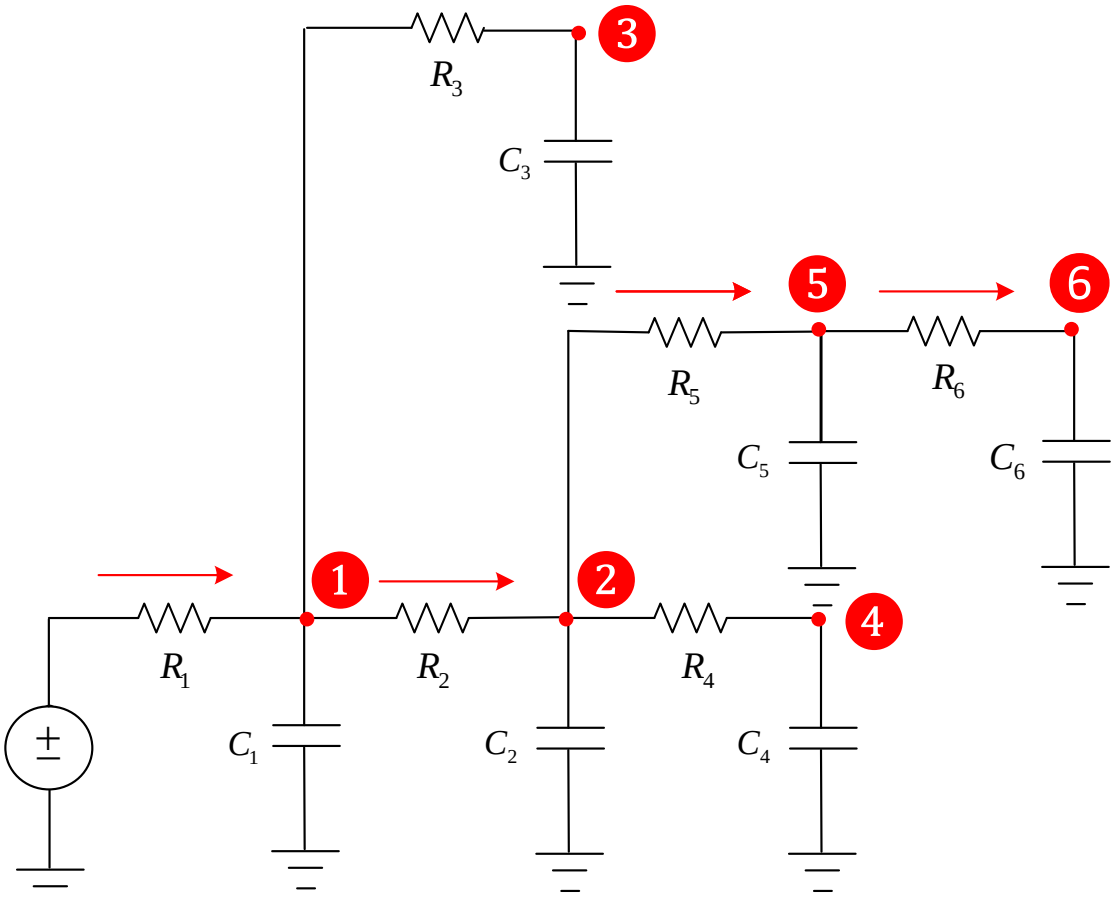


- 5 $\tau_{V_{in}-V_{out5}} = R_1\left(C_1+C_2+C_3+C_4+C_5+C_6\right)$
$+R_2\left(C_2+C_4+C_5+C_6\right)+R_5C_5$

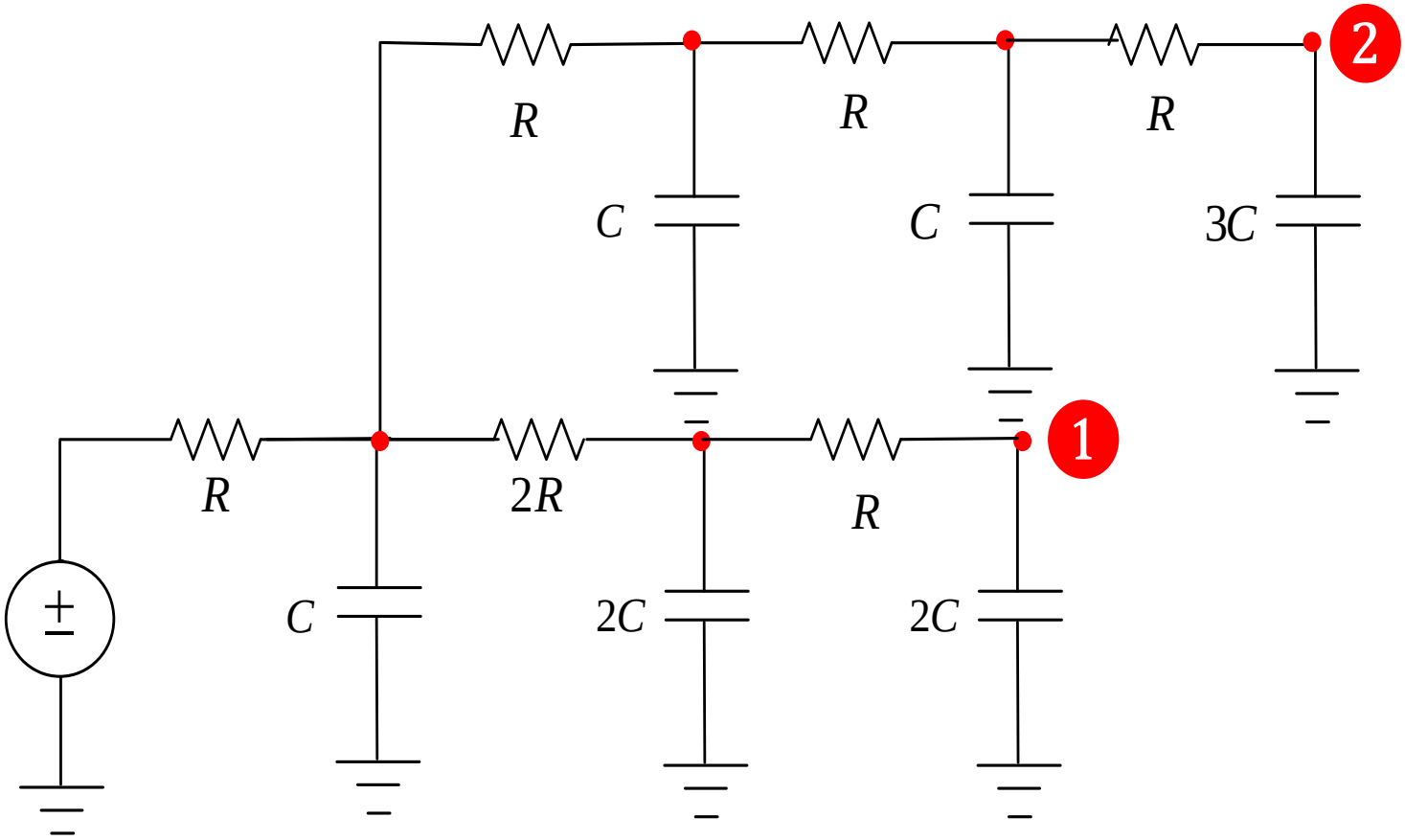


- 6 $\tau_{V_{in}-V_{out\,6}} = R_1\left(C_1+C_2+C_3+C_4+C_5+C_6\right)$

$$+R_2\left(C_2+C_4+C_5+C_6\right)+R_5\left(C_5+C_6\right)+R_6C_6$$

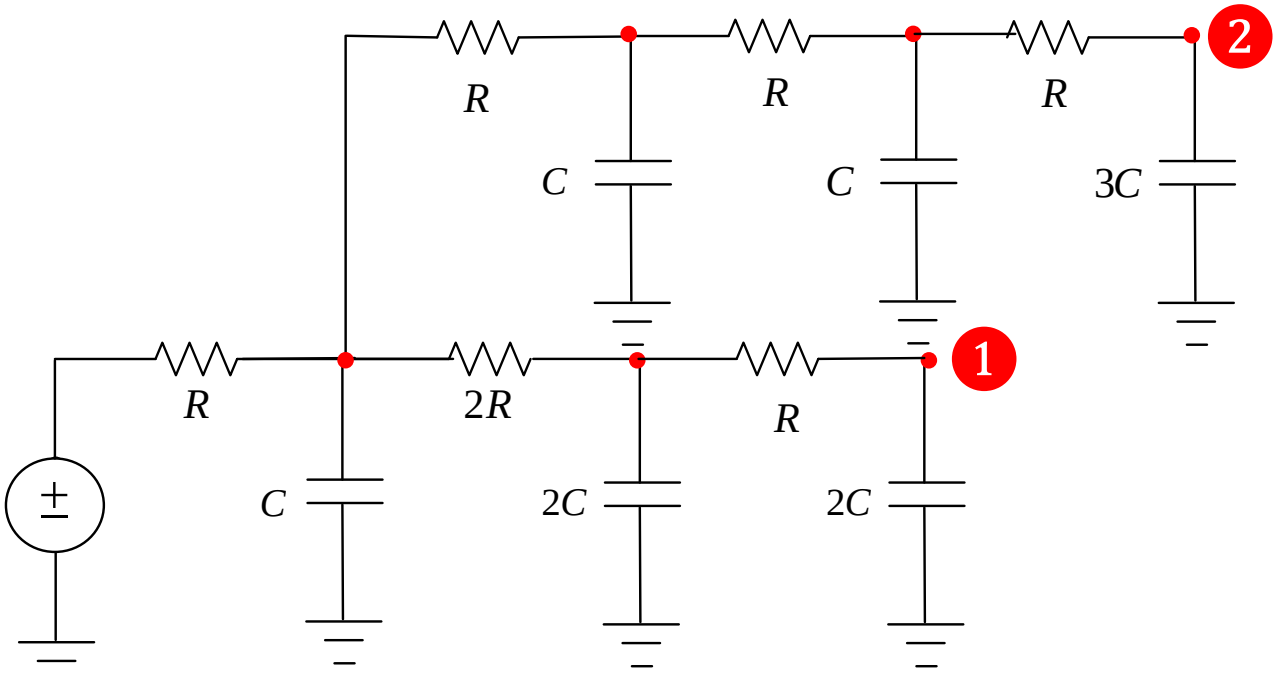


- Find the Time constant at all nodes.



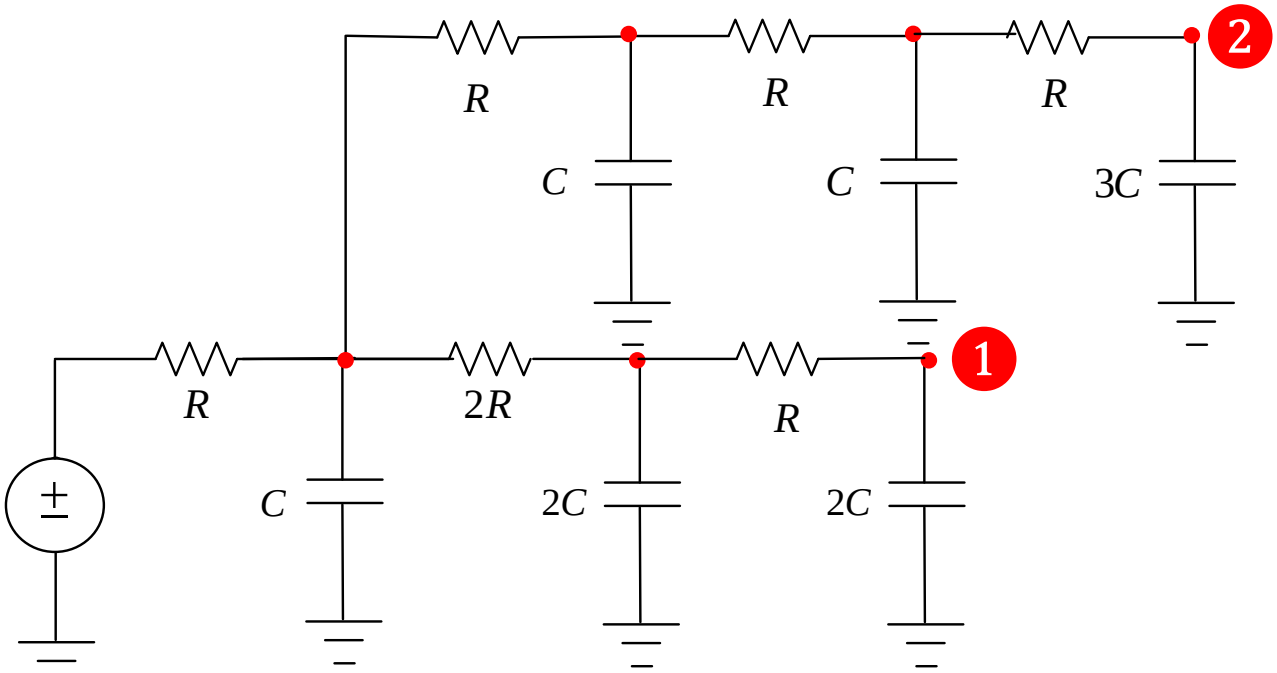
- Find the Time constant at all nodes.

$$\tau_{V_{in}-V_{out1}} = RC + 2C(R+2R) + 2C(R+2R+R)$$
$$+ R(C+C+3C) = 20RC$$

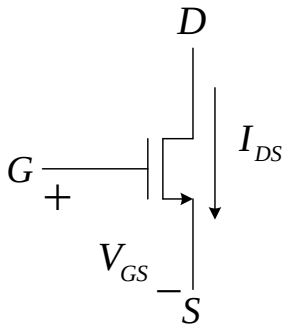


- Find the Time constant at all nodes.

$$\tau_{V_{in}-V_{out\,2}} = RC + C(R+R) + C(R+R+R)$$
$$+ 3C(R+R+R+R) + R(2C+2C) = 22RC$$

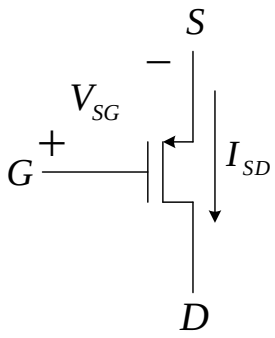


- nMOSFET



Operation Regions	Voltages	Current
Cut Off	$V_{GS} \le V_{Tn}$	$I_{DS} = 0$
Saturation	$V_{GS} > V_{Tn}$ $V_{DS} > V_{GS} - V_{Tn}$	$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2\left(1+\lambda V_{DS}\right)$
Resistive	$V_{GS} > V_{Tn}$ $V_{DS} < V_{GS} - V_{Tn}$	$I_{DS} = \mu_n C_{ox}\frac{W}{L}\left[\left(V_{GS} - V_{Tn}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$

- pMOSFET

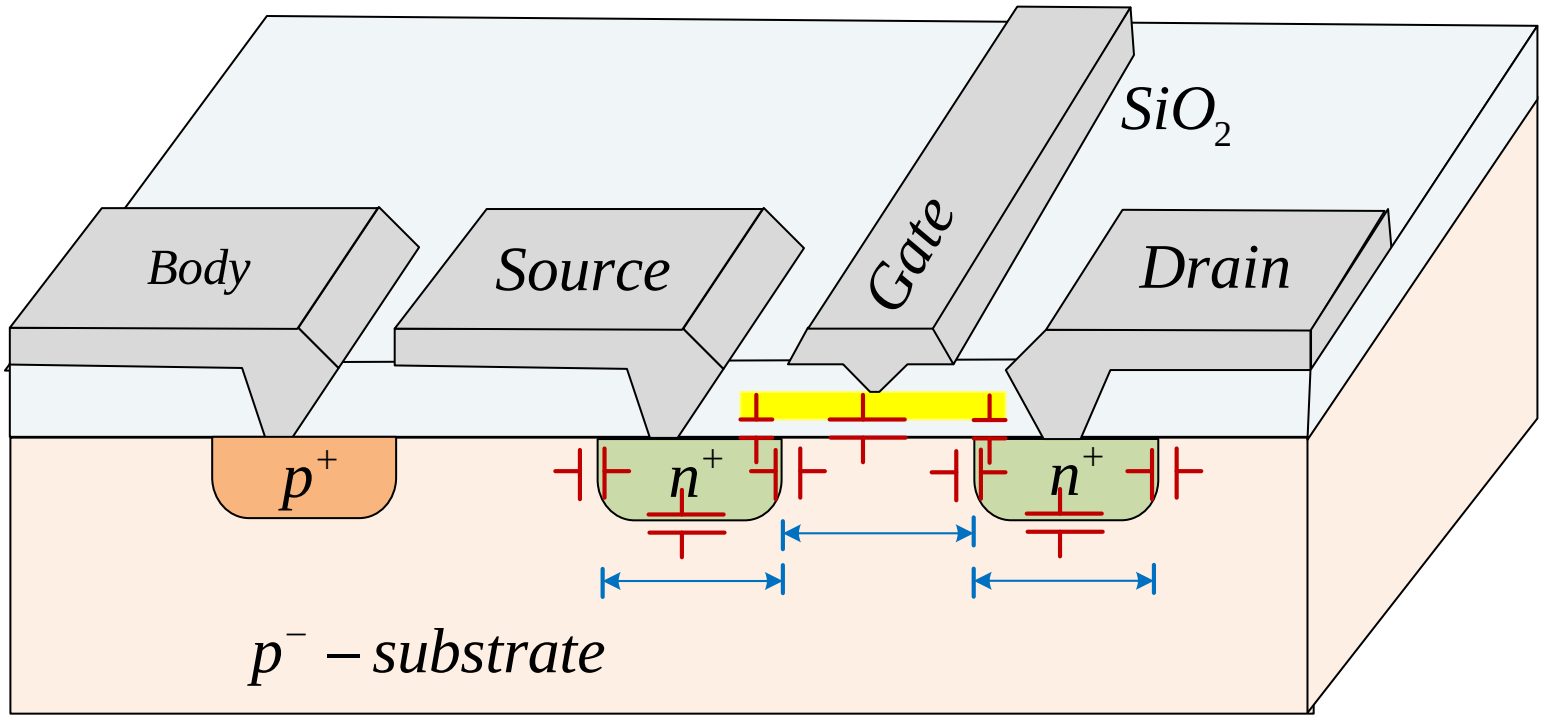


Operation Regions	Voltages	Current
Cut Off	$V_{SG} \le \lvert V_{Tp} \rvert$	$I_{SD} = 0$
Saturation	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} > V_{SG} - \lvert V_{Tp} \rvert$	$I_{SD} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG} - \lvert V_{Tp} \rvert\right)^2\left(1+\lambda V_{SD}\right)$
Resistive	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} < V_{SG} - \lvert V_{Tp} \rvert$	$I_{SD} = \mu_p C_{ox}\frac{W}{L}\left[\left(V_{SG} - \lvert V_{Tp} \rvert\right)V_{SD} - \frac{V_{SD}^2}{2}\right]$

- Enhancement mode MOSFET transistor region of operation

	Cut-off	Resistive	Saturation
nMOS	$V_{GSn} < V_{Tn}$ $V_{IN} < V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} < V_{GSn} - V_{Tn}$ $V_{OUT} < V_{IN} - V_{Tn}$	$V_{GSn} > V_{Tn}$ $V_{IN} > V_{Tn}$ $V_{DSn} > V_{GSn} - V_{Tn}$ $V_{OUT} > V_{IN} - V_{Tn}$
pMOS	$V_{GSp} > V_{Tp}$ $V_{IN} > V_{Tp} + V_{DD}$	$V_{GSp} < V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} > V_{GSp} - V_{Tp}$ $V_{OUT} > V_{IN} - V_{Tp}$	$V_{GSp} = V_{Tp}$ $V_{IN} < V_{Tp} + V_{DD}$ $V_{DSp} < V_{GSp} - V_{Tp}$ $V_{OUT} < V_{IN} - V_{Tp}$

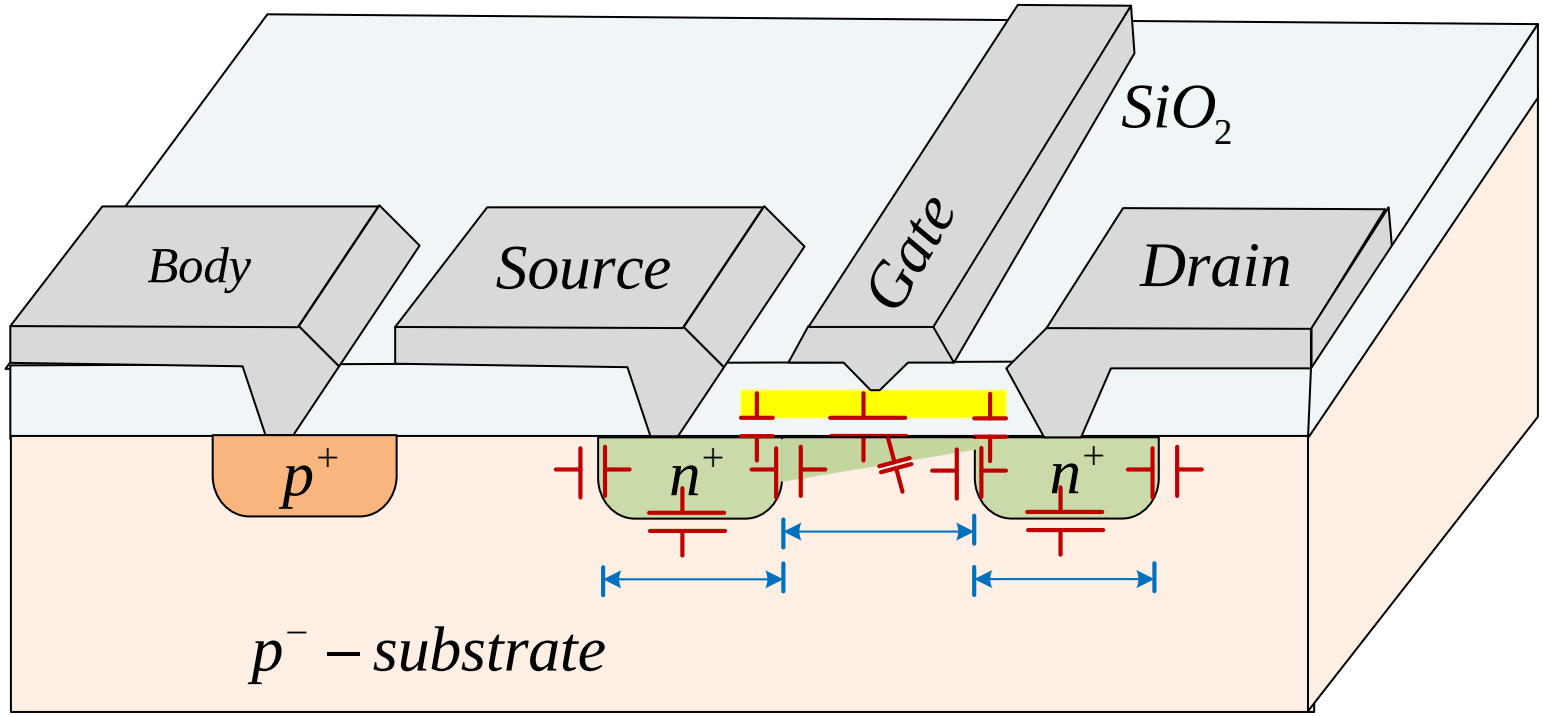
- Parasitic capacitors in the cut-off $V_{GS} < V_{TN}$



- Channel is not inverted

$$C_{gate} = C_{gate-body} = C_0 = C_{ox}WL = \frac{\varepsilon_{ox}}{t_{ox}}WL$$

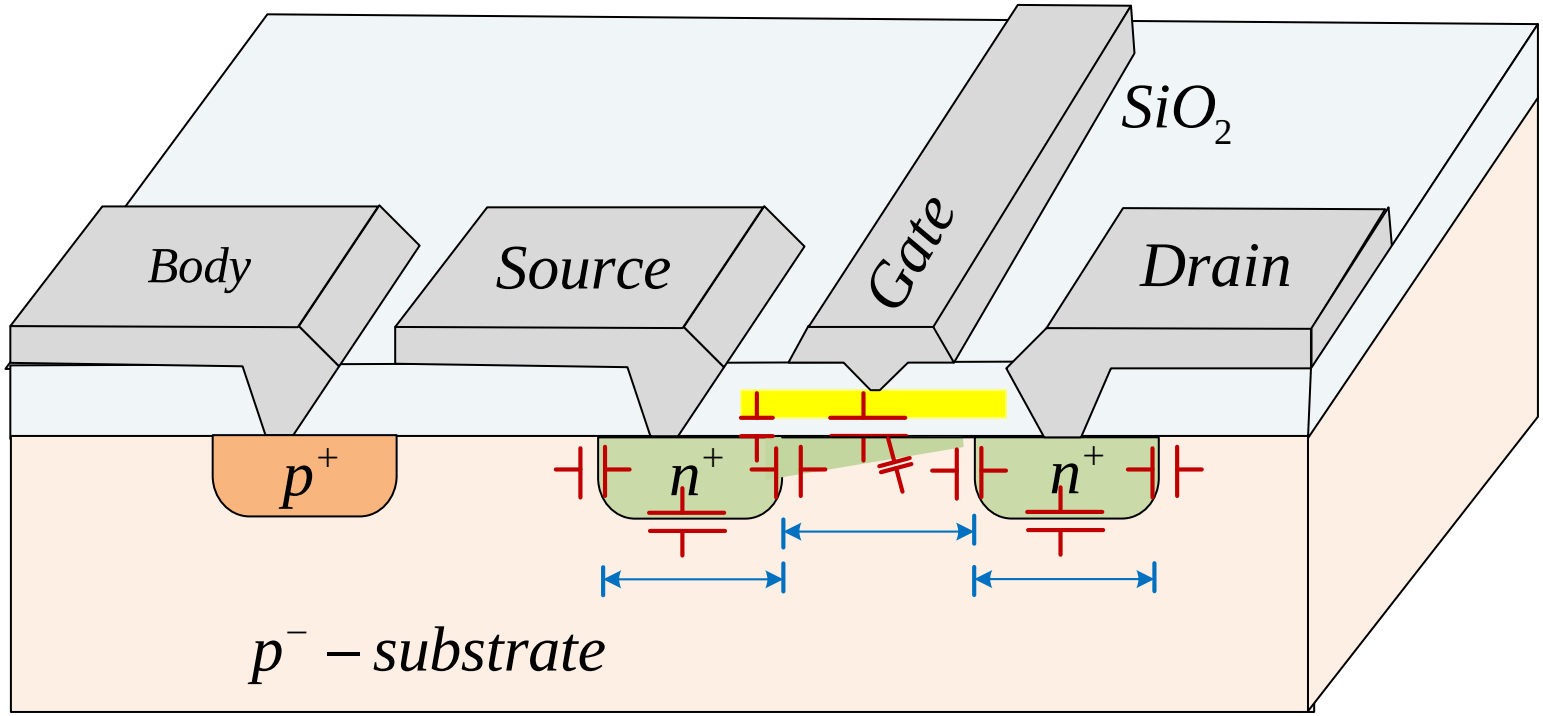
- Parasitic capacitors in the non-saturation $V_{GS} > V_{TN}$ & $V_{DS} < V_{GS} - V_{TN}$



$$C_{gate} = C_{gate-body} + C_{gate-source} + C_{gate-drain}$$

$$C_{gate} = 0 + \frac{C_0}{2} + \frac{C_0}{2} = C_0$$

- Parasitic capacitors in the saturation $V_{GS} > V_{TN}$ & $V_{DS} > V_{GS} - V_{TN}$



$$C_{gate} = C_{gate-body} + C_{gate-source} + C_{gate-drain}$$

$$C_{gate} = 0 + \frac{2C_0}{3} + 0 = \frac{2C_0}{3}$$

- Parasitic capacitors in the cut-off