Electronic Design Automation

Project 3

Presented to:

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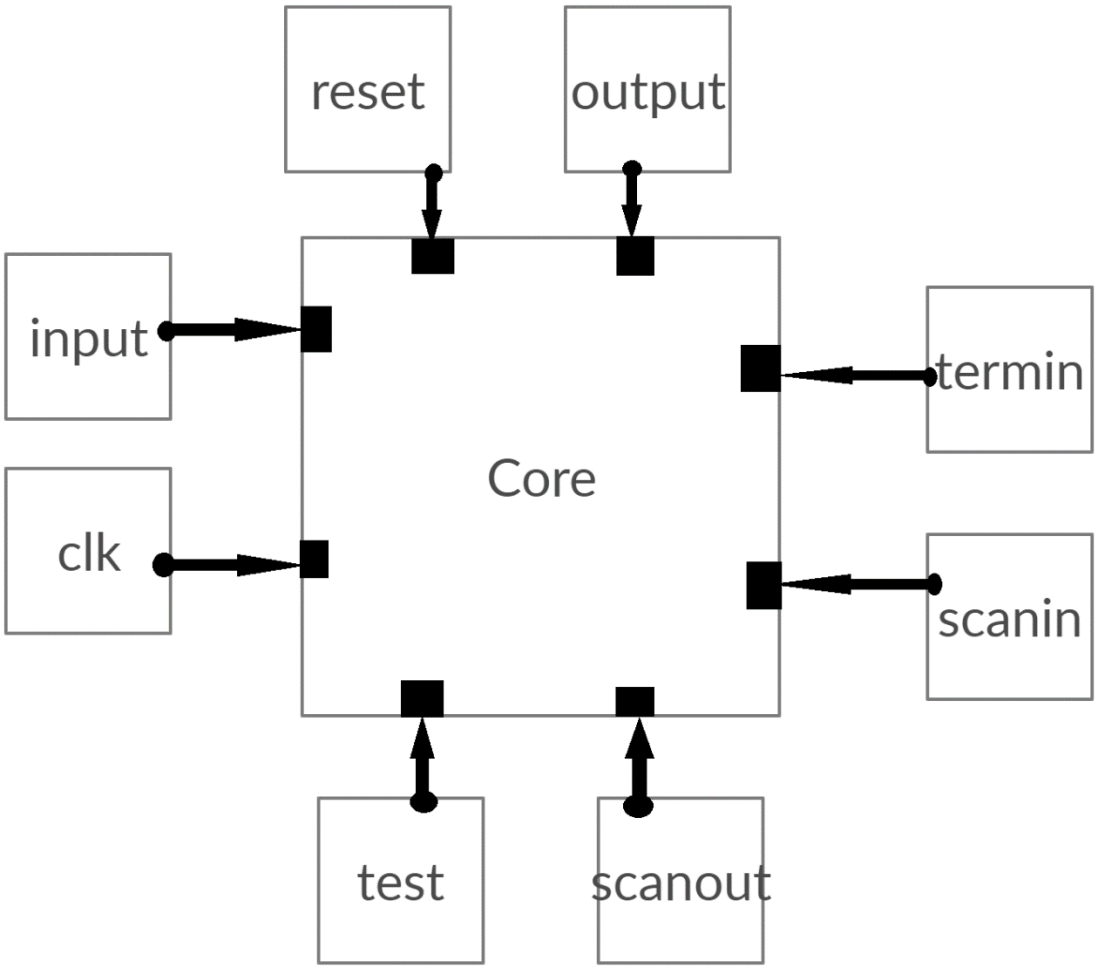
CESS

Contents

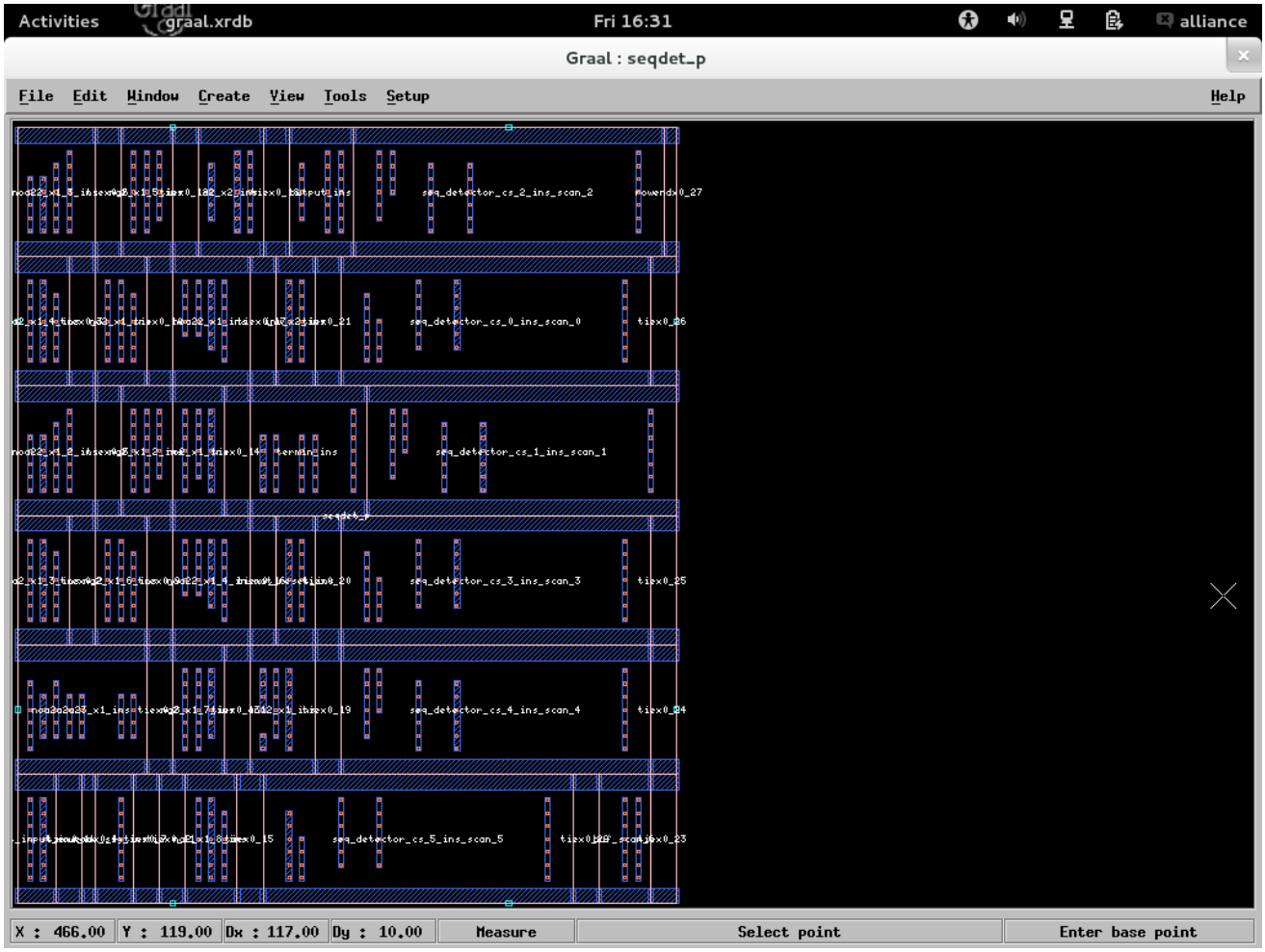
Introduction

This is the final step in our chip, and it is the physical synthesis. We will continue our work from the previous project and by the end we will obtain a ready-for-production chip layout.

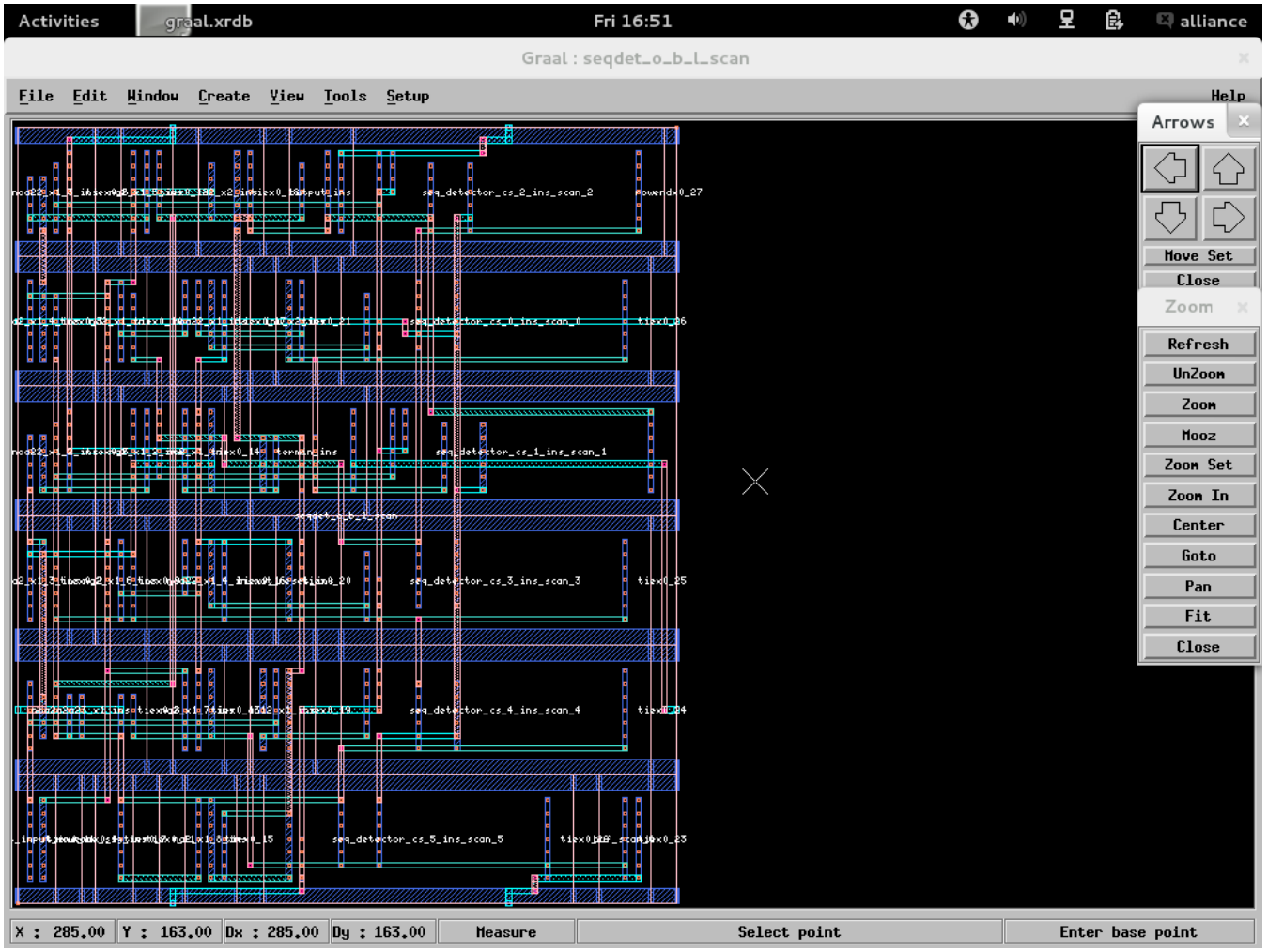
FloorPlanning



Placement


Activities
graal.xrdb
Fri 16:31
alliance
Graal : seqdet_p
File Edit Window Create View Tools Setup Help
seq_detector_cs_2_ins_scan_2
seq_detector_cs_0_ins_scan_0
seq_detector_cs_1_ins_scan_1
seq_detector_cs_3_ins_scan_3
seq_detector_cs_4_ins_scan_4
seq_detector_cs_5_ins_scan_5
X : 466.00
Y : 119.00
Dx : 117.00
Dy : 10.00
Measure
Select point
Enter base point

Routing


Activities
graal.xrdb
Fri 16:51
alliance
Graal : seqdet_o_b_l_scan
File Edit Window Create View Tools Setup Help
Arrows
Move Set
Close
Zoom
Refresh
UnZoom
Zoom
Mooz
Zoom Set
Zoom In
Center
Goto
Pan
Fit
Close
seq_detector_cs_2_ins_scan_2
seq_detector_cs_1_ins_scan_1
seq_detector_cs_3_ins_scan_3
seq_detector_cs_4_ins_scan_4
seq_detector_cs_5_ins_scan_5
X : 285.00
Y : 163.00
Dx : 285.00
Dy : 163.00
Measure
Select point
Enter base point

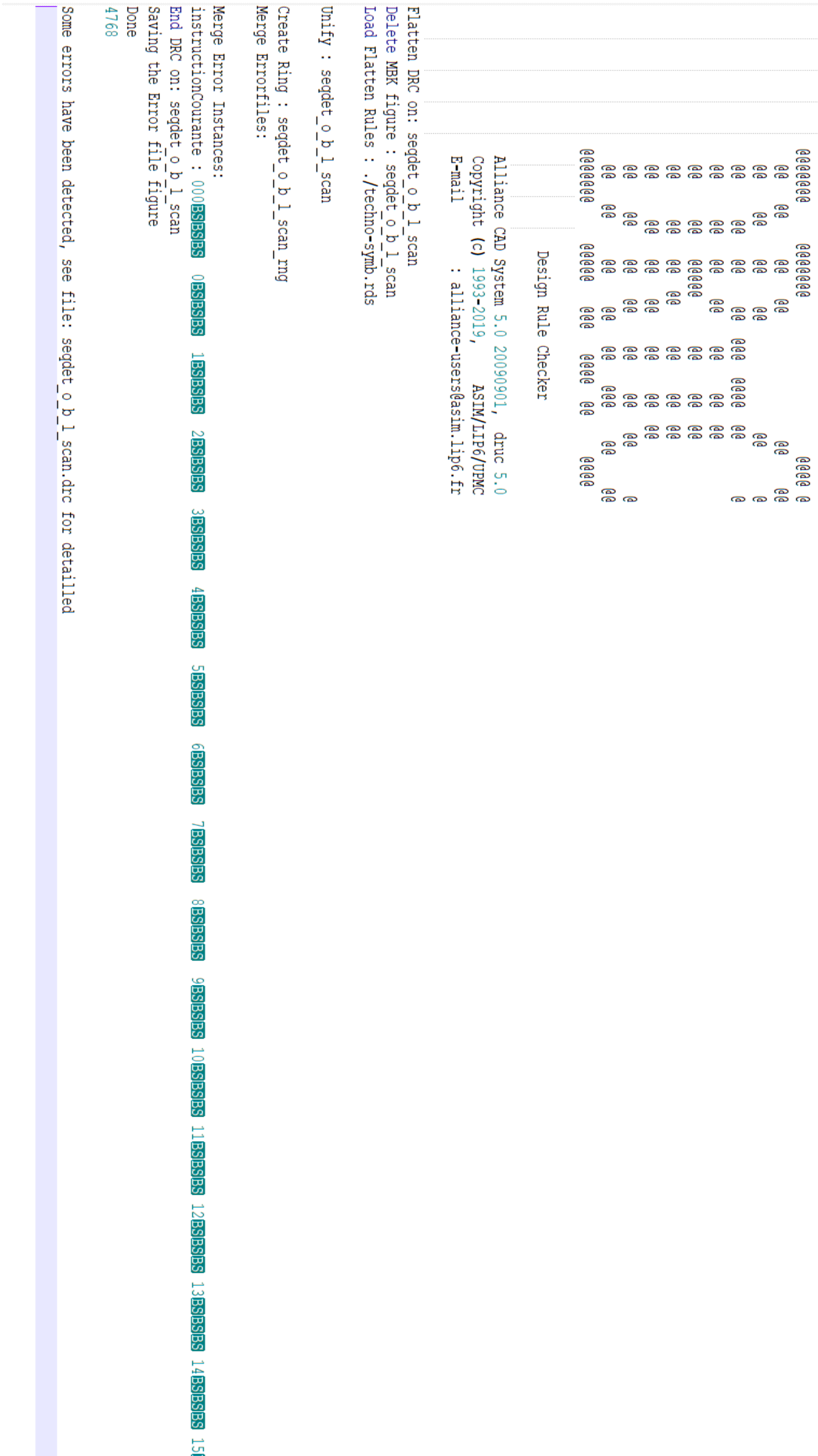
Post-Layout Verification

Layout-vs-Schematics (LVS)

Output:

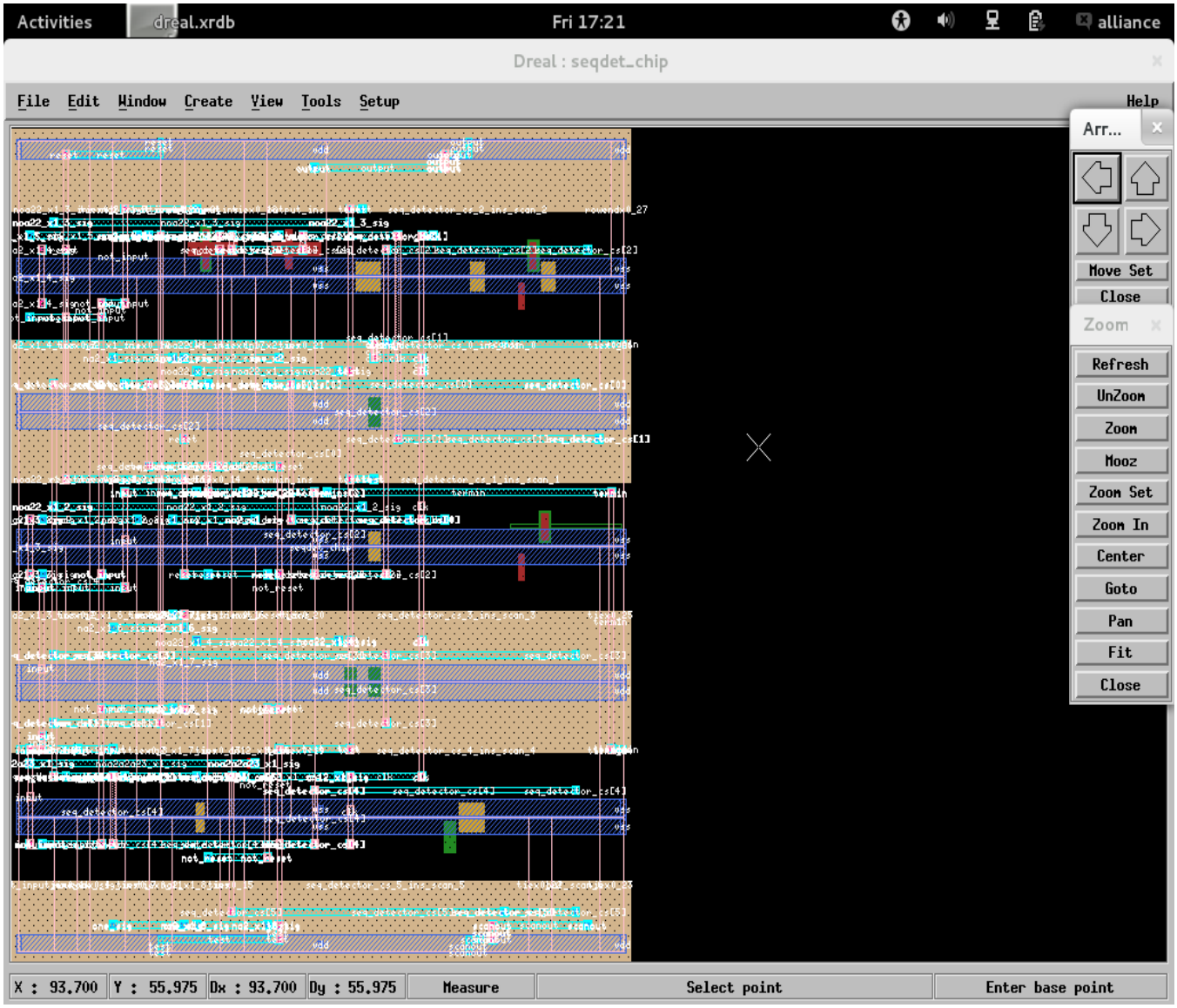
```
> cougar -v seqdet_o_b_l_scan > cougar_seqdet_o_b_l_scan.out
[alliance@localhost ~]$ lvx vst al seqdet_o_b_l_scan seqdet_o_b_l_scan -f
                        @@@@@@      @@@@    @@@ @@@@   @@@@
                          @@         @@      @   @@     @
                          @@         @@      @    @@   @
                          @@          @@    @      @@ @
                          @@          @@    @       @@
                          @@           @@  @        @@
                          @@           @@  @        @@@
                          @@            @@@        @  @@
                          @@      @     @@@       @    @@
                          @@     @       @       @      @@
                        @@@@@@@@@@       @      @@@    @@@@

                             Gate Netlist Comparator

                      Alliance CAD System 5.0 20090901,   lvx 1.4
                      Copyright (c) 1992-2019,     ASIM/LIP6/UPMC
                      E-mail        : alliance-users@asim.lip6.fr


***** Loading and flattening seqdet_o_b_l_scan (vst)...

***** Loading and flattening seqdet_o_b_l_scan (al)...


***** Compare Terminals .............
***** O.K.  (0 sec)

***** Compare Instances ..........
***** O.K.  (0 sec)

***** Compare Connections .............
***** O.K.  (0 sec)

===== Terminals .......... 10
===== Instances .......... 29
===== Connectors ......... 171


***** Netlists are Identical. ***** (0 sec)
```

Design-Rule Checking (DRC)



```
                 Design Rule Checker

  Alliance CAD System 5.0 20090901,  druc 5.0
  Copyright (c) 1993-2019,     ASIM/LIP6/UPMC
  E-mail        : alliance-users@asim.lip6.fr

Flatten DRC on: seqdet_o_b_l_scan
Delete MBK figure : seqdet_o_b_l_scan
Load Flatten Rules : ./techno-symb.rds

Unify : seqdet_o_b_l_scan

Create Ring : seqdet_o_b_l_scan_rng
Merge Errorfiles:

Merge Error Instances:
instructionCourante : 000BSBSBS  0BSBSBS  1BSBSBS  2BSBSBS  3BSBSBS  4BSBSBS  5BSBSBS  6BSBSBS  7BSBSBS  8BSBSBS  9BSBSBS 10BSBSBS 11BSBSBS 12BSBSBS 13BSBSBS 14BSBSBS 15
End DRC on: seqdet_o_b_l_scan
Saving the Error file figure
Done
4768

Some errors have been detected, see file: seqdet_o_b_l_scan.drc for detailled
```

Symbolic-to-Real Conversion



References

- Lectures
- Project description