**QUESTION NO : 6 (a)**

Elaborate logic of CLC that takes 2-bit input value and produces the square of the value in

binary form with the help of truth table. Draw neat & clean logic diagram. (Attach Simulated

circuit diagram as well).

* **EXPECTED TRUTH TABLE FOR 2-bit CLC FOR SQUARE DETERMINATION:**
* The number of inputs should be **2 i-e A and B**
* The range of input will be **0-3**
* The highest square value will be **3­­2 = 9**
* The binary form of 9(max range) is **1001 i-e 4-bit output**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** | **B** | **P0** | **P1** | **P2** | **P3** |
| **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** | **0** |
| **1** | **1** | **1** | **0** | **0** | **1** |

* **BOOLEAN EQUATION FOR P0:**

**AB**

* **BOOLEAN EQUATION FOR P1:**

**AB’**

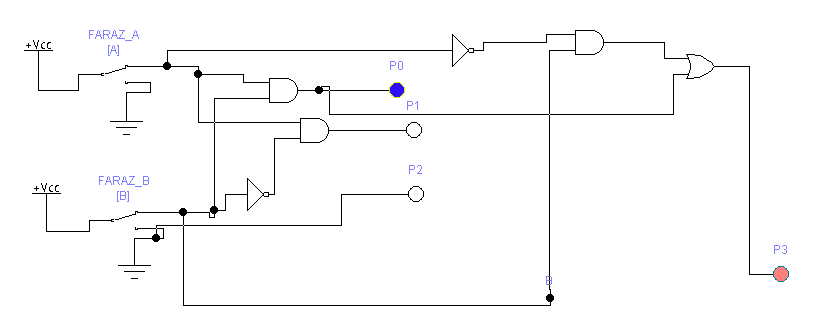
* **BOOLEAN EQUATION FOR P2:**

**0**

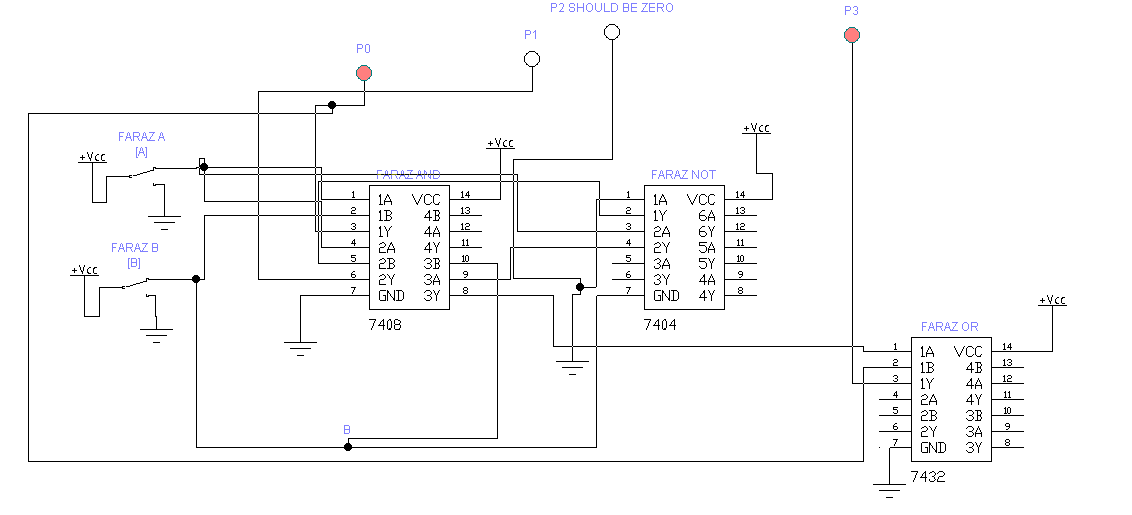
* **BOOLEAN EQUATION FOR P3:**

**A’B+AB**

* **GATE LEVEL DIAGRAM FOR CLC-SQUARE CIRCUIT:**



* **IC-LEVEL DIAGRAM FOR CLC-SQUARE CIRCUIT:**



**QUESTION NO : 6 (b)**

1. **Cascade two 8 \*1 and one 2 \*1 multiplexers to implement 16 \*1 multiplexer logic.**

* **TRUTH TABLE OF EXPECTED 16\*1 MUX:**
* **Where S0 , S1 , S2 and S3  are selecting input lines and S3 being MSB.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S3** | **S2** | **S1** | **S0** | **OUTPUT FROM** |
| **0** | **0** | **0** | **0** | **I0** |
| **0** | **0** | **0** | **1** | **I1** |
| **0** | **0** | **1** | **0** | **I2** |
| **0** | **0** | **1** | **1** | **I3** |
| **0** | **1** | **0** | **0** | **I4** |
| **0** | **1** | **0** | **1** | **I5** |
| **0** | **1** | **1** | **0** | **I6** |
| **0** | **1** | **1** | **1** | **I7** |
| **1** | **0** | **0** | **0** | **I8** |
| **1** | **0** | **0** | **1** | **I9** |
| **1** | **0** | **1** | **0** | **I10** |
| **1** | **0** | **1** | **1** | **I11** |
| **1** | **1** | **0** | **0** | **I12** |
| **1** | **1** | **0** | **1** | **I13** |
| **1** | **1** | **1** | **0** | **I14** |
| **1** | **1** | **1** | **1** | **I15** |

* **ROUGH SKETCH FOR ABOVE CASCADING:**

**1 OUTPUT LINE**

**16 INPUT LINES**

**FARAZ**

**2\*1 MUX**

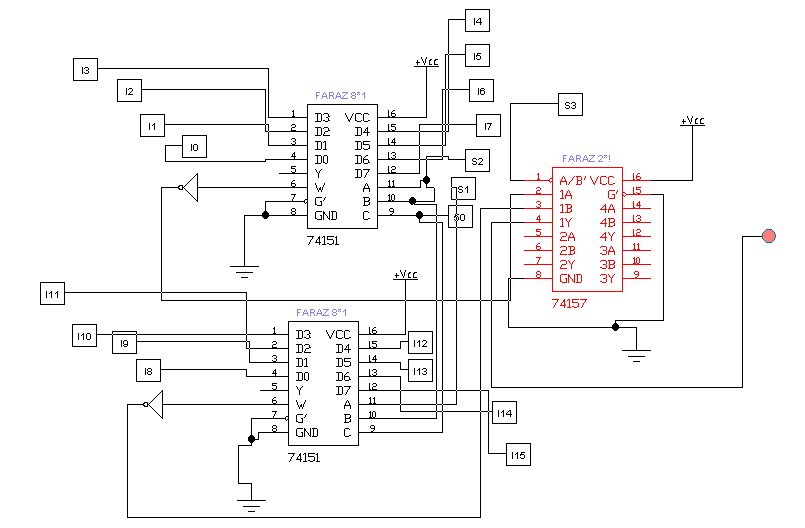
**FARAZ**

**8\*1 MUX**

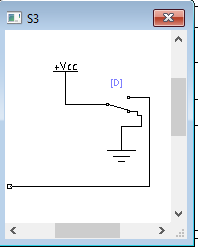
**FARAZ**

**8\*1 MUX**

* **IC-LEVEL IMPLEMENTATION FOR 16\*1 MUX CASCADING:**



* **SUB-CIRCUIT FOR EACH SWITCH:**
* **Where toggle key for each switch is different**

* **EXPLAINATION:**

In 16\*1 multiplexer , there are 16 input lines and one output line with 4 selecting input lines. The selecting input lines decides which input line transmit the signal to output.

To cascade the above from two 8\*1 and one 2\*1 mux, we have 3 select input lines in both 8\*1 mux. So connect the selecting inputs of both 8\*1 mux with eachother which are S0 , S1 , S2. The 2\*1 MUX has only one selecting input line which become the 4th one which is S3. In the circuit S3  will be MSB.

This S3 will be responsible to switch two 8\*1 mux to generate desired output.

For example, if the input is 1000 .Since in this example S3 is ‘1’ then output will be from second 8\*1 mux then later bits are ‘000’ hence output will be from ‘D0(from IC)’ which is ‘I8’.

**ii. Draw the logic diagram of a 2-to-4 line decoder using NOR gates only. Include an enable**

**input. (Attach Simulated circuit diagram as well).**

* **TRUTH TABLE FOR 2\*4 DECODER:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **E** | **A** | **B** | **P0** | **P1** | **P2** | **P3** |
| **1** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** | **0** | **0** |
| **1** | **1** | **0** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** | **0** | **1** |
| **0** | **DON’T CARE** | **DON’T CARE** | **0** | **0** | **0** | **0** |

* **BOOLAEN EQUATION FOR P0:**

**E A’ B’**

* **BOOLAEN EQUATION FOR P1:**

**E A’ B**

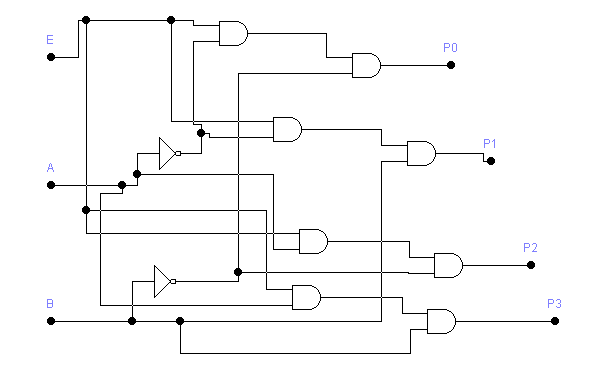
* **BOOLAEN EQUATION FOR P2:**

**E A B’**

* **BOOLAEN EQUATION FOR P3:**

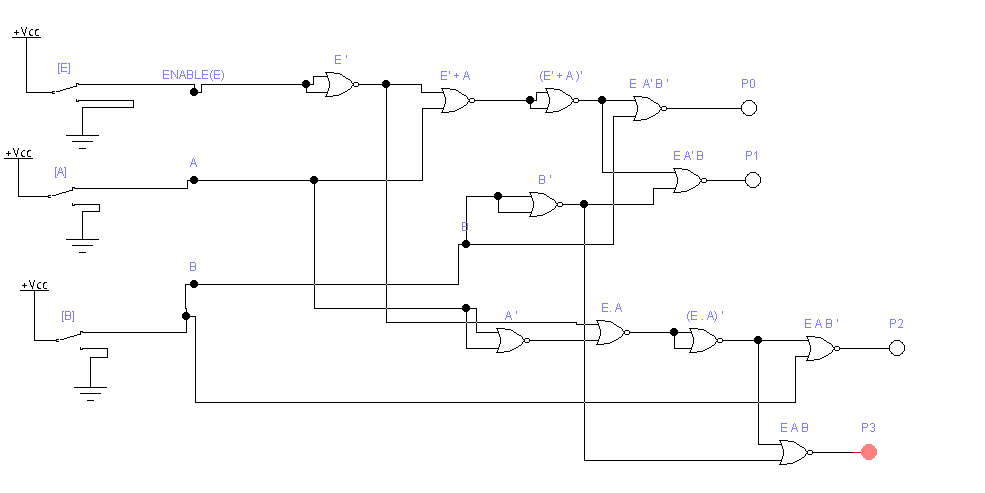
**E A B**

* **CIRCUIT FOR 2\*4 LINE DECODER WITHOUT USING NOR-GATES:**

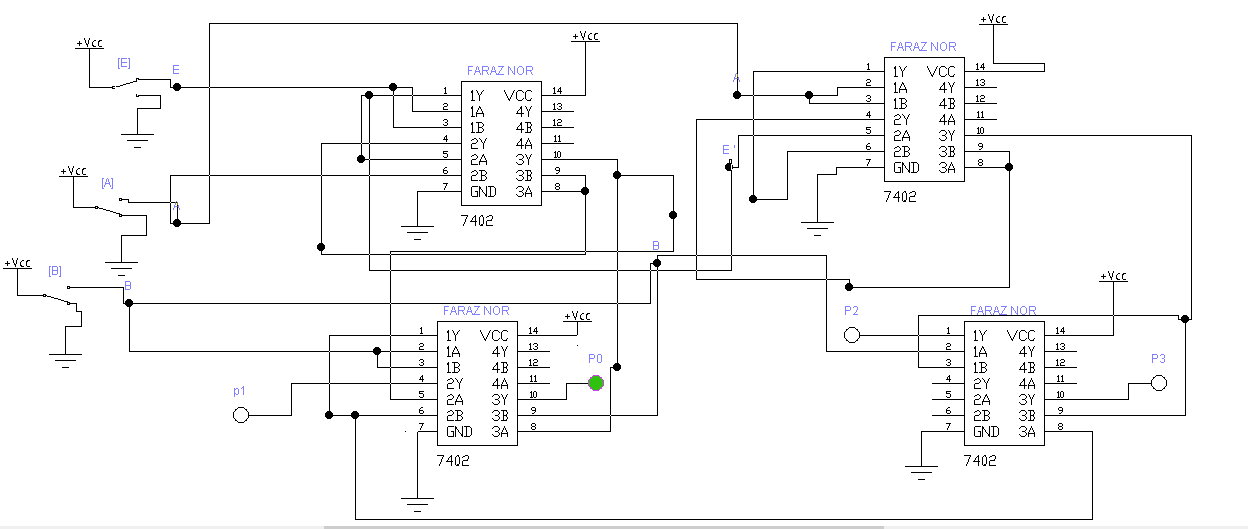


* **NOR – REALIZATION OF ABOVE CIRCUIT:**

By applying NOR-REALIZATION to above simple circuit, we got 2\*4 line decoder WITH only NOR-GATES.



* **IC-LEVEL IMPLEMENTATION FOR ABOVE DECODER:**



* **EXPLAINATION:**

From truth table of 2\*4 line decoder, we pick the Boolean equations for each output lines i-e P0 , P1 , P2 and P3.

Then we draw the simple circuit without using NOR GATES.

After all we applied NOR-REALIZATION METHOD to convert that circuit to NOR-GATES.