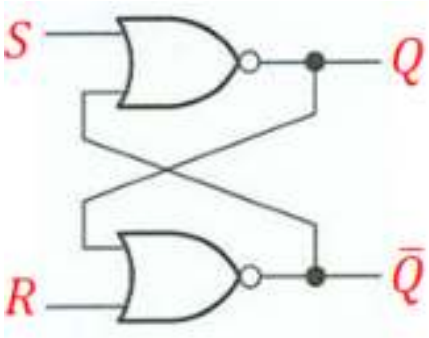
Chapter 7 (Part I)
Latches and Flip-Flops

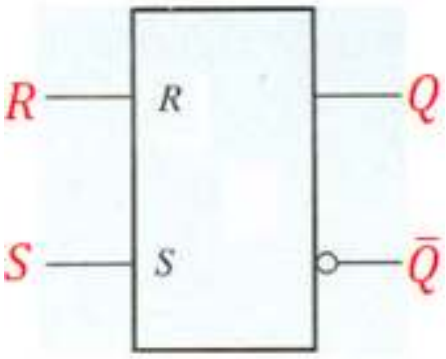
Latches

- Temporary storage device that has two stable states (bistable) or multivibrator.
- Be able to:
  1. Explain the operation of basic S-R latch
  2. Explain the operation of a gated S-R latch
  3. Explain the operation of a gated D latch
  4. Implement an S-R or D latch with logic gates

S-R (Set-Reset) Latch

- Active-HIGH input S-R latch





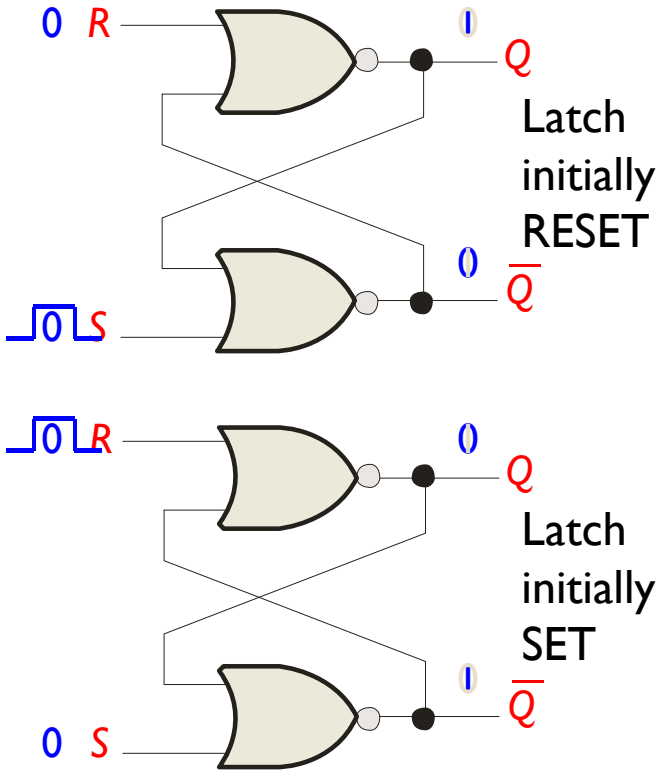
S	R	Q	$\bar{Q}$	Remarks
0	0	NC	NC	No change
0	1	0	1	Latch RESET
1	0	1	0	Latch SET
1	1	?	?	Invalid Condition

Truth table for active-HIGH input S-R Latch

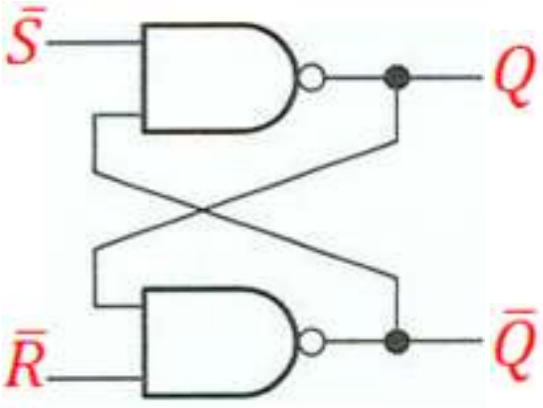
The active-HIGH *S*-*R* latch is in a stable (latched) condition when both inputs are LOW.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the *S* input while the *R* remains LOW.

To RESET the latch ($Q = 0$), a momentary HIGH signal is applied to the *R* input while the *S* remains LOW.

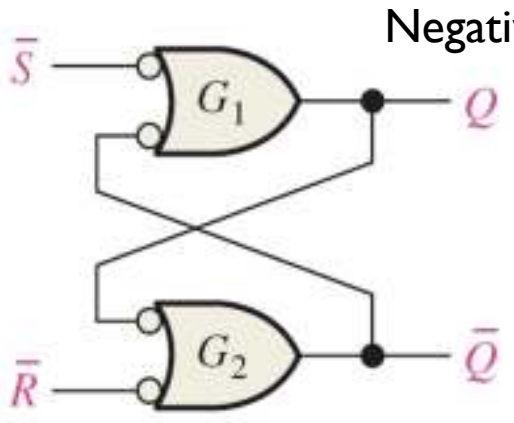


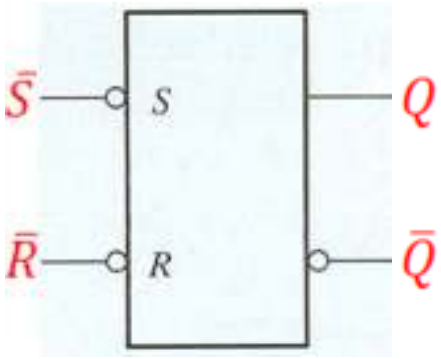
- Active-LOW input $\bar{S} - \bar{R}$ latch



NAND

Negative-OR





$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	Remarks
0	0	?	?	Invalid Condition
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
1	1	NC	NC	No change (latch remain in present state, stable condition)

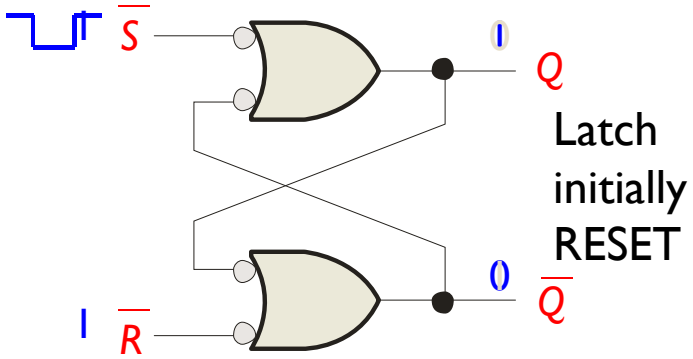
Truth table for active-LOW input $\bar{S} - \bar{R}$ Latch

The active-LOW *S*-*R* latch is in a stable (latched) condition when both inputs are HIGH.

Assume the latch is initially RESET (Q = 0) and the inputs are at their inactive level (1). To SET the latch (Q = 1), a momentary LOW signal is applied to the $\overline{S}$ input while the $\overline{R}$ remains HIGH.

To RESET the latch a momentary LOW is applied to the $\overline{R}$ input while $\overline{S}$ is HIGH.

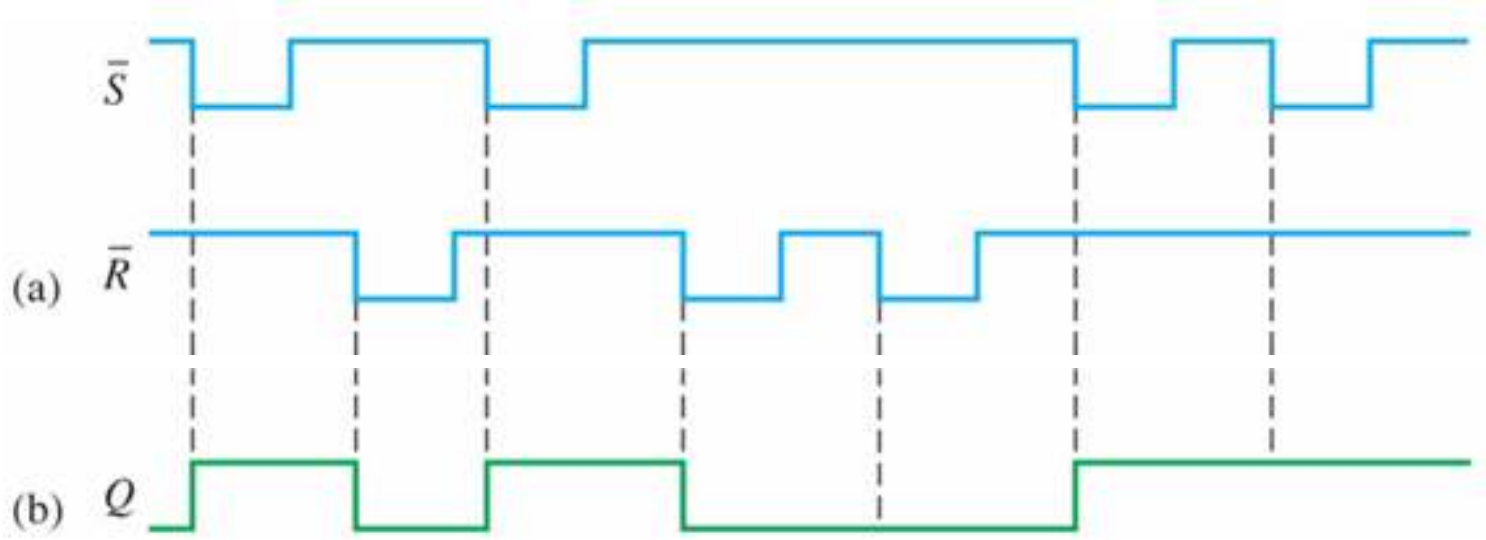
Never apply an active set and reset at the same time (invalid).



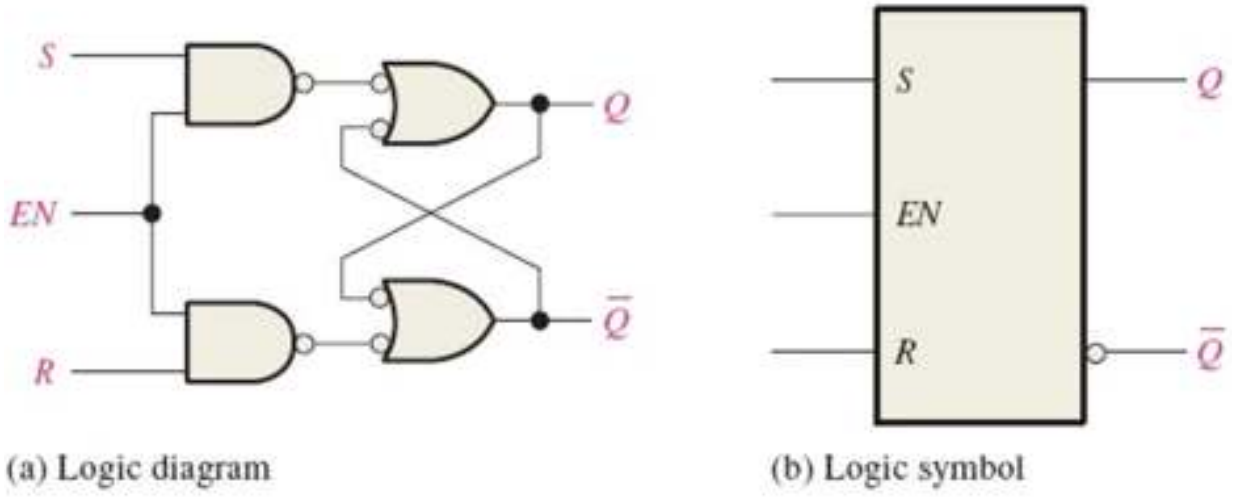
Example

If the $\bar{S} - \bar{R}$ waveforms are applied to the inputs of the latch. Determine the waveform that will be observed on the Q output. Assume that Q is initially LOW

Solution



Gated S-R (Set-Reset) Latch



(a) Logic diagram (b) Logic symbol

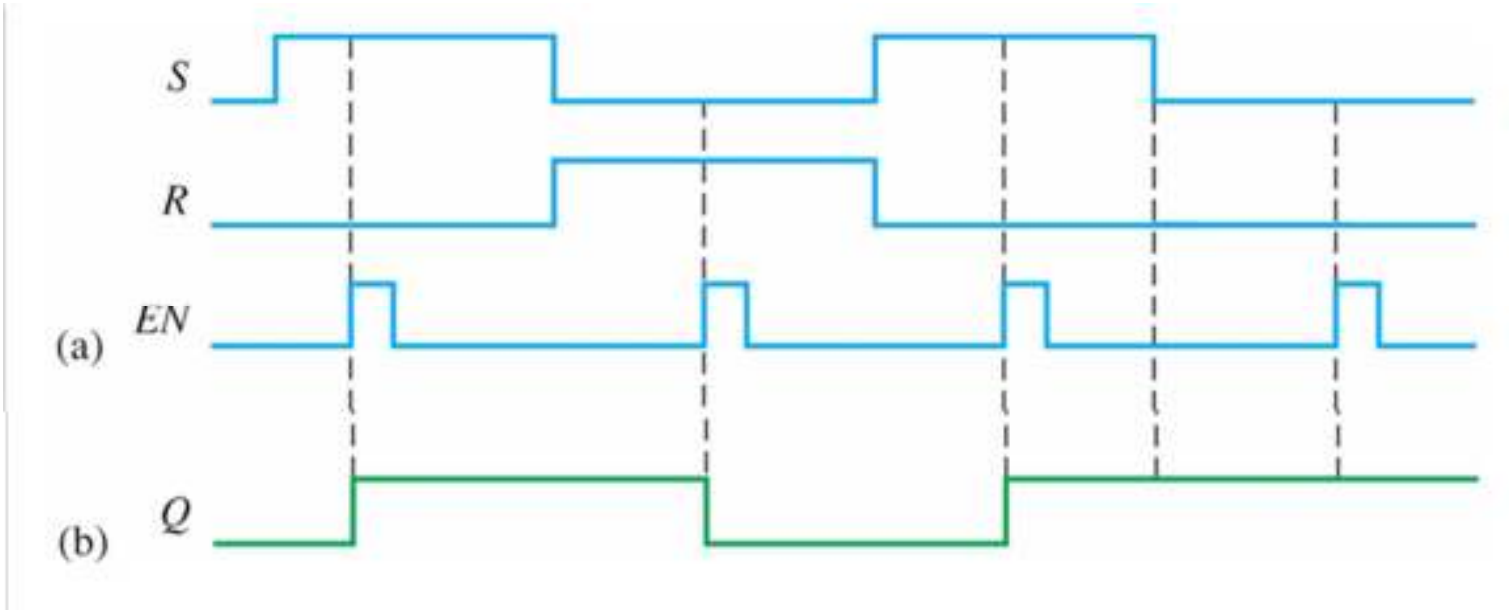
- A gate input is added to the S-R latch to make the latch synchronous.
- The gated latch has an additional input, called enable (*EN*) that must be HIGH in order for the latch to respond to the *S* and *R* inputs.
- When the enable input is LOW, the latch remains in the hold condition.

Example

Determine the Q output waveform if the inputs shown below are applied to a gated S-R latch that is initially RESET

Solution

Keep in mind that *S* and *R* are only active when *EN* is HIGH.



Gated D Latch

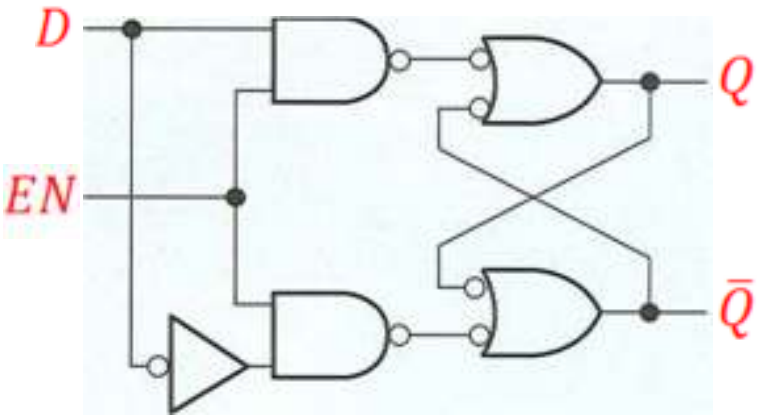


Figure 7.9: Logic diagram for gated D Latch

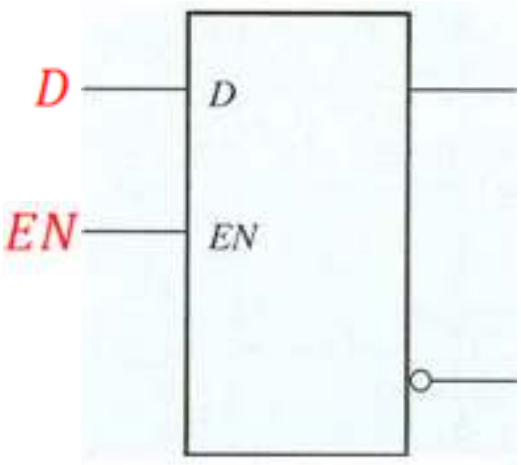


Figure 7.10: Logic symbol for gated D Latch

D	EN	Q	$\bar{Q}$	Remarks
0	1	0	1	RESET
1	1	1	0	SET
X	0	NC	NC	No Change

Table 7.3: Truth table for gated D Latch

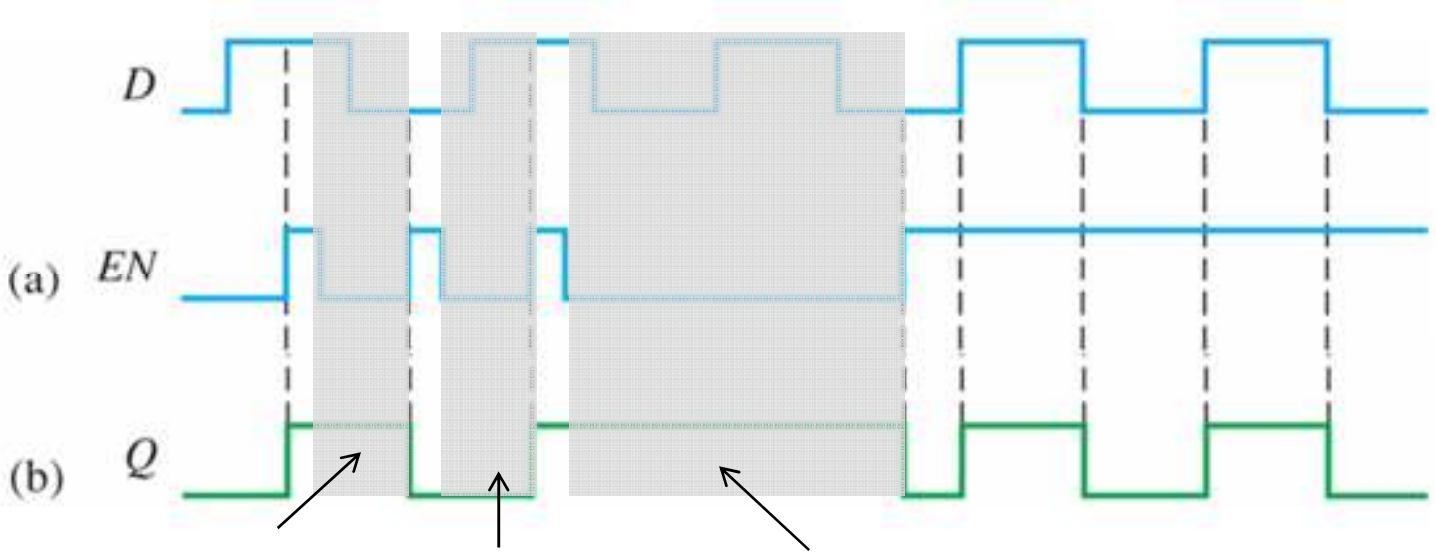
A simple rule for the *D* latch is:

Q follows *D* when the Enable is active.

Example

Determine the Q output waveform if the inputs shown below are applied to a gated D latch that is initially RESET

Solution



Notice that the Enable is not active during these times, so the output is latched.

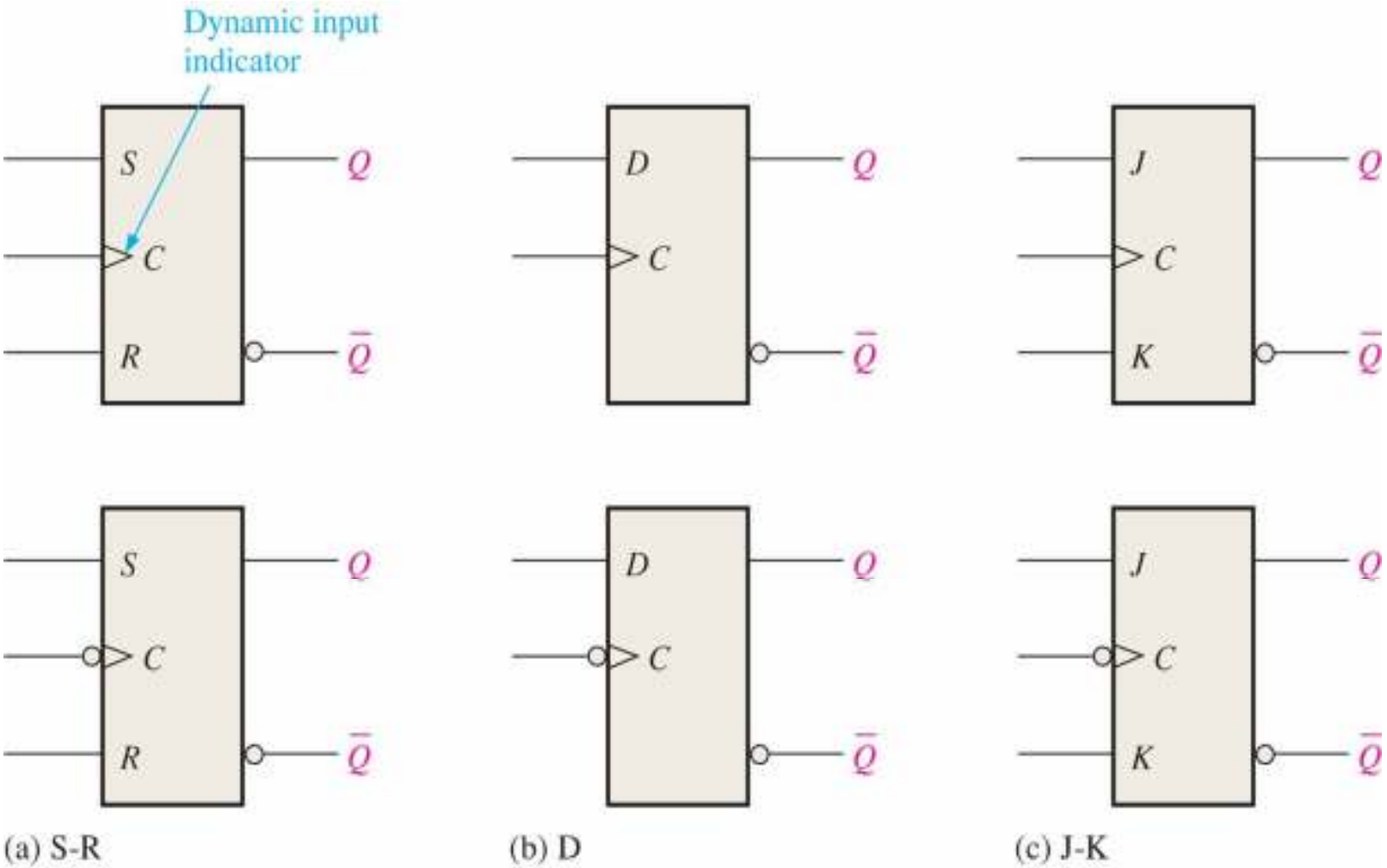
Flip-Flop

- Synchronous bistable devices aka bistable multivibrators.
- Be able to:
  1. Differentiate between latches and flip-flop
  2. Explain the operation of basic S-R, D and J-K flip-flop
  3. Explain flip-flop operating characteristic
  4. Discuss flip-flop applications

Edge-Triggered flip-flop

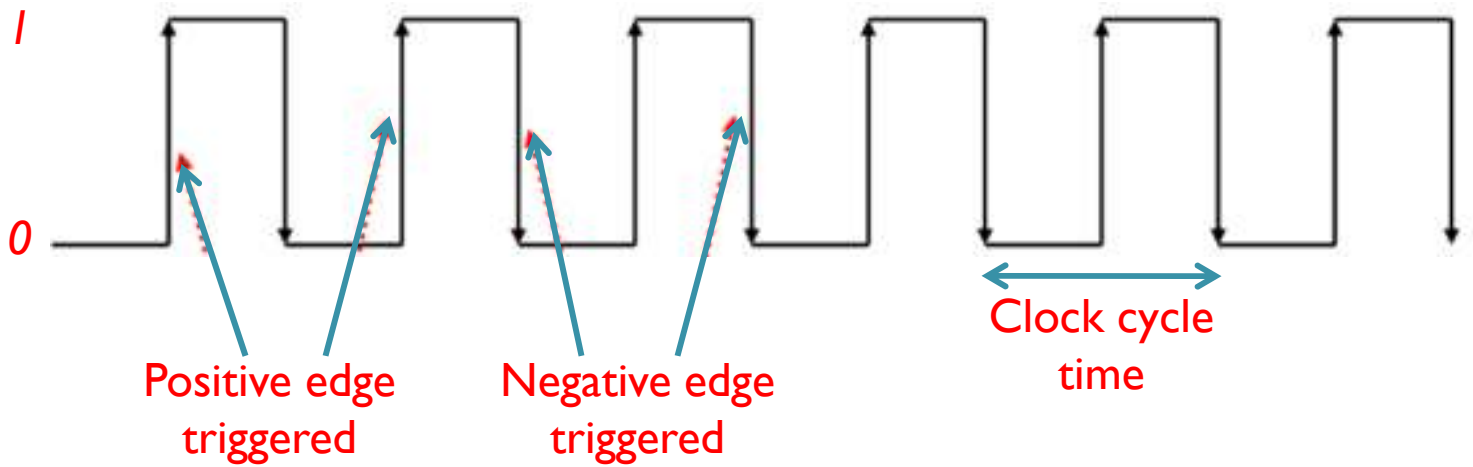
- The output changes state only at a specified point on the triggering input called CLOCK (CLK), control input.
- Can be either positive edge triggered (no bubble at clock (*C*) input) or negative edge triggered (bubble at clock (*C*) input).

Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).



Clock Signal

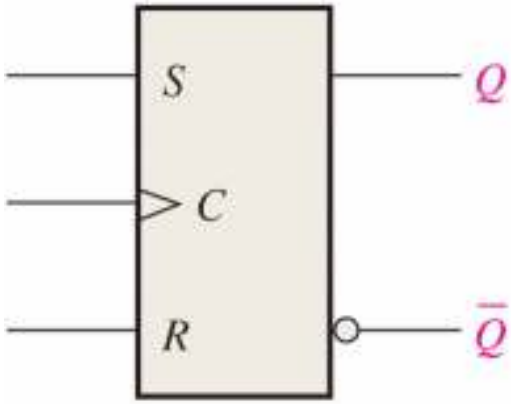
- Clock signal is a periodic square wave that indefinitely switches values from 0 to 1 and 1 to 0 at fixed intervals.



Clock signal.

Edge triggered S-R flip-flop

- SET (S) and RESET (R) inputs of the S-R flip-flop are called synchronous input.
- Data on these inputs are transferred to the output only on the triggering edge of the clock pulse.



Logic symbol for positive edge triggered S-R flip-flop

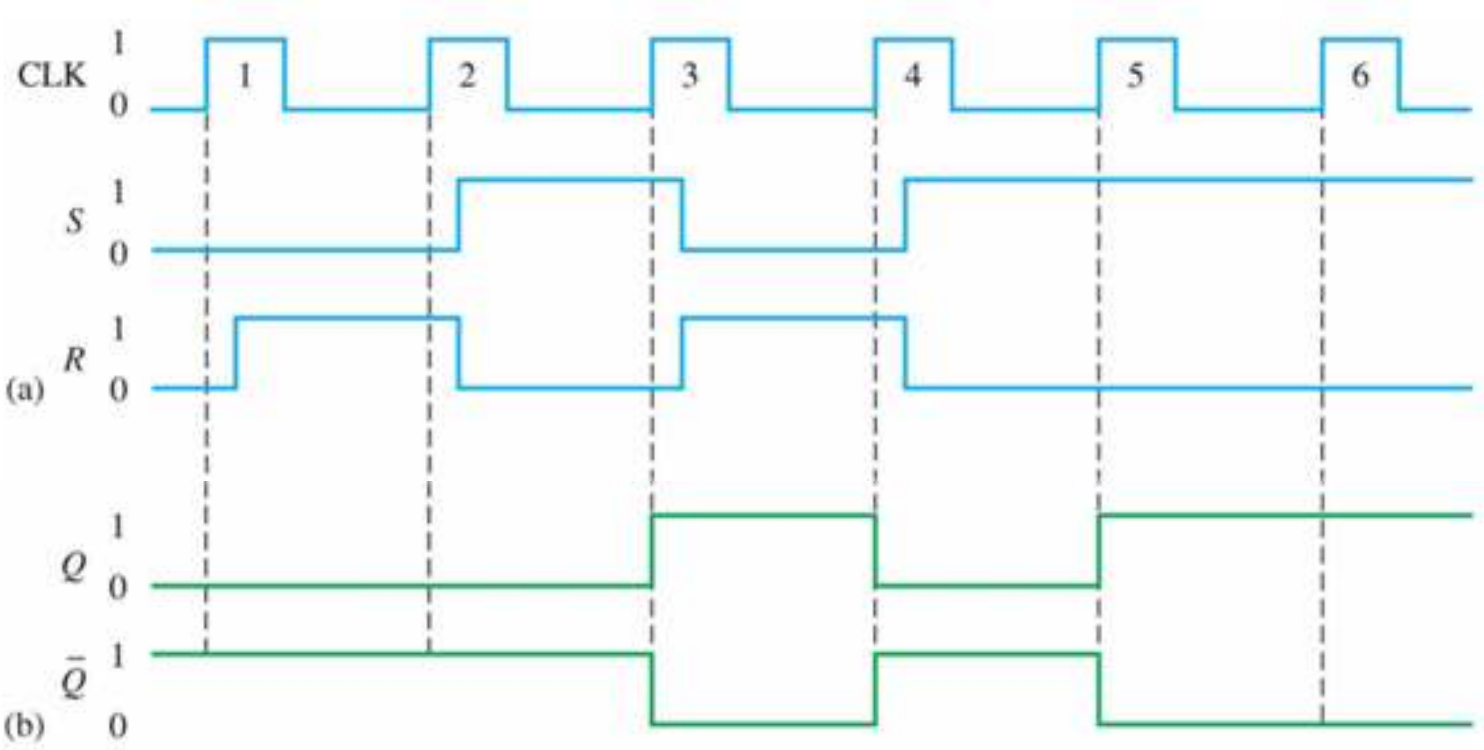
S	R	CLK	Q	$\bar{Q}$	Remarks
X	X	X	NC	NC	No Change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid Condition
↑ = clock transition from LOW to HIGH					
X = Don't care (0 or 1)					
NC = No change					
? = Invalid condition					

Truth table for positive edge triggered S-R flip-flop

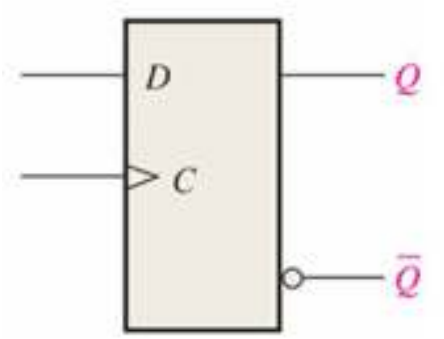
Example

Determine the Q and $\bar{Q}$ output waveform of the positive edge triggered S-R flip-flop for the S, R and CLK input below. Assume that the flip-flop is initially RESET

Solution



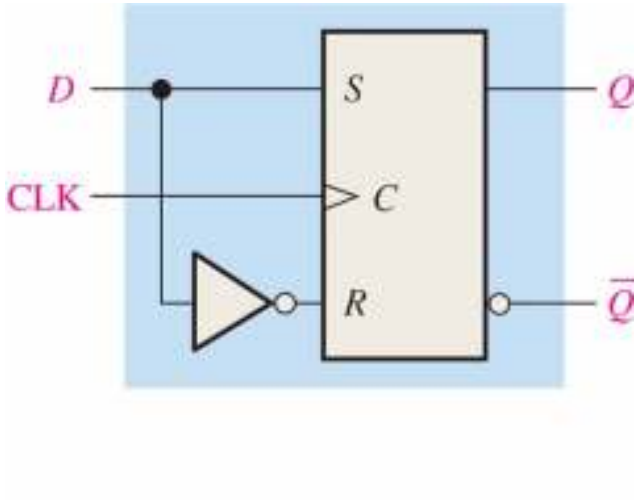
Edge triggered D flip-flop



Logic symbol for positive edge triggered D flip-flop

D	CLK	Q		Remarks
X	X	NC	NC	No Change
1	↑	1	0	SET
0	↑	0	1	RESET
↑ = clock transition from LOW to HIGH				
X = Don't care (0 or 1)				
NC = No change				

Truth table for positive edge triggered D flip-flop

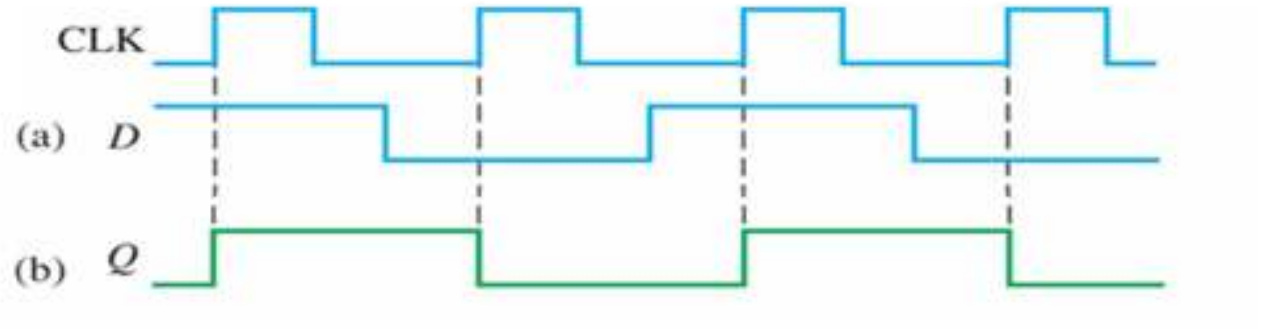


A positive edge-triggered D flip-flop formed with an S-R flip-flop and an inverter

Example

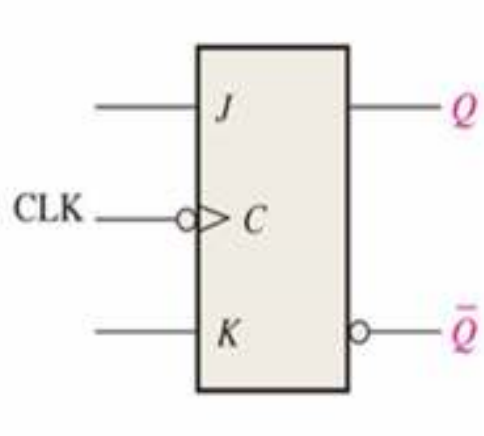
From the waveform for the D input and the clock, determine the Q output waveform if the flip-flop starts out RESET

Solution



Edge triggered J-K flip-flop

- Edge triggered J-K will only accept the *J* and *K* inputs during the active edge of the clock.



Logic symbol for positive edge triggered J-K flip-flop

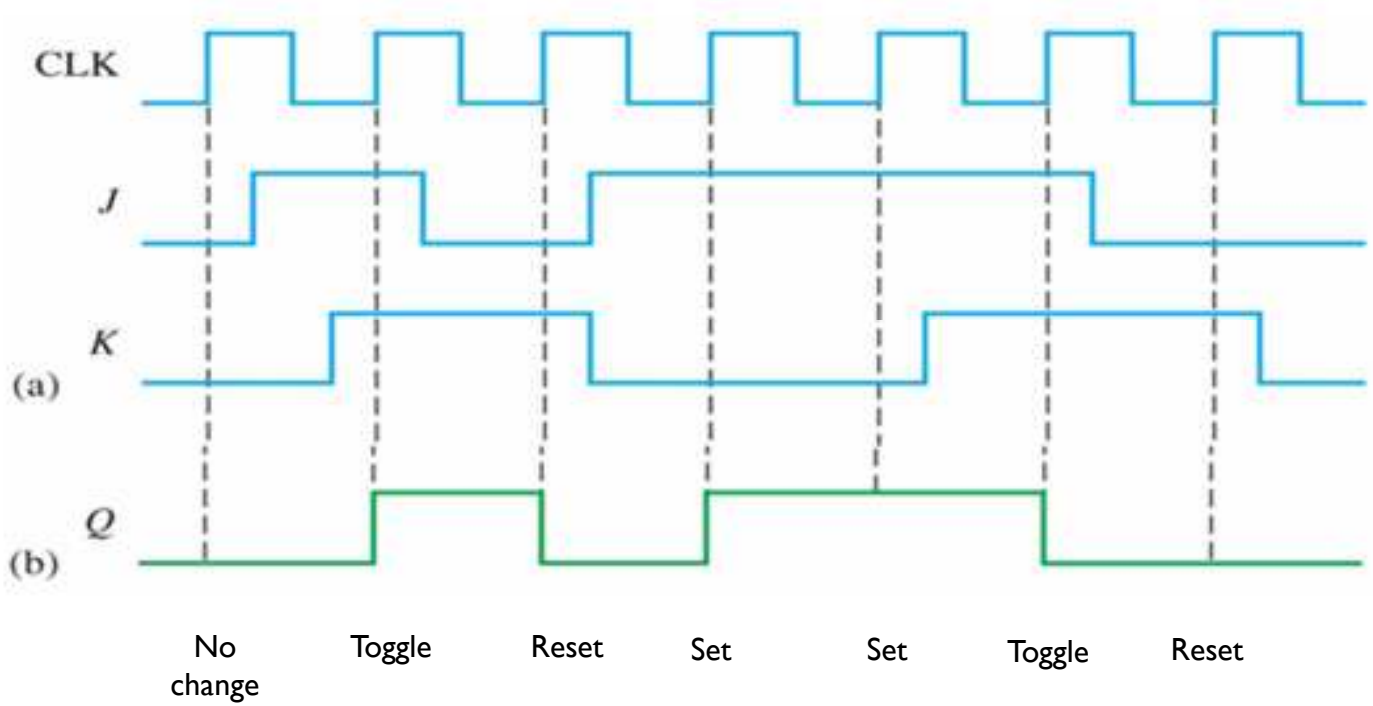
J	K	CLK	Q	$\bar{Q}$	Remarks
X	X	X	Q_0	$\bar{Q}_0$	No Change
0	0	↑	Q_0	$\bar{Q}_0$	No Change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle
↑ = clock transition from LOW to HIGH					
Q_0 = output level prior to clock transition					
X = Don't care (0 or 1)					

Truth table for positive edge triggered J-K flip-flop

Example

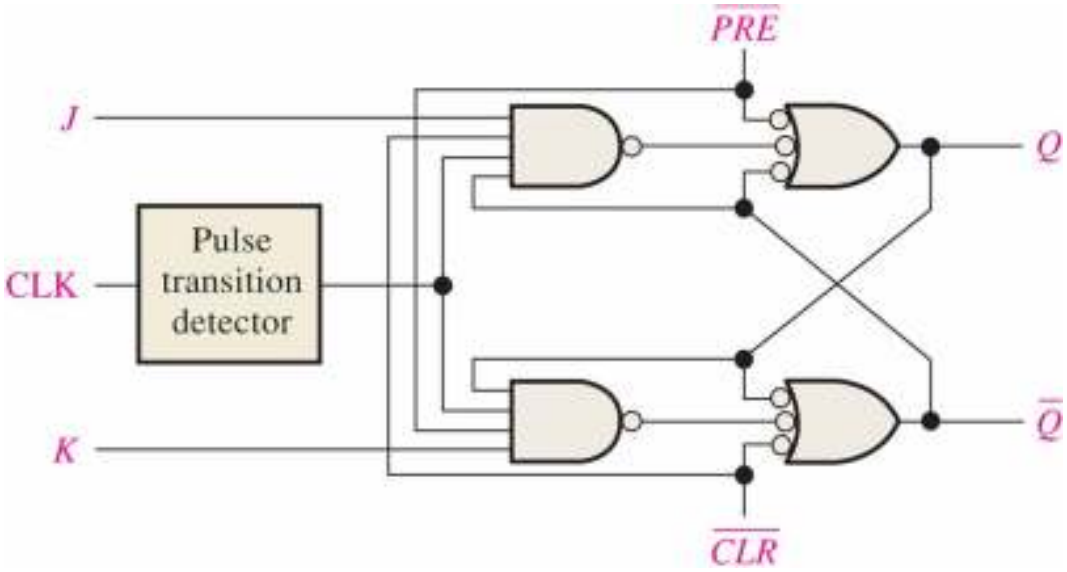
From the waveform for the positive edge triggered J-K input and the clock, determine the Q output waveform if the flip-flop starts out RESET

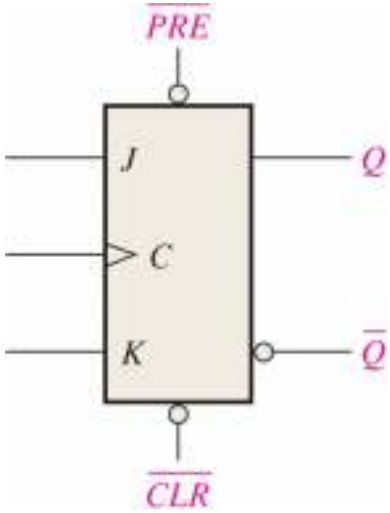
Solution



How about for negative edge triggered J-K flip flop?

Asynchronous Preset and Clear Inputs



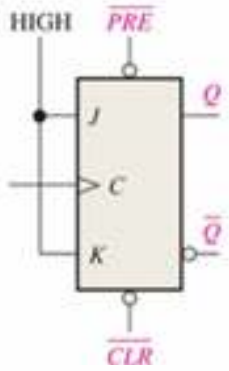


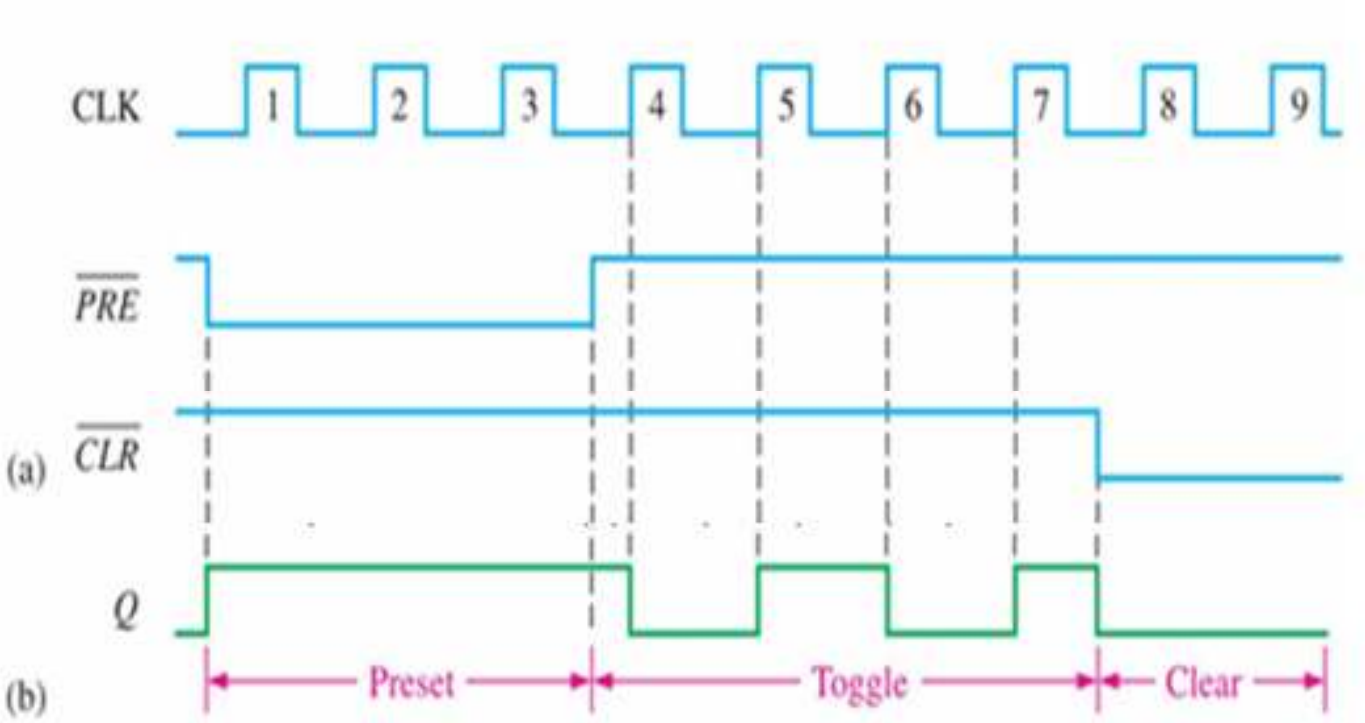
- Most flip-flops have other inputs that are *asynchronous*, meaning they affect the output independent of the clock.
- They are labeled as $\overline{PRE}$ (preset) and $\overline{CLR}$ (clear).
- An active level on preset input will set the flip-flop, and an active level on clear input will reset it.
- In normal condition, preset and clear would not be LOW at the same time. But must be kept HIGH for synchronous operation

Example

Determine the Q output shown in the timing diagram if Q is initially LOW.

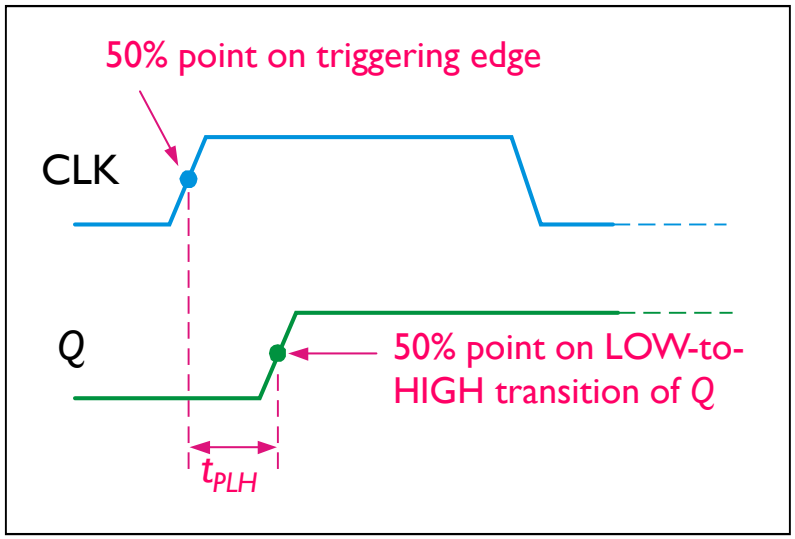
Solution





Flip-flop Operating Characterictic

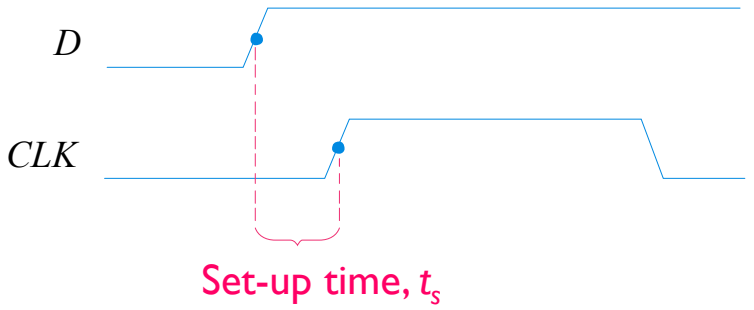
Propagation delay time is specified for the rising and falling outputs. It is measured between the 50% level of the clock to the 50% level of the output transition.



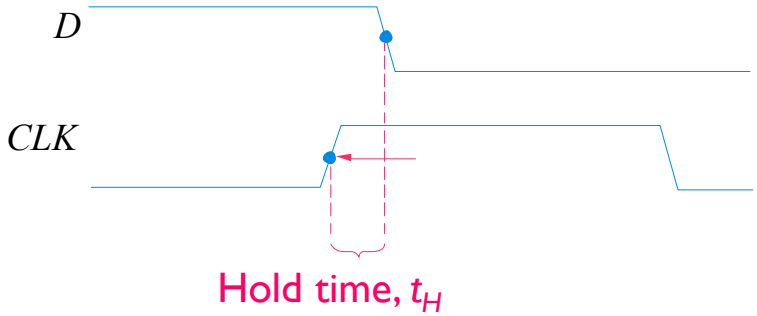
The typical propagation delay time for the 74AHC family (CMOS) is 4 ns. Even faster logic is available for specialized applications.

Set-up time and **hold time** are times required before and after the clock transition that data must be present to be reliably clocked into the flip-flop.

Setup time is the minimum time for the data to be present *before* the clock.



Hold time is the minimum time for the data to *remain* after the clock.



Maximum clock frequency, f(max), highest rate at which a flip-flop can be reliably triggered. Above that the flip-flop will be unable to respond quickly.

Assignment

- Examples of application of flip-flops are as follow:
  - Parallel Data Storage.
  - Frequency Division.
  - Counting.
- Discuss all the above applications by showing its logic circuit and timing diagram.
- Create a problem to show its application.
- Due date: 5th May 2014

THE END OF PART III