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 # Module : RISCV Arch Test
 # Section: RISCV Arch Test
 # Task Name: Task 4

Test Description:

This test verifies the correct behavior of the **mstatus.FS** (Floating-Point Status) field and the **mstatus.SD** (State Dirty) bit in Machine mode of the RISC-V privileged architecture specification. The purpose of the test is to confirm that the processor correctly implements the defined states of the FS field — OFF (00), INITIAL (01), CLEAN (10), and DIRTY (11) — and that the summary dirty bit (SD, bit 31 of mstatus) reflects the correct state when the floating-point unit (FPU) becomes dirty.

Output Explanation:

At the beginning of execution, it starts in Machine mode with FS=OFF (default reset state). It then executes a floating-point instruction (fmv.w.x) while FS is OFF. According to the RISC-V privileged specification, this must generate an illegal instruction exception, because floating-point instructions are disabled when FS=00.

```
core   0: 0x80002014 (0xfedfd06f) j       pc - 0x2014
core   0: 3 0x80002014 (0xfedfd06f)
core   0: 0x80000000 (0xf0000053) fmv.w.x ft0, zero
core   0: exception trap_illegal_instruction, epc 0x80000000
core   0:           tval 0xf0000053
core   0: >>>>  trap_vector
core   0: 0x80002018 (0x34202f73) csrr    t5, mcause
core   0: 3 0x80002018 (0x34202f73) x30 0x00000002
```

The trap handler captures this exception, increments a signature memory location to record that the trap occurred, and resumes execution. This confirms correct enforcement of the OFF state. Next, the test sets FS=INITIAL (01) by modifying bits [14:13] of mstatus. It then checks the SD bit (bit 31) and verifies that it remains 0, since INITIAL does not indicate a dirty floating-point state.

```
core   0: 0x80000004 (0x000022b7) lui     t0, 0x2
core   0: 3 0x80000004 (0x000022b7) x5  0x00002000
core   0: 0x80000008 (0x3002a073) csrs    mstatus, t0
core   0: 3 0x80000008 (0x3002a073) c768_mstatus 0x00002080
core   0: 0x8000000c (0x30002373) csrr    t1, mstatus
core   0: 3 0x8000000c (0x30002373) x6  0x00002080
core   0: 0x80000010 (0x01f35393) srli    t2, t1, 31
core   0: 3 0x80000010 (0x01f35393) x7  0x00000000
core   0: 0x80000014 (0x06039663) bnez    t2, pc + 108
```

The test then explicitly sets FS=CLEAN (10) and again verifies that SD=0, ensuring that the summary dirty bit is not set when the floating-point state is clean.

```
core   0: 0x8000002c (0x00536333) or      t1, t1, t0
core   0: 3 0x8000002c (0x00536333) x6  0x00004080
core   0: 0x80000030 (0x30031073) csrw    mstatus, t1
core   0: 3 0x80000030 (0x30031073) c768_mstatus 0x00004080
core   0: 0x80000034 (0x300023f3) csrr    t2, mstatus
core   0: 3 0x80000034 (0x300023f3) x7  0x00004080
core   0: 0x80000038 (0x01f3d393) srli    t2, t2, 31
core   0: 3 0x80000038 (0x01f3d393) x7  0x00000000
core   0: 0x8000003c (0x04039263) bnez    t2, pc + 68
```

Finally, the test executes a floating-point instruction while FS is enabled. This should automatically transition the FS field to DIRTY (11). The test reads back mstatus, verifies that FS=11, and confirms that the SD bit is now 1, demonstrating that SD correctly reflects the dirty floating-point state.

```
79   core   0: 0x80000040 (0xf00000d3) fmv.w.x ft1, zero
80   core   0: 3 0x80000040 (0xf00000d3) f1  0xffffffff00000000 c768_mstatus 0x80006080
81   core   0: 0x80000044 (0x30002373) csrr    t1, mstatus
82   core   0: 3 0x80000044 (0x30002373) x6  0x80006080
83   core   0: 0x80000048 (0x01f35393) srli    t2, t1, 31
84   core   0: 3 0x80000048 (0x01f35393) x7  0x00000001
85   core   0: 0x8000004c (0x02038a63) beqz    t2, pc + 52
```

On any unexpected behavior (wrong FS value, incorrect SD state, or missing exception), it branches to fail and writes a failure pattern (0xcafebeef) to tohost.

On success, it writes 1 to tohost.

Reference:

Extension Context Status in mstatus Register: RISCV Privileged Architecture v1.12, 3.1.6.6