**Aleena Raza(0155)**

**Assignment # 3**

Consider the MIPS processor you have studied in the class, you are required to modify the MIPS Architecture to support 1K Byte of Cache and answer the following questions.

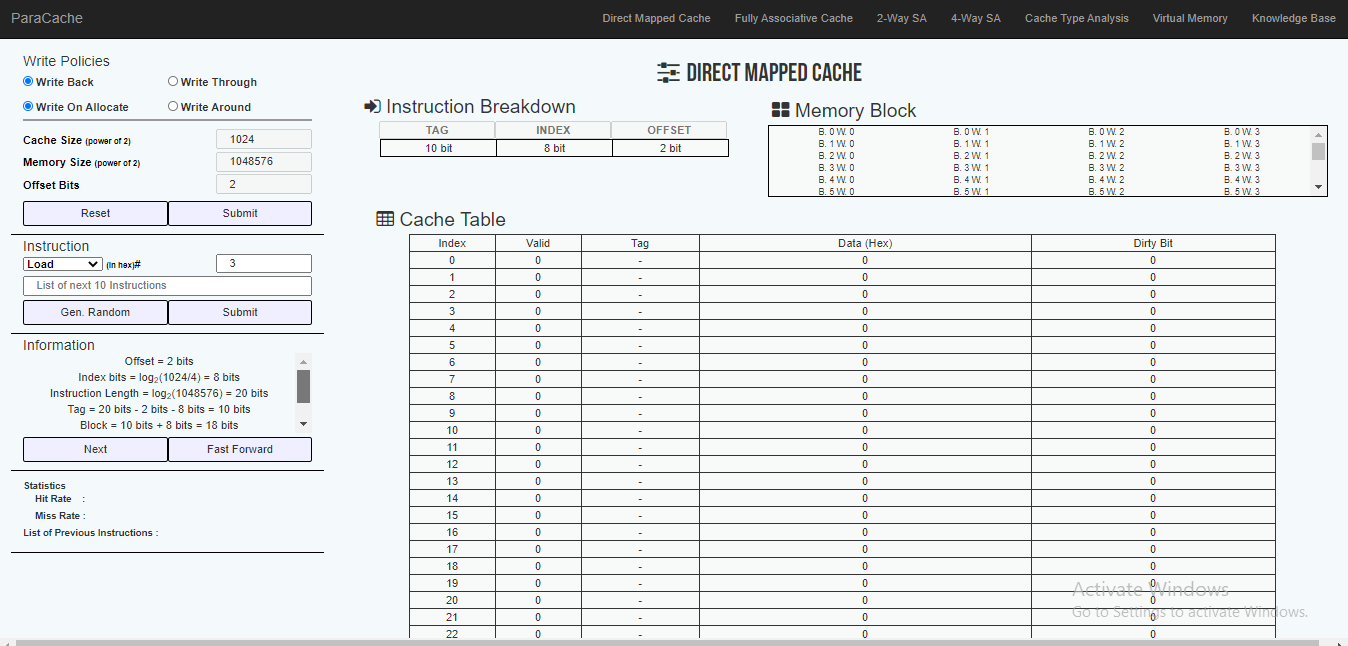
1. Draw the **Direct cache Mapping** diagram showing the Cache Main Memory and MPIS Processor. Also specify the bits for direct mapping.

Solution:

* Mips = 32 bits Architecture
* Main Memory = 1 MB = 2^0 \* 2^20 bytes = 2^20 bytes
* Cache = 1 KB == 2^0 \* 2^10 bytes = 2^10 bytes
* Offset = 32 = (32/8) = 4 = 2^2 = 2 bits
* Index = 8 bits
* Tag =(20-8-2) = 10 bits

After Alignment the cache bit:

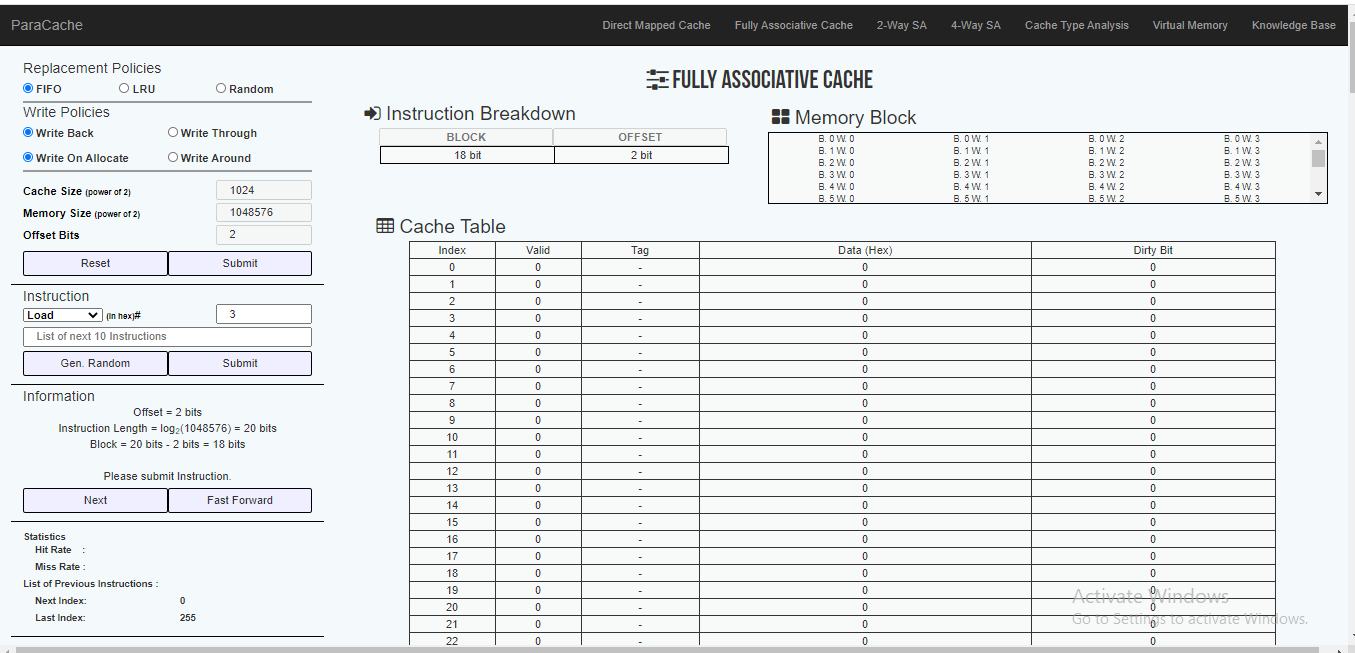
* Index = 8 bits
* Tag =(20-8-2) = 10 bits



1. Draw the **fully associative cache Mapping** diagram showing the Cache Main Memory and MPIS Processor. Also specify the bits for fully associative cache mapping.

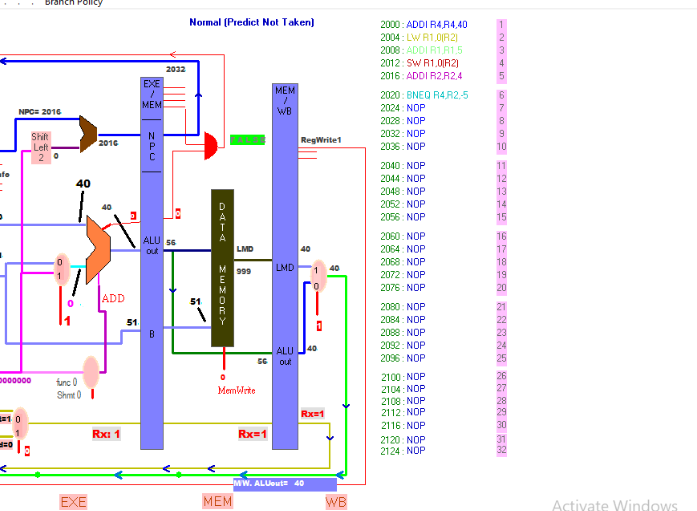
Solution:

* Mips = 32 bits Architecture
* Main Memory = 1 MB = 2^0 \* 2^20 bytes = 2^20 bytes
* Cache = 1 KB == 2^0 \* 2^10 bytes = 2^10 bytes
* Offset = 32 = (32/8) = 4 = 2^2 = 2 bits

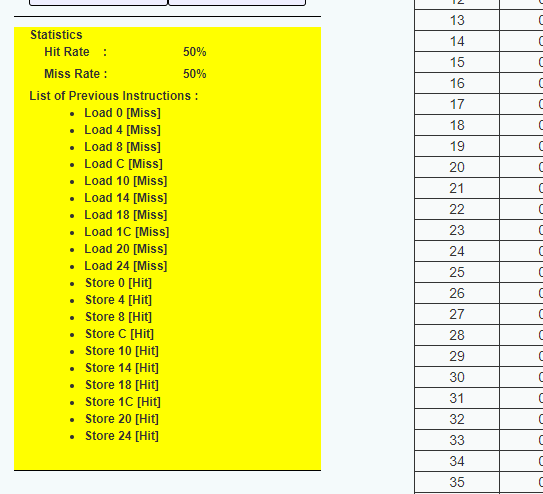


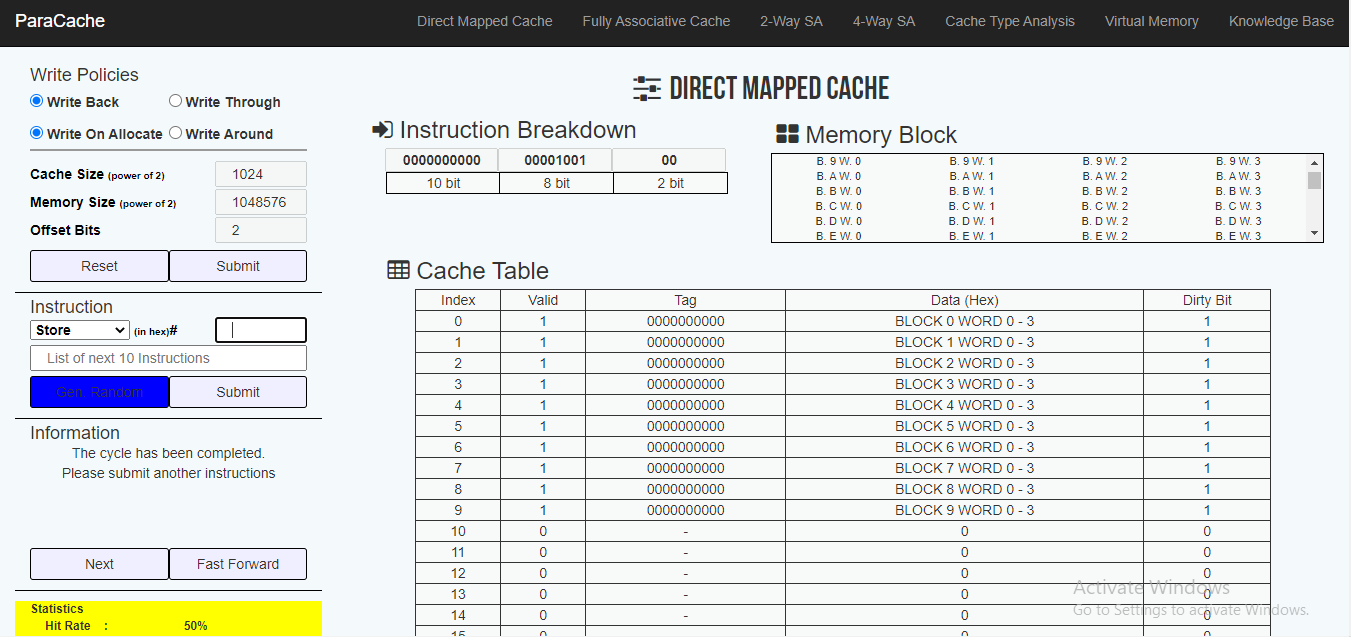
1. **Write a program that reads the value of 10 elements from the data memory, then add 5 to each element and store them back to data memory. For this program which mapping scheme is best Direct Mapping or the fully associative mapping. Hint: count the number of hits.**

Mips



### Direct Mapped Cache





Fully Associative Cache

