Muhammed Çelik

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Professional Experience

Procenne **July 2022 – August 2022**

Digital Design Intern *İstanbul, TR*

- Worked on Secure Memory Project.
- Implemented AES ciphering algorithm in Verilog.
- Integrated AES design into SRAM Controller module to cipher plain-text data and store.
- Synthesized and implemented the top module design via OpenLane Flow.

Pavelsis **June 2022 – July 2022**

Digital Design Intern *İstanbul, TR*

- Worked on MAX1363 ADC IC Hardware Driver Project.
- Studied datasheet of MAX1363 to configure and operate properly.
- Developed I2C Controller in VHDL to communicate and transmit digital signals from the ADC to FPGA.
- Tested the design on the FPGA and verified correct functionality of the driver.

Yongatek Microelectronics **November 2021 – June 2022**

Digital Design Intern *İstanbul, TR*

- Worked on Turbo Encoder Project and translated the design into Verilog HDL.
- Utilized OpenLane Flow to generate GDSII file for Turbo Encoder Design.
- Worked on 5G New Radio LDPC Encoder project. Proposed a top level schematic and implemented the design in VHDL.
- Verified the LDPC Encoder design via VHDL testbench.

Education

Bogazici University **September 2018 –**

Senior Electrical and Electronics Engineering student *İstanbul, TR*

- Current GPA: 3.19/4.00
- Member, BUEC IEEE Student Branch (2019-2020)
- Member, UAV-IN Unmanned Aerial Vehicle Team (2019-2020)
- MSMB, Mimar Sinan Engineering Society

Projects

UART Transmitter & Receiver Module | *VHDL, Xilinx Vivado, XSim* **September 2021**

- The project involves digital design of both transmitter and receiver components of UART communication protocol.
- The data to be transmitted is set as 1 byte.
- Clock frequency, baudrate and stop bit number are set as generic to implement the modules for various setups.
- The design is verified by Vivado testbench simulations.

Prime Number Detector | *VHDL, Xilinx ISE, ISim* **June 2021**

- Digital Systems Design project aims to find first 256 prime numbers and display them on a VGA monitor consecutively.
- In order to detect prime numbers among the other integers, Sieve of Eratosthenes algorithm is used with sufficient number of prime counters.
- After detection of the primes, numbers are converted into BCD format to be displayed on the screen.
- Using VGA interface of Xilinx Spartan FPGA, prime numbers are printed on the screen one by one.

Computing Eigenvalues and Eigenvectors | *C++* **April 2021**

- Aim of the project is implementing the normalized power iteration algorithm together with deflation to find two eigenvalues and corresponding eigenvector for the dominant eigenvalue of a given matrix A, where A is a square matrix.
- The program takes three command line arguments for the parameters: Name of the file which includes matrix A, tolerance and name of the output file.
- To implement Object Oriented Programming, matrix class is defined. Entries of matrices are stored in dynamic 2-d vector variable.
- Matrix operations such as addition, multiplication, transpose are defined as class methods.

Skills

Languages: Turkish (Native), English (Advanced)
Programming: C/C++, Python, VHDL, Verilog HDL, MATLAB
Technology/Tools: GNU/Linux, Microsoft Office, Xilinx Vivado/ISE, QuestaSim, Caravel OpenLane, LTSpice, Simulink