

Muhammed Evgin 110510163

Video link:

https://drive.google.com/file/d/1lQuPTYrXtjQWr8uHLeUx1Rn4SGBHf9ZW/view?usp=share_link

Simulating Matrix Multiplication Application in gem5 Simulator

In this homework, I work on gem5 simulation for calculating hit rate for different cache line sizes. These are the subtitles I am going to explain.

Which files in the simulator you mainly changed?

I mainly changed two files in the simulator those are 'simple.py' and 'caches.py'. When I said changed, I want to mention that those files are exist as default, but I made some changes.

What is the main code you added into the simulator (not all the lines, just your main change is enough)?

In cache.py:

I just changed 'size = 64KB' for both instruction cache and data cache. We don't need to change those lines. We can set size value when we build the simulation from terminal by just adding '--l1d_size=64kB --l1i_size=64kB'.

In simple.py:

```
from caches import * // importing caches script
system.cpu.icache = L1ICache() // creation of L1 instruction and data cache
system.cpu.dcache = L1DCache()
system.cache_line_size = 128 //changing cache line size
system.cpu.icache.connectCPU(system.cpu) // connections to the CPU
system.cpu.dcache.connectCPU(system.cpu)
system.cpu.icache.connectBus(system.membus) // connections to system bus
system.cpu.dcache.connectBus(system.membus)
"tests/test-progs/mm/MatrixMultiplication" // changed path.
```

Table showing the L1 hit rate for different block sizes for the L1 data cache.

	2	4	8	16	32	64	128
Hit rate	No output	No output	0.997201	0.998498	0.999177	0.99954	0.999737

We can see that when we increase block size, we get better hit rate.

Graph showing the changes in the hit rate according to the block size for L1 data cache.

