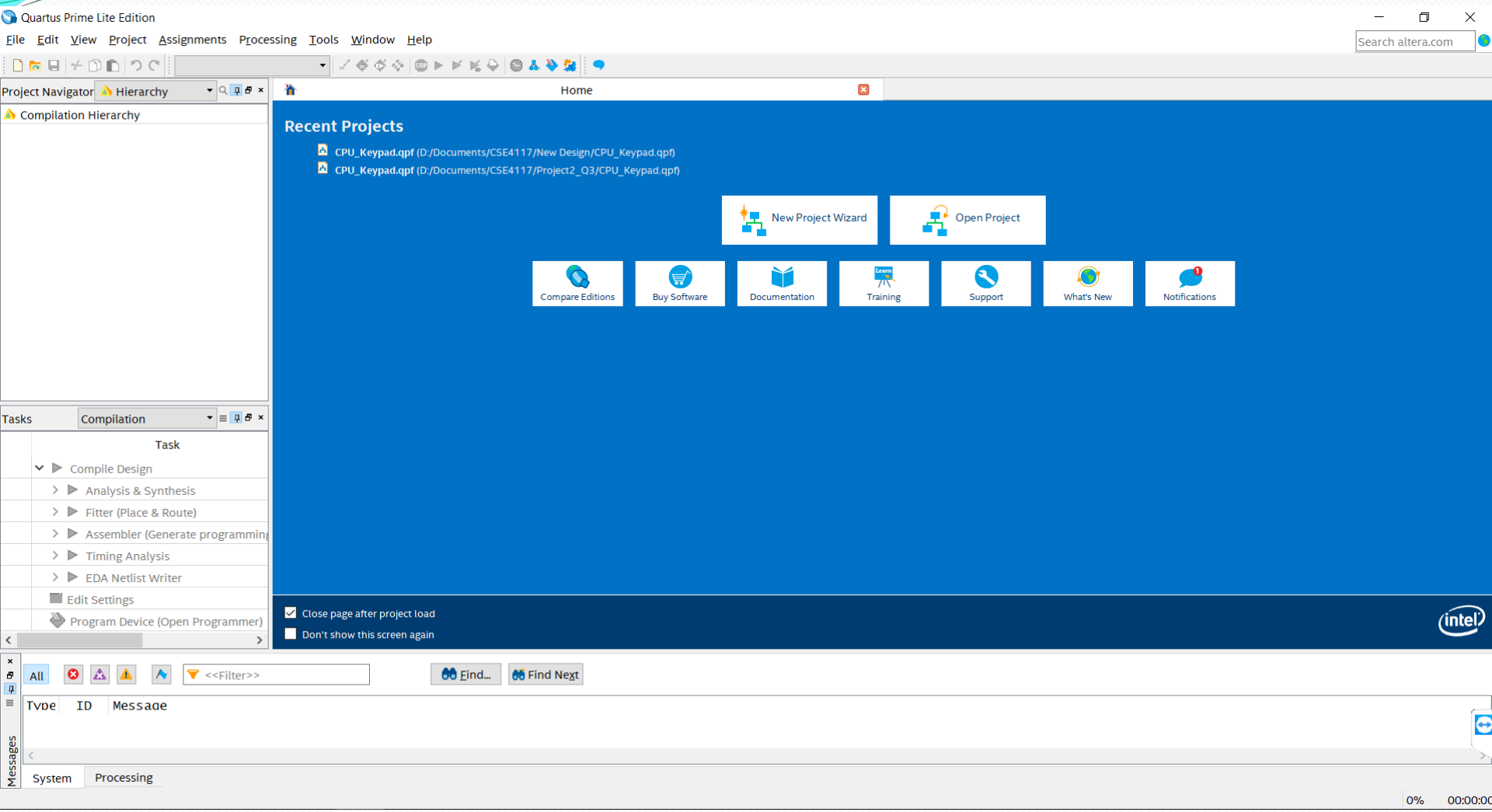
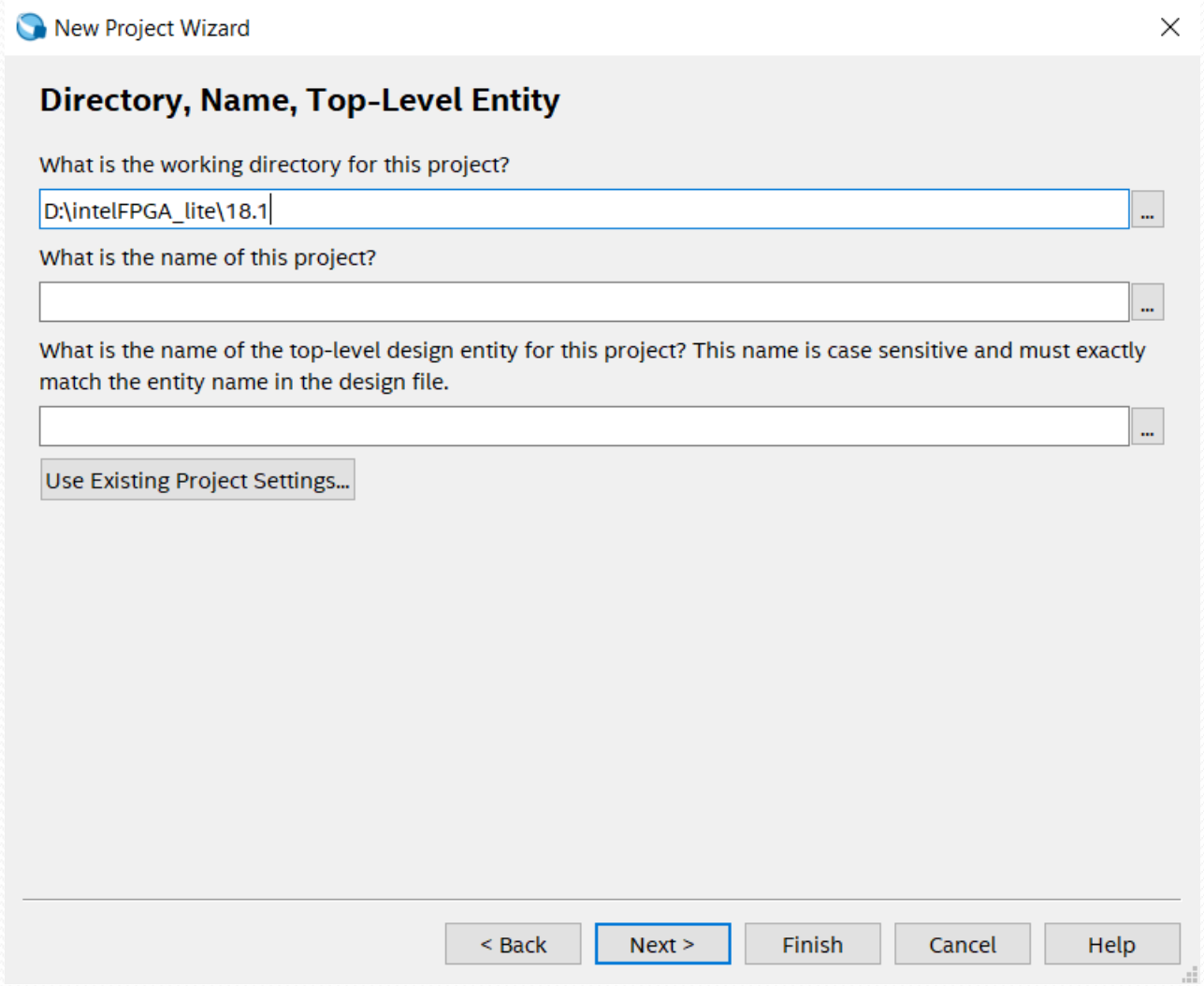
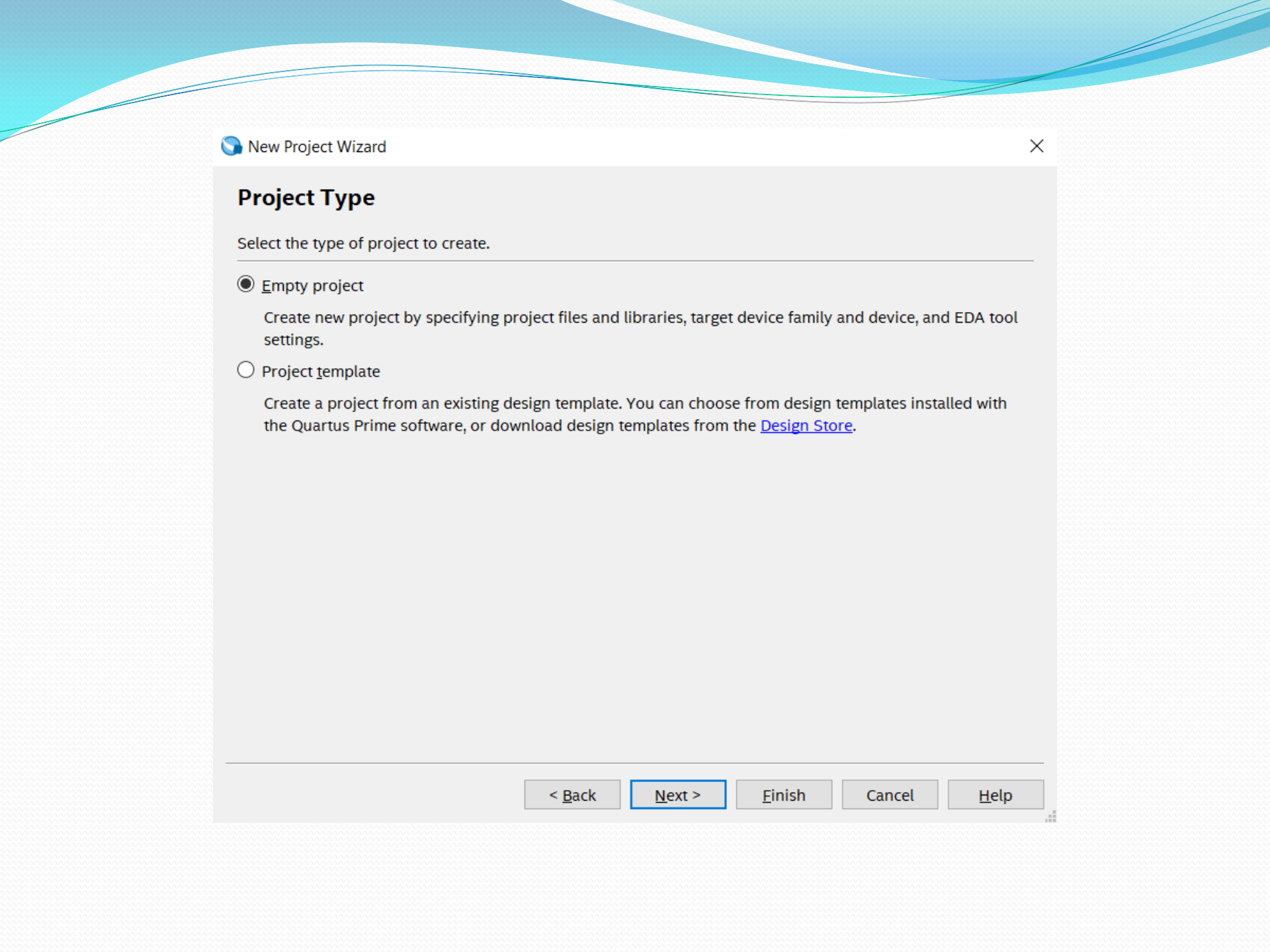
First Project Example For FPGA With Quartus


Quartus Prime Lite Edition
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Project Navigator Hierarchy
Compilation Hierarchy
Home
Recent Projects
CPU_Keypad.qpf (D:/Documents/CSE4117/New Design/CPU_Keypad.qpf)
CPU_Keypad.qpf (D:/Documents/CSE4117/Project2_Q3/CPU_Keypad.qpf)
New Project Wizard
Open Project
Compare Editions
Buy Software
Documentation
Training
Support
What's New
Notifications
Close page after project load
Don't show this screen again
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
0%
00:00:00


New Project Wizard
Directory, Name, Top-Level Entity
What is the working directory for this project?
D:\intelFPGA_lite\18.1
...
What is the name of this project?
...
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
...
Use Existing Project Settings...
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Project Type
Select the type of project to create.
Empty project
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.
Project template
Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the Design Store.
< Back
Next >
Finish
Cancel
Help

New Project Wizard

Family, Device & Board Settings

Device | Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the Device Support List webpage.

Device family

Family: Cyclone IV E

Device: All

Target device

- Auto device selected by the Fitter
- Specific device selected in 'Available devices' list
- Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

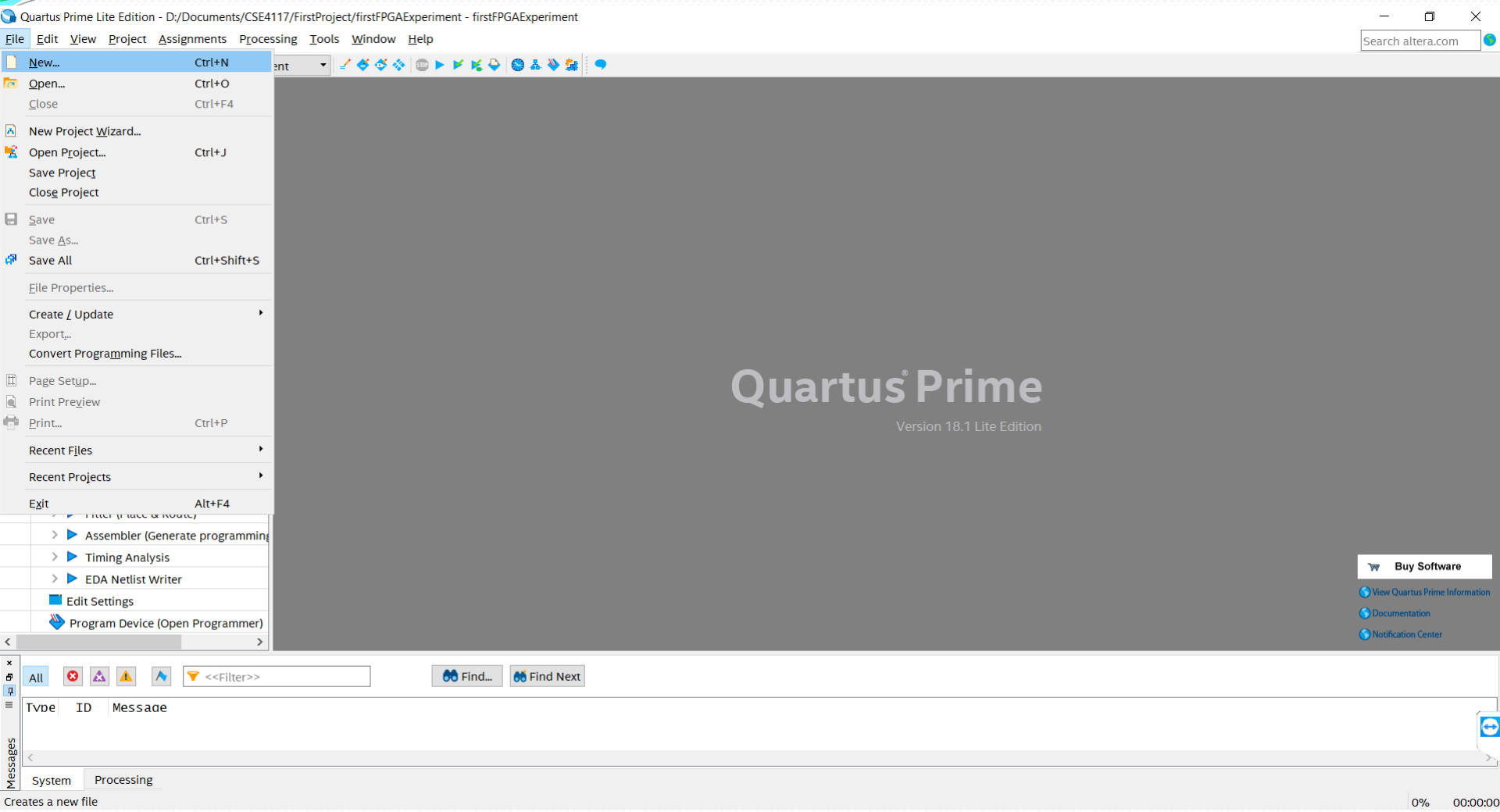
Name filter:

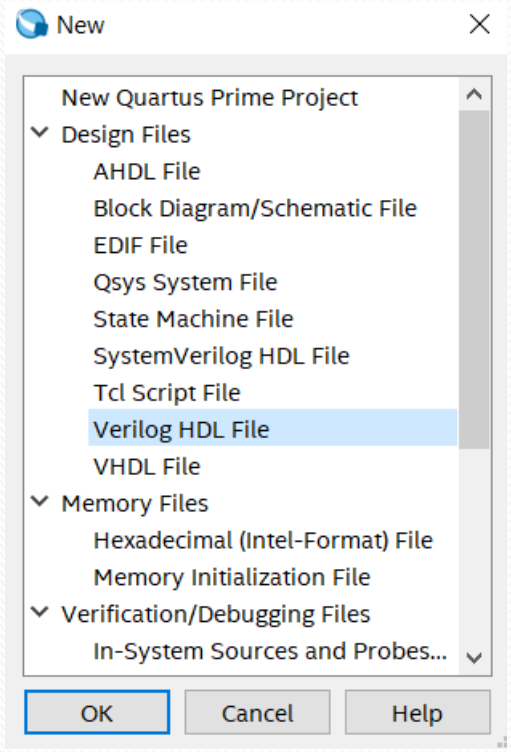
Show advanced devices

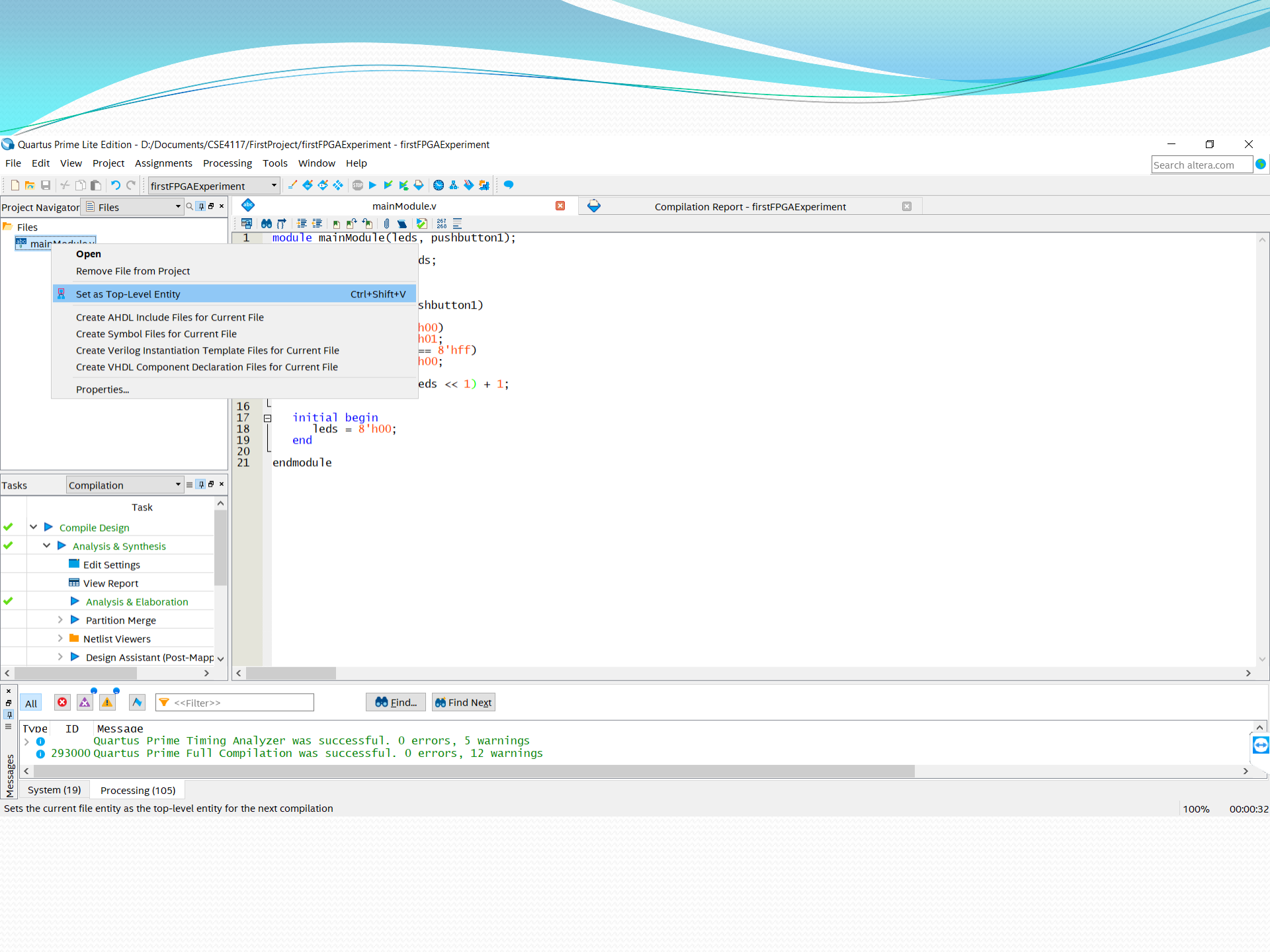
Available devices:

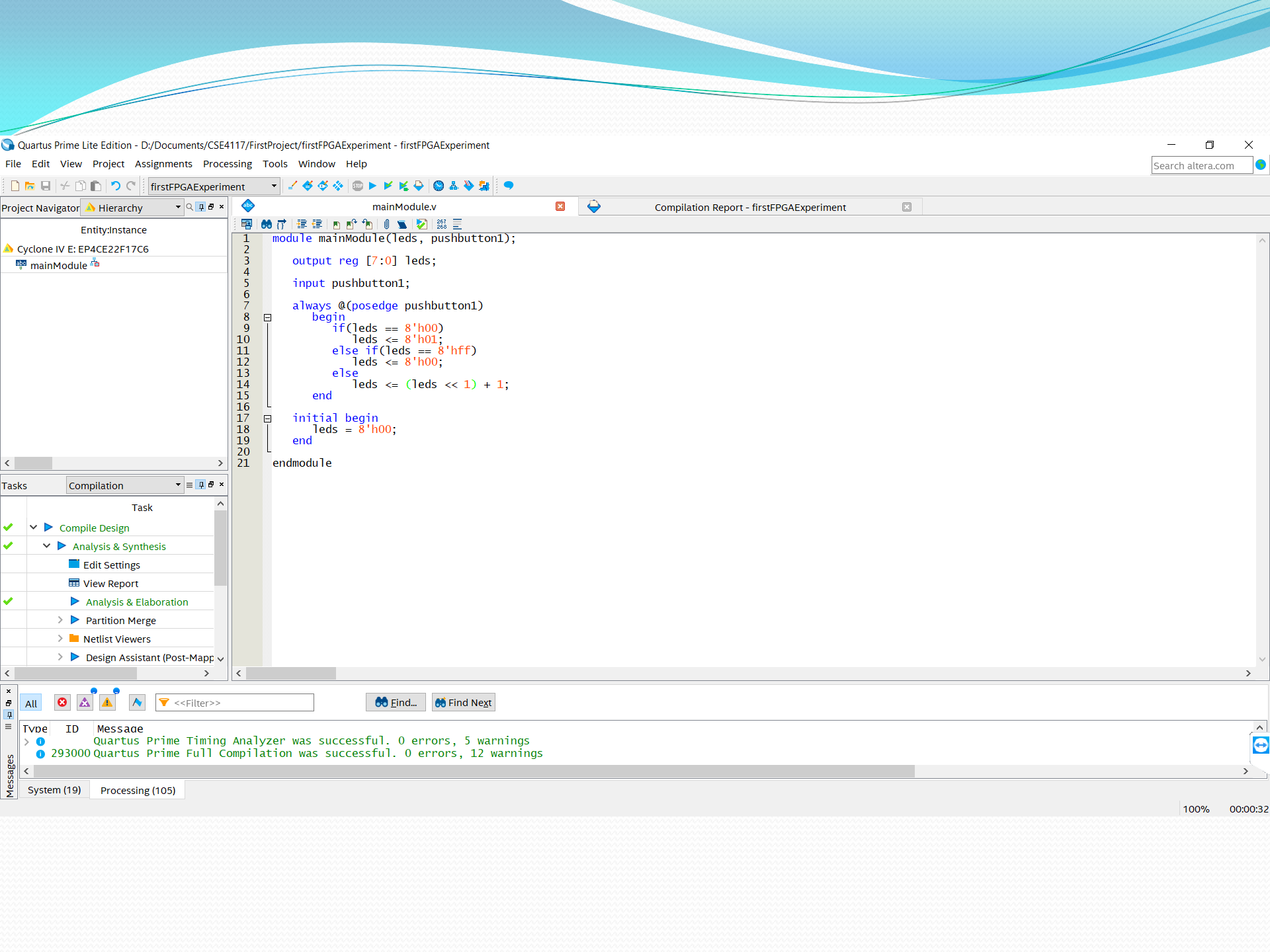
Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit elements	PLLs	Global Clocks
EP4CE22E22C8	1.2V	22320	80	80	608256	132	4	20
EP4CE22E22C8L	1.0V	22320	80	80	608256	132	4	20
EP4CE22E22C9L	1.0V	22320	80	80	608256	132	4	20
EP4CE22E22I7	1.2V	22320	80	80	608256	132	4	20
EP4CE22E22I8L	1.0V	22320	80	80	608256	132	4	20
EP4CE22F17A7	1.2V	22320	154	154	608256	132	4	20
EP4CE22F17C6	1.2V	22320	154	154	608256	132	4	20
EP4CE22F17C7	1.2V	22320	154	154	608256	132	4	20
EP4CE22F17C8	1.2V	22320	154	154	608256	132	4	20
EP4CE22F17C8L	1.0V	22320	154	154	608256	132	4	20
EP4CE22F17C9L	1.0V	22320	154	154	608256	132	4	20
EP4CE22F17I7	1.2V	22320	154	154	608256	132	4	20

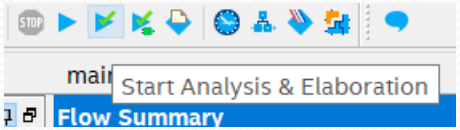
< Back | Next > | Finish | Cancel | Help

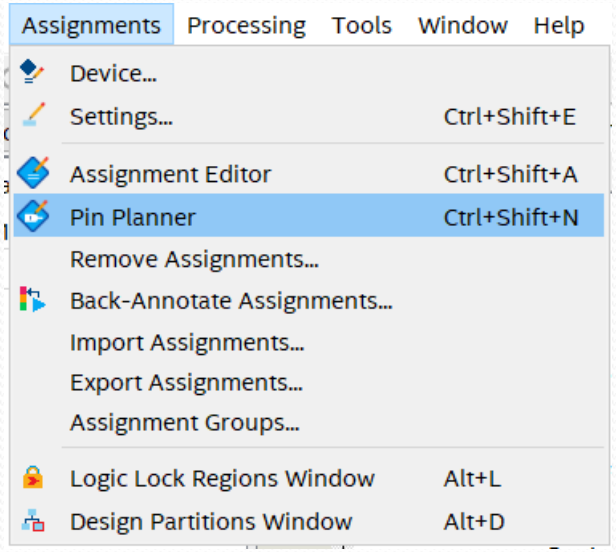

Quartus Prime Lite Edition - D:/Documents/CSE4117/FirstProject/firstFPGAExperiment - firstFPGAExperiment
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
Assembler (Generate programming
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
Quartus Prime
Version 18.1 Lite Edition
Buy Software
View Quartus Prime Information
Documentation
Notification Center
All
<<Filter>>
Find...
Find Next
Type ID Message
Messages
System
Processing
Creates a new file
0%
00:00:00


New
New Quartus Prime Project
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
Qsys System File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes...
OK
Cancel
Help


Quartus Prime Lite Edition - D:/Documents/CSE4117/FirstProject/firstFPGAExperiment - firstFPGAExperiment
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
firstFPGAExperiment
Project Navigator Files
Files
mainModule.v
Compilation Report - firstFPGAExperiment
Open
Remove File from Project
Set as Top-Level Entity Ctrl+Shift+V
Create AHDL Include Files for Current File
Create Symbol Files for Current File
Create Verilog Instantiation Template Files for Current File
Create VHDL Component Declaration Files for Current File
Properties...
1 module mainModule(leds, pushbutton1);
16
17 initial begin
18 leds = 8'h00;
19 end
20
21 endmodule
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
Design Assistant (Post-Mapp
All
<<Filter>>
Find...
Find Next
Type ID Message
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System (19)
Processing (105)
Sets the current file entity as the top-level entity for the next compilation
100%
00:00:32

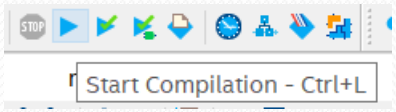

Quartus Prime Lite Edition - D:/Documents/CSE4117/FirstProject/firstFPGAExperiment - firstFPGAExperiment
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
firstFPGAExperiment
Project Navigator Hierarchy
Entity:Instance
Cyclone IV E: EP4CE22F17C6
mainModule
mainModule.v
Compilation Report - firstFPGAExperiment
1 module mainModule(leds, pushbutton1);
2
3 output reg [7:0] leds;
4
5 input pushbutton1;
6
7 always @(posedge pushbutton1)
8 begin
9 if(leds == 8'h00)
10 leds <= 8'h01;
11 else if(leds == 8'hff)
12 leds <= 8'h00;
13 else
14 leds <= (leds << 1) + 1;
15 end
16
17 initial begin
18 leds = 8'h00;
19 end
20
21 endmodule
Tasks Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
Design Assistant (Post-Mapp
All
<<Filter>>
Find...
Find Next
Type ID Message
Quartus Prime Timing Analyzer was successful. 0 errors, 5 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 12 warnings
Messages
System (19)
Processing (105)
100%
00:00:32


Start Analysis & Elaboration
Flow Summary

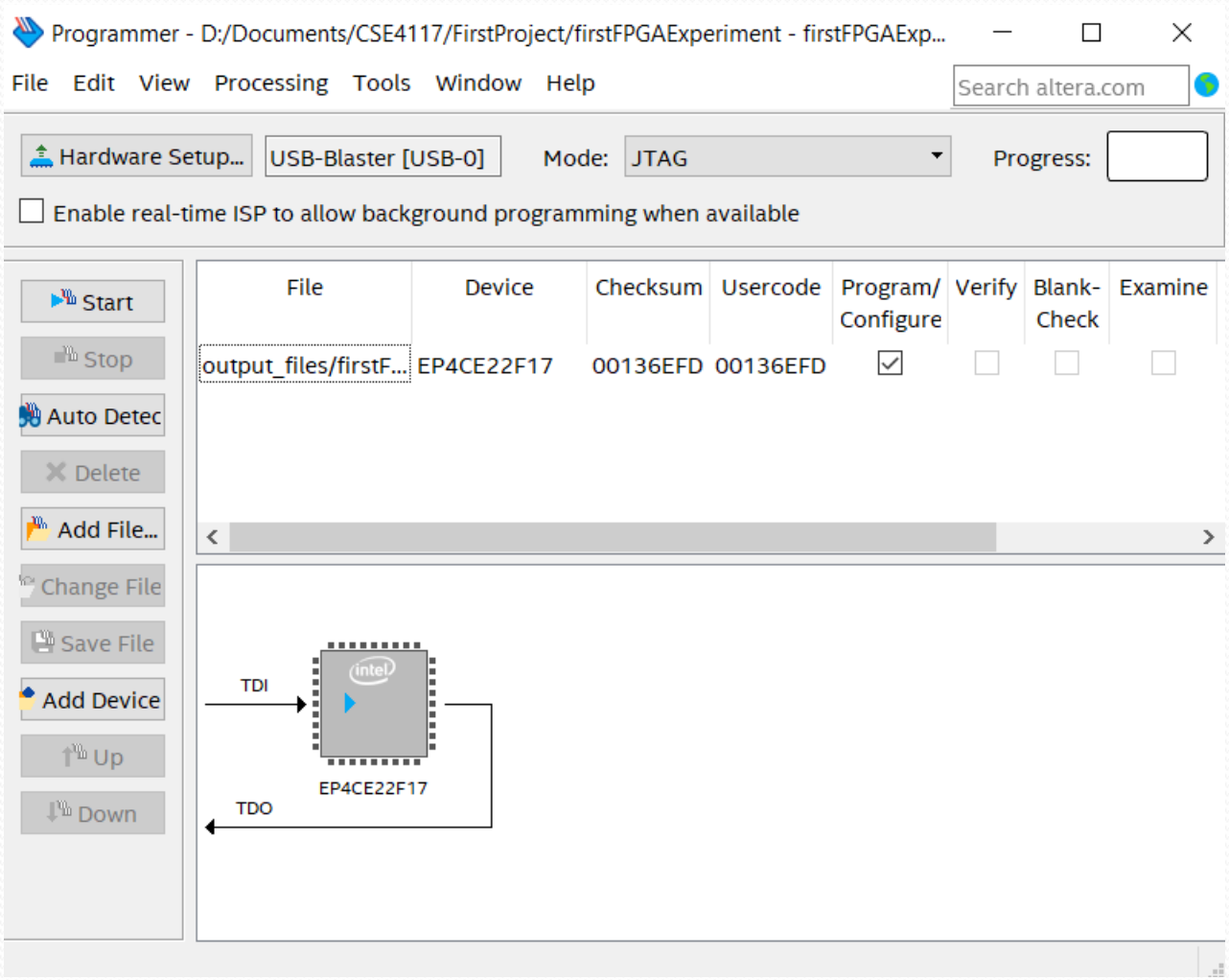

Assignments
Processing
Tools
Window
Help
Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
Logic Lock Regions Window Alt+L
Design Partitions Window Alt+D

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	urrent Streng	Slew Rate	ifferential Pai	ict Preservati
leds[7]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[6]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[5]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[4]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[3]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[2]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[1]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
leds[0]	Output				2.5 V ...fault)		8mA (default)	2 (default)		
pushbutton1	Input				2.5 V ...fault)		8mA (default)			
<<new node>>										

leds[7]	Output	PIN_L3	2	B2_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[6]	Output	PIN_B1	1	B1_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[5]	Output	PIN_F3	1	B1_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[4]	Output	PIN_D1	1	B1_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[3]	Output	PIN_A11	7	B7_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[2]	Output	PIN_B13	7	B7_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[1]	Output	PIN_a13	7	B7_N0	2.5 V ...fault)		8mA (default)	2 (default)
leds[0]	Output	PIN_A15	7	B7_N0	2.5 V ...fault)		8mA (default)	2 (default)
pushbutton1	Input	PIN_J15	5	B5_N0	2.5 V ...fault)		8mA (default)	
<<new node>>								


Start Compilation - Ctrl+L


mainModule.v
Programmer


Programmer - D:/Documents/CSE4117/FirstProject/firstFPGAExperiment - firstFPGAExp...
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming when available
Start
Stop
Auto Detec
Delete
Add File...
Change File
Save File
Add Device
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Examine
output_files/firstF...
EP4CE22F17
00136EFD
00136EFD
TDI
TDO
EP4CE22F17

Necessary Files

- User Manual
  - http://www.ti.com/lit/ug/tidu737/tidu737.pdf