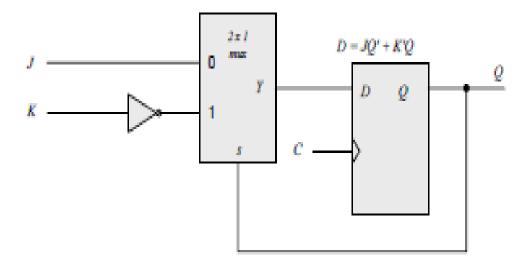
Chapter5-Synchronous Sequential Logic

Lecture8- Problem Solving Session

Fall 2021

5-2: Construct a JK flip-flop using a D flip-flop, a two-to-one line multiplexer, and an inverter

Solution:

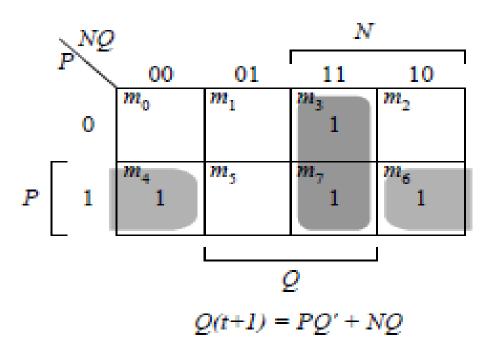


- **5-4:** A PN flip-flop has four operations, clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11 respectively.
- a) Tabulate the characteristic table
- b) Derive the characteristic equation
- c) Tabulate the excitation table
- d) Show how the PN flip-flop can be converted to a D flip-flop

Fall 2021

(a)	P	N	Q(t+1)
	0	0	0
	0	1	Q(t)
	1	0	Q'(t)
	1	1	1

(b)	P	N	Q(t)	Q(t+1)
•	0	0	0	0
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	1
	1	0	1	0
	1	1	0	1
	1	1	1	1



(c)	Q(t)	Q(t+1)	P	N	
	0	0	0	x	
	0	1	1	x	
	1	0	x	0	
	1	1	x	1	

(d) Connect P and N together.

5-8: Derive the state table and the state diagram of the sequential circuit shown in Fig5-8. Explain the function that the circuit performs.

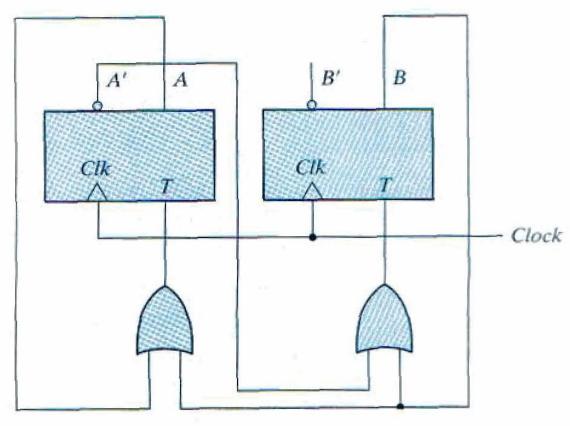


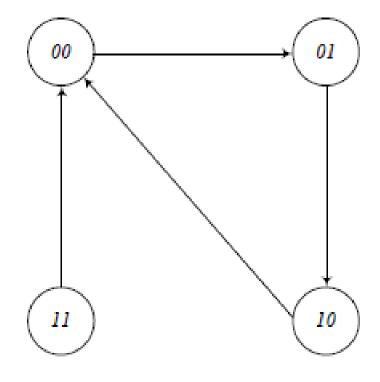
FIGURE P5.8

A counter with a repeated sequence of 00, 01, 10.

Present	state	№ Next	es state	FF Inp T _A	nuts T _B
0	0	0	0	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1
	T_A T_B	=		+ B + B	

Repeated sequence:

$$\rightarrow 00 \rightarrow 01 \rightarrow 10 \rightarrow$$



Problem5-10: A sequential circuit has two JK flip-flops, two inputs x and y, and one output z. The flip-flop input equations and circuit output equations are

$$J_A=Bx+B'x'$$
 $K_A=B'xy'$
 $J_B=A'x$
 $K_B=A+xy'$
 $Z=Ax'y'+Bx'y'$

(b) ν Present Output FFsmduj Next state $\begin{array}{cccc} \textit{Outputs} \\ J_{_A} \ K_{_A} \ J_{_A} \ J_{_B} \end{array}$ x y0 0 0 0

(c) State Equations of A and B

A(t+1)=
$$J_AA' + K_A'A$$

=(Bx+B'y')A'+(B'xy')'A
=A'Bx+A'B'y'+AB+Ax'+Ay
=Bx+A'B'y'+AB+Ax'+Ay
=Bx+A'B'y'+Ax'+Ay
B(t+1)= $J_BB' + K_B'B$
=A'xB'+(A+xy')'B
=A'B'x+A'Bx'+A'By

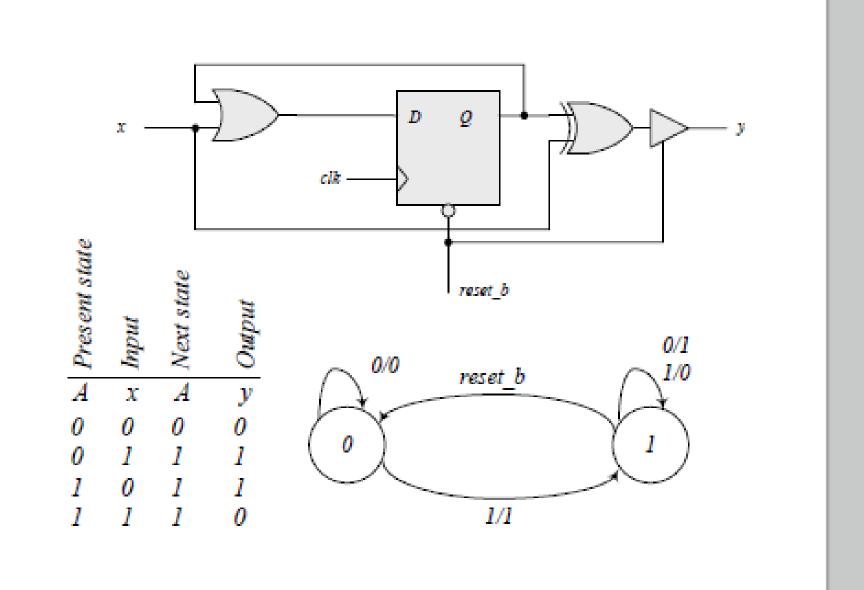
Problem 5-12: Reduce the number of states in the following state table, and tabulate the reduced state table.

	Next State		Output	
Present State	x = 0	x = 1	x = 0	x = 1
а	f	b	0	0
b	d	c	0	0
C	f	e	0	0
d	8	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

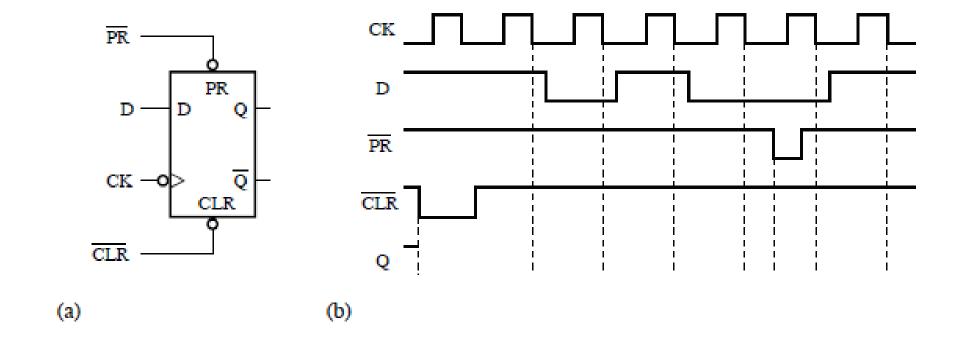
Present	Next state	Output
state	0 1	0 1
а	f b	0 0
Ь	d a	0 0
d	g a	1 0
f	f b	1 1
g	g d	0 1

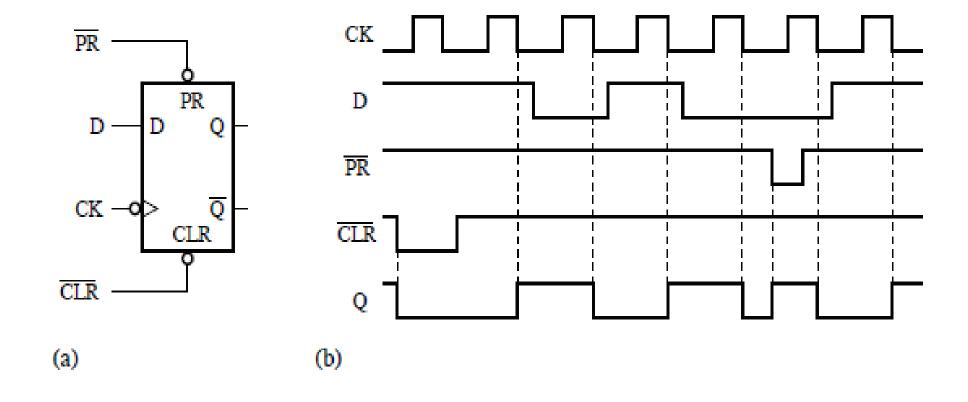
Problem 5-17:

Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation.



Problem: The logic circuit for a D flip-flop with asynchronous inputs is represented in the following Figure (a). Complete the timing diagram in Figure (b).





The End