EE-421: Digital System Design

Doing MATHS on an FPGA

Arithmetic Circuit:
(Revisiting) Adder – Carry Select Adder

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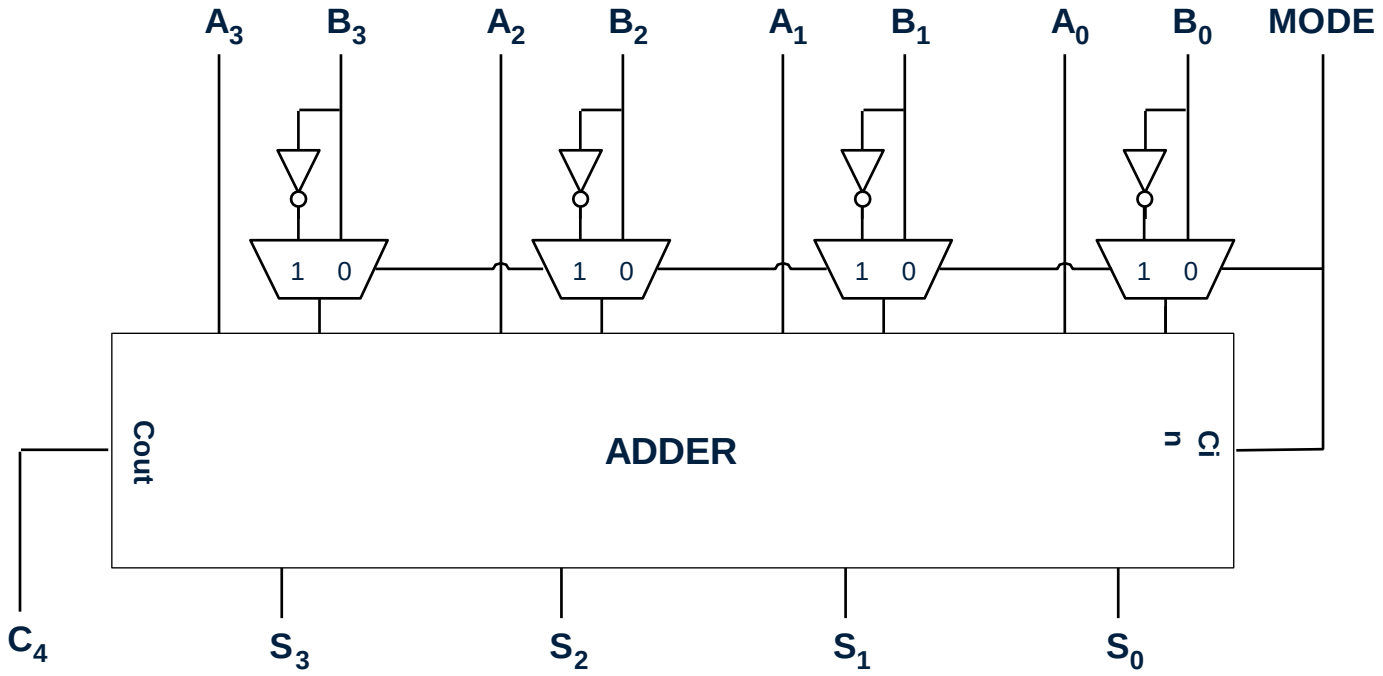
Aside: Combined Adder/Subtractor

$$A - B = A + B` + 1$$



Subtraction: Mode = 1

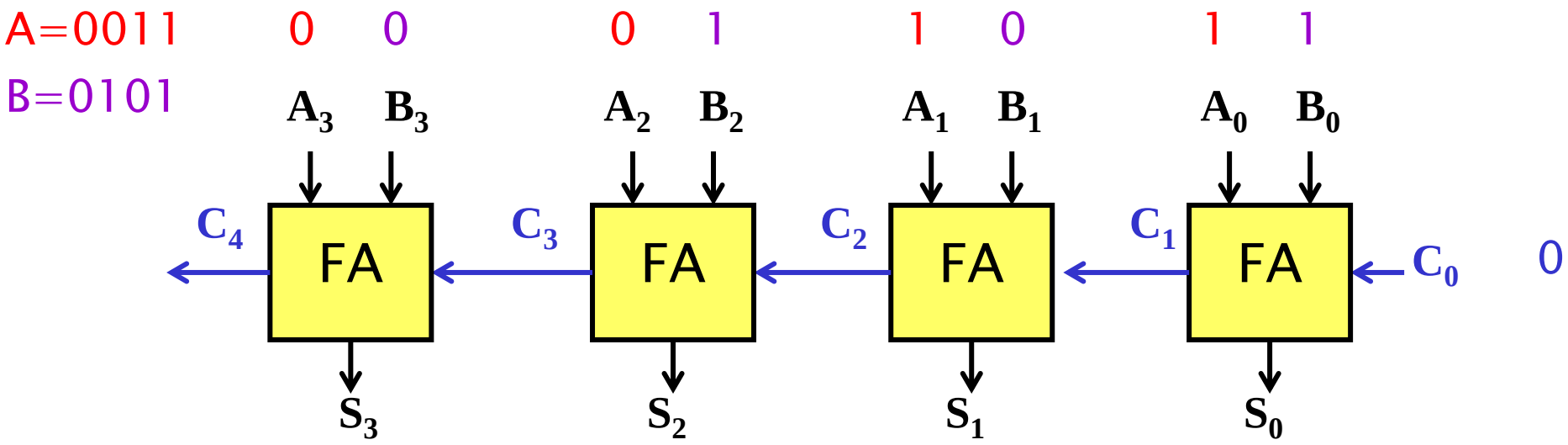
- B inputs are inverted
- Carry-in is 1

Addition: Mode = 0

- B inputs are NOT inverted
- Carry-in is 0

Exercise: How does this affect delay?

Recall: 4-bit Ripple Carry Addition



T=0	0	0		0	0		0	0	S=0000
T=1	0	0		0	1		1	0	S=0110
T=2	0	0		0	1		1	0	S=0100
T=3	0	0		1	0		1	0	S=0000
T=4	0	1		1	0		1	0	S=1000

$$\text{Delay} = 2(N-1)t_{PD} + 3t_{PD}$$

8-bit Ripple Carry Addition

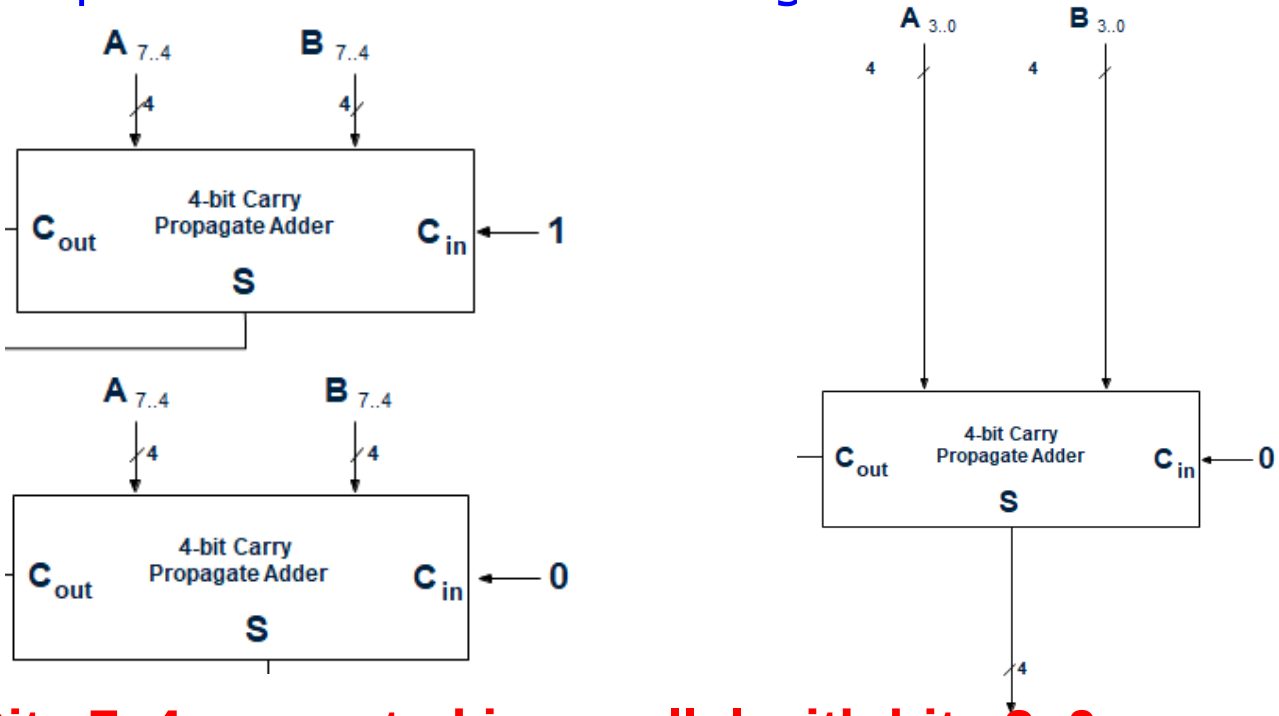
- What's the delay for 8-bit ripple carry addition?

Can we make Fast Adders i.e.
Do something about the Carry Generation?

Carry Select Adder (CSA)

Carry-Select Adder

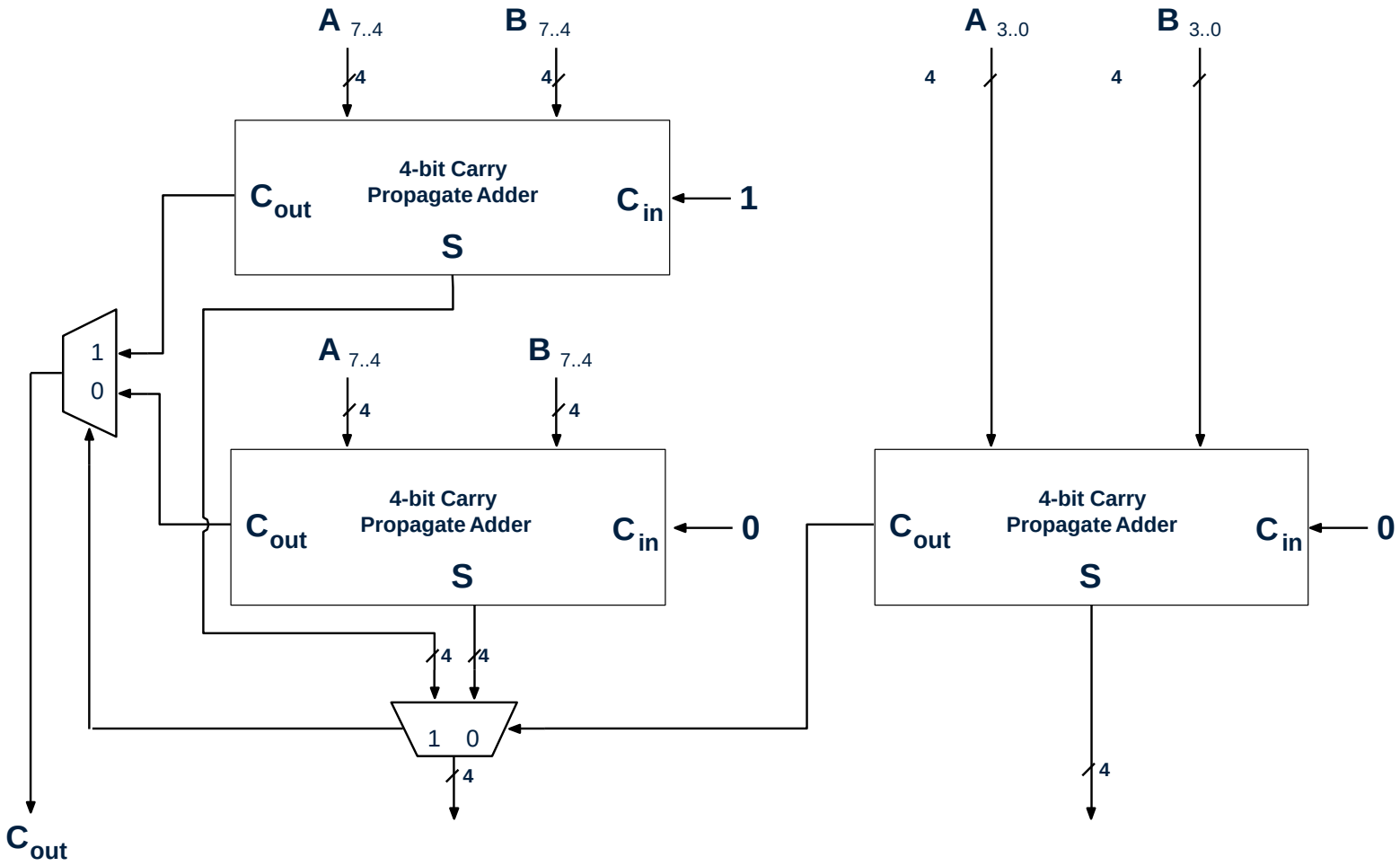
- Basic Idea:
  - Trick for critical paths dependent on late input X
    - Precompute two possible outputs for X = 0, 1
    - Select proper output when X arrives
- Carry-select adder precomputes n-bit sums
  - For both possible carries into n-bit group



Bits 7..4 computed in parallel with bits 3..0

Carry-Select Adder

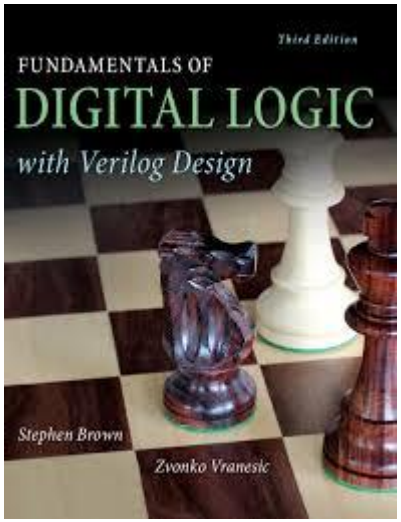
- Then select the correct case when carry-in is ready
  - Trade-off area (use more gates) for faster performance



What's the delay for 8-bit addition using CSA?

Recommended Reading

- Digital System Design with Verilog HDL, 3/e, b **S**tephen Brown and **Z**vonko Vranesic. [**S&Z**]
  - S&Z,
    - Chapter-3
      - 3.2



THANK YOU