EE-421: Digital System Design

Circuit Timing: Path Slack and CAD Tool

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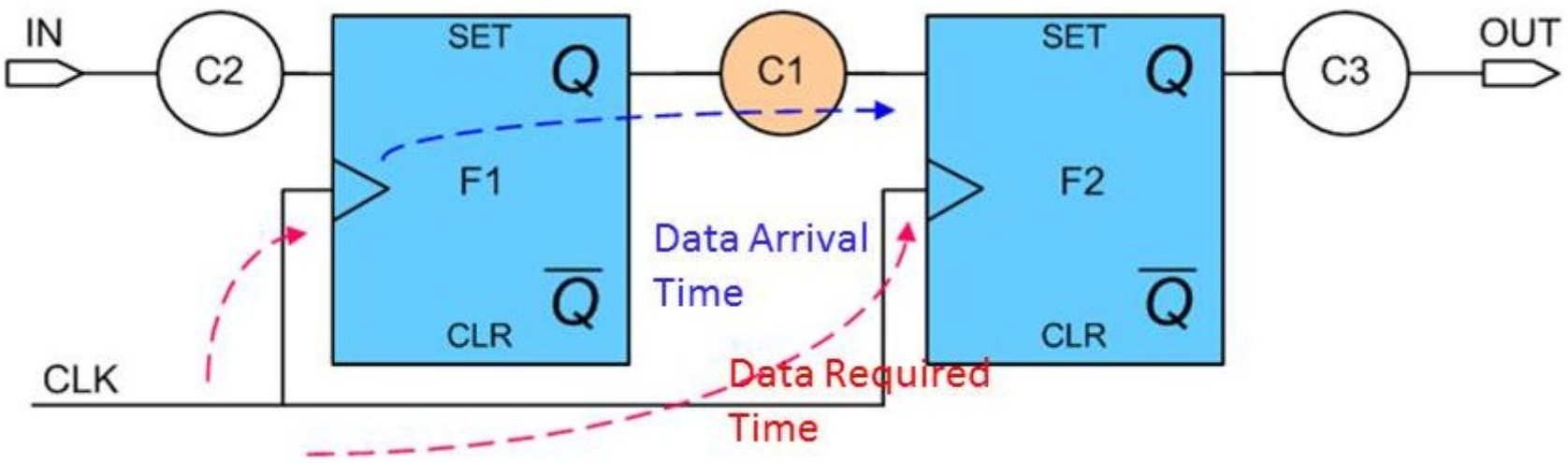
Path Slack

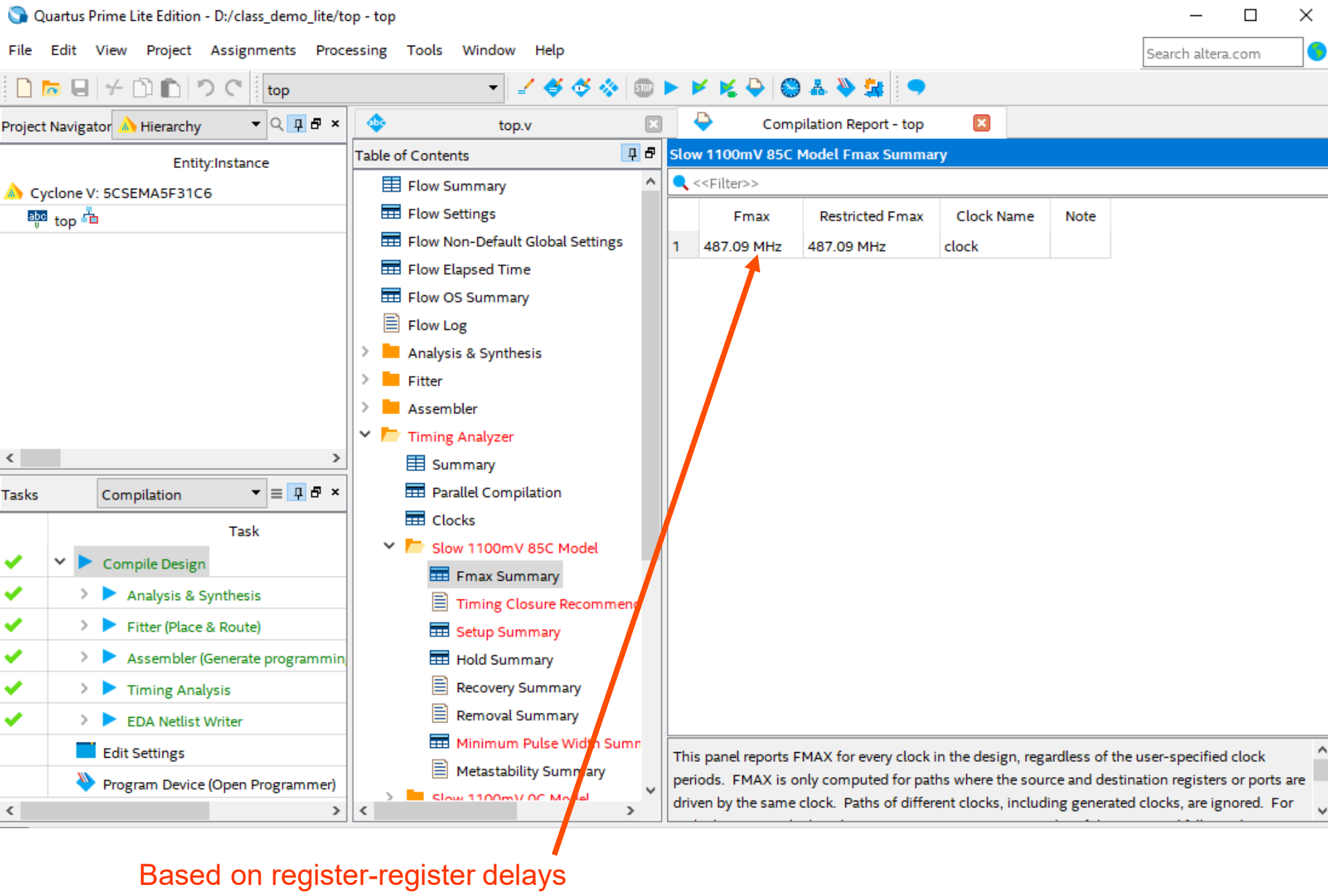
Path Slack



- Slack is defined as difference between actual or achieved time and the desired time for a timing path: [Required Time – Arrival Time]
  - A +ve slack means design is working at the specified frequency and it has some more margins as well.
  - Zero slack specifies design is exactly working at the specified frequency and there is no margin available.
  - -ve slack implies that design doesn't achieve the constrained frequency and timing. Timing Violation!

Slide Credit: http://asic-soc.blogspot.com/2013/08/setup-and-hold-slack.html

What does the CAD Tool do with the Timing?



Based on register-register delays

Quartus can show you the worst-case timing paths:

Slow 1100mV 85C Model

Command Info | Summary of Paths

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-1.053	reg_C[5]	reg_sum[8]	clock	clock	1.000	-0.064	1.819
2	-1.035	reg_B[3]	reg_sum[8]	clock	clock	1.000	-0.066	1.799
3	-1.009	reg_C[1]	reg_sum[8]	clock	clock	1.000	-0.072	1.767
4	-1.005	reg_C[5]	reg_sum[8]	clock	clock	1.000	-0.064	1.771
5	-0.998	reg_C[5]	reg_sum[6]	clock	clock	1.000	-0.066	1.762
6	-0.984	reg_B[5]	reg_sum[8]	clock	clock	1.000	-0.066	1.748
7	-0.980	reg_B[3]	reg_sum[6]	clock	clock	1.000	-0.068	1.742

Path #1: Setup slack is -1.053 (VIOLATED)

Path Summary | Statistics | Data Path

Data Arrival Path

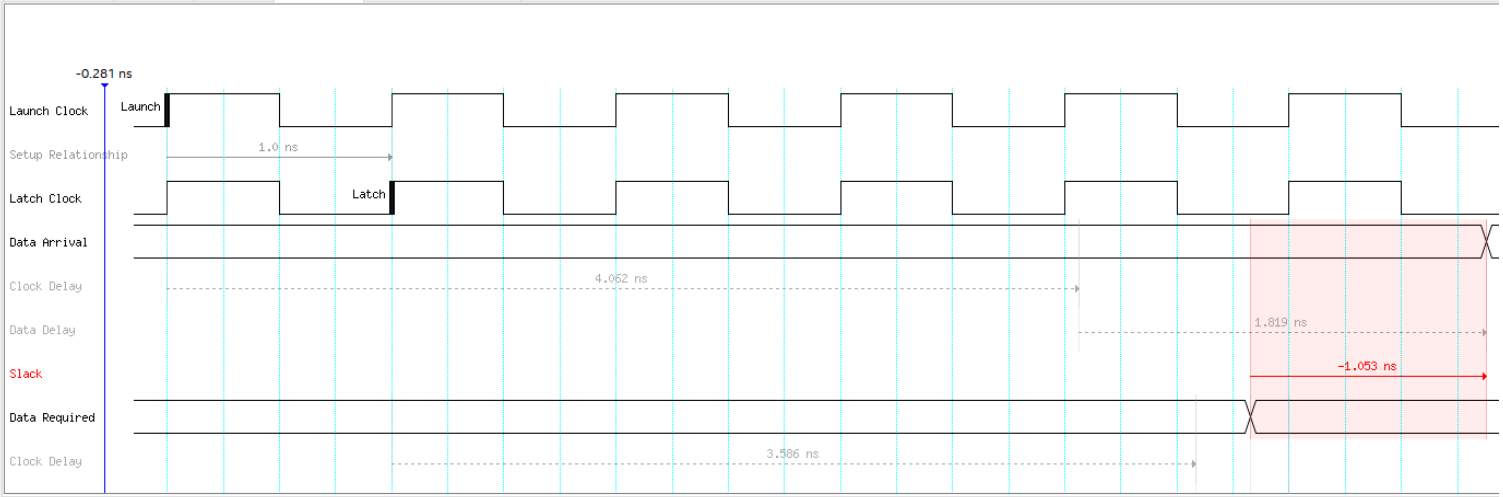
	Total	Incr	RF	Type
1	0.000	0.000		
2	4.062	4.062		
1	0.000	0.000		
2	0.000	0.000		
3	0.000	0.000	RR	IC
4	0.650	0.650	RR	CELL

Data Required Path

	Total	Incr	RF	Type
1	1.000	1.000		
2	4.998	3.998		
1	1.000	0.000		
2	1.000	0.000		
3	1.000	0.000	RR	IC
4	1.650	0.650	RR	CELL
5	2.111	0.461	RR	IC

Path #1: Setup slack is -1.053 (VIOLATED)

Path Summary | Statistics | Data Path | Waveform | Extra Fitter Information



Quartus Timing Optimization

- Tries to optimize your design to meet your desired clock frequency:
  - May not necessarily meet your target
  - Limited by the delays of the various logic and routing resources inside of the FPGA

- If you don't set a timing constraint, tool sets an unachievable value (e.g. 1GHz)

Quartus Timing Optimization

- Effects on optimization when you ask for
  - Slow clock frequency:
    - Leads to smaller circuits. More weight on optimizing for logic utilization
  - Fast clock frequency
    - Leads to larger circuit – more things happening in parallel

All about tradeoffs!

Can Go Faster Than Predicted fmax?

- Overclocking:
  - Quartus gives a conservative estimate
  - Actual delays within the chip vary from chip-to-chip

- Dangerous… don't do it:
  - In your testing, it might appear to work. But, how do you know that you are exercising the critical path?
  - Some chips will be slower than the one you use for prototyping
  - Operating conditions such as temperature affect actual performance

Take a look at the
Timing Analyzer Tutorial on LMS!

THANK YOU