National University of Sciences & Technology (NUST)
School of Electrical Engineering and Computer Science (SEECS)
Department of Electrical Engineering

EE-421: Digital System Design

Course Code:	EE-421	**Semester:**	Spring 2023
Credit Hours:	3 + 1	**Prerequisite Codes:**	Digital Logic Design
Instructor:	Dr. Rehan Ahmed	**Discipline:**	Electrical Engineering
Office:	A-103, RIMMS	**Telephone:**	051-90852127
Lecture Days:	Refer to timetable	**E-mail:**	rehan.ahmed@seecs.edu.pk
Class Room:	Refer to timetable	**Office Hours:**	By Appointment
Knowledge Group:	Integrated Circuits and Systems (ICS)	**Updates on LMS:**	After Lecture

Course Description:

This course is about describing digital logic circuits using Verilog HDL (hardware description language) that are targeted for FPGAs and ASICs. A lot of focus is given to understanding of the interplay between HDL and RTL synthesis to achieve the desired circuit functionality. A broad range of circuits, including but not limited to, conventional combinational & sequential circuits, combinational & multicycle arithmetic circuits and FSM control-path, are discussed and expressed in Verilog HDL. The course focusses on building complex digital systems by integrating various IPs, their functional verification and timing closure of the overall design targeted on an FPGA. An overview of advanced and emerging topics along with the research challenges in the field of digital design is given at the end.

Course Objectives:

After successful completion of this course, students will have practical knowledge of building digital systems using Verilog HDL. They will learn building key logic elements such as storage, clocks, memory, bus architecture and FPGA IPs design, and furthermore how to combine these basic blocks to create complex Datapath. They will learn how to implement finite state machines for control-path. Students will be able to handle cross clock domain issues and design for best PPA (performance, power and area) metric. Students will also develop a strong knowledge base to further pursue research & development in digital system design.

Upon successful completion of this course the students will be able to demonstrate the following:-		**BT LEVEL**	**PLO**
1	**Analyze** various digital system blocks, such as combinational and sequential, for performance metrics, such as speed, area, timing, and power.	C4	2
2	**Design** digital systems using Hardware Description Language (HDL), such as Verilog or VHDL, targeted for programmable logic devices such as FPGAs or CPLDs.	C5	3
3	**Conduct** experiments as well as **analyze** and **interpret** experimental data	P3	4
4	**Construct** digital systems of moderate complexity using laboratory equipment and simulation tools.	P4	5
5	**Exhibit** good professional and ethical behavior. **Adhere** to lab safety rules.	A3	8
6	**Function** effectively both individually and as a member of a team	A4	9
* BT=Bloom's Taxonomy, C=Cognitive domain, P=Psychomotor domain, A=Affective domain			

Recommended Books:

Text Book: 1. Digital System Design with Verilog HDL, 3/e, by Stephen Brown and Zvonko Vranesic.

Support Books:
2. Digital Design with an Introduction to the Verilog HDL by M. Morris R. Mano.
3. Digital Design: Principles and Practices 4th Edition by John F. Wakerly

Lecture Breakdown (Tentative. Topics can be revised and/or new topics can be added during the semester depending on the class interest and need):

Week	Topic	Description/ Lecture Breakdown
1	**Course Introduction + Programmable Logic Devices + EDA**	Introduction to Course + Review of classical digital design methods Evolution of PLDs FPGA Architecture + EDA tools
2	**Verilog + Combinational Logic**	Introduction to Verilog Combinational Building Blocks in Verilog
3	**Verilog + Sequential Logic**	Sequential Circuits in Verilog (Blocking vs Non-Blocking) Sequential-Cct Building Blocks
4	**Testbenches**	Testbenches in Verilog Self-testing testbenches
5	**Finite State Machines**	Expressing Moore and Mealy state machine in Verilog Impact of State-encoding FSMs and EDA
6		**OHT 1**
7	**Design using IP Blocks**	Templates vs IPs Synthesis cookbook approach Example System
8	**Circuit Timing + Metastability**	Critical Path and Fmax Circuit timing analysis Metastability
9	**Timing Closure in FPGA EDA + Cross Clock Domain**	Timing Closure Cross-Clock Domain Issues & RESET circuits
10	**Arithmetic Circuits - I**	Adders (CPG, CSA, CLA)
11	**Arithmetic Circuits - II**	Multipliers (Combinational + Multicycle)
12		**OHT 2**
13	**Arithmetic Circuits - III**	Dividers in Hardware Floating Point Arithmetic and its implementation in Hardware
14	**Fixed-Point Arithmetic**	Fixed-point Arithmetic and its Implementation in Hardware

15	**System-on-Chip (SoC)Design on FPGA**	Soft vs. Hard Microprocessors Interconnect standards Putting together a SOC system
16	**Power in Digital Circuits**	Power in digital circuits Power Optimization Techniques
17	**Research Challenges**	Emerging topics in Digital Systems Architectures
18		**END SEMESTER EXAM**

Grading Policy:

Assignments In order to develop comprehensive understanding of the subject, assignments will be given. Late assignments will not be accepted / graded. All assignments will count towards the total (No 'best-of' policy). The students are advised to do the assignment themselves. Copying of assignments is highly discouraged and violations will be dealt with severely by referring any occurrences to the disciplinary committee. The questions in the assignment are meant to be challenging to give students confidence and extensive knowledge about the subject matter and enable them to prepare for the exams.

Quizzes Please note that the quizzes will be UN-ANNOUNCED.

Other Matters

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other's work, including the copying of Assignments and laboratory results from the other students. Plagiarism is considered a serious offence by the university and severe penalties apply. Therefore, all the students must display originality of efforts and avoid plagiarism in any form.

Classroom Etiquettes

It is the collective responsibility of all the students to make the class environment conducive for learning. To create and maintain a friendly atmosphere, the following standards of class room behavior will be observed:-

1. Students will be punctual for the class. The teacher considers late comers disrespectful of those who manage to be on time.
2. If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended.
3. All the cell phones must be switched OFF prior to entering the class room.

Tools / Software Requirement:

Students will require any good Verilog Simulator such as Modelsim/Verilator and FPGA CAD tools (Xilinx Vivado or Intel Quartus) on their personal machines for practice. Though students will have access to FPGA boards in labs for limited time, it would be far more rewarding to own a decent academic FPGA board for increased learning.