Chapter6: Registers and Counters

Lecture3- Counters with Unused States

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Objectives

- Study Counters with Unused states

Other Counters

- *n* flip-flops can produce 2^n binary states
- Some counters have truncated modulus and have states that are not used in specifying the FSM. Such states
  - may be treated as don't-care conditions or
  - may be assigned specific next states
- Self-correcting counter
  - Ensure that when a counter enters one of its unused states on power up, it eventually goes into one of the valid states after one or more clock pulses so it can resume normal operation.
  - Analyze the counter to determine the next state from an unused state after it is designed

Example: Counter with unused States

Table 6-7
State Table for Counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Count: 0, 1, 2, 4, 5, 6, and repeat. Two unused states: 011 & 111

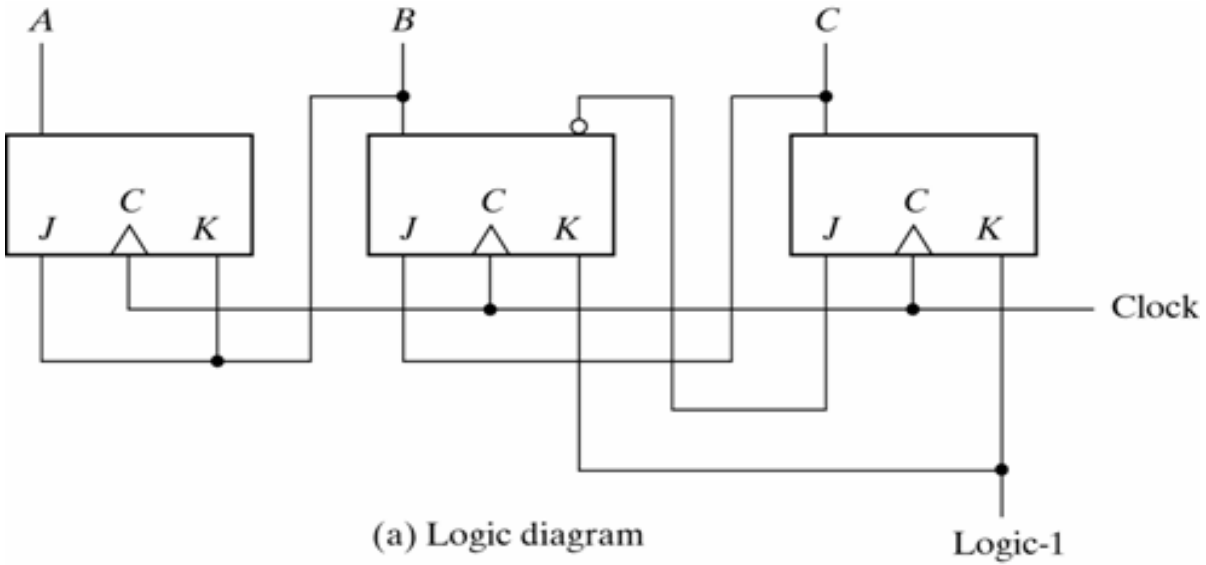
The simplified flip-flop input equations using map method are:

$J_A = B,\ K_A = B$

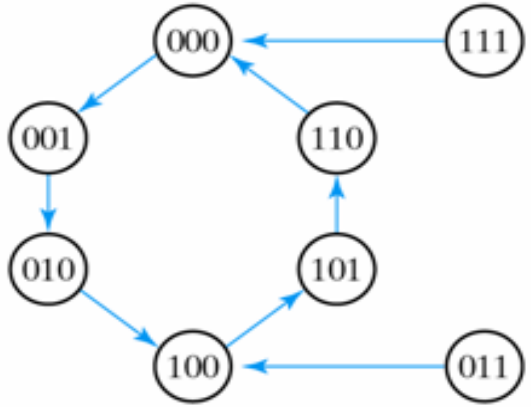
$J_B = C,\ K_B = 1$

$J_C = B',\ K_C = 1$

The logic diagram & state diagram of the counter



(a) Logic diagram



(b) State diagram

Fig. 6-16 Counter with Unused States

Ring counter

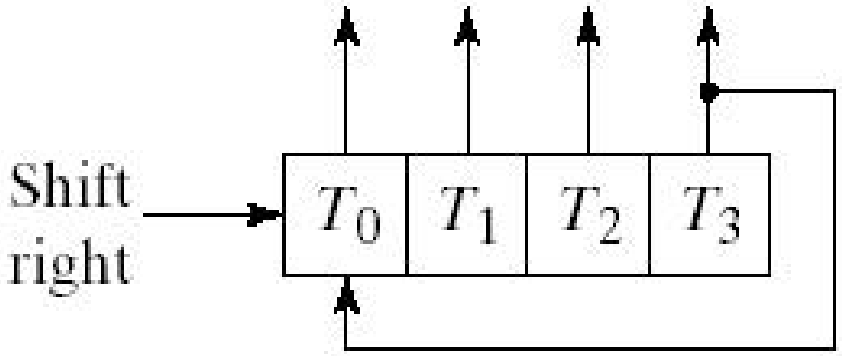
- The timing signals that control the sequence of operations in a digital system can be generated either with a shift register or a counter with a decoder.
- A ring counter is a circular shift register with only one flip-flop being set at any particular time, all others are cleared

  (initial value = 1 0 0 … 0)
- The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals.
- A 4-bit Ring counter can be designed using conventional design procedures to follow the sequence 0001, 1000, 0100, 0010, and repeat. We can take advantage of 12 unused states as don’t cares to optimize the design. Any type of flip-flops can be used in the design. The behavior of unused states will reveal that it is not self-correcting.

Ring counter

- A 4-bit ring counter will follow the following counting sequence

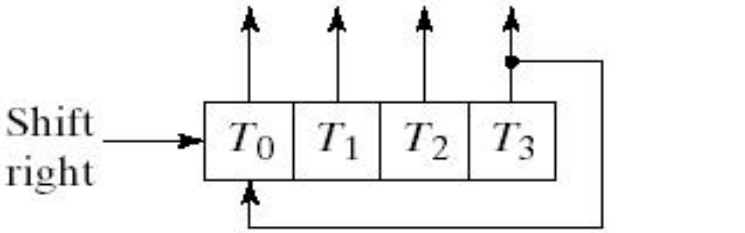
A_3	A_2	A_1	A_0
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0



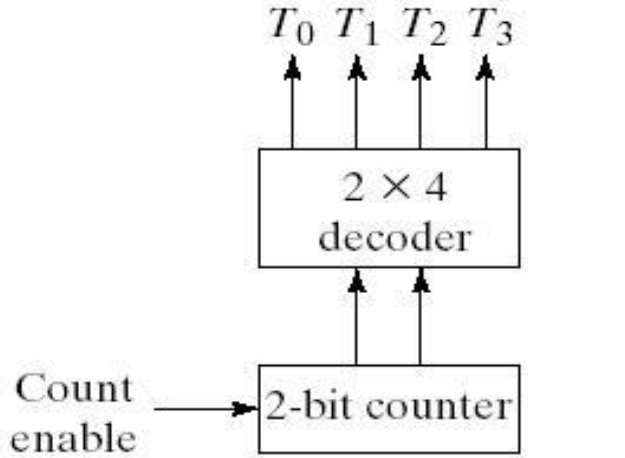
(a) Ring-counter (initial value = 1000)

Ring counters

- Application of counters
  - Counters may be used to generate timing signals to control the sequence of operations in a digital system.
- Approaches for generation of 2^n timing signals
  1. a shift register with 2^n flip-flops
  2. an n-bit binary counter together with an n-to-2^n-line decoder



(a) Ring-counter (initial value = 1000)



(b) Counter and decoder

Ring Counter Timing Signals

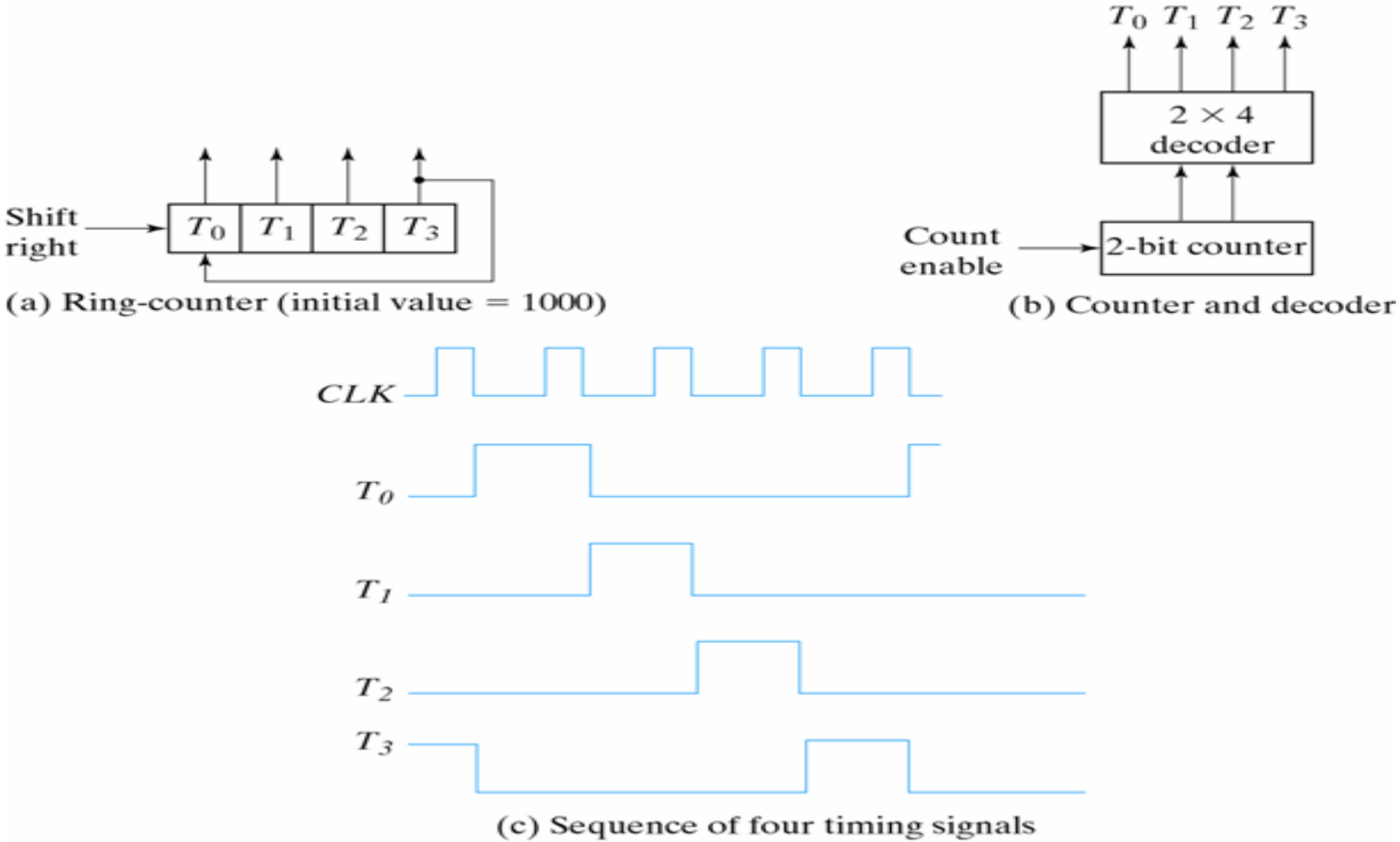


Fig. 6-17 Generation of Timing Signals

Johnson counter

- Ring counter vs. Switch-tail ring counter
  - Ring counter
    - a *k*-bit ring counter circulates a single bit among the flip-flops to provide *k* distinguishable states.
  - Switch-tail ring counter (Johnson)
    - is a circular shift register with the complement output of the last flip-flop connected to the input of the first flip-flop
    - a k-bit switch-tail ring counter will go through a sequence of 2k distinguishable states. (initial value = 0 0 … 0)
- To generate 2^n timing signals, we require either a shift register with 2^n flip-flops or an *n*-bit binary counter together with an *n*-to-2^n-line decoder. For example, 16 timing signals can be generated with a 16-bit shift register or a 4-bit binary counter and a 4-16 line decoder. It is also possible to generate 16 timing signals with a combination of an 8-bit shift register and 8x 2-input AND gates. This combination is called a Johnson (Twisted) Ring counter. A Johnson counter is not a self-correcting counter but after adding correction it can be made self-correcting.

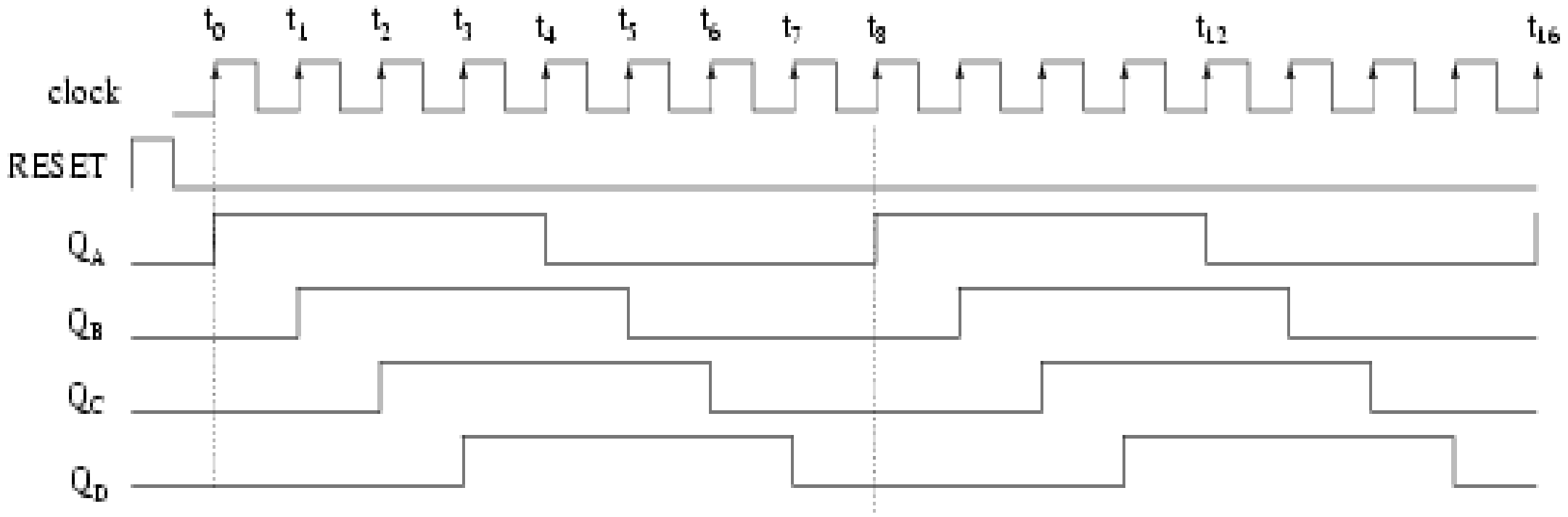
4-bit Johnson counter

- To provide for 2*k* timing signals, a *k*-bit switch-tail ring counter + 2*k* decoding gates are required
  - Example: 4-bit Johnson counter design

Sequence number	Flip-flop outputs				AND gate required for output
	A	*B*	*C*	*E*	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

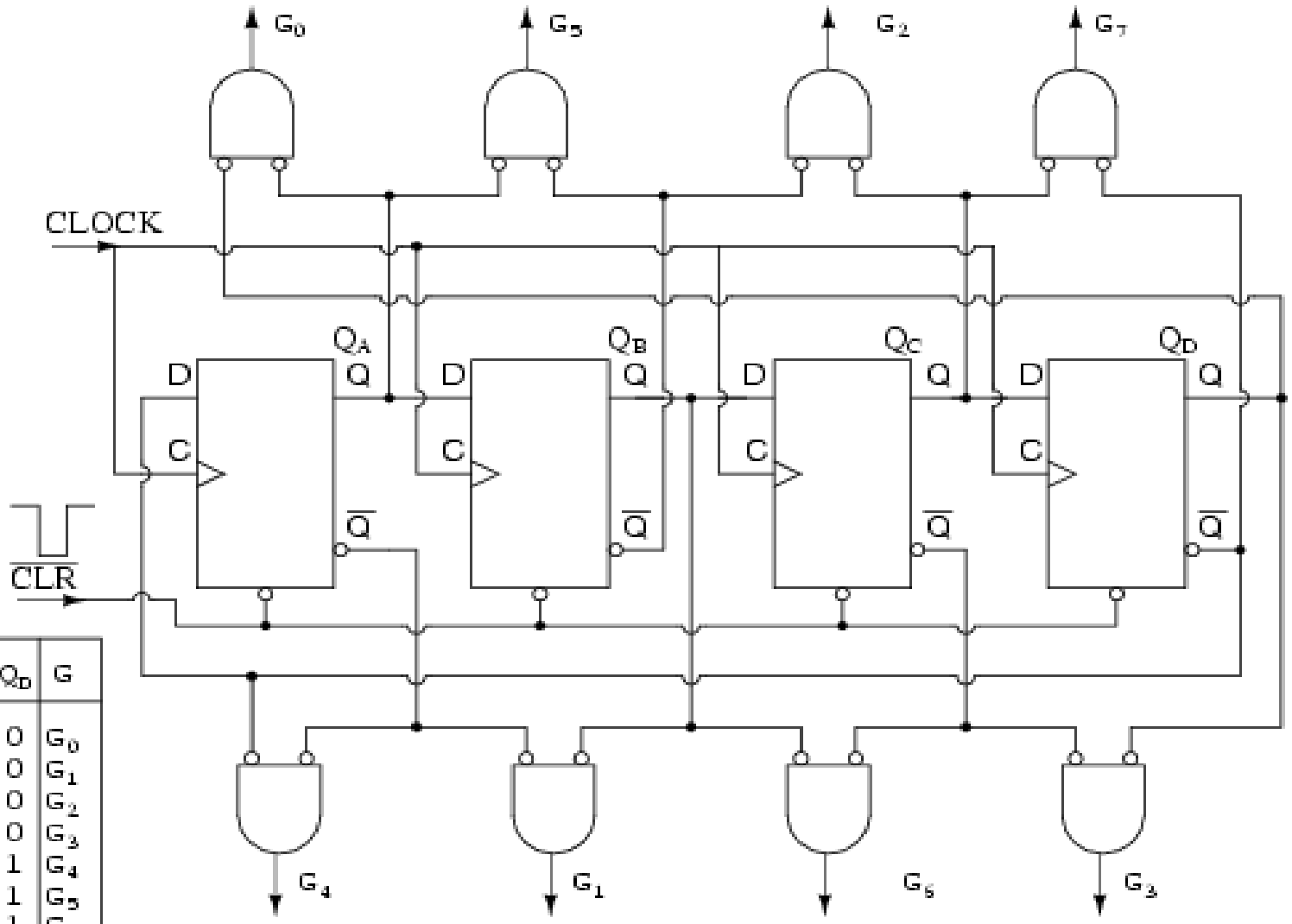
- The decoding follows a regular pattern
  - ➢ 2 inputs per decoding gate

Johnson Counter Timing Diagram



Four stage Johnson counter waveforms

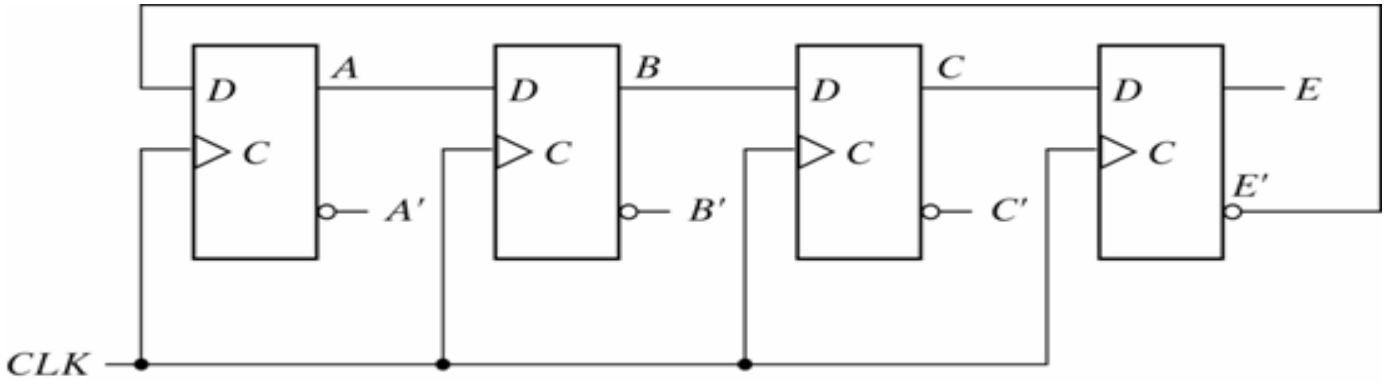
States decoding using NOR gates



Q_A	Q_B	Q_C	Q_D	G
0	0	0	0	G_0
1	0	0	0	G_1
1	1	0	0	G_2
1	1	1	0	G_3
1	1	1	1	G_4
0	1	1	1	G_5
0	0	1	1	G_6
0	0	0	1	G_7

Johnson counter with decoder (CD4022B)

Johnson counter example: Switch-tail ring counter



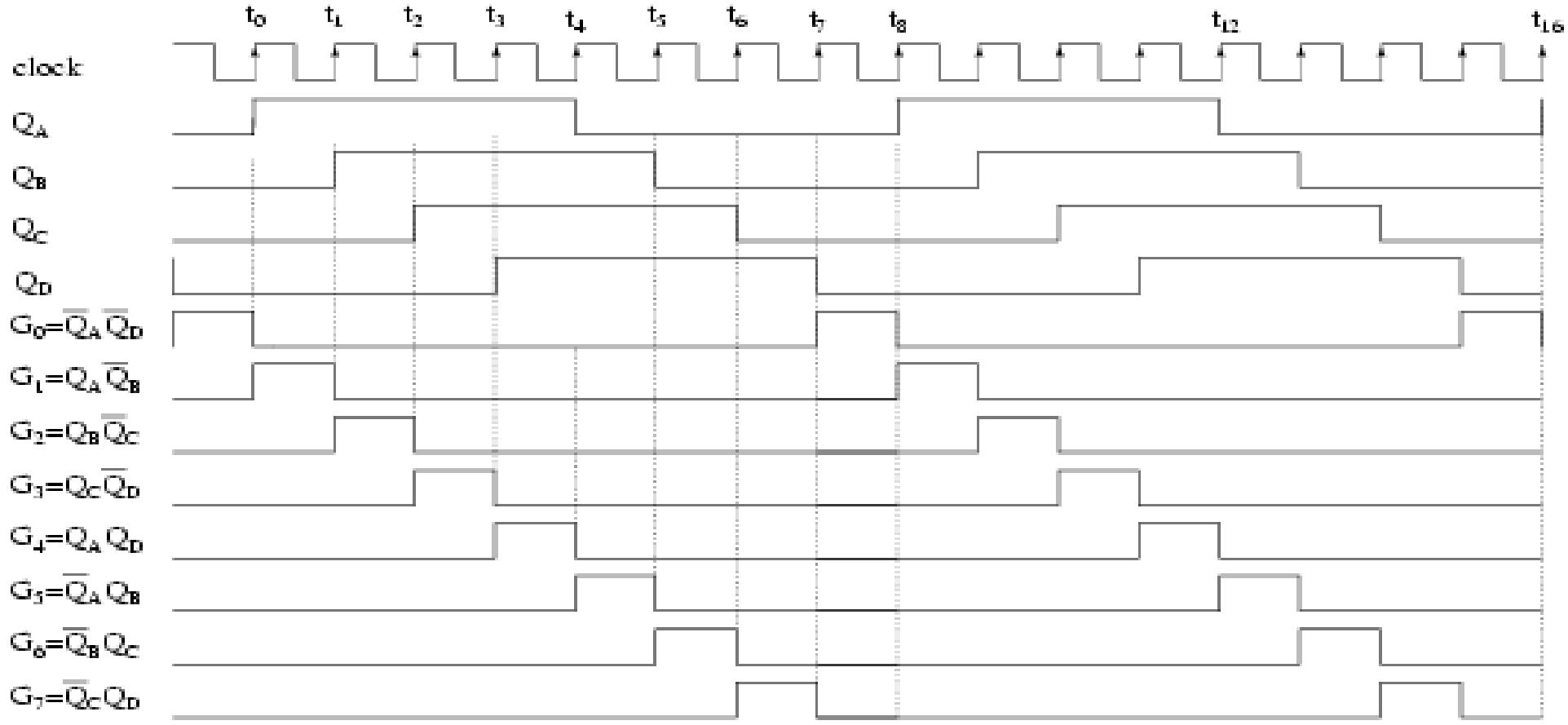
(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs				AND gate required for output
	A	B	C	E	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

Fig. 6-18 Construction of a Johnson Counter

Timing Signals with States decoding



Four stage (8-state) Johnson counter decoder waveforms

Important to note

- Disadvange of the switch-tail ring counter
  - If it finds itself in an unused state, it will persist to circulate in the invalid states and never find its way to a valid state.
  - One correcting procedure: $D_C = (A + C)\, B$
  - ABC = 010 will make $D_C = 0$ instead of $D_C = B = 1$
- Summary:
  - Johnson counters can be constructed for any # of timing sequences:

    # of flip-flops = 1/2 (the # of timing signals)

    # of decoding gates = # of timing signals

    2-input per gate

The End