School of Electrical Engineering and Computer Science
National University of Sciences & Technology (NUST)

Practice Assignment No-4

Subject:	**Digital Logic Design**	Course:	**BEE-12CD**
Teacher:	**Engr. Arshad Nazir**	Issue:	**19 Nov 2021**

- ✓ *This is a non-graded assignment prepared to enhance problem-solving skills of students from chapter3 of the textbook.*
- ✓ *The students are advised to attempt it any time of their convenience.*

Problem No-1 Design a code converter that should convert a Hexadecimal digit to 7-bit ASCII code. List truth table, write minterm list equations for each output variable, simplify each output function using K-maps and draw the logic diagram using minimum number of AND, OR, and NOT gates. Assume that only normal inputs are available from the source. If AND/OR gates have a propagation delay of 10 ns, and propagation delay of NOT gates be 5ns. What is the total propagation delay time in the converter?

Problem No-2 A BCD to seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in a display indicator used for displaying the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in figure P4-9(a) of your textbook and reproduced below. The numeric display chosen to represent the decimal digit is shown in figure P4-9(b). Design the BCD to seven-segment decoder using a minimum number of gates. The six invalid combinations result in a blank display.

Problem No-3 Braille is a system which allows a blind person to read alphanumeric by feeling a pattern of raised dots. Design a circuit that converts BCD to Braille. The table shows the correspondence between BCD and Braille.

				W	X
A	B	C	D	Z	Y
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		

Realize this circuit with two-level NAND gates having a maximum fan-in of four. Use minimum number of gates in design.

Problem No-4 Design a 4-bit Arithmetic Logic Unit (ALU) to perform the following functions

Select Lines		Output Z	Comments
S_1	S_0		
0	0	A plus B	Addition
0	1	A plus B´plus 1	2's complement Subtraction
1	0	A·B	Logical AND
1	1	(A⊕B)	Exclusive-OR

Use 2-to-1 multiplexers, binary adders, and gates as needed. Assume that A and B are both 4-bit numbers. Draw the logic circuit.

Problem No-5 A computer can execute instructions to perform shift operations on the contents of a general-purpose shift register. A logic shifter is a combinational circuit capable of rotating the given 4-bit data to the left by n positions, where 0≤n≤3.

Design a combinational logic shifter with 4-bit input and 4-bit output as follows:

$\overline{\text{OE}}$	Shift Count S_0 S_1	Output
1	× ×	High impedance output lines
0	0 0	No Shift
0	0 1	Left Shift once
0	1 0	Left Shift twice
0	1 1	Left Shift three times

Where x means don't care conditions, List truth table.

Draw logic diagram of 4×4 shifter register using multiplexers and tri-state buffers.

Problem No-6 Implement the following Boolean function with 4:1 multiplexer and external gates: -

$$F(A,B,C,D)=\sum(1,3,4,11,12,13,14,15)$$

Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of the variables C and D. The values of these variables are obtained by expressing F as a function of C and D for each of the four cases when AB=00, 01,10and 11. These functions must be implemented with external gates.

Problem No-7 Design a "disk spinning" animation circuit for a CD player. The input to the circuit will be a 3-bit binary number A_1, A_2, A_3 provided by another circuit. It will count from 0 to 7 in binary, and then it will repeat. The animation will appear on the top four lights of the LED display of Figure P7, i.e on X_1, X_2, X_7, and X_6, going clockwise. The animation should consist of a blank spot on a disk spinning around once, beginning with X_1. Then, the entire disk should blink on and off twice.

Figure P7 Disk Spinning Animation Circuit

Design the circuit using only 2, 3, and 4-input NOR gates and inverters. Try to minimize the number of gates required. Any solution which uses 11 or fewer gates (not counting the inverters for the inputs) is acceptable.

Problem No-8 Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

Problem No-9 Realize the logic circuit shown in Figure P9 with an 8:1 multiplexer constructed from two 4:1 multiplexer with enable input E, an inverter, and one OR gate. Use minimum number external logic gates.

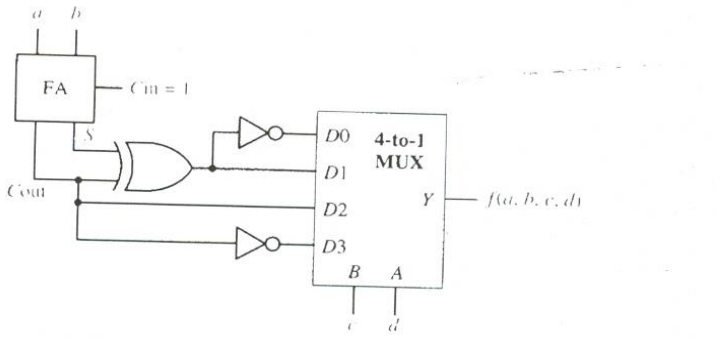


Figure P9: Logic Circuit

Problem No-10 Design a circuit which displays the letters A through J on a seven-segment indicator. The circuit has four inputs W, X, Y, and Z which represent the last 4 bits of the ASCII code to be displayed. For example, if WXYZ=0001, "A" will be displayed. The letters should be displayed in the following form:

Design your circuit using only 2, 3, and 4-input NOR gates and inverters. Any solution with 22 or fewer gates and inverters (not counting the four inverters for the inputs) is acceptable.

Problem No-11 Design a commercial Octal-to-binary priority encoder with inputs D_0, D_1, D_2…, D_7 and outputs x, y, z. Provide an output V to indicate that at least one of the inputs is present. The input with the lowest subscript number has the highest priority.

Specify the truth table, derive algebraic expressions for each output function and draw the logic diagram of the encoder circuit using AND, OR, and NOT gates.

Problem No-12 Implement the following functions using decoders and any size OR gates you may need

F(P,Q,R)= (PQ+R)´ using a 3:8 decoder
F(P,Q,R,S,T)=(P+Q)S+(R+T)S´ using two 2:4 decoders
f(a,b,c,d)=Σ_m(0,3,5,7,11,12,13,15) using a 4:16 decoder

Problem No-13 In a certain chemical – processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified point.

Design a circuit that monitors the chemical level and indicate when the level in any two of the tanks drops below the specified point.

Draw the circuit using NAND – AND two-level implementation.

Problem No-14 In a simple copy machine, a stop signal s is to be generated to stop the machine operation and energizing an indicator light whenever either of the following conditions exist: (1) There is no paper in the paper feeder tray or (2) the two micro switches in the paper path are activated, indicating a jam in the paper path.

The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the micro switches produces a logic signal (Q & R) that goes HIGH whenever a paper is passing over the switch to activate it. Design the logic circuit to produce a HIGH at output signals for the stated condition and implement it using two-input NAND gates only.

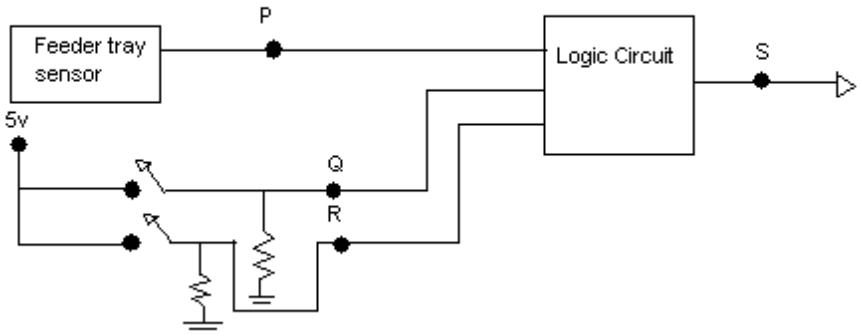


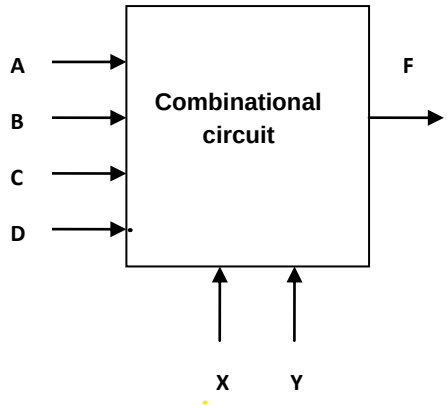
Figure Problem 14: A Combinational Circuit

Problem No-15 Professor Ali computes grades as follows: He uses only the first digit (that is, 9 for averages between 90 and 99). He never has an average of 100. He gives a P (pass) to anyone with an average of 60 or above and an F to anyone with an average below 60. That first digit is coded in 8421 code (that is, straight binary, 5 as 0101, for example); these are inputs w, x, y, and z.

Give the truth table of the problem. Implement the circuit using decoder and logic

Problem No-16 The system is a speed warning device. It receives, on two lines, an indication of the speed limit on the highway. There are three possible values 45, 55, or 65 MPH. It receives from the automobile, on two other lines, an indication of speed of the vehicle. There are four possible values under 45, between 46 and 55, between 56 and 65, and over 65 MPH. It produces two outputs. The first f indicates whether the car is going above the speed limit. The second g indicates that the car is driving at "dangerous speed" – defined as either over 65 MPH or more than 10 MPH above the speed limit. Show how each of the inputs and outputs are coded (in terms of binary values) and complete the truth table for the system. Design the system using appropriate size of multiplexers.

Problem No-17 A combinational circuit is depicted below,



The system truth table is

X	Y	F
0	0	C
0	1	A Plus D
1	0	B Plus C
1	1	D

Implement the circuit using following components only

Two 2 X 1 MUX
One Half Adder
One gate of each type (As required)

Problem No-18 Design a priority encoder with four active high inputs 0, 1, 2 and 3 and three active high outputs A and B indicating the number of the highest priority device requesting service, and N indicating no active requests. Input 0 is the highest priority (and 3 the lowest). Give the truth table and Boolean expression for the outputs as a function of inputs.

Problem No-19 Design a circuit that either Adds 5 or subtracts 5 from a 4-bit binary number N. Let the inputs N_3, N_2, N_1, N_0 represent N. The input K is a control signal. The circuit should have outputs M_3, M_2, M_1, M_0, which represent the 4-bit number M. When K=0, M=N+5. When K=1, M=N-5. Assume that the inputs for which $M>1111_2$ or $M<0_2$ will never occur.

a. Implement your design with Two-Level NOR-NOR form. one **4-bit Binary Adder**, one **Quad 2-1 Multiplexer** and **NOT** gates as required. Also design a circuit for error **E** display in case any invalid combination occurs.
b. Implement your design with one **4-bit Binary Adder**, one **Quad 2-1 Multiplexer** and **NOT** gates as required. Also design a circuit for error **E** display in case any invalid combination occurs.

Problem No-20 Design a 4-bit priority encoder with inputs D_O, D_1, D_2, and D_3, two outputs x, y and one valid bit indicator function V. Assign highest priority to D_O and lowest priority to D_3. Use AND, OR, and NOT gates to implement your design.

Problem No-21 Design a combinational circuit that accepts a 4-bit number and generates a 3-bit binary number that approximates the square root of the number. For example, if the square root is 3.5 or larger, give a result of 4. If the square root is < 3.5 and ≥ 2.5, give a result of 3.

Problem No-22 A traffic light control at a simple intersection uses a binary counter to produce the following sequence of combinations on lines A, B, C, and D: 0000, 0001, 0011, 0010, 0110, 0111, 0101, 0100, 1100, 1101, 1111, 1110, 1010, 1011, 1001, and 1000. After 1000, the sequence repeats, beginning again with 0000. Each combination is present for 5 seconds before the next one appears. These lines drive combinational logic with outputs to lamps RNS (Red- North/South), YNS (Yellow- North/South), GNS (Green- North/South), REW (Red- (East/West), YEW (Yellow- East/West), and GEW (Green- East/West). The lamp controlled by each output is ON for a 1 applied and OFF for a 0 applied. For a given direction, assume that green is on for 30 seconds, yellow is on for 5 seconds, and red is on for 45 seconds. (The red intervals overlap for 5 seconds.) Divide up the 80 seconds available for the cycle through the 16 combinations into 16 intervals and determine which lamps should be lit in each interval based on expected driver behavior. Assume that, for interval

0000, a change has just occurred and that GNS =1, REW=1, and all other outputs are 0.

Design the logic circuit to produce the six outputs using AND and OR gates and inverters

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“Good Luck”