Chapter6: Registers and Counters

Lecture4- Problem-Solving Session

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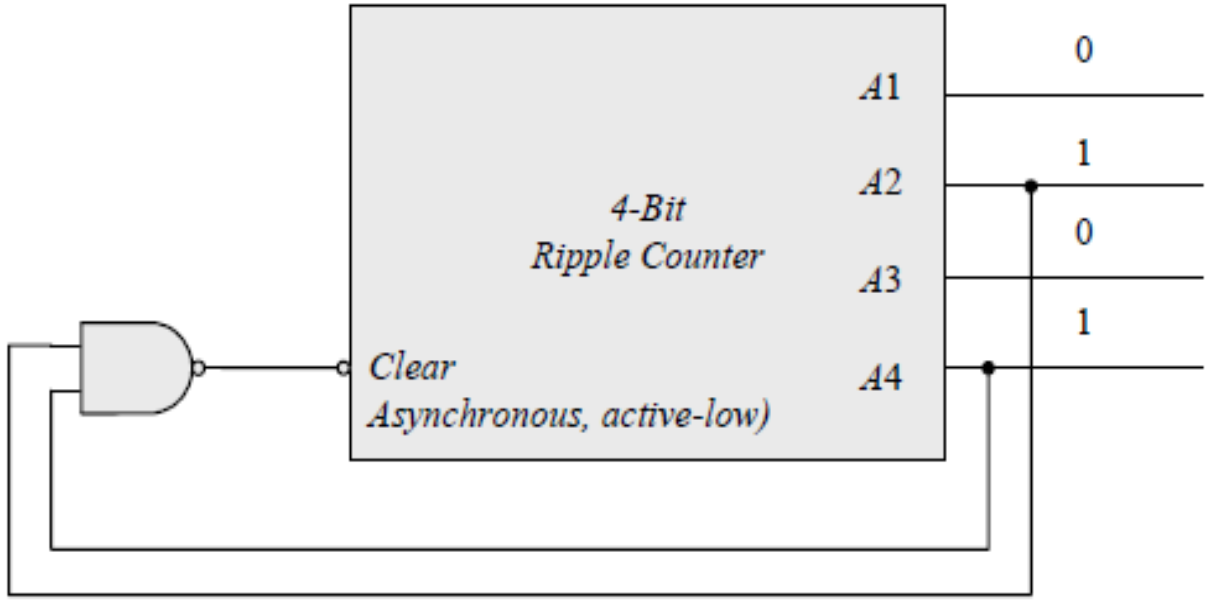
Problem6-6: Design a four-bit shift register with parallel load, using D flip-flips. There are two control inputs: Shift and Load. When Shift=1, the contents of the register are shifted by one position. New data are transferred into the register when Load=1 and Shift=0. If both control inputs are equal to 0, the contents of the register do not change.

Problem6-7: Draw the logic diagram of a 4-bit register with four D flip-flops and four 4:1 multiplexers with mode selection inputs S1 and S0. The register operates according to the following function table.

s_1	s_0	Register Operation
0	0	No change
0	1	Complement the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

Problem 6-13: Show that a BCD ripple counter can be constructed from a 4-bit binary ripple counter with asynchronous Clear input and a NAND gate that detects the occurrence of the count 1010.



Problem 6-19: The flip-flop input equations for a BCD counter using T flip-flops are given in section 6-4. Obtain the input equations for a BCD counter that uses

(a) JK flip-flops and

(b) D flip-flops

(b) From the state table in Table 6.5:

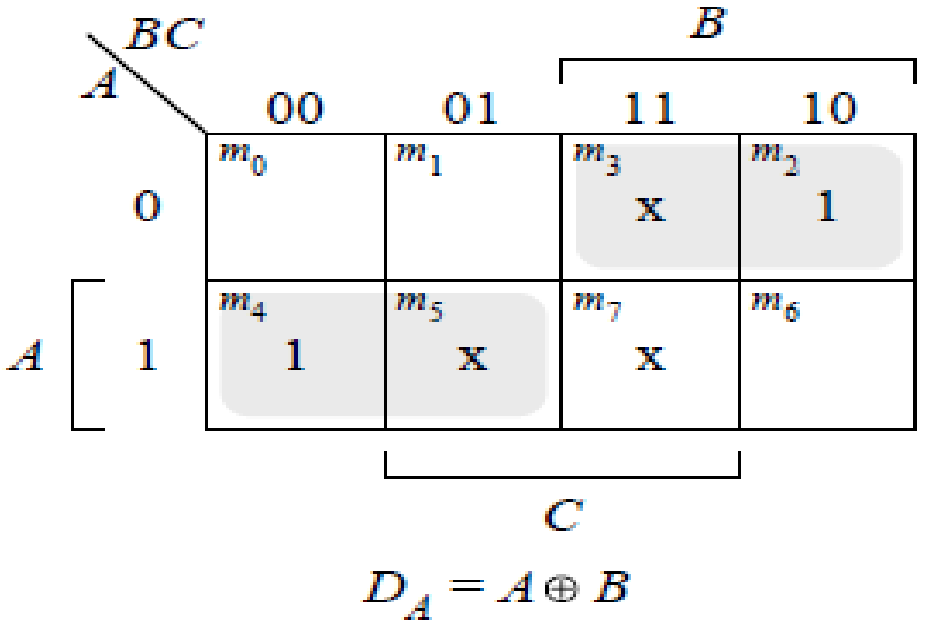
$$D_{Q1} = Q'_1$$
$$D_{Q2} = \sum (1, 2, 5, 6)$$
$$D_{Q4} = \sum (3, 4, 5, 6)$$
$$D_{Q8} = \sum (7, 8)$$
$$\text{Don't care: } d = \sum (10, 11, 12, 13, 14, 15)$$

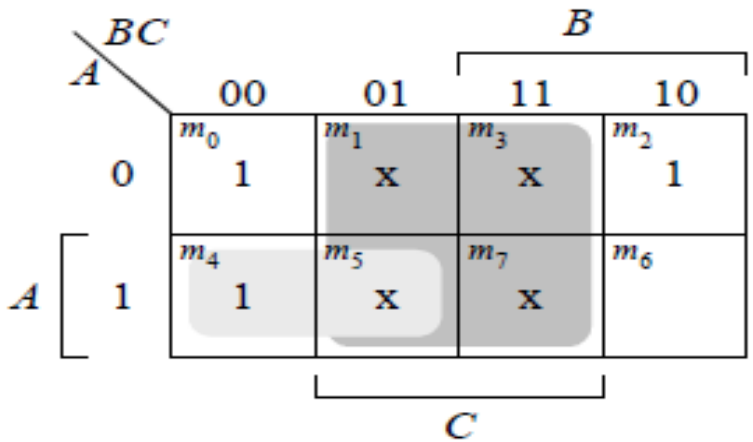
Simplifying with maps:

$$D_{Q2} = Q_2Q'_1 + Q'_8Q'_2Q_1$$
$$D_{Q4} = Q_4Q'_1 + Q4Q'2 + Q'_4Q_2Q_1$$
$$D_{Q8} = Q_8Q'_1 + Q_4Q_2Q_1$$

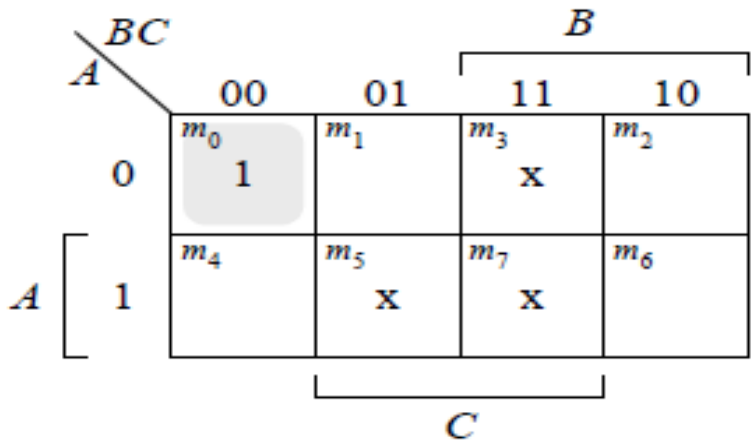
Problem 6-28: Design a 3-bit counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use D flip-flops. Is your counter self-correcting.

Present state *ABC*	*Next state* *ABC*
000	001
001	010
010	100
011	xxx
100	110
101	xxx
110	000
111	xxx



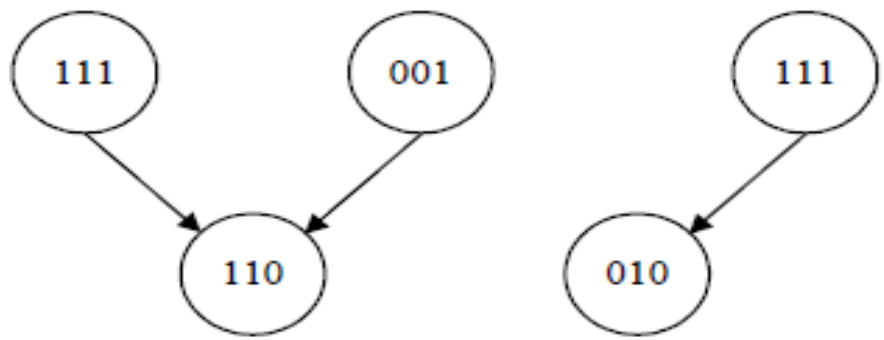


$$D_B = AB' + C$$



$$D_C = A'B'C'$$

Self-correcting



Problem: Design a synchronous modulo-6 up-down counter with a single input line x. The counter uses a creeping code, advances following x=0 and regresses for x=1. it operates as under:-

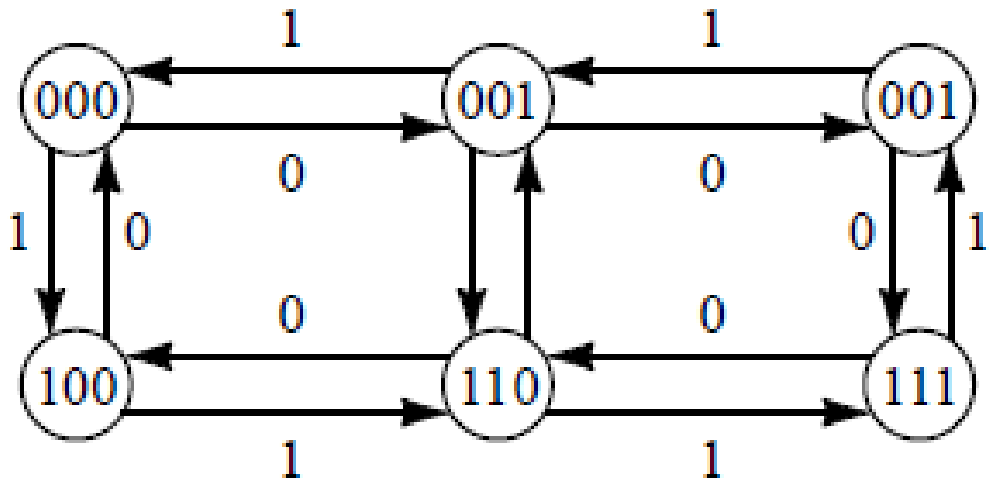
When x=0: counts up through the sequence 000, 001, 011, 111, 110, 100, and repeat

When x=1: counts down through the sequence 000, 100, 110, 111, 011, 001, and repeat.

(a) Draw the state diagram

(b) List the state transition table

(c) Design the modulo-6 up-down counter with D flip-flops and external AND, OR, and NOT gates as required.

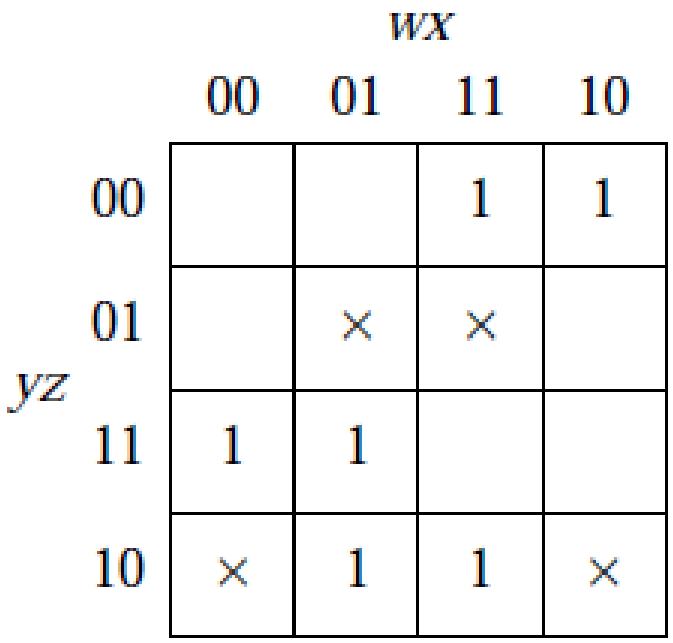


(*a*)

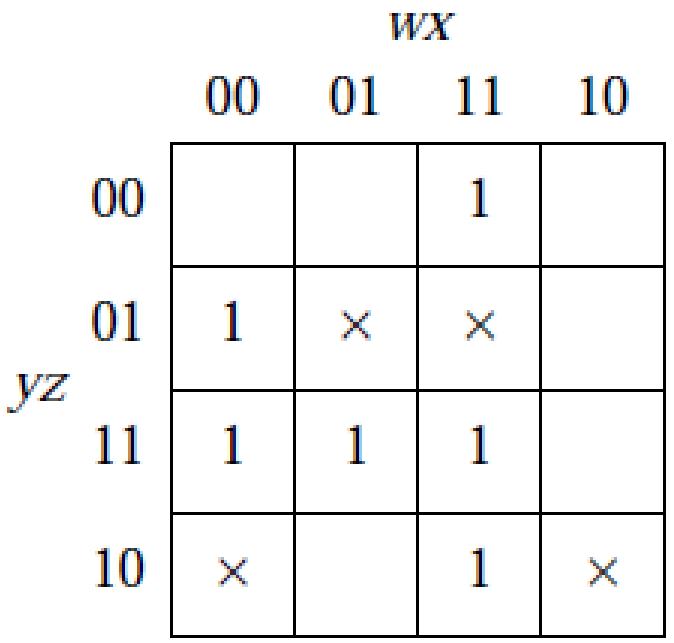
$y_1y_2y_3$	$y_1^+y_2^+y_3^+$ $x=0$	$x=1$
000	001	100
100	000	110
110	100	111
111	110	011
011	111	001
001	011	000

(*b*)

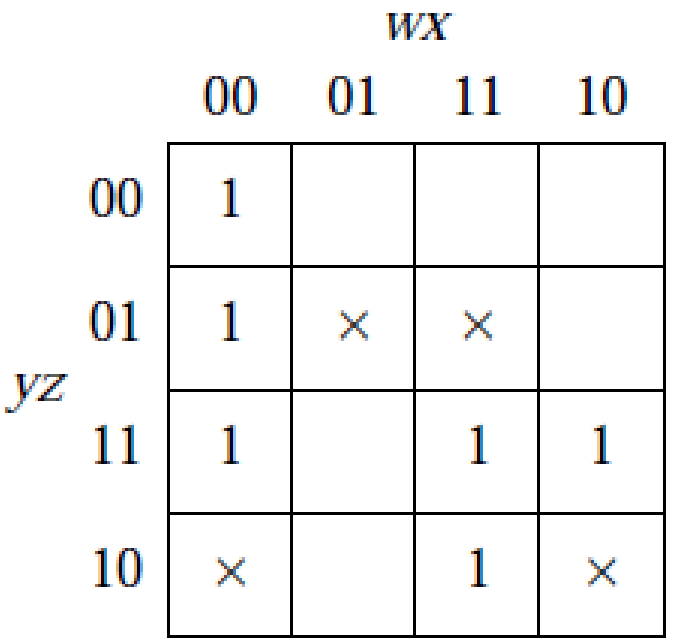
Figure State table and transition table for a modulo-6 up-down counter.



$$D_1 = x'y_2 + xy_3'$$



$$D_2 = x'y_3 + xy_1$$



$$D_3 = x'y_1' + xy_2$$

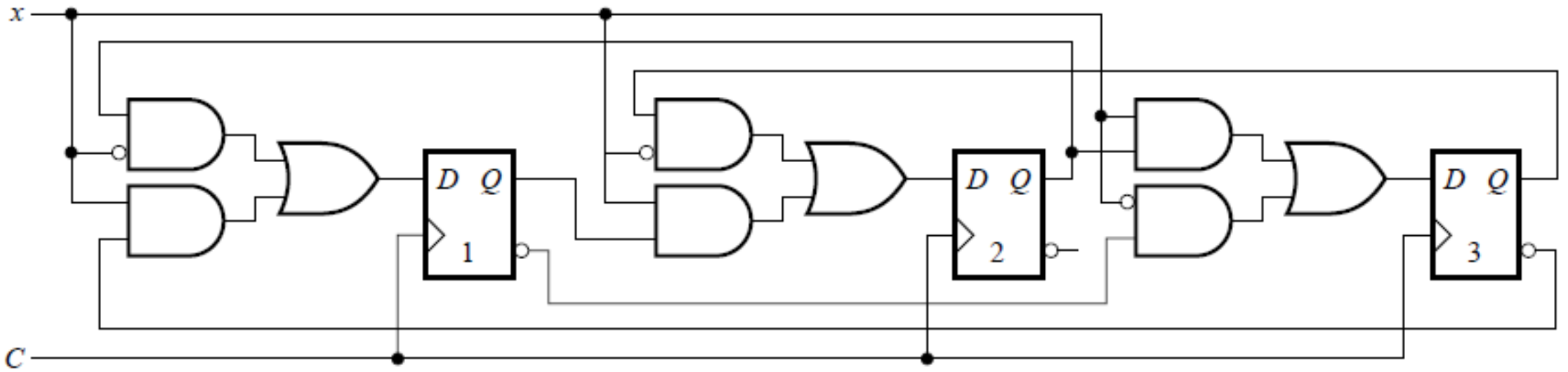


Figure Design of Modulo-6 up-down Counter with D Flip-Flops and external gates

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