Chapter4: Combinational Logic

Lecture9- Study Design of Tri-state Gates, Function Implementation using Tri-state Gates

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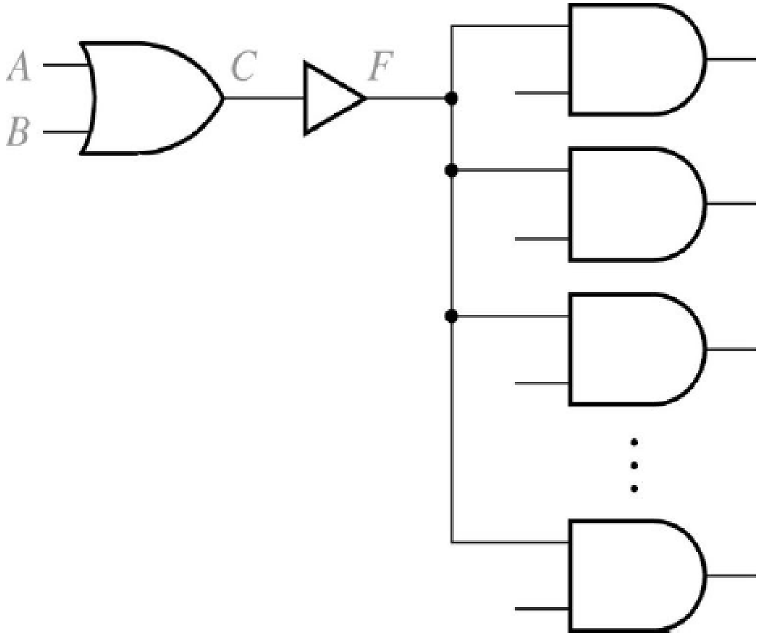
Objectives

- Study Design and Applications of Tri-state Gates
- Function Implementation using Tri-state Gates

Three-state gates

- Logic gates have limited driving capability. A gate output can only drive a limited number of other gate inputs without degrading circuit performance. Buffers can be inserted to increase the driving capability of a gate output.



- Direct connection of two or more gate outputs together is dangerous. Use of three-state (tri-state) buffers permits such connections.

Three-state gates

- A three-state gate is a digital circuit that exhibits three states: 0, 1, and high-impedance (high z state). The high-impedance state behaves as an open circuit.

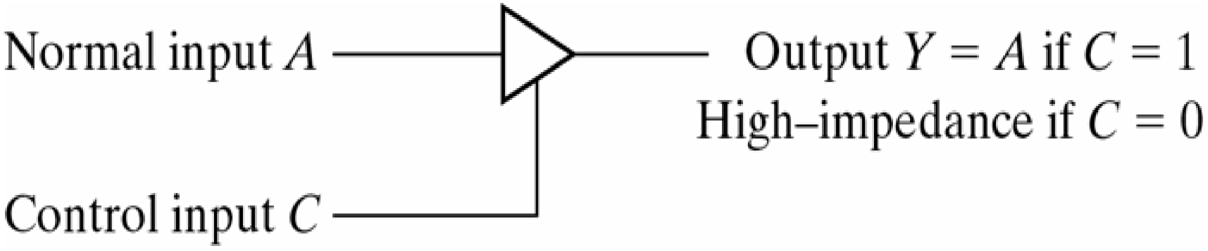
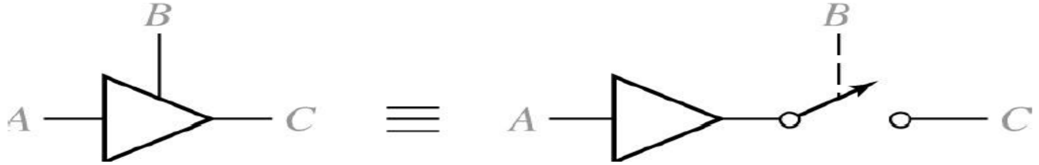
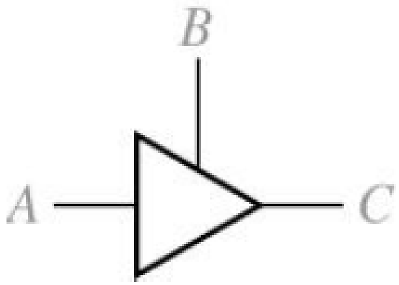


Fig. 4-29 Graphic Symbol for a Three-State Buffer

- Because of this feature (high z state), a large number of three-state gate outputs can be connected to form a common line without endangering loading effects.
- The Figure below nt.

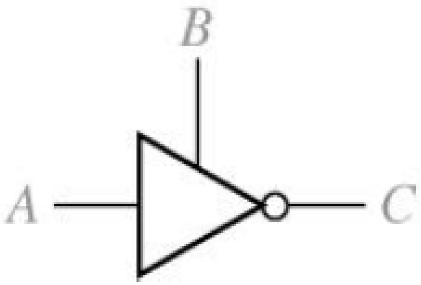


Four Kinds of Tri-State Buffers



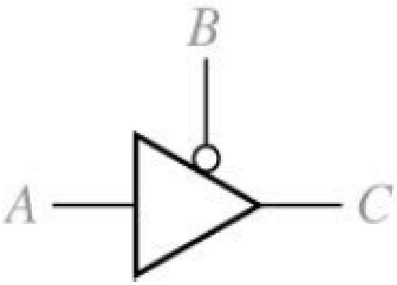
B	A	C
0	0	Z
0	1	Z
1	0	0
1	1	1

(a)



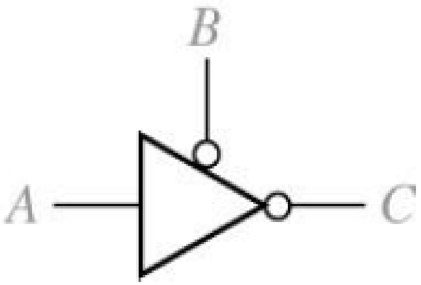
B	A	C
0	0	Z
0	1	Z
1	0	1
1	1	0

(b)



B	A	C
0	0	0
0	1	1
1	0	Z
1	1	Z

(c)



B	A	C
0	0	1
0	1	0
1	0	Z
1	1	Z

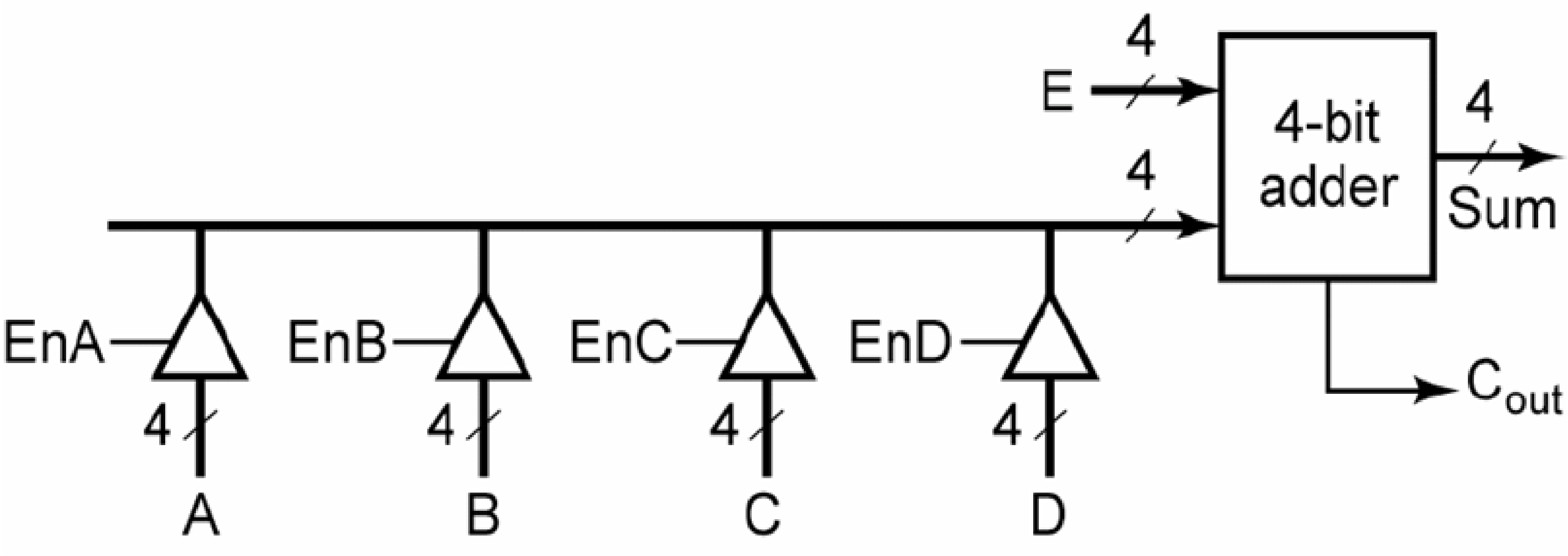
(d)

We use the Symbol Z to represent high-impedance state

Three-state gates Applications

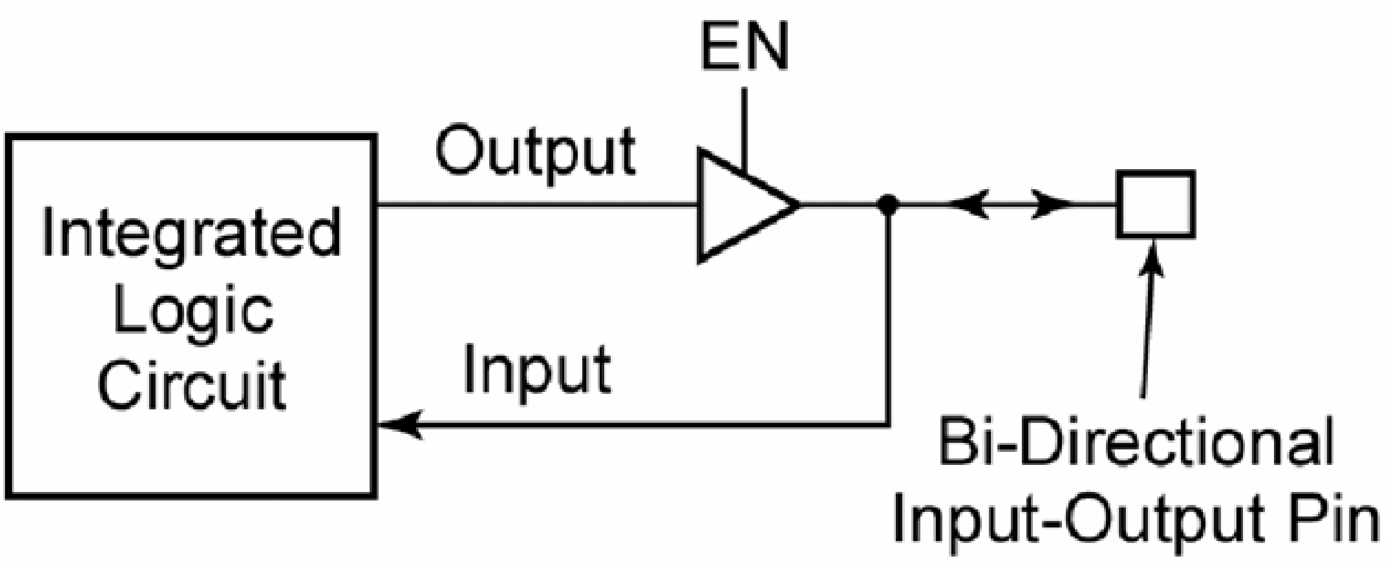
- Data selection/communication over a shared channel(bus).
- Integrated circuits with bidirectional input/output pins.
- Used in the design of multiplexers.
- Data isolation.
- Output state: 0, 1, and high-impedance(Hi-Z)

Data Selection over a Shared Bus



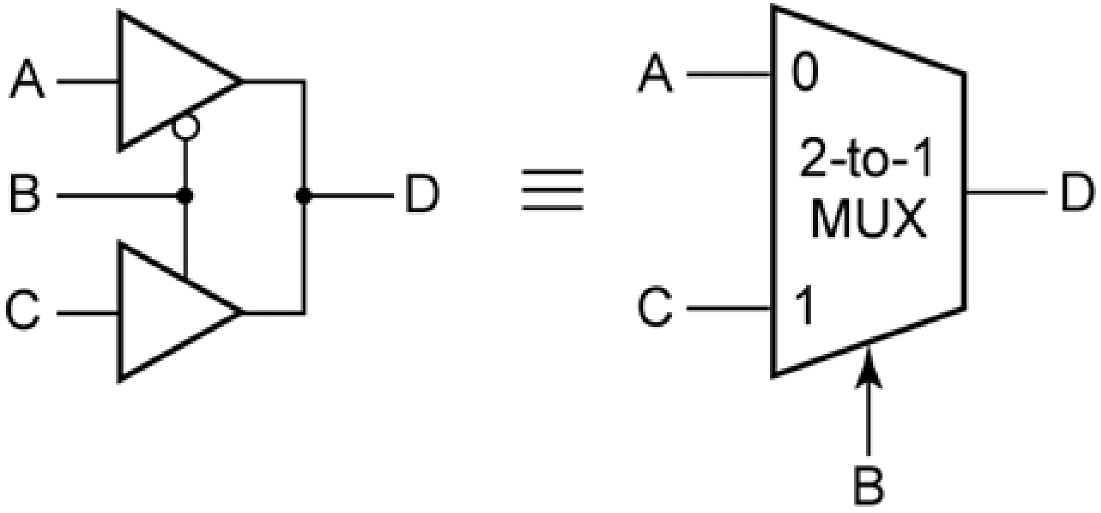
4-Bit Adder with Four Sources for One Operand

Integrated circuits with Bi-Directional Input-Output Pins



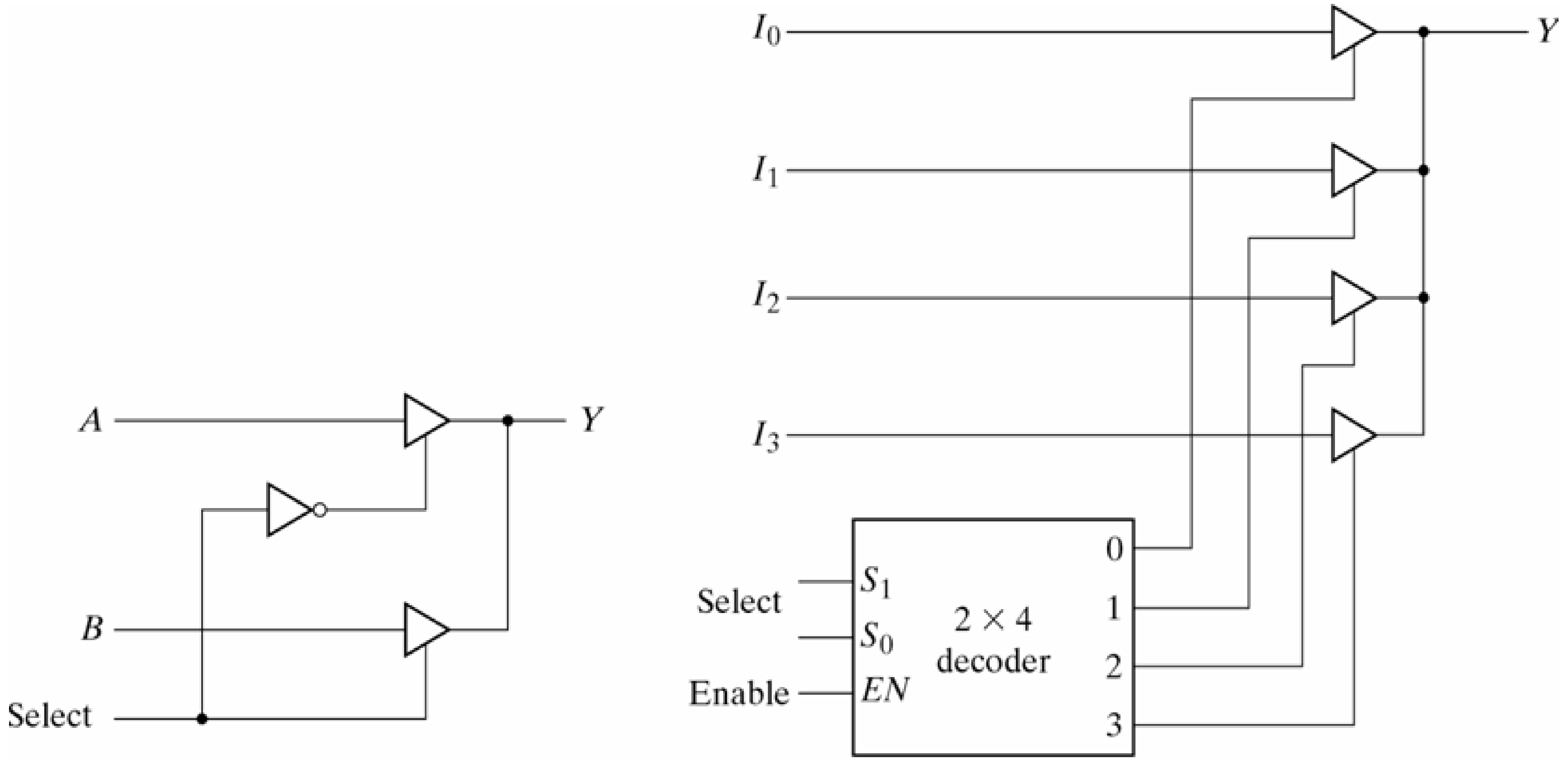
Integrated Circuit with Bi-Directional Input/Output Pin

Design of Multiplexers using Three-State Gates



Data Selection Using Three-State Buffers

MUX Design using Tri-State gates



(a) 2-to-1- line mux

(b) 4 - to - 1 line mux

Fig. 4-30 Multiplexers with Three-State Gates

Problem Solving Session

Problem:4-5

Design a combinational circuit with three inputs, x, y and z, and the three outputs, A, B, and C. when the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

Solution:

Design procedure:

Derive the truth table that defines the required relationship between inputs and outputs.

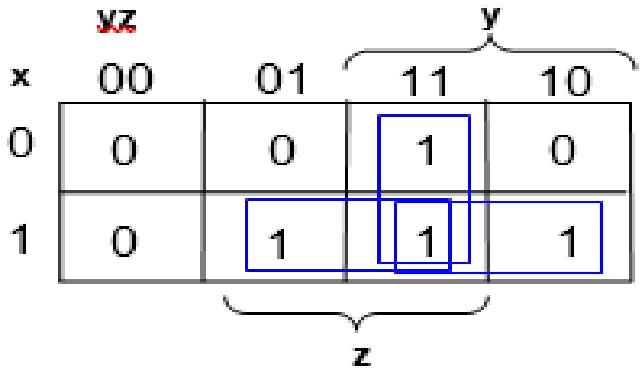
X	Y	Z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

2. Obtain the simplified Boolean functions for each output as a function of the input variables.

Map for output A:

The simplified expression from the map is:

$A = xz + xy + yz$

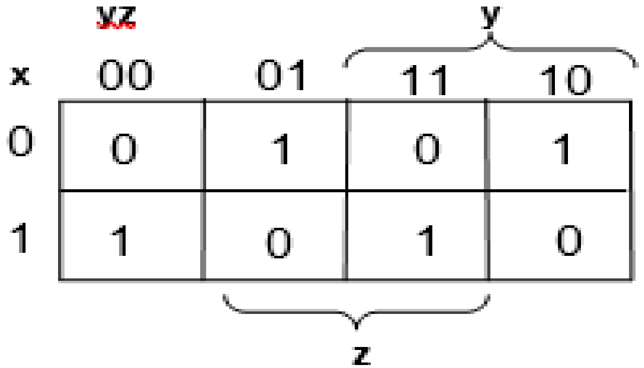


x \ yz	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Map for output B:

The simplified expression from the map is:

$B = x'y'z + x'yz' + xy'z' + xyz$

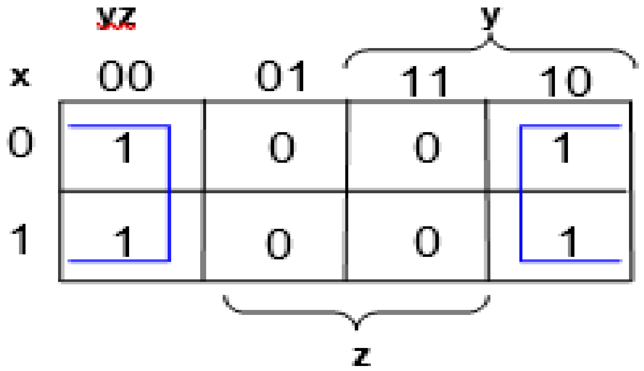


x \ yz	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Map for output C:

The simplified expression from the map is:

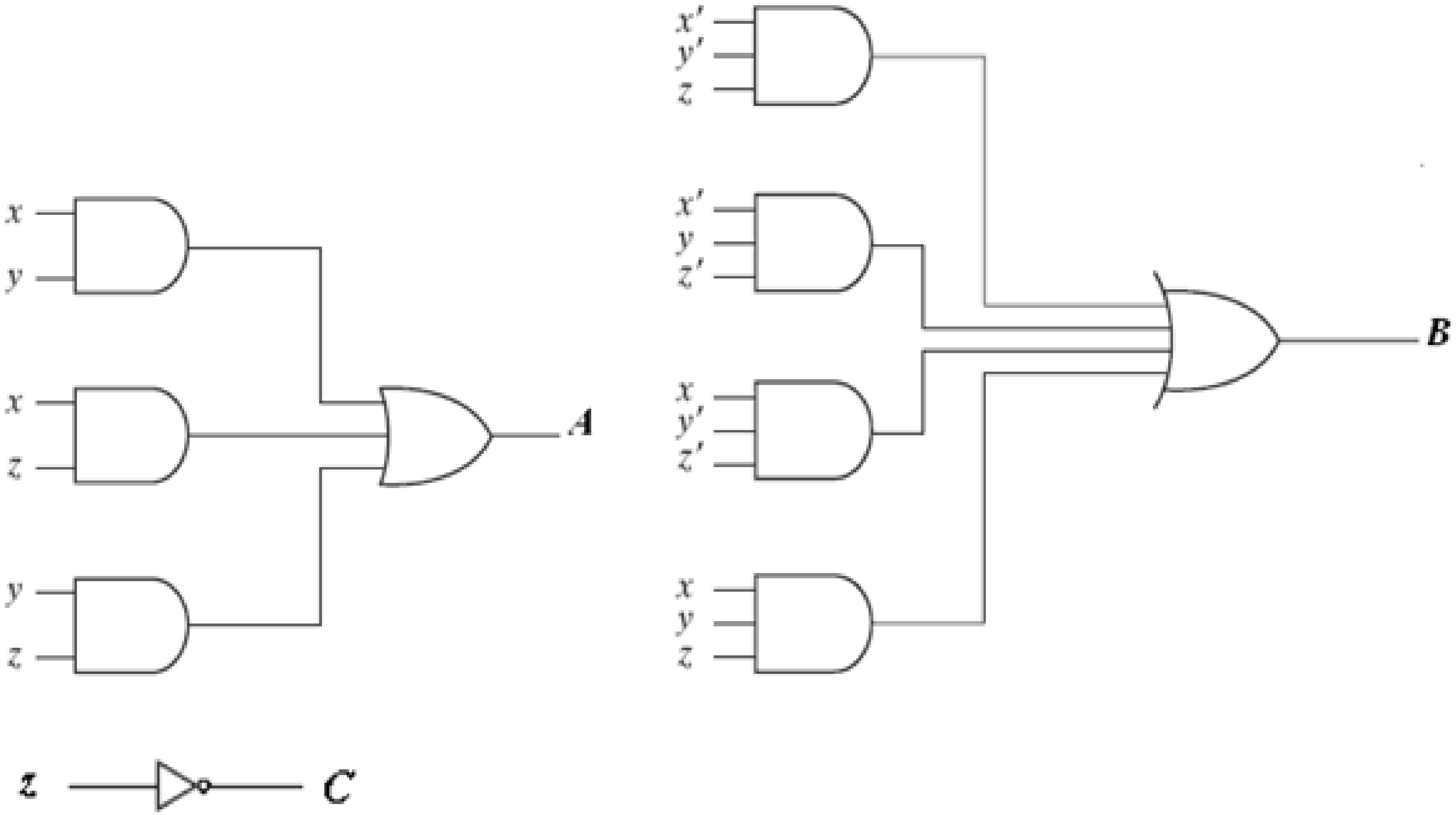
$C = z'$



x \ yz	00	01	11	10
0	1	0	0	1
1	1	0	0	1

3. Draw the logic diagram.

$$A = xy + xz + yz$$
$$B = x'y'z + x'yz' + xy'z' + xyz$$
$$C = z'$$

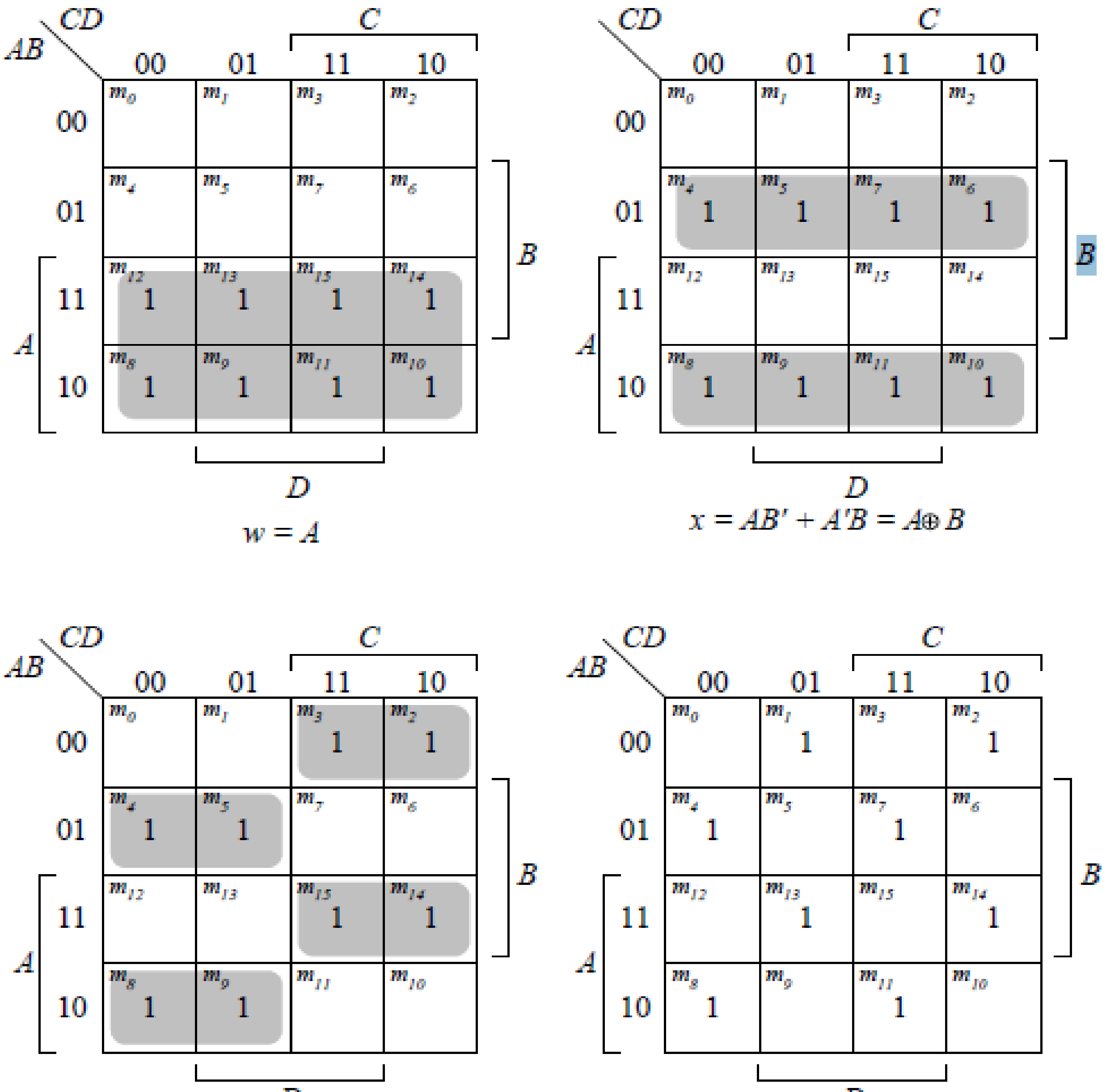


Problem 4-7

Design a combinational Circuit that converts 4-bit Gray code to 4-bit Binary code. Implement the circuit using exclusive-OR gates.

(a)

ABCD	*wxyz*
0000	0000
0001	0001
0011	0010
0010	0011
0110	0100
0111	0101
0101	0110
0100	0111
1100	1000
1101	1001
1111	1010
1110	1011
1010	1100
1011	1101
1001	1110
1000	1111



AB \ *CD*	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4	m_5	m_7	m_6
11	m_{12} 1	m_{13} 1	m_{15} 1	m_{14} 1
10	m_8 1	m_9 1	m_{11} 1	m_{10} 1

$w = A$

AB \ *CD*	00	01	11	10
00	m_0	m_1	m_3	m_2
01	m_4 1	m_5 1	m_7 1	m_6 1
11	m_{12}	m_{13}	m_{15}	m_{14}
10	m_8 1	m_9 1	m_{11} 1	m_{10} 1

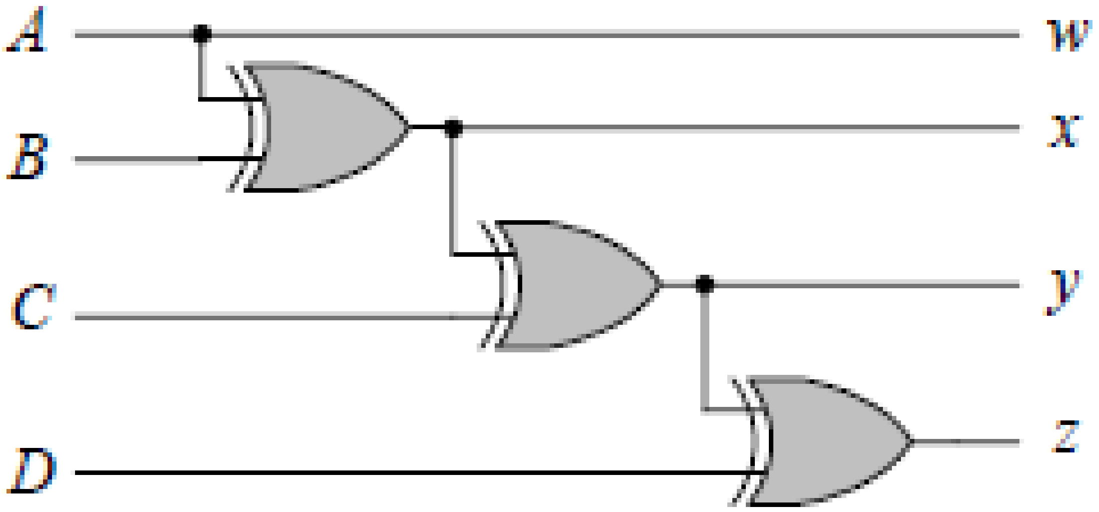
$x = AB' + A'B = A \oplus B$

AB \ *CD*	00	01	11	10
00	m_0	m_1	m_3 1	m_2 1
01	m_4 1	m_5 1	m_7	m_6
11	m_{12}	m_{13}	m_{15} 1	m_{14} 1
10	m_8 1	m_9 1	m_{11}	m_{10}

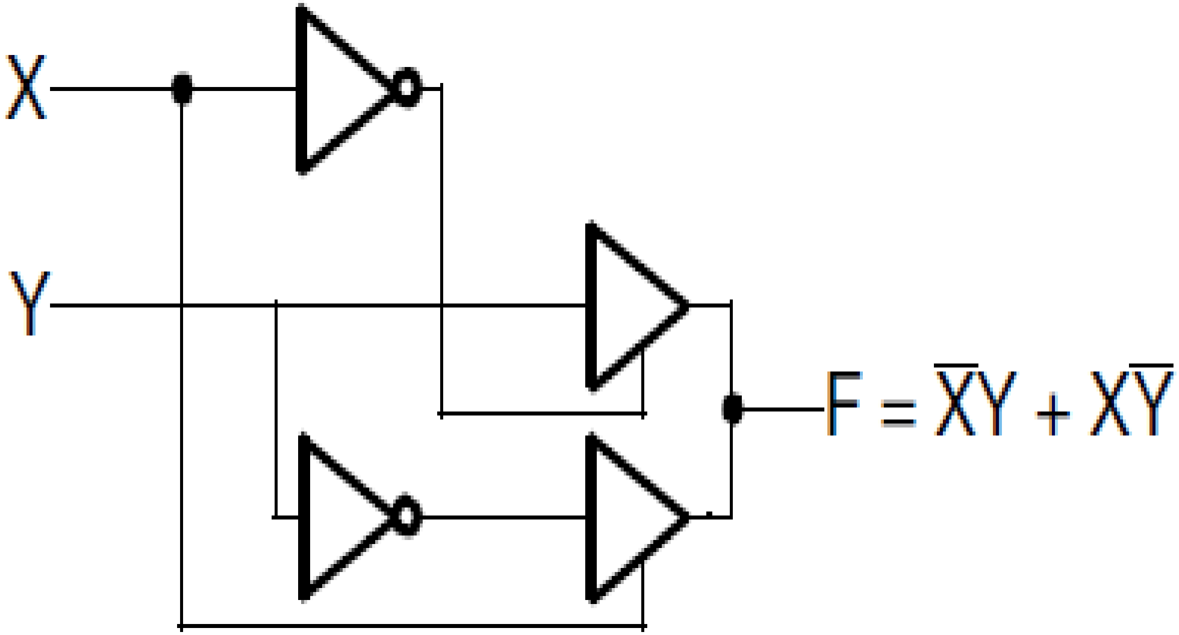
AB \ *CD*	00	01	11	10
00	m_0	m_1 1	m_3	m_2 1
01	m_4 1	m_5	m_7 1	m_6
11	m_{12}	m_{13} 1	m_{15}	m_{14} 1
10	m_8 1	m_9	m_{11} 1	m_{10}

$$
\begin{aligned}
y &= A'B'C\ \ A'BC' + ABC + AB'C' \\
&= A'(A \oplus B) + A(B \oplus C)' \\
&= A \oplus B \oplus C \\
&= X \oplus C
\end{aligned}
$$

$$
\begin{aligned}
z &= A \oplus B \oplus C \oplus D \\
&= y \oplus D
\end{aligned}
$$



Problem Implement the exclusive-OR function with two tri-state gates and NOT gates.



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