EE-421: Digital System Design

Circuit Timing

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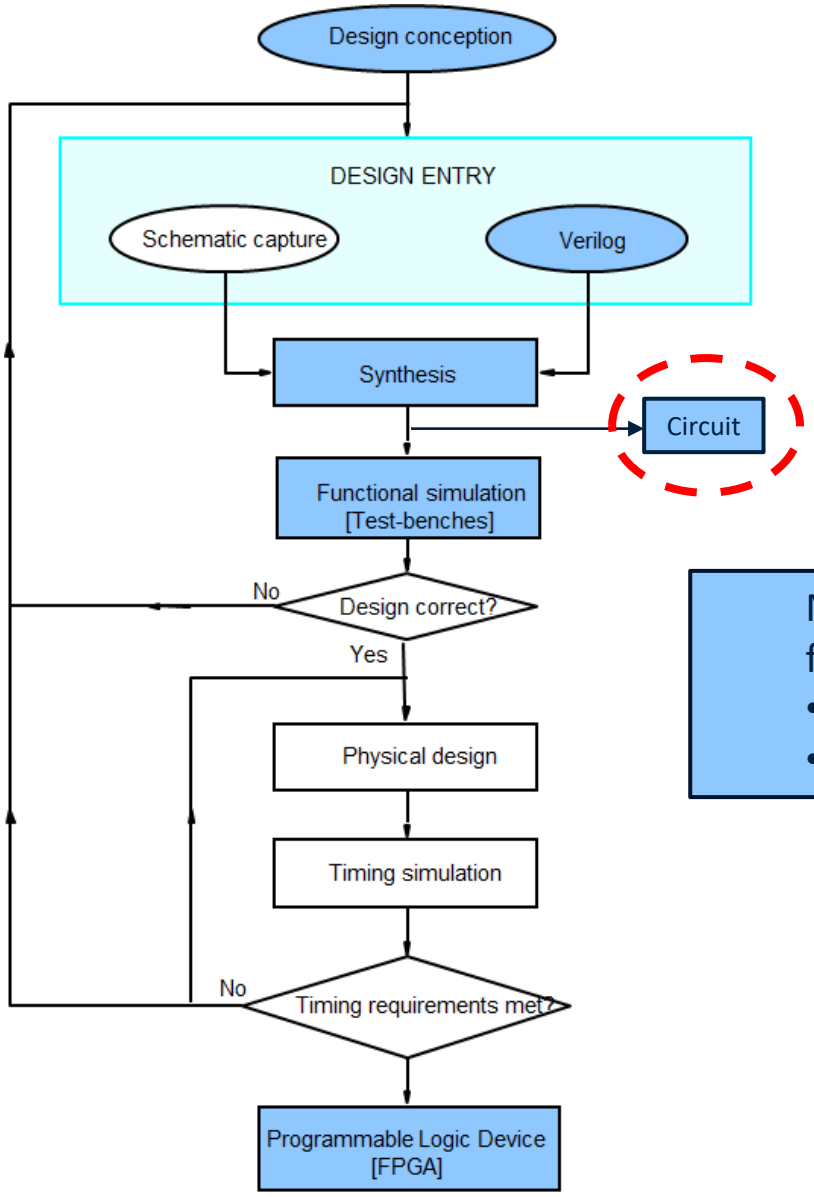
Where are we Heading?



More specifically, we'll focus on the following circuit attributes:

- Circuit Timing
- Metastability

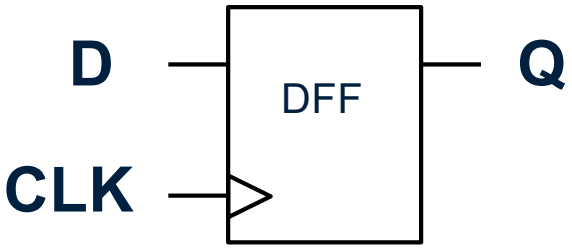
Flip-Flop Timing Constraints

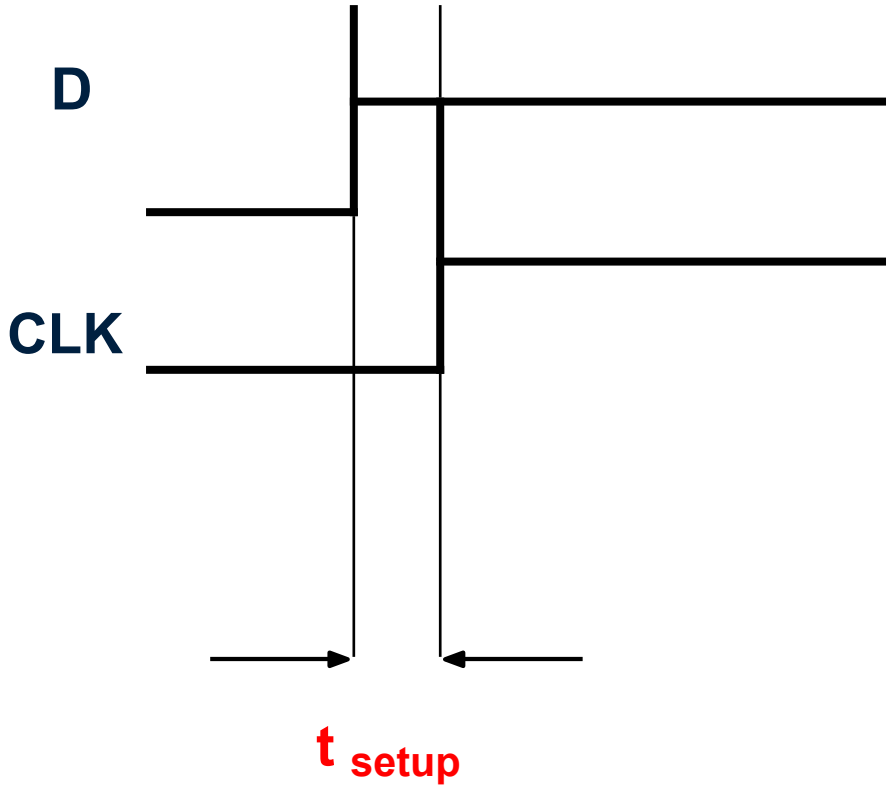
Flip-flop Timing Constraints

- Flip-Flop Timing Constraints:
  - Clock-to-Q Delay
  - Setup Time
  - Hold Time

Setup Time

- Input to flip-flop cannot change for a certain amount of time **PRIOR** to clock rising-edge.

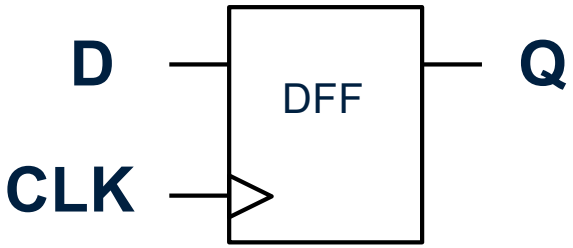


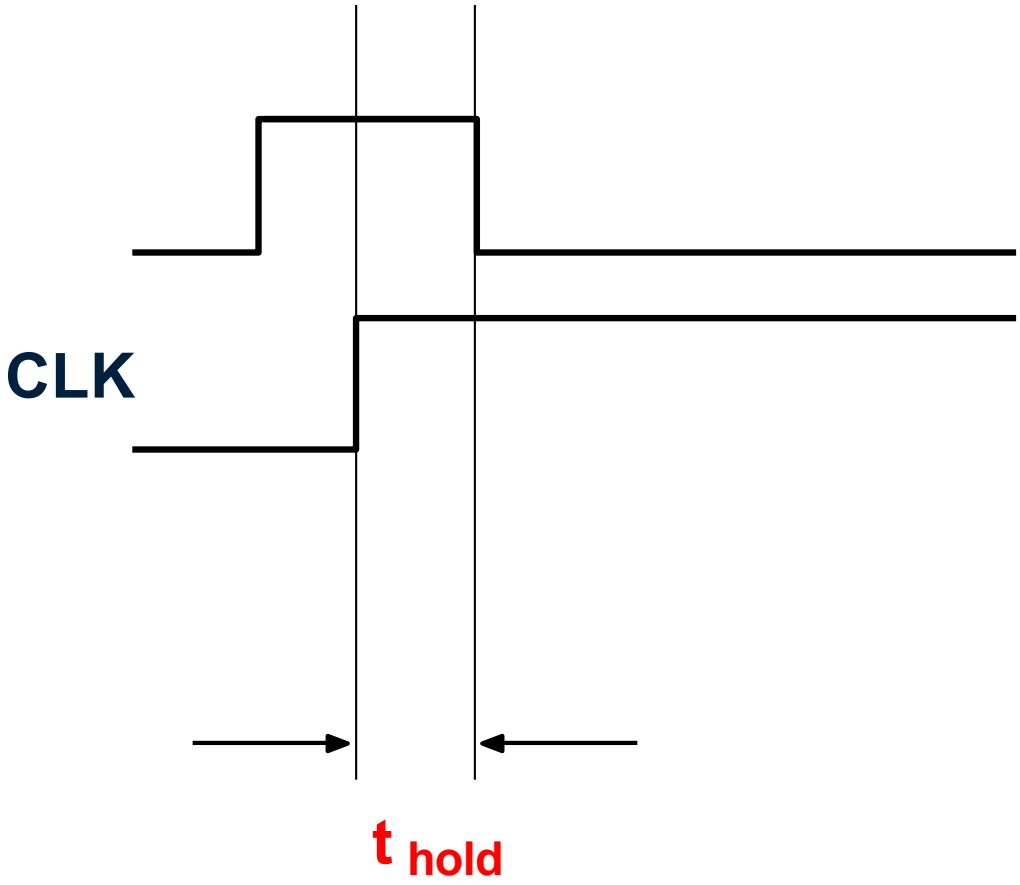


Time for input to propagate “into” the flip-flop before clock arrives

Hold Time

- Input to flip-flop cannot change for a certain amount of time **AFTER** clock rising-edge.

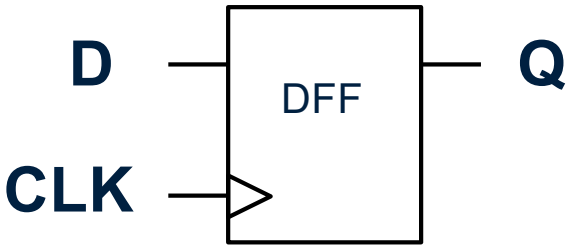


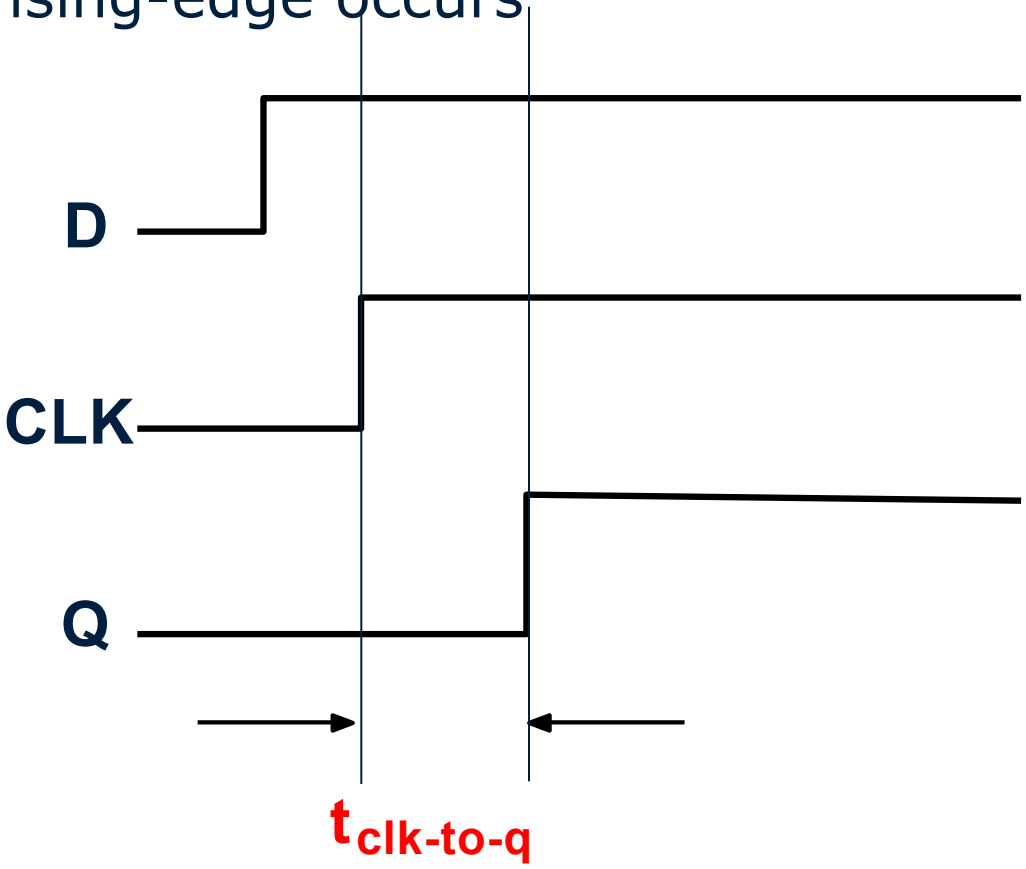


Time for flip-flop to fully read input before the value is “taken away”

Clock-to-Q Delay

- The time that it takes for the output of a Flip-Flop to settle after the clock rising-edge occurs





Note: the delay may not be exactly the same for the cases when Q changes from 1 to 0 or 0 to 1. Therefore, clk-to-q delay is often given as a max and a min value.

Summary of Flip-Flop Timing