EE-421: Digital System Design

Course Introduction
&
Logistics

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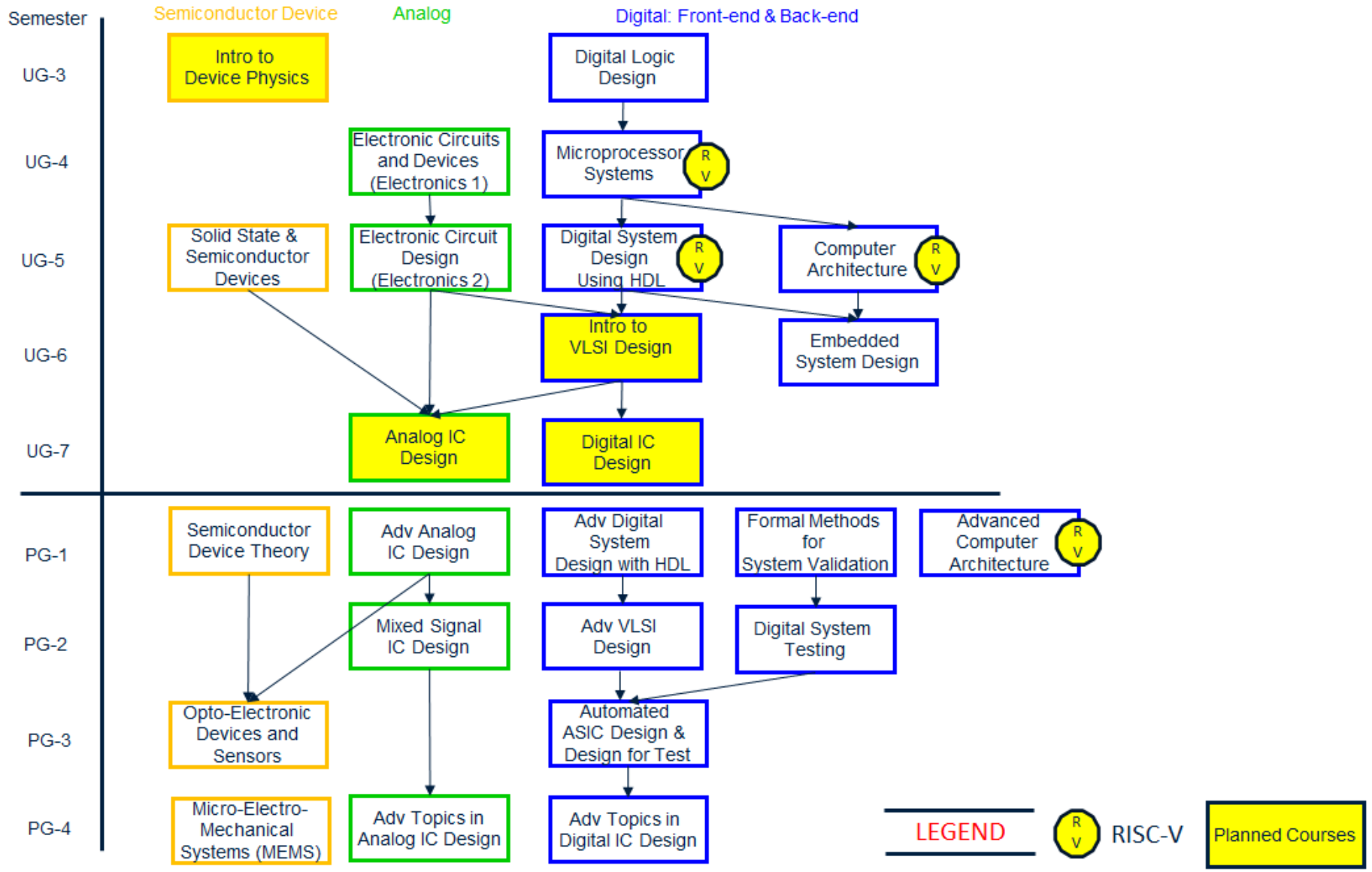
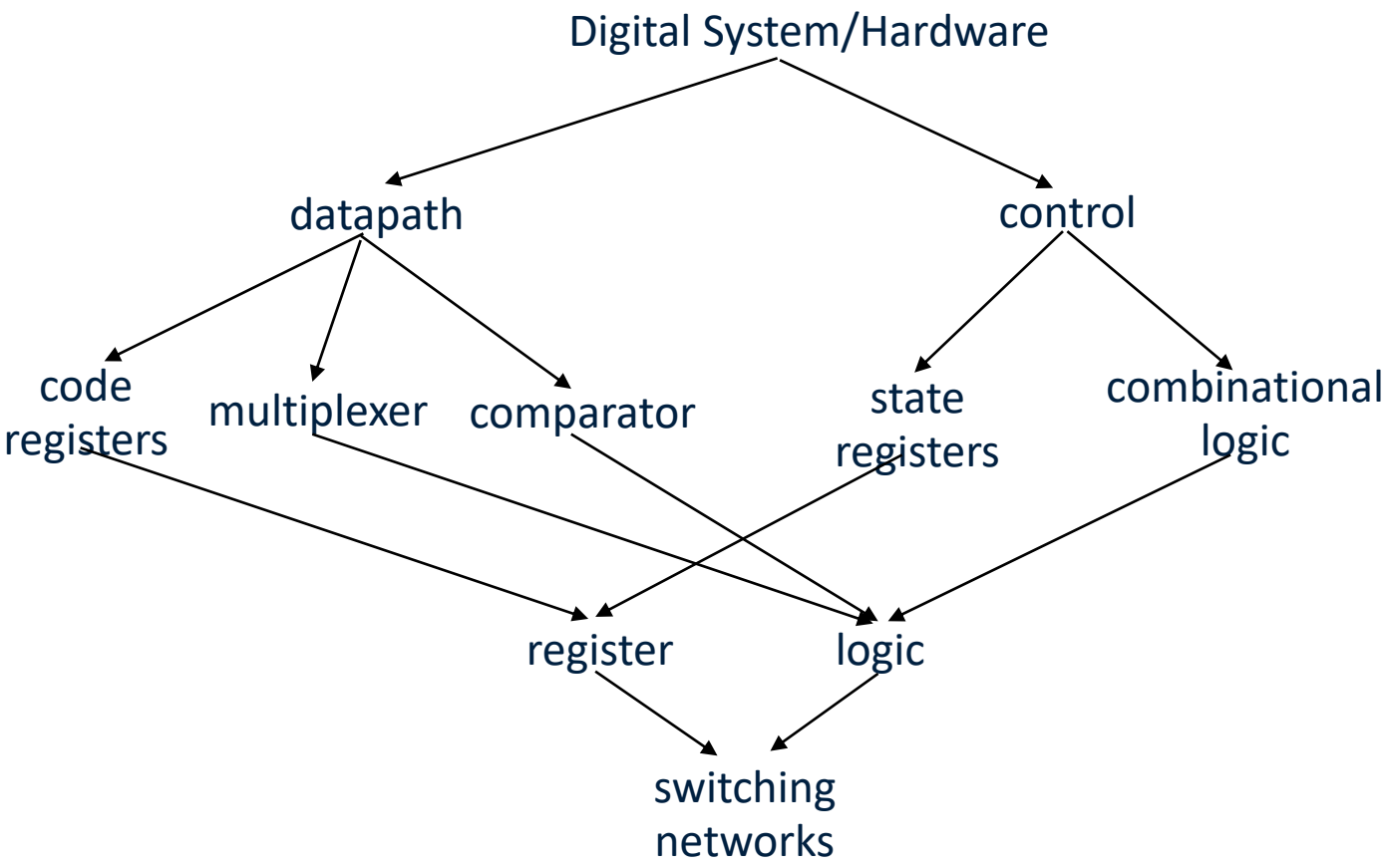
NUST
SCHOOL OF ELECTRICAL ENGINEERING &
COMPUTER SCIENCE (SEECS)

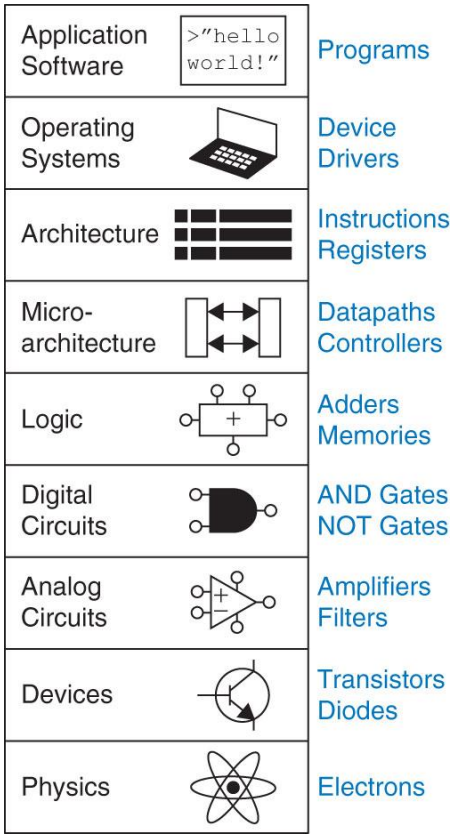
DSD Course Placement and Importance



Recall: Digital Hardware/System Hierarchy

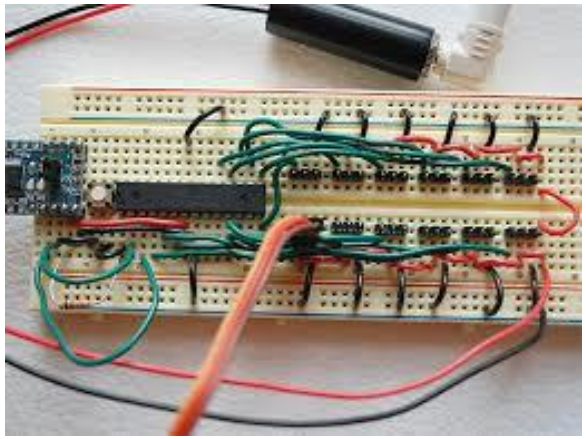
- Logic circuits are used to build computer hardware, as well as many other types of products:
  - All such products are broadly classified as digital hardware



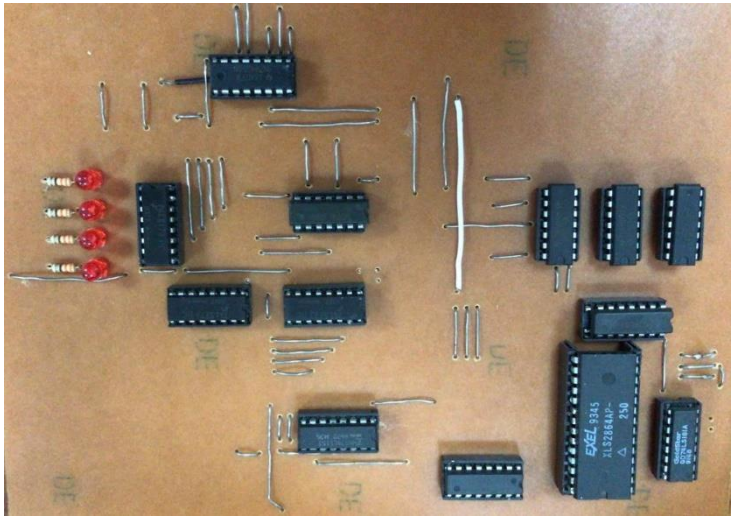


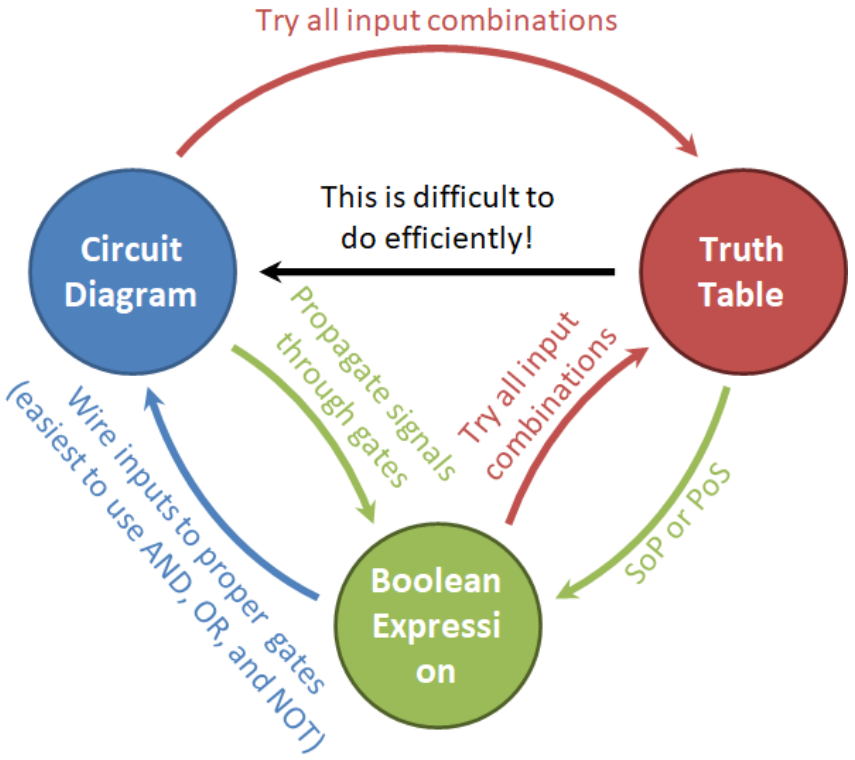
Did you build Digital Hardware Before?

- Your DLD Labs



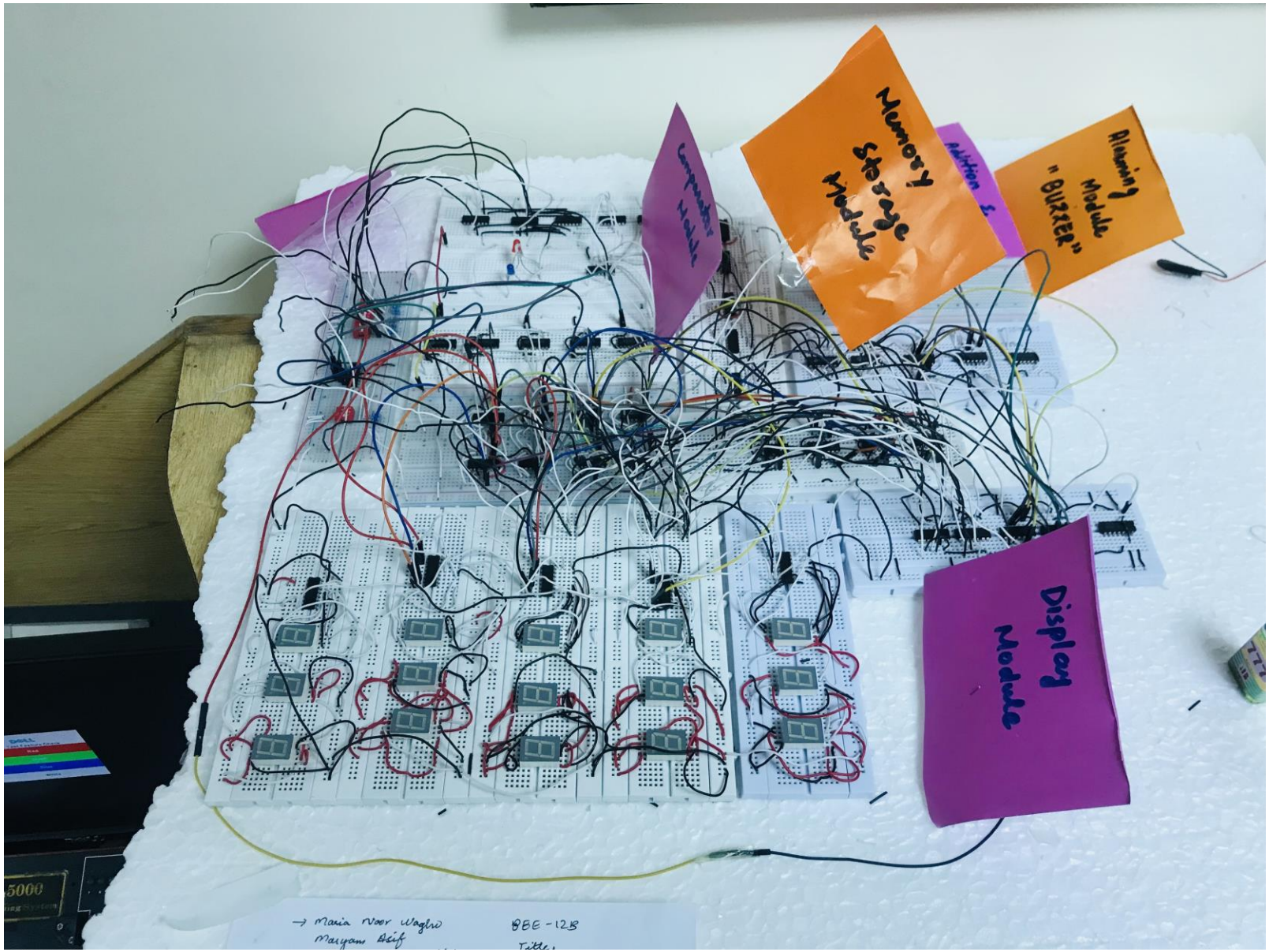
- MPS Assignments





What's limiting in this approach?

Your Digital Circuits from DLD



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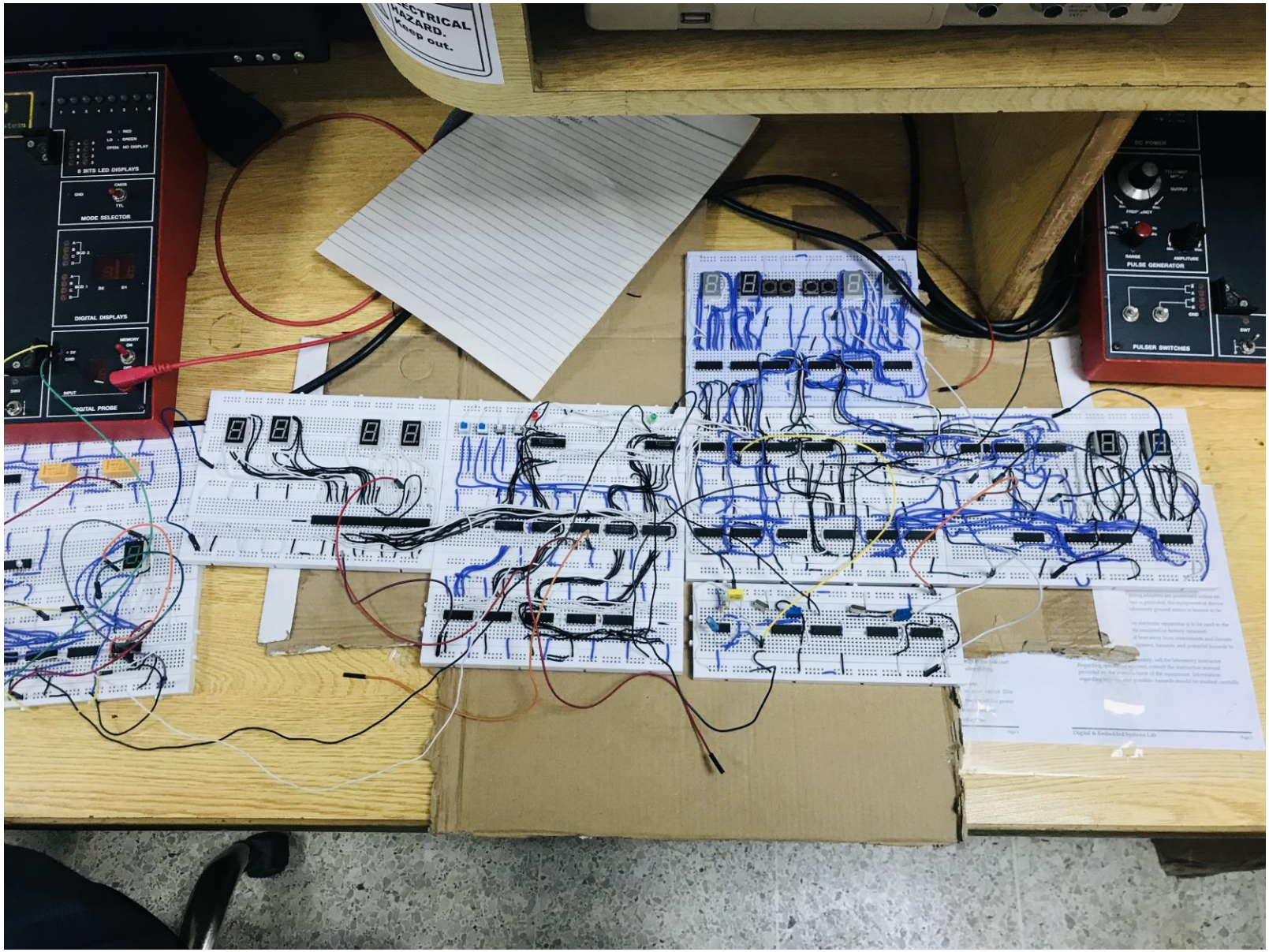

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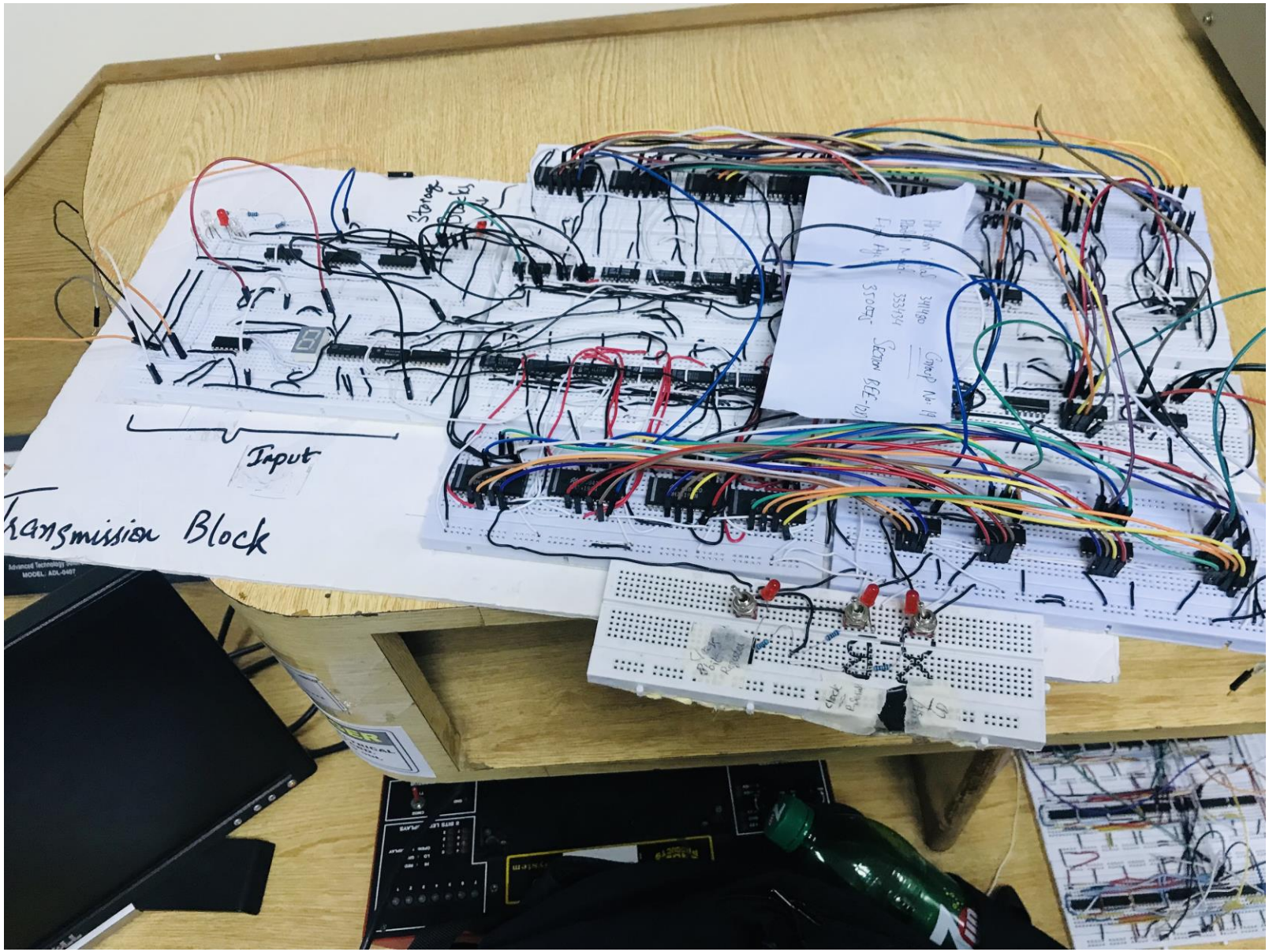
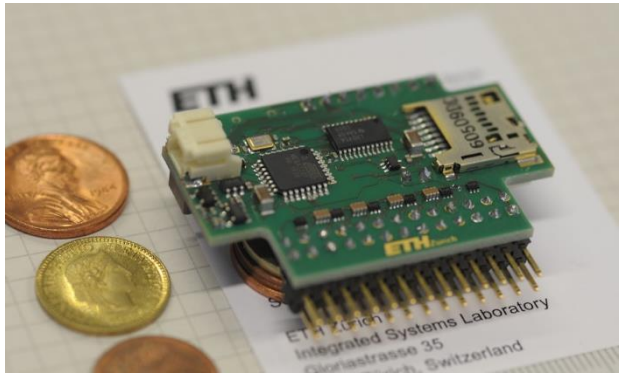
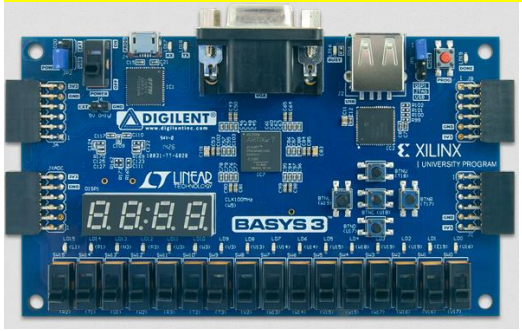


Computing Platforms for Digital Systems

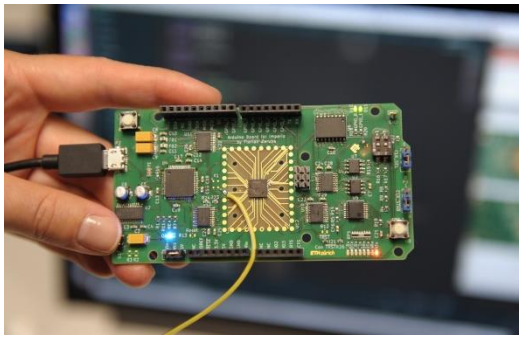
Microprocessor and Microcontroller



Field **P**rogrammable **G**ate **A**rray [FPGA]



Application **S**pecific **I**ntegrated **C**ircuit [ASIC]



They All Look the Same

	Microprocessors	FPGAs	ASICs
			
In short:	Common building block of computers	Reconfigurable hardware, flexible	You customize everything

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Program Development Time	minutes	days	months
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Good for	Ubiquitous Simple to use	Prototyping Small volume	Mass production, Max performance
Programming	Executable file	Bit file	Design masks
Languages	C/C++/Java/…	Verilog/VHDL	Verilog/VHDL
Main Companies	Intel, ARM, AMD	Xilinx, Intel (Altera), Lattice, Microsemi	TSMC, UMC, ST, Globalfoundries

Course Goal and Game Plan

	Microprocessors	FPGAs	
			
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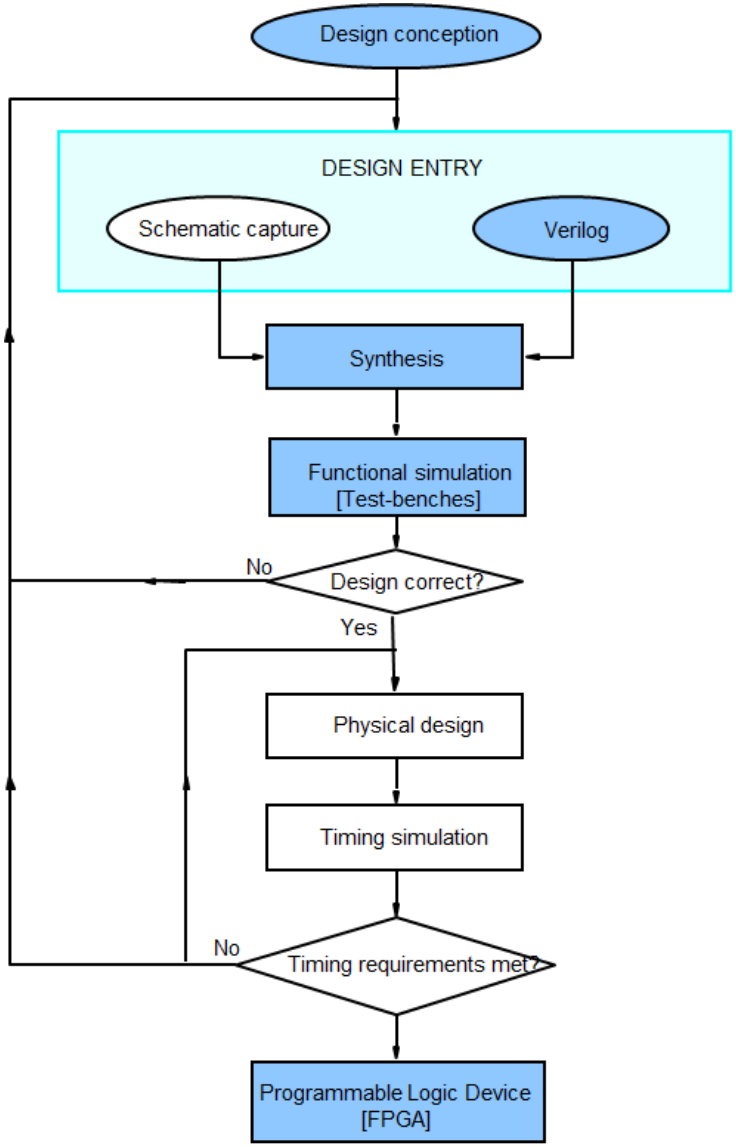
Want to build Digital Hardware By programming these

Using this language

What this Course is About: Bird's-Eye View



Overall, this course is about the *art* of designing digital circuits using *modern CAD-tool-based* methods.

Broad topics include, but not limited to:

- FPGA architecture
- Describing hardware using Verilog (Synthesis focused)
  - Combinational and Sequential design
  - Key logic elements such as storage, clocks, and memory
  - How to implement finite state machines in circuitry
- Designing circuits to perform arithmetic calculations
- Building complex designs from multiple functions and FPGA IP
- Power-Performance-Area (PPA)
- Bus Architecture(s)
- FPGA System-on-Chip (SoC) [Soft + Hard up]
- Case Designs + Case Studies

Some Goals of This Course

- Teach/enable/empower you to:
  - **Understand** the principles of digital design
  - **Learn** how digital systems are designed using HDL
  - **Learn** to systematically design increasingly complex digital designs
  - **Understand** how to **analyze** and **make tradeoffs** in a digital design

What Do I Expect From You?

- Required background in Digital Logic Design course:
  - Fundamentals concepts in classical *manual* digital design:
    - Truth tables
    - Logic gates and networks
      - Synthesis using universal gates
      - SOP and POS
    - Logic Optimization
      - Boolean algebra
    - Target implementation platform:
      - Digital IC 7400-series
    - Combinatorial Logic
    - Sequential Logic
    - State Machines

Though manual techniques are not used for complex designs,

- **but grips on fundamentals give an intuitive feeling for how digital circuits operate**

What Do I Expect From You?

- Enthusiasm, Dedication and Honesty!!!
- How you prepare and manage your time is very important !!!
- There will be heavy assignments:
  - They **will** take time
  - Start early, work hard
- This **will** be a **heavy** course
  - However, you will learn a lot of fascinating topics
  - And, it will hopefully change how you look at and think about designs around you

Lastly, What Do I Expect From You?

- Learn the material thoroughly
  - attend lectures, do the readings, do the exercises, do the labs
- Work hard: this will be a hard but fun & informative course
- Ask questions, take notes, participate
- Perform the assigned readings
- **Come to class on time**
- Start early – do not procrastinate
- If you want feedback, come to office hours

- Remember "**Chance favors the prepared mind**." (Pasteur)

Course Logistics

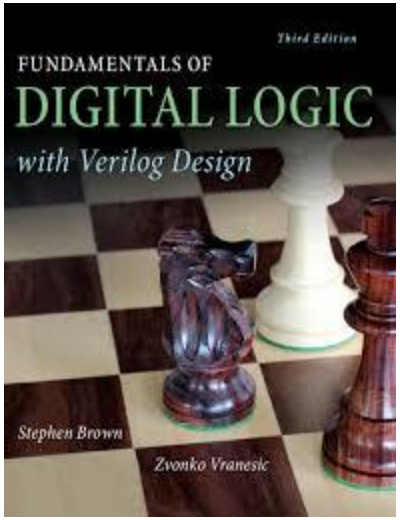
- Lectures:
  - Wednesday
    - 11am-12:50pm in CR-18 IAEC
  - Thursday (Gp-01 & Gp-02 Combined):
    - 12pm-12:50pm in in CR-18 IAEC
  - Course Website: http://lms.nust.edu.pk/
    - Lecture Updates: After every lecture or by the end of week
- Labs:
  - Please refer to the timetable
- Office Hours:
  - By appointment only:
    - send me an email at rehan.ahmed@seecs.edu.pk

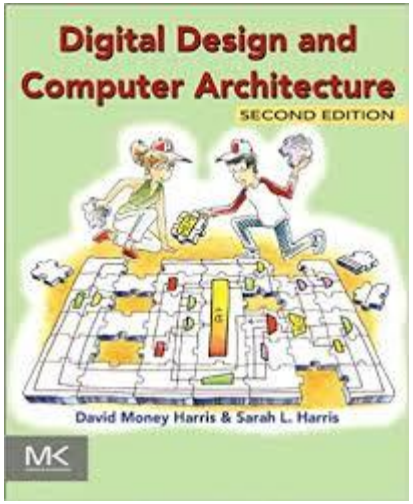
Text and Support Books

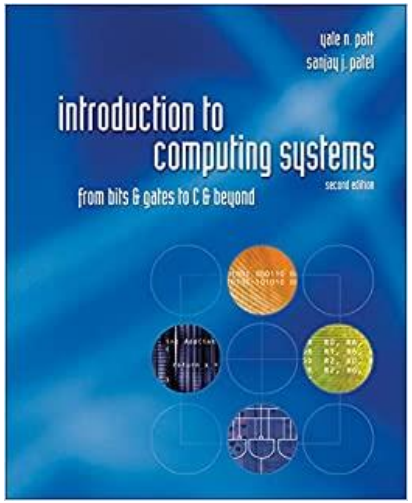
- [main] Digital System Design with Verilog HDL, 3/e, b **S**tephen Brown and **Z**vonko Vranesic. [**S&Z**]

- [ref] Digital Design and Computer Architecture, 2/e, by **H**arris and **S**arah. [**H&S**]

- [ref] Introduction to Computing Systems, Yale. N **P**att & SanjayJ. **P**atel. [**P&P**]







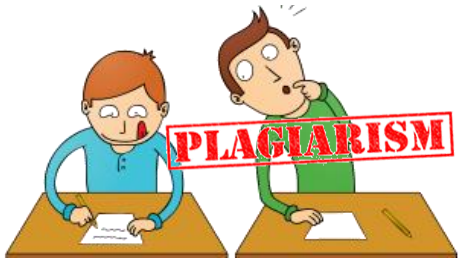
Tentative Grading Scheme

Type	Weight (%)
Assignments	5-10
Quizzes	5-10
MSE	20-30
Labs	10-15
Project	10-15
Final	35-50

- This scheme *will* be adjusted during the semester!

Course Discipline: Ground Rules

- Classroom Etiquettes:
  - Students will be punctual for the class.
    - No attendance if you are late more than 5 mins.
  - If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended.
  - All the cell phones must be switched OFF prior to entering the class room.
- Academic Honesty and Plagiarism: [Both in Class and Labs]
  - Plagiarism is considered a serious offence by the university and severe penalties apply.
  - ZERO tolerance. Subject activity will be nullified.



Recommended Reading

- S&Z, Chapter-1 and 2.9

THANK YOU