EE-421: Digital System Design

Programmable Logic Devices: FPGA

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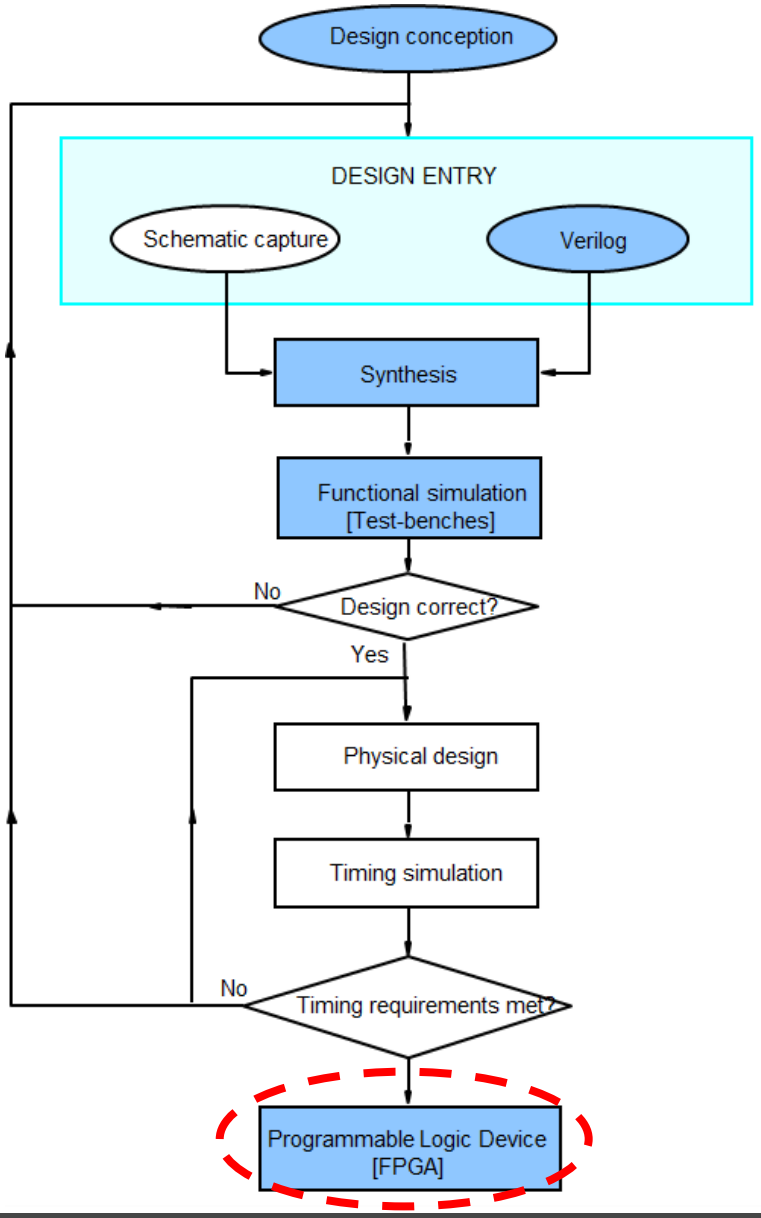
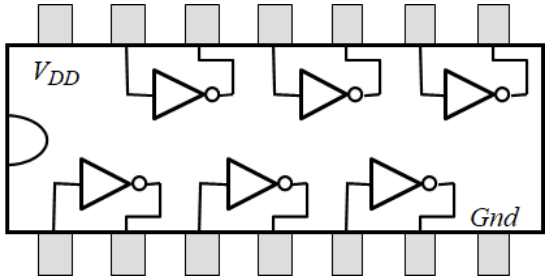
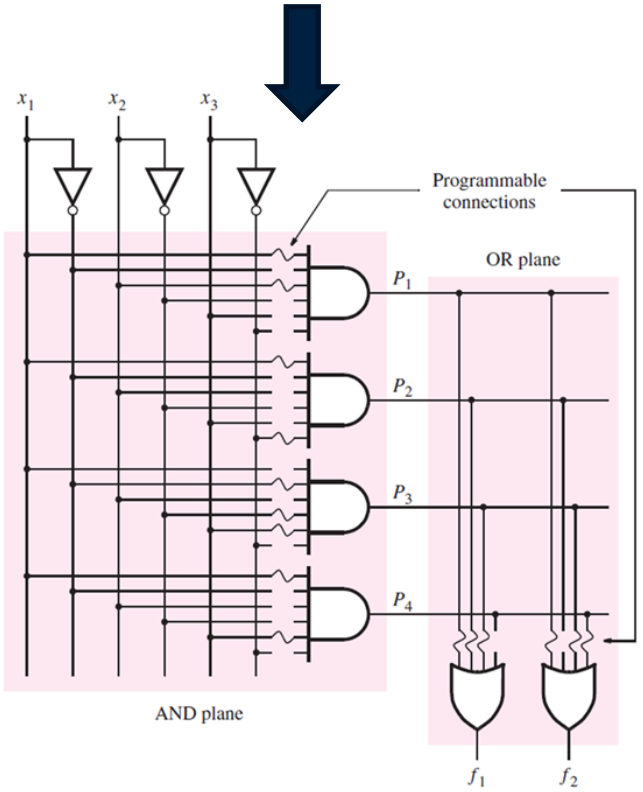
Where are we Heading?

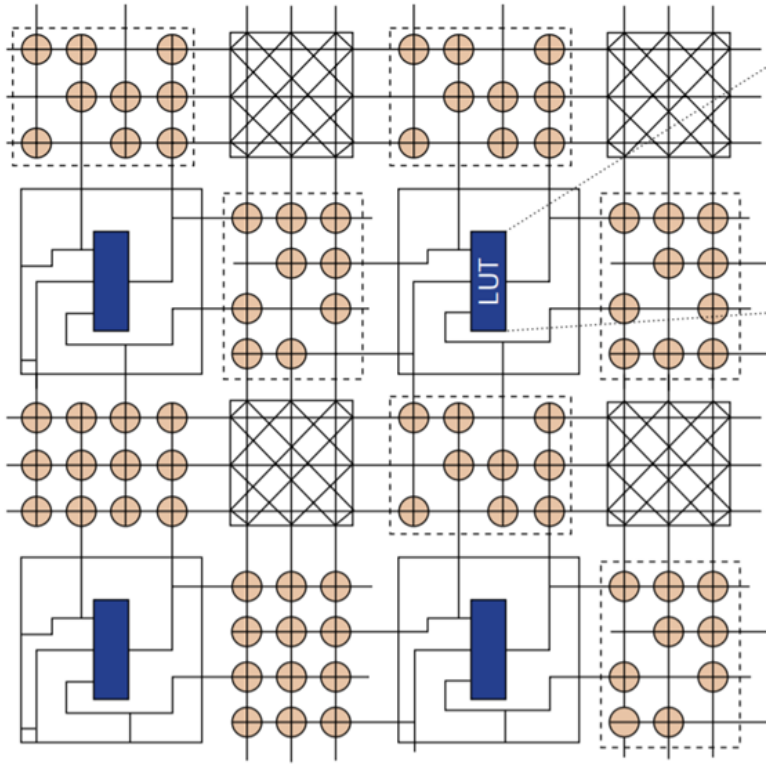


Programmable Logic Devices (computing platforms):





How did we get here?



Programmable Logic Devices: FPGA

FPGA CAD and Architecture

- The main focus of this slide set is:
  - What the architecture of an FPGA look like?

- Do we care? The tools shield us pretty well from the internals.

- But, it helps to understand what is going on under-the hood

- Important when you are selecting an FPGA for a project

FPGAs are available from Several Companies

- Market leaders, about equal ($2B+/year):
  - Intel (former Altera): tools are easy to use, future FPGAs w/ Intel
  - Xilinx: "power user" tools, future FPGAs w/ TSMC
- Second tier, about equal ($250M+/year):
  - Microsemi: non-volatile, very low power, radiation hardened
  - Lattice Semiconductor: focusing on mobile, low power, small, low cost
- Others (smaller, but established) :
  - Cypress, Quicklogic, Atmel, …

What is an FPGA?

- Field Programmable Gate Array [FPGA]:
  - is an Integrated Circuit (IC) that can be programmed in the field *after* manufacturing.

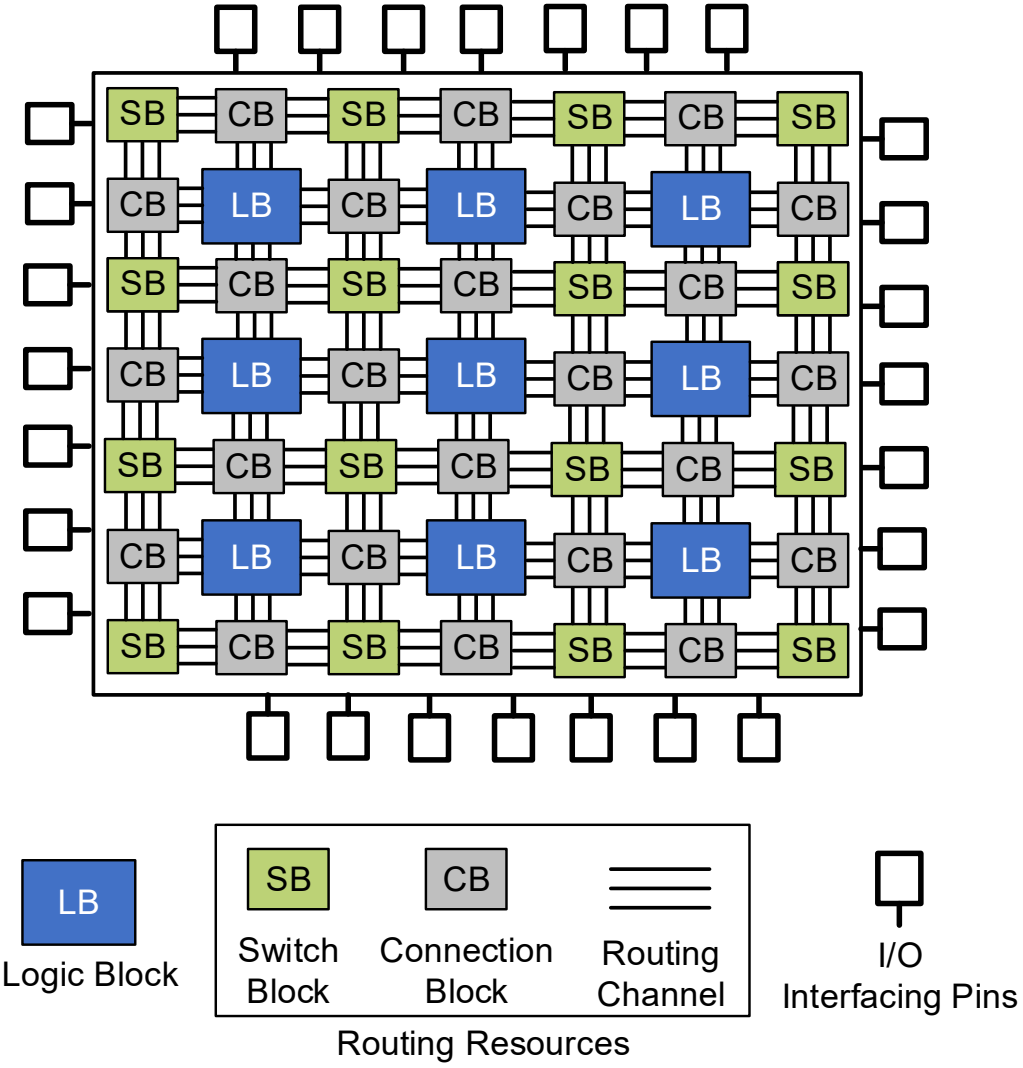
- FPGA is a reconfigurable substrate
  - Reconfigurable functions
  - Reconfigurable interconnection of functions
  - Reconfigurable input/output (IO)
  - User can implement *any* digital circuit on it

- FPGAs fill the gap between software and hardware
  - Achieves higher performance than software
  - Maintains more flexibility than hardware

- Industrial Benefits:
  - No high cost of fabrication
  - Narrow Time-to-Market

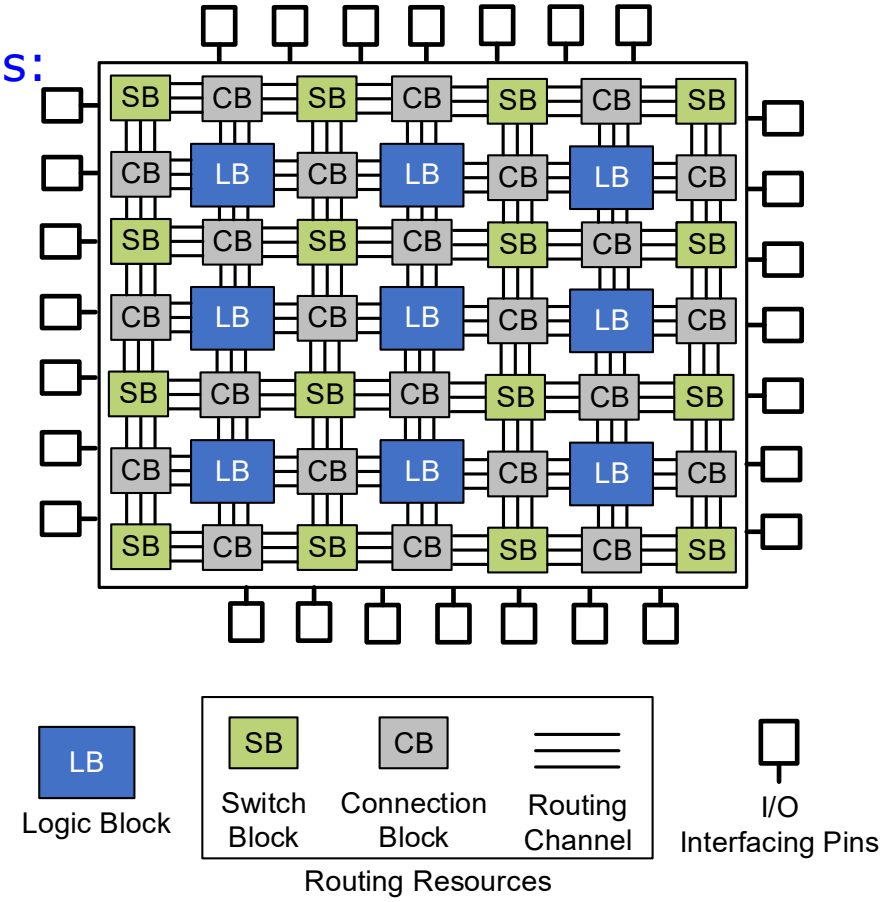
What's Inside an FPGA?

- **F**ield **P**rogrammable **G**ate **A**rray [FPGA]



What's Inside an FPGA?

- Composed of three main types of resources:
  1. Logic-Block [LB]:
     - Implements logic functions
  2. Programmable Routing Resources:
     - Switch-Block [SB]:
       - Connects incident wires
     - Connection-Block [CB]:
       - Connects LB to wires
  3. I/O Interfacing Pins:
     - interface off-chip
       - Multi I/O standards

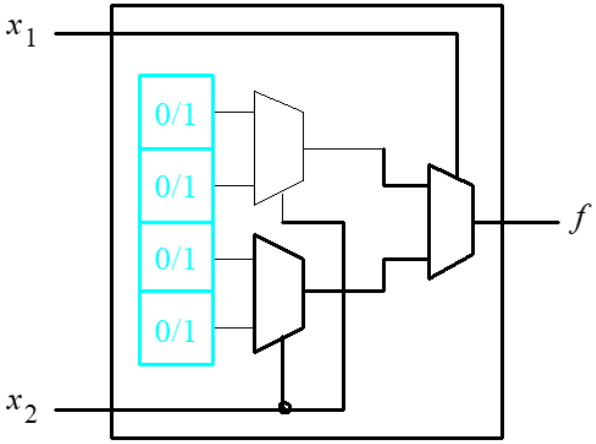


Programmable Logic-Block

- A logic block is a basic component that can be programmed with any kind of logic function.
- These logic blocks are organized in a two-dimensional array and are interconnected with programmable routing channels.
- Thus, a complete digital circuit is implemented by programming each of these logic blocks with parts of the logic functions making up the complete circuit.

What's inside a Logic-Block?

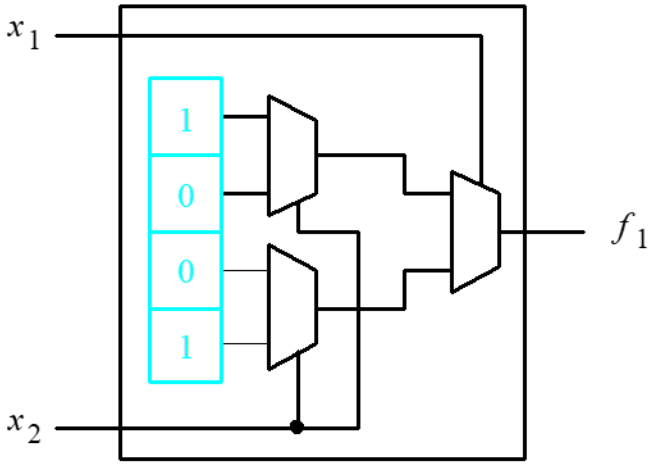
- Inside a Logic-Block is a lookup table (LUT):
  - that contains storage cells to store the Truth-Table of a logic function



(a) Circuit for a two-input LUT

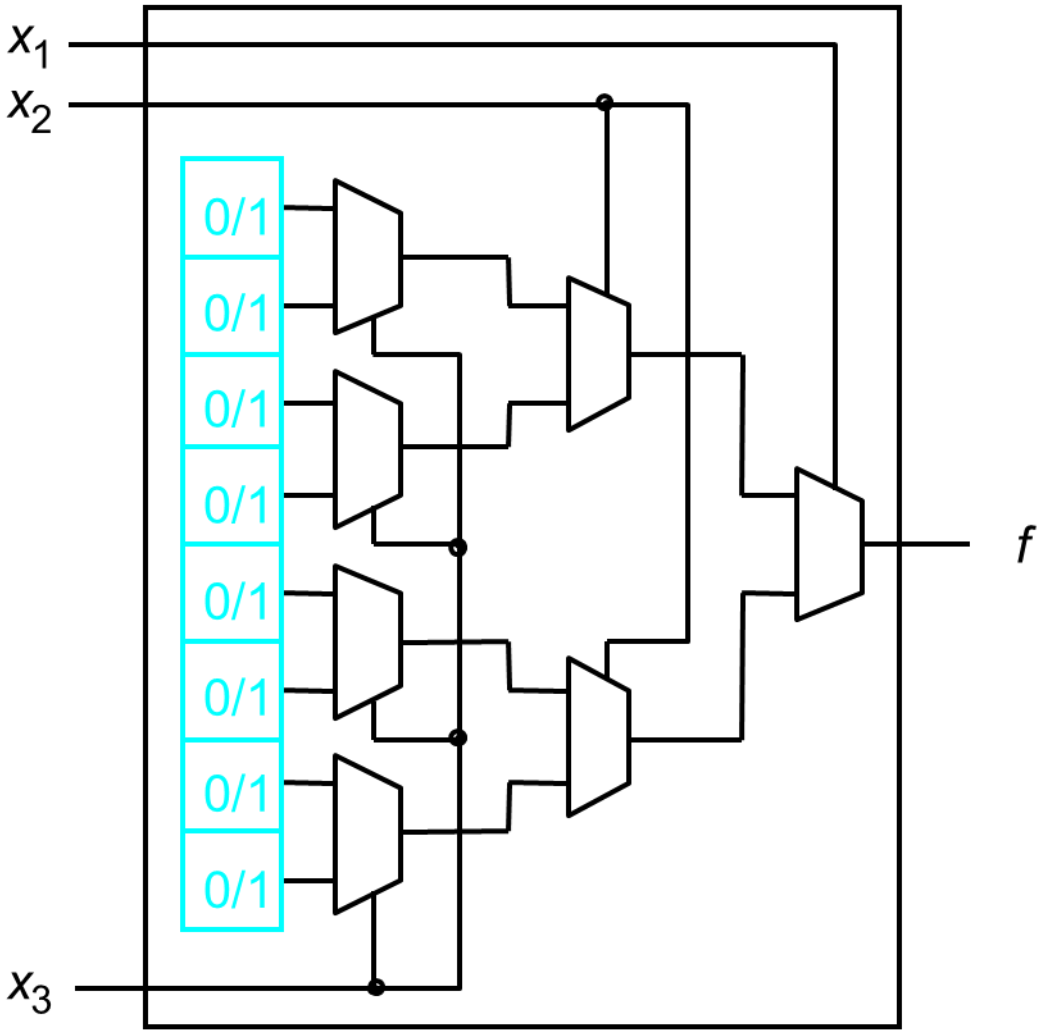
x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1\bar{x}_2 + x_1x_2$



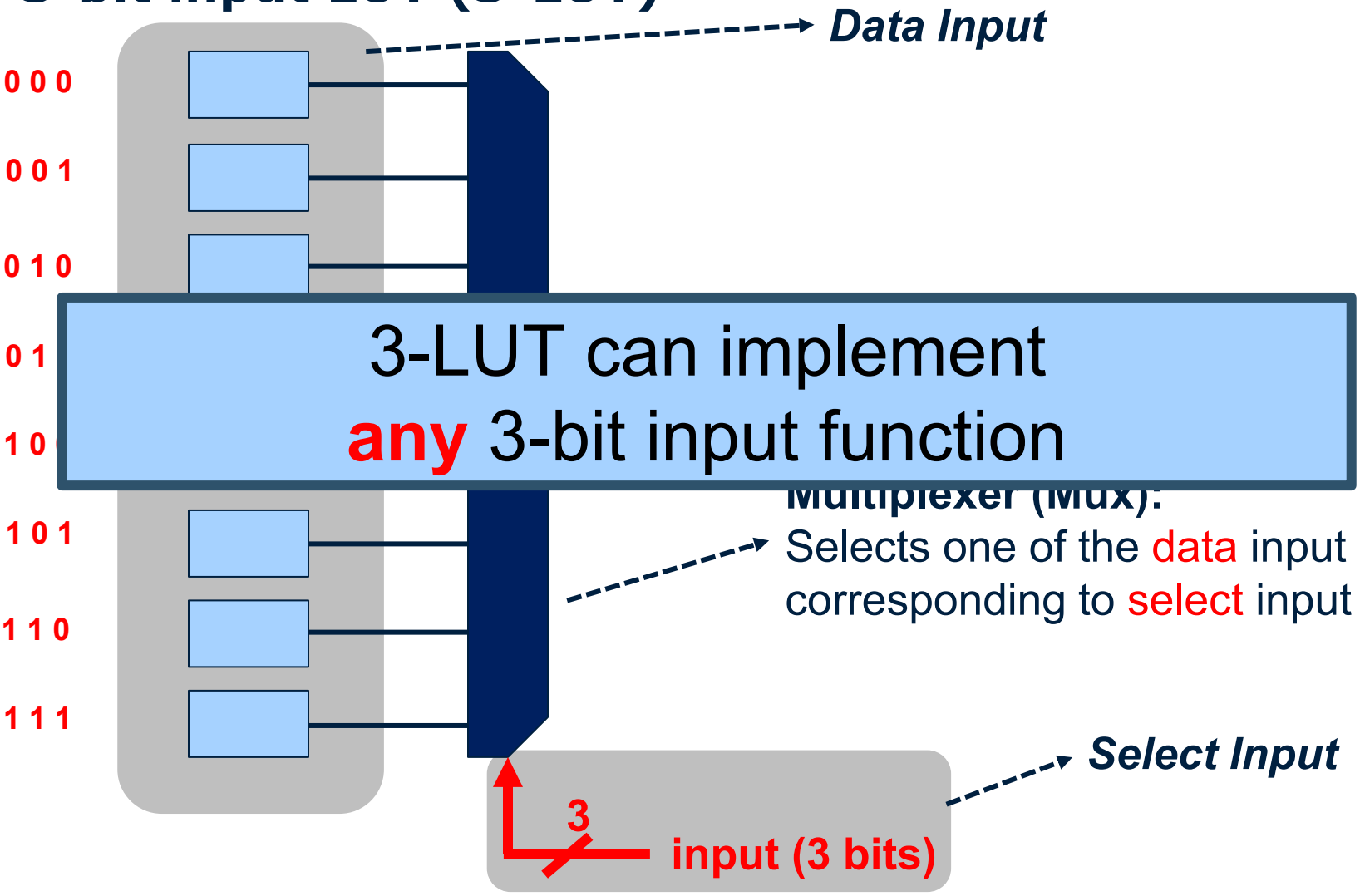
(c) Storage cell contents in the LUT

A Three-Input LUT



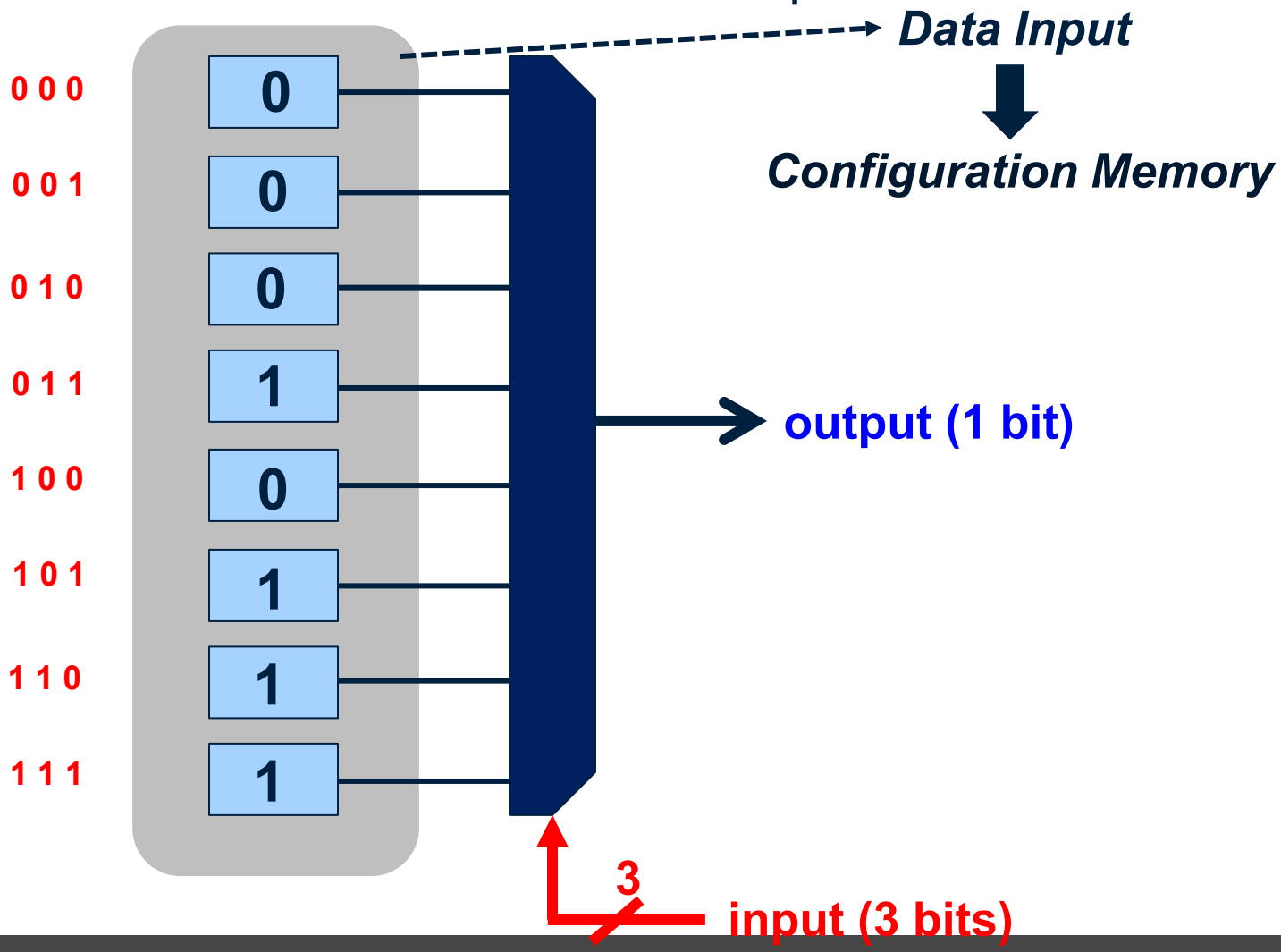
How Do We Program LUTs?

- **3-bit input LUT (3-LUT)**



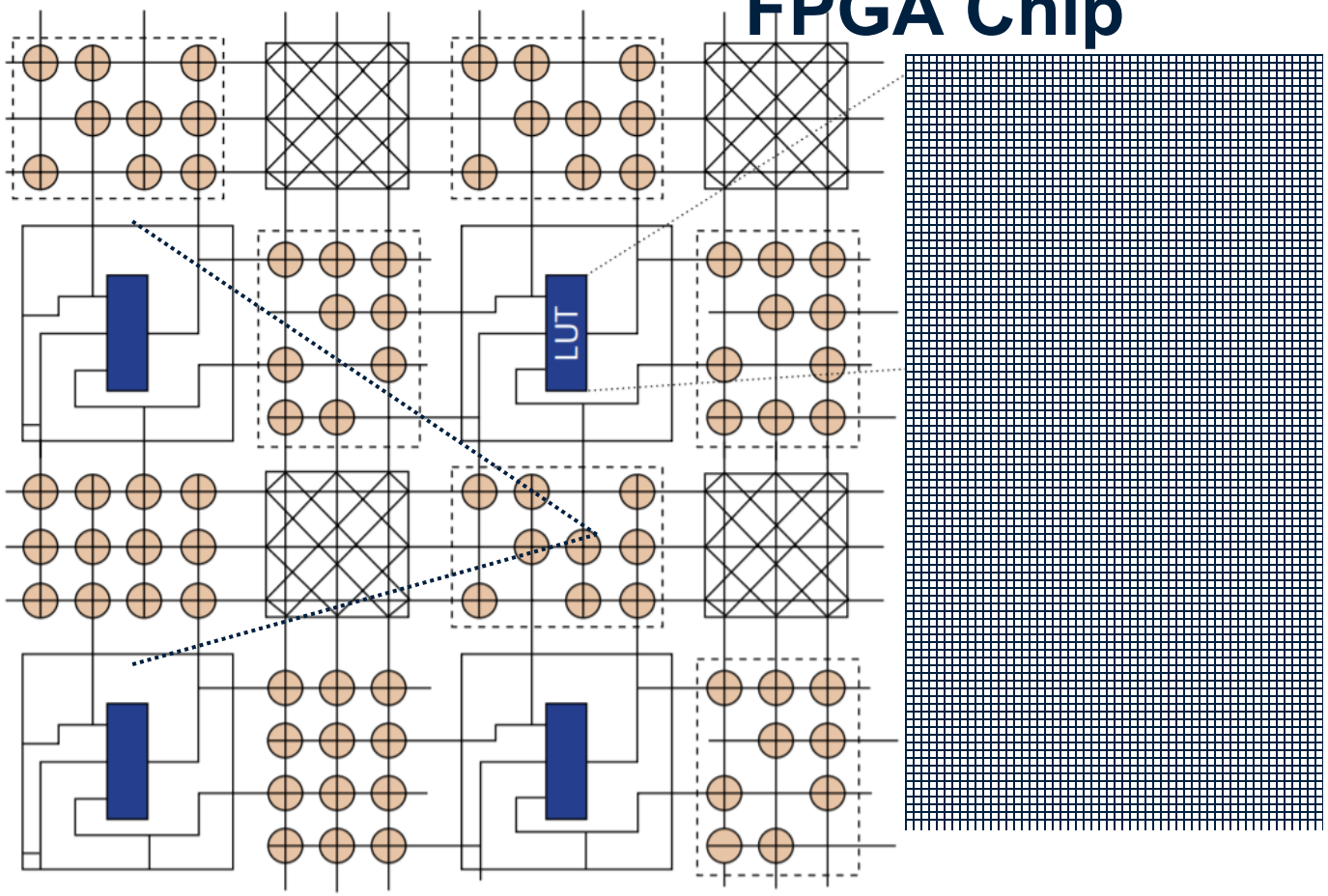
An Example of Programming a LUT

- Let's implement a function that outputs '1' when there are more than one '1' in select inputs



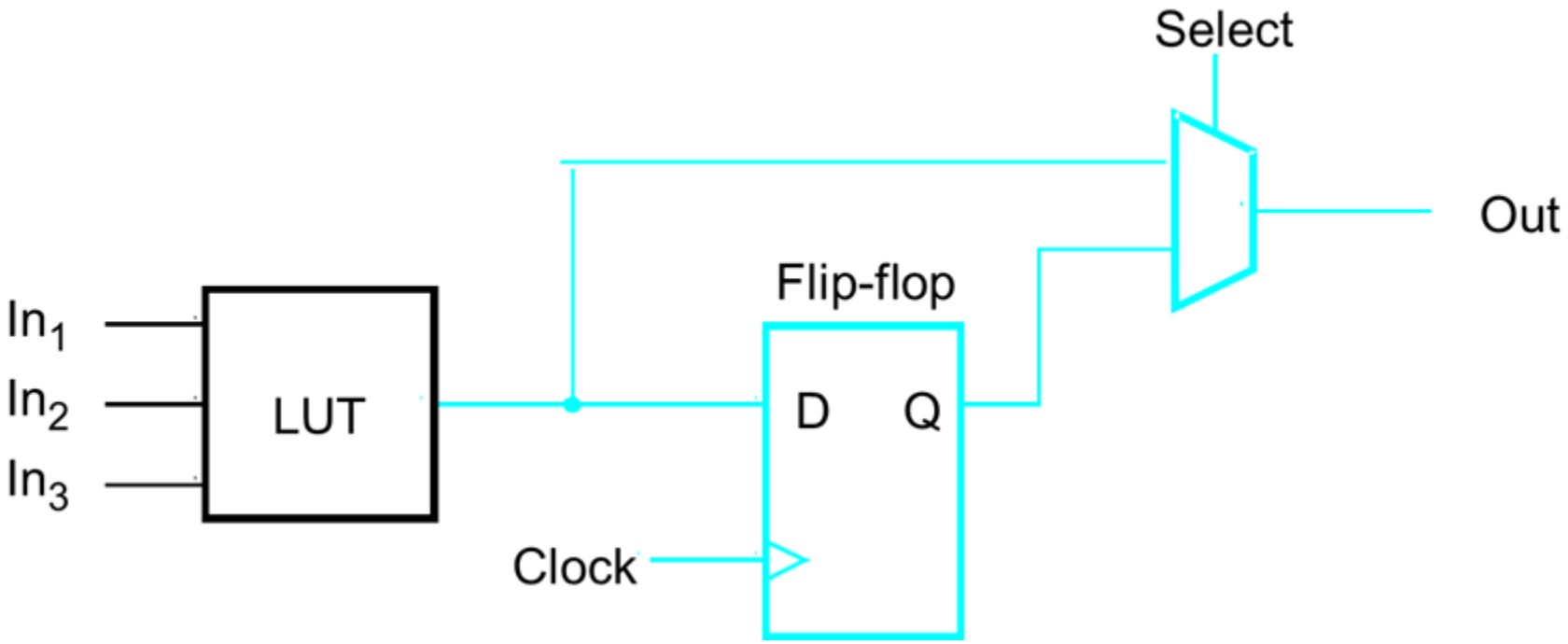
How to Implement Complex Functions?

- FPGAs are composed of a large number of LUTs and switches

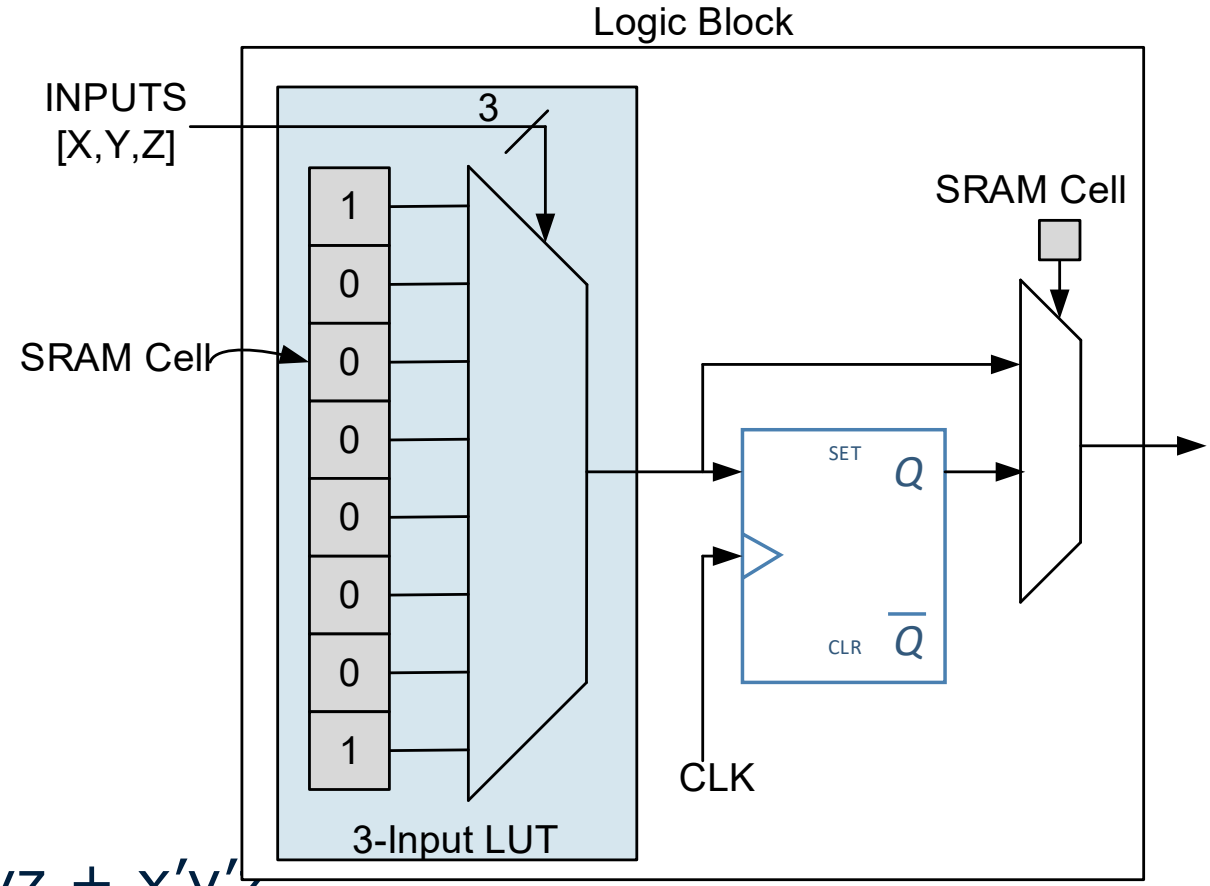


What's inside a Logic-Block? (contd.)

- In addition to a LUT, FPGA logic elements also include a flip-flop



Your Turn: What function would be implemented?

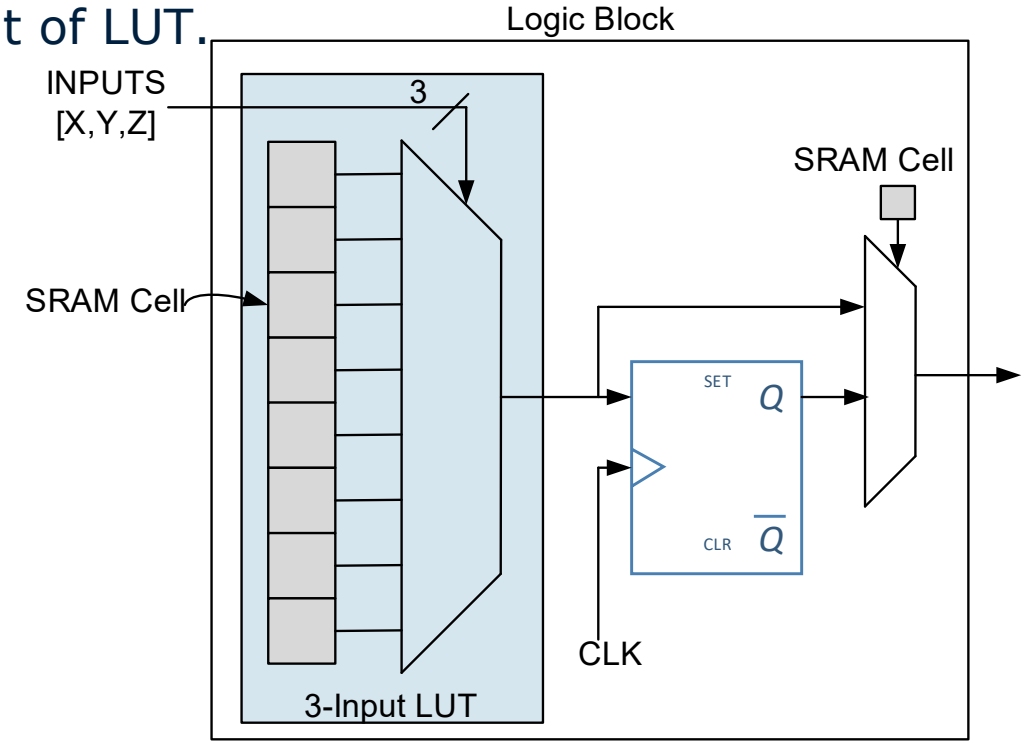


- F = xyz + x'y'z

- Take-away: A LUT is simply a way of building the truth table in silicon

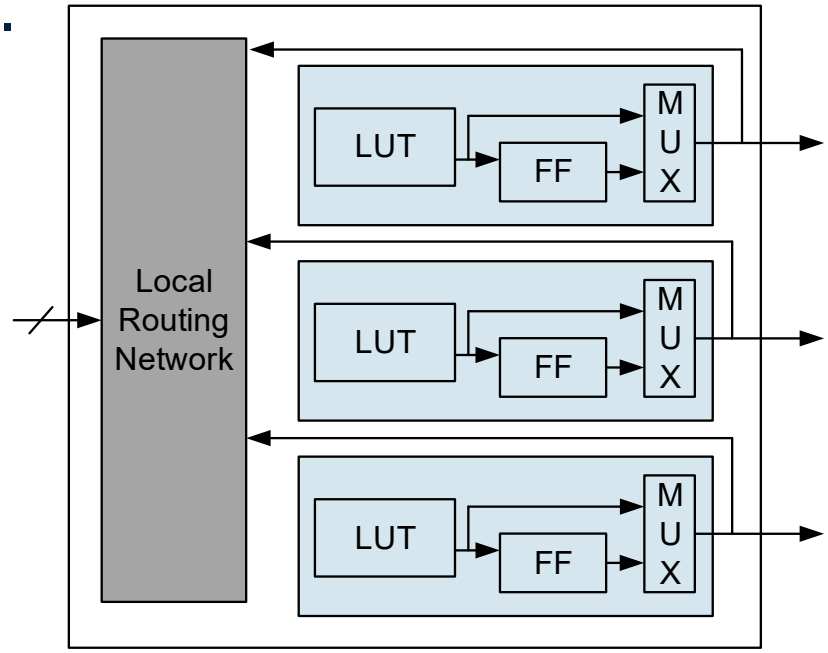
Logic-Block: Take-Away

- The number of memory cells in a LUT is defined by it's number of inputs.
- An n-input LUT requires:
  - 2^n memory cells and
  - a 2^n-input multiplexer
    - which forwards the contents of one of the memory cells to the output of LUT.



Logic-Cluster

- Modern FPGAs combine multiple logic blocks together to form a logic-cluster.



- The logic blocks in a cluster are interconnected through a local routing network.
  - The logic-clusters are called by various names by different vendors:
    - Altera calls it Logic Array Block (LAB)
    - Xilinx refers to it as a Configurable Logic Block (CLB)

Your Turn

- Find the n-input LUTs and logic-cells in modern commercial FPGAs i.e Xilinx and Intel device families.

Modern FPGA Architectures

- Typically 6-LUTs
  - Thousands of them
- An order of MB distributed on-chip memory
- Hard-coded special purpose hardware blocks for high-performance operations
  - Memory interface
  - Low latency and high bandwidth off-chip I/O
  - …
- Even a processor embedded within the FPGA chip

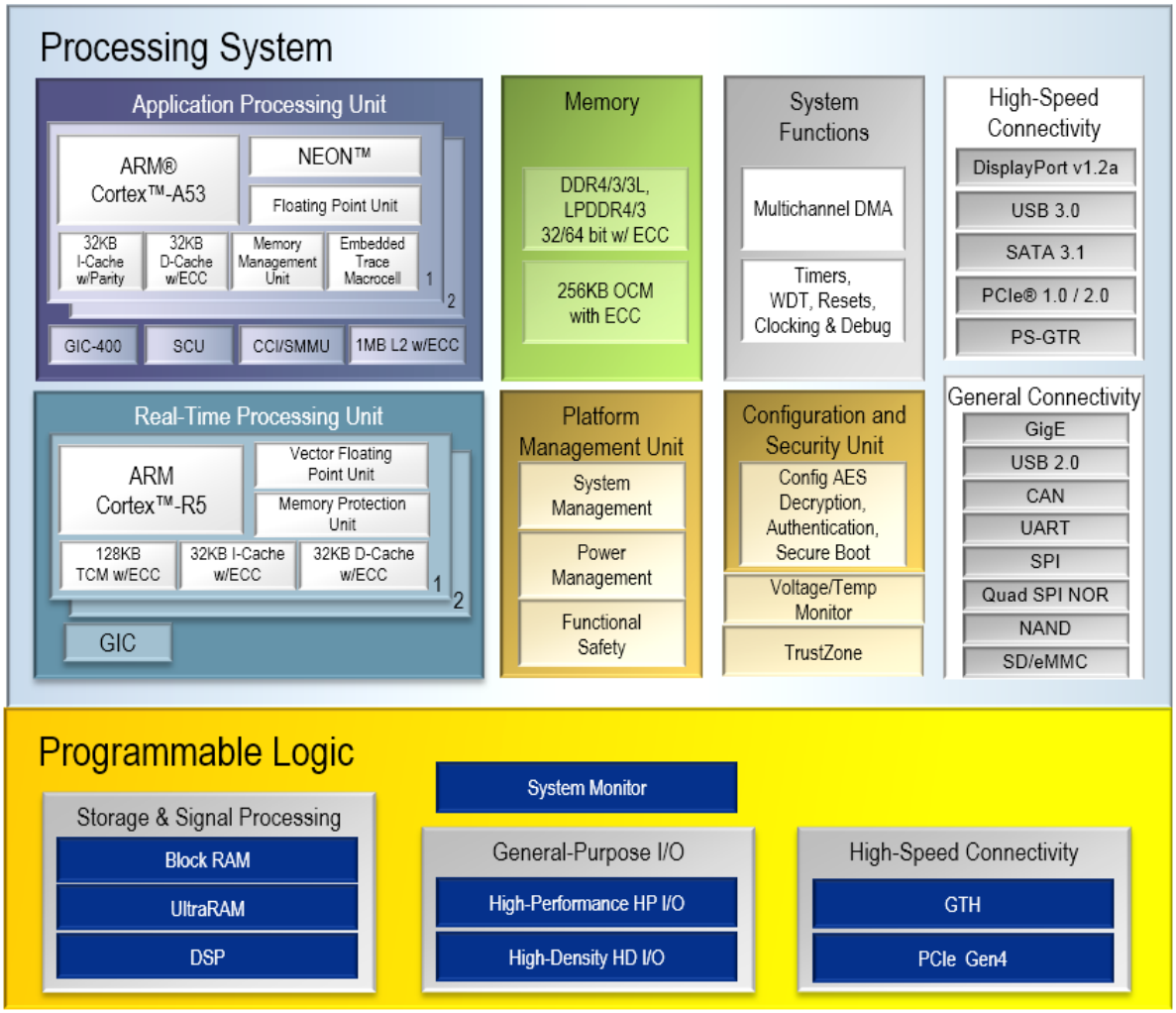
Logic Blocks in a Typical FPGA

Xilinx Multi-Node Product Portfolio Offering

FPGA Comparison Table

	Spartan-6	Artix-7	Kintex-7	Virtex-7	Kintex UltraScale	Kintex UltraScale+	Virtex UltraScale	Virtex UltraScale+
Logic Cells (K)	147	215	478	1,955	1,161	915	4,433	2,863
UltraRAM (Mb)	-	-	-	-	-	36.0	-	432.0
Block RAM (Mb)	4.8	13	34	68	76	34.5	132.9	94.5
DSP Slices	180	740	1,920	3,600	5,520	3,528	2,880	11,904
DSP Performance (symmetric FIR)	140 GMACs	930 GMACs	2,845 GMACs	5,335 GMACs	8,180 GMACs	6,287 GMACs	4,268 GMACs	21,213 GMACs
Transceiver Count	8	16	32	96	64	76	120	128
Transceiver Speed (Gb/s)	3.2	6.6	12.5	28.05	16.3	16.3	30.5	32.75
Total Transceiver Bandwidth (full duplex) (Gb/s)	50	211	800	2,784	2,086	2,478	5,886	8,384
Memory Interface (DDR3)	800	1,066	1,866	1,866	2,133	2,133	2,133	2,133
Memory Interface (DDR4)	-	-	-	-	2,400	2,667	2,400	2,667
PCI Express®	x1 Gen1	x4 Gen2	x8 Gen2	x8 Gen3	x8 Gen3	x8 Gen 4 x16 Gen 3	x8 Gen3	x8 Gen 4 x16 Gen 3

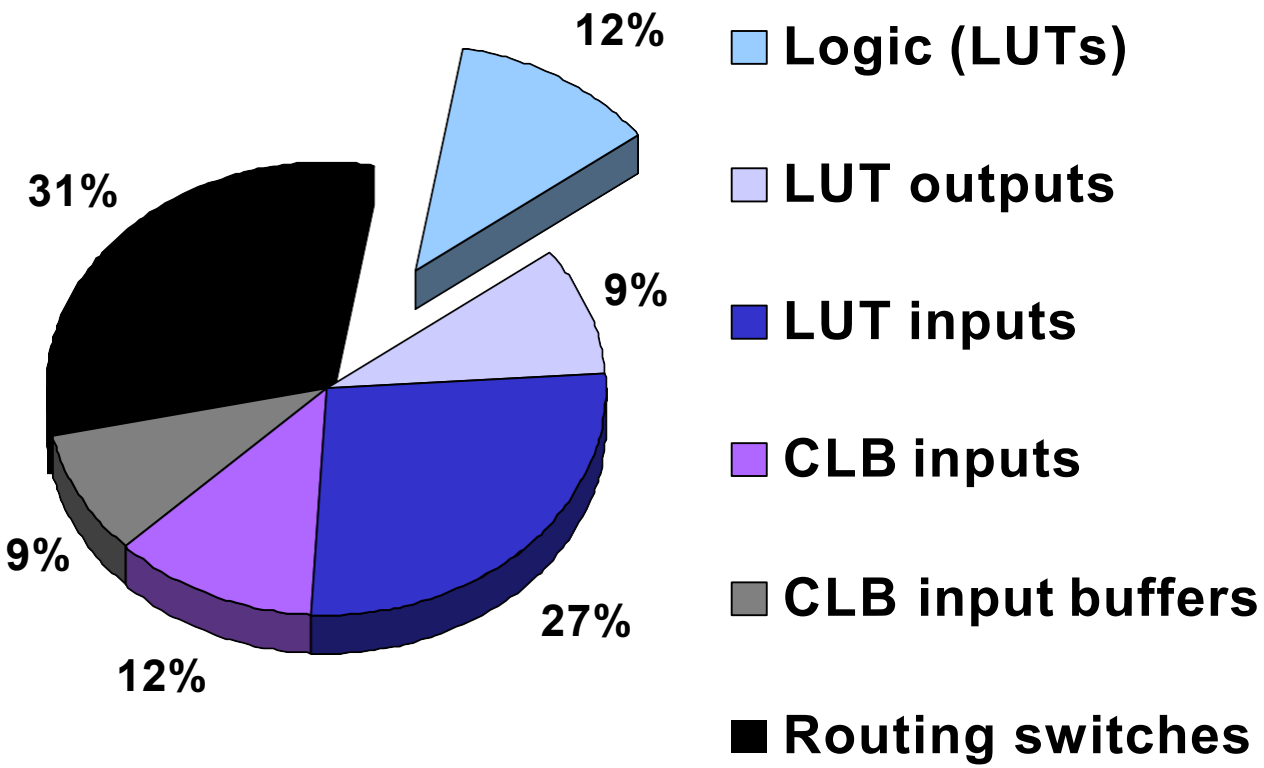
Xilinx Zynq Ultrascale+



https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html

FPGA Routing Fabric

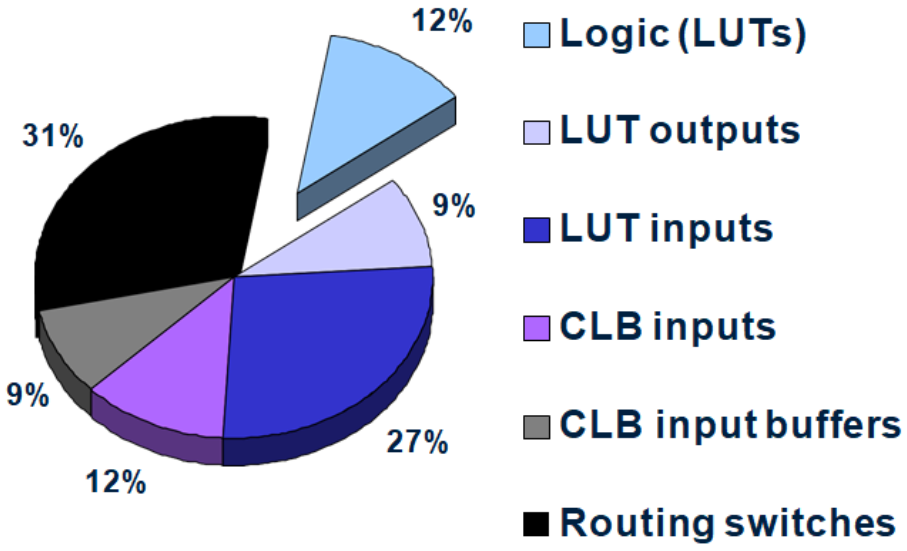
- Routing is important!

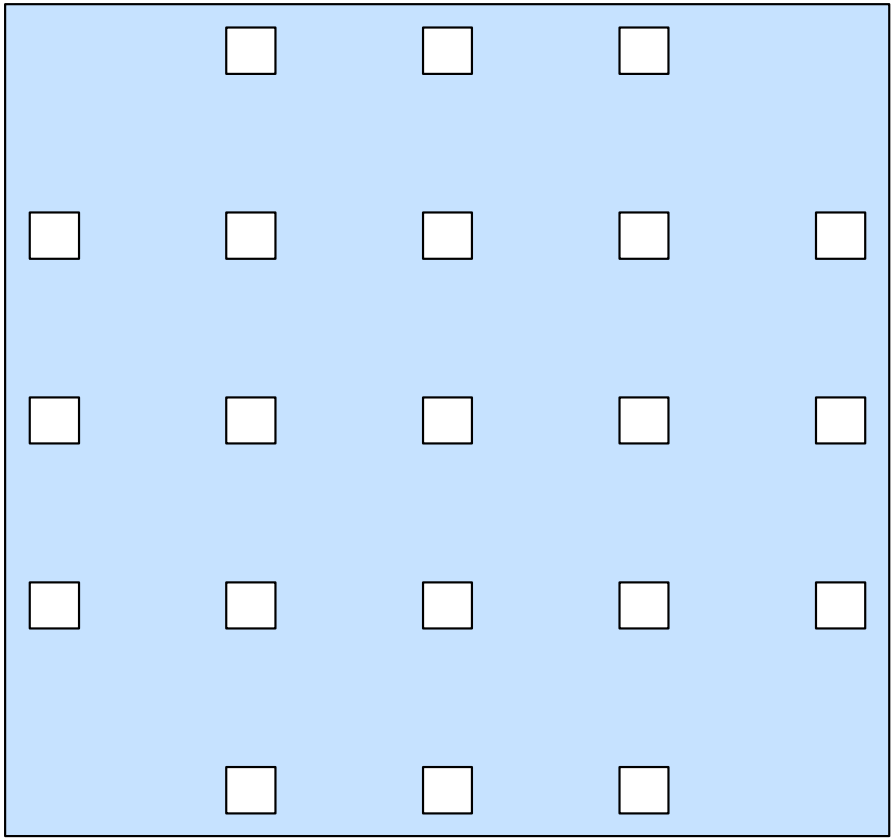


Source: Guy Lemieux

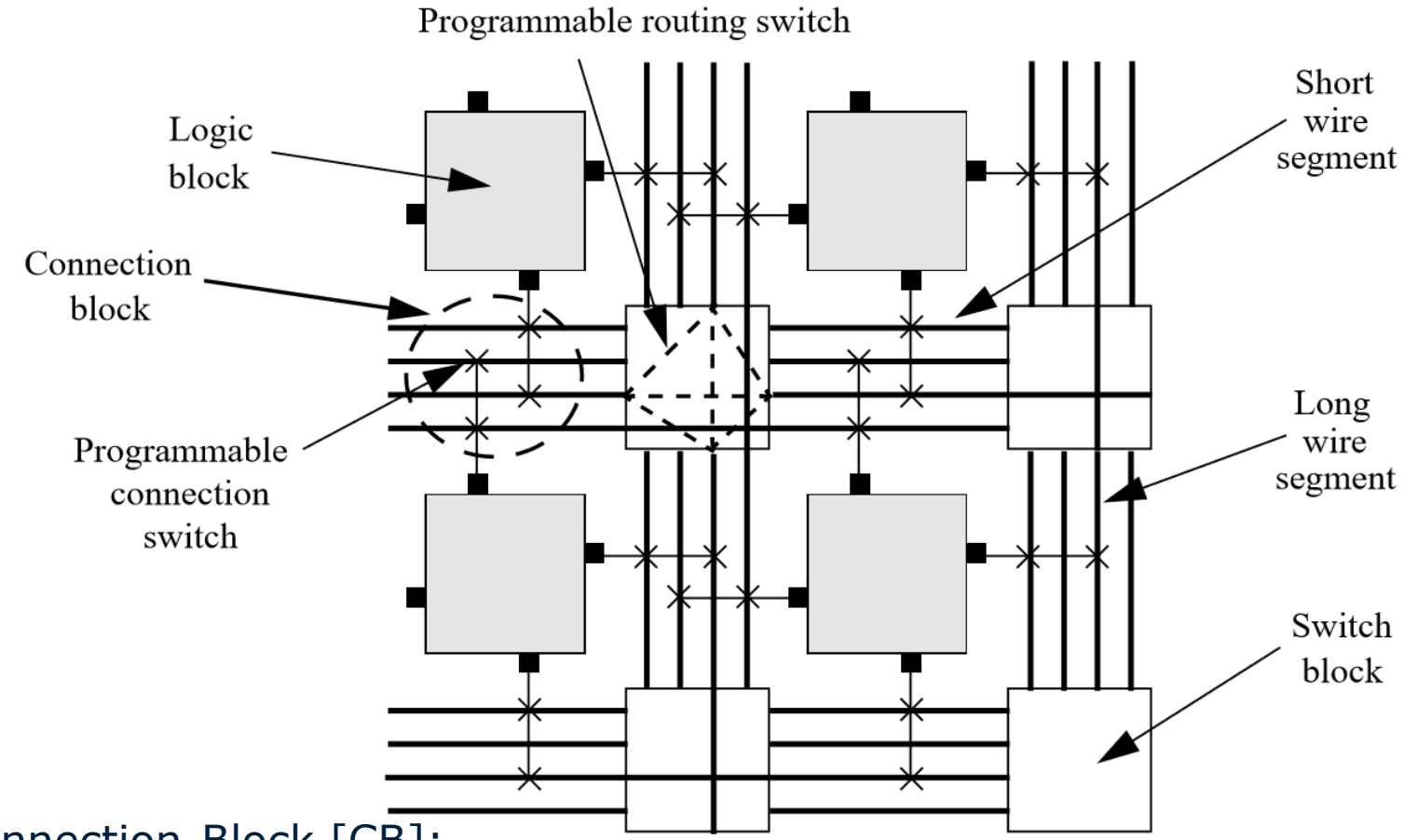
FPGA Routing Fabric

- Most of the FPGA area is due to routing:
  - Fixed metal tracks arranged in horizontal and vertical channels





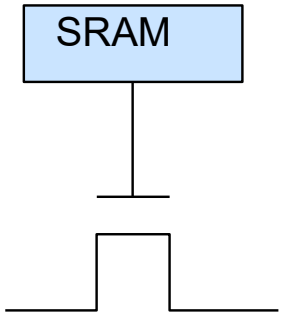
FPGA Routing Fabric



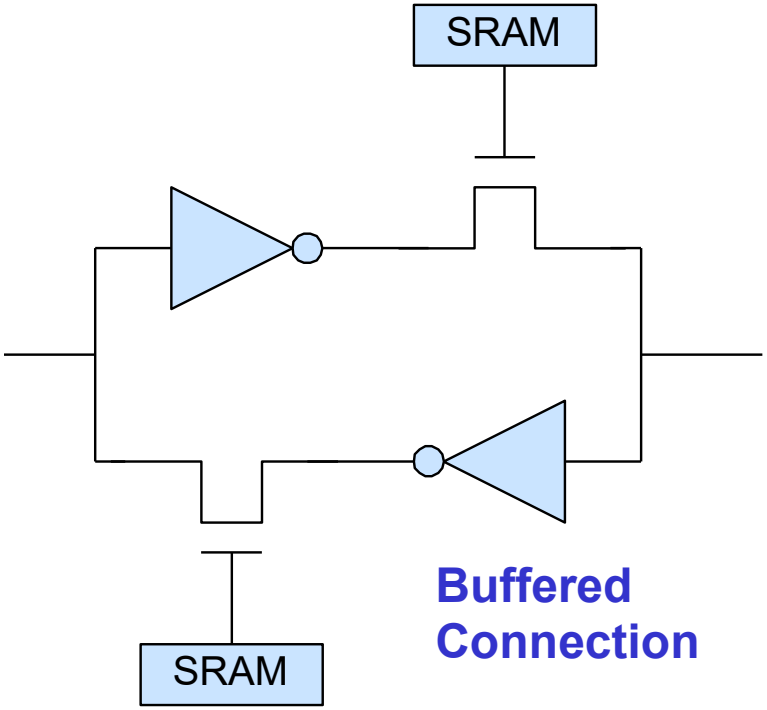
- Connection-Block [CB]:
  - Connects LB to wires through programmable switches
- Switch-Block [SB]:
  - At every intersection of a horizontal channel and a vertical channel, there is a switch block

Fig. Source: Vaughn Betz PhD. Thesis. Figure 2.4 on page 12.

How does a Programmable Switch look like?



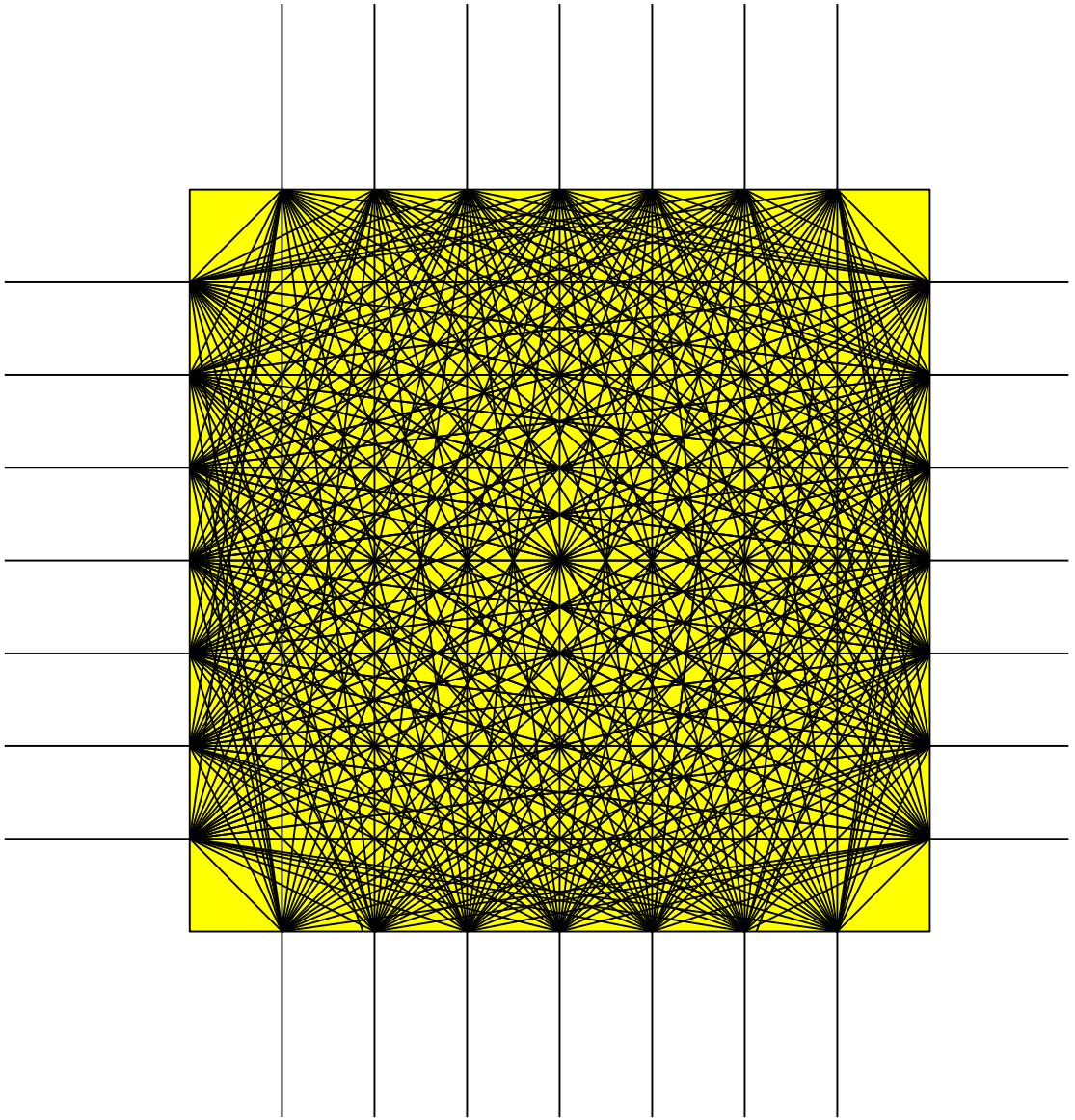
Unbuffered Connection



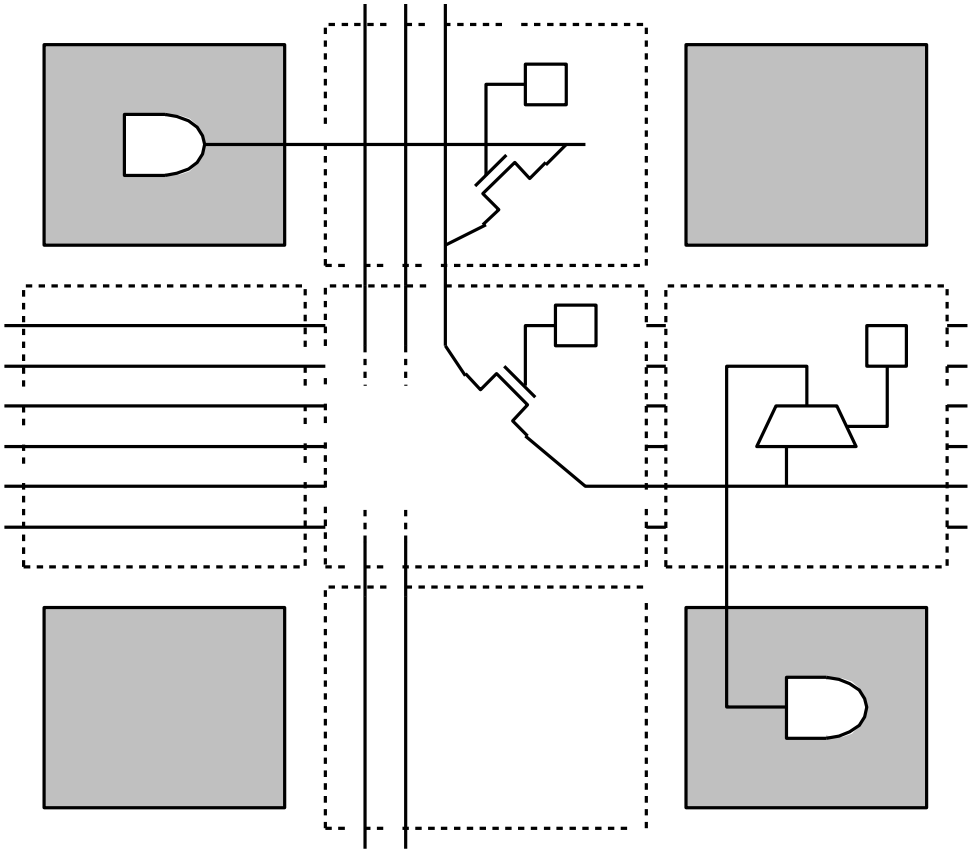
Buffered Connection

Switch Block

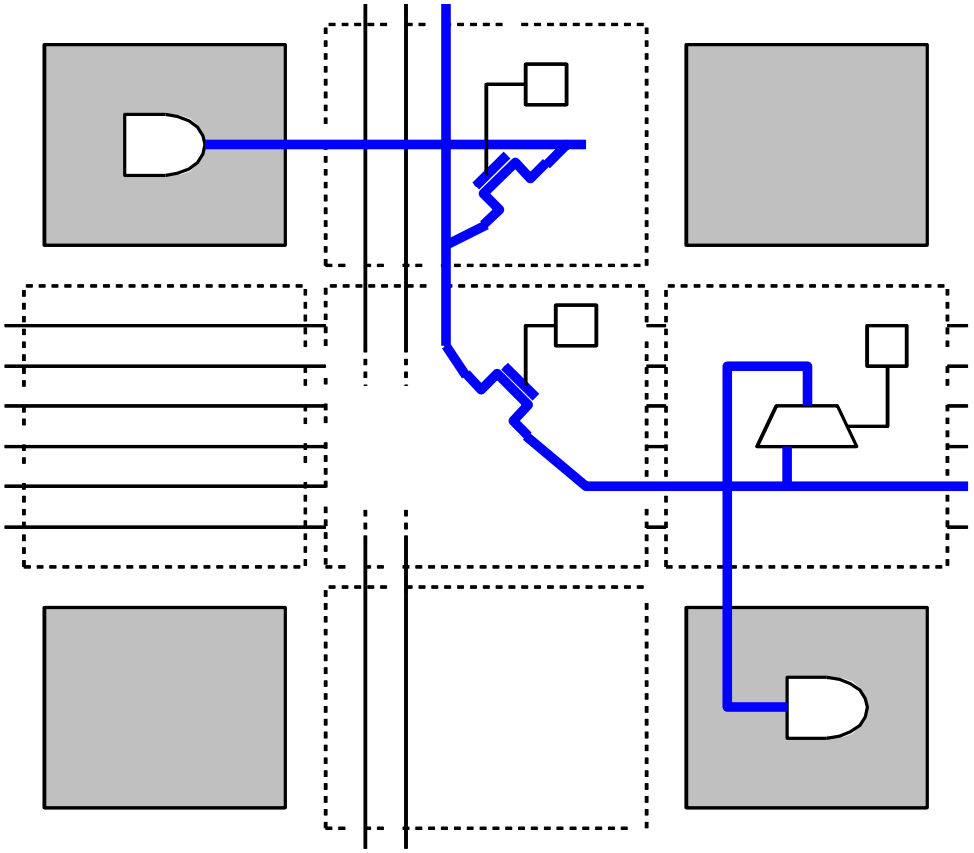
- Switch Block connects every possible connection
- Too big and Too slow



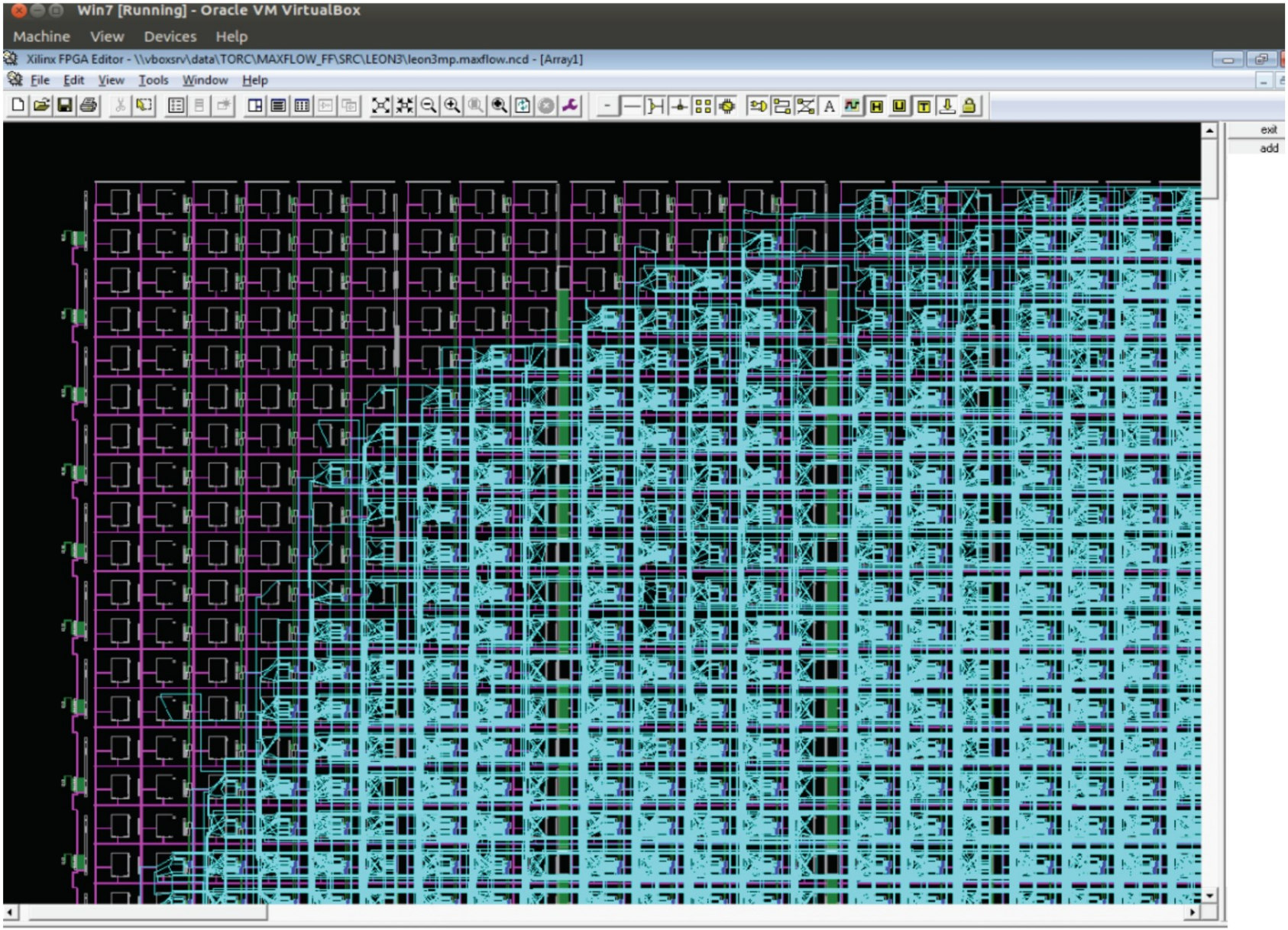
Routing Example



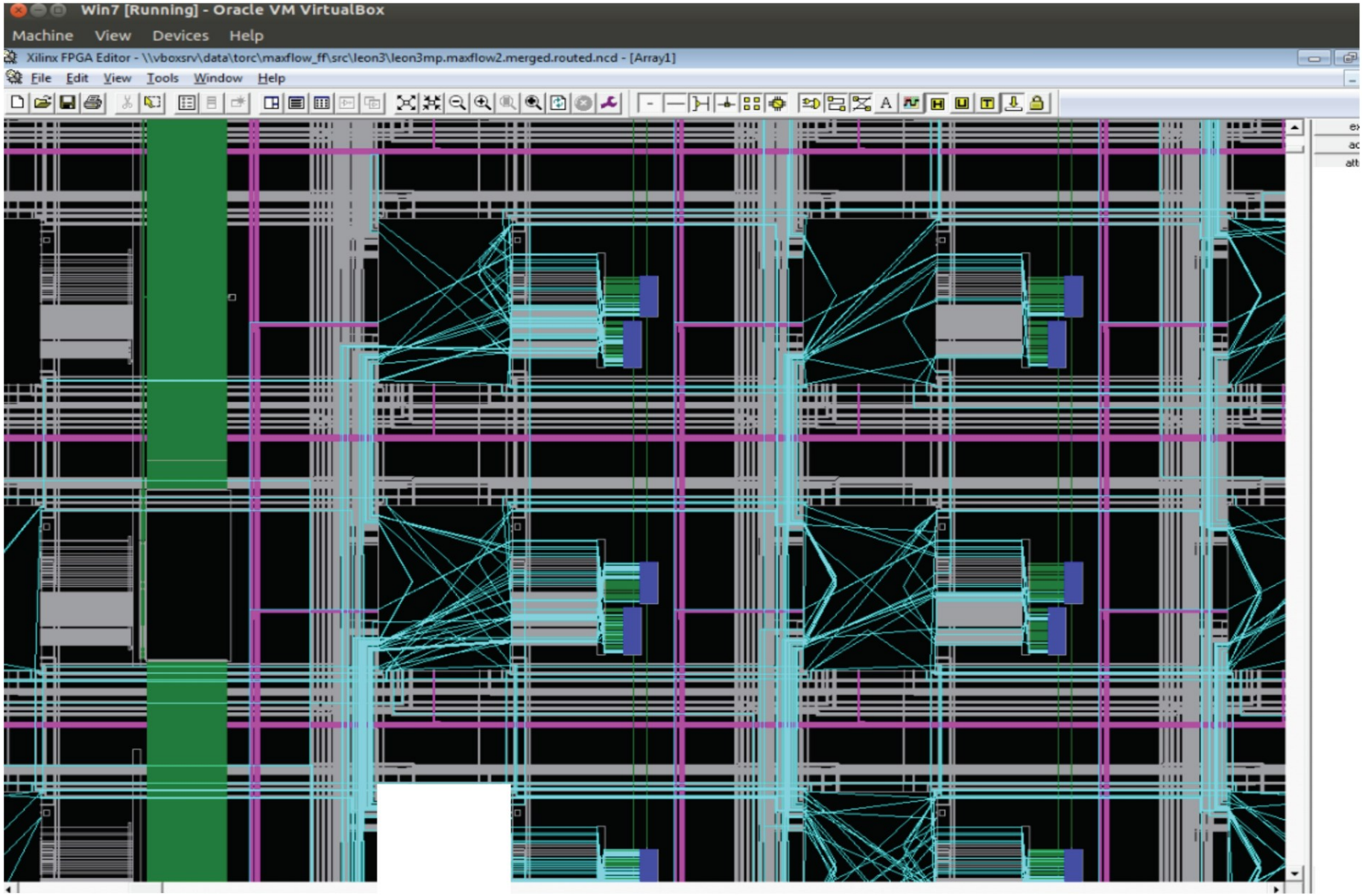
Routing Example



Example: Placed and Routed Design



Previous Example: Zoomed to Routing



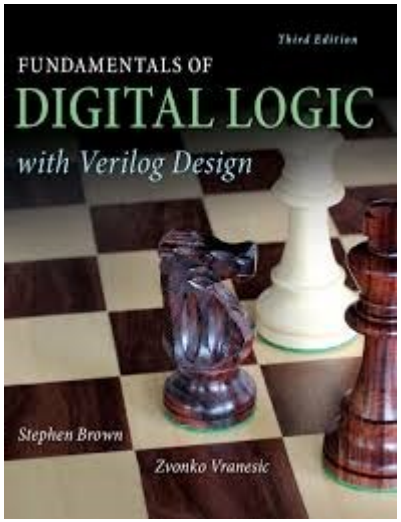
Advantages & Disadvantages of FPGAs

- Advantages
  - Low development cost
  - Short time to market
  - Reconfigurable in the field
  - Reusability
  - An algorithm can be implemented directly in hardware
    - No ISA, high specialization

- Disadvantages
  - Not as fast and power efficient as *application specific hardware*
  - Reconfigurability adds significant area overhead

Recommended Reading

- Digital System Design with Verilog HDL, 3/e, b **S**tephen Brown and **Z**vonko Vranesic. [**S&Z**]
  - S&Z,
    - Appendix-B
      - B.5 to B.8



- Compulsory Article Reading:
  - FPGA_Architecture_Principles_and_Progression
    - Uploaded on LMS

THANK YOU