# Chapter5-Synchronous Sequential Logic

Lecture7- Design of Clocked Sequential Circuits

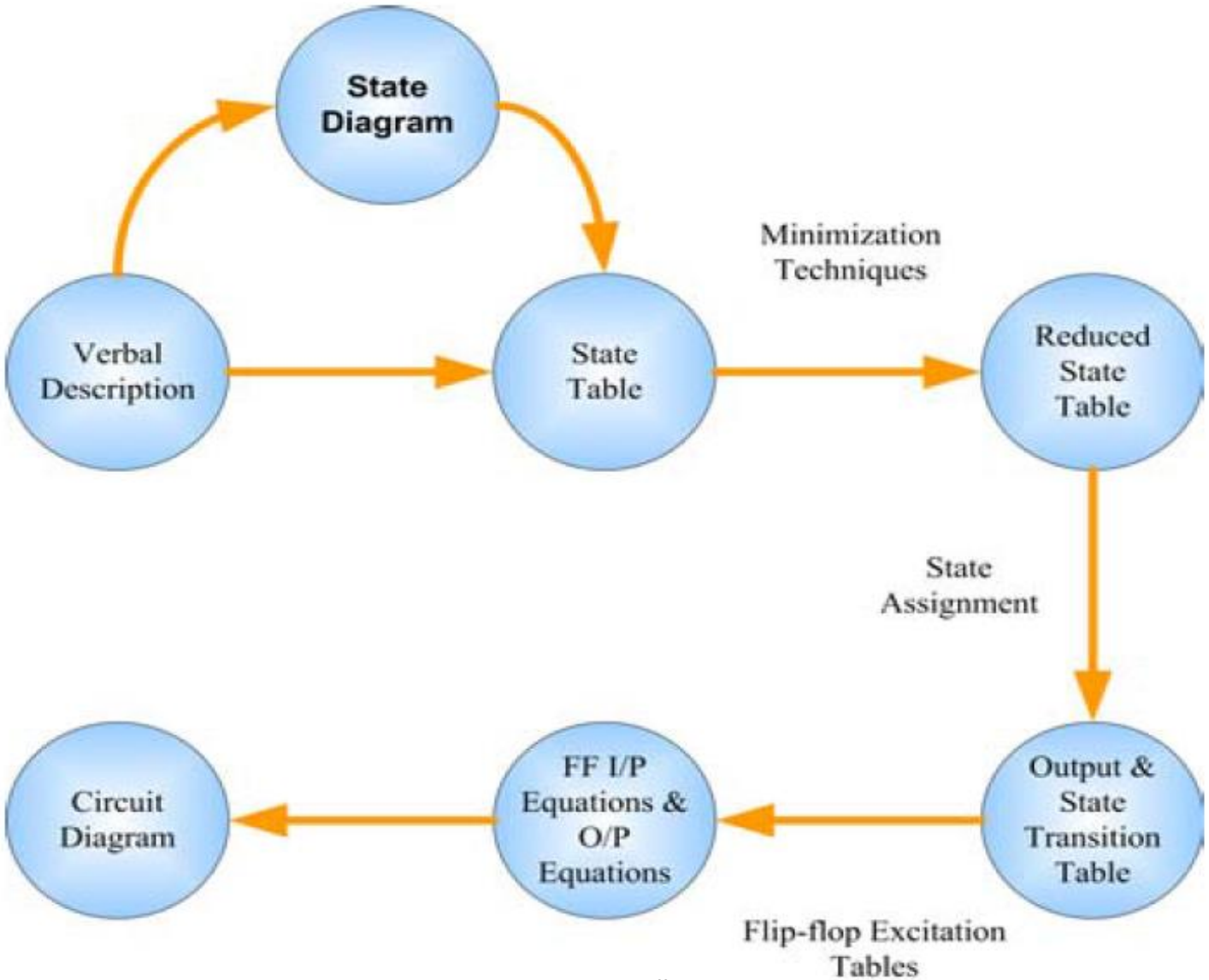
# Objectives

- Design of Clocked Sequential Circuits
- Conversion of Flip-Flops

# Design Procedure

- Design starts from verbal specifications of design and results in a logic diagram or a list of Boolean functions.
- The steps to be followed are:
  - Derive a state diagram
  - Reduce the number of states
  - Assign binary values to the reduced states
  - Obtain the binary coded state table
  - Choose the type of flip flops to be used
  - Derive the simplified flip flop input equations and output equations
  - Draw the logic diagram

# Design Steps



# Design Example: A Sequence Detector

- Design a sequence detector (Moore FSM) that detects three or more consecutive 1's from the serial binary data.
  - From the verbal specifications of design, we derive state diagram as shown below.

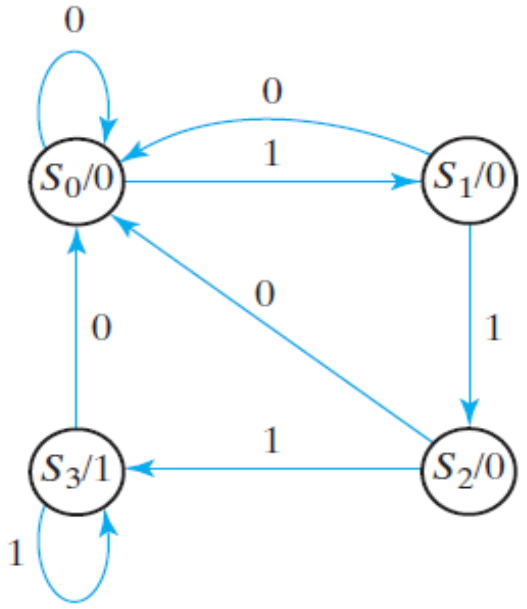



Fig. 5-24 State Diagram for Sequence Detector

# Synthesis Using D Flip Flops

- The next step is to create a state table and reduce states. No state reduction is possible in our design example.
- Make binary assignment to the four states i.e 00, 01, 10, and 11 and list Transition Table (Binary Coded State Table).
- Choose the type of flip-flops i.e two D flip flops to represent four states, and label their outputs as A and B.
- There is one input, x, and one output, y, representing the input sequence and the output value respectively.
- Remember that the characteristic equation of the D flip flop is
  - $Q(t + 1) = D_Q$
  - This means that the next-state values in the state table specify the D input condition for the flip flop.

# State Table for Sequence Detector

| Present State | | | Input | | Next State | | | Output |
|---|---|---|---|---|---|---|---|---|
| A | B | | x | | A | B | | y |
| 0 | 0 | | 0 | | 0 | 0 | | 0 |
| 0 | 0 | | 1 | | 0 | 1 | | 0 |
| 0 | 1 | | 0 | | 0 | 0 | | 0 |
| 0 | 1 | | 1 | | 1 | 0 | | 0 |
| 1 | 0 | | 0 | | 0 | 0 | | 0 |
| 1 | 0 | | 1 | | 1 | 1 | | 0 |
| 1 | 1 | | 0 | | 0 | 0 | | 1 |
| 1 | 1 | | 1 | | 1 | 1 | | 1 |

- Input equations can be obtained directly from the table using minterms:
  - $A(t + 1) = D_A(A, B, x) = \sum(3, 5, 7)$
  - $B(t + 1) = DB(A, B, x) = \sum(1, 5, 7)$
  - $y(A, B, x) = \sum(6, 7)$

# Boolean Minimization

- K-Maps can be used to minimize the input equations, resulting in
  - $D_A = Ax + Bx$;  $D_B = Ax + B'x$;  $Y = AB$

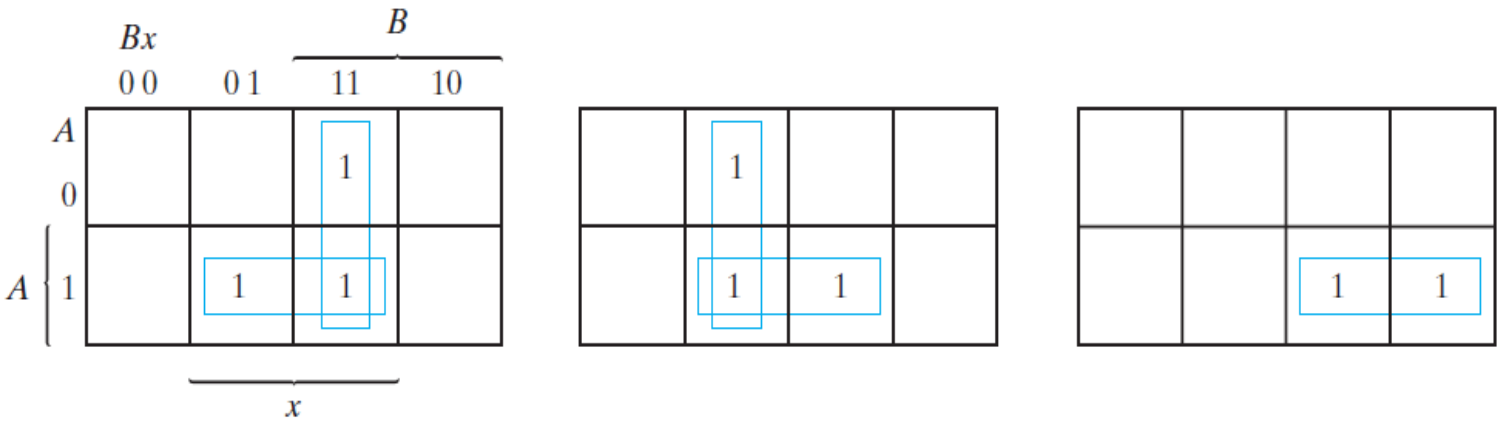



Fig. 5-25 Maps for Sequence Detector

- From Flip Flop Input Equations and Output Equation we can draw the logic diagram of the circuit as shown in the next slide.

# Logic Diagram

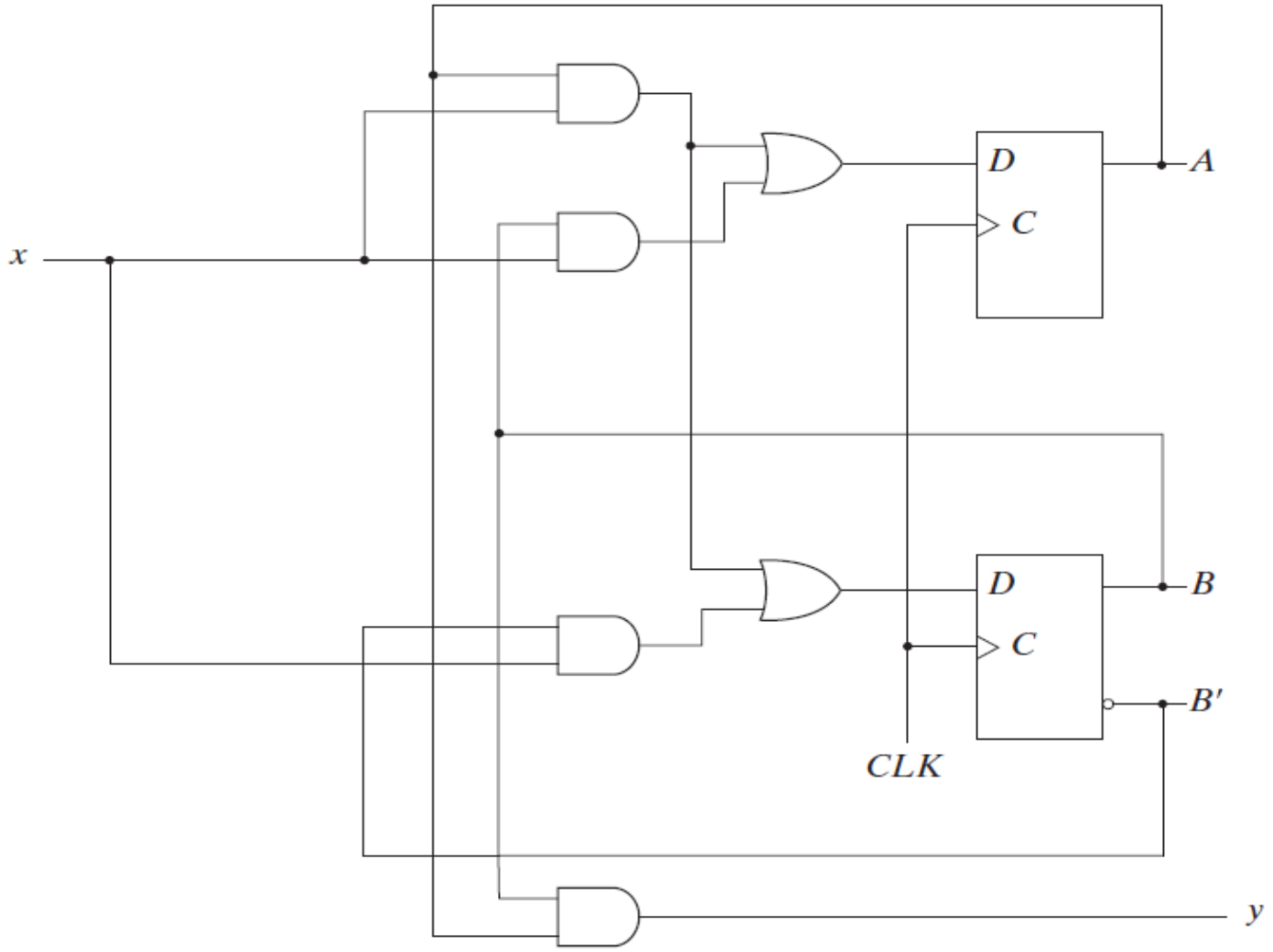
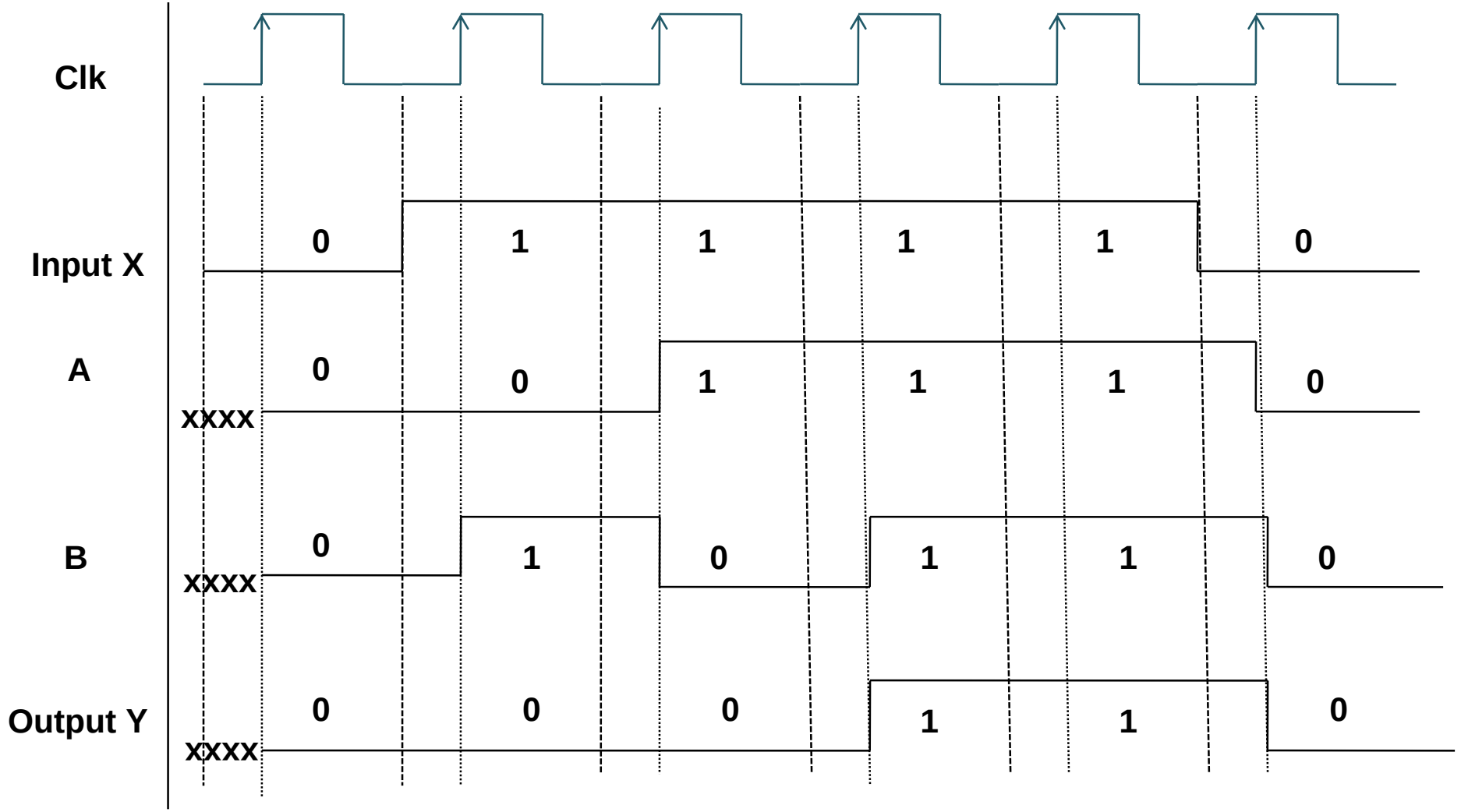



Fig. 5-26 Logic Diagram of Sequence Detector

# Timing Diagram Moore

Example: Sequence detector to detect three or more consecutive 1's




**Y=AB**

# Excitation Table

- The design of sequential circuits other than D type flip flops is complicated by the fact that input equations must be derived indirectly from the state table.
  - ➢ It is necessary to derive a functional relationship between the state table and the input equations.
- During the design, we usually know the transition from present to next state but we need to find the flip flop input conditions that will cause the required transition.
  - ➢ We need a table that lists the required inputs for a given change of state, called an excitation table.

# Excitation Tables for JK and T Flip-Flops

| JK Flip Flop | | | |
|---|---|---|---|
| J | K | Q(t+1) | |
| 0 | 0 | Q(t) | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | Q'(t) | Complement |

| Q(t) | Q(t+1) | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

| T Flip Flop | | |
|---|---|---|
| T | Q(t+1) | |
| 0 | Q(t) | No change |
| 1 | Q'(t) | Complement |

| Q(t) | Q(t+1) | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Synthesis Using JK Flip Flops

- Synthesis of circuits with JK flip flops is the same as with D flip flops except that the input equations must be evaluated from the present-state to the next-state transition derived from the excitation table.
- Consider a sequential circuit described by the state table shown in the next slide.
- Note that one extra section i.e Flip Flop Inputs has been added and we are required to derive algebraic expressions for Flip Flop Inputs as a function of present state and external inputs.

# Example JK Synthesis

| Present State | | Input | Next State | | Flip-Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| A | B | X | A | B | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
| 0 | 0 | 0 | 0 | 0 | 0 | X | 0 | X |
| 0 | 0 | 1 | 0 | 1 | 0 | X | 1 | X |
| 0 | 1 | 0 | 1 | 0 | 1 | X | X | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | X | X | 0 |
| 1 | 0 | 0 | 1 | 0 | X | 0 | 0 | X |
| 1 | 0 | 1 | 1 | 1 | X | 0 | 1 | X |
| 1 | 1 | 0 | 1 | 1 | X | 0 | X | 0 |
| 1 | 1 | 1 | 0 | 0 | X | 1 | X | 1 |

| Q(t) | Q(t + 1) | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

# JK Synthesis Logic Cont…

- By using K-maps we can minimize the flip flop input equations as under:-

  $J_A = Bx'$; $K_A = Bx$ $\quad\quad$ $J_B = x$; $K_B = (A \oplus x)'$

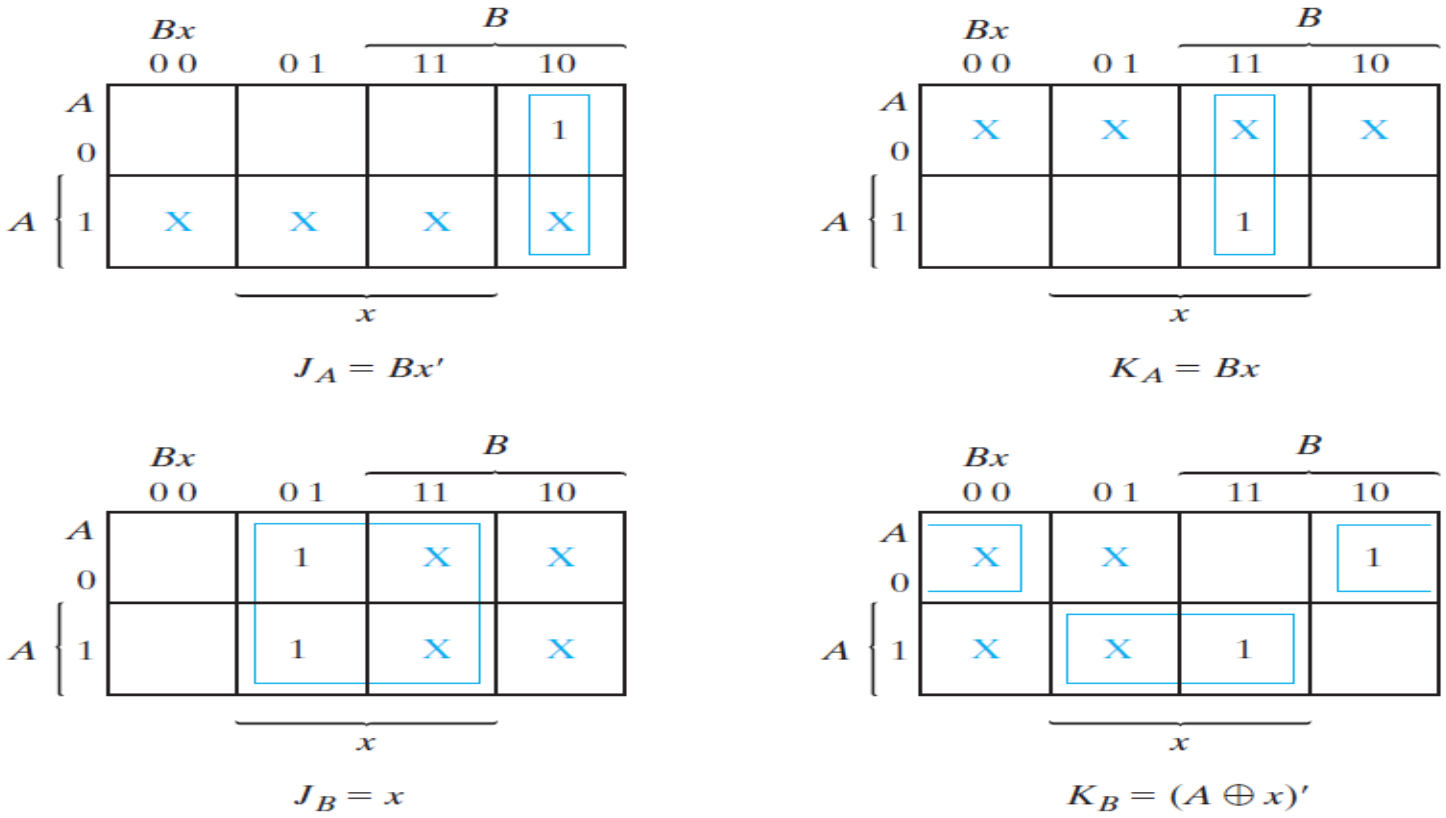



Fig. 5-27 Maps for $J$ and $K$ Input Equations

# JK Synthesis Logic Cont…

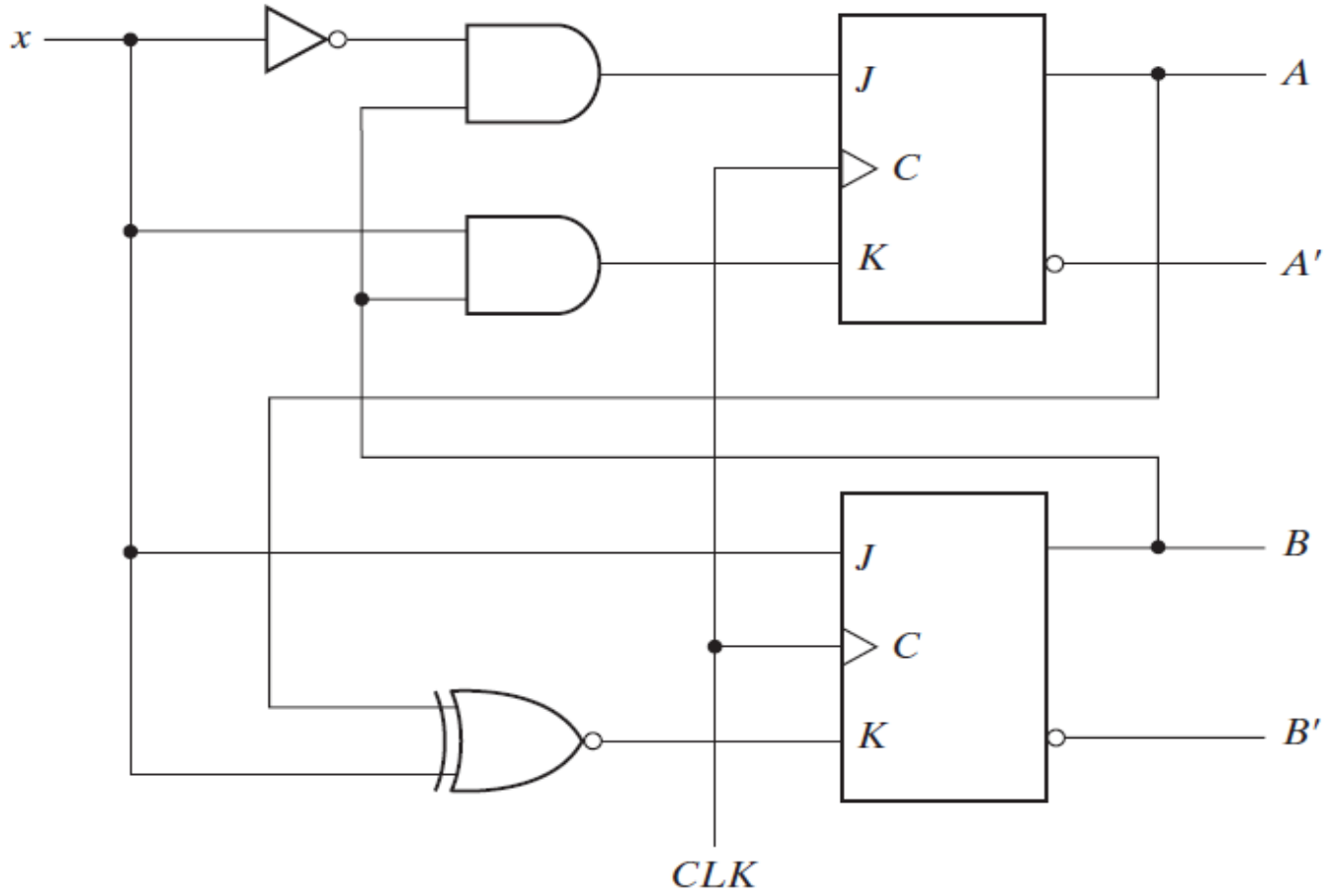



Fig. 5-28 Logic Diagram for Sequential Circuit with *JK* Flip-Flops

# Synthesis using T flip-flops

Example: Three-bit binary counter Design. The state diagram is as shown

**State Table**

| Present State | | | Next State | | | Flip-Flop Inputs | | |
|---|---|---|---|---|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | $A_2$ | $A_1$ | $A_0$ | $T_{A2}$ | $T_{A1}$ | $T_{A0}$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

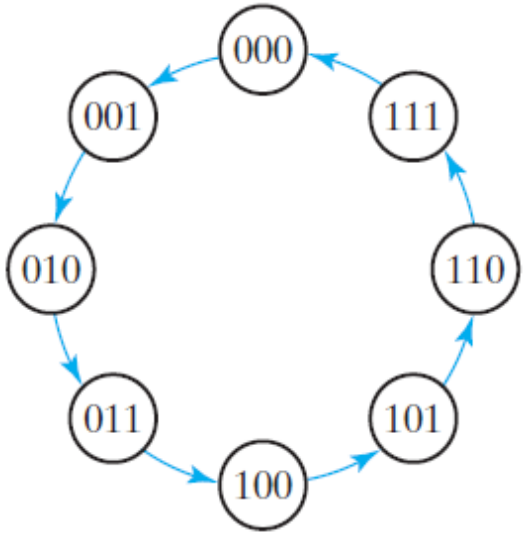



Fig. 5-29 State Diagram of 3-Bit Binary Counter

# Synthesis using T flip-flops Cont…

- By using K-maps we can minimize the flip flop input equations as under:-

  $T_{A2} = A_1 A_0$ ; $T_{A1} = A_0$ ; $T_{A0} = 1$

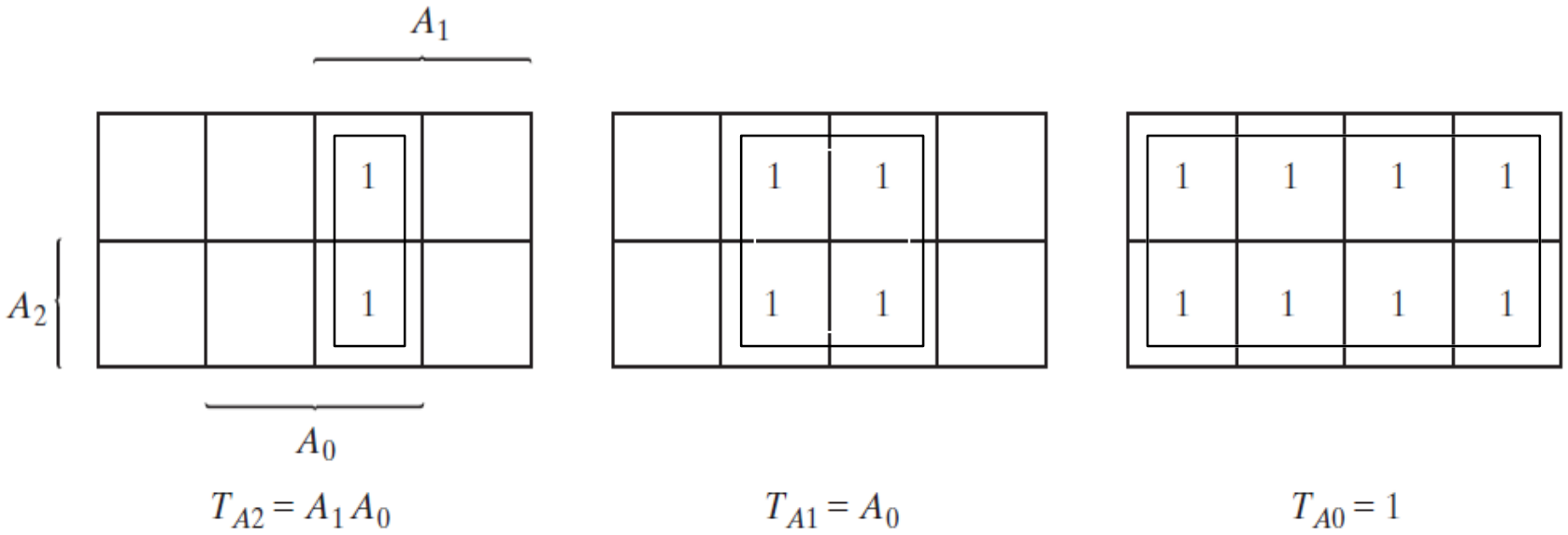



Fig. 5-30 Maps for 3-Bit Binary Counter

# Synthesis using T flip-flops Cont…

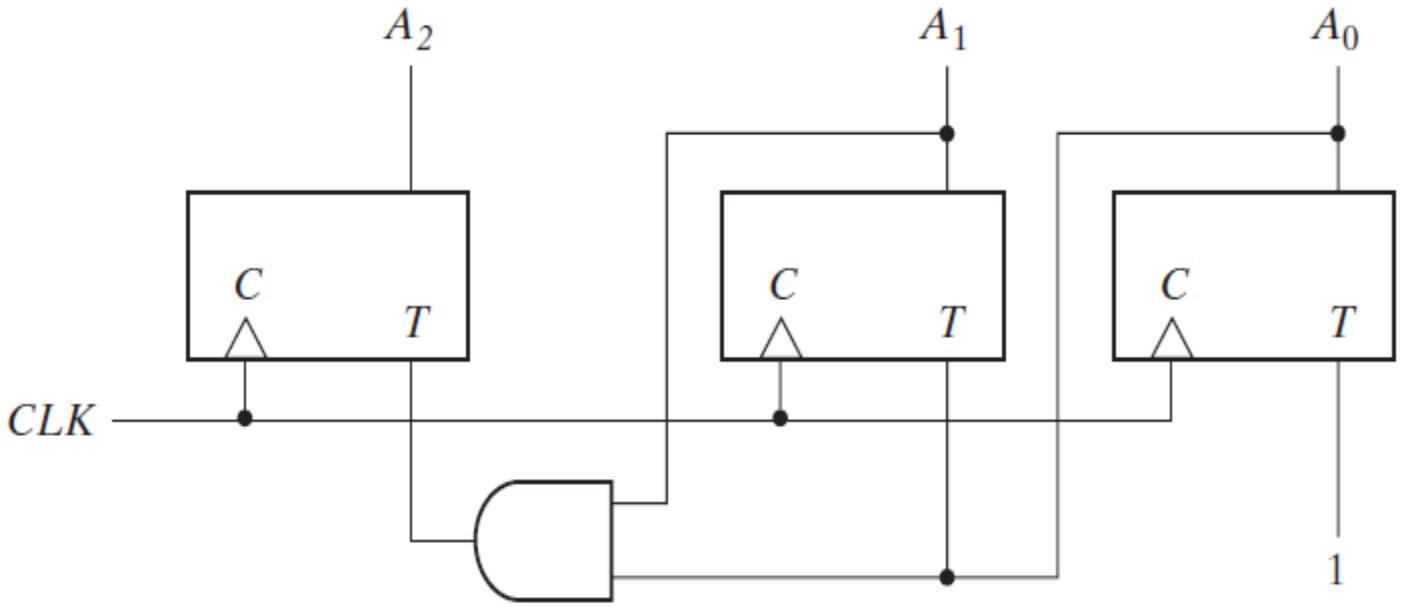



Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

# Design Example: A Sequence Detector

- Design a sequence detector (Mealy FSM) that detects three or more consecutive 1's from the serial binary data.
  - From the verbal specifications of design, we derive state diagram as shown below.

# Problem: Design a Sequence detector to detect an overlapping sequence 1010

Design a FSM that has one input w and one output z. The machine is a sequence detector that produces z=1 when the previous two values of w were 00 or 11; otherwise z=0.

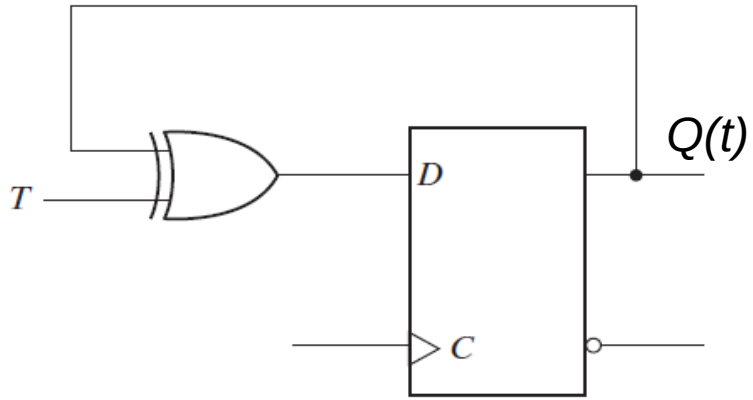
# Conversion of Flip-Flops

- We can covert one flip flop to another by the following procedure.
  - List characteristic table of flip flop to be constructed.
  - From this derive excitation table of the given flip flop.
  - Derive flip flop input equations of given flip flop as a function of present state and inputs of flip flop to be designed.
  - From this we can draw the logic diagram of new flip-flop and perform hardware implementation.

# Example-Conversion From D to T Flip-Flop

| T | Q(t) | Q(t+1) | D |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

D= T⊕Q(t)




Conversion from D to T Flip Flop

# The End