EE-421: Digital System Design

Circuit Timing

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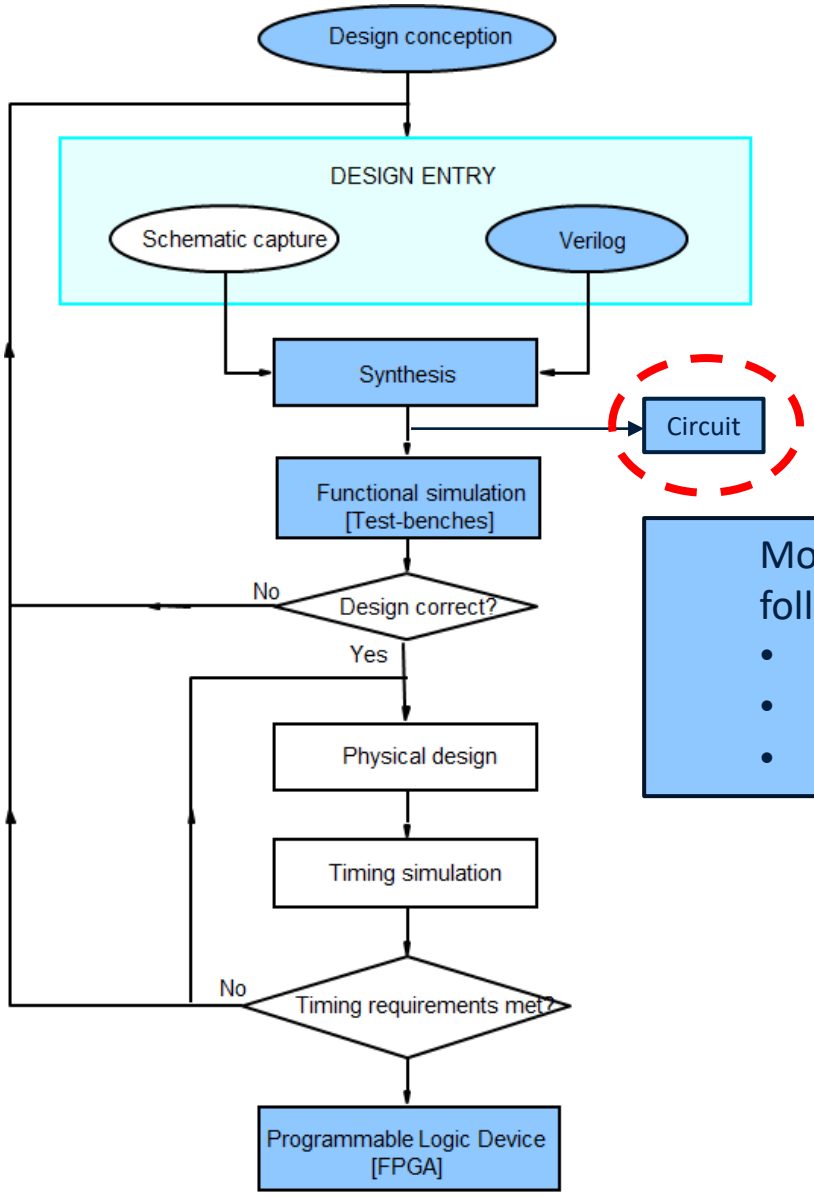
Where are we Heading?



More specifically, we'll focus on the following circuit attributes:

- Combinational Timing Constraints
- Circuit Speed
- Flip-flop Timing Constrains

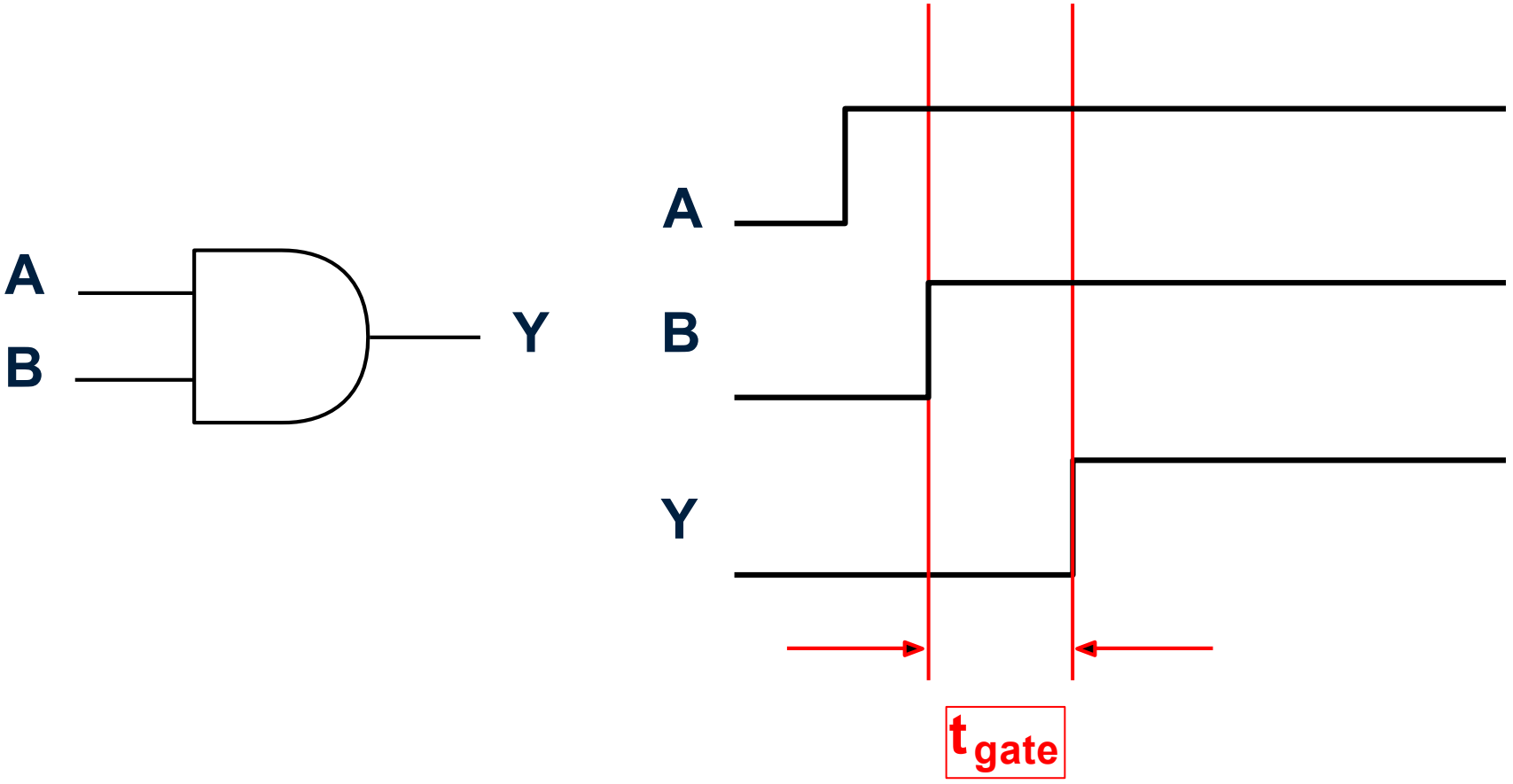
This Lesson: Timing Concepts and Terminology

- Combinational Timing Constraints:
  - Gate Propagation Delay
  - Critical Path Delay
- Circuit Speed:
  - Minimum Clock Period
  - Maximum Clock Frequency
- Flip-Flop Timing Constraints:
  - Clock-to-Q Delay
  - Setup Time
  - Hold Time

Propagation Delay in Gates

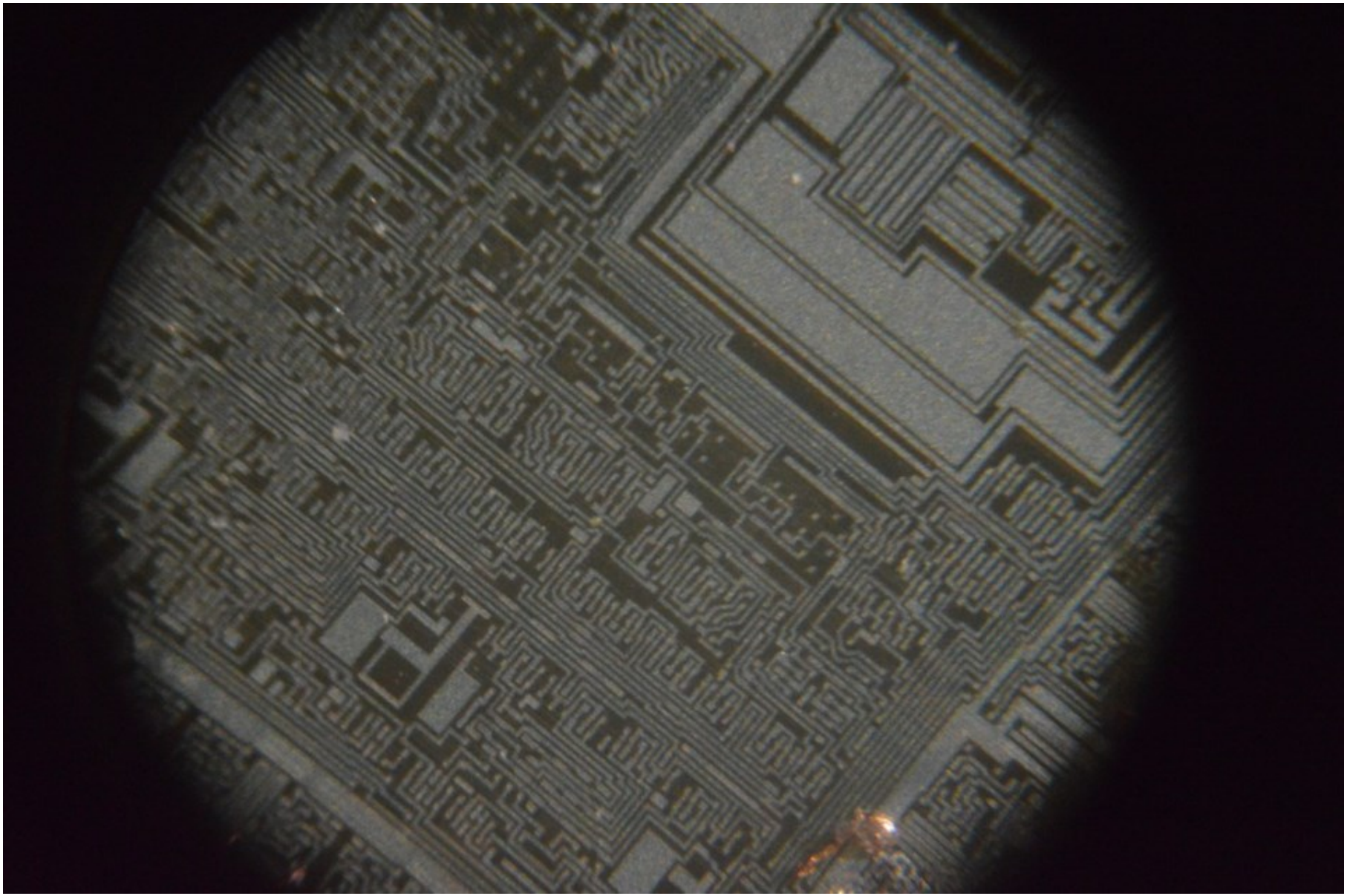
Gate Delay (Propagation Delay)

- Time that it takes for combinational gate output to change after inputs change



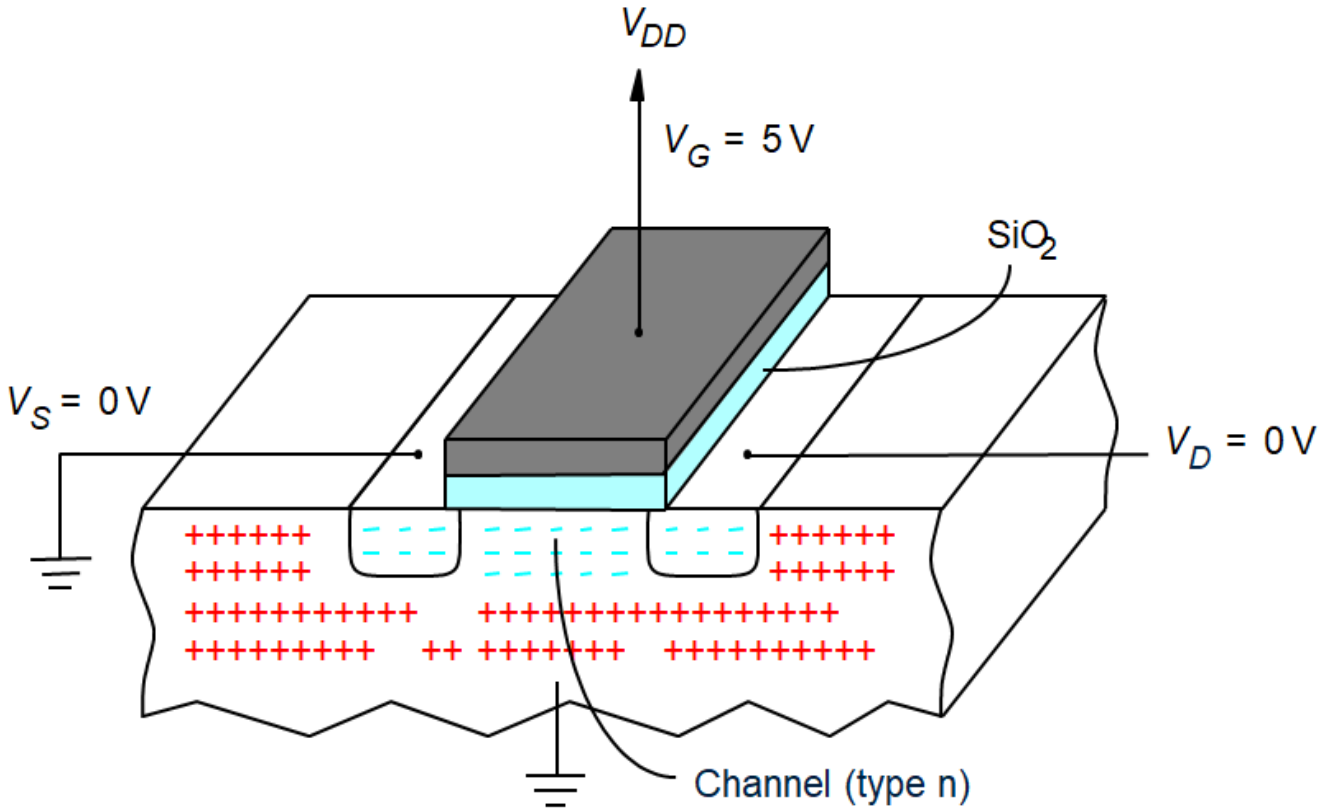
Propagation Delay in Gates: But WHY?

Inside a Chip: Microscopic View



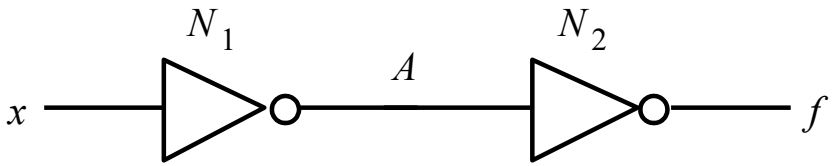
Courtesy of Shaheer Sajid (BEE-9)

Physical Structure of an NMOS Transistor

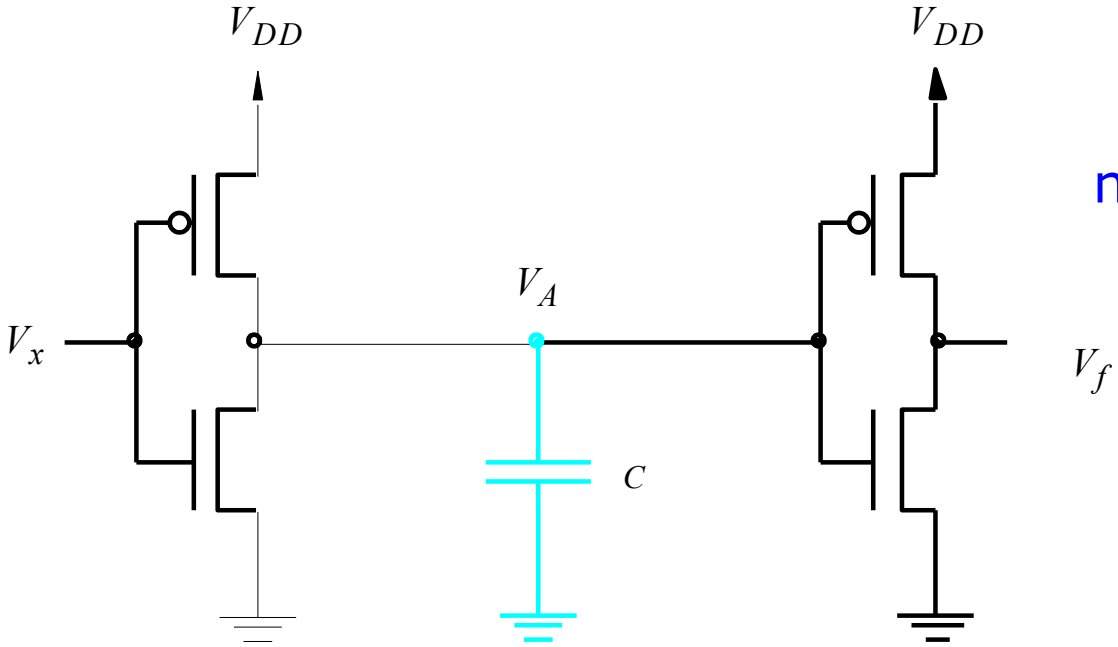


- Wherever two types of materials meet or overlap inside the transistor, a *capacitor* is effectively created:
  - aka, *parasitic* or *stray* capacitance
    - Results as an undesired side effect of a transistor fabrication

Stray Capacitance in Logic Gates



(a) A NOT gate driving another NOT gate

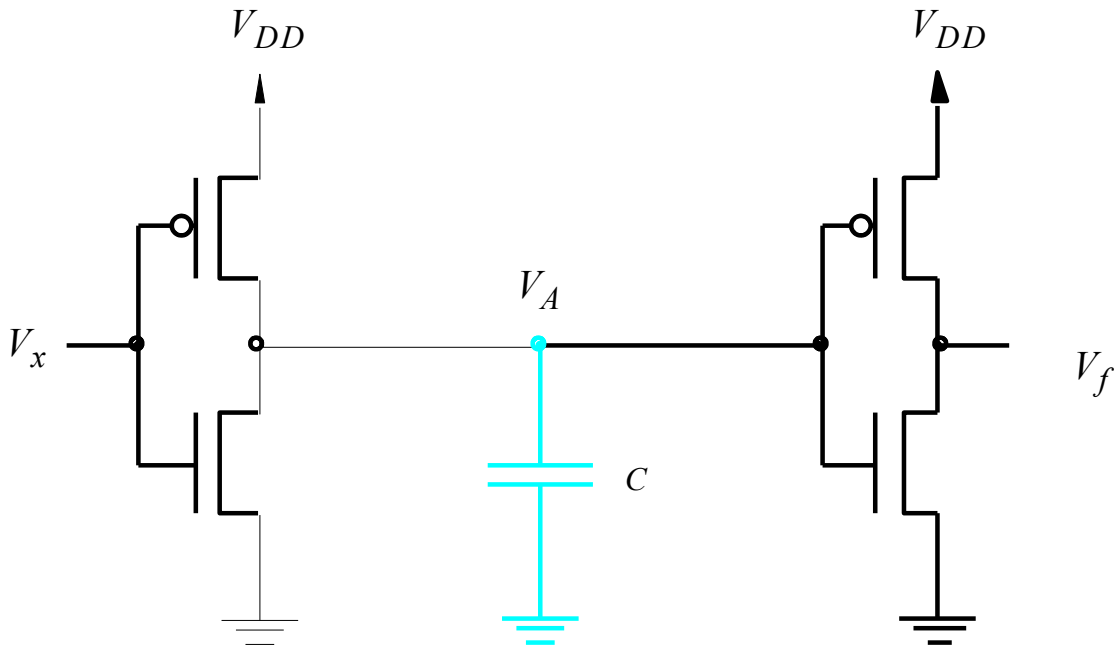


(b) The capacitive load at node A

A number of parasitic capacitors are attached to node A, some caused by N1 and others caused by N2.

All capacitances are approximated by a single equivalent capacitance.

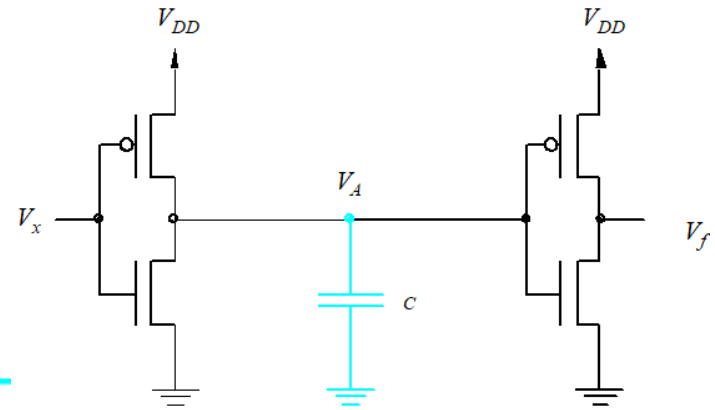
Impact of Stray Capacitance on Speed of Operation (1)

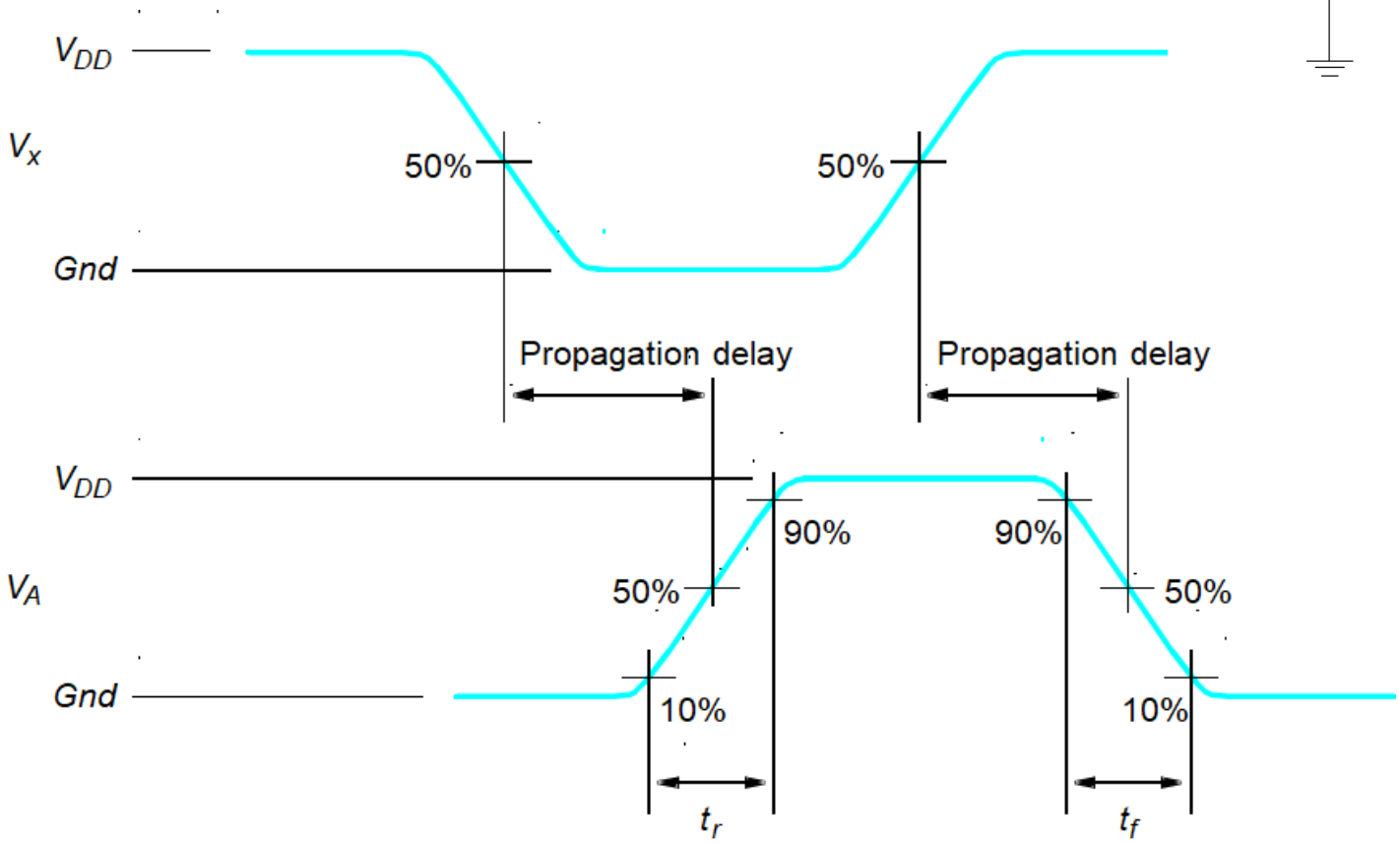


- The existence of stray capacitance has a negative effect on the speed of operation of logic circuits.

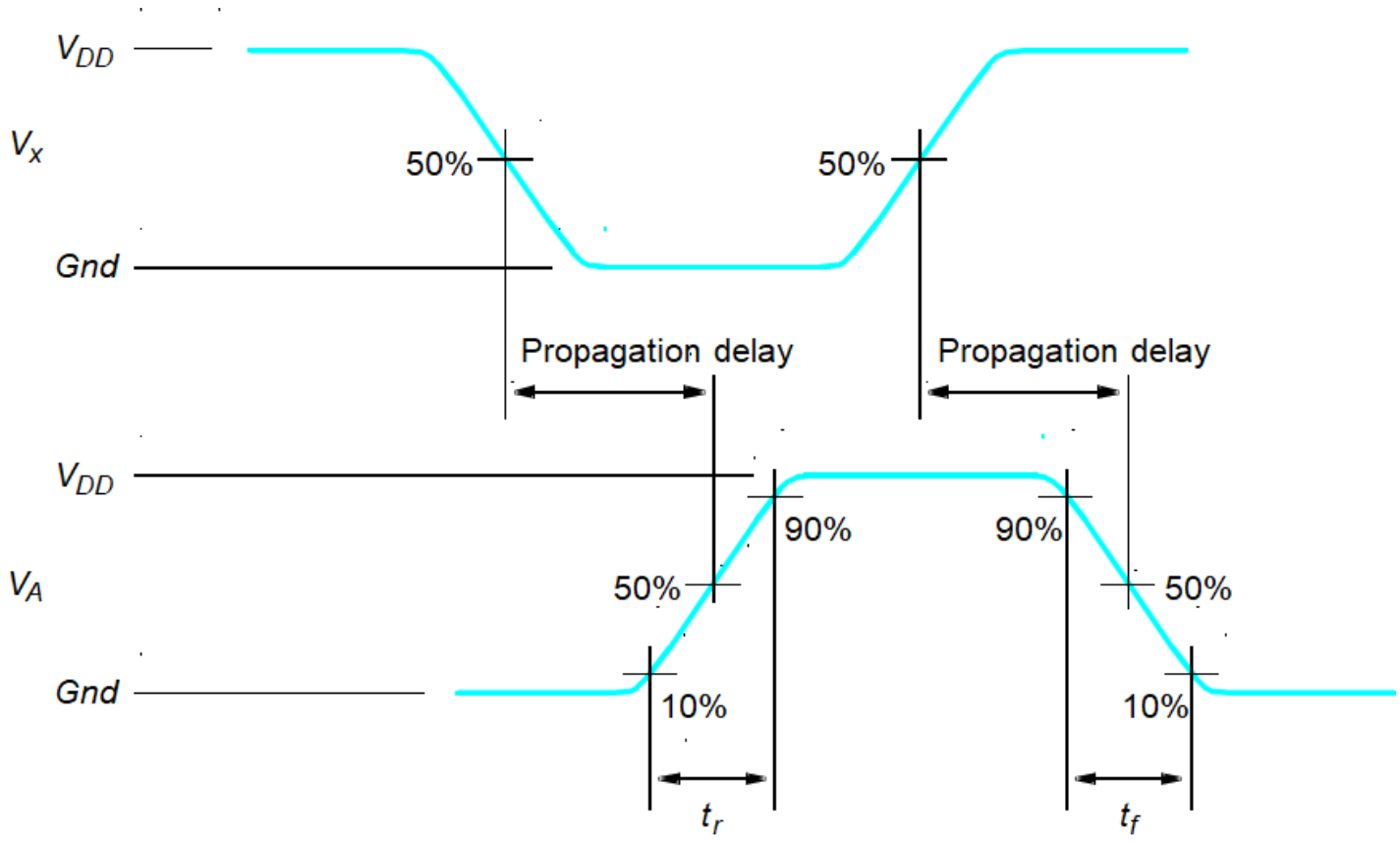
- Voltage across a capacitor cannot change instantaneously,
  - The time needed to charge or discharge a capacitor depends on the size of the capacitance C and on the amount of current through the capacitor.

VTC: Voltage Transfer Characteristics



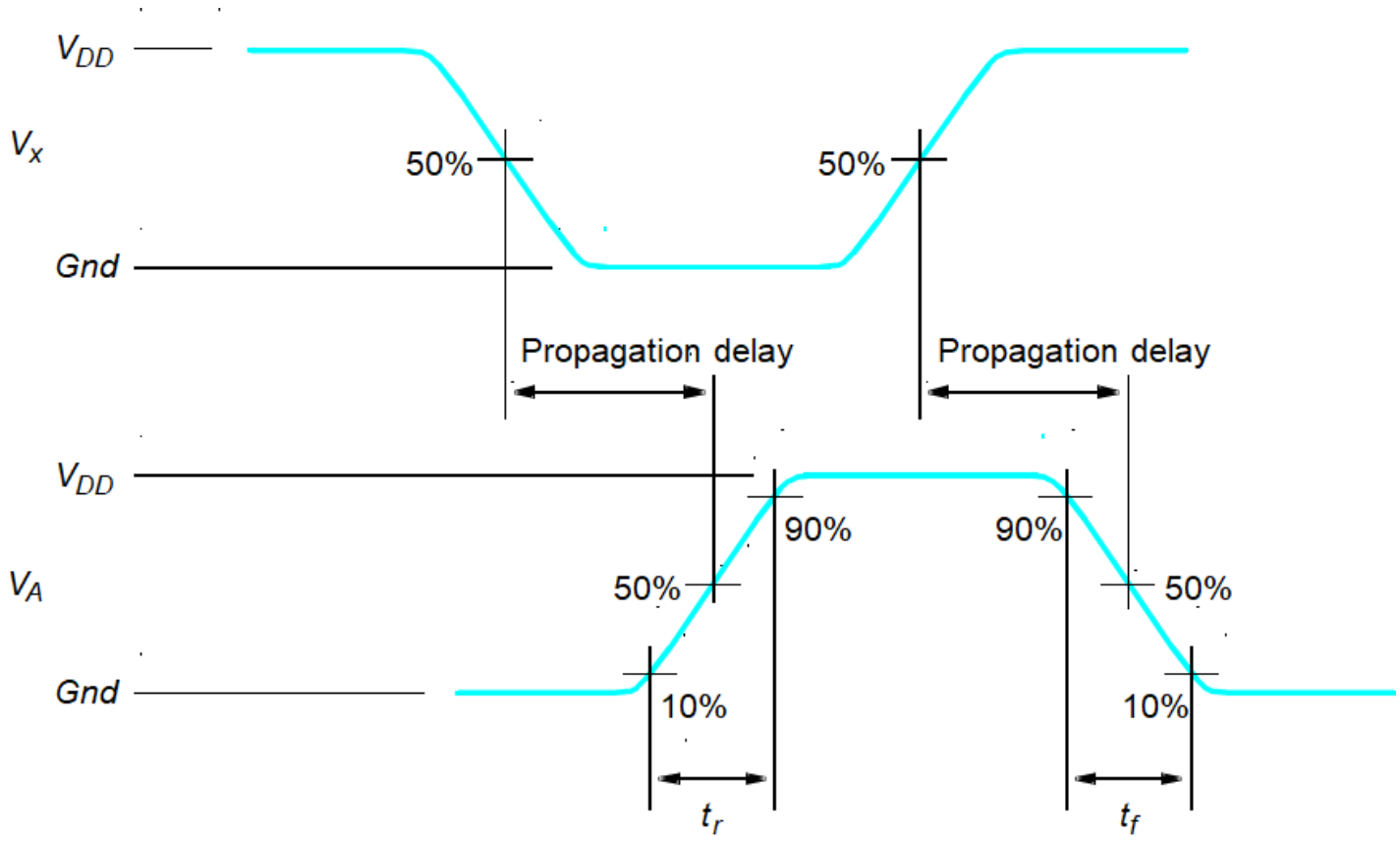


Rise Time



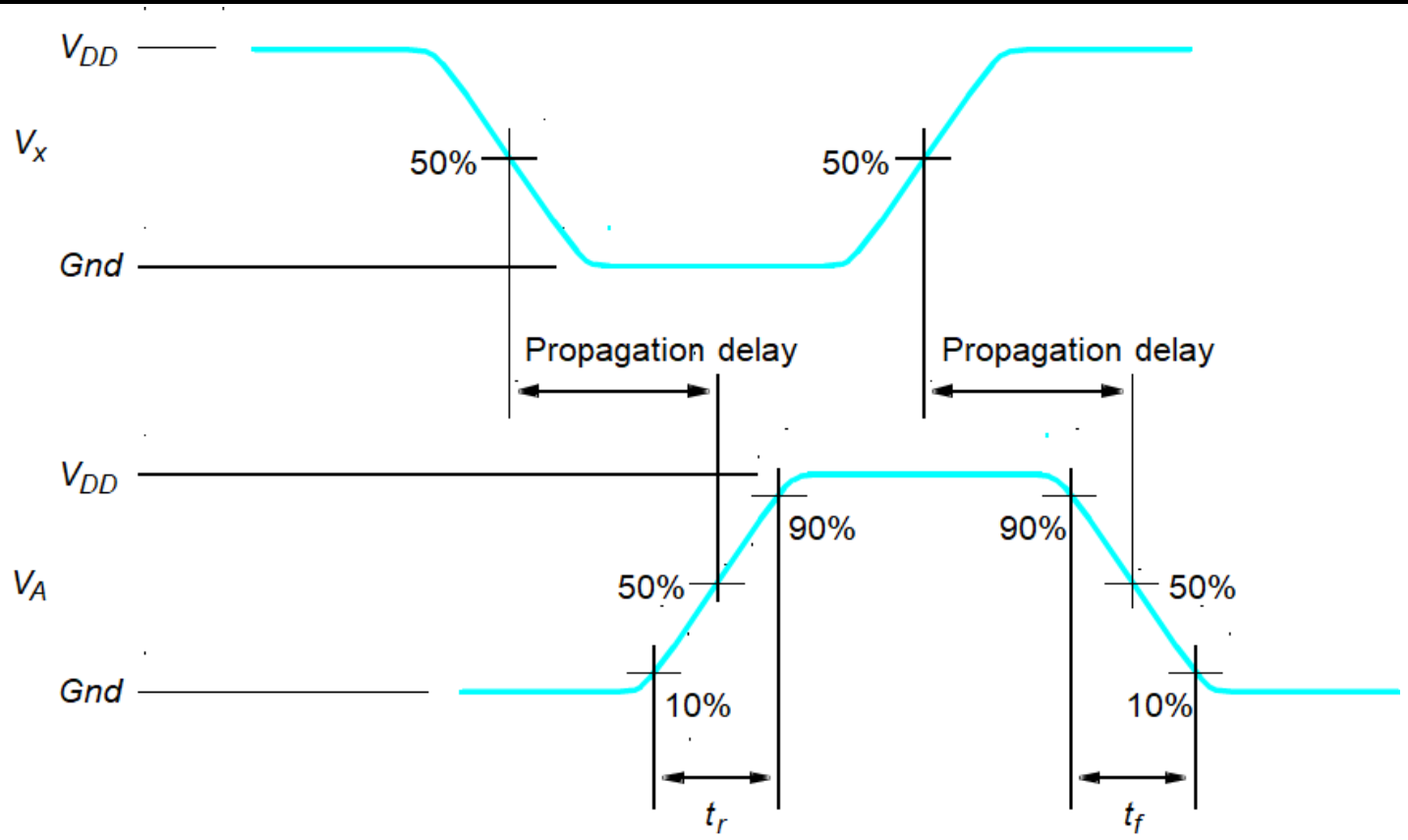
- The time needed for V_A to change from *low to high* is called the *rise time*
  - i.e time elapsed from when V_A is at 10% of V_{DD} until it reaches 90% of V_{DD}

Fall Time



- The time needed for V_A to change from *high to low* is called the *fall time*
  - i.e time elapsed from when V_A is at 90% of V_{DD} until it reaches 10% of V_{DD}

Propagation Delay – (1)



- The total amount of time needed for the change at Vx to cause a change in VA:
  - This interval is known as the *propagation delay* (*tp*)
  - i.e the time from when Vx reaches 50% of VDD until the time VA reaches the same level

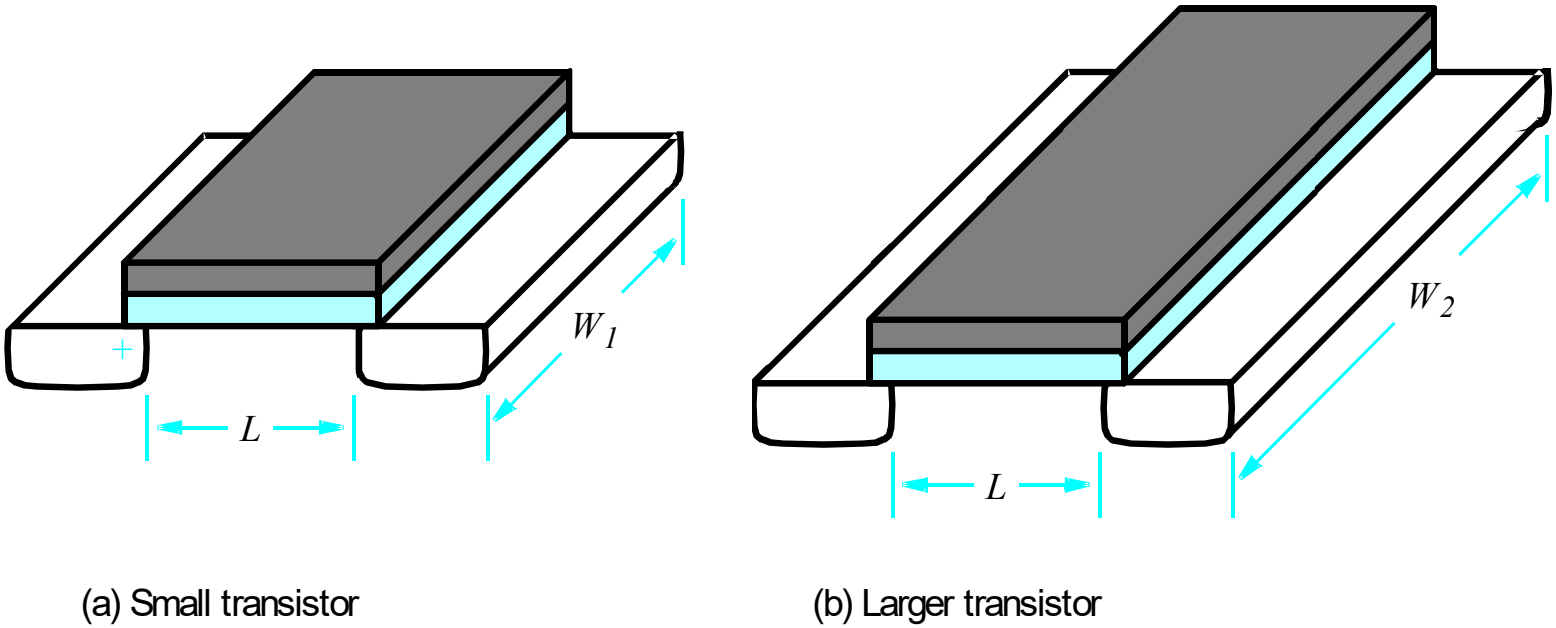
Propagation Delay – (2)

- Propagation delay is given as:

$$t_p \cong \frac{1.7\,C}{k_n' \frac{W}{L} V_{DD}}$$

- This expression specifies that speed of the circuit depends on:
  - C
  - W/L (dimension of the transistor or transistor size)

Transistor Sizes



(a) Small transistor

(b) Larger transistor

- In logic circuits,
  - *L* is usually set to the minimum value that is permitted according to the specifications of the fabrication technology used (technology node i.e 180nm, 65nm … 16nm, 7nm)
  - The value of *W* is chosen depending on the amount of current flow, hence propagation delay, that is desired

FPGA Speed Grade

- FPGA speed grade indicates the device speed:
  - Check the vendor documentation on speed grade
  - For example: Intel MAX and Classic devices use the speed grade to indicate the delay in nanoseconds (ns) through a macrocell in the device.
    - For example, a MAX device with a -10 speed grade has a delay of 10 ns through a macrocell.
  - Devices with low speed grade numbers run faster than devices with high speed grade numbers.
    - While true in general, again check the vendor documentation.

Sample Code: EPF10K130EQC240-1X

EPF 10K130E	Q	C	240	-1	X
FLEX 10K130E	Quad flat pack	Commercial range	240 pins	-1 speed grade	Has phase-locked loops (PLLs)