School of Electrical Engineering and Computer Science
National University of Sciences & Technology (NUST)

Home Assignment No-5(CLO2)

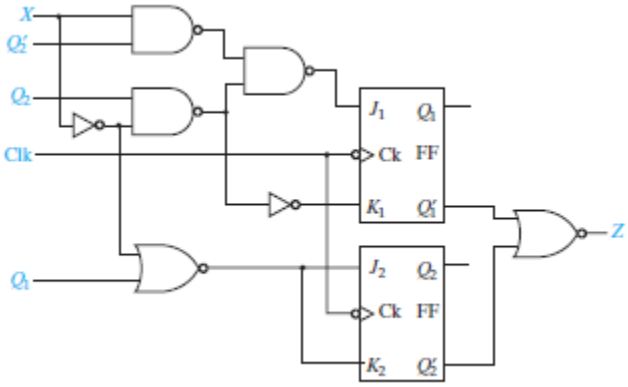
Subject:	**Digital Logic Design**	Marks :	**50**
Course:	**BEE-12CD**	Issue:	**16 Dec 2021**
Teacher:	**Engr. Arshad Nazir**	Due:	**23 Dec 2021**

Instructions:

- ✓ *Attempt the given problem. No late submissions will be accepted unless a prior approval from the teacher is obtained under extremely genuine reasons. The assignments submitted after due date/time will be graded **zero**.*
- ✓ *University has zero tolerance for plagiarism and serious penalties apply. All assignments mutually copied will be graded **zero** and recurrence will result in award of **zero** marks out of total assignments weight age.*
- ✓ *All the students will submit a certificate with the assignment work stating the originality of their efforts and no copying from others.*
- ✓ *Note that **FIVE** marks have been reserved for neat work, table of contents, and certificate to be attached on the page following title page.*

Problem No-1 Consider the following sequential circuit that has one input x, one output z and two JK flip-flops shown with symbols Q_1 and Q_2.

a. Construct a transition table and state graph for the circuit.
b. Draw a timing diagram for the circuit showing the clock, X, Q_1, Q_2 and Z. Use the input sequence X=01100 and assume that X changes midway between falling and rising clock edges.
c. What is the output sequence for the given input sequence?



"Good Luck"