School of Electrical Engineering and Computer Science
National University of Sciences & Technology (NUST)

Practice Assignment No-5

Subject:	**Digital Logic Design**	Course:	**BEE-12CD**
Teacher:	**Engr. Arshad Nazir**	Issue:	**11 Dec 2021**

- ✓ *This is a non-graded assignment prepared to enhance problem-solving skills of students from chapters 5&6 of the textbook.*
- ✓ *The students are advised to attempt it any time of their convenience.*

Problem No-1: A sequential circuit of the form shown in figure P-1 is constructed with two D flip-flops and external gates.

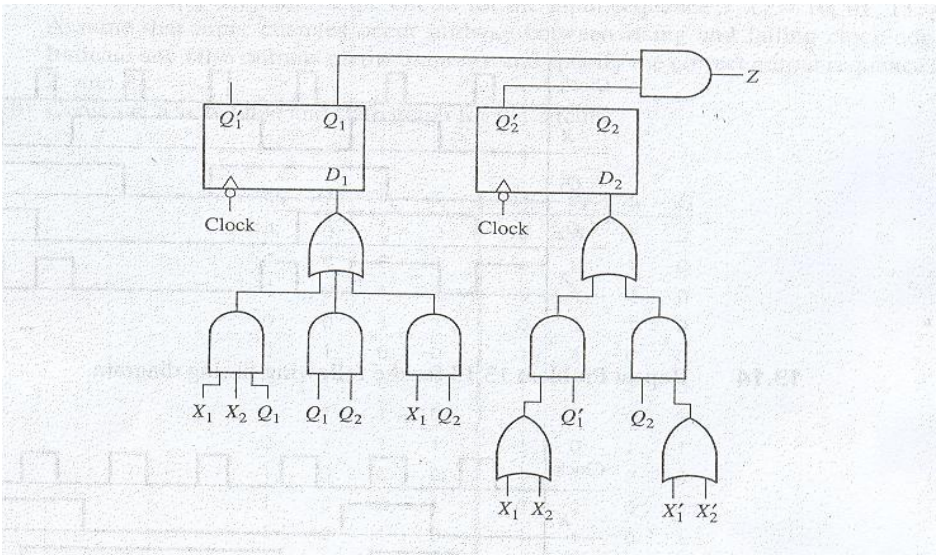


Figure P-1 Sequential Circuit to be analyzed

a. List the state table and draw state diagram for the given circuit.
b. Construct a timing chart for the circuit for the given input sequence X_1X_2=10, 01, 10, 11, 11, and 10. Indicate at what times Z has the correct value and specify the correct output sequence. (Assume that X changes midway between falling and rising clock edges.) Initially, Q_1=Q_2=0.

Problem No-2: Design a sequential circuit with two JK flip-flops A and B and two inputs E and x. If E =0, the circuit remains in the same state regardless of the value of x. When E=1 and x=1, the circuit goes through the state transitions from 00 to 01 to 10 to11, back to 00, and repeats. When E=1

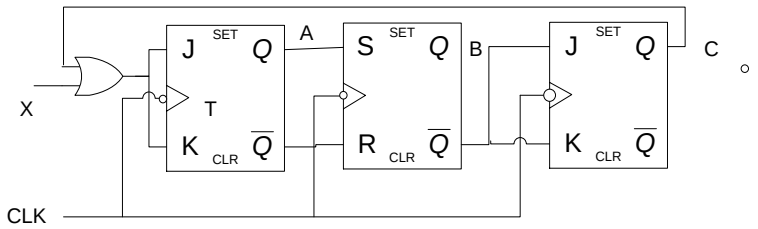
and x=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01, back to 00, and repeats.

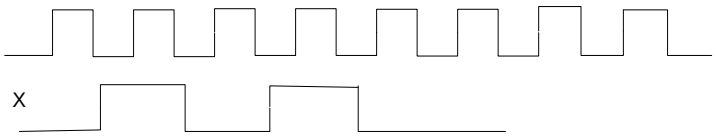
Problem No-3: A serial logic unit has two 8-bit shift registers, X and Y, shown in figure P-8. Inputs K_1 and K_2 determine the operation to be performed on X and Y. When St=1, X and Y are shifted into the logic circuit one bit at a time and replaced with new values. If K_1K_2=00, X is complemented and Y is unchanged. If K_1K_2=01, X and Y are interchanged. If K_1K_2=10, Y is reset to 0 and each bit of X is replaced with the exclusive-OR of the corresponding bits of X and Y, that is, the new x_i is x_i yi. If K_1K_2=11, X is unchanged and Y is set to all 1's.

Problem No-4: We have a new flip flop with three inputs S, R and T (in addition to a trailing edge triggered clock input). No more than one of these inputs may be 1 at any time. The S and R inputs behave exactly as they do in an SR flip flop (that is S puts a 1 into the flip flop and R puts a 0 in the flip flop). The T input behaves as it does in a T flip flop (that is it causes the flip flop to change state).

a. Show State diagram for the flip flop.
b. Write a state equation of output of S, R, T and Q.
c. Create an excitation table for the flip flop.

Problem No-5: Complete the timing diagram for the state of each flip flop and output, where shown. All flip flops are trailing edge triggered. (Assume that three flip flops are all initially 0).





X

A

B

C

Problem No-6: For the State table and each of the state assignment shown. Design a system using D flip flops.

Q	Q (t+1)		Z	
	x= 0	x=1	x= 0	x=1
A	B	C	1	0
B	D	A	0	0
C	B	C	1	1
D	D	A	1	0

(a)

Q	Q1	Q2
A	0	0
B	0	1
C	1	0
D	1	1

(b)

Q	Q1	Q2
A	0	0
B	0	1
C	1	1
D	1	0

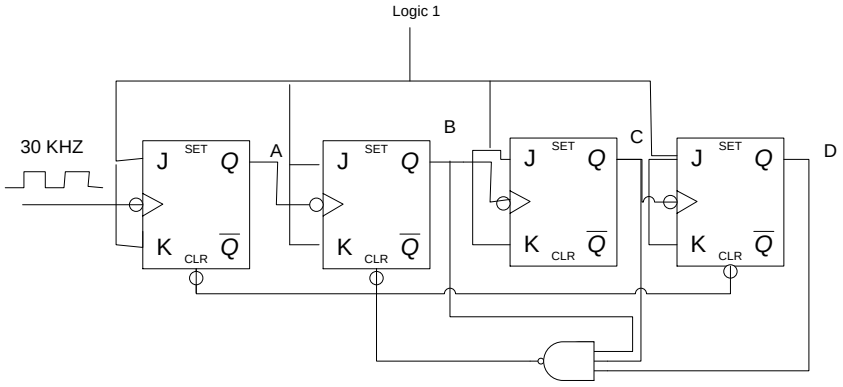
(c)

Q	Q1	Q2
A	0	0
B	1	1
C	1	0
D	0	1

Design each part and find out which state assignment gives optimized design (Less no. of gates & less no of inputs to gates).

Problem No-7: Design an up/down Saturating Counter with two JK flips Flops). A & B, and one input x. If x = 0 it counts 0,1,2,3,3,……..; if x =1 it counts 3,2,1,0,0,……..

Problem No-8: Determine the count sequence and determine frequency at D output.



Problem No-9: Design of Stepper Motor of Robot

A Stepper motor is a motor that rotates in steps rather than in a continuous motion typically 15° per step. Magnetic coils or winding within the motor must be energized and de-energized in a specific sequence in order to produce this stepping action. Digital signals are normally used to control the current in each of the motor's coils. Stepper, motors are used extensively in situation where precise position control is needed, such as in position of read/write heads or magnetic digits, in controlling printer heads in printers and in robots.

Figure shown is a diagram of typical stepper motor with four coils. For the motor to rotate properly coil 1 & 2 motor always be in opposite state, that is

when coil 1 is energized, coil 2 is not and vice versa. Likewise coils 3 and coil 4 must always be in opposite state.

Since the stepper motor can rotate wither clockwise a center clockwise we have direction input D, which is used to control the direction of rotation. For CW rotation to occur we have D = 0 & state of counter BA, must follow the sequence 11, 10, 00, 01, 11, 10,… And so as it clocked by the step input signal. For CCW rotation D =1 and center must follow the sequence 11, 01, 00, 10, 01, and so on

Design the stepper motor circuit using JK flips flop and appropriate logic gates.

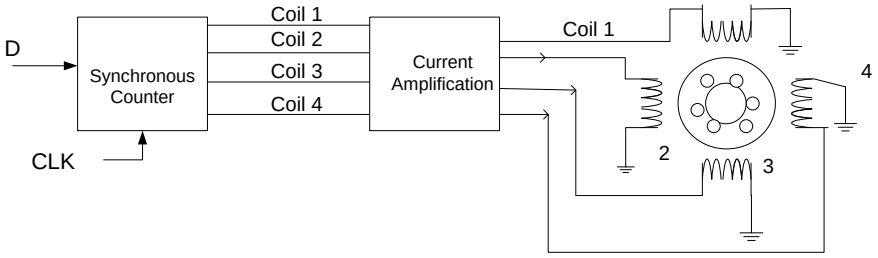


Figure P9: Stepper Motor

Problem 10: The two sequential circuits N_1 and N_2 with one input x and one output y are described by the following state tables:

N_1

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	B	A	0	0
B	C	D	0	1
C	A	C	0	1
D	C	B	0	0

N_2

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
S_0	S_3	S_1	0	1
S_1	S_3	S_0	0	0
S_2	S_0	S_2	0	0
S_3	S_2	S_3	0	1

Figure P-10 State Tables

a. Draw the state graphs for both the circuits.

b. Using Implication table determine the circuit equivalence.

c. Starting from state A for N_1, state S_2 for N_2, and input Sequence1101110, determine the output sequence and verify that both are equivalent circuits.

Problem No-11: The 4-bit Johnson counter advances through the sequence 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000 and repeat.

a. Using the standard counter design process show how to implement this count sequence using SR flip-flops.

b. Show the timing diagram for the counter.

Problem No-12: A serial logic unit has two 8-bit shift registers, X and Y, shown in figure P-12. Inputs K_1 and K_2 determine the operation to be performed on X and Y. When St=1, X and Y are shifted into the logic circuit one bit at a time and replaced with new values. If K_1K_2=00, X is complemented and Y is unchanged. If K_1K_2=01, X and Y are interchanged. If K_1K_2=10, Y is reset to 0 and each bit of X is replaced with the exclusive-OR of the corresponding bits of X and Y, that is, the new x_i is x_i yi. If K_1K_2=11, X is unchanged and Y is set to all 1's.

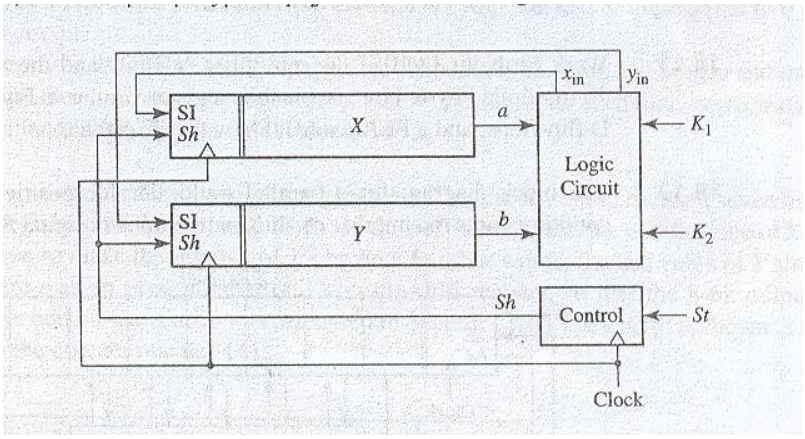


Figure P-12 Serial Logic Unit

a. Derive the logic equations for x_{in} and $y_{in.}$

b. Derive the state graph for the control unit. Assume that once St is set to 1, it will remain 1untill all 8 bits have been processed. Then, St will be changed back to zero some time before the start of the next computation cycle.

c. Realize the logic circuit using two 4-to-1 multiplexers and a minimum number of added gates.

Problem No-13: Design a Mealy sequential circuit to convert a 4-bit binary number in the range 0000 through 1010 to its 10's complement. (The 10's complement of a number N is defined as 10-N.) The input and output should be serial

with the least significant bit first. The input x represents the 4-bit binary number, and the output z represents the corresponding 10's complement. After four time steps, the circuit should be reset to the starting state regardless of the input sequence.

Find a state table with a minimum number of states. Design the circuit using three JK flip-flops and external gates as required. Assign 000 to the reset state.

Problem No-14: Draw the logic diagram of a 4-bit universal shift register with four D flip-flops and four 4:1 line multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table

Selection Inputs S_1 S_0	Register Operation
0 0	Complement Output
0 1	Parallel Load
1 0	Shift Left
1 1	Synchronous Clear

Problem No-15: Design a counter using SR flip-flops and logic gates which counts in the sequence 000, 010, 011, 101, 110, (repeat) 000…….. What will happen if the counter is started in states 001, 100, and 111?

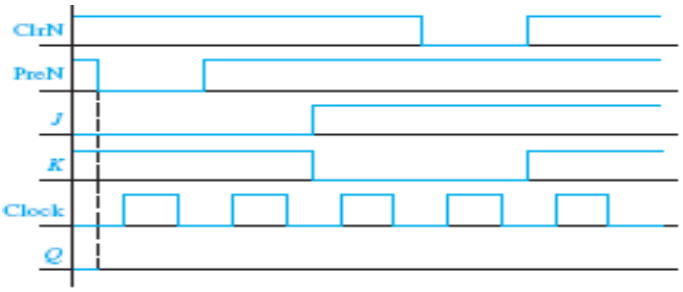
Problem No-16: Construct the state diagram for a Mealy sequence machine that will detect the following sequences: x=01101 or 01111. If input sequence x=01101 is met, cause z_1=1. If x=01111, cause zz_2=1. Each input sequence may overlap with itself or the other sequence.

Problem No-17 a. Construct a JK flip-flop using a D flip-flop, two tri-state buffers and one inverter.

b. A PN flip-flop has four operations: Clear to 0, No change, Complement output, and Set to 1, when inputs P and N are 00, 01, 10, and 11, respectively:-

i. Tabulate the characteristics table
ii. Derive the characteristics equation
iii. List the excitation table
iv. Show that the PN flip-flop can be converted to a T flip-flop

c. Draw the state diagram and complete the following timing diagram for a JK flip-flop with a falling-edge trigger and asynchronous ClrN and PreN inputs.



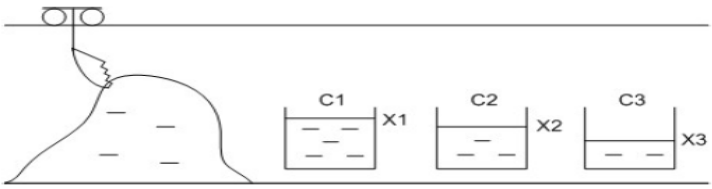
Problem No-18 A Moore finite state machine has one input x and one output z. The output becomes 1 and remains 1 thereafter when at least two 0's and two 1's have occurred as inputs, regardless of the order of the appearance. Assuming this is to be implemented as a Moore machine:-

a. Draw a state transition diagram for the machine. Hint:You can do this in nine states.

b. Make straight binary assignment to the states and derive the flip-flop input equations and output equation for your design.

Draw the logic diagram of the circuit using negative edge-triggered JK and external NAND gates as required.

Problem No-19: Three containers C_1, C_2, and C_3 as displayed in the figure below are supplemented by some material. The containers are equipped with sensors X_1, X_2, and X_3, indicating the level of material in particular containers. Logical 1 signalizes the low amount of material and thus the demand for service. Design a circuit (Moore FSM) controlling the operation of trolley developing material to the containers.



Block scheme of a sample sequential logics in a factory.

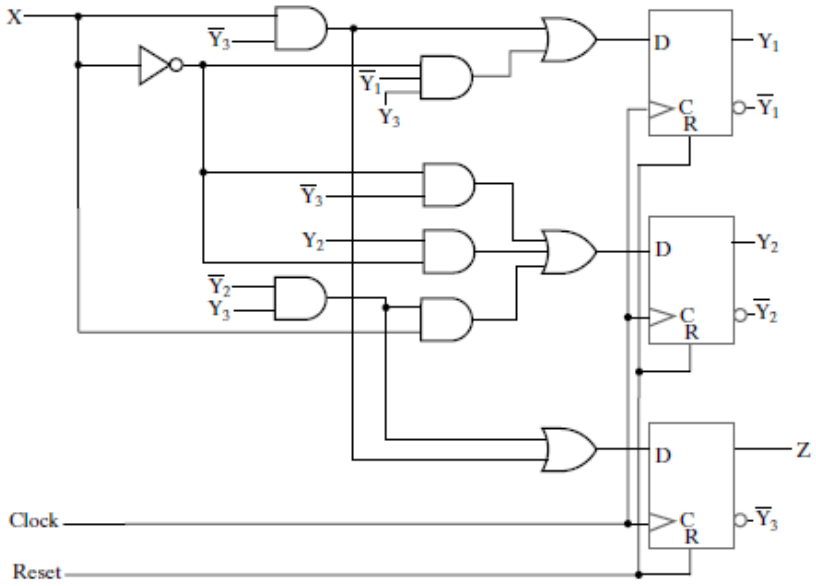
The controller operates as per the following enabling logic:

- If every container indicates low amount of material, service should be provided in the order: C_1, C_2, C_3, C_1, C_2, C_3, and C_1…

- If two of the three containers are empty, service is provided alternately: C_a, C_b, C_a, C_b, and Ca…
- If one of the three boxes is empty, provide the service to it.
- If no sensor is active, there is no action.
- C_1 has higher priority than C_3.

Use Gray state assignment, D flip-flops and NAND gates for your design.

Problem No-20: The circuit given in the following figure is to be redesigned to cut its cost



a. Find the state table for the circuit and replace the state codes with single letter identifiers. States 100 and 111 were unused in the original design.

b. Check for and combine equivalent states.

c. Make a state assignment such that the output is one of the state variables

d. Find the gate-input costs of the original circuit and your circuit, assuming that the gate-input cost of D flip-flops is 14. Is the cost of the new circuit reduced?

Problem No-21: Design a 2-bit counter that behaves according to the two control inputs I_0 and I_1 as follows: I_0,I_1=0,0: stop counting; I_0,I_1=0,1: counts up by 1; I_0,I_1=1,0: counts down by 1; I_0,I_1=1,1: count by two.

a. Draw the state diagram and the state transition table.

b. Implement the counter using D flip-flops.

c. Assume that only 2-input NAND, NOR, XOR, XNOR gates are available. Braw the schematics for your minimum gate count application.

Problem No-22: Draw the logic diagram of a 4-bit register with four JK flip-flops and four 4:1 multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table

s_1	s_0	Register Operation
0	0	No change
0	1	Complement the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

Problem No-23: Obtain a minimal state table for a clocked synchronous sequential network having a single input line x, in which the binary symbols 0 and 1 are applied, and a single output line z. The network is to analyze each sequence of four binary digits and produce the corresponding 2's complement of the4-bit sequence. Assume each 4-bit sequence is occurring with the least significant bit first. As an example of input/output sequences that satisfy the conditions of the network specifications is:

X=0101000111000100
Y=0110000110110111

Problem No-24: You are to design the control for an automatic candy vending machine. The candy bars inside the machine cost 25 cents, and the machine accepts, nickels, dimes, and quarters only. The inputs to the control are a set of three signals that indicate what kind of coin has been deposited, as well as reset signal. The control should generate an output signal that causes the candy to be delivered whenever the amount of money received is 25 cents or more (no change is returned). Once the candy has been delivered, some external circuitry will generate a reset signal to put the control back into its original state. Identify your inputs and outputs, and draw the state diagram that implements this finite state machine.

Problem No-25: Design a Mealy sequential circuit which adds 5 to a binary number in the range 0000 through 1010. The input and output should be serial with the least significant bit first. Find a state table with a minimum number of states. Design the circuit using NAND gates, NOR gates and three flip-flops. Any solution which is minimal for your state assignment and uses nine or fewer gates and inverters is acceptable. (Assign 000 to the reset state.)

"Good Luck"