EE-421: Digital System Design

Programmable Logic Devices

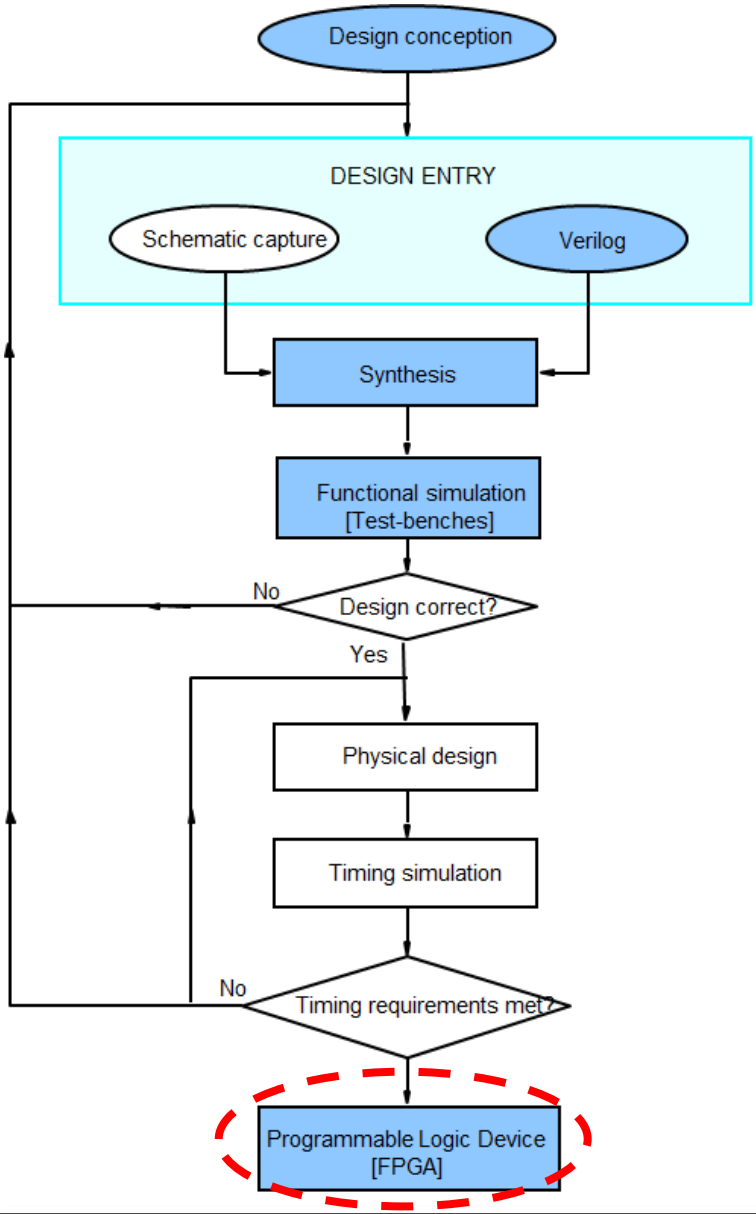
Dr. Rehan Ahmed [rehan.ahmed@seecs.edu.pk]

NUST

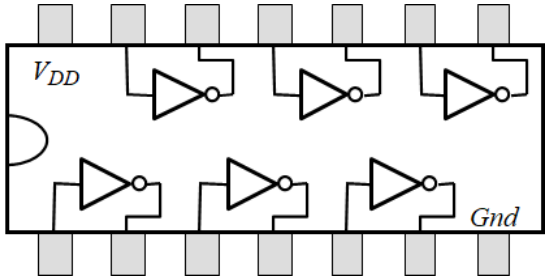
SCHOOL OF ELECTRICAL ENGINEERING &
COMPUTER SCIENCE (SEECS)

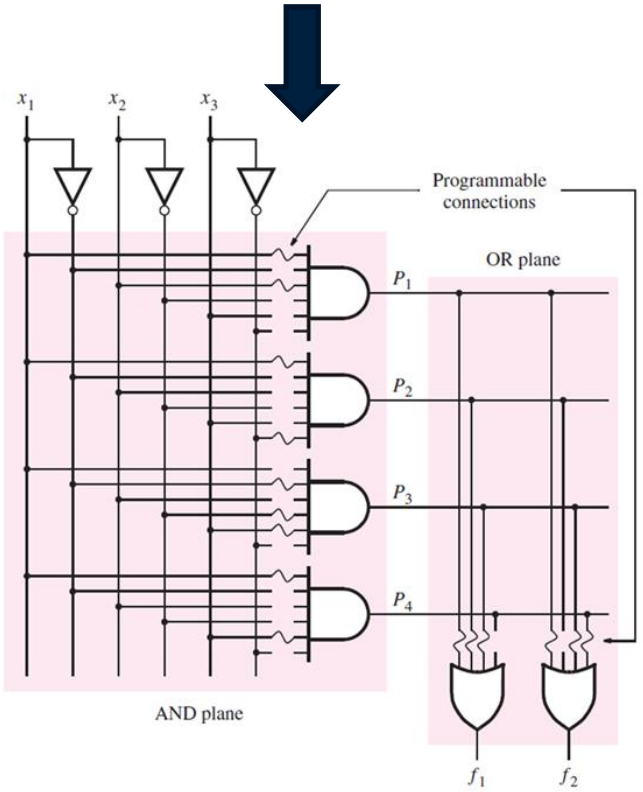
RISC
RESEARCH LAB

Where are we Heading?

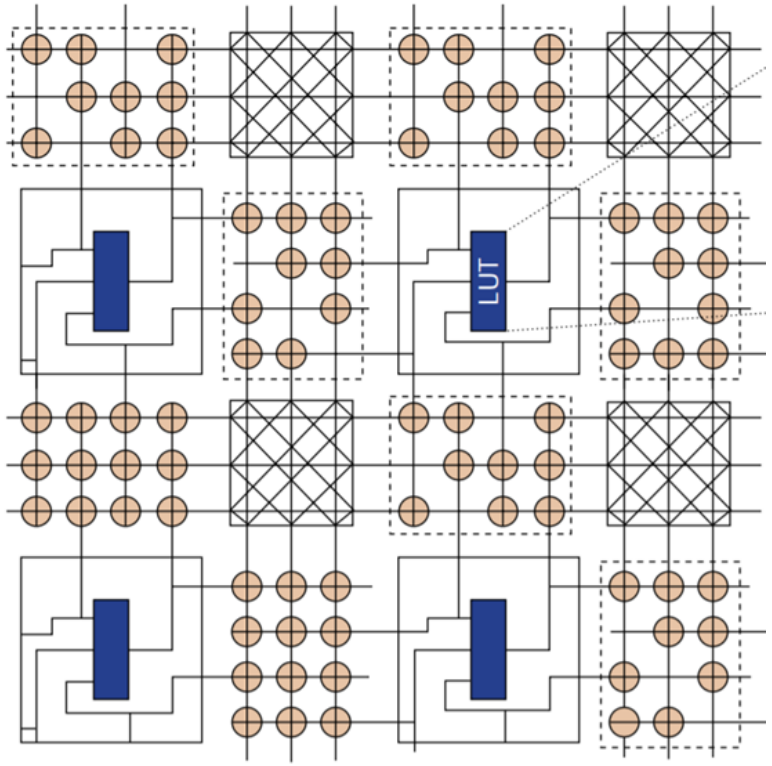


Programmable Logic Devices (computing platforms):





How did we get here?

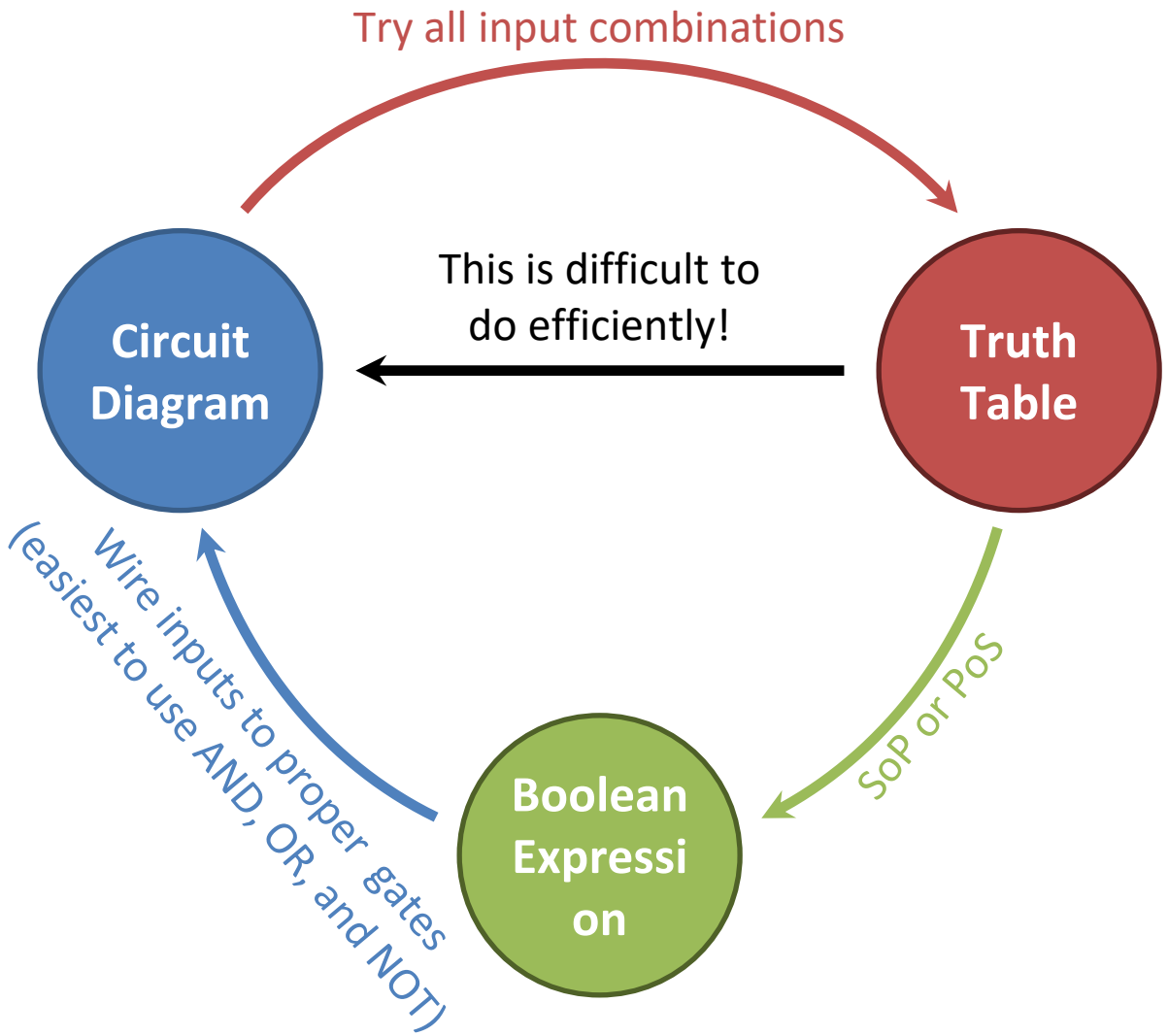


Review: SOP and POS

Type of Circuits

- *Digital Systems* consist of two basic types of circuits:
  - Combinational Logic (CL)
    - Output is a function of the inputs only, not the history of its execution
    - e.g. circuits to add A, B (ALUs)
  - Sequential Logic (SL)
    - Circuits that “remember” or store information
    - a.k.a. “State Elements”
    - e.g. memory and registers (Registers)

Converting Combinational Logic



Representations of Combinational Logic

- ✓ Text Description
- ✓ Circuit Diagram
  - Transistors and wires
  - Logic Gates
- ✓ Truth Table
- ✓ Boolean Expression

✓ *All are equivalent*

Three Variable Minterms and Maxterms

Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \overline{x}_1\overline{x}_2\overline{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \overline{x}_1\overline{x}_2 x_3$	$M_1 = x_1 + x_2 + \overline{x}_3$
2	0	1	0	$m_2 = \overline{x}_1 x_2\overline{x}_3$	$M_2 = x_1 + \overline{x}_2 + x_3$
3	0	1	1	$m_3 = \overline{x}_1 x_2 x_3$	$M_3 = x_1 + \overline{x}_2 + \overline{x}_3$
4	1	0	0	$m_4 = x_1\overline{x}_2\overline{x}_3$	$M_4 = \overline{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1\overline{x}_2 x_3$	$M_5 = \overline{x}_1 + x_2 + \overline{x}_3$
6	1	1	0	$m_6 = x_1 x_2\overline{x}_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$
7	1	1	1	$m_7 = x_1 x_2 x_3$	$M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

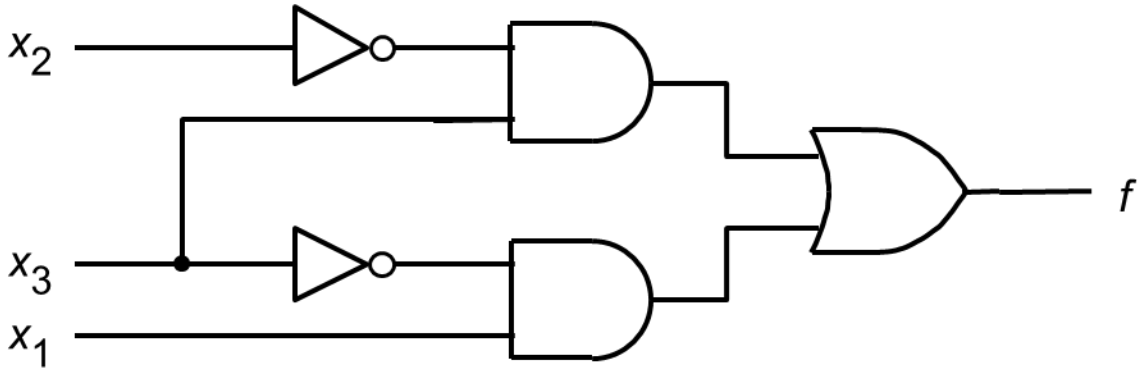
Activity: A Three-Variable Function

Row number	x_1	x_2	x_3	$f(x_1, x_2, x_3)$
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	1
7	1	1	1	0

- What is the function f?
- Draw the logic circuit

Activity Answer

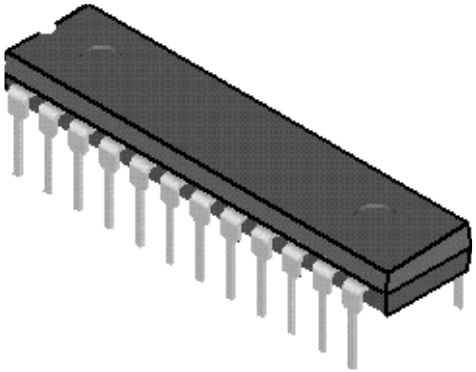
- f=x1'x2' +x1'x2 +x1x2



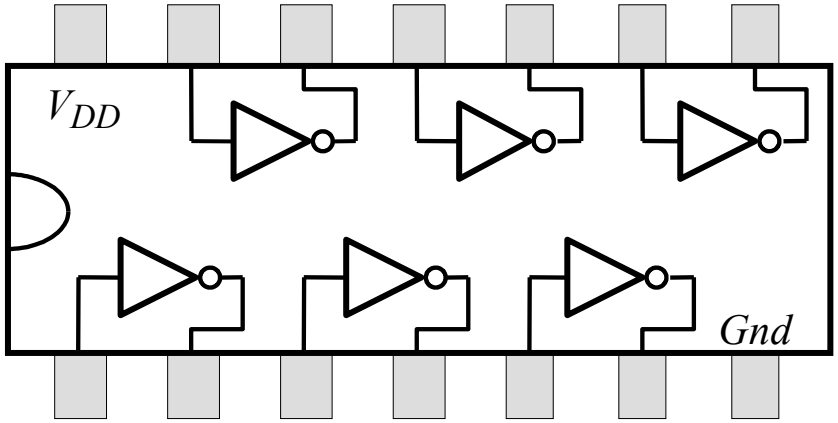
- How would you implement the above circuit in HW?

Standard Chips

Review: Standard Chips



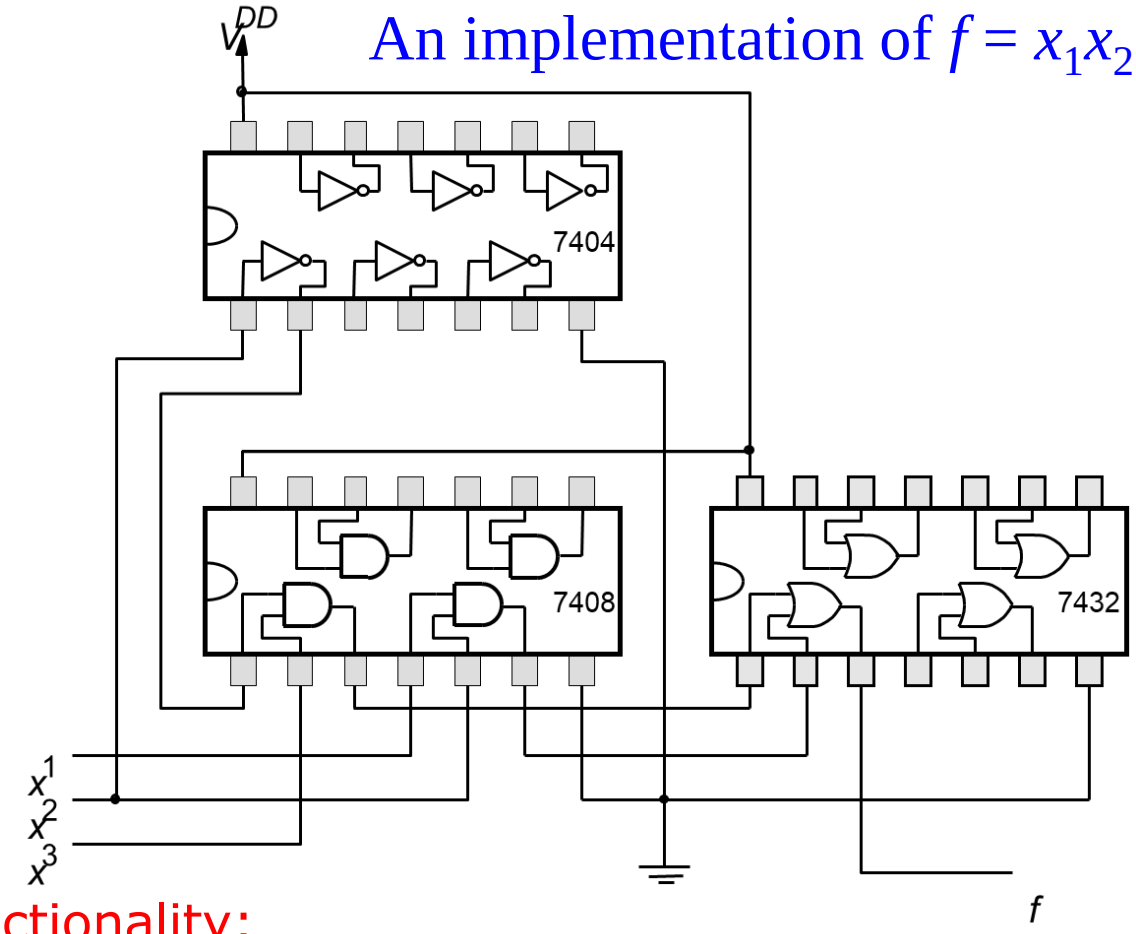
(a) Dual-inline package



(b) Structure of 7404 chip

Review: Standard Chips

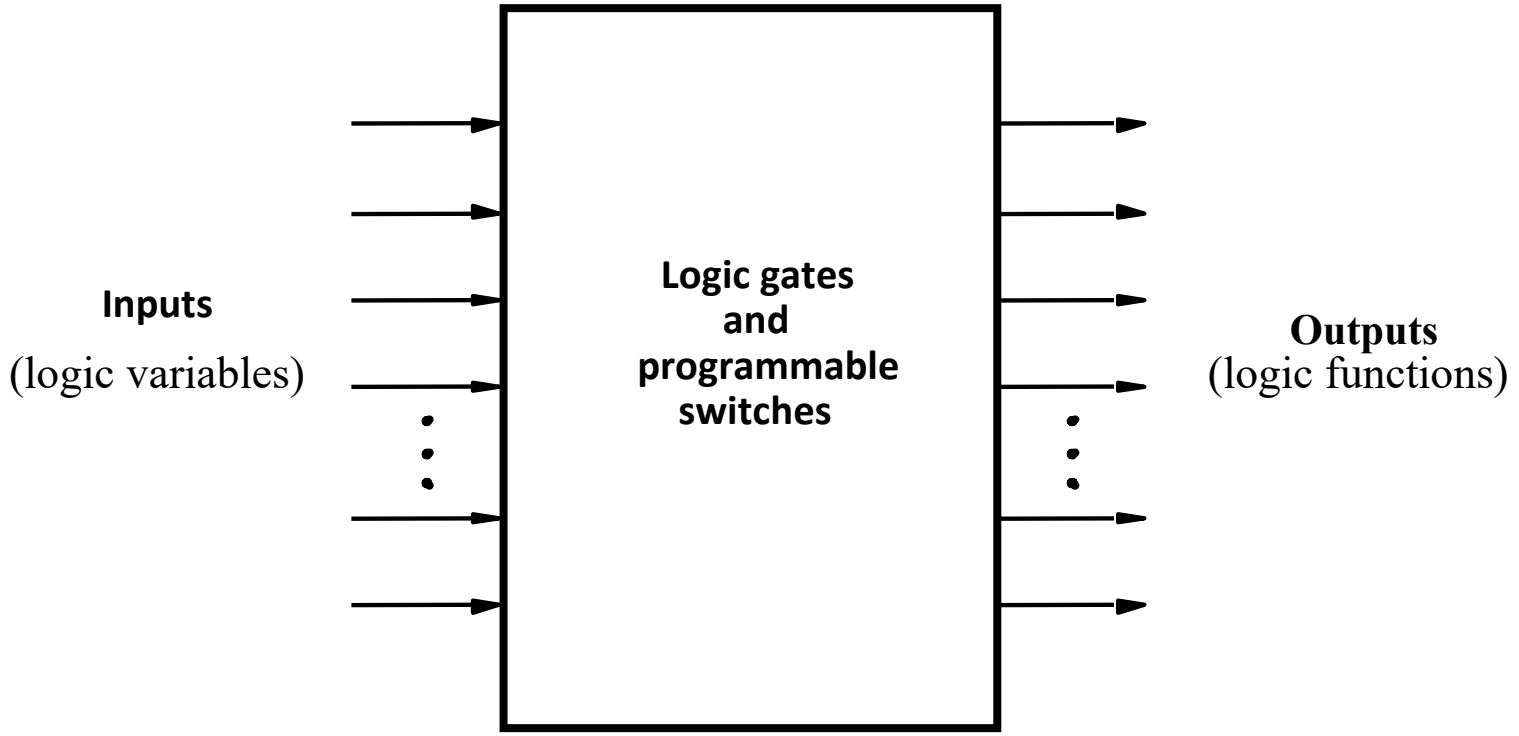
An implementation of $f = x_1x_2 + \overline{x}_2x_3$.



- Limitations:
  - Fixed functionality:
    - Cannot be tailored to suit a particular design situation
  - Each chip contains only a few logic gates:
    - Inefficient for building large circuits

Programmable Logic Devices:
PLA,
PAL,
CPLD
and
FPGA

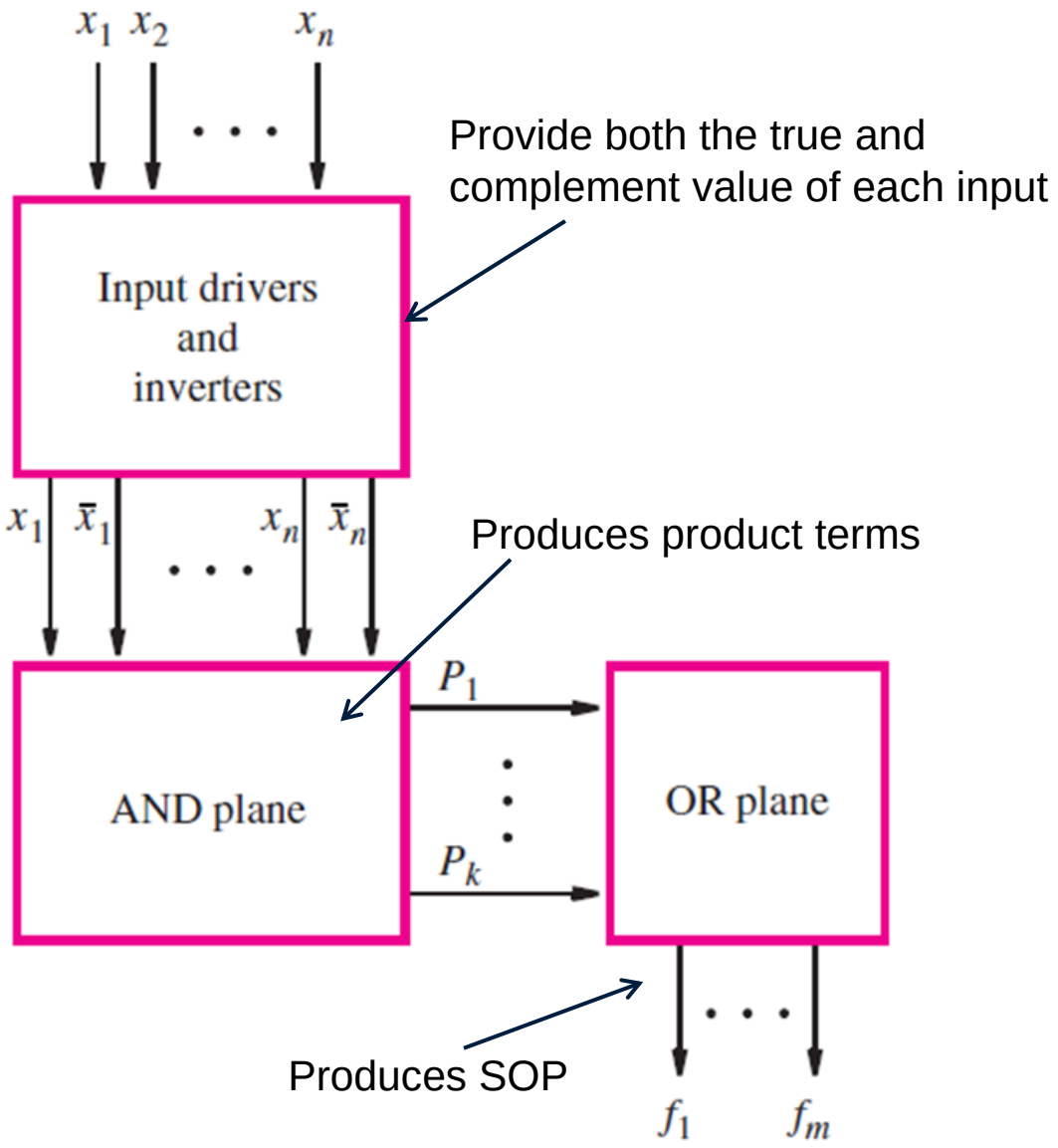
Programmable Logic Devices (PLD)



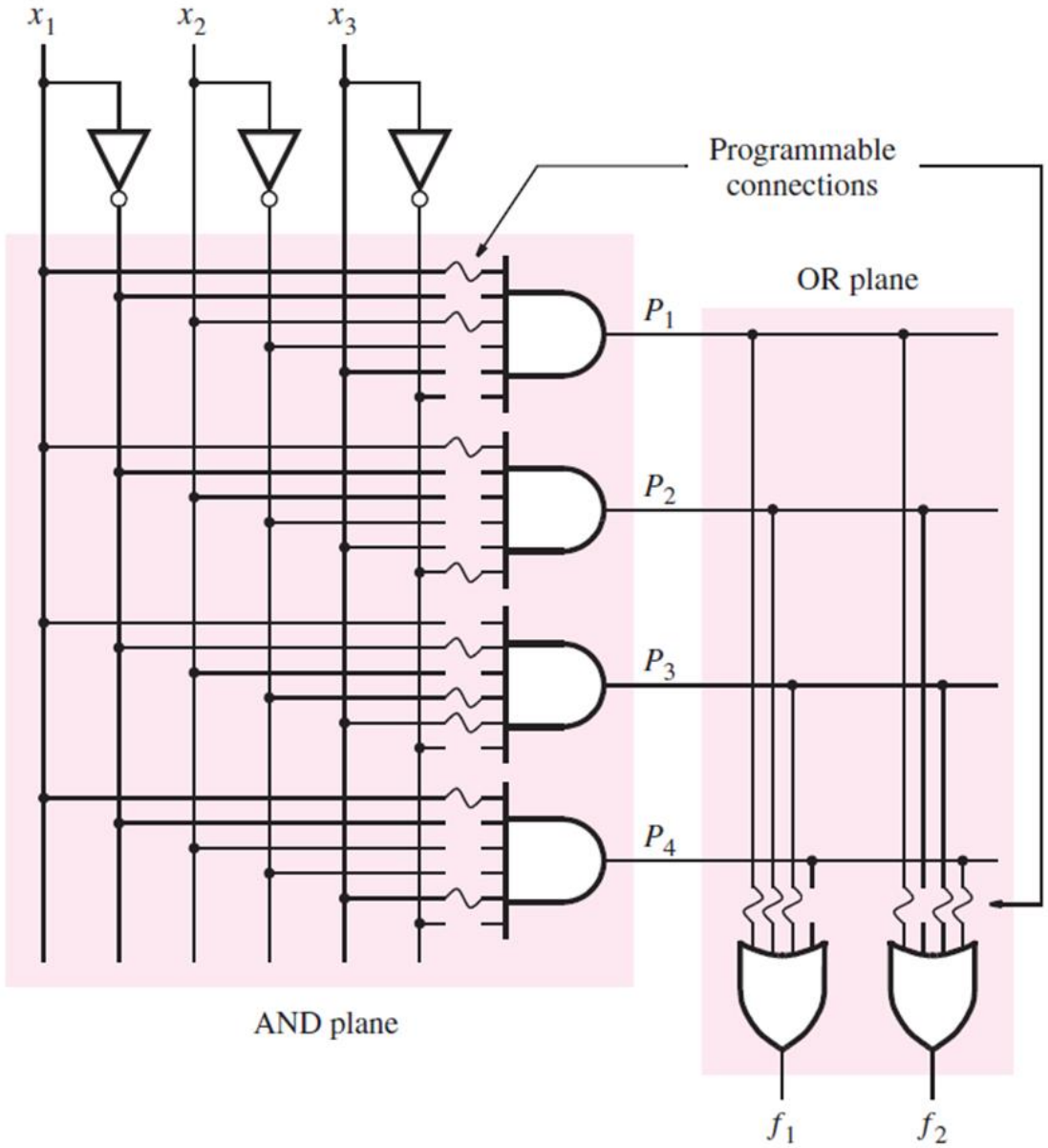
- PLD as a black box: (introduced in 1970s)
  - Inside: *Logic gates and Programmable Switches*
    - customizable in different ways -> *programmable switches* that allow the internal circuitry in the chip to be configured in many different ways.
    - The switches are programmed by the end user, rather than when the chip is manufactured !!

Programmable Logic Array (PLA)

- Based on the idea:
  - *Logic function can be realized in SOP form*



Inside PLA

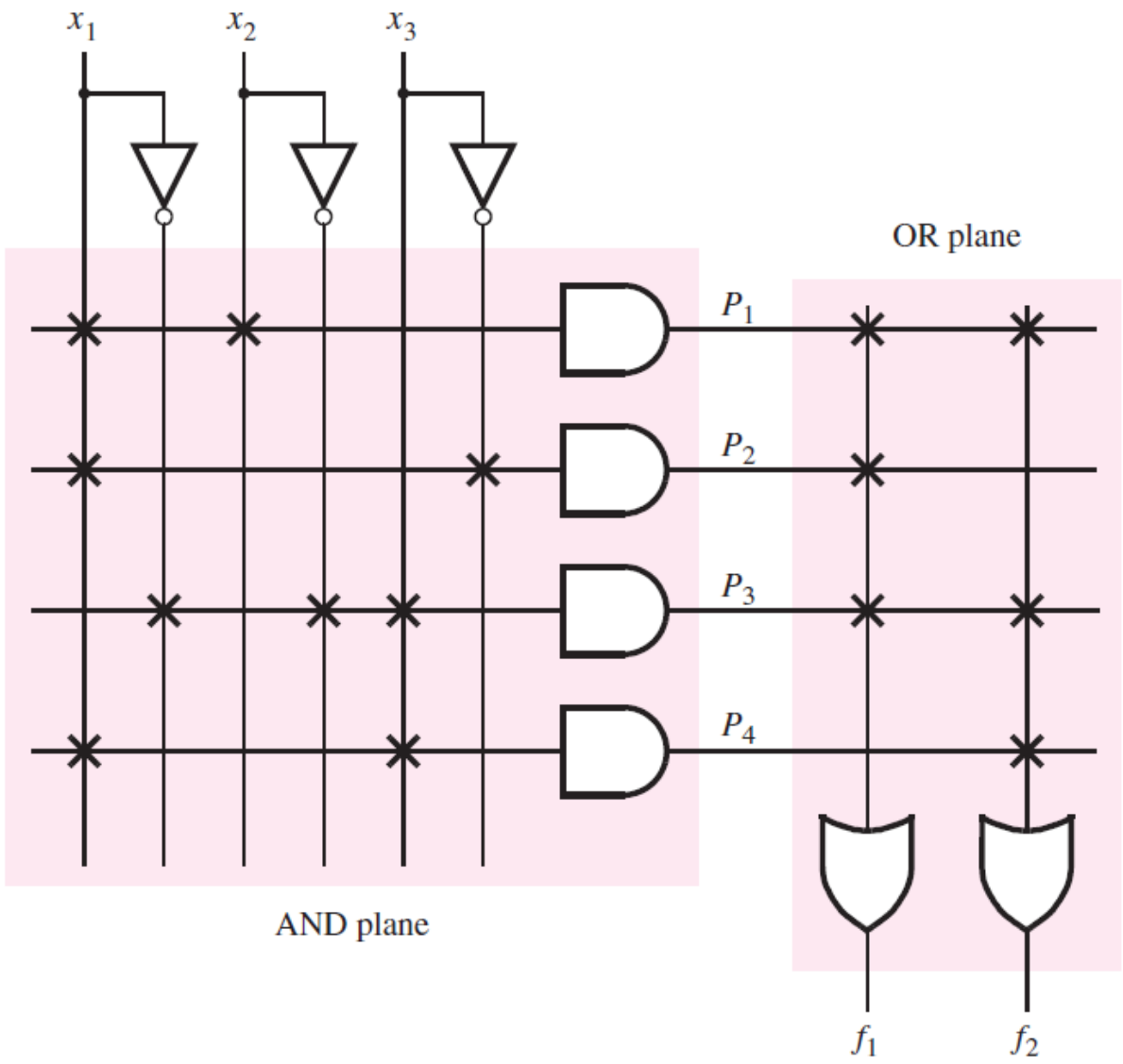


- Programming AND and OR planes differently could implement various functions.
  - Constraints:
    - size of AND/OR planes

- What is f1 and f2?

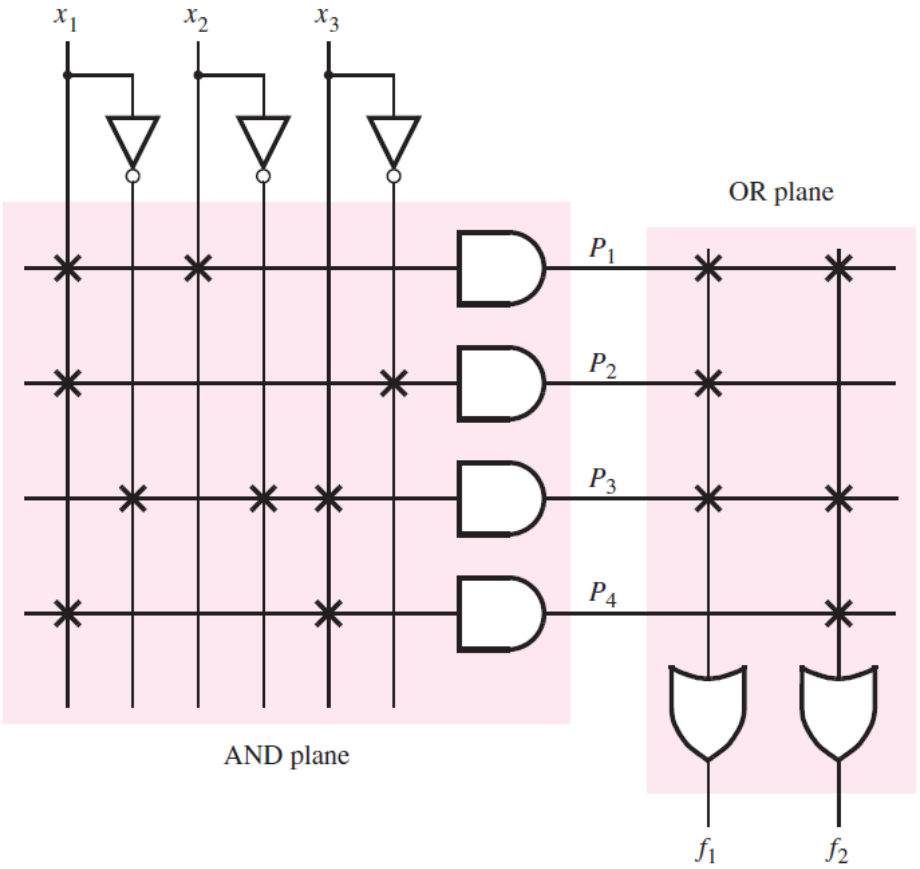
- $f1 = x1x2 + x1x3' + x1'x2'x3.$
- $f2 = x1x2 + x1'x2'x3 + x1x3$

Customary Schematic of PLA



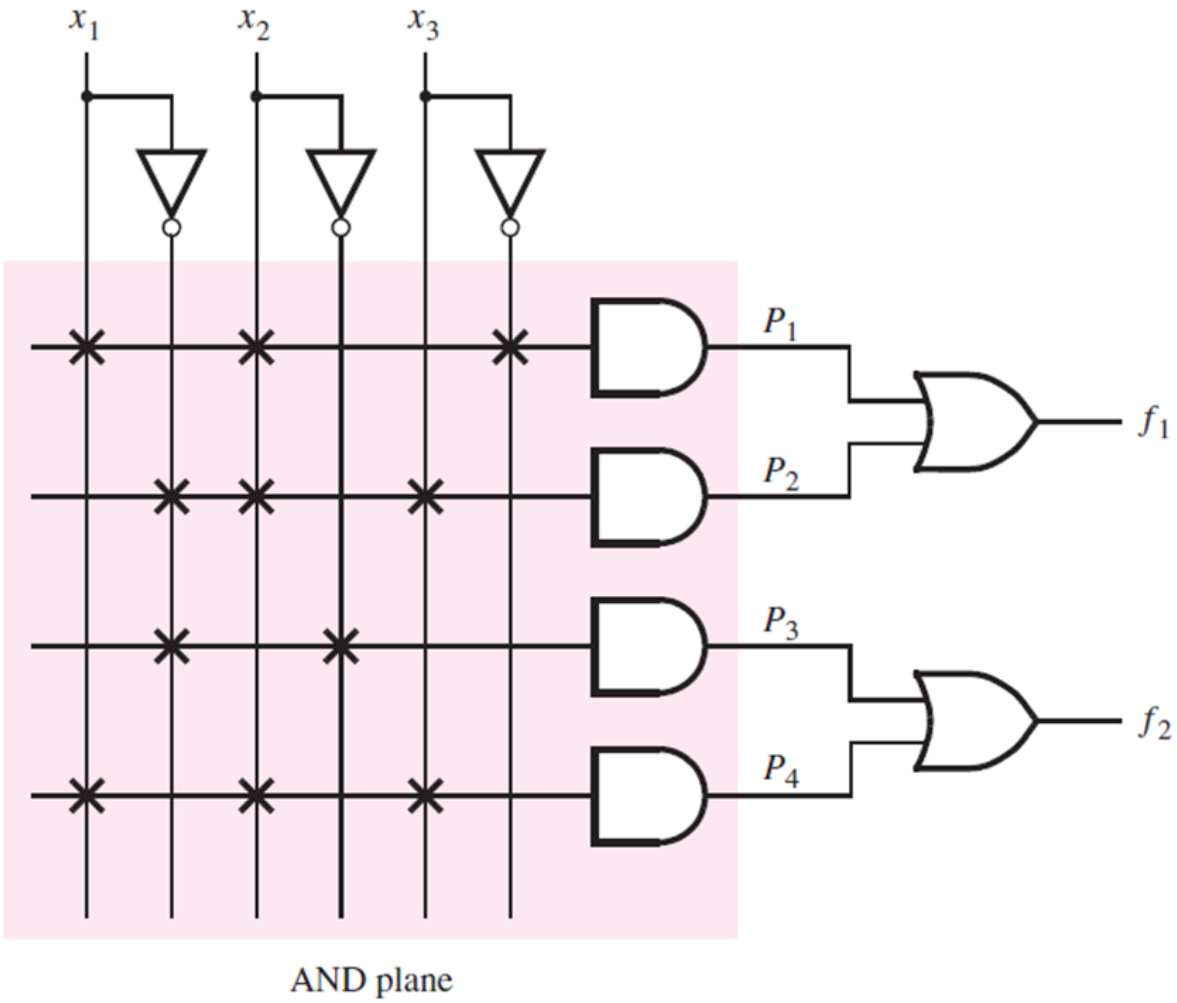
- Programming AND and OR planes differently could implement various functions.
  - Constraints:
    - size of AND/OR planes
- Typical commercially available PLAs:
  - 16-inputs
  - 32 product terms
  - 8 outputs

Limitations of PLA



- Historically, the programmable switches presented two difficulties for manufacturers of these devices:
  - they were hard to fabricate correctly, and
  - they reduced the speed performance of circuits implemented in the PLAs.
- Both programmable planes occupy larger area

Programmable Array Logic (PAL)



AND plane

- AND plane: Programmable
- OR plane: **Fixed**

- Less flexible than PLA but improved speed-performance

- What is f1 and f2?

$$f_1 = x_1 x_2 \bar{x}_3 + \bar{x}_1 x_2 x_3$$

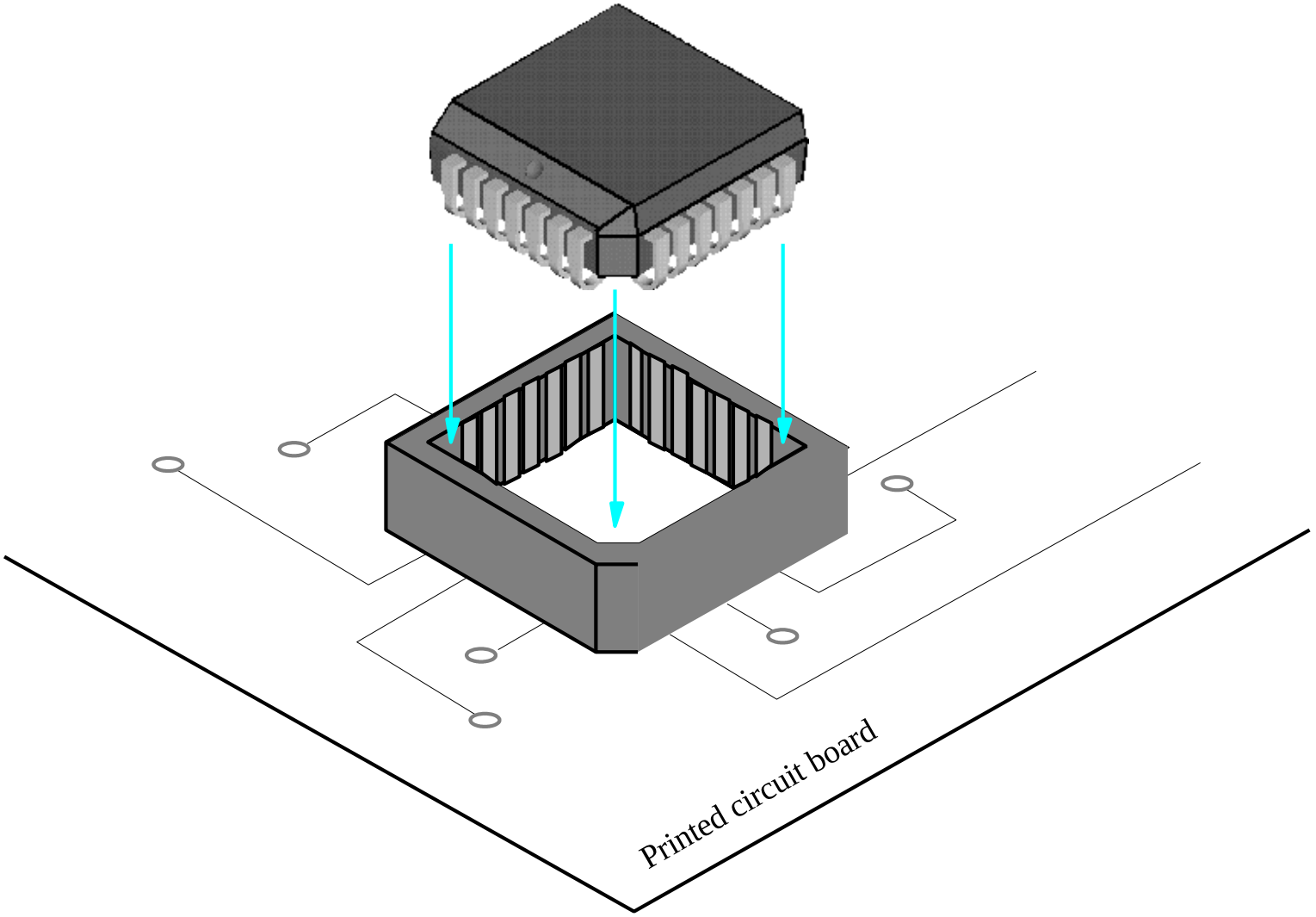
$$f_2 = \bar{x}_1 \bar{x}_2 + x_1 x_2 x_3$$

Programming of PLAs and PALs

- Commercial PAL and PLA chips contain a few thousand programmable switches:
  - not feasible for a user to specify manually

- CAD systems are employed for this purpose:
  - Generate a file, known as *Programming File/Fuse Map*
    - specifies the state of each programmable switch

Programming of PLAs and PALs



A Plastic Lead PLCC package with socket.

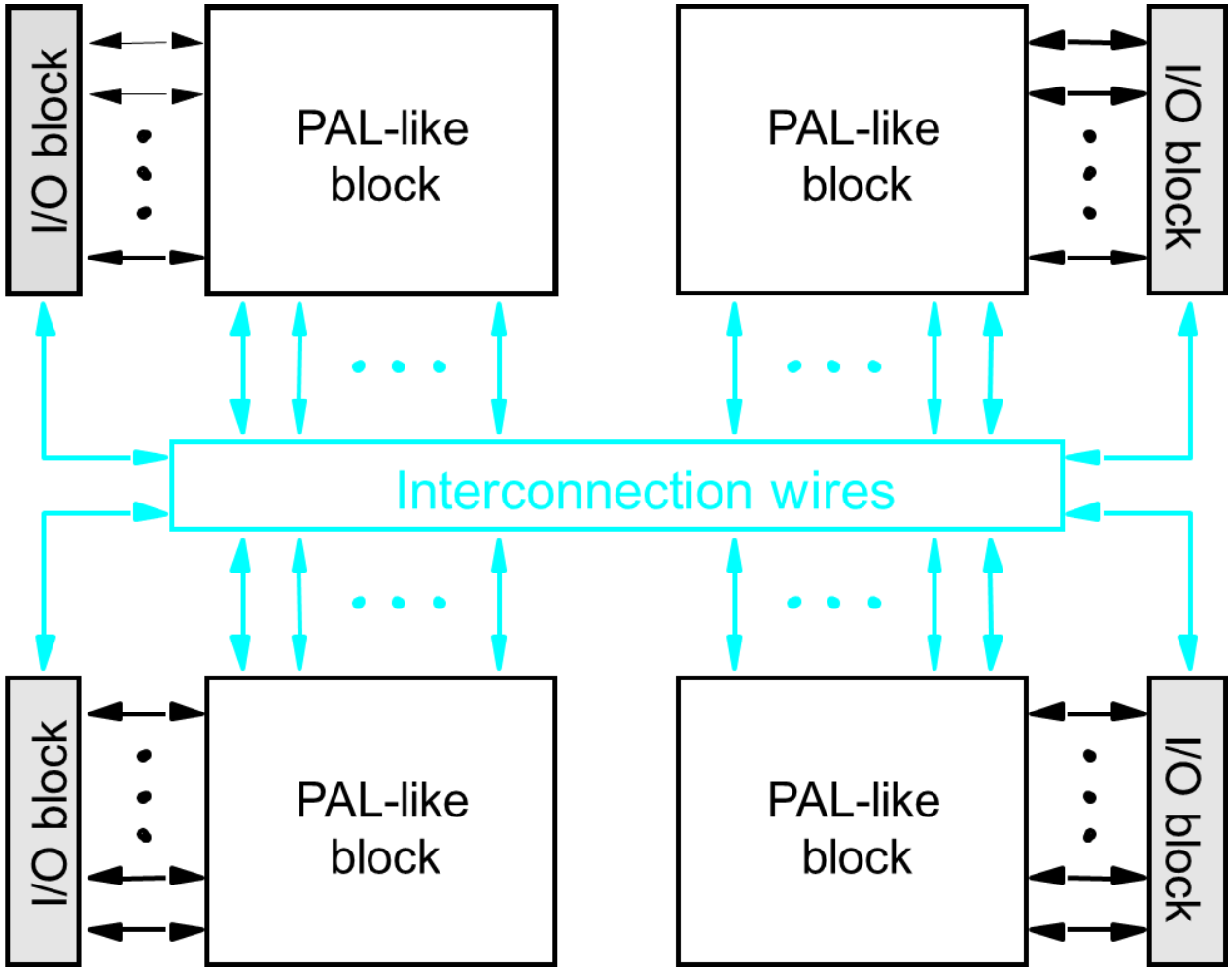
Programmable Logic Devices [CPLD]

Why CPLD?

- PLAs and PALs are useful for implementing a wide variety of small digital circuits:
  - Each device can be used to implement circuits that do not require more than:
    - the number of inputs,
    - product terms, and
    - outputs that are provided in the particular chip.

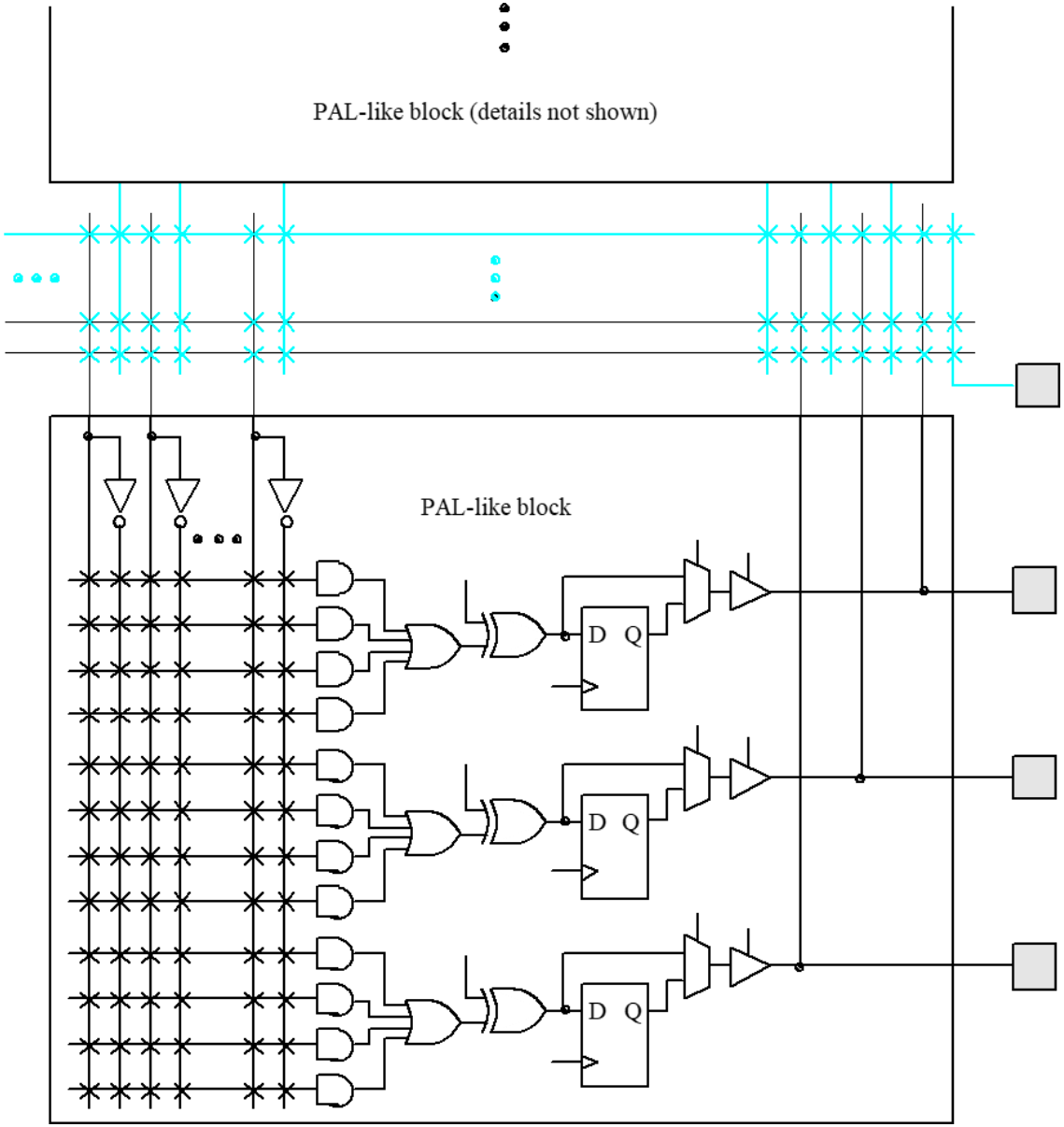
- These chips are limited to fairly modest sizes:
  - typically supporting a combined number of inputs plus outputs of not more than 32!

Complex Programmable Logic Devices (CPLDs) - Structure

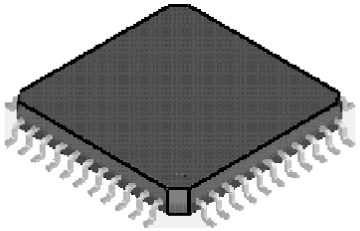


- Commercial CPLDs range in size from only 2 PAL-like blocks to more than 100 PAL-like blocks

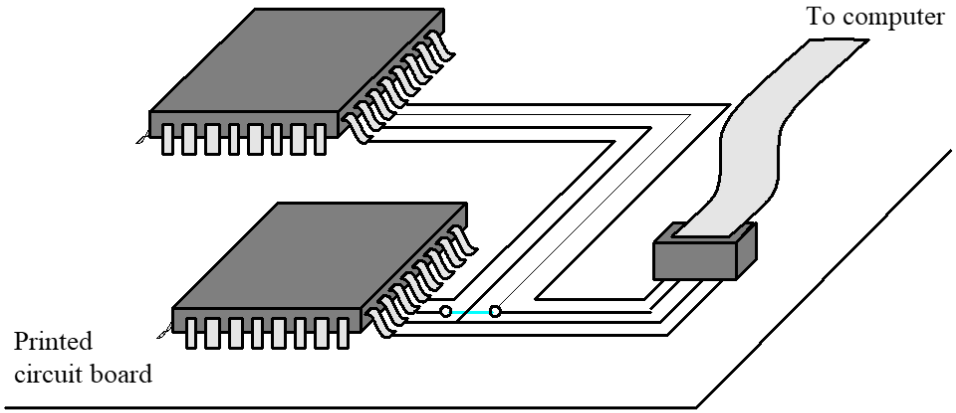
CPLD – Inside PAL-like Block



CPLD Programming



(a) CPLD in a Quad Flat Pack (QFP) package

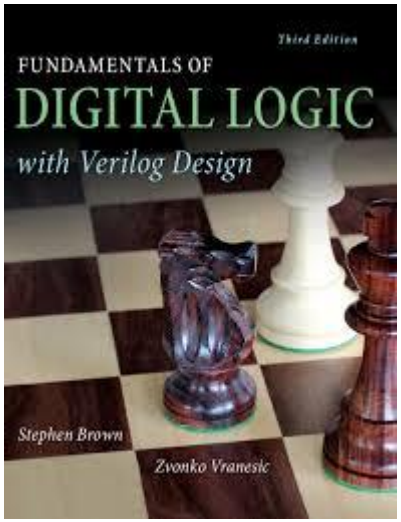


(b) JTAG programming

- Quad Flat Package (QFP) pins are much thinner than those on a PLCC:
  - programmed through In-System Programming (ISP) technique
    - Circuitry for ISP is Standardized by IEEE and is called JTAG port
      - (JTAG = Joint Test Access Group)

Recommended Reading

- Digital System Design with Verilog HDL, 3/e, b **S**tephen Brown and **Z**vonko Vranesic. [**S&Z**]
  - S&Z,
    - Appendix-B
      - B.5 to B.8



THANK YOU