# Laboratory Exercise 2

Switches, Lights, and Multiplexers

The purpose of this exercise is to learn how to connect simple input and output devices to an FPGA chip and implement a circuit that uses these devices. We will use the switches on the DE-series boards as inputs to the circuit. We will use light emitting diodes (LEDs) and 7-segment displays as output devices.

## Part I

The objective of this part is to display a character on a 7-segment display. The specific character displayed depends on a two-bit input. Figure 1 shows a *7-segment decoder* module that has the two-bit input $c_1c_0$. This decoder produces seven outputs that are used to display a character on a 7-segment display. Table 1 lists the characters that should be displayed for each valuation of $c_1c_0$ for your DE-series board. Note that in some cases the 'blank' character is selected for code 11.

The seven segments in the display are identified by the indices 0 to 6 shown in the figure. Each segment is illuminated by driving it to the logic value 0. You are to write a Verilog module that implements logic functions to activate each of the seven segments. Use only simple Verilog **assign** statements in your code to specify each logic function using a Boolean expression.

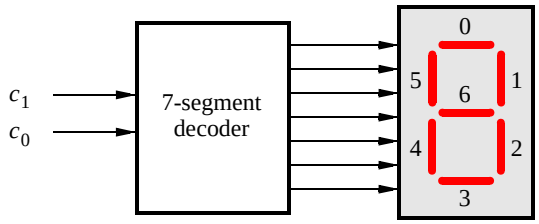


Figure 1: A 7-segment decoder.

| $c_1c_0$ | DE10-Lite | DE0-CV | DE1-SoC | DE2-115 |
|---|---|---|---|---|
| 00 | d | d | d | d |
| 01 | E | E | E | E |
| 10 | 1 | 0 | 1 | 2 |
| 11 | 0 | | | |

Table 1: Character codes for the DE-series boards.

Perform the following steps:

1. Create a new Quartus project for your circuit.
2. Create a Verilog module for the 7-segment decoder. Connect the $c_1c_0$ inputs to switches $SW_{1-0}$, and connect the outputs of the decoder to the *HEX0* display on your DE-series board. The segments in this display are called $HEX0_0$, $HEX0_1$, . . ., $HEX0_6$, corresponding to Figure 1. You should declare the 7-bit port

**output** [0:6] HEX0;

in your Verilog code so that the names of these outputs match the corresponding names in your board's user manual and pin assignment file.

3. After making the required pin assignments, compile the project.

4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling the $SW_{1-0}$ switches and observing the 7-segment display.

# Part II

Consider the circuit shown in Figure 2. It uses a two-bit wide 4-to-1 multiplexer to enable the selection of four characters that are displayed on a 7-segment display. Using the 7-segment decoder from Part IV this circuit can display the characters d, E, 0, 1, 2, or 'blank' depending on your DE-series board. The character codes are set according to Table 1 by using the switches $SW_{7-0}$, and a specific character is selected for display by setting the switches $SW_{9-8}$.

An outline of the Verilog code that represents this circuit is provided in Figure 3. Note that we have used the circuits from Parts III and IV as subcircuits in this code. You are to extend the code in Figure 3 so that it uses four 7-segment displays rather than just one. You will need to use four instances of each of the subcircuits. The purpose of your circuit is to display any word on the four 7-segment displays that is composed of the characters in Table 1, and be able to rotate this word in a circular fashion across the displays when the switches $SW_{9-8}$ are toggled. As an example, if the displayed word is dE10, then your circuit should produce the output patterns illustrated in Table 2.

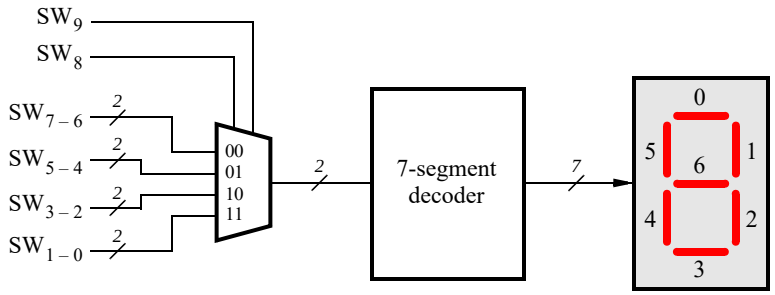


Figure 2: A circuit that can select and display one of four characters.

| $SW_{9-8}$ | Characters | | | |
|---|---|---|---|---|
| 00 | d | E | 1 | 0 |
| 01 | E | 1 | 0 | d |
| 10 | 1 | 0 | d | E |
| 11 | 0 | d | E | 1 |

Table 2: Rotating the word dE10 on four displays.

Perform the following steps.

1. Create a new Quartus project for your circuit.

2. Include your Verilog module in the Quartus project. Connect the switches $SW_{9-8}$ to the select inputs of each of the four instances of the two-bit wide 4-to-1 multiplexers. Also connect $SW_{7-0}$ to each instance of the multiplexers as required to produce the patterns of characters shown in Table 1. Connect the SW switches

```
module  part5 (SW, LEDR, HEX0);
    input [9:0] SW;                          // slide switches
    output [9:0] LEDR;                       // red lights
    output [0:6] HEX0;                       // 7-seg display

    wire [1:0] M0;

    mux_2bit_4to1 U0 (SW[9:8], SW[7:6], SW[5:4], SW[3:2], SW[1:0], M0);
    char_7seg H0 (M0, HEX0);
    . . .
endmodule

// implements a 2-bit wide 4-to-1 multiplexer
module mux_2bit_3to1 (S, U, V, W, X, M);
    input [1:0] S, U, V, W, X;
    output [1:0] M;
    . . . code not shown

endmodule

// implements a 7-segment decoder for d, E, 1 and 0
module char_7seg (C, Display);
    input [1:0] C;           // input code
    output [0:6] Display;    // output 7-seg code
    . . . code not shown

endmodule
```

Figure 3: Verilog code for the circuit in Figure 2.

.

to the red lights LEDR, and connect the outputs of the four multiplexers to the 7-segment displays *HEX3*, *HEX2*, *HEX1*, and *HEX0*.

3. Include the required pin assignments for your DE-series board for all switches, LEDs, and 7-segment displays. Compile the project.

4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by setting the proper character codes on the switches $SW_{7-0}$ and then toggling $SW_{9-8}$ to observe the rotation of the characters.

# Part III

Extend your design from Part V so that is uses all 7-segment displays on your DE-series board. Your circuit needs to display a three- or four-letter word, corresponding to Table 2, using 'blank' characters for unused displays. Implement rotation of this word from right-to-left as indicated in Table 3 and Table 4. To do this, you will need to connect 6-to-1 multiplexers to each of six 7-segment display decoders for the DE10-Lite, DE0-CV and DE1-SoC. Note that for the DE10-Lite you will need to use 3-bit codes for your characters, because five characters are needed when including the 'blank' character (your 7-segment decoder will have to use 3-bit codes, and you will need to use 3-bit wide 6-to-1 multiplexers). For the DE2-115, you will need to connect 8-to-1 multiplexers to each of the eight 7-segment display decoders. You will need to use three select lines for each of the multiplexers: connect the select lines to switches $SW_{9-7}$. In your Verilog code connect constants to the 6-to-1 (or 8-to-1) multiplexers that select each character, because there are not enough *SW* switches.
Perform the following steps:

| $SW_{9-7}$ | Character pattern | | | | | |
|---|---|---|---|---|---|---|
| 000 | | | d | E | 1 | 0 |
| 001 | | d | E | 1 | 0 | |
| 010 | d | E | 1 | 0 | | |
| 011 | E | 1 | 0 | | | d |
| 100 | 1 | 0 | | | d | E |
| 101 | 0 | | | d | E | 1 |

Table 3: Rotating the word dE10 on six displays.

| $SW_{9-7}$ | Character pattern | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 000 | | | | | | d | E | 2 |
| 001 | | | | | d | E | 2 | |
| 010 | | | | d | E | 2 | | |
| 011 | | | d | E | 2 | | | |
| 100 | | d | E | 2 | | | | |
| 101 | d | E | 2 | | | | | |
| 110 | E | 2 | | | | | | d |
| 111 | 2 | | | | | | d | E |

Table 4: Rotating the word dE2 on eight displays.

1. Create a new Quartus project for your circuit.

2. Include your Verilog module in the Quartus project. Connect the switches $SW_{9-7}$ to the select inputs of each instance of the multiplexers in your circuit. Connect constants in your Verilog code to the multiplexers as required to produce the patterns of characters shown in Table 3 or Table 4 depending on your DE-series board. Connect the outputs of your multiplexers to the 7-segment displays *HEX5*, . . ., *HEX0* of the DE10-Lite, DE0-CV and DE1-SoC or *HEX7*, . . ., *HEX0* for the DE2-115.

3. Include the required pin assignments for your DE-series board for all switches, LEDs, and 7-segment displays. Compile the project.

4. Download the compiled circuit into the FPGA chip. Test the functionality of the circuit by toggling $SW_{9-7}$ to observe the rotation of the characters.