Chapter6: Registers and Counters

Lecture2- An Introduction to Counters

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Objectives

- Study Asynchronous (Ripple) and Synchronous Counters

Counter

- A special type of register that goes through a prescribed sequence of states upon the application of input pulses
  - Input pulses: May be clock pulses or originate from some external source
  - The sequence of states may follow
    - the binary number sequence ($\Rightarrow$ Binary counter) or
    - any other sequence of states
- There are two main categories if counters
  - Ripple counters (Asynchronous Counters)

    There is no common clock pulse (not synchronous) and t he flip-flop output transition of one serves as a source for triggering other flip-flops
  - Synchronous counters

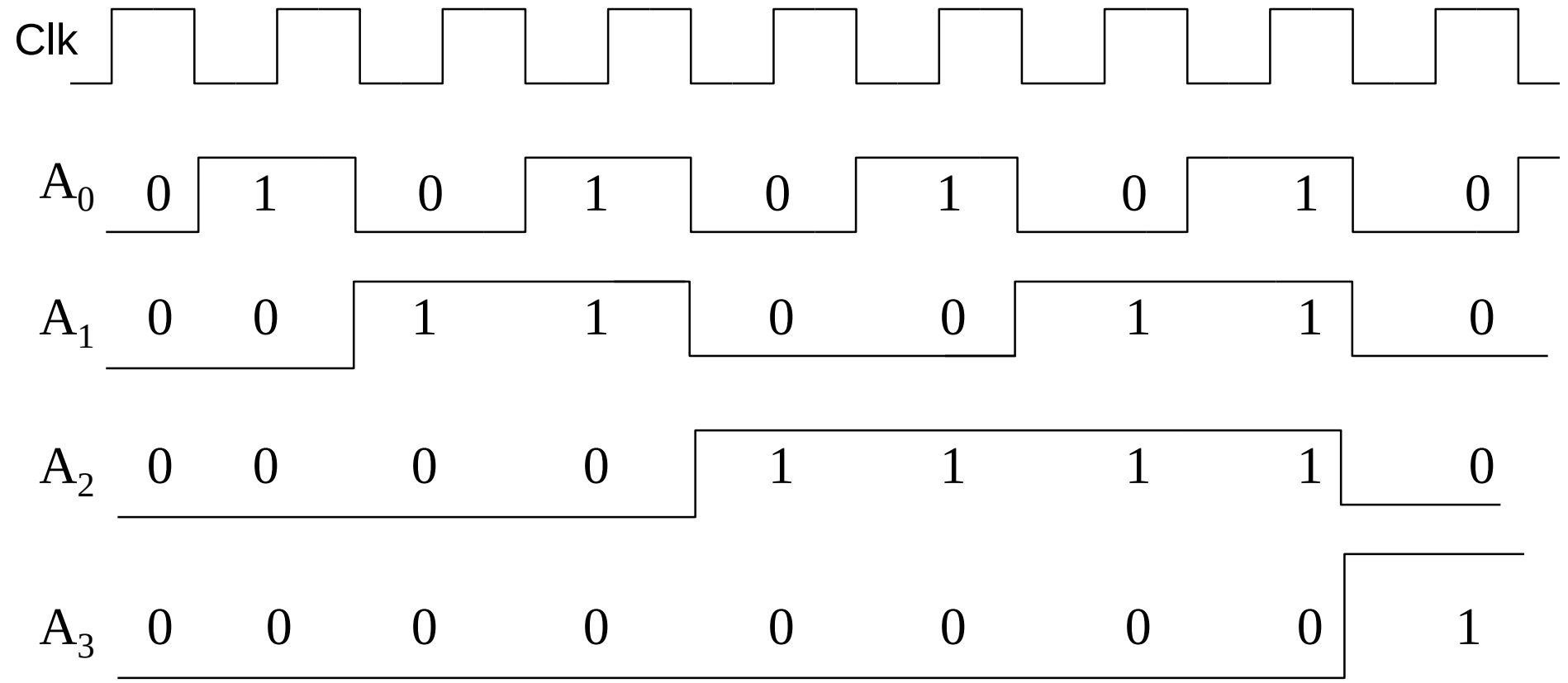
    The CLK inputs of all flip-flops receive a common clock

Example: 4-bit Binary Ripple Counter

- A 4-bit Binary Ripple Up Counter follows the sequence 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111, back to 0000, and repeat.
- Count pulse is applied only to A_0 generating the least significant bit of counting sequence. The output state transition of A_0 will be connected with C input of A_1 and trigger it , and so on.
- The flip-flops used in the design of 4-bit Binary Ripple Counters are self-complementing and toggle output state on negative edge of each count pulse.
- The timing diagram of the counter for counting sequence 0000 through 1000 is shown in the next slide.

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Partial Timing of a 4-bit binary ripple counter



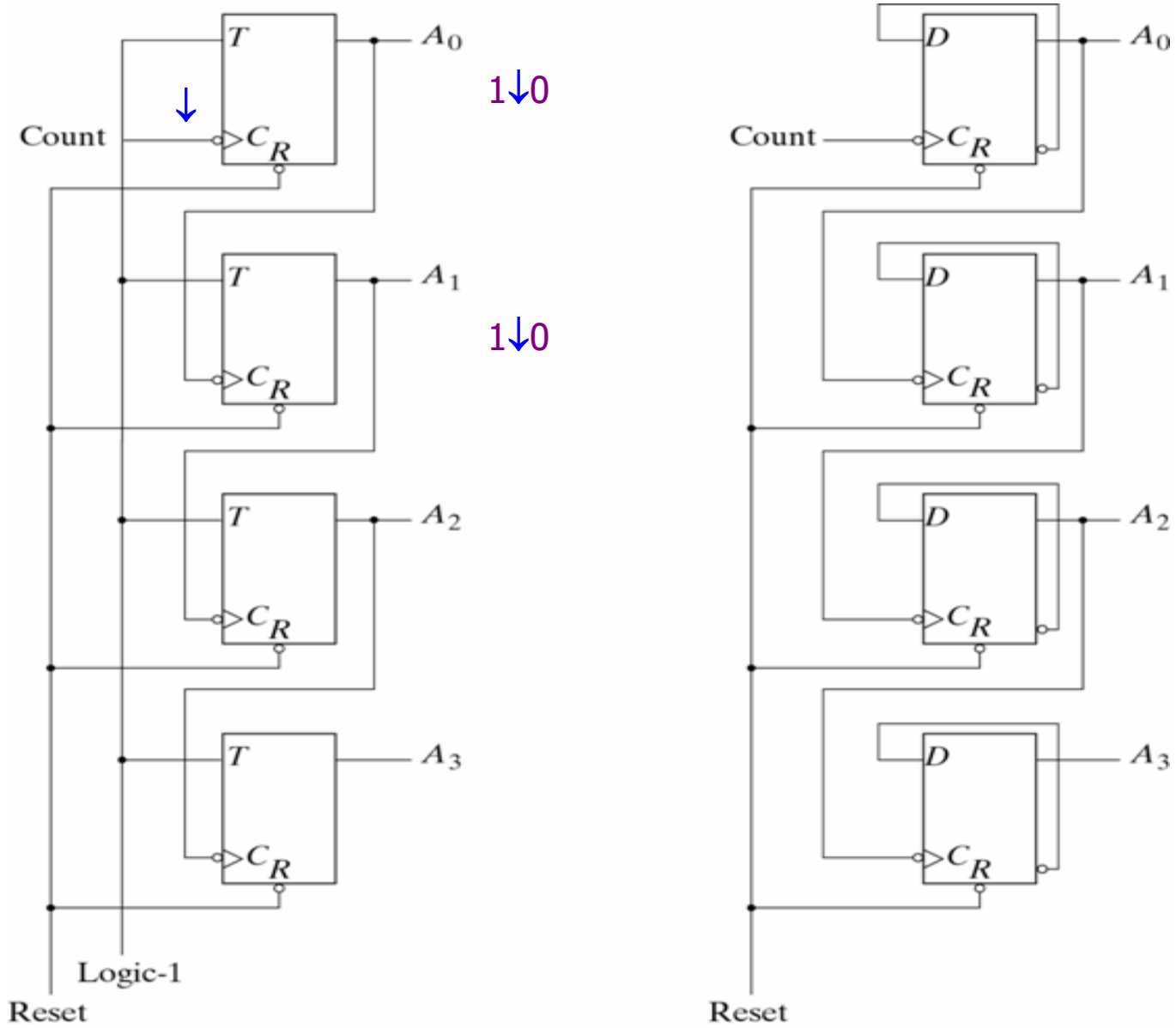
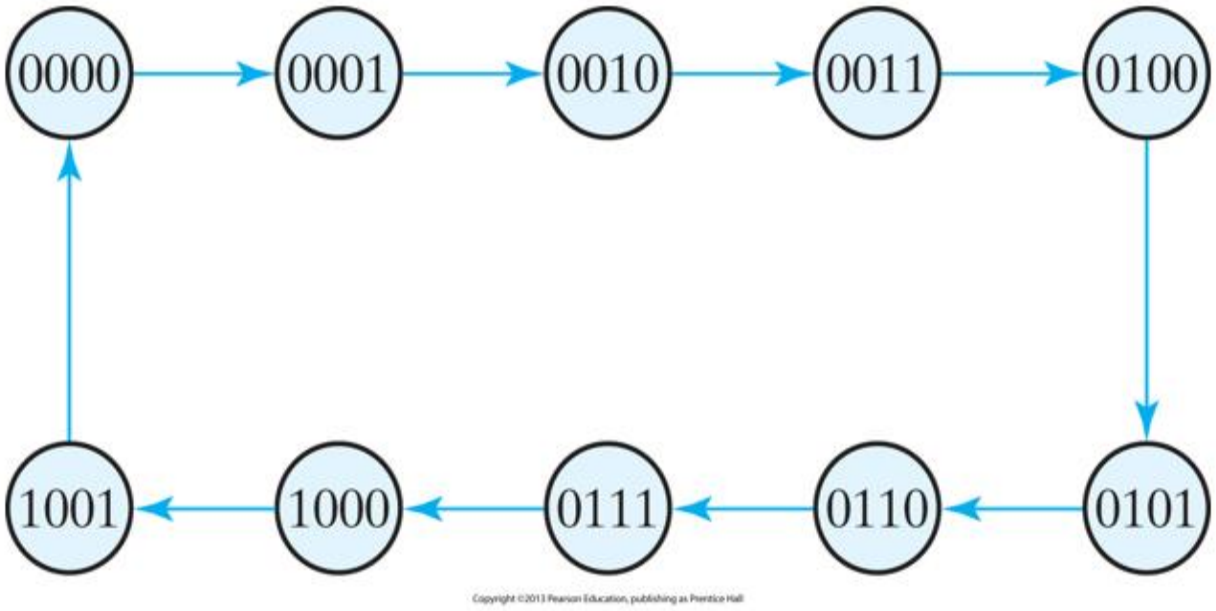


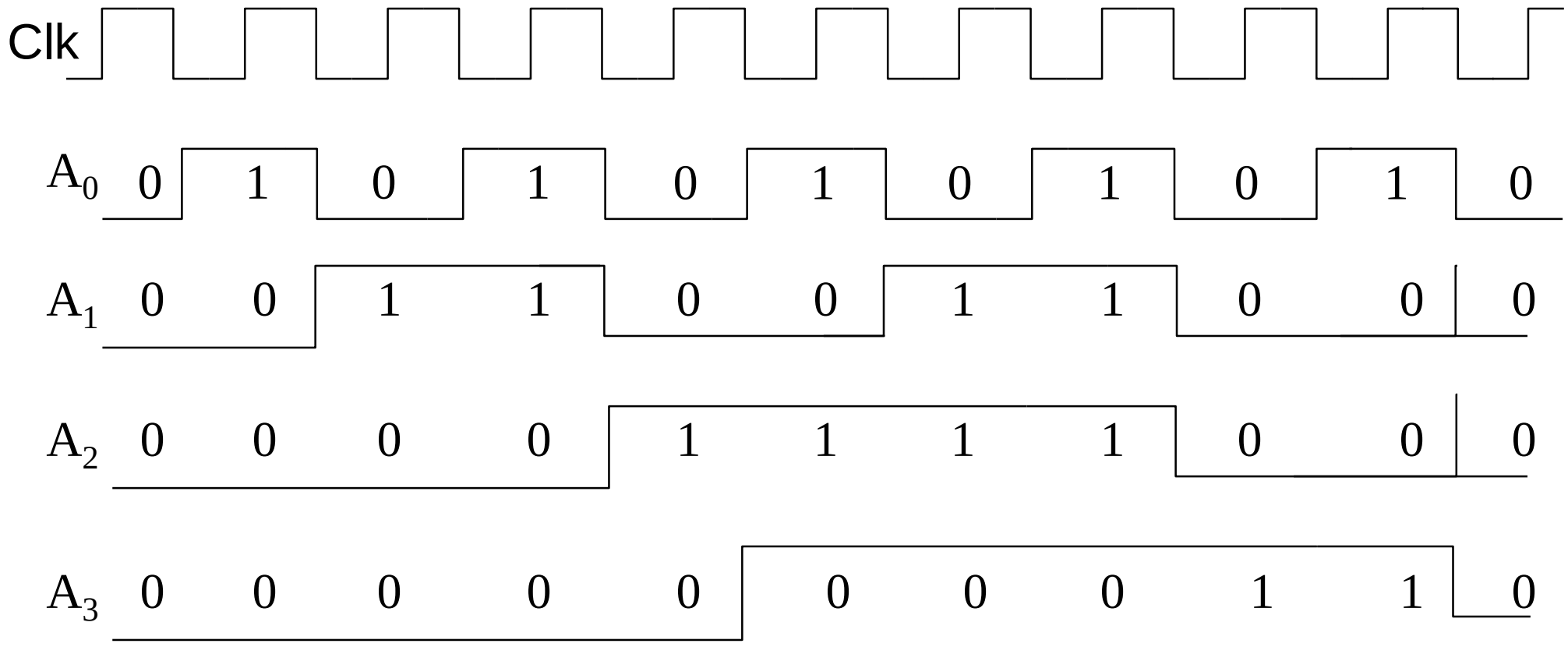
Fig. 6-8 4-Bit Binary Ripple Counter

Example: BCD Ripple Counter



- A BCD Ripple Counter follows the sequence 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, back to 0000 and repeats.
- It can also be constructed using different types of flip-flops such that count pulse is applied to the flip-flop generating the least significant bit of counting sequence and output state transition of one triggers others.

Timing Diagram of BCD Ripple Counter



The BCD Ripple Counter Circuit (with JK FF)

Counting Sequence

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010 **(0000)**

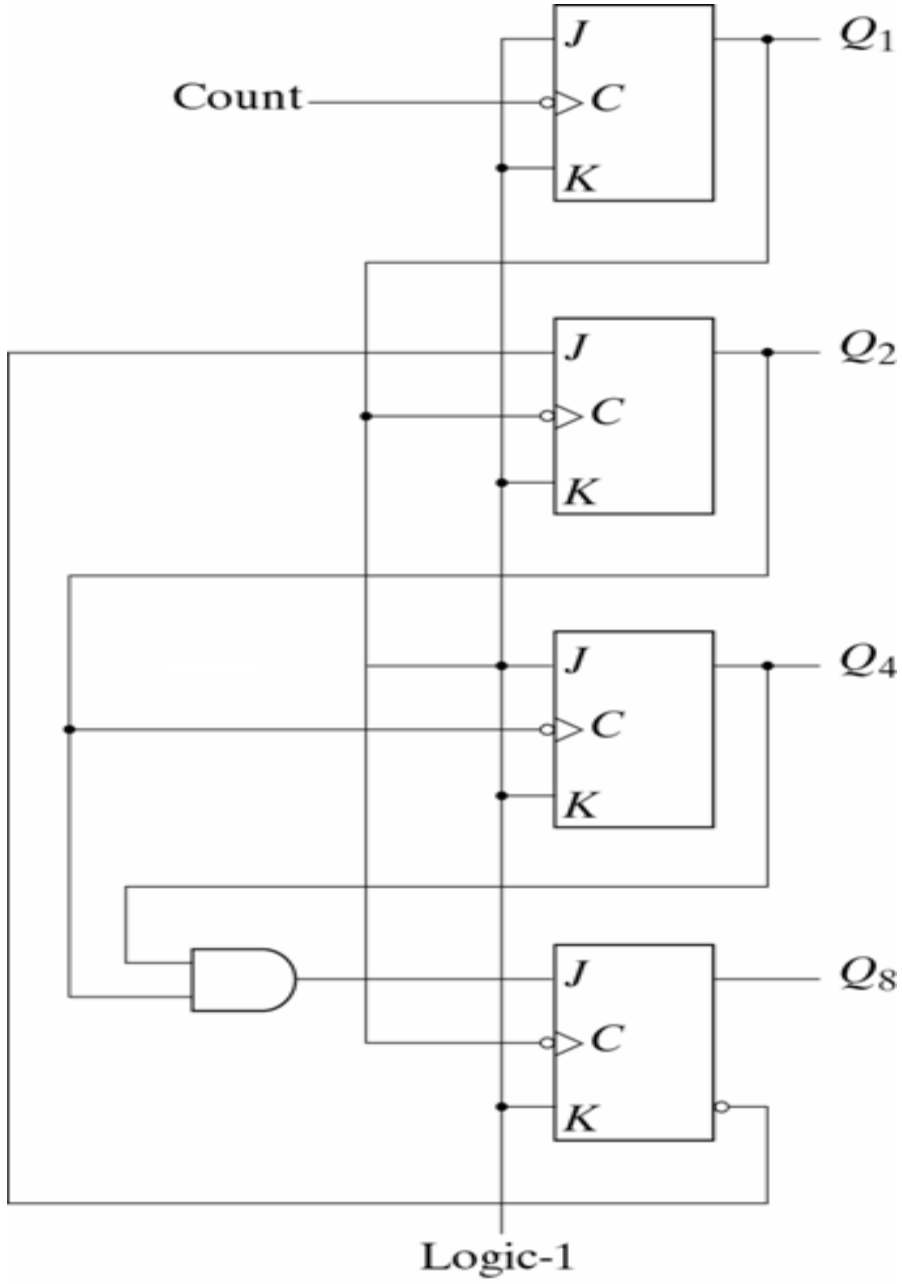


Fig. 6-10 BCD Ripple Counter

Cascading Counter Stages

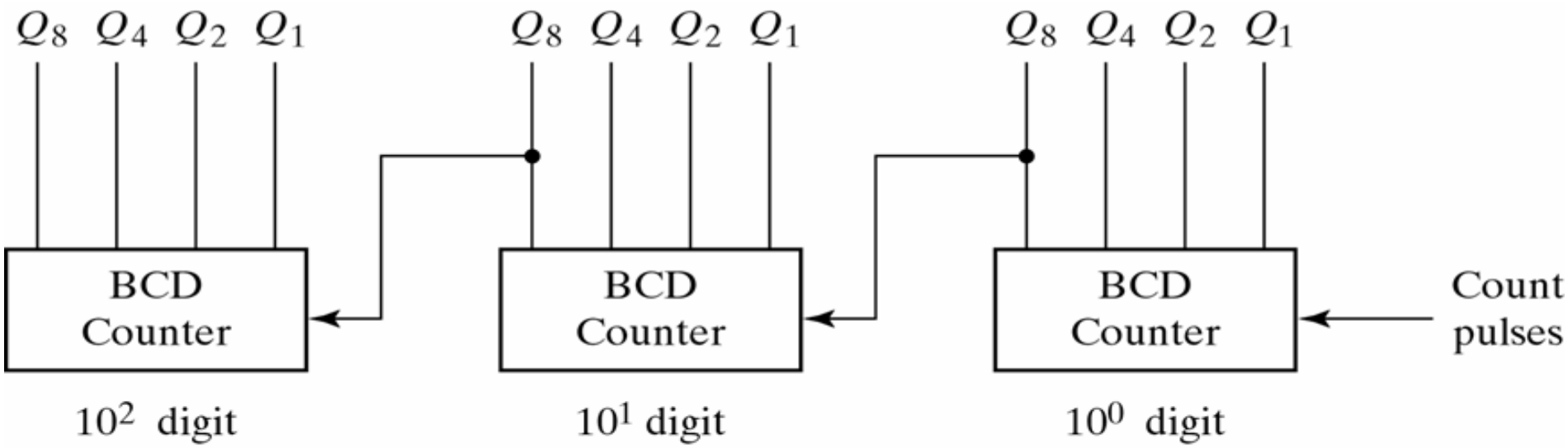


Fig. 6-11 Block Diagram of a Three-Decade Decimal BCD Counter

Synchronous Counters

- Synchronous counters are those in which common clock triggers all flip-flops simultaneously.
- In the design of synchronous counters, apply the same procedure of synchronous sequential circuits.
- Design of 4-bit Binary Up Synchronous Counter is much simpler and can be implemented after due scrutiny of counting sequence bits pattern.
- Flip-flops may be positive or negative-edge triggered.

A_0 =1 will complement A_1 , $A_0 A_1$ =1, $A_0 A_1 A_2$ =1, and $A_0 A_1 A_2 A$ =1 will reset all flip-flops to 0 synchronously.

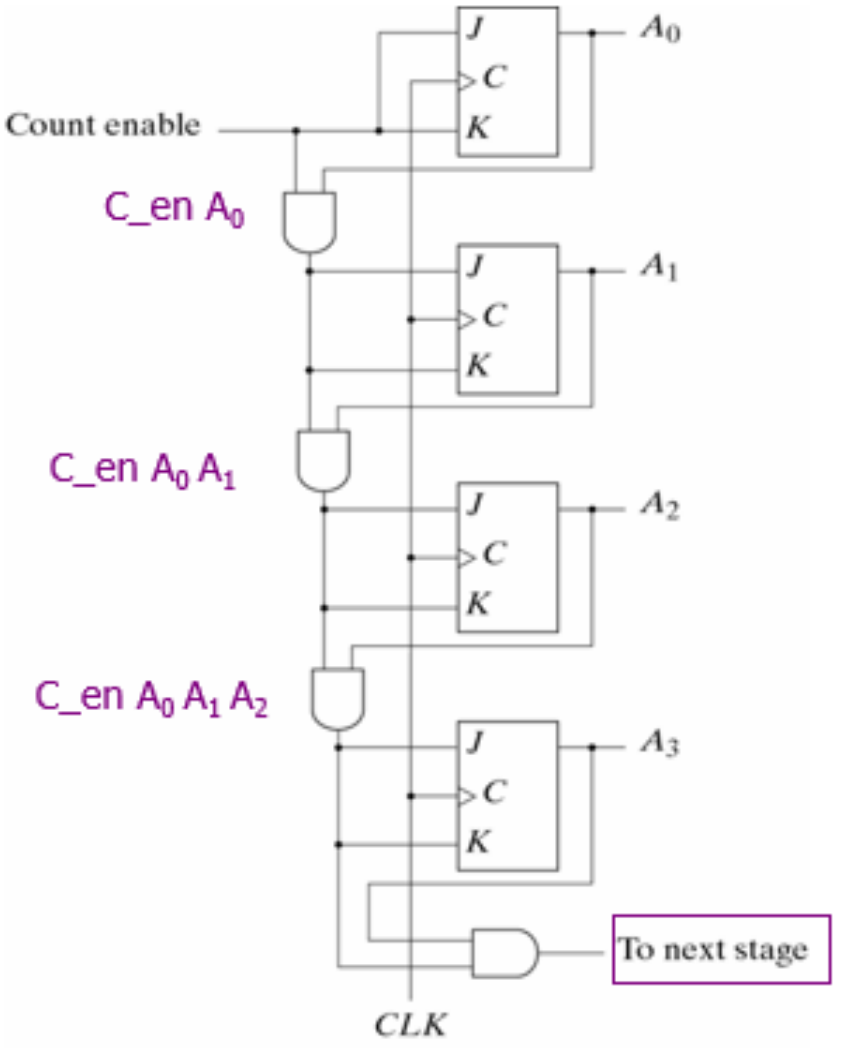


Fig. 6-12 4-Bit Synchronous Binary Counter

4-bit up/down binary counter

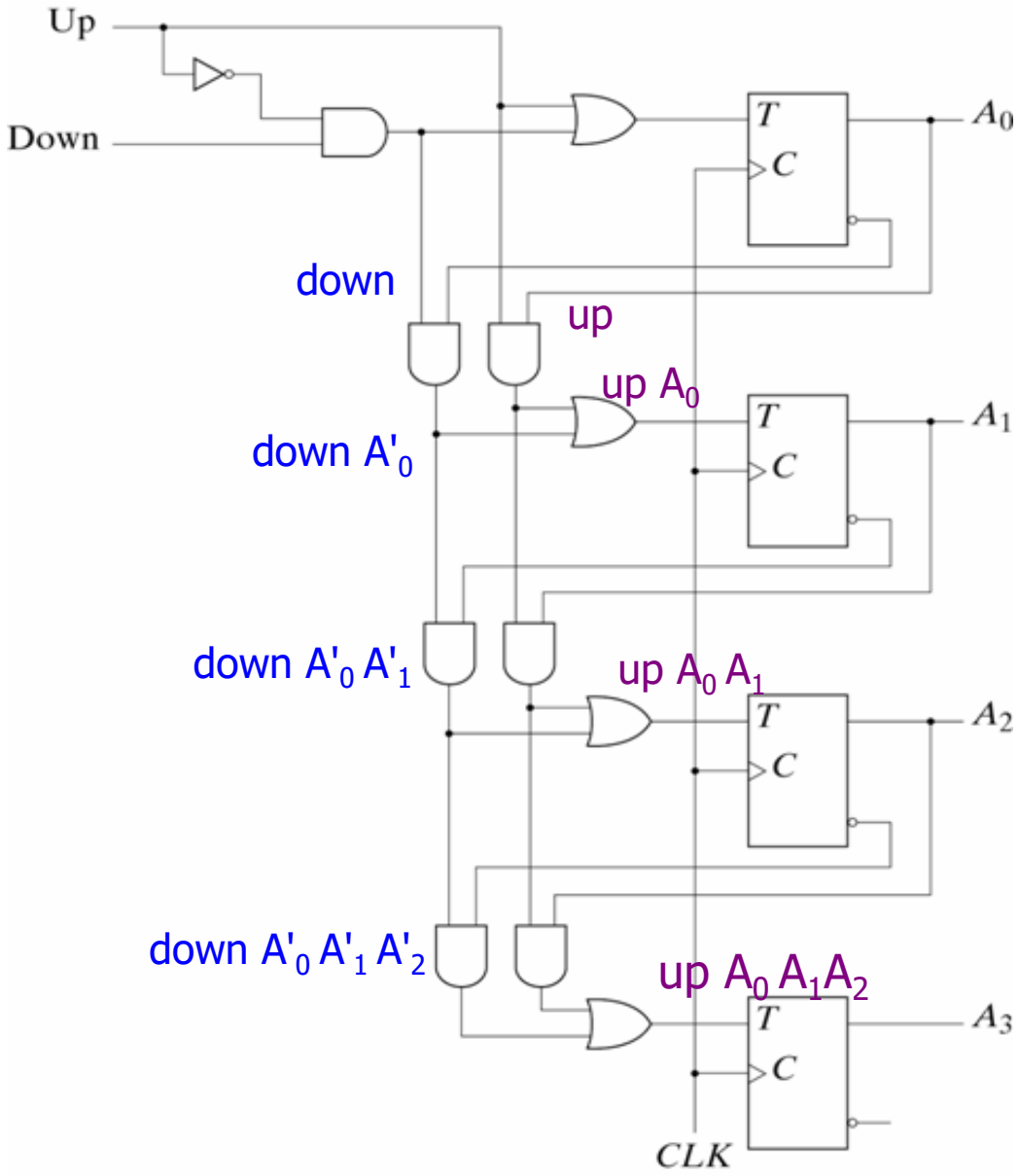


Fig. 6-13 4-Bit Up-Down Binary Counter

BCD Counters

Table 6-5
State Table for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

Using map method, we get

$TQ_1=1$; $TQ_2 = Q_8'Q_1$; $TQ_4 = Q_2Q_1$; $TQ_8 = Q_8Q_1+Q_4Q_2Q_1$

$Y = Q_8Q_1$

4-bit Binary Counter with Parallel Load

Table 6-6
Function Table for the Counter of Fig. 6-14

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	*X*	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

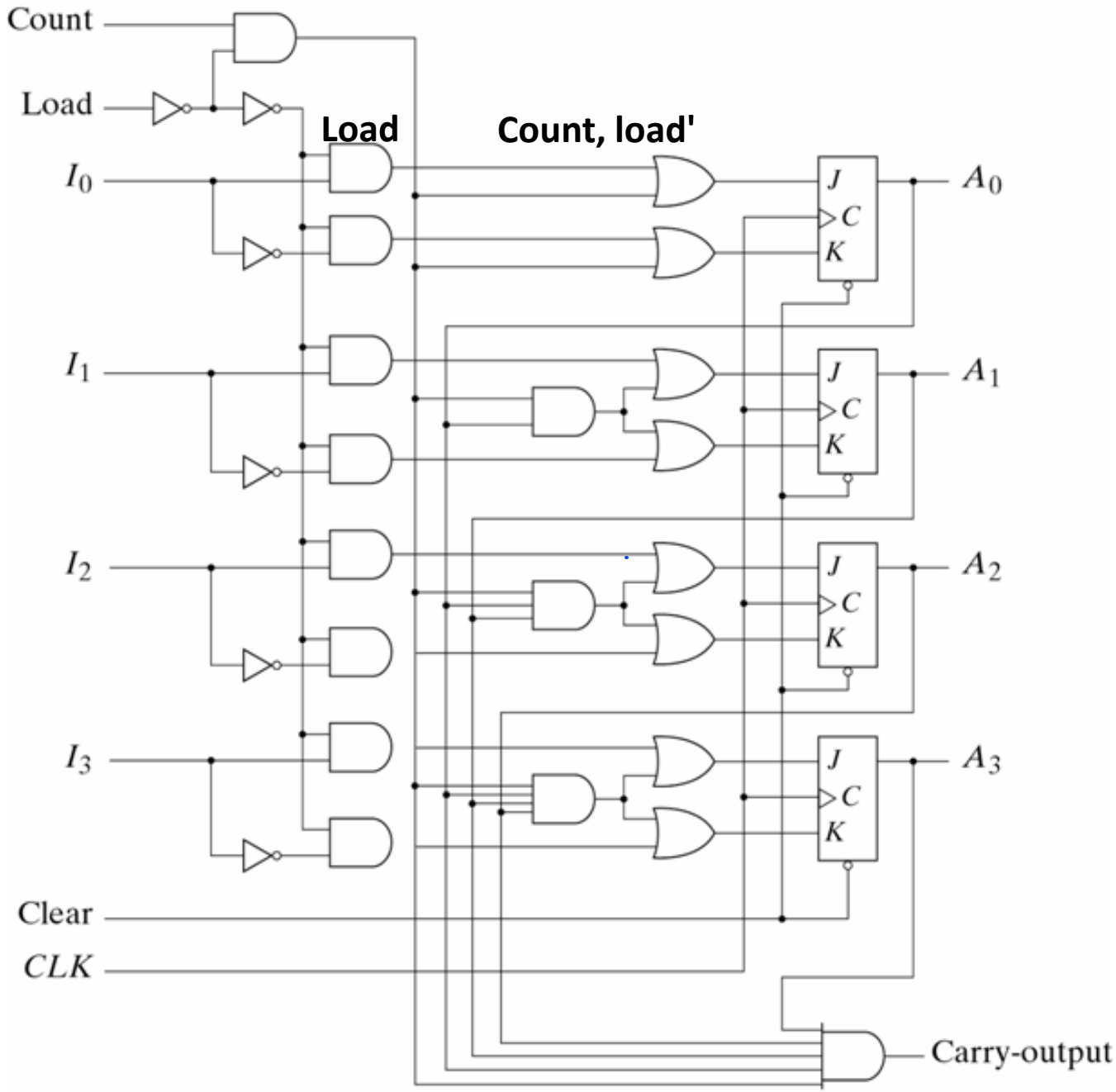


Fig. 6-14 4-Bit Binary Counter with Parallel Load

BCD Counter Design Examples

- Generate any count sequence using this counter with parallel load i.e BCD counting sequence after states decoding

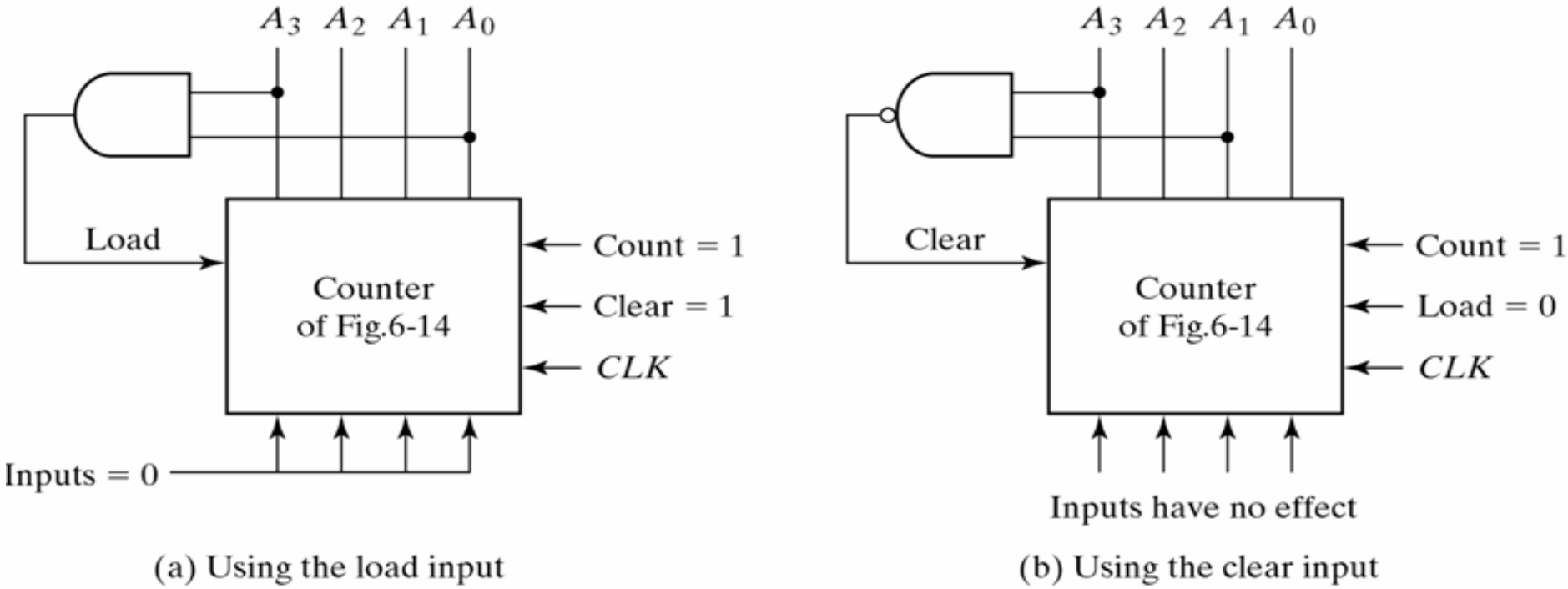


Fig. 6-15 Two ways to Achieve a BCD Counter Using a Counter with Parallel Load

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