Chapter5-Synchronous Sequential Logic

Lecture2- Study problems in Latches, Design Positive-edge Triggered D Flip-Flop

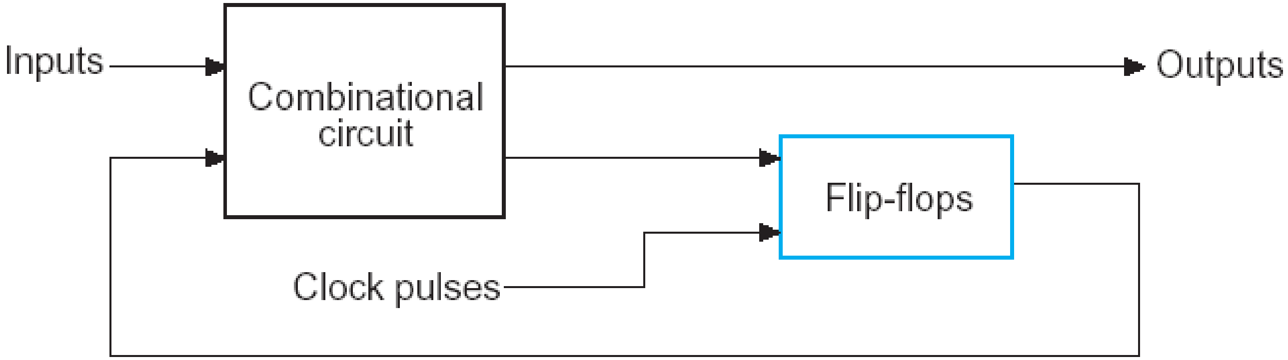
Objectives

- Study Problems in Latches
- Design different Types of D Flip-Flops

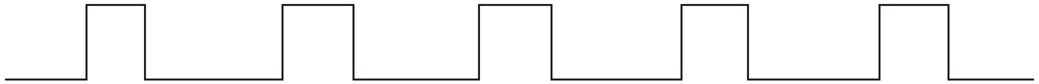
Flip Flops

- The state of a latch or a flip flop is switched by a change in the control input.
- This momentary change in the control input is called a trigger and the transition it causes is said to trigger the flip-flop.
  - As long as the control input is enabled, the data in and data out can be changed.
- Typically the output of a flip flop is used as an input of the combinational circuit which in turn provides input back to the flip flop (see Figure 5-2 in the next slide).
  - If a latch is used, we run the risk of unpredictable results because the latch changes output for as long as the control input is enabled. If the input changes while the clock pulse (control input) is still in logic 1 level, the output will change as per the new input i.e racing conditions.
  - Therefore, the output of a latch cannot be applied directly or through combinational logic to the input of the same or another latch.
- Flip flop circuits are constructed in such a way as to make them operate properly when they are part of a sequential circuit that employs a common clock.

Synchronous Clocked Sequential Circuit



(a) Block diagram



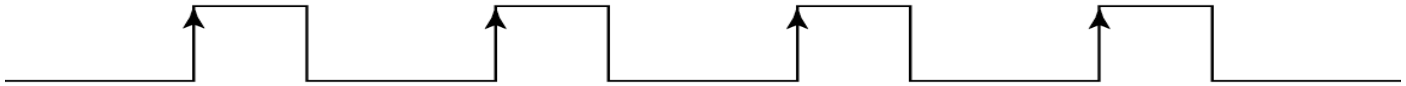
(b) Timing diagram of clock pulses

Problems with Latches

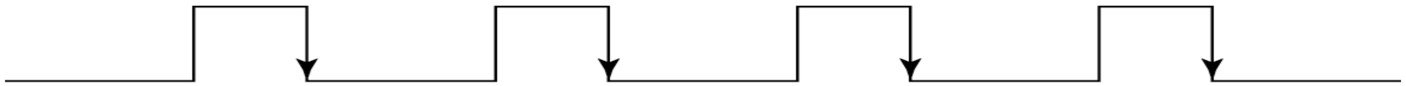
- The problem with the latch is that it responds to a change in the level of a clock pulse.
  - ➢ A positive level response in the control input allows changes in the output when the D input changes while the clock pulse stays at logic-1.
- The key to solving the latch problem in flip flops is to ensure that changes are only allowed to occur during a signal transitions (at the point in value change).
  - ➢ A positive transition is called a positive-edge response.
  - ➢ A negative transition is called a negative-edge response.

Clock Responses

(a) Response to positive level



(b) Positive-edge response



(c) Negative-edge response

Fig. 5-8 Clock Response in Latch and Flip-Flop

Modifying Latches to form Flip Flops

- Flip-flops can be constructed from latches by employing latches in different configurations.
- The problem with latches is that they are level- sensitive and change state as long as pulse stays at logic 1.
- The key to proper operation of a flip-flop is to trigger it during a signal transition i.e on edges.
- There are two ways that a latch can be modified to form a flip-flop.
  - ➢One way is to employ two latches in a special configuration that isolates the output of the flip-flop from being affected while its input is changing.
  - ➢Another way is to produce a flip-flop that triggers only once during a signal transition (from 0 to 1 or from 1 to 0), and is disabled during the rest of the clock pulse duration.

Edge-Triggered D Flip-Flop

- An Edge-triggered D flip flop is constructed with two D latches and an inverter.
  - The first latch is called the master and second the slave.
  - The circuit samples the D input and changes its output Q only at the negative-edge of the controlling clock.
  - When the clock is 0, the output of the inverter is 1, the slave latch is enabled and its output Q is equal to the master output Y.
    - The master latch is disabled because the clock is 0.
  - When the input pulse changes to the logic 1 level, the data from the external D input is transferred to the master.
    - The slave is disabled as long as the clock remains in the 1 level because its C input is equal to 0.
    - Any change in the input changes the master output at Y, but cannot affect the slave output.
    - When the pulse returns to 0 the master is disabled and the slave is enabled causing the value of Y to be transferred to output Q.

Master-Slave D Flip Flop

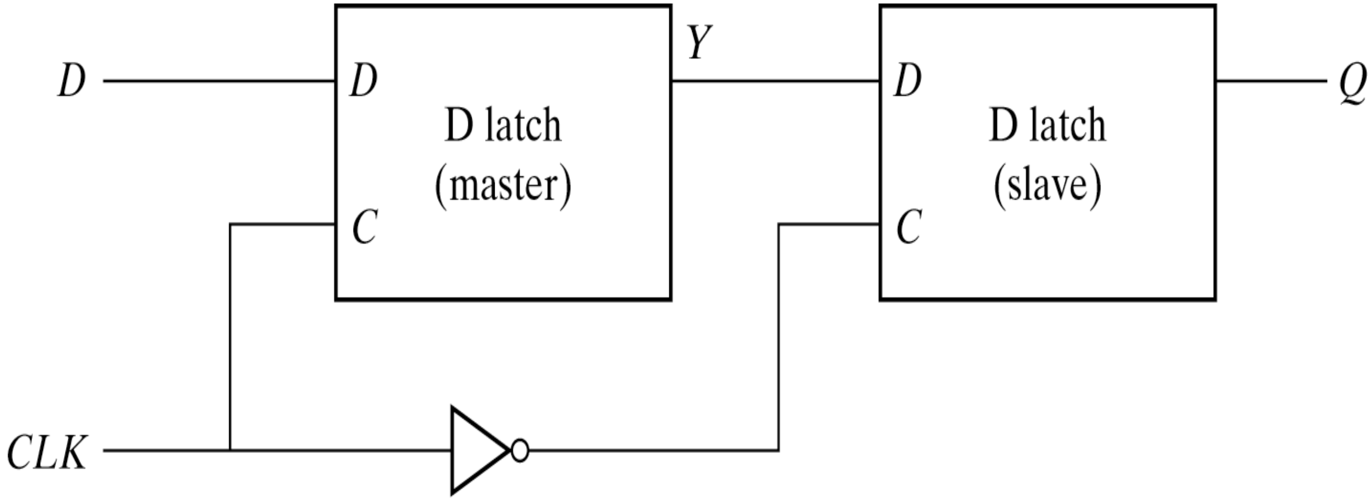


Fig. 5-9 Master-Slave *D* Flip-Flop

Characteristic Tables

- Characteristic tables define the logical properties of a flip flop by describing its operations in tabular form.
  - They define the next state as a function of the inputs and the present state.
  - Q(t) refers to the present state prior to the application of a clock edge.
  - Q(t + 1) refers to the next state one clock period later.
  - Clock edge input is not listed as inputs but is implied to occur by the transition from t to t + 1.
- An equation that expresses the next state of a latch or Flip-Flop in terms of its present state and inputs is referred to as a next-state equation, or characteristic equation.

Master-Slave D Flip Flop Characteristic Table

- The next state of D flip flop is dependent only on the D input and independent of the present state i.e. Q(t+1) = D

D Flip-Flop

D	Q(t+1)	
0 1	0 1	Reset Set

Positive Edge Transition is also possible?

- The previous implementation uses a negative edge transition.
  - The output only changes during the negative edge of the clock.
- A positive edge transition implementation can be constructed by placing an inverter on the CLK input prior to any other gate or inverter. i.e. between the CLK terminal and the junction between the other inverter and input C of the master latch.
- Such flip flop is triggered with a negative pulse, so that negative edge of the clock affects the master and the positive edge affects the slave and the output terminal

Alternative Positive-Edge-Triggered D Flip Flop

- A more efficient construction of an edge-triggered D flip flop uses three SR latches.
  - Two latches respond to the external D (data) and CLK (clock) inputs.
  - The third latch provides the outputs for the flip flop.
  - The S and R inputs of the output latch are maintained at logic 1 level when CLK = 0 causing the output to remain in its present state.
  - If D = 0 when CLK = 1, R changes to 0 causing a reset state and making Q = 0.
  - If there is a change in D while CLK = 1, terminal R remains at 0, thus locking out the flip flop (unresponsive to further changes in the input).
  - If D = 1 when CLK = 1, S changes to 0 causing the circuit to go to the set state making Q = 1.

Positive Edge -Triggered D Flip-Flop with 3 SR Latches

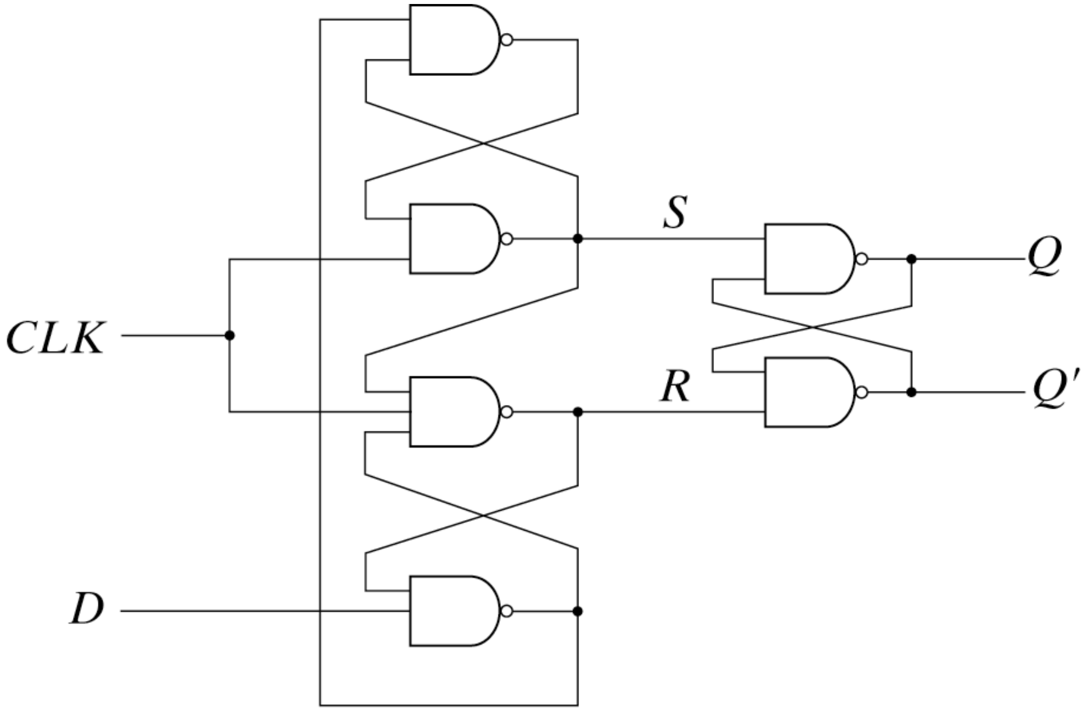


Fig. 5-10 *D*-Type Positive-Edge-Triggered Flip-Flop

Positive-Edge Triggered D Flip-Flop Summary

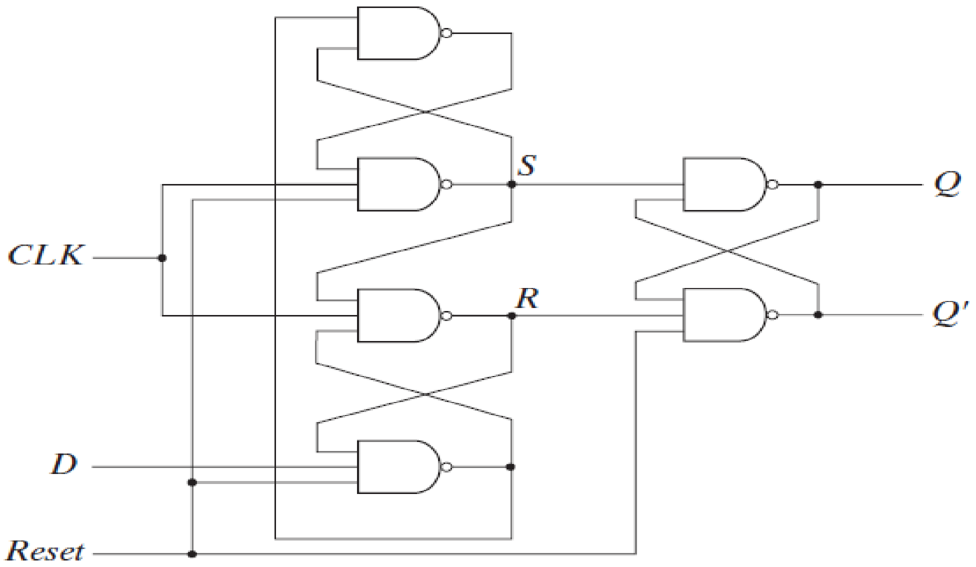
- When the input clock makes the positive transition, the value of D is transferred to Q
- A negative transition from 1 to 0 or steady CLK state: (logic 1 or logic 0) doesn't affect the output
- This flip flop responds to transition from 0 to 1 only

Function Table

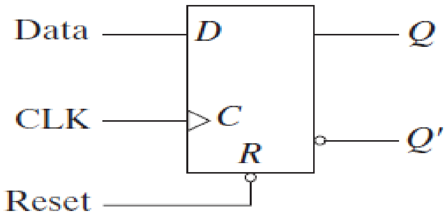
S	R	D	Clock	Q(t+1)
1	1	X	0	No change
1	0	0	1	0 (Reset)
1	0	1	1	No change, unresponsive
1	1	X	0	No change
0	1	1	1	1 (Set)

Direct Inputs

- Some flip flops have asynchronous inputs that are used to force the flip flop to a particular state independent of the clock.
  - ➢ The input that sets the flip flop to 1 is called preset or direct set.
  - ➢ The input that clears the flip flop to 0 is called clear or direct reset.
- Direct inputs are useful for setting all flip flops to a known starting state prior to clocked operation.
- A positive-edge-triggered D flip-flop constructed from three SR latches with asynchronous reset is shown in Figure 5-14.



(a) Circuit diagram



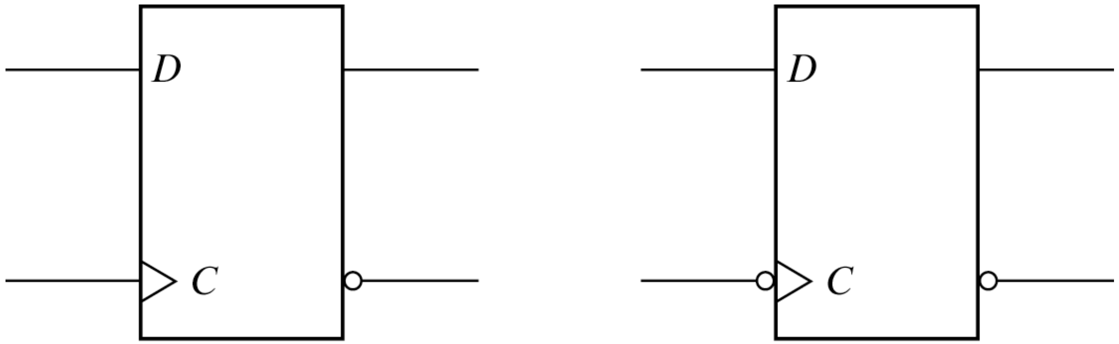
(b) Graphic symbol

R	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Fig. 5-14 *D* Flip-Flop with Asynchronous Reset

Edge-Triggered D Flip Flop Graphic Symbols



(a) Positive-edge (a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop

Notes on Flip Flops

- The timing of the response of a flip flop to input data and clock must be taken into consideration when using edge-triggered flip flops.
- There is a minimum time, called setup time, for which the D input must be maintained at a constant value prior to the occurrence of the clock transition.
- There is a minimum time, called hold time, for which the D input must not change after the application of the positive transition of the clock.
- The propagation delay time of the flip flop is defined as the time interval between the trigger edge and the stabilization of the output to a new state.

The End