National University of Sciences & Technology (NUST)
School of Electrical Engineering and Computer Science (SEECS)
Department of Electrical Engineering

EE221 Digital Logic Design			
Course Code:	EE221	**Semester:**	Fall 2021
Credit Hours:	3+1	**Pre-requisites:**	Nil
Instructor:	Engr. Arshad Nazir	**E-mail:**	arshad.nazir@seecs.edu.pk
Office:	Room A-215, Faculty Block	**Telephone:**	+92 (0)51 9085 2117
Students Batch:	BEE-12CD	**Discipline/Year:**	Electrical Engineering/Second
Lecture/Lab Days:	**Mon:**1200-1250 (C/CR-18) 1400-1450 (D/CR-16) **Tues:**1100-1150 (C/CR-18) 1200-1250 (D/CR-16) **Wed:**1000-1050(D/CR-16) 1100-1150(D/CR-18) **Thu:** 1100-1250 (D/Digital Lab) 1500-1650 (C/Digital Lab) **Fri:** 1100-1250 (D/Digital Lab) 1400-1550 (C/Digital Lab)	**Consulting Hours:**	**Wed:** 1200-1250 Hours (CD/Off) or Appointment via email
Lab Engr:	Engr. Mughees Ahmed	**E-mail:**	mughees.ahmed@seecs.edu.pk
Knowledge Group:	Digital Systems and Signal Processing	**Updates on LMS:**	After lecture/on required basis

Course Description:

Digital Logic Design is a one-semester course taken by Electrical Engineering students during second year of their engineering program. This course introduces the logic operators and gates to lay the framework for strengthening the basic understanding of computer building blocks. Both combinational and sequential circuits are studied in this course along with their constituent elements comprising Arithmetic circuits, Comparators, Decoders, Encoders, Multiplexers, Tristate gates as well as Latches, Flip-flops, Counters and Registers. It lays down foundations for advanced studies in Microprocessor Systems to be taught in the following semester. In this course students will learn principles of Digital Logic Design. They will combine classical design methodologies with a series of laboratory assignments in which they will demonstrate their ability to successfully design, implement, and debug digital systems using Computer Aided Design tools and physical prototyping.

Course Learning Outcomes (CLO)

	Description After the successful completion of the course the students will be able to:	**BT Level**	**PLO**
1	**Describe** digital systems, computer arithmetic, and simplify Boolean functions.	C3	1
2	**Analyze** combinational and sequential medium-scale integration circuits using standard analysis procedures to determine their functionality.	C4	2
3	**Design** combinational and sequential circuits of moderate complexity within the given hardware constraints.	C5	3
	Conduct experiments as well as **analyze** and **interpret** experimental data	P4	4
5	**Construct** digital systems of moderate complexity using laboratory equipment and simulation tools.	P4	5
6	**Exhibit** good professional and ethical behavior while **adhering** to lab safety rules.	A3	8
7	**Function** effectively both individually and as a member of a team	A3	9

Mapping of CLOs TO Program Learning Outcomes

PLOs/ CLOs	CLO1	CLO2	CLO3	CLO4	CLO5	CLO6	CLO7
PLO1 (Engineering Knowledge)	√						
PLO2 (Problem Analysis)		√					
PLO3 (Designing/Development of Solutions)			√				
PLO4 (Investigation)				√			
PLO5 (Modern tool usage)					√		
PLO6 (The Engineer and Society)							
PLO7 (Environment and Sustainability)							
PLO8 (Ethics)						√	
PLO9 (Individual and Teamwork)							√
PLO10 (Communication)							
PLO11 (Project Management)							
PLO:12 (Lifelong Learning)							

Assessment Modules, Weightages, and Mapping to CLOs

Assessments/CLOs	CLO1	CLO2	CLO3	CLO4	CLO5	CLO6	CLO7
Quizzes: 12% @9 Marks	√	√	√				
Assignments: 8% @ 6 Marks	√	√	√				
OHT 1: 16% @ 12 Marks	√	√					
OHT 2: 16% @ 12 Marks		√	√				
End Semester Exam: 48% @ 36 Marks	√	√	√				
Regular Labs:70% @ 17.5				√	√	√	√
Semester Design Project/Final Lab Exam: 30% @ 7.5				√	√	√	√

Books:

Textbook: Digital Design (Fourth Edition) by M. Morris Mano and Michael Ciletti

Reference Books:

1. Digital Fundamentals (Eleventh Edition) by Floyd
2. Logic and Computer Design Fundamentals (Fourth Edition) by M. Morris Mano and Charles R. Kime
3. Fundamentals of Logic Design (Sixth Edition) by Charles H. Roth Jr
4. Digital Systems: Principles and Applications (Tenth Edition) by TocciWidmer
5. Contemporary Logic Design (Second Edition) by Randy H. Katz
6. Verilog HDL: A guide to Digital Design and Synthesis (Second Edition) by Samir Palnitkar

Main Topics to be Covered:

1. Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Numbers. Binary Codes.
2. Basic Definitions. Axiomatic Definition of Boolean algebra. Basic Theorems and Properties of Boolean Algebra
3. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates. Integrated Circuits
4. The K-Map Method. Four-Variable Map. Product of Sums and Sum of Products simplifications. Introduction to Five-Variable Map. Quine-McCluskey minimization technique (Tabulation).
5. Don't-Care Conditions. NAND and NOR Implementations. Other Two-Level Implementations
6. Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder-Subtractor. Decimal Adder. ALU Design using Combinational Circuits.
7. Binary Multiplier. Magnitude Comparator. Decoders. Encoders. Multiplexers
8. Sequential Circuits. Latches and Flip-flops
9. Analysis of Clocked Sequential Circuits.
10. Mealy and Moore FSM. State Reduction and Assignment. Design of clocked sequential circuits.
11. Registers. Shift Registers. Ripple Counters
12. Synchronous Counters. Other Counters

Lectures Breakdown:

Week No	Lecture	Topics	Textbook Reference	Other References	Remarks
1.	**1.**	**Introduction**: Digital Systems and motivation for study	1-1		
	2.	Number Systems: Binary, Octal, Decimal and Hexadecimal Numbers and Base Conversions.	1-2,1-3, &1-4	1-2 Ref Book (3)	
	3.	Complements: Subtraction of Unsigned Numbers using Complements.	1-5	.	
	Lab 01	Familiarization of Basic Gates and Digital ICs			
2.	4.	Signed Binary Numbers Arithmetic: Addition and Subtraction of Signed Binary Numbers.	1-6	2-6 Ref Book (2)	
	5.	Binary Codes.	1-7		
	6.	Binary Storage and Registers. Binary Logic: Definition of Binary Logic and Logic gates.	1-8&1-9		
	Lab 02	Introduction to Verilog HDL.			

		Basic language constructs and design entry using Verilog HDL.			
3.	**7.**	**Introduction**: Boolean Algebra: Basic and Axiomatic Definition of Boolean Algebra; Two-Valued Boolean Algebra.	2-1,2-2, &2-3	2-2 Ref Book (3)	
	8.	Basic Theorems and Properties of Boolean Algebra.	2-4		
	9.	Boolean Functions; Canonical and Standard Forms.	2.5 &2-6		
	Lab 03	Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Verilog HDL Gate-Level modeling.			
4.	10.	Other Logic Operations.	2-7	8-1 Ref Book (5)	
	11.	Digital Logic Gates and Integrated Circuits.	2-8&2-9		
	12.	**Introduction**: The K-Map Method; Two, and Three -Variable K- Maps. Sum-of-Products (SOP) simplification using Three-Variable K-Map.	3-1 & 3-2	5-2 Ref Book (4)	
	Lab 04	Minimization of Boolean Functions and its Hardware implementation.			
5.	13.	Sum-of-Products (SOP) simplification using Four-Variable K-Map; Essential and Non-essential Prime Implicants.	3-3	5-3 Ref Book (4) 2.5 Ref Book (3)	
	14.	Five-Variable K-Map; Sum-of-Products (SOP) simplification using Map Method.	3-4	5-4 Ref Book (4)	
	15.	Product- of- Sums (POS) Simplifications and Don't Care conditions.	3-5 & 3-6		
	Lab 05	Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates.			
6.	**OHT1**				
7.	16.	Quine-McCluskey Minimization algorithm (Tabulation).		6-1, 6-2 &6.3 Ref Book (4)	
	17.	NAND and NOR implementations.	3-7		
	18.	Other Two-Level implementations.	3-8		
	Lab 06	BCD-to-Seven Segment Decoder Design.			
8.	19.	Exclusive-OR function: Parity Generation and Checking.	3-9		

	20.	**Introduction**: Combinational Circuits: Design Procedure with Code Conversion Example.	4-1, 4-2 & 4-4		
	21.	Combinational Circuits: Analysis Procedure.	4-3		
	Lab 07	Design of a 2-bit Magnitude Comparator using Classical design method. Verilog HDL gate-level modeling.			
9.	22.	Half and Full Adders: Design of 4-BIT Ripple Carry Adder-Subtractor using Full Adders.	4-5		
	23.	Design of 4-Bit Adder-Subtractor with Carry Look-ahead Generator and Overflow.	4-5		
	24.	Decimal Adder, Binary Multiplier	4-6 & 4-7		
	Lab 08	Design of a 2-bit Adder/Subtractor Circuit. Combinational Logic Design using Verilog HDL.			
10.	25.	Magnitude Comparator, Decoders/De-multiplexers.	4-8 & 4-9		
	26.	Decoders/De-multiplexers, Encoders	4-9 & 4-10		
	27.	Multiplexers and Tri-State Gates.	4-11	4-2-2, 3, &4 Book (6)	
	Lab 09	Design of 4-bit ALU.			
11.	**28.**	**Introduction**: Sequential Circuits and different types of Latches.	5-1 & 5-2		
	29.	Storage Elements: Latches	5-3		
	30.	Storage Elements: Flip-Flops, Other Flip-Flops, Conversion of Flip-Flops.	5-4	11-4,11-5,11-6 &11-7 Ref Book (4)	
	Lab 10	Voting Machine Design.			
12.	**OHT2**				
13.	31.	Analysis of Clocked-Sequential Circuits; State Equations, State Table, State Diagram, and Flip-Flop input equations.	5-5		
	32.	Analysis with D Flip-Flops, JK Flip-Flops, and T Flip-Flops.	5-5		
	33.	Mealy and Moore Models. Mealy-Moore Conversion Procedure.	5-5		
	Lab 11	Memory Elements: Latches and Flip-flops. Design of a positive edge triggered D flip-flop.			
14.	34.	State Reduction using Row Matching and Implication Table Techniques. State	5-7	15.3 Ref Book (4)	

		Assignment Method.			
	35.	Design Procedure- Synthesis using D Flip-Flops.	5-8		
	36.	Design Procedure- Synthesis using JK Flip-Flops, and T Flip-Flops.	5-8		
	Lab 12	Flip-Flop Applications & Proteus Simulation of Digital Circuits			
15.	37.	Problem Solving Session from Chap5			
	38.	**Introduction**: Registers with Parallel Load.	6-1		
	39.	Shift Registers; 4-Bit Shift Register; Serial Transfer and Serial Addition.	6-2		
	Lab 13	Sequence Detector Design. Sequential Logic Design using Verilog HDL			
16.	40.	4-Bit Universal Shift Register.	6-3		
	41.	Ripple Counters; Binary and BCD Ripple Counters.	6-3		
	42.	Synchronous Counters; Binary and BCD Counters.	6-4		
	Project Work				
17.	43.	Other Counters; Counters with unused states, Ring Counter and Johnson Counter	6-5		
	44.	Problem Solving Session from Chap6			
	45.	Course Revision			
	Project Evaluations/Final Exam				
18	**End Semester Exam**				

Lab Experiments:
Lab 1: Familiarization of Basic Gates and Digital ICs
Lab 2: Introduction to Verilog HDL. Basic language constructs and design entry using Verilog HDL.
Lab 3: Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Function implementation using Verilog HDL Gate-Level modeling.
Lab 4: Minimization of Boolean Functions and its Hardware implementation.
Lab 5: Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates. Gate-Level Modeling of Combinational Circuits using Verilog HDL.
Lab 6: BCD-to-Seven Segment Decoder Design.
Lab 7: Design of a 2-bit Magnitude Comparator using Classical design method. Combinational Logic Design using Verilog HDL.
Lab 8: Design of a 2-bit Adder/Subtractor Circuit. Combinational Logic Design using Verilog HDL.
Lab 9: Design of 4-bit ALU.
Lab 10: Voting Machine Design.
Lab 11: Memory Elements: Latches and Flip-flops. Design of a positive edge triggered D flip-flop. Sequential Logic Design using Verilog HDL
Lab 12: Flip-Flop Applications & Proteus Simulation of Digital Circuits
Lab 13: Sequence Detector Design. Sequential Logic Design using Verilog HDL

Tools / Software Requirement:
1. Verilog Hardware Description Language (Verilog HDL) software and HDL simulator ModelSim version 5.7f will be used for the design and simulation of logic circuits. 2. Digital and Embedded System lab will be used for hands on practice.

Grading Policy:	
Quizzes	A minimum of 6 Quizzes will be conducted during the semester in which students will be evaluated from the most recently covered topics. The purpose of these quizzes is to check student's comprehension level of students during lectures. The quizzes will be unannounced and bit challenging.
Assignments	In order to give enough practice and comprehensive understanding of the subject, six home assignments will be given to the students. Homework will be submitted at the beginning of class on the due date. The students are advised to do the assignment themselves. Copying

	of assignment is highly discouraged, taken as cheating case and dealt accordingly. No late submissions will be accepted.
Conduct of Labs	The labs will be conducted every week other than exam weeks as per the weekly schedule. A lab handout comprising pre-lab, in-lab, and post-lab report parts will be provided to the students for study and analysis during the week preceding each lab session. The students are expected to complete pre-lab work before lab starts and come prepared for the lab. Any student failing to complete pre-lab will not be allowed to attend lab session. The students will be evaluated during each lab based on demonstration, oral viva, and lab report submitted by them individually on completion of lab work. The students are required to be punctual in the lab; late comers will be penalized in award of marks. All the students are strictly instructed to wear masks, use sanitizers, and maintain social distance. Lab staff will check and impose heavy penalties in case of any violation. Any lab-related queries will be resolved with Lab Engr and genuine cases will be referred to teacher in case the issue is not addressed at that level.
Design Projects	The students will be allocated course projects if applicable during the week preceding OHT2 and evaluated before final exams based on parameters spelled out in Project Reservation form provided to them. The students will be grouped into syndicates with each syndicate having a maximum strength of 3 students depending upon the complexity level of design. However, any student desirous of carrying out design work individually will be encouraged and graded in the same pretext. The students are advised to select project titles well before their submission schedule. Alternately, students may be evaluated through final lab exam.

Other Matters:	
Online Discussions	In this semester we will be using section-level WhatsApp for as an announcement platform. However, teams will be used for outside class discussions and problems solving. CRs will be responsible for creation and admin of their respective sections WhatsApp groups.
Academic Honesty and Plagiarism	Plagiarism is the unacknowledged use of other's work, including the copying of assignments and laboratory results from the other students. Plagiarism is considered a serious offence by the university and severe penalties apply. Therefore, all the students must display originality of efforts and avoid plagiarism in any form.
Classroom Etiquettes	It is the collective responsibility of all the students to make the class environment conducive for learning. To create and maintain a friendly atmosphere, the following standards of classroom behavior will be observed: - 1. Students both hostelites and day scholars will attend classes as per the weekly schedule issued by Academic Coordination Branch (ACB). 2. Students will be punctual for the class. The teacher considers late comers disrespectful of those who manage to be on time. 3. If a student decides to attend the class, he or she will not disrupt class by leaving before the lecture has ended. 4. All the cell phones must be switched OFF prior to entering the classroom. 5. **The students must wear face masks, keep hand sanitizers in their bags and use them, periodically wash their hands, and ensure minimum distance of six feet in the class.** 6. **The students must use sanitizers before and after using trainers and other lab accessories and perform labs singly.**

Conduct of Classes:

Due to COVID-19 the classes will be conducted in hybrid mode (FTF/DL). The existing sections will be divided into two groups (Gp-1 & Gp-2). Both groups will attend an equal number of classes i.e 50% both in FTF and DL mode but on the alternate days as per the following plan

Week#	Mode	Monday	Tuesday	Wednesday	Thursday	Friday
First Week/ Odd Week	FTF	Grp-1	Grp-2	Grp-1	Grp-2	Grp-1
	DL	Grp-2	Grp-1	Grp-2	Grp-1	Grp-2
Second Week/ Even Week	FTF	Grp-2	Grp-1	Grp-2	Grp-1	Grp-2
	DL	Grp-1	Grp-2	Grp-1	Grp-2	Grp-1

Codes for MS teams:

The students in DL mode will use the following codes to join MS teams

Section C Link:
https://teams.microsoft.com/l/team/19%3anZ2reYb8CgUEMbmESaH9mg_BH12z4QrTZXw1Qh1gW9A1%40thread.tacv2/conversations?groupId=add9ab19-88b3-412f-88d8-e416be6728eb&tenantId=1511ab2e-502b-4e2d-bd68-f679f549b5a2

Section D Link: https://teams.microsoft.com/l/team/19%3atJ0bMYu_Ph_-nUUAHsRcAGyD2eRzURTrzafxSFkPmnY1%40thread.tacv2/conversations?groupId=01f5fb66-bd95-4b43-86f4-208d505e4df6&tenantId=1511ab2e-502b-4e2d-bd68-f679f549b5a2