How fast can we run the clock?

Revisited to account for flip-flop constraints

Two Requirements

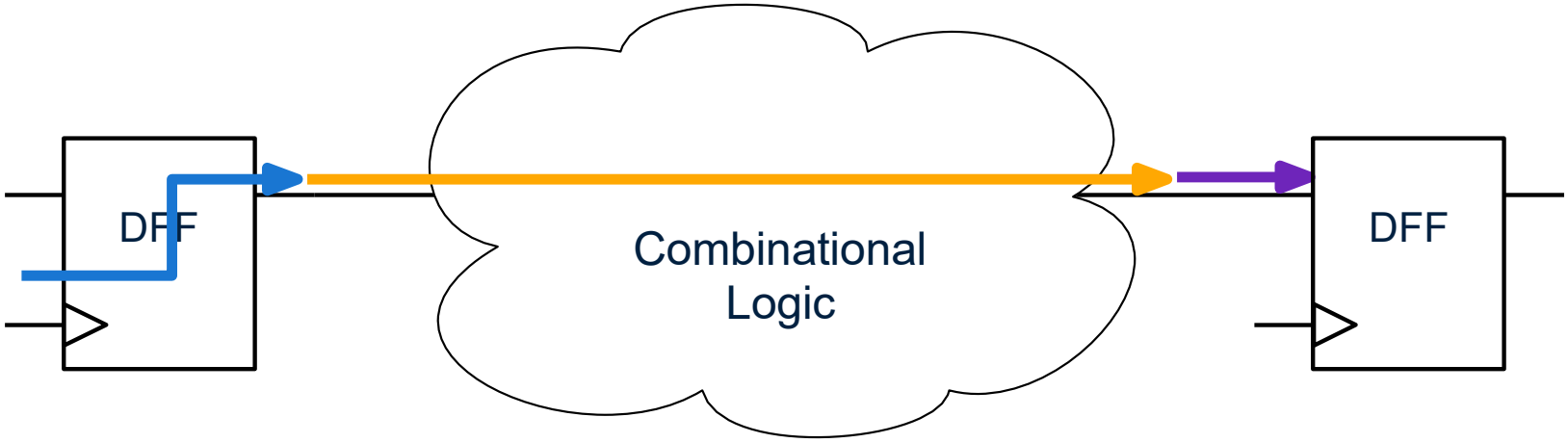
1. Setup Requirement:
   - Input values must be ready for destination flop ahead of when the rising clock edge arrives.

2. Hold Requirement:
   - Input values of destination flop must not change for a short time after rising clock edge.

Setup Time Requirement

After clock rising-edge, there must be enough time so that:

1. source flip-flop's output can settle to correct value
2. critical path can settle to correct value
3. value arrives at destination flip-flop early enough for setup time



$$t_{Clock\text{-}min} >= t_{clk-to-q\max} + t_{CriticalPath} + t_{setup}$$

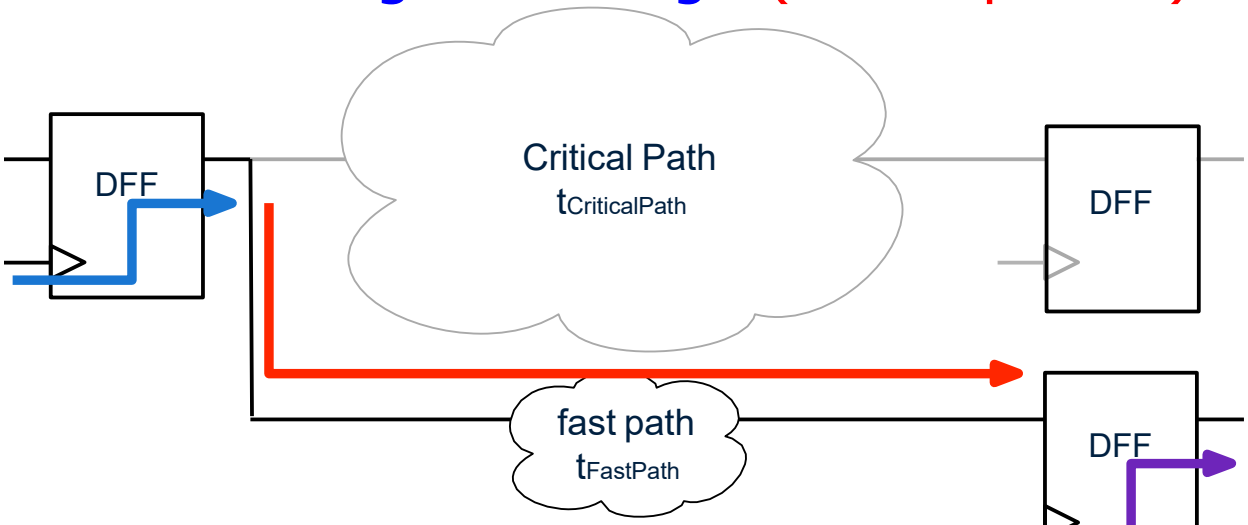
Also known as MaxPath Timing Constraint

Key Concept for Setup Time:

Must have enough time for input of destination FF to settle before destination FF reads in value

Hold Time Requirement

- Input values of destination flop must not change for a short time after rising clock edge (for all paths!)

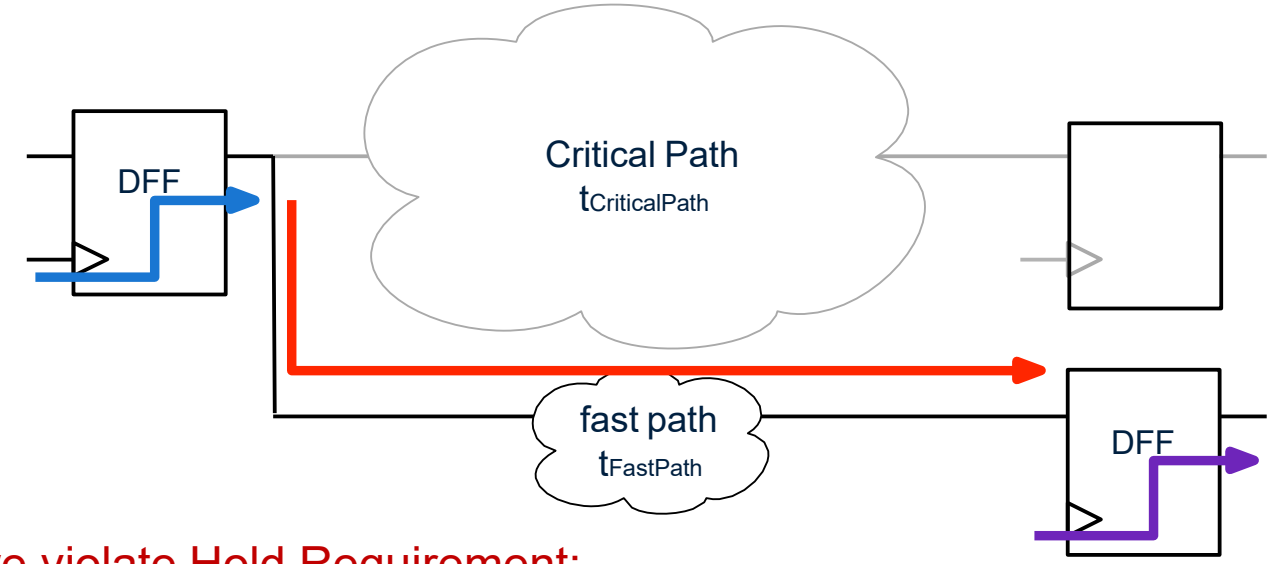


$$t_{clk-to-q\min} + t_{path} >= t_{hold}$$

Minimum clk-to-q delay because we need to design for the fastest possible arrival time of signal to destination flop

Also known as MinPath Timing Constraint

Hold Time Requirement



Say that we violate Hold Requirement:

$$t_{clk-to-q\,\min} + t_{FastPath} < t_{hold}$$

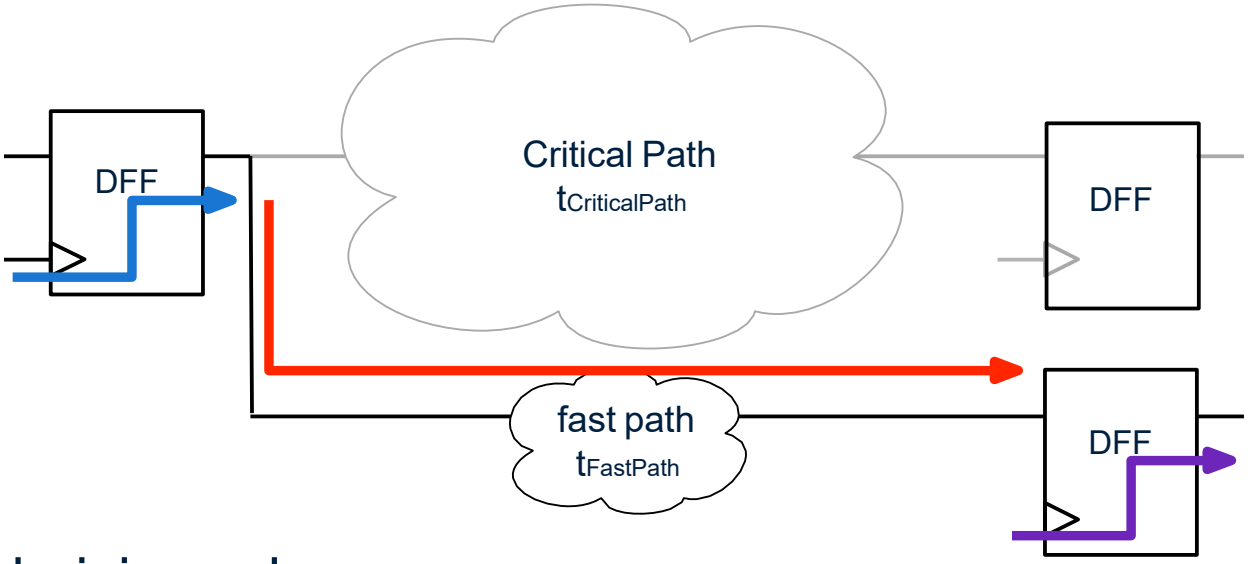
After clock rising-edge,

1. source flip-flop's output settles
2. fast path settles SUPER QUICKLY to correct value
3. destination flop is still reading in "old" value from fast path logic (i.e. hold time has not yet passed for that reading)

(i.e The new value from source FF can get there so fast that when the clock arrives the new value may change before it has been latched into destination FF.)

Hold Time Requirement – (1)

- Consider the example cct below:



- After clock rising-edge,

1. source flip-flop's output settles
2. fast path settles SUPER QUICKLY to correct value
3. destination flop is still reading in "old" value from fast path logic (i.e. hold time has not yet passed for that reading)
   - i.e The new value from source FF can get there so fast that when the clock arrives the new value may change before it has been latched into destination FF

Hold Requirement

- Remember, after rising edge of clock, FF is now reading in data. Input to the FF cannot change for t_{hold} amount of time!
  - Unlikely to be a problem for Critical Path
  - Need to be careful for the **fast (non-critical) path**
    - **Key: Consider what happens when the same clock edge is considered at both the source and destination flops.**

Note: On each clock cycle, flip-flop is BOTH reading in a new value (when you look at it as a destination flip-flop) AND providing a value to the next stage (when you look at it as a source flip-flop)

How to Fix Timing Violations?

- Setup Violation:
  - Slow down clock
  - Move registers around (reduce length of critical path)

- Hold Violation:
  - CANNOT address by changing clock frequency!
  - Can add more gate-delays to path (e.g. add buffers)

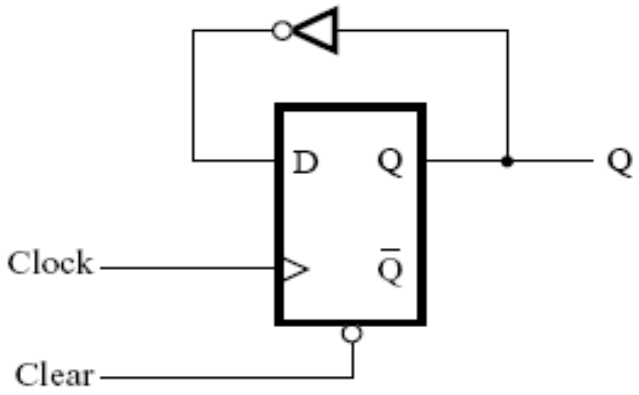
GOOD NEWS! CAD Tools handle all this for you!

Well not all the time! You may need to do timing closure manually, which could be quite a task!

But its not an excuse! the material in this slide set will definitely be on the exam

Timing Analysis: Examples

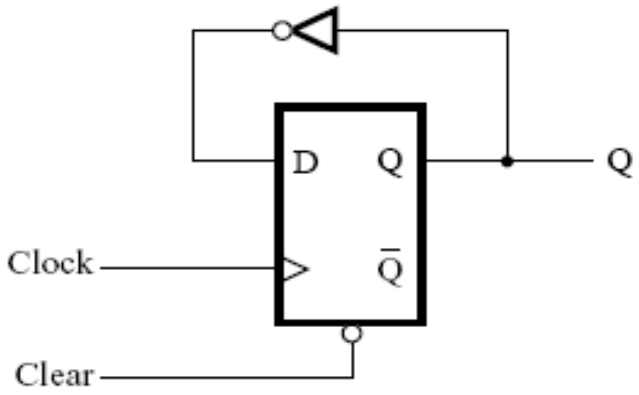
Example: Timing Analysis



- Given flip-flop timing parameters:
  - t_{su} = 0.6 ns,
  - t_h = 0.4 ns, and
  - 0.8 ns ≤ t_{cQ} ≤ 1.0 ns
  - Not delay: 1.1ns

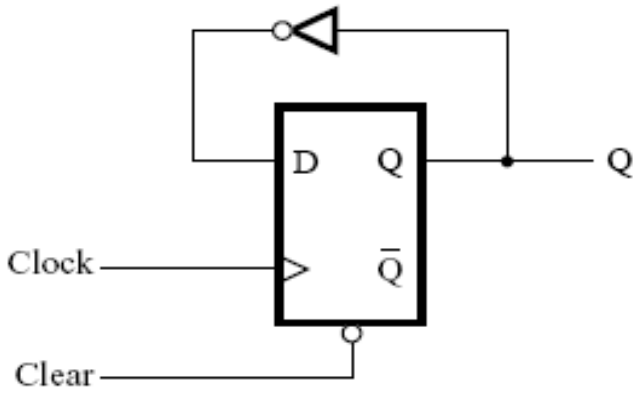
- Find out F_{max} and hold time violations?

Example: Timing Analysis



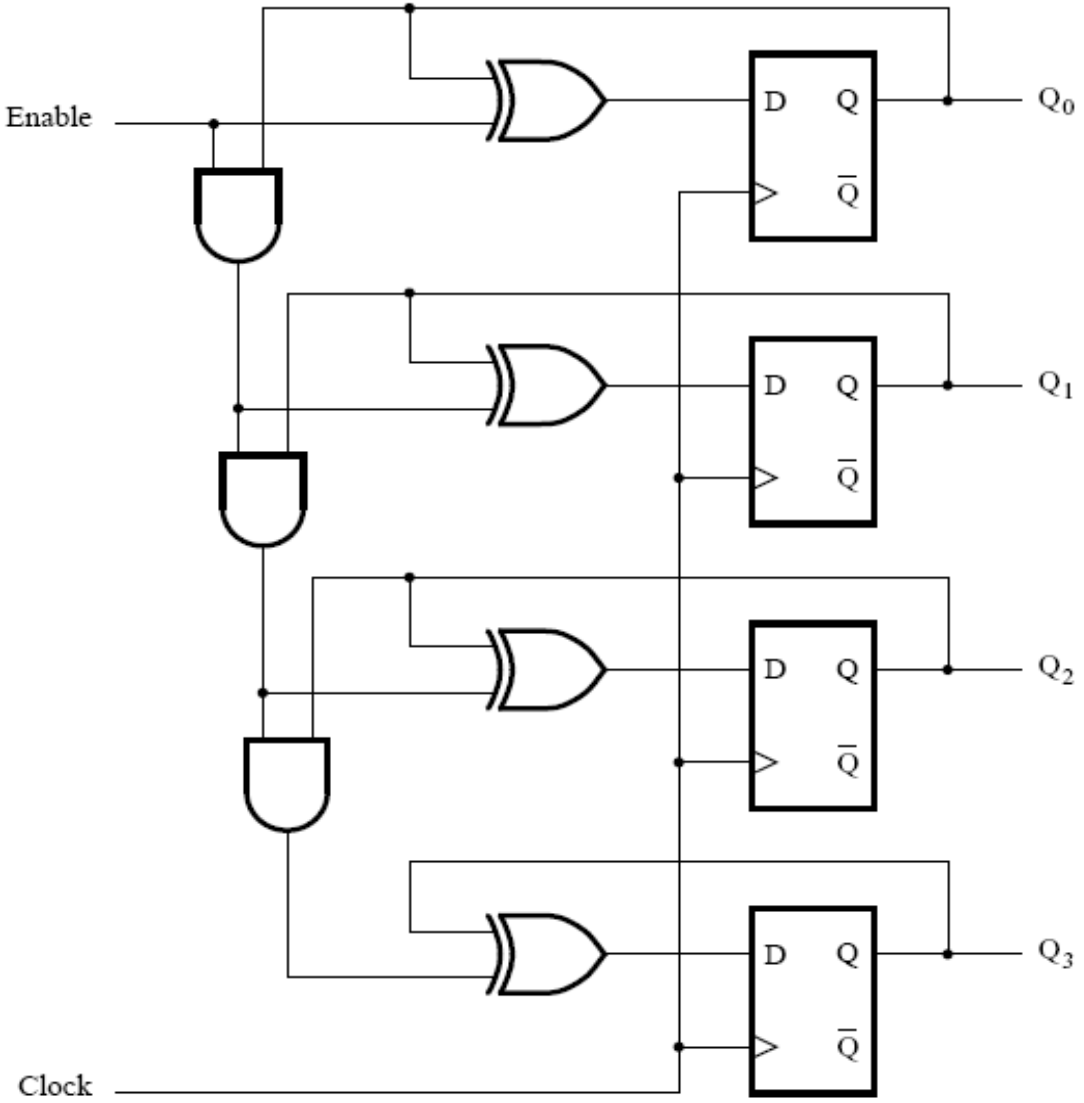
- $T_{min} = 1/F_{max}$
- Consider all paths in the circuit that start and end at flip-flops
- $T_{min} = t_{cQ} + t_{NOT} + t_{su}$
  - $T_{min} = 1.0 + 1.1 + 0.6 = 2.7$ ns
- $F_{max} = 1/2.7$ ns $= 370.37$ MHz

Example: Timing Analysis



- Hold time violation:
  - examine the shortest possible delay from a positive clock edge to a change in the value of the D input.
  - The delay is given by $t_{cQ} + t_{NOT} = 0.8 + 1.1 = 1.9$ ns.
  - Since 1.9 ns > t_h = 0.4 ns there is no hold time violation.

Class Exercise: Timing Analysis

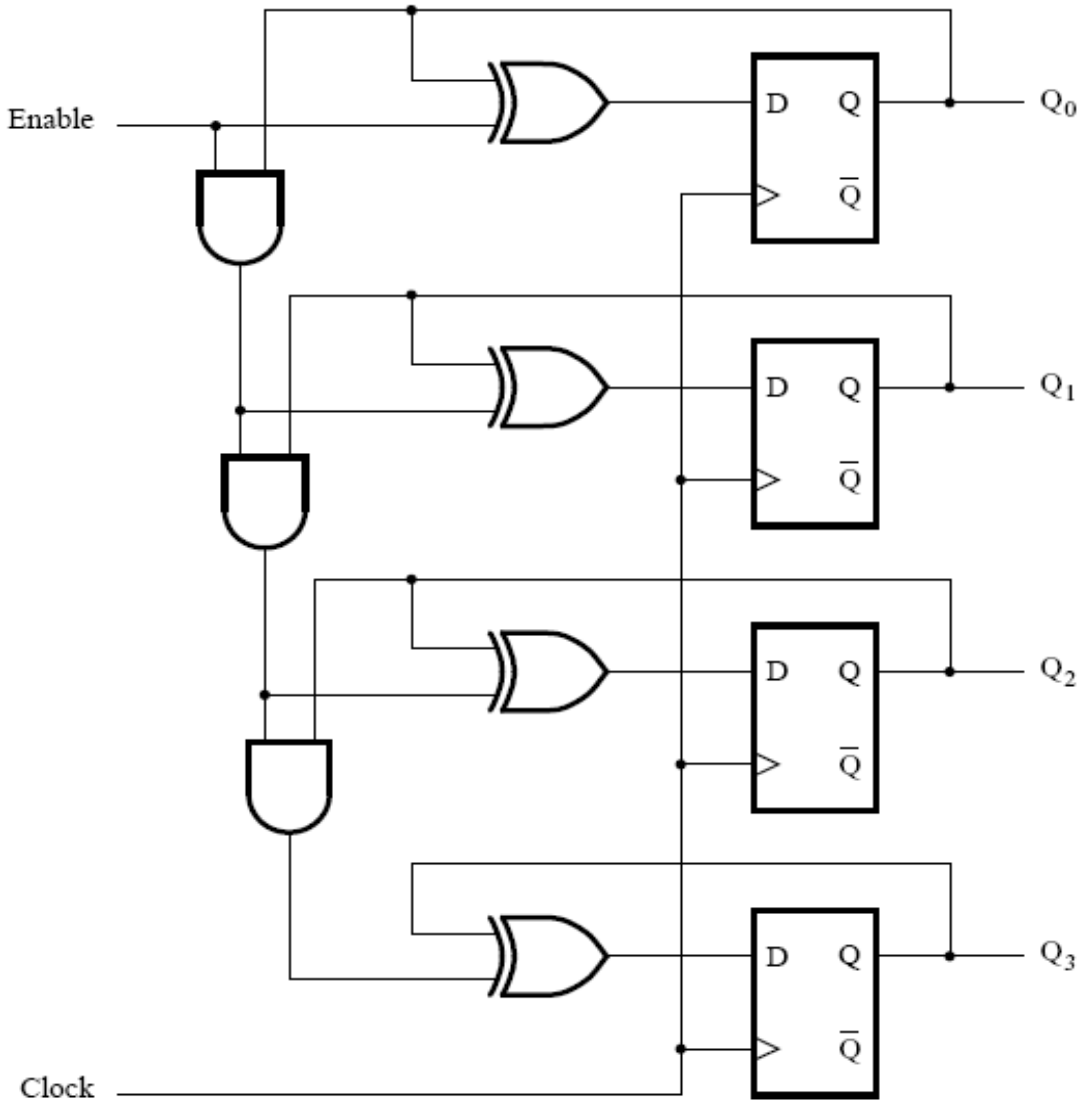


Assume the same FF timing parameters as we did in our previous example.

Assume the gate delay of 1.2ns.

Calculate the maximum clock frequency for which this circuit will operate properly and find out if there is any hold-time Violation?

Class Exercise: Timing Analysis



There are many paths in this circuit that start and end at flip-flops.

The longest such path starts at flip-flop Q0 and ends at flip-flop Q3.
Aka: Critical Path

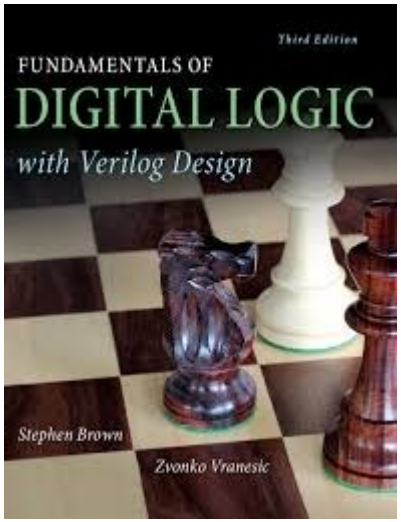
The delay of the critical path includes the clock-to-Q delay of flip-flop Q0, the propagation delay through three AND gates, and one XOR-gate delay.

Tmin = tcQ + 3(tAND) + tXOR + tsu
Tmin = 1.0 + 3(1.2) + 1.2 + 0.6 ns = 6.4 ns
Fmax = 1/6.4 ns = 156.25 MHz

The shortest paths through the circuit are from each flip-flop to itself, through an XOR gate. The minimum delay along each such path is tcQ + tXOR = 0.8 + 1.2 = 2.0 ns. Since 2.0 ns > th = 0.4 ns there are no hold time violations.

Recommended Reading

- Digital System Design with Verilog HDL, 3/e, b **S**tephen Brown and **Z**vonko Vranesic. [**S&Z**]
  - S&Z,
    - Chapter-5
      - 5.4.4
      - 5.15



THANK YOU