Chapter5-Synchronous Sequential Logic

Lecture4- Understand Timing Behavior of Latches and Flip-Flops, Study Mealy and Moore Finite State Machines (FSM)

Objectives

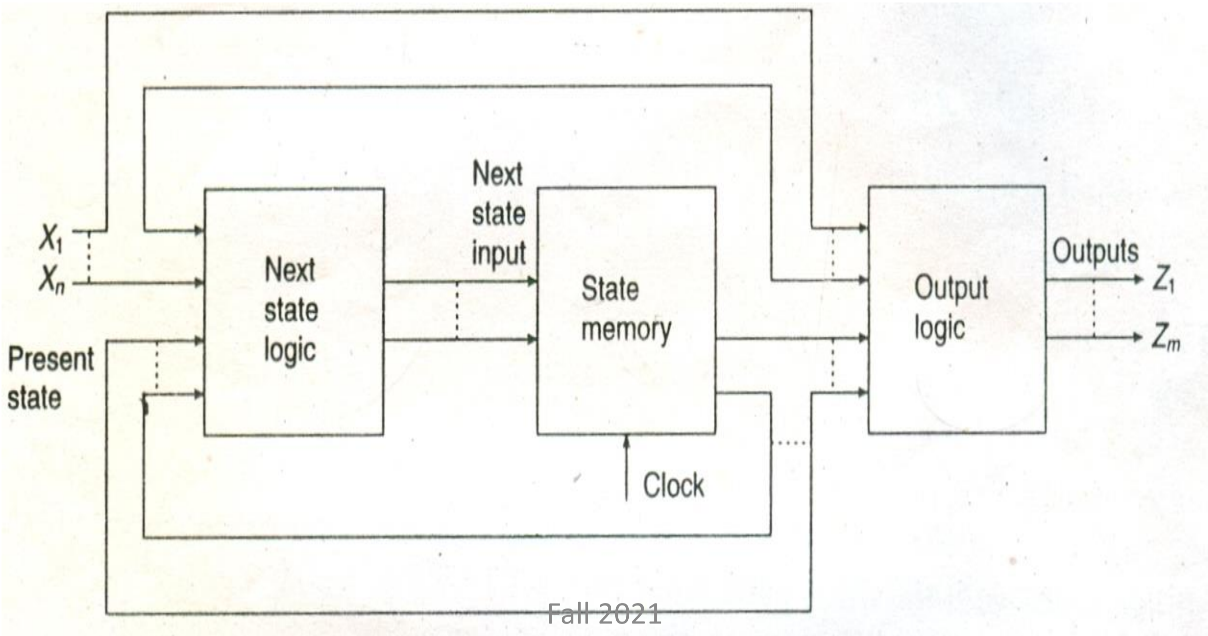
- Understand the timing behavior of Latches and Flip-flops
- Study Mealy and Moore Finite State Machines (FSM)

Mealy and Moore Models

- There are two types of synchronous sequential machines namely Mealy and Moore. These machines differ in the way the output is generated.
  - In the first type of machine the output depends on both its present state and also its inputs. This type of machine is referred to as the Mealy machine and its behavior is defined by the following equations:

    Next State=f(Present State, inputs)

    Output=g(Present State, inputs)

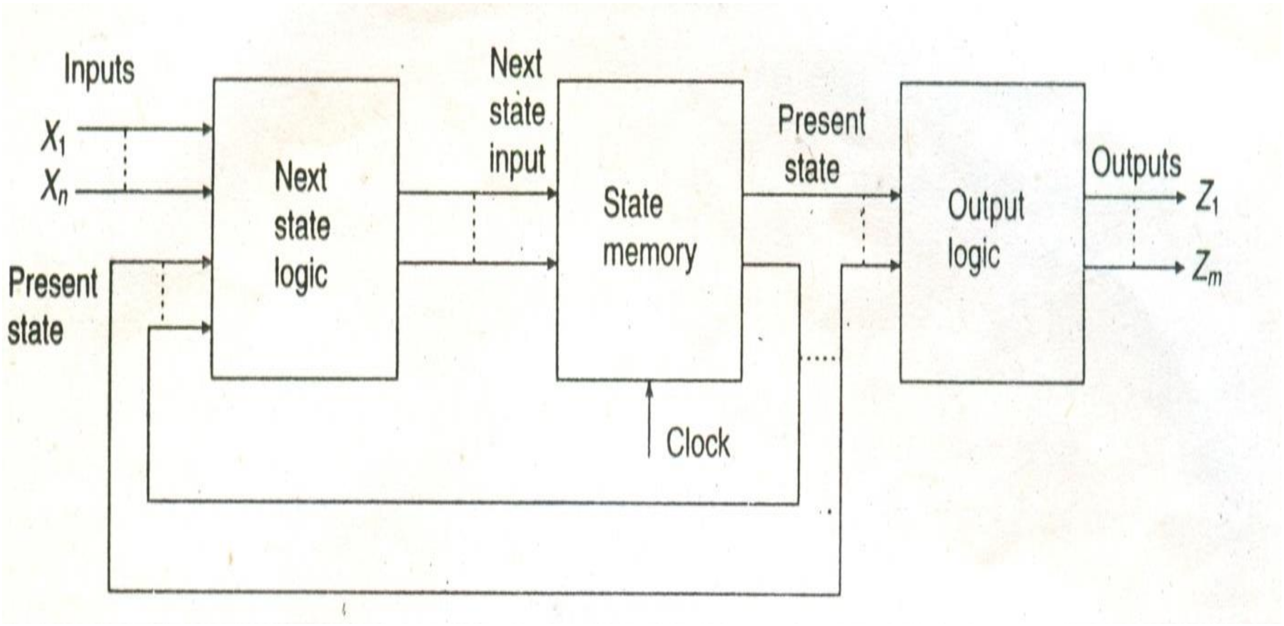


Mealy and Moore Models

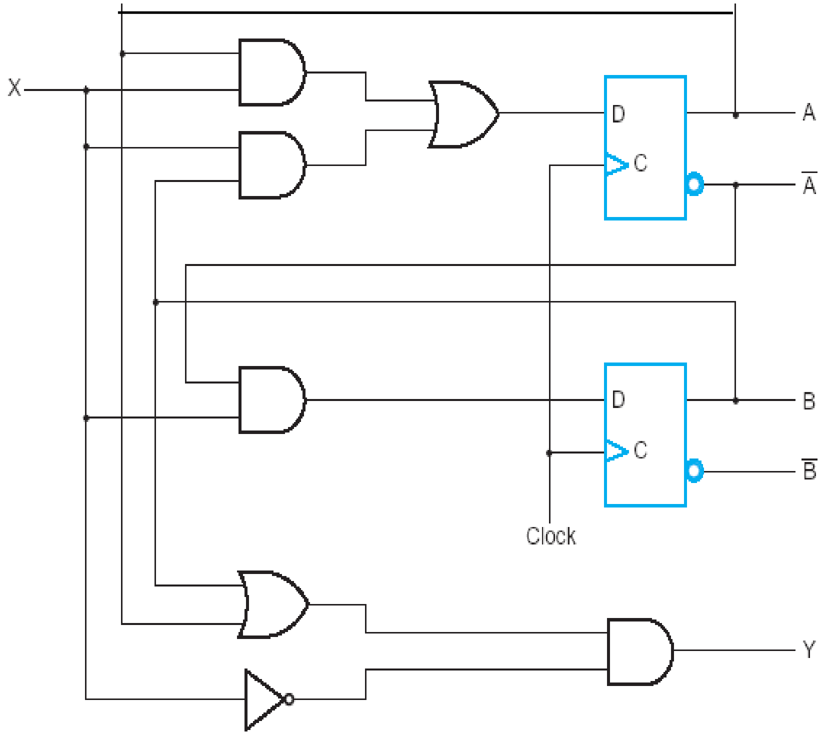
The second of these machines has an output that depends only on its present state and is referred to as Moore machine. The behavior of the machine is defined by the following equations:

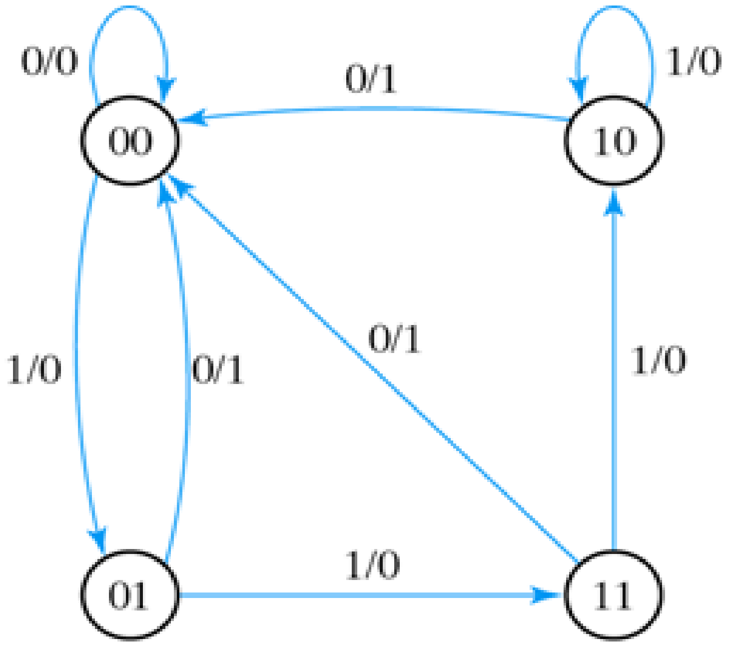
Next State=f(Present State, inputs)

Output=g(Present State)



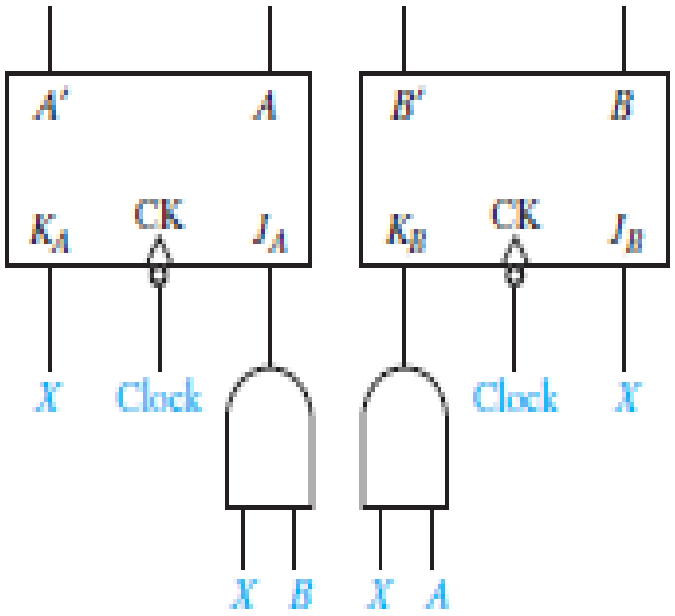
Example Mealy Model

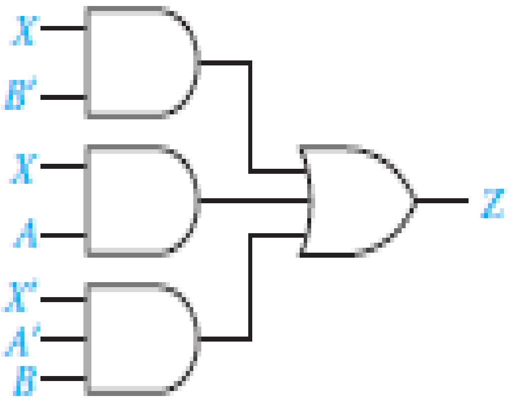


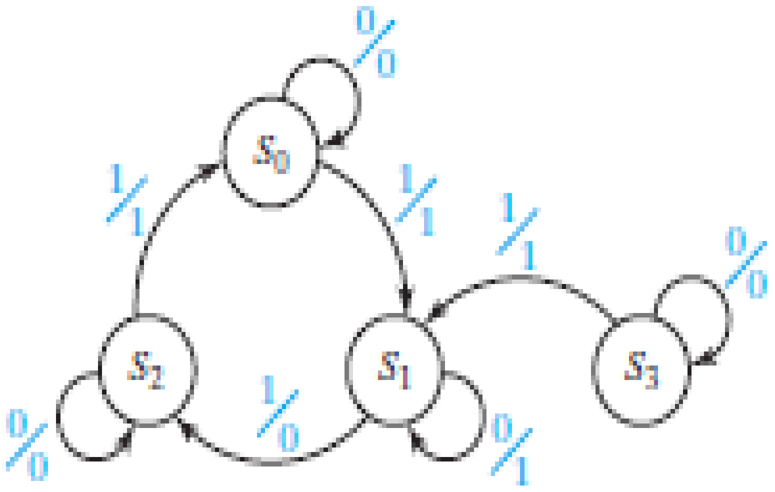


The above sequential circuit is Mealy FSM since output y is a function of both input x and the present state of A and B.

Example Mealy Model Cont…

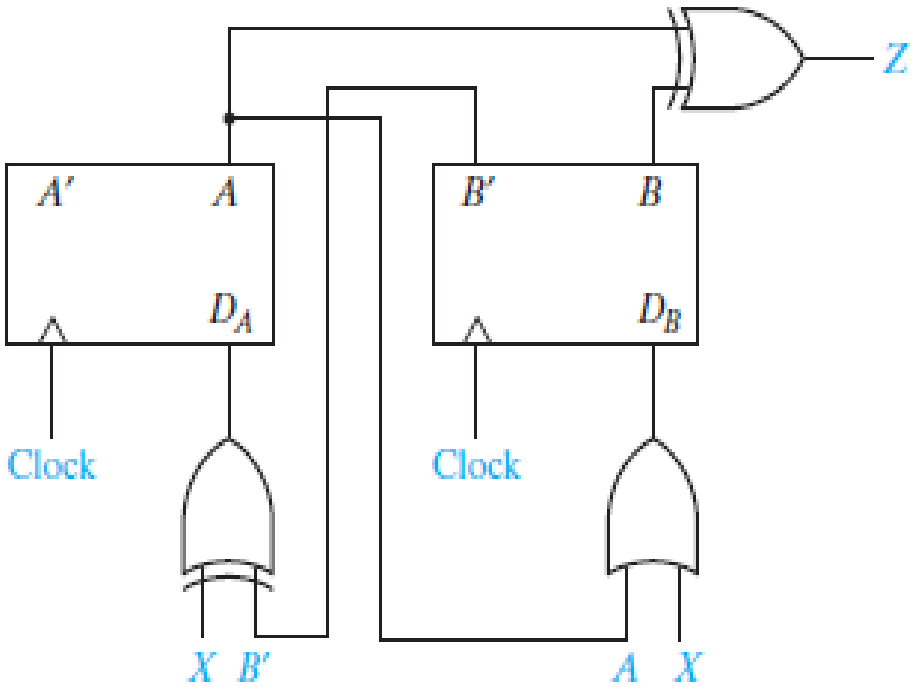


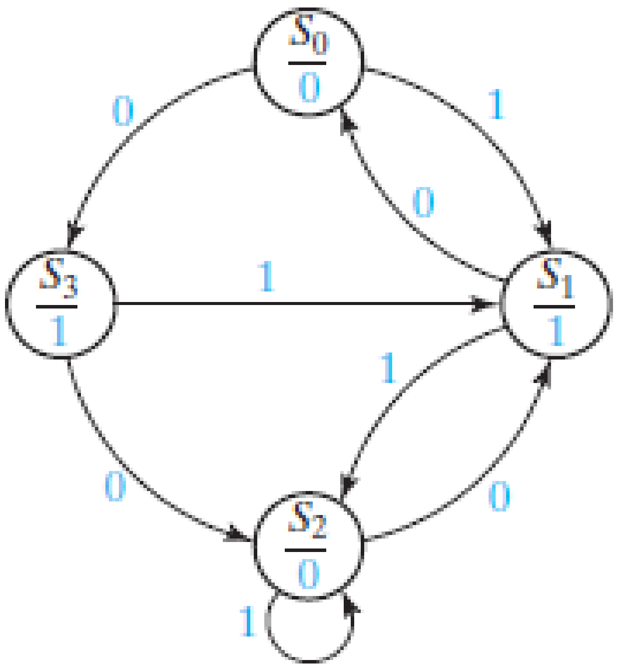




The above sequential circuit is Mealy FSM since output y is a function of both input x and the present state of A and B.

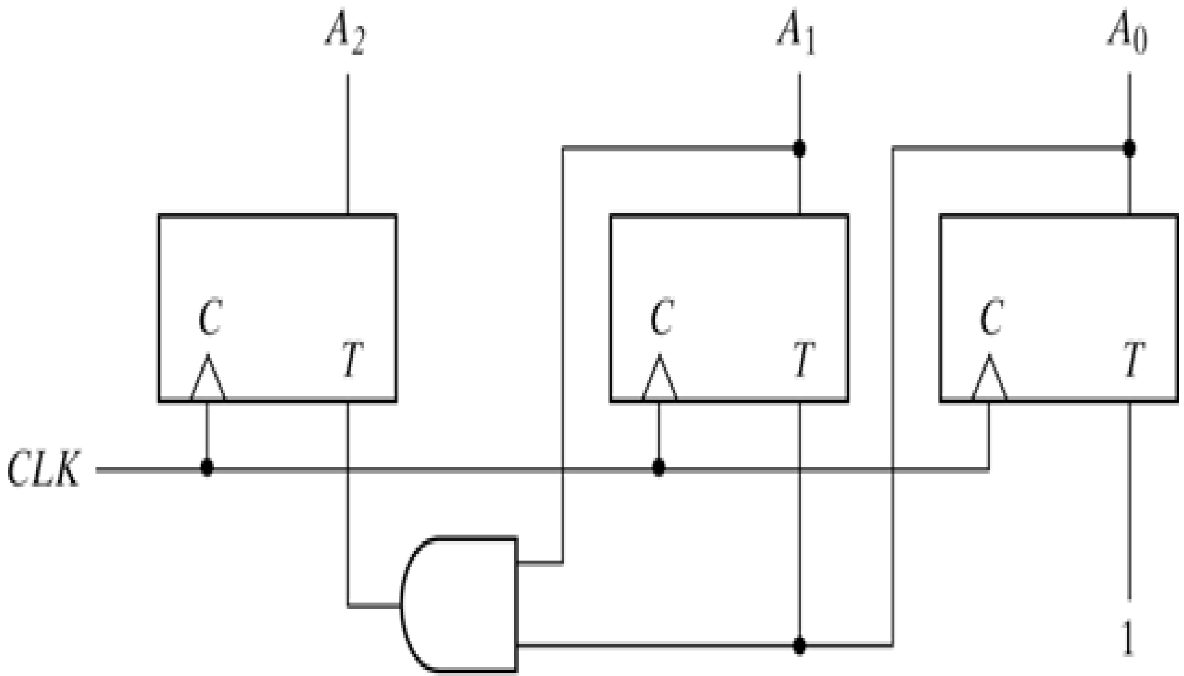
Example Moore Model

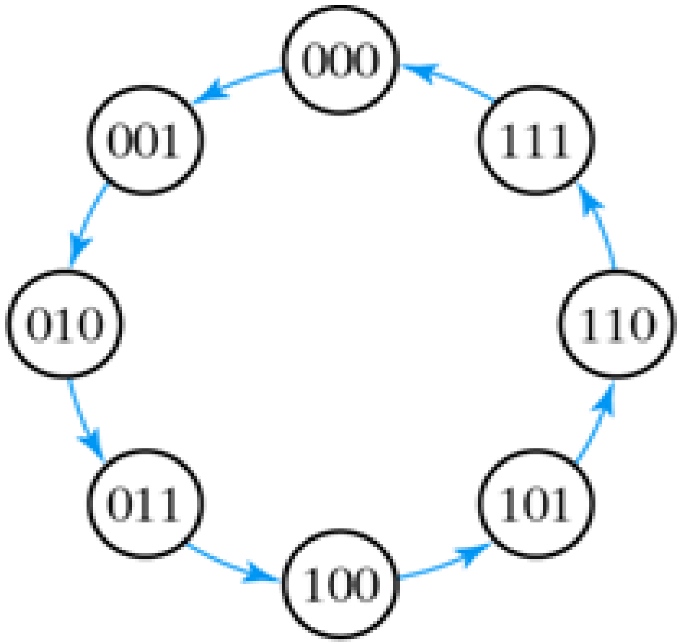




The above sequential circuit is Moore FSM since output is a function of the present state of flip-flops A and B only.

Example Moore Model Cont…





The above sequential circuit is Moore FSM since output is a function of the present state of flip-flops A and B only.

Notes on Mealy and Moore

- In the Moore model, the outputs of the sequential circuit are synchronized with the clock because they depend on only flip flop outputs that are synchronized with the clock.
- In the Mealy model, the outputs may change if the inputs change during the clock cycle and the outputs may have momentary false values because of the delay encountered from the time that the inputs change and the time that the flip flop outputs change.
  - To synchronize a Mealy type circuit, the inputs of the sequential circuit must be synchronized with the clock and the outputs must be sampled only during the clock edge.

Comparison of Mealy and Moore FSM

Mealy

- Output depends on current input and state.
- Output changes asynchronously with the enabling clock.
- Will have the same or fewer states than a Moore machine.
- Faster because output appears earlier once input changes.
- Output occurs in same state by change in input.
- Less stable due to glitches/false outputs encountered with asynchronous behavior.
- Somewhat difficult to clock.
- More power efficient due to less number of flip flops.
- A counter is not a Mealy machine.

Moore

- Output depends only on current state.
- Output changes synchronously with this clock edge.
- Will have more states than Mealy machine.
- Slower because of one clock cycle delay.
- Output is delayed i.e doesn’t occur until next change.
- More stable due to synchronous behavior.
- Generally easier to clock.
- Less power efficient.
- A counter is a Moore machine.

Conversion from Moore to Mealy

- To convert Moore to Mealy, we look for the states and their associated outputs. This can be obtained from the first and last column of the state table.
- Now, we draw the Mealy machine table and write these outputs associated with each of the states with a slash.
- Eliminate equivalent states where possible, the resulting state table will be for Mealy machine.

Conversion from Moore to Mealy Example

Present State	Next State X=0	Next State x=1	Output y
S_0	S_0	S_1	0
S_1	S_0	S_2	0
S_2	S_0	S_3	0
S_3	S_0	S_3	1

Present State/Output relations are:
$S_0/0$; $S_1/0$; $S_2/0$; $S_3/1$
Move outputs with next states

Present State	Next State X=0	Next State x=1
S_0	$S_0/0$	$S_1/0$
S_1	$S_0/0$	$S_2/0$
S_2	$S_0/0$	S_2 $\cancel{S_3}/1$
~~S_3~~	~~$S_0/0$~~	~~$S_3/1$~~

$S_2 \equiv S_3$
Remove S_3 from the state table.

Conversion from Moore to Mealy Example

- Move the outputs in the output section to obtain Mealy State Table.

Present State	Next State		Output Y	
	X=0	x=1	X=0	x=1
S_0	S_0	S_1	0	0
S_1	S_0	S_2	0	0
S_2	S_0	S_3	0	1

The End