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**Department of Electrical Engineering**

**Faculty Member:** Arshad Nazir **Dated:** 21/09/2021

**Semester:** 3rd **Section:** BEE 12C

**Group No.: 7**

**EE-221: Digital Logic Design**

Lab 1: FAM of Basic Gates and ICs

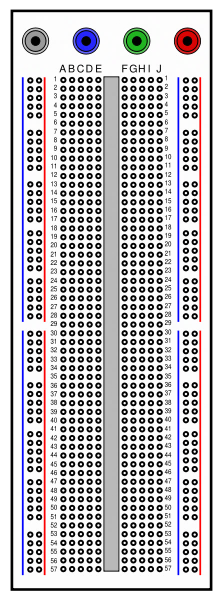
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| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **PLO4/CLO4** | **PLO4/CLO4** | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |  |
| **Name** | **Reg. No** | **Viva / Lab Performance** | **Analysis of data in Lab Report** | **Modern Tool Usage** | **Ethics and Safety** | **Individual and Teamwork** | **Total marks Obtained** |
|  |  | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **25 Marks** |
| **Muhammad Adil Azeem** | 342459 |  |  |  |  |  |  |
| **Muhammad Umer** | 345834 |  |  |  |  |  |  |
| **Raahim Ahmad Waqar** | 342287 |  |  |  |  |  |  |
| **Saad Bakhtiar** | 341150 |  |  |  |  |  |  |
| **Syed Aun Ali Kazmi** | 342384 |  |  |  |  |  |  |

**Introduction:**

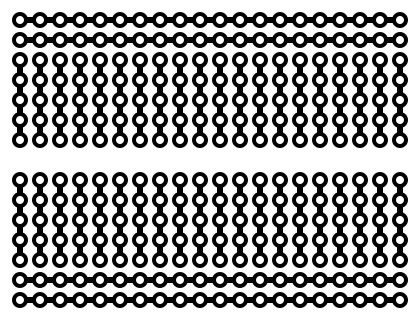
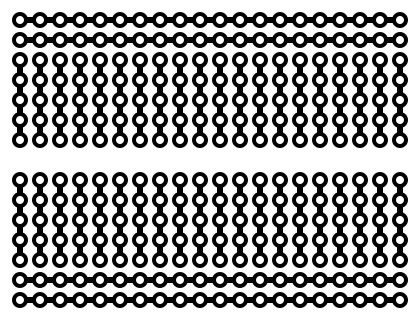
Logic gates are the heart of digital electronics. A gate is an electronic device which is used to compute a function on a two valued signal, and they are the basic building block of digital circuits. By combining logic gates, we can design many specific circuits like flip flops, latches, multiplexers, shift registers etc. The purpose of this lab is to familiarize ourselves with the functioning of the fundamental gates as well as patching ICs on a breadboard.

**Breadboard**

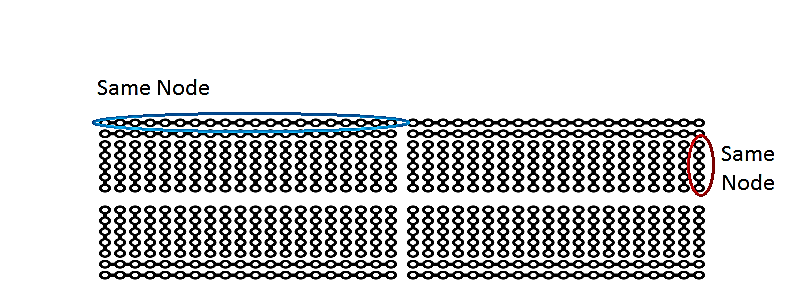
Breadboards are usually used for patching small circuits and prototypes. A typical breadboard would look like this.



The internal connections are as shown below:



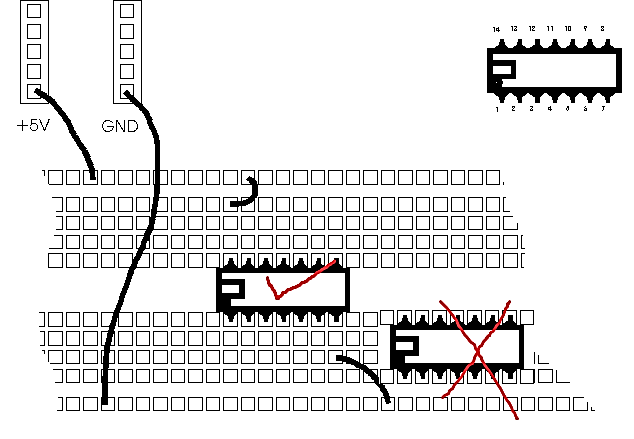
The points in ABCDE (and FGHIJ) grid are vertically connected as indicated by red circle. So, all 5 points on are the same point. It makes No difference whether you connect a wire on any one of these points. The next vertical strip is a different point and so on**. *It should be noted that upper and lower grids are horizontally connected indicated below. Each grid consists of 4 such separate horizontal strips:***



**IC Placement on Breadboard**

A typical 14 pin IC placement on such a bread board is shown below:

The upper and lower horizontal strips are normally served for power (+5V) and ground (0V) respectively. But it is not necessary to do so.



**Never place any IC such that its opposite pins are within (connected to) the same Node on the same grid.**

## 

**Lab Description**

This lab is about the introduction to the three fundamental logic gatesnamely the **AND, OR and NOT gates** and how to use and verify them using ICs in both ways i.e., software and hardware. Verification through simulation will be done through **Proteus** whereas the hardware implementation is done on a **Digital Training System**.

## Lab 1: Familiarization of Basic Gates and Digital ICs

This Lab Activity has been designed to familiarize the beginning students with logic gates and IC chips, using breadboard and testing of gates and logic circuits.

**Objectives:**

* Familiarize the students with ICs, their categories, and different logic families.
* Identify ICs based on series number as well as their functional behavior and pin numbers.
* Search data sheets of ICs from different sources and optimally use them in the design of digital circuits.
* Perform functional verification of basic logic gates by listing the truth tables and establishing IN/OUT relationship.
* Carry out best wiring practices in digital design.

**Lab Instructions:**

* This lab activity comprises three parts, namely Pre-lab, Lab tasks, and post-lab viva session.
* The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for subsequent evaluation. Alternately each group to upload completed lab report on LMS for grading.
* The students failing to complete Pre-lab will not be allowed to attend lab session.
* The students will start lab task and demonstrate design steps separately for stepwise evaluation (teacher/lab engineer will sign each step after ascertaining functional verification). Any report submitted without teacher/lab engineer signatures will not be accepted.
* Remember that a neat logic diagram with pins numbered and nicely patched circuit will simplify troubleshooting/fault diagnostic process.
* After completion of lab, the students are expected to unwire the circuit and deposit back components to lab staff.
* The students will complete lab task within the prescribed time and submit complete report to lab engineer before leaving the lab.
* There will be a viva session after demonstration for which students will be graded individually.

**Pre-Lab Tasks: (5 marks)**

1. **Read the topic Integrated Circuits (2.9) from your course book and answer the following questions:**

Digital ICs can be categorized according to the complexity of their circuits usually termed as *scale integration*. The following are the six major categories. Give their full names and range of gates available in each of them.

|  |  |  |
| --- | --- | --- |
| **SSI** | Small Scale Integration | Less than 12 gates |
| **MSI** | Medium Scale Integration | 12 – 99 gates |
| **LSI** | Large Scale Integration | 100 – 9999 gates |
| **VLSI** | Very Large-Scale Integration | 10000 – 99999 gates |
| **ULSI** | Ultra-Large-Scale Integration | 100000 – 999999 gates |
| **GSI** | Giga Scale Integration | 1000000 – More gates |

1. **Another categorization is with respect to the Logic Families of Digital ICs. The seven of these are listed below. Give their full name and give their utilization in terms of speed, power etc. (e.g., Low Power, High Speed).**
2. **RTL – Resistor Transistor Logic**

Slow speed, draws significant amount of current from the supply for each gate

1. **ECL – Emitter-Coupled Logic**

High speed operation, propagation delay less than a nanosecond, high power usage

1. **TTL – Transistor-Transistor Logic**

Less power consumption as compared to ECL but substantially slower operation speed

1. **DTL – Diode Transistor Logic**

Low speed relative to TTL, better noise margins and greater fan-outs than RTL

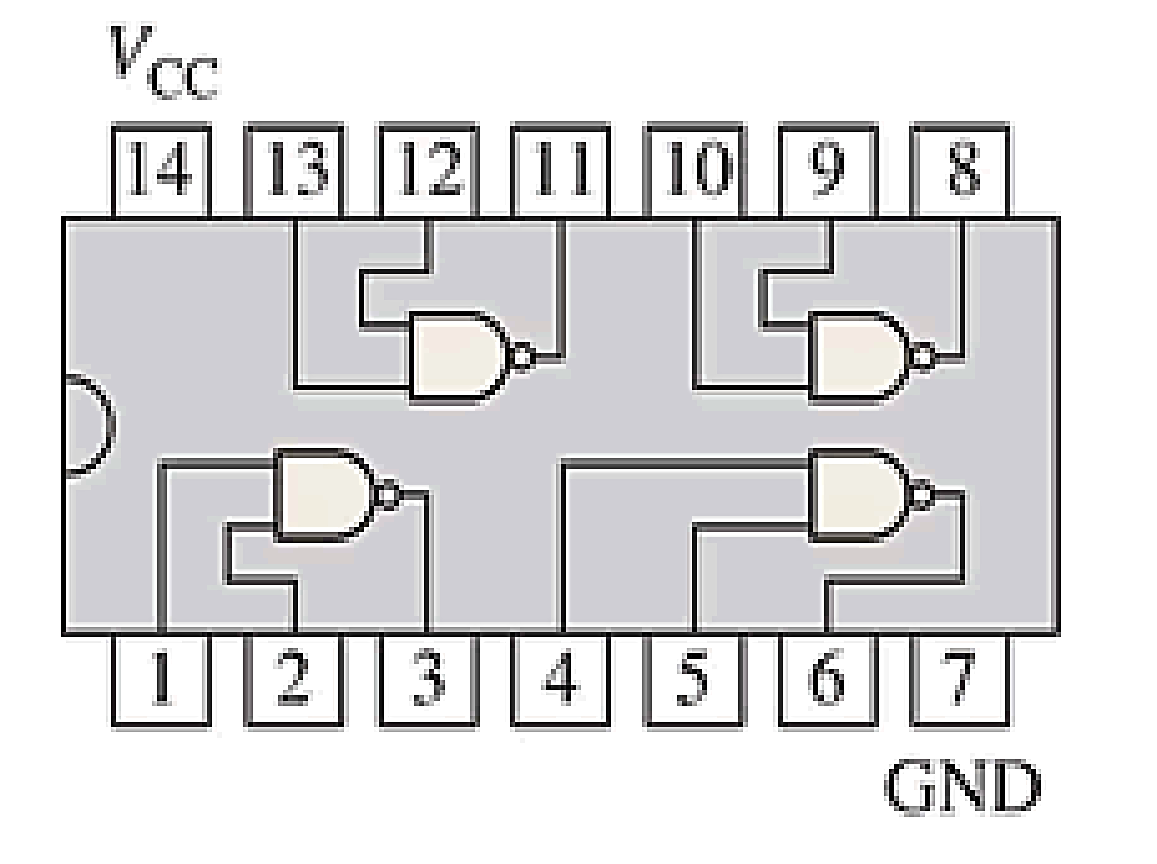
1. **CMOS – Complementary Metal Oxide Semiconductor**

Low static power consumption, high noise immunity, complex implementation

1. **Differentiate b/w Fan in and Fan Out of an IC.**

Fan-in refers to the maximum number of inputs available in a logic gate whereas Fan-out refers to the number of standard loads that a typical gate can drive without disturbing its normal operation.

**IC Pin Numbers:**

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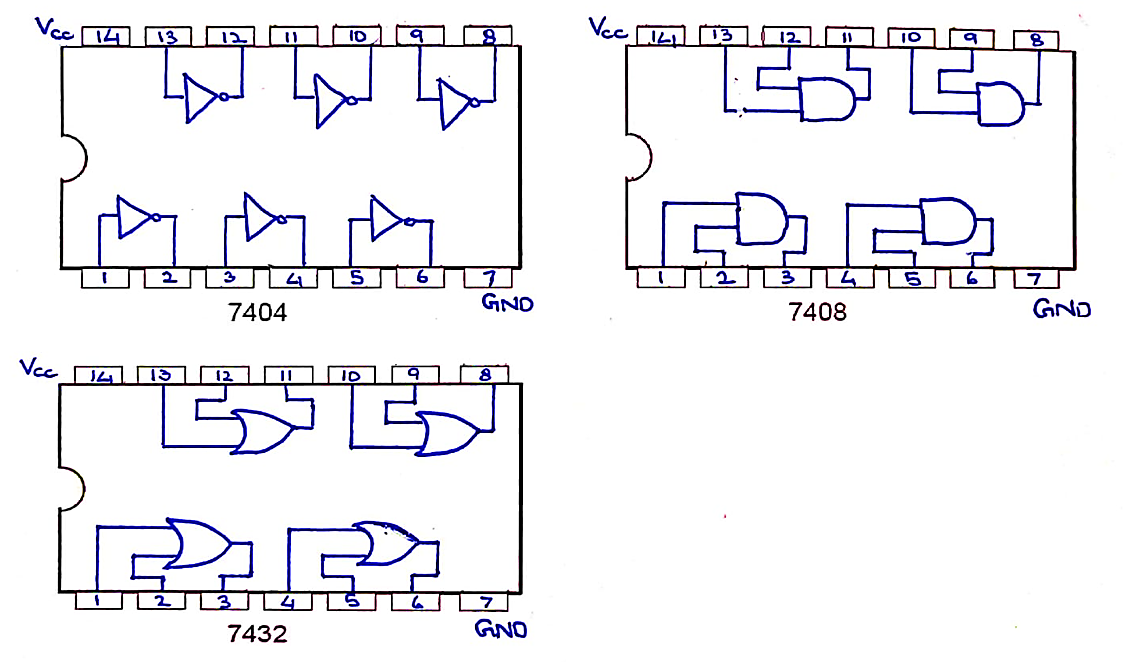
**Top View**

Most of the ICs have a Notch (or sometimes a dot) to denote the start of the PIN numbering. Place the IC such that the Notch is on left side, then the lower left PIN is numbered 1, and the numbering continues in the anticlockwise direction.

**Datasheet:**

The information about any IC (its number of pins and gates inside it) can be found by simply searching by its name on internet. The document containing information about the IC is called its **datasheet**. Different manufacturers of these chips have this information on their sites.

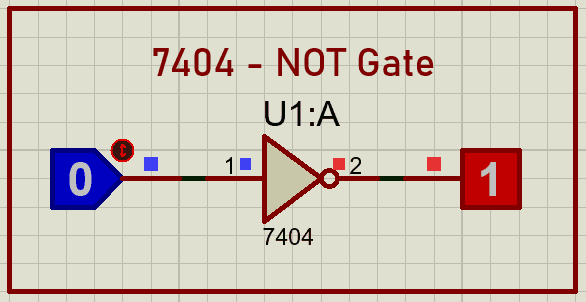
1. **Show the correct pin numbering and connection of gates inside these blank chips with the help of their datasheets.**



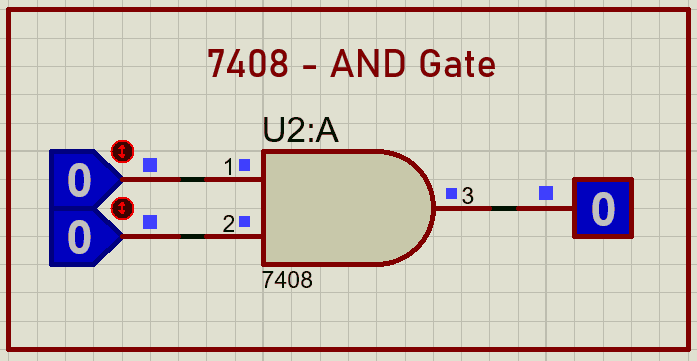
1. **Mention the manufacturer whose datasheet you consulted.**

TexasInstruments

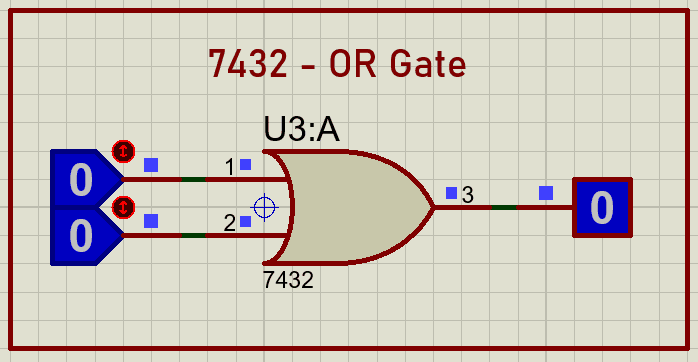
**Proteus Simulation**

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**NOT Gate Simulation**

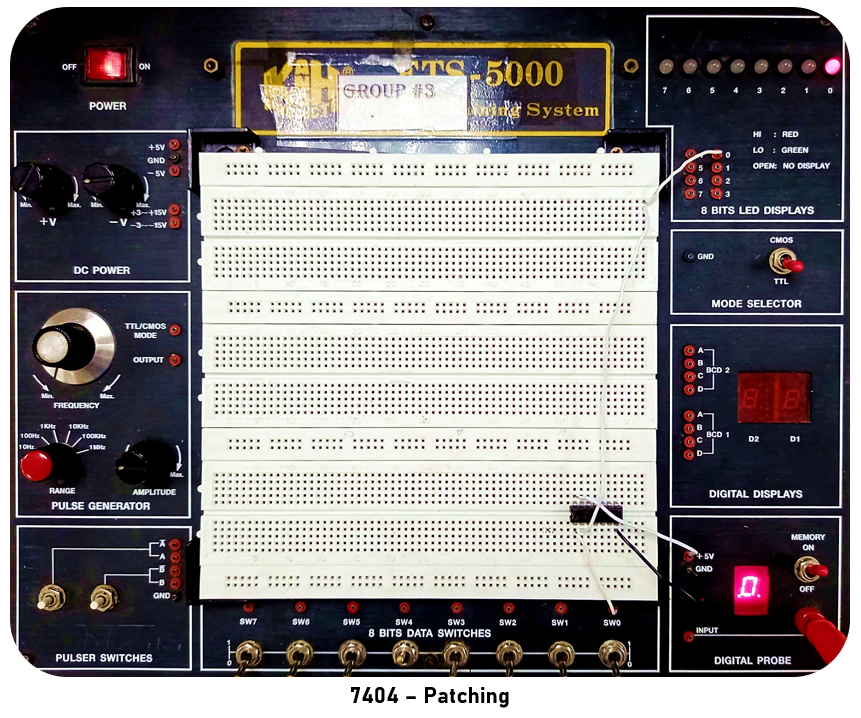
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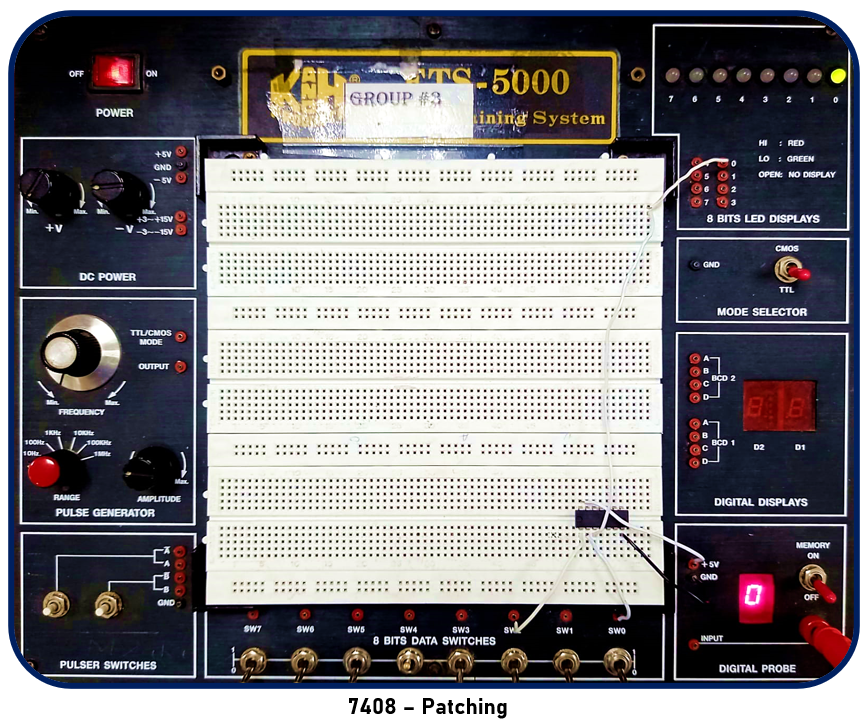
**AND Gate Simulation**

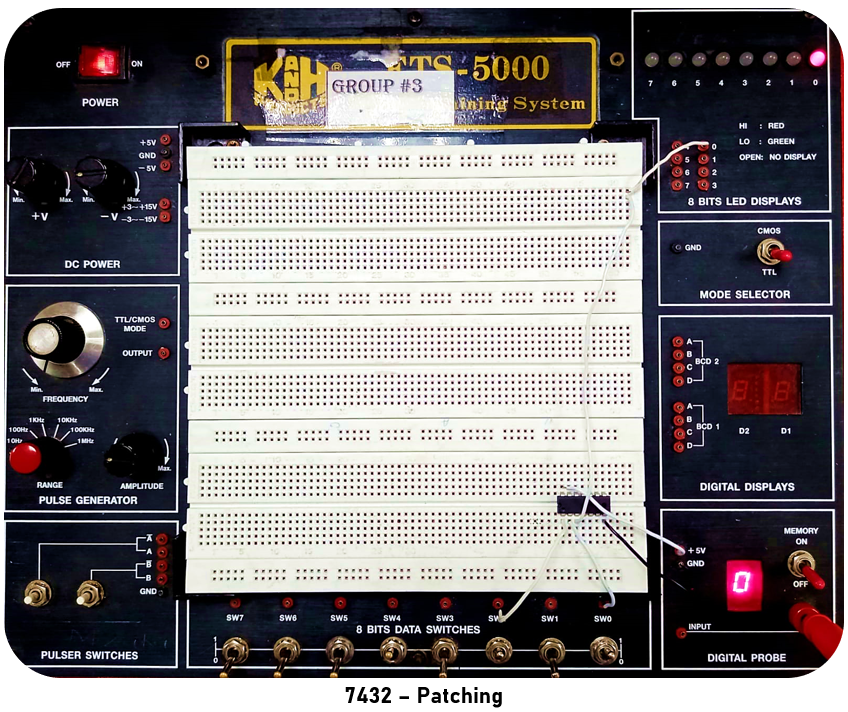
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**OR Gate Simulation**

**Hardware Implementation**



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After passing a series of inputs i.e., (0, 0), (0, 1), (1, 0), (1,1), to the above attached implementation of different ICs, we successfully verified their respective functioning through an LED output which has been further elaborated on further in the post – lab section.

**Circuit Description**

The circuit shown above is the most fundamental implementation of an IC and in-accordance with the schematic layout of the given ICs. Since we’re only concerned with the function of the logical gates, only a single input is needed for a 7404 (NOT) IC whereas two inputs are required for 7408 (AND) and 7432 (OR) ICs. The following section, post – lab, elaborates on the results of both our hardware implementation and proteus simulation essentially leading to the conclusion of our lab.

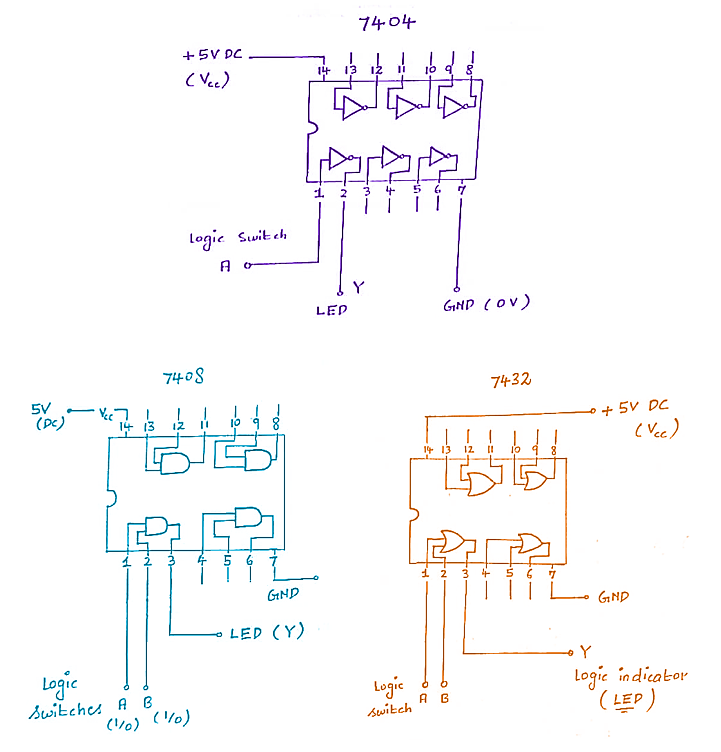
**Lab** (**5 Marks)**

Verify the functioning of the following ICs:

* 7408
* 7432
* 7404

**Procedure**

1. Make a **schematic layout diagram** in the space provided below, showing ICs pin numbers and their connections to form the logic circuit.



1. Plug in all ICs in bread board and power the ICs providing ground and VCC = 5V to appropriate pins. The ground pin is to be connected first and then any other connections are made.
2. By looking at pin configuration apply input signals from a switch on logic lab. Connect the output to LED for display. The operation of circuit is verified and results to be shown to teacher or Lab Asst. For trouble shooting of circuit use the logic probe provided in the lab.
3. Make the **truth tables** in the space provided below:

**7404**

|  |  |
| --- | --- |
| 0 | 1 |
| 1 | 0 |

**7408**

|  |  |  |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**7432**

|  |  |  |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

1. Mention the full name of each IC provided to you with the help of its datasheet and explain the naming convention (You should be able to get this information from internet).

**HD74LS04P**

|  |  |
| --- | --- |
| HD | Renesas Technology |
| 74 | Commercial Grade |
| LS | Low Power Schottky TTL |
| 04 | Hex Inverter Gates |
| P | DILP-14 |

**SN74HC32N**

|  |  |
| --- | --- |
| SN | Texas Instruments |
| 74 | Commercial Grade |
| HC | High Speed CMOS |
| 32 | Quad 2 – Input OR |
| N | PDIP-14 |

**SN74LS08N**

|  |  |
| --- | --- |
| SN | Texas Instruments |
| 74 | Commercial Grade |
| LS | Low Power Schottky TTL |
| 08 | Quad 2 – Input AND |
| N | PDIP-14 |

**Naming Convention**

*<Manufacturer> <Product line> <Generation> <Model No.> <Suffix>*

**Fill in the blanks**

1. *The ICs in 7400 series are based on* ***TTL*** *logic family?*
2. *The commercial grade IC is denoted by* ***74*** *prefix.*
3. *The military grade IC is denoted by* ***54*** *prefix.*

**Conclusions:**

Given ICs performed as they were designed to do so. Logic probe was used to ensure the circuit is patched correctly and that there is no floating ground error or other errors. Input was given in ascending order i.e., 0 0, 0 1, 1 0, 1 1.