



School of Electrical Engineering and Computer Science
National University of Sciences & Technology (NUST)

Home Assignment No-2[CLO1]

Subject: **Digital Logic Design**
Course: **BEE-12CD**
Teacher: **Engr. Arshad Nazir**

Marks: **50**
Issue: **12 Oct 2021**
Due: **27 Oct 2021**
(10:00 AM)

Note:

- ✓ Attempt the given problem set in a sequential order. Show all the design steps.
- ✓ Make an index showing summary of the problems solved with page numbers and also specify the missing ones.
- ✓ No late submissions will be accepted unless a prior approval from the teacher is obtained with extremely genuine reasons. The assignments submitted after the due date/time will be graded **zero**.
- ✓ University has zero tolerance for plagiarism and serious penalties apply. All assignments found mutually copied will be marked **zero**.
- ✓ The students will submit a certificate with the assignment work stating the originality of their efforts and no copying from others.
- ✓ **FIVE** marks are reserved for neat and clean work, table of contents, and certificate to be attached with the assignment work.

Problem No-1 Prove the identity of the following Boolean equations, using algebraic manipulation:-

- a. $(A \oplus B \oplus AB)(A \oplus C \oplus AC) = A + BC$
- b. $(A+B')(B+C')(C+D')(D+A') = (A'+B)(B'+C)(C'+D)(D'+A)$
(Use Consensus theorem only)

Problem No-2 Apply postulates and theorems of Boolean algebra to reduce the given function to the indicated number of literals:-

$$F(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + (A+D+E)' + B'C'D + B'C'E + B'D'E' + C'D'E'$$

to five literals

Problem No-3 Convert the given expressions into the forms indicated against each by algebraic manipulation:

- a. $f(w,x,y,z) = (w'+x)(y+z)(w'+y)(x+y'+z)$ (SOP)
- b. $F(A,B,C,D) = B(A'C'+AC) + D'(A+B'C)$ (POS)

Problem No-4 Write the simplified output Boolean expression Y for the circuit of Figure P4 and use it to determine the complete truth table. Then apply the waveform sketched below to the circuit inputs, and draw the resulting output waveform without gate delays.

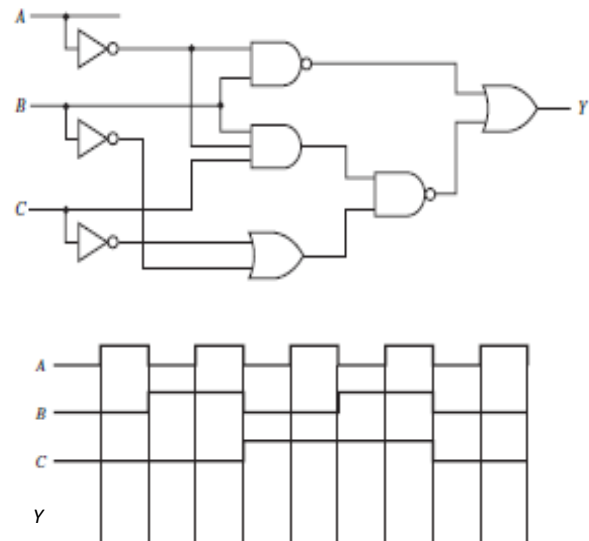


Figure P4 Logic Circuit and input waveforms

“Good Luck”