School of Electrical Engineering and Computer Science
National University of Sciences & Technology (NUST)

Home Assignment No-6[CLO3]

Subject:	**Digital Logic Design**	Marks:	**50**
Course:	**BEE-12CD**	Issue:	**24 Dec 2021**
Teacher:	**Engr. Arshad Nazir**	Due:	**31 Dec 2021**
Note:			*(11:00 AM)*

- ✓ *Attempt the given problem set in a sequential order. Show all the design steps.*
- ✓ *Make an index showing summary of the problems solved with page numbers and also specify the missing ones.*
- ✓ *No late submissions will be accepted unless a prior approval from the teacher is obtained with extremely genuine reasons. The assignments submitted after the due date/time will be graded **zero**.*
- ✓ *University has zero tolerance for plagiarism and serious penalties apply. All assignments found mutually copied will be marked **zero**.*
- ✓ *The students will submit a certificate with the assignment work stating the originality of their efforts and no copying from others.*
- ✓ *Five marks are reserved for neat and clean work, table of contents, and certificate to be attached with the assignment work.*

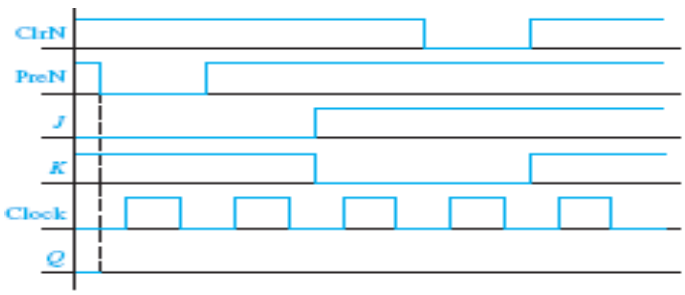
Problem No-1

a. Construct a negative edge-triggered D flip-flop using three-S-R latches. Draw the logic diagram and also list its function table. Add asynchronous active-low Preset and Reset inputs as direct inputs.

b. A certain flip-flop has four operations: Clear to 0, No change, Complement output, and Set to 1, when inputs M and N are 00, 01, 10, and 11, respectively:-

i. Tabulate the characteristics table
ii. Derive the characteristics equation
iii. List the excitation table
iv. Show how the flip-flop can be converted into a D flip-flop

c. Draw the state diagram and complete the following timing diagram for a JK flip-flop with a falling-edge trigger and asynchronous ClrN and PreN inputs.



Problem No-2 Design a clocked synchronous sequential circuit having a single input x and a single output z. The circuit is to produce an output of 1 whenever the previous three inputs and the current input correspond to the 4-bit binary number equivalents of decimal number 1, 6, 9, and 14 where the current input is considered the least significant of the 4-bit binary number. All other times the circuit is to produce 0 outputs. An example of the input/output sequences that satisfy the conditions of the circuit specifications is

x=0010100100010111010
z=0000000100010000100

a. Construct state diagram for the circuit.
b. Perform state reduction, if required.
c. Encode states using straight binary assignment and list the state transition table.
d. Derive the flip-flop input and output equations using J-K flip-flops.
e. Draw the resulting logic diagram of your design.

"**Good Luck"**