

# Chapter5-Synchronous Sequential Logic

## Lecture6- State Reduction and Assignment

# Objectives

- Study State Reduction using Row Matching and Implication Table Methods
- Make Binary State Assignments

# State Reduction and Assignment

- The **analysis** of sequential circuits starts from a circuit diagram and culminates in a state table or diagram whereas the **design** of a sequential circuit starts from a set of specifications and culminates in a logic diagram.
- State reduction is one of the important steps in the design of sequential circuits.
- The reduction of the number of flip flops is referred to as the **state reduction** problem.
  - Algorithms have been developed that aim at reducing the number of states in the state diagram, while keeping the external input-output requirements unchanged.
  - Since  $m$  flip flops produce  $2^m$  states, a reduction in the number of states may or may not result in a reduction in the number of flip flops.
  - An unpredictable effect in reducing the number of flip flops is that sometimes the equivalent circuit with fewer flip flops may require more combinational gates.

# State Reduction and Assignment Cont...

- There are two methods of state reduction:-
  - Row Matching (Row Elimination)
  - Implication Table (Pairs Chart)
- In the design procedure, initially states are labeled with alphabets and are subsequently assigned binary codes to derive expressions.

# State Reduction using Row-Elimination Method Example

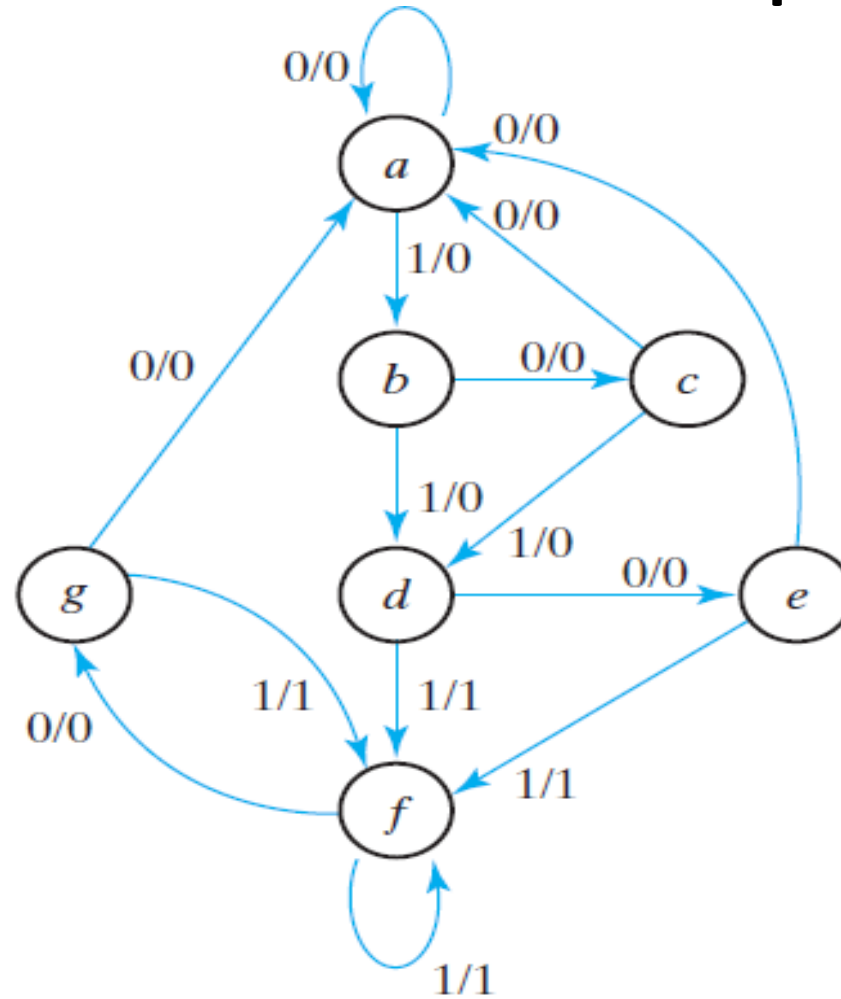


Fig. 5-22 State Diagram

Fall 2021

# State Reduction using Row-Elimination

## Method Example Cont...

- What we would like to find with our example is an equivalent FSM with fewer states that still generates the same output sequences for identical input sequences.
- It must be remembered that any two states are equivalent if for the same set of inputs, both produce the same outputs and are driven into the same next-states or equivalent states.
- The problem of state reduction is to find ways of reducing the number of states in a sequential circuit without altering the input-output relationships.
- Let the given input sequence be 01010110100...
- We can describe the behavior of given sequential circuit by listing input-output sequence as shown below:-

State	a	a	b	c	d	e	f	f	g	f	g	a
Input	0	1	0	1	0	1	1	0	1	0	0	
Output	0	0	0	0	0	1	1	0	1	0	0	

# State Reduction using Row-Elimination Method Example Cont...

- From the given state diagram of Mealy FSM, we can list State Table as shown below:-

Present State		Next State			Output	
		x = 0	x = 1		x = 0	x = 1
a		a	b		0	0
b		c	d		0	0
c		a	d		0	0
d		e	f		0	1
e		a	f		0	1
f		g	f		0	1
g		a	f		0	1

# State Reduction using Row-Elimination Method Example Cont...

- Two states are said to be equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state.
  - When two states are equivalent, one of them can be removed without altering the input-output relationships.
- In our example, we look for two present states that go to the same next state and have the same output for both input combinations.
  - States **g** and **e** are examples, so **g** can be eliminated and substituted with **e** in the leftover state table. This results in one row representing state g struck/eliminated in the state table.
  - This state equivalency steps will continued till all non-equivalent states are left. The resulting state tables are shown next.



# State Reduction using Row-Elimination Method Example Cont...

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

→

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

$e \equiv g$  &  $d \equiv f$

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

# State Reduction using Row-Elimination Method Example Cont...

- From reduced state table we can draw state diagram with fewer states as shown below:-

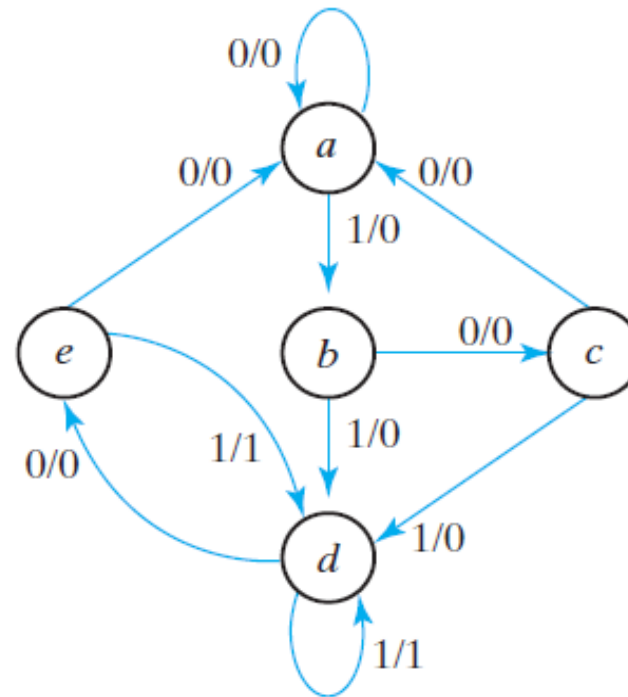


Fig. 5-23 Reduced State Diagram

# State Reduction using Row-Elimination

## Method Example Cont...

- We can once again evaluate the circuit behavior with the same input i.e 01010110100...
- The input out-put sequence after state reduction is listed below:-

State	a	a	b	c	d	e	d	d	e	d	e	a
Input	0	1	0	1	0	1	1	0	1	0	0	
Output	0	0	0	0	0	1	1	0	1	0	0	

- Input-output sequence comparison of both circuits reveals that they are equivalent.

# State Reduction using Implication Table

## Method Example

- We can also use **Implication Table** (sometimes referred to as a “**pairs chart**”) to check each pair of states for possible equivalence. The non-equivalent pairs are systematically eliminated until only the equivalent pairs remain.
- Implication tables provide graphic method of identifying redundant states and use grid array to list the possible state equivalencies.
- After equivalent states are found, we can apply row-matching reduction algorithm to eliminate states. This method is more reliable because using this method we can find equivalency of those states whose next-states are not same but equivalent.
- If desired, row matching method can be used to partially reduce the state table before constructing implication table.

# State Reduction using Implication Table

## Method Example Cont...

The diagram illustrates the structure of an implication table for state reduction. It consists of a grid of cells arranged in a staircase pattern. The rows are labeled on the left as  $q_2$ ,  $q_3$ , followed by three vertical dots, then  $q_{n-2}$ ,  $q_{n-1}$ , and  $q_n$ . The columns are labeled at the bottom as  $q_1$ ,  $q_2$ ,  $q_3$ , followed by three horizontal dots, then  $q_{n-2}$  and  $q_{n-1}$ . The cells are arranged such that the first row has one cell under  $q_1$ ; the second row has two cells under  $q_1$  and  $q_2$ ; the third row has three cells under  $q_1$ ,  $q_2$ , and  $q_3$ ; the fourth row has four cells under  $q_1$ ,  $q_2$ ,  $q_3$ , and  $q_{n-2}$ ; the fifth row has five cells under  $q_1$ ,  $q_2$ ,  $q_3$ ,  $q_{n-2}$ , and  $q_{n-1}$ ; and the sixth row has six cells under  $q_1$ ,  $q_2$ ,  $q_3$ ,  $q_{n-2}$ ,  $q_{n-1}$ , and an additional unlabeled column.

Figure: Structure of Implication Table

# State Reduction using Implication Table

## Method Example Cont...

- We will use the example of state table shown below to illustrate the implication table method:-

Present State	Next State		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
A	A	B	0	0
B	D	C	0	1
C	F	E	0	0
D	D	F	0	0
E	B	G	0	0
F	G	C	0	1
G	A	F	0	0

# State Reduction using Implication Table

## Method Example Cont...

- Construct implication table of the form as shown in the next slide. This chart has a square for every possible pair of states. A square in column  $i$  and row  $j$  corresponds to state pair  $i-j$ . Thus the squares in the first column correspond to state pairs A-B, A-C etc.
- $A \equiv B$ : iff  $A \equiv D$ ,  $B \equiv C$  & outputs are same. As outputs of A and B are different so these states are not equivalent and we inset a cross in the square A-B. Likewise we compare each state with all other states.
- Note that the squares above the diagonal are not included in the chart. Why? How do you interpret crosses in some squares?
- After the implication table has been constructed and some of the non-equivalent states found shown with crosses due to different outputs, go for first pass. The Implication Table after First and second passes will be as shown in the next slide.
- Another pass will result in no further elimination of non-equivalent states. The squares not crossed represent equivalent states i.e  $A \equiv D \equiv G$  and  $B \equiv F$ .

# State Reduction using Implication Table Method Example Cont...

B	$\times$					
C	A, F B, E	$\times$				
D	B, F	$\times$	D, F E, F			
E	A, B B, G	$\times$	B, F E, G	B, D F, G		
F	$\times$	D, G	$\times$	$\times$	$\times$	
G	B, F	$\times$	A, F E, F	A, D	A, B F, G	$\times$
	A	B	C	D	E	F

(a)

B	$\times$					
C	<del>A, F</del> <del>B, E</del>	$\times$				
D	B, F	$\times$	<del>D, F</del> <del>E, F</del>			
E	<del>A, B</del> <del>B, G</del>	$\times$	B, F E, G	<del>B, D</del> <del>F, G</del>		
F	$\times$	D, G	$\times$	$\times$	$\times$	
G	B, F	$\times$	<del>A, F</del> <del>E, F</del>	A, D	<del>A, B</del> <del>F, G</del>	$\times$
	A	B	C	D	E	F

(b)

B	$\times$					
C	<del>A, F</del> <del>B, E</del>	$\times$				
D	B, F	$\times$	<del>D, F</del> <del>E, F</del>			
E	<del>A, B</del> <del>B, G</del>	$\times$	<del>B, F</del> <del>E, G</del>	<del>B, D</del> <del>F, G</del>		
F	$\times$	D, G	$\times$	$\times$	$\times$	
G	B, F	$\times$	<del>A, F</del> <del>E, F</del>	A, D	<del>A, B</del> <del>F, G</del>	$\times$
	A	B	C	D	E	F

(c)

The initial Table

After the first pass

After the second pass



# State Reduction using Implication Table

## Method Example

- Now we can use row elimination to reduce the state table .

Present State	Next State	Output (z)
	Input (x) 0 1	Input (x) 0 1
A	A B	0 0
B	<del>D</del> <sup>A</sup> C	0 1
C	<del>F</del> <sup>B</sup> E	0 0
D	D F	0 0
E	B <del>G</del> <sup>A</sup>	0 0
F	<del>G</del> <sup>A</sup> C	0 1
G	A F	0 0

Present State	Next State	Output (z)
	Input (x) 0 1	Input (x) 0 1
A	A B	0 0
B	A C	0 1
C	B E	0 0
E	B A	0 0

# State Assignment

- In order to design a sequential circuit with physical components, it is necessary to assign coded binary values to the states.
  - For a circuit with  $m$  states, the codes must contain  $n$  bits where  $2^n \geq m$
  - In our example,
    - The unreduced table requires assignment of 7 states
    - The reduced table requires assignment of 5 states
- Binary assignment made in both cases requires three flip-flops with one and three unused states respectively.
- Unused states of a combination of binary values become our don't care conditions which normally leads to a reduction in the number of gates used for implementation.

# State Assignment Cont...

- Many different assignments can be made to reduced states. The simplest way to code small state sets is to use the first five integers in binary counting order
- Another similar assignment is to use the Gray code
- Another possible assignment is the one-hot

State	Assignment 1 Binary	Assignment 2 Gray Code	Assignment 3 One-hot
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

# Reduced State Table with Binary Assignment

- The binary form of the state table is used to derive the combinational circuit part of the sequential circuit.

Present State		Next State			Output	
		x = 0	x = 1		x = 0	x = 1
000		000	001		0	0
001		010	011		0	0
010		000	011		0	0
011		100	011		0	1
100		000	011		0	1

# The End