



Upgrade



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Explanations / Fundamentals of Logic Design

Exercise 20



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Fundamentals of Logic Design
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Explanation Verified

Step 1**Next-state equations**

We note that there are two K flip-flops with outputs Q_1 and Q_2 , thus the states of the machine are the bit strings of length 2.

$$\begin{aligned}
 J_1 &= [(XQ_2)'(Q_2X')']' \\
 &= [(X' + Q_2)(Q_2' + X)]' && \text{DeMorgan's law} \\
 &= XQ_2' + Q_2X' && \text{DeMorgan's law} \\
 K_1 &= [(Q_2X')']' \\
 &= Q_2X' && \text{Involution law} \\
 J_2 &= (X' + Q_1)' \\
 &= XQ_1' && \text{DeMorgan's law} \\
 K_2 &= J_2 = XQ_1' \\
 Z &= (Q_1' + Q_2')' \\
 &= Q_1Q_2 && \text{DeMorgan's law}
 \end{aligned}$$

The next-state equation for a J-K flip-flop is $Q^+ = JQ' + K'Q$.

$$\begin{aligned}
 Q_1^+ &= J_1Q_1' + K_1'Q_1 \\
 &= XQ_1'Q_2' + X'Q_1'Q_2 + (Q_2X')'Q_1 \\
 &= XQ_1'Q_2' + X'Q_1'Q_2 + (Q_2' + X)Q_1 && \text{DeMorgan's law} \\
 &= XQ_1'Q_2' + X'Q_1'Q_2 + Q_1Q_2' + Q_1X && \text{Distributive law} \\
 Q_2^+ &= J_2Q_2' + K_2'Q_2 \\
 &= XQ_1'Q_2' + (XQ_1')'Q_2 \\
 &= XQ_1'Q_2' + (X' + Q_1)Q_2 && \text{DeMorgan's law} \\
 &= XQ_1'Q_2' + X'Q_2 + Q_1Q_2 && \text{Distributive law}
 \end{aligned}$$

Step 2**Transition table**

Let us use the next-state equations to determine the next state based on the current state and the input X .

Similarly, we will use the output equation to determine the output corresponding to each current state.

	Present state Q_1Q_2	Next state $Q_1^+Q_2^+$		Z
		$X = 0$	$X = 1$	
S_0	00	00	11	0
S_1	01	11	00	0
S_2	10	10	10	0
S_3	11	01	11	1

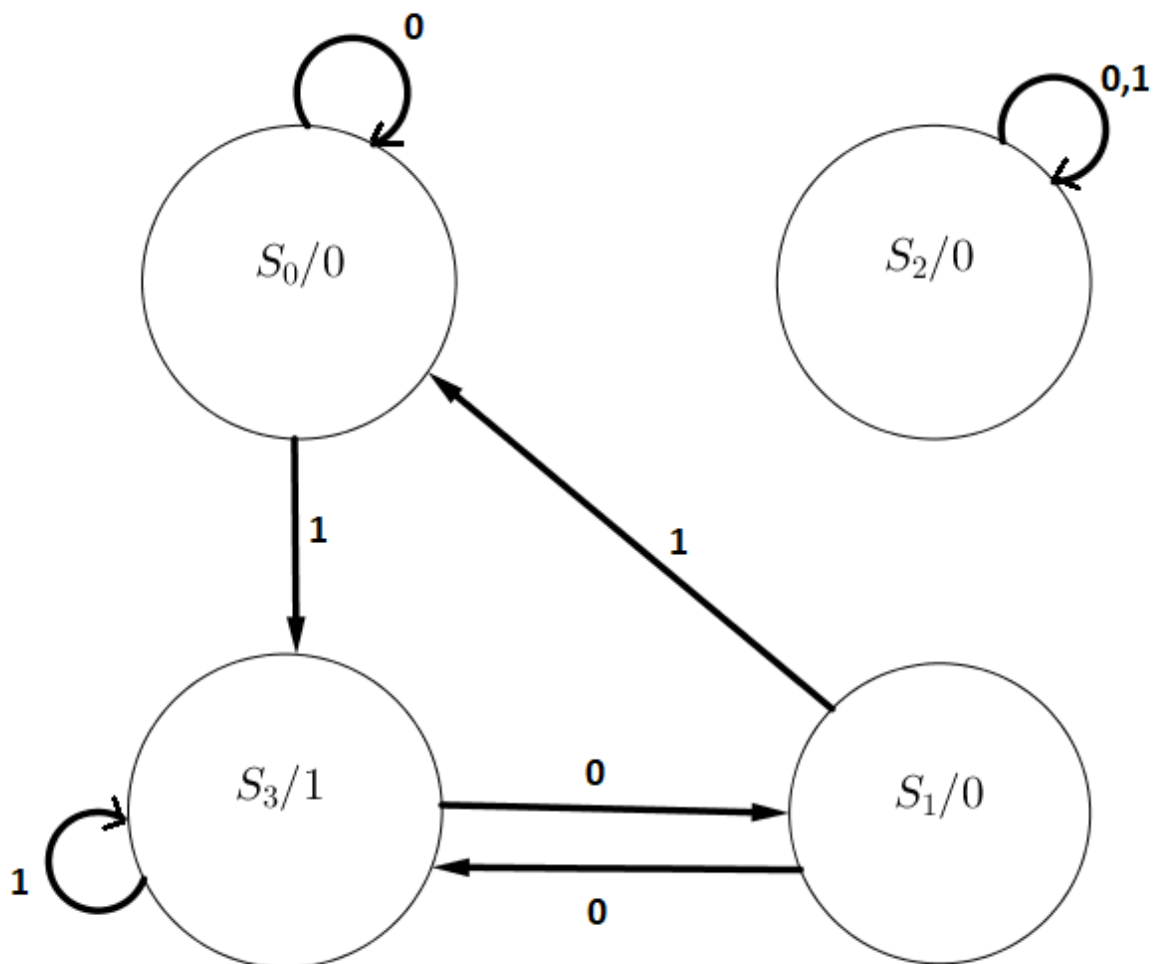
Step 3

State graph

There are four states S_0 to S_3 mentioned in the present state column, thus we need to draw four states.

When the output b is mentioned in the row starting with S_i , then we mention S_i/b in the corresponding state.

When the state S_j is mentioned in the row starting with S_i and in the next-state column with input $X = a$, then we draw an arc from state S_i to state S_j and label the arc with a .

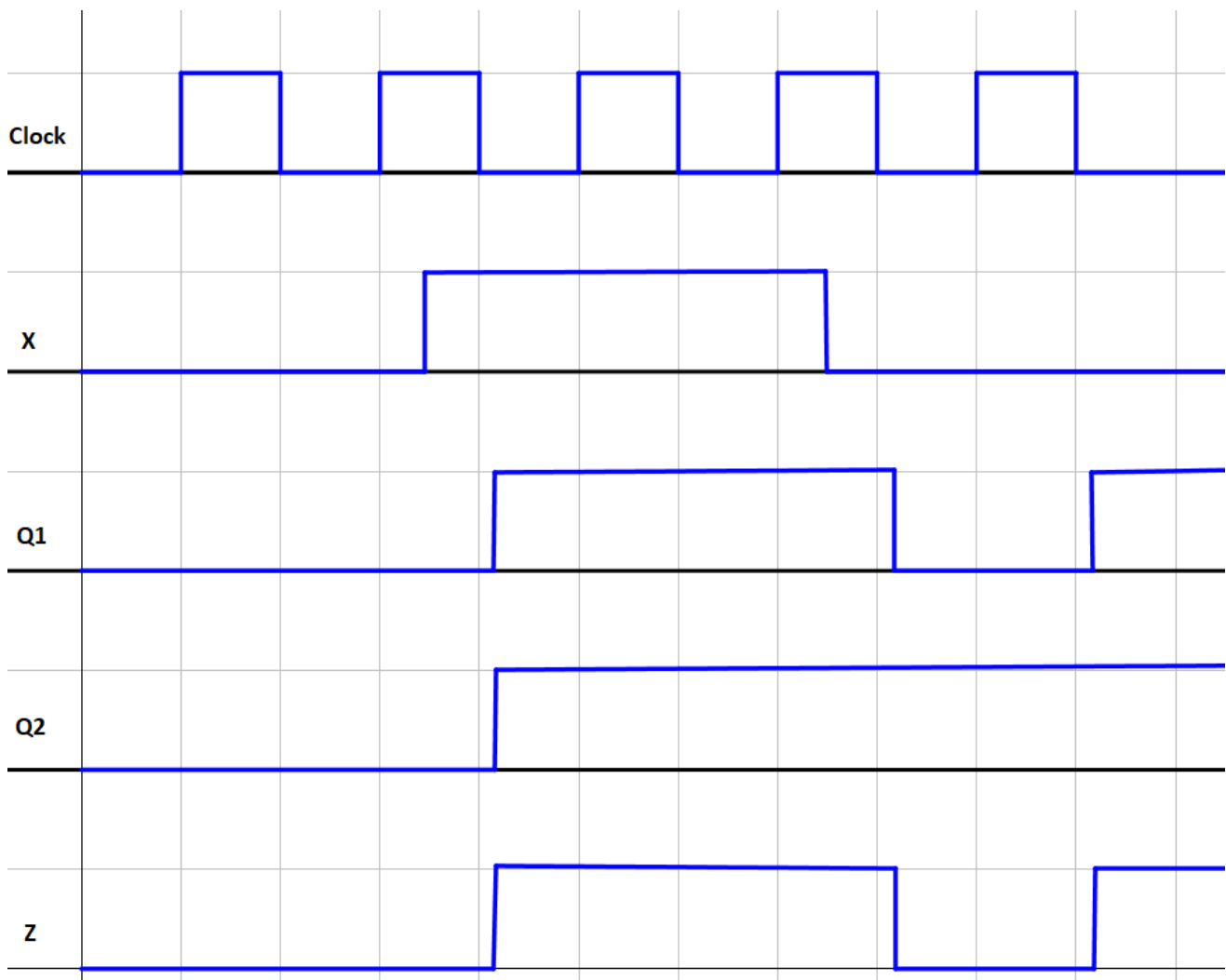


Step 4**(b) Timing diagram**

We know that the input X is 01100, while any changes in X need to occur in the middle between rising and falling clock edges.

We assume that the initial state is $Q_1Q_2 = 00$.

Since the clock is inverted, any changes in the states Q_1 , Q_2 , and Z will occur right after the falling edge of the clock. Moreover, the next-states and output can be found in the transition table.



Step 5

(c)

$$X = 01100$$

Output sequence

Since $Q_1 = Q_2 = 0$ initially, we start at state S_0 .

The first input is $X = 0$ and the present state is S_0 , thus we remain at state S_0 with output $Z = 0$.

$$Z = 0$$

The second input is $X = 1$ and the present state is S_0 , thus we move to state S_3 with output $Z = 1$.

$$Z = 1$$

The third input is $X = 1$ and the present state is S_3 , thus we remain at state S_3 with output $Z = 1$.

$$Z = 1$$

The fourth input is $X = 0$ and the present state is S_3 , thus we move to state S_1 with output $Z = 0$.

$$Z = 0$$

The fifth input is $X = 0$ and the present state is S_1 , thus we move to state S_3 with output $Z = 1$.

$$Z = 1$$

Thus we then note that the output sequence is $Z = 01101$.

Result

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(a)

	Present state Q_1Q_2	Next state $Q_1^+Q_2^+$		Z
		$X = 0$	$X = 1$	
S_0	00	00	11	0
S_1	01	11	00	0
S_2	10	10	10	0
S_3	11	01	11	1

(b) No false outputs

(c) $Z = 01101$ [< Exercise 19](#)[Exercise 21 >](#)