**Department of Electrical Engineering**

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**Semester: 1st Section: BEE-12C **

**EE-111: Linear Circuit Analysis**

**Lab 3: Verification of KVL,KCL, Voltage & Current Divider Rule**

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| **PLO4/CLO4** | | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |
| **Name** | **Reg. No** | **Viva /Quiz / Lab Performance**  **5 marks** | **Analysis of data in Lab Report**  **5 marks** | **Modern Tool Usage**  **5 marks** | **Ethics and Safety**  **5 marks** | **Individual and Team Work**  **5 marks** |
| **Muhammad Umer** | **345834** |  |  |  |  |  |
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**Lab 3: Verification of KVL, KCL, Voltage & Current Divider Rule**

1. **Introduction**

Humans strive to be efficient, same is the case with engineers. Being able to save up bits of time using shortcuts is always a viable and preferred option. This lab will make aspiring engineers to be able to prove that VDR and CDR do, indeed, comply with the simulated values. Any discrepancy in measured and theoretical values is subject to evaluation.

1. **Objective**

After performing this lab, students will be able to:

* Make series and parallel circuits on breadboard.
* Use the Multimeter as Ammeter or Voltmeter to measure the Currents and Voltage respectively.
* Explain any discrepancy in the obtained results.

1. **Lab Equipment**

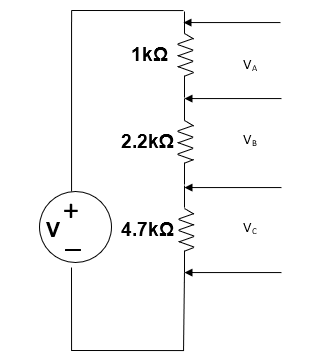
The following equipment would be used in this experiment:

* Test Bench
* The Multimeter
* The Power Supply
* Digital Multimeter

1. **Tasks:**

* **KVL**

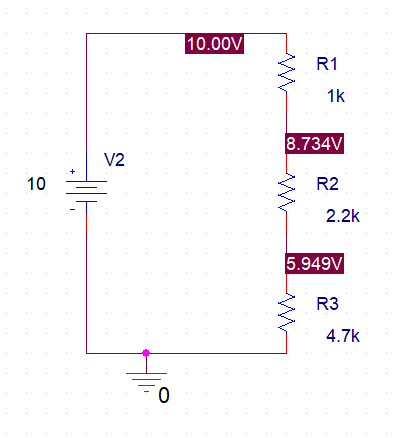
To verify KVL and VDR, we connect three different resistors in series with a voltage source and alter it’s value in steps.

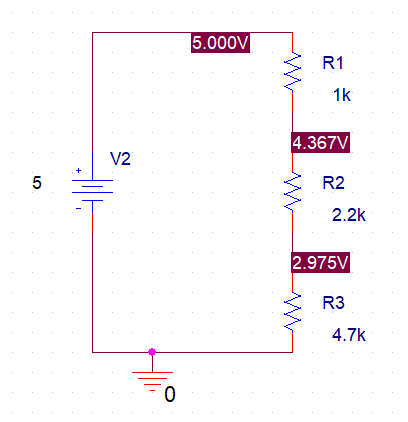
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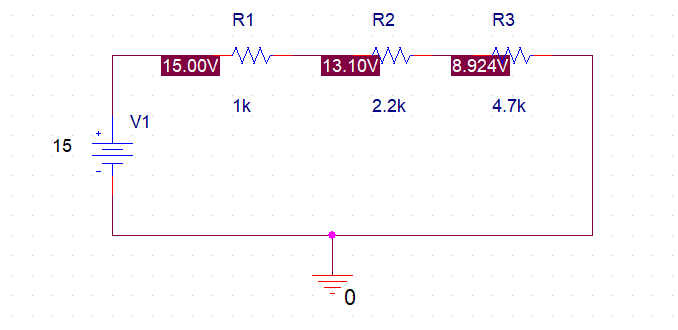
**Base Circuit**

**Table – 1 (KVL) Simulated values**

Making the circuit on PSpice, we get the simulated voltages across each node. The difference between adjacent voltages is the voltage across the resistors between them.







|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No** | **Applied Voltage** | **VA :Voltage at A** | **VB: Voltage at B** | **VC:Voltage at C** | **VT= VA + VB + VC** |
| **1** | **5V** | 0.63 | 1.39 | 2.97 | 5 |
| **2** | **10V** | 1.26 | 2.78 | 5.94 | 10 |
| **3** | **15V** | 1.89 | 4.17 | 8.92 | 15 |

**Table – 2 (KVL) Measured values**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No** | **Applied Voltage** | **VA :Voltage at A** | **VB: Voltage at B** | **VC:Voltage at C** | **VT= VA + VB + VC** |
| **1** | **5V** | 0.62 | 1.34 | 2.95 | 4.91 |
| **2** | **10V** | 1.25 | 2.77 | 5.92 | 9.94 |
| **3** | **15V** | 1.88 | 4.12 | 8.97 | 14.97 |

**Table – 3 (KVL) Calculated values**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No** | **Applied Voltage** | **VA :Voltage at A** | **VB: Voltage at B** | **VC:Voltage at C** | **VT= VA + VB + VC** |
| **1** | **5V** | 0.63 | 1.39 | 2.97 | 5 |
| **2** | **10V** | 1.26 | 2.78 | 5.94 | 10 |
| **3** | **15V** | 1.89 | 4.17 | 8.92 | 15 |

**Table –4 (VDR)**

**For (Vapplied1)**

**S.No Resistances Ratios Calculated voltages Measured Voltages**

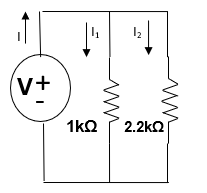
1 *=* 0.63 *VA : Voltage at A=* 0.63

2 *=* 1.39 *VB : Voltage at B=* 1.39

30.59 *=* 2.97 *VC :Voltage at C=* 2.97

* **KCL**

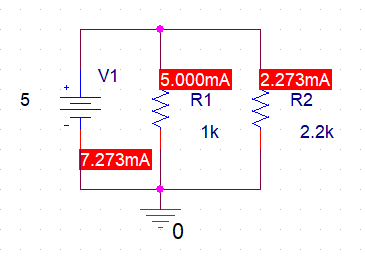
To verify KCL and CDR, we connect two different resistors in parallel with a voltage source and alter it’s value in steps.

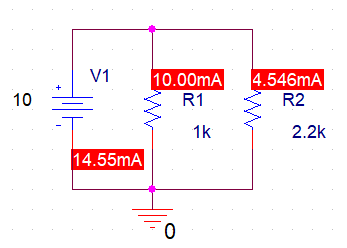


**Base Circuit**

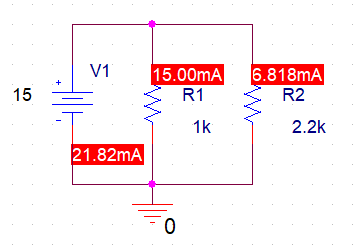
**Table –5 (KCL) Simulated values**

Making the circuit on PSpice, we get the simulated current through each resistor. We step up the source by 5, thrice, to check the validity of CDR.

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **S.No** | **Applied Voltage** | **Current: I**  **(measured)** | **Current: I1**  **(measured)** | **Current: I2**  **(measured)** | **I= I1 + I2**  **(Calculated)** |  |
| **1** | 5V | 7.27mA | 5.00mA | 2.27mA | 7.27mA | 0.6875 |
| **2** | 10V | 14.55mA | 10.00mA | 4.54 mA | 14.55mA | 0.6875 |
| **3** | 15V | 21.82mA | 15.00mA | 6.81 mA | 21.82mA | 0.6875 |

**Table –6 (KCL) Measured values**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **S.No** | **Applied Voltage** | **Current: I**  **(measured)** | **Current: I1**  **(measured)** | **Current: I2**  **(measured)** | **I= I1 + I2**  **(Calculated)** |  |
| **1** | 5V | 7.11mA | 4.74mA | 2.18mA | 6.92mA | 0.6875 |
| **2** | 10V | 14.3 mA | 9.84 mA | 4.36 mA | 14.2mA | 0.6875 |
| **3** | 15V | 21.78 mA | 14.89 mA | 6.85 mA | 21.74 mA | 0.6875 |

**Table –7 (KCL) Calculated Values**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **S.No** | **Applied Voltage** | **Current: I**  **(measured)** | **Current: I1**  **(measured)** | **Current: I2**  **(measured)** | **I= I1 + I2**  **(Calculated)** |  |
| **1** | 5V | 7.27mA | 5.00mA | 2.27mA | 7.27mA | 0.6875 |
| **2** | 10V | 14.55mA | 10.00mA | 4.54 mA | 14.55mA | 0.6875 |
| **3** | 15V | 21.82mA | 15.00mA | 6.81 mA | 21.82mA | 0.6875 |

**Table –8 (CDR)**

**For (Vapplied1)**

**S.No Resistances Ratios Calculated Current Measured Current**

1 = 0.6875 = 5mA I1: Current of Branch 1= 5.00mA

2 = 0.3125 = 2.27mA I2: Current of Branch 2= 2.27mA

1. **Conclusion:**

I can firmly state that I’ve learnt how to apply CDR and VDR on either platform, be it breadboard, PSpice or on paper. The above states set specific rules also help us get familiar with the basics of circuit analysis as to what is the behaviour of the base components of a circuit i.e, Voltage dividing in series, Current dividing in parallel.