**Department of Electrical Engineering**

**Faculty Member:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Dated: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Semester:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

*Group No.:*

**EE-221: Digital Logic Design**

**Assessment Rubrics for Lab 10: Voting Machine**

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|  |  | **PLO4/CLO4** | **PLO4/CLO4** | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |  |
| **Name** | **Reg. No** | **Viva / Lab Performance** | **Analysis of data in Lab Report** | **Modern Tool Usage** | **Ethics and Safety** | **Individual and Team Work** | **Total marks Obtained** |
|  |  | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **25 Marks** |
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## Lab10: Voting Machine

This Lab experiment has been designed to familiarize the students with use of **multiplexers** to implement a Boolean function and use **BCD-to-Seven-Segment Decoder** to drive the 7-segment Display. This lab requires some knowledge of SSI/MSI combinational circuits like Multiplexers, decoders, and Numeric Read-out Display.

**Objectives**

* Understand the function of Multiplexers and their uses in implementing a given Boolean function.
* Familiarization with BCD-to-Seven-Segment Decoder IC as a driver to drive Numeric Read-out.
* Transform any problem statement to truth table description, and choose output functions that need Multiplexers implementation or other simplification techniques using logic gates.
* Design and verify combinational circuit design.

**Lab Instructions**

* This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
* The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
* The students will start lab task and demonstrate design steps separately for step-wise evaluation( course instructor/lab engineer will sign each step after ascertaining functional verification)
* Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
* After the lab, students are expected to unwire the circuit and deposit back components before leaving.
* The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
* There are related questions at the end of this activity. Give complete answers.

**A. Pre-Lab Tasks 5 marks**

1. Draw the Logic Diagram for a 4 to 1 MUX and also give its Truth Table and Block Diagram Representation.

2. For implementing a Boolean function of n variables, a MUX with how many Selection Lines and Inputs are needed?

3. For implementing the Function F(x,y,z)=∑(1,2,6,7), a MUX with how many selection lines is needed?

4. Implement the above function (Draw its Logic Diagram) F with the MUX suggested in answer to above question.

**B. Lab Task 5 marks (complete the paper work before coming to the lab)**

Voting Machine Problem:

A small corporation has 9 shares of stock. The corporation board consists of 4 members (A Chairman, 2 senior members and 1 junior member).Each member of the Corporation Board has a voting right at a Corporation Financial meeting. The committee has agreed to assign the following share(s) to vote of each member.

Chairman : 4 shares

# Senior Member : 2shares

# Senior Member : 2 shares

# Junior Member : 1 shares

The Committee wants to automate the voting process and get a voting machine that gets input from each member and then display the total number of shares. Each of these persons has a switch to close when voting yes (Logic 1) and to open when voting No (Logic 0) for his share.

You are a Design Engineer in the same corporation and have been asked to design such a voting machine. The only ICs available to you are two 8x1 multiplexers a 3-input NAND gates and a 7-Segment Decoder IC and a 7segemt LED Display.

5. Draw a simplified Block Diagram of such a voting machine (You do not need to make exact Logic Diagram).

6. There are four inputs to this machine (one for each member) and the output is a binary number (4-bit). Draw the truth table for the Output Function.

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| **Input** | | | | **Output** | | | |
| W(4) | X(2) | Y(2) | Z(1) | A | B | C | D |
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7. You are provided with two 8- to-1 MUXs, so how many functions can you implement with them?

8. Which of the above functions would you implement with MUX? Specify and also give their Logic Diagram using MUX.

9. Give the PIN Configuration of the 8-to-1 MUX provided to you in the lab.

10. Give the Boolean expressions for the remaining two functions and also give their Logic Diagram (You can only use 3-input NAND Gate).

11. The 4 outputs ABCD are in binary (BCD), so we will have to use a BCD to 7-segment Decoder to drive the 7-segment LED Display. Look for the BCD to 7-segment Decoder IC in the lab and give its number and PIN Configuration. Look up on internet for the data sheet of this IC.

12. Draw the truth table for the above IC.

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| **Inputs** | | | | Outputs | | | | | | |
| A | B | C | D | a | b | c | d | e | f | g |
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13. After selecting the decoder IC you need a 7-Segment LED Display. It comes in two configurations Common Anode and Common Cathode. Differentiate between them by drawing their Circuit Configuration (Showing their connection to ground and power supply and logic level of inputs for each).

14. What configuration have you decided to choose and why?

15. If you were to choose the other configuration of 7-Segment Display what change would you need in your circuit?

16. Show your complete circuit in working condition after completing the **Logic Diagram** for the whole voting Machine System mentioning the ICs name and Configuration and implement it in hardware.