**Department of Electrical Engineering**

**Faculty Member:** Arshad Nazir **Dated:** 17/12/2021

**Semester:** 3rd **Section:** BEE 12C

**Group No.: 7**

**EE-221: Digital Logic Design**

Lab 13: Sequence Detector

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|  |  | **PLO4/CLO4** | **PLO4/CLO4** | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |  |
| **Name** | **Reg. No** | **Viva / Lab Performance** | **Analysis of data in Lab Report** | **Modern Tool Usage** | **Ethics and Safety** | **Individual and Teamwork** | **Total marks Obtained** |
|  |  | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **25 Marks** |
| **Muhammad Adil Azeem** | **342459** |  |  |  |  |  |  |
| **Muhammad Umer** | **345834** |  |  |  |  |  |  |
| **Raahim Ahmad Waqar** | **342287** |  |  |  |  |  |  |
| **Saad Bakhtiar** | **341150** |  |  |  |  |  |  |
| **Syed Aun Ali Kazmi** | **342384** |  |  |  |  |  |  |

## Lab 13: Sequence Detector

This Lab Activity has been designed to familiarize the students with design and implementation of a sequence detector from an incoming binary stream received serially. The students are expected to do the following:

**Objectives:**

* Complete the Sequential Design Method
* Design the circuit using D Flip-Flops.
* The students are required to complete Pre-Lab work before coming to the lab and submit lab report before leaving

**Lab Instructions**

* This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
* The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation. Alternately each group to upload completed lab report on LMS for grading.
* The students will start lab task and demonstrate design steps separately for stepwise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
* Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
* After the lab, students are expected to unwire the circuit and deposit back components before leaving.
* The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
* **The Total duration for the lab is 3 hrs. After lab duration, a deduction of 5 marks per day will be done for late submission.**
* **A lab with in-complete lab tasks will not be accepted.**
* There are related questions at the end of this activity. Give complete answers.

**Pre – Lab Tasks**

**Pre – Lab Task 1**

**We wish to design a circuit with single input x, and a single output z, that detects three or more consecutive 1’s in a string of bits coming through an input line. We start it in the initial state S0. In our design, the detector circuit will only advance to the next state if some valid bit of the specified sequence is received otherwise will go back to either S0 or any other state depending upon whether sequence breaks totally or partially. As and when any of the two sequences is received completely, the detector circuit will output 1.**

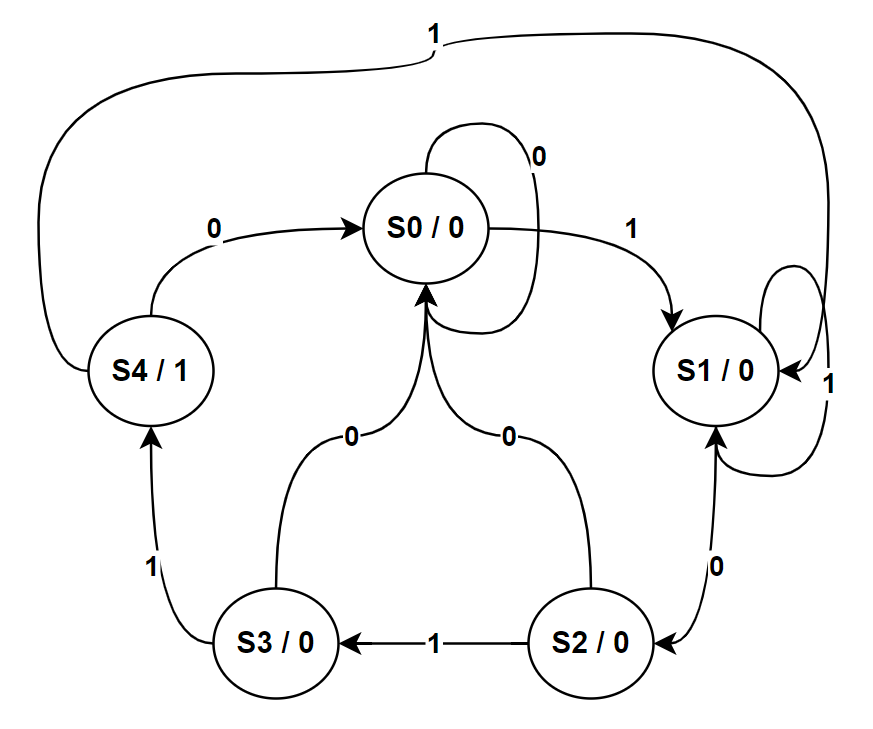
**There are two FSM models for each design. Name these models and give advantages/ disadvantages of each? Which method you prefer and why?**

The two types of models that can tackle this problem are Moore FSM and Mealy FSM. Mealy Models are less stable but can be implemented using a lesser number of flip flops whereas Moore Models are more stable but at the cost of more states and hence, a greater number of flip flops.

For the purpose of this lab, we have preferred to go with Moore as it is more stable because the output does not change upon a sudden change in the input.

**Pre – Lab Task 2**

**Draw the Moore state diagram for the sequence detector. How many D Flip-Flops would you need for implementing the sequence detector and why?**



We would require 3 D – Flip Flops as there are five possible states.

**Pre – Lab Task 3**

**List the State Transition Table.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Present State** | | | **Input** | **Next State** | | | **Output** |
| **QA** | **QB** | **QC** | **X** | **QA+** | **QB+** | **QC+** | **Y** |
| 0 | 0 | 0 | **0** | **0** | **0** | **0** | **0** |
| 0 | 0 | 0 | **1** | **0** | **0** | **1** | **0** |
| 0 | 0 | 1 | **0** | **0** | **1** | **0** | **0** |
| 0 | 0 | 1 | **1** | **0** | **0** | **1** | **0** |
| 0 | 1 | 0 | **0** | **0** | **0** | **0** | **0** |
| 0 | 1 | 0 | **1** | **0** | **1** | **1** | **0** |
| 0 | 1 | 1 | **0** | **0** | **0** | **0** | **0** |
| 0 | 1 | 1 | **1** | **1** | **0** | **0** | **0** |
| 1 | 0 | 0 | **0** | **0** | **0** | **0** | **1** |
| 1 | 0 | 0 | **1** | **0** | **0** | **1** | **1** |
| 1 | 0 | 1 | **0** | X | | | |
| 1 | 0 | 1 | **1** |
| 1 | 1 | 0 | **0** |
| 1 | 1 | 0 | **1** |
| 1 | 1 | 1 | **0** |
| 1 | 1 | 1 | **1** |

**Pre – Lab Task 4**

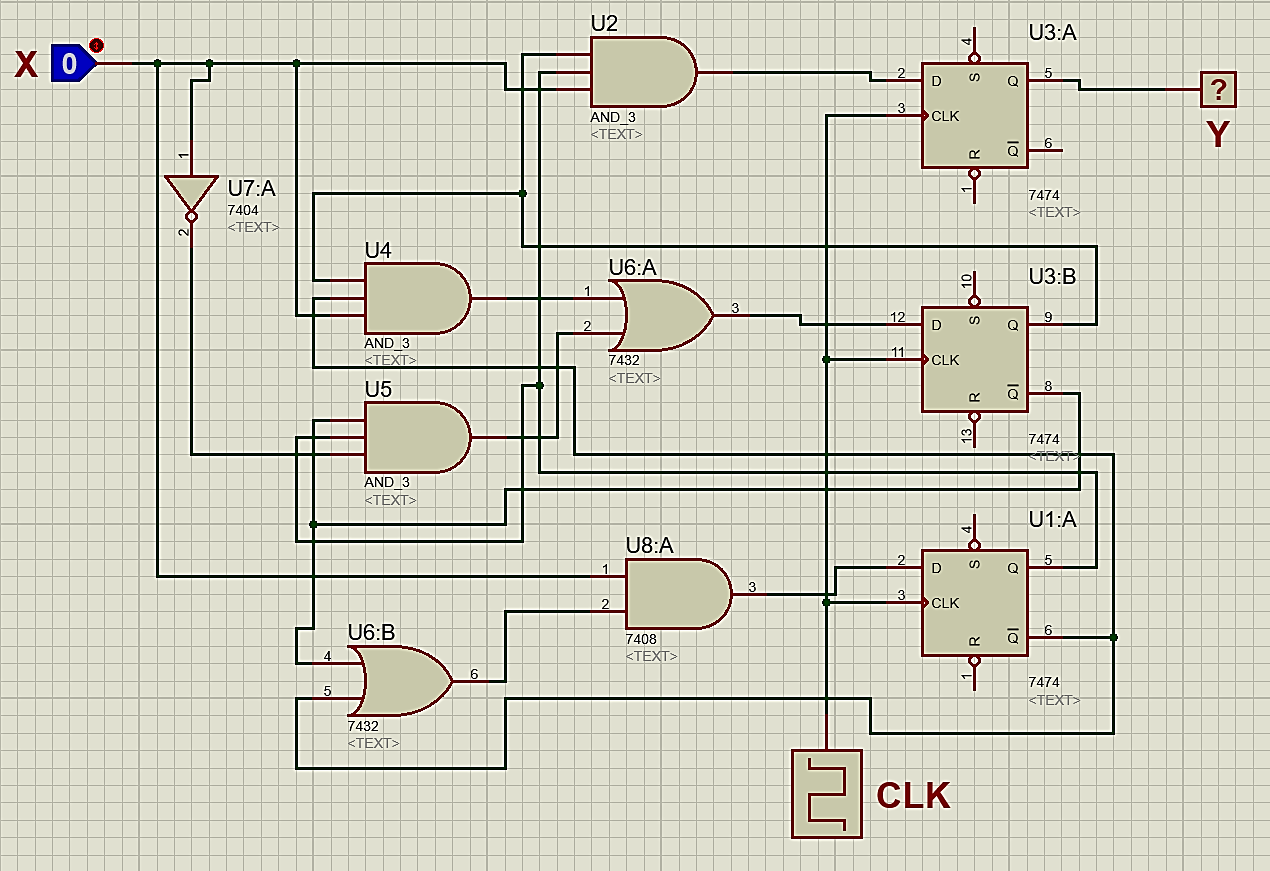
**Obtain the simplified equations for Output y and Flip-Flop Inputs using map method.**

|  |  |
| --- | --- |
| **Function** | **Expression** |
| **QA+** | **QBQCX** |
| **QB+** | **QBQC’X + QB’QCX’** |
| **QC+** | **X (QA’ + QB’)** |
| **Y** | **QA** |

**Pre – Lab Task 5**

**Draw the logic diagram of Moore Sequence Detector.**

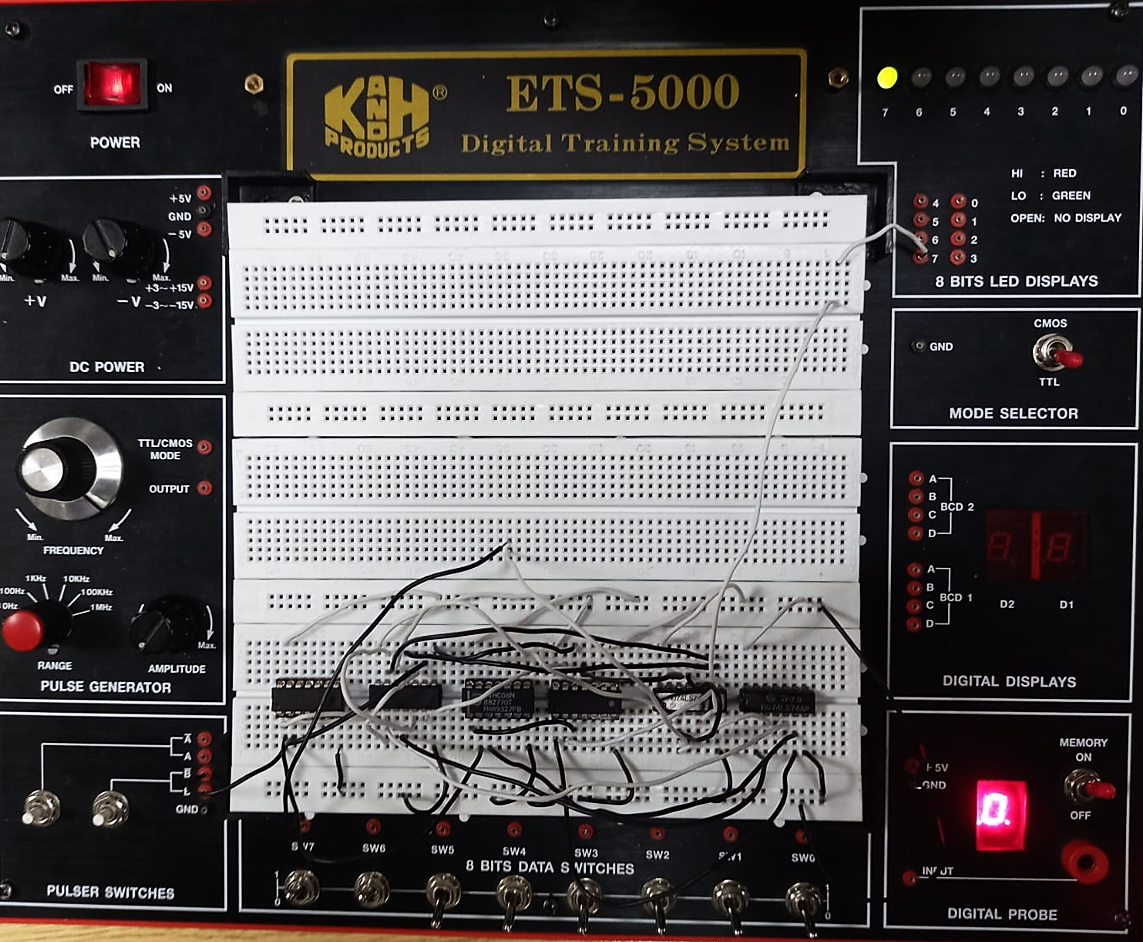
The logic diagram of such a sequence detector can be made by using three flip flops; no state reduction is applicable in the present case.



**Lab Tasks**

**Lab Task 1**

**Implement the sequence detectors in hardware and show results to your Instructor/Lab Engr.**

**Hardware Implementation**

**Proteus Simulation**

