Department of Electrical Engineering

**Department of Electrical Engineering**

**Faculty Member: Dated:**

**Semester: Section:**

*Group No.:*

**EE-221: Digital Logic Design**

**Assessment Rubrics for Lab 13: Sequence Detector**

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| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **PLO4/CLO4** | **PLO4/CLO4** | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |  |
| **Name** | **Reg. No** | **Viva / Lab Performance** | **Analysis of data in Lab Report** | **Modern Tool Usage** | **Ethics and Safety** | **Individual and Team Work** | **Total marks Obtained** |
|  |  | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **25 Marks** |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
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## Lab12: Sequence Detector

This Lab Activity has been designed to familiarize the students with design and implementation of a sequence detector from an incoming binary stream received serially. The students are expected to do the following: -

* Complete the Sequential Design Method
* Design the circuit using D Flip-Flops.
* The students are required to complete Pre-Lab work before coming to the lab and submit lab report before leaving.

**Pre-Lab Tasks:**

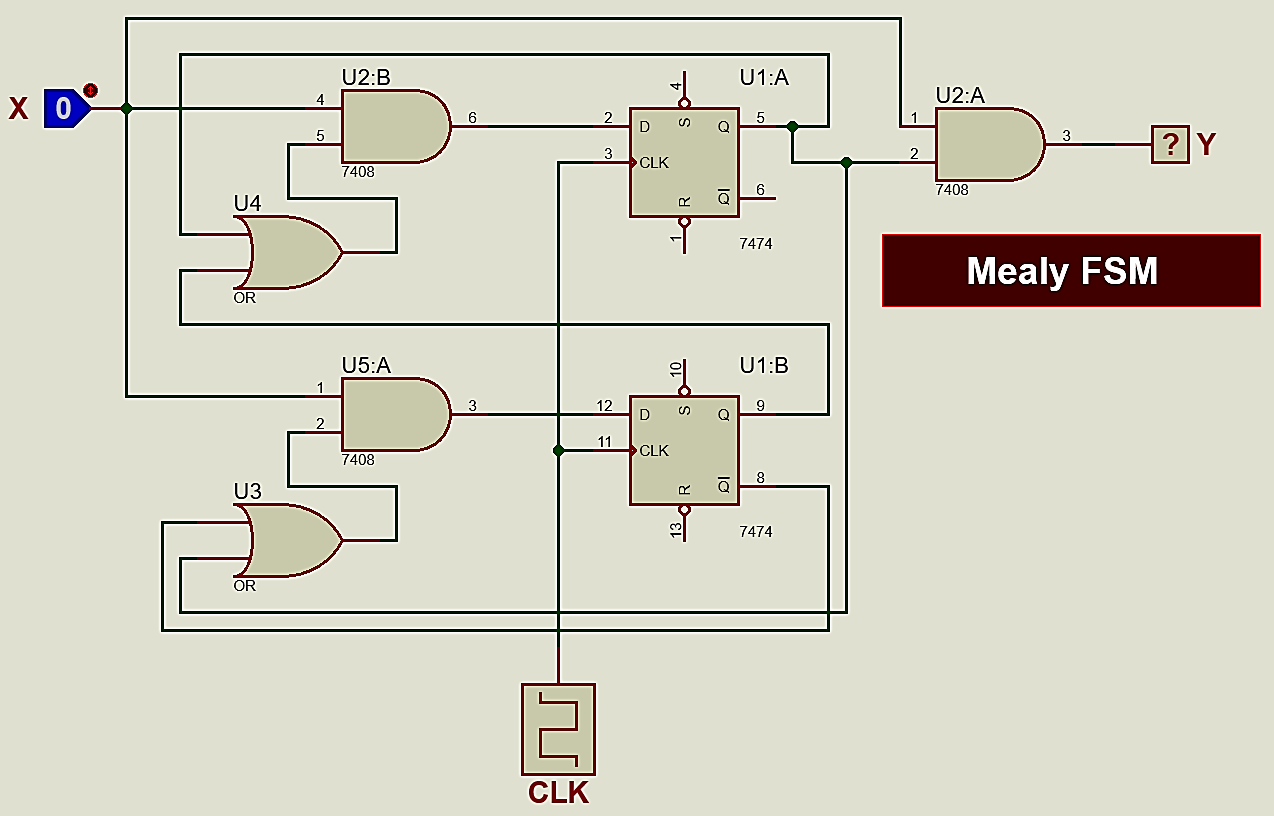
1. We wish to design a circuit with single input **x**, and a single output **z**, that detects three or more consecutive 1’s in a string of bits coming through an input line. We start it in the initial state **S0**. In our design, the detector circuit will only advance to the next state if some valid bit of the specified sequence is received otherwise will go back to either **S0** or any other state depending upon whether sequence breaks totally or partially. As and when any of the two sequences is received completely, the detector circuit will output 1.

There are two FSM models for each design. Name these models and give advantages/ disadvantages of each? Which method you prefer and why? (1 Mark)

**The two types of models that can tackle this problem are Moore FSM and Mealy FSM. Mealy Models are less stable but can be implemented using a lesser number of flip flops whereas Moore Models are more stable but at the cost of more states and hence, a greater number of flip flops.**

**For the purpose of this lab, we have preferred to go with Mealy as it requires lesser hardware, and we are not strictly imposed / concerned with the stability of our system.**

Draw the Mealy state diagram for the sequence detector. How many D Flip-Flops would you need for implementing the sequence detector and why? (5 Marks)



We would require 2 D – Flip Flops as there are four possible states.

2. List the State Transition Table (2 Marks)

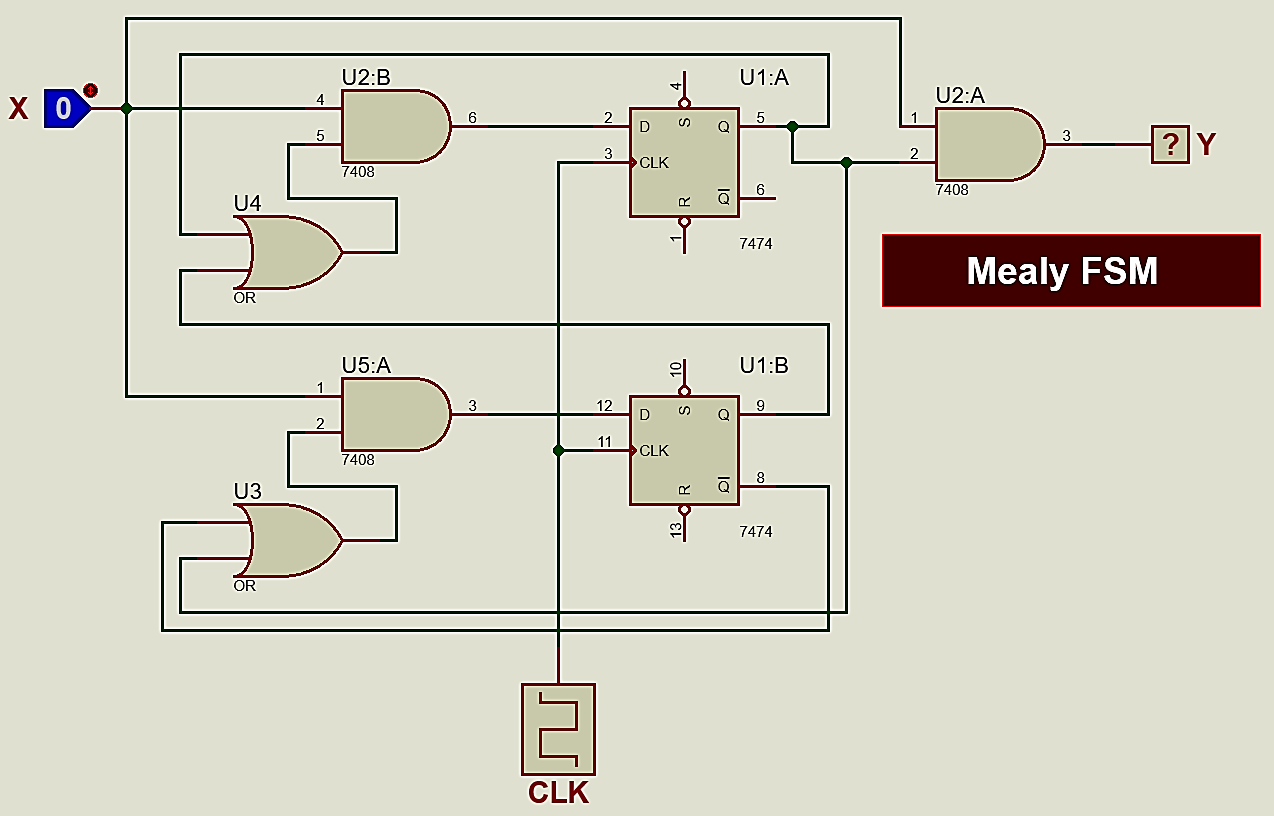
Done

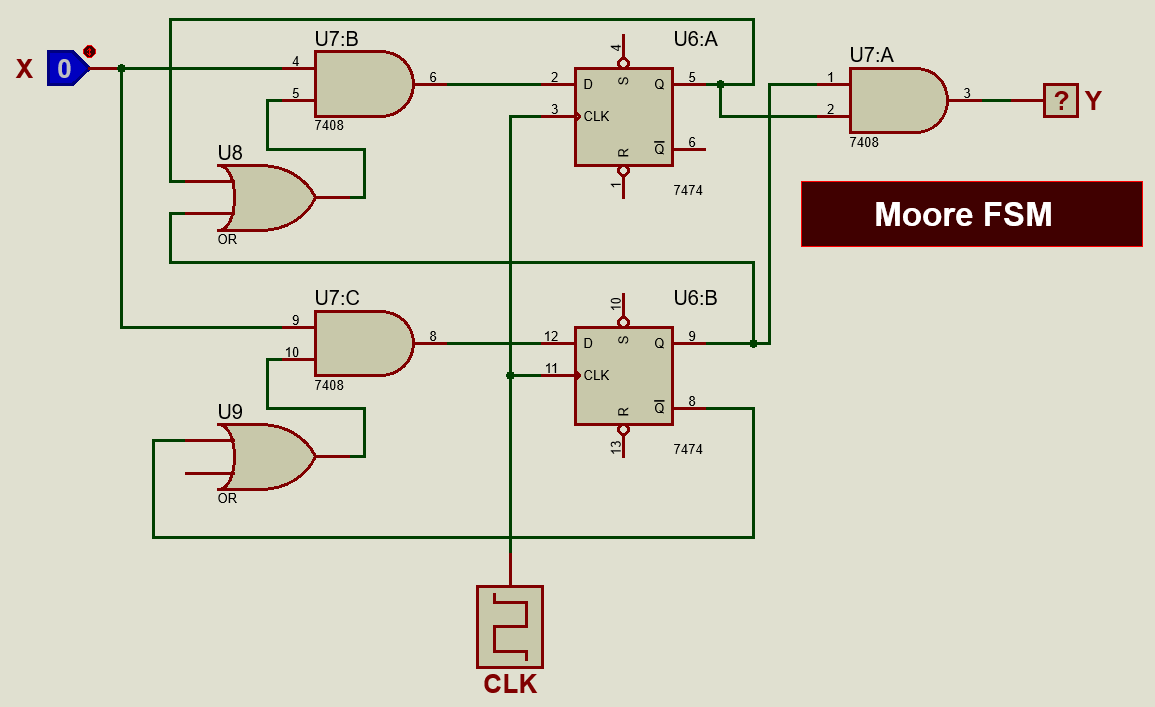
3. Obtain the simplified equations for Output y and Flip-Flop Inputs using map method.

(4 Marks)

Done

4. Draw complete circuit diagrams for both the sequence detectors using D flip flops and external AND, OR gates . (3 Marks)





**Lab Task:**

5. Implement the sequence detectors in hardware and show results to your Instructor/Lab Engr. (10 Marks)

ICs Used:

7474 for D Flip-Flop