**Department of Electrical Engineering**

**Faculty Member:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Dated: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Semester:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_** 

**EE-221: Digital Logic Design**

**Lab 8: 2-bit binary Adder and Subtractor**

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|  |  | **PLO4/CLO4** | **PLO4/CLO4** | **PLO5/CLO5** | **PLO8/CLO6** | **PLO9/CLO7** |  |
| **Name** | **Reg. No** | **Viva / Lab Performance** | **Analysis of data in Lab Report** | **Modern Tool Usage** | **Ethics and Safety** | **Individual and Team Work** | **Total marks Obtained** |
|  |  | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **5 Marks** | **25 Marks** |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

## Lab 8: 2-bit binary Adder and Subtractor

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**Lab Instructions**

* This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
* The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation. Alternately each group to upload completed lab report on LMS for grading.
* The students will start lab task and demonstrate design steps separately for step-wise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
* Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
* After the lab, students are expected to unwire the circuit and deposit back components before leaving.
* **The Total duration for the lab is 3 hrs.**
* **A lab with in-complete lab tasks will not be accepted.**
* The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
* There are related questions at the end of this activity. Give complete answers.

**Pre-Lab Tasks: (2 marks)**

1. What do you understand by half and full adders and why are these circuits so named?

**Half Adder:**

A combinational circuit that adds two bits (Two Inputs) and generates a SUM and a CARRY. It is called a half adder because two half adders combined form a full adder.

A, B → S, COUT

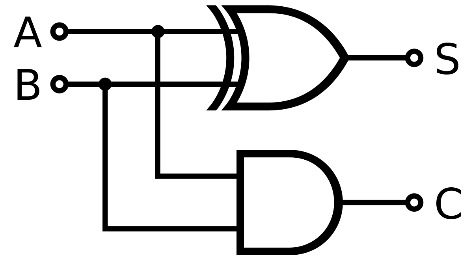
**Full Adder:**

A combination circuit that adds three bits (Two Inputs and a Carry In) to yield a SUM and a CARRY. It is named so because complete addition can be performed with such an IC.

A, B, CIN → S, COUT

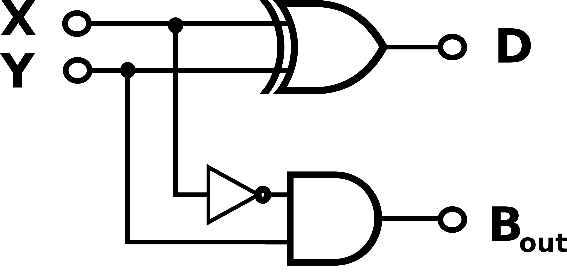
1. Give the truth table and circuit for half adder and half subtractor.

**Half Adder**



|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **SUM** | **CARRY** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

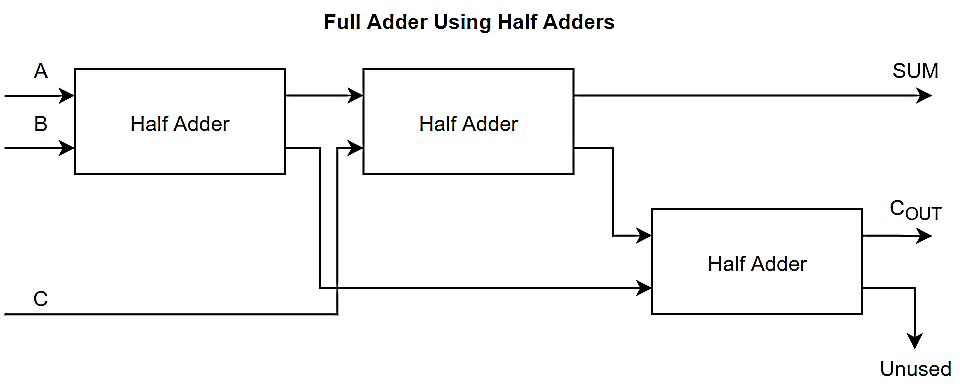
**Half Subtractor**



|  |  |  |  |
| --- | --- | --- | --- |
| **X** | **Y** | **DIFFERENCE** | **BORROW** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

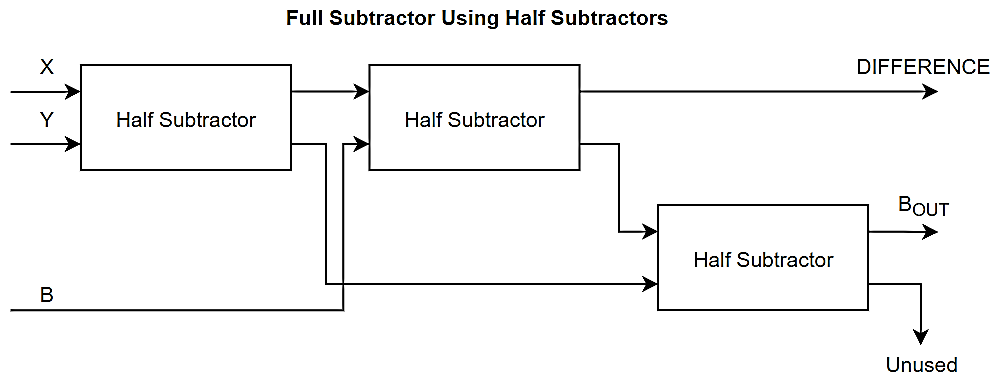
1. Design a full adder/subtractor using the above designed half adders/subtractor.

**Full Adder Using Half Adders**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **SUM** | **CARRY** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Full Subtractor Using Half Subtractors**

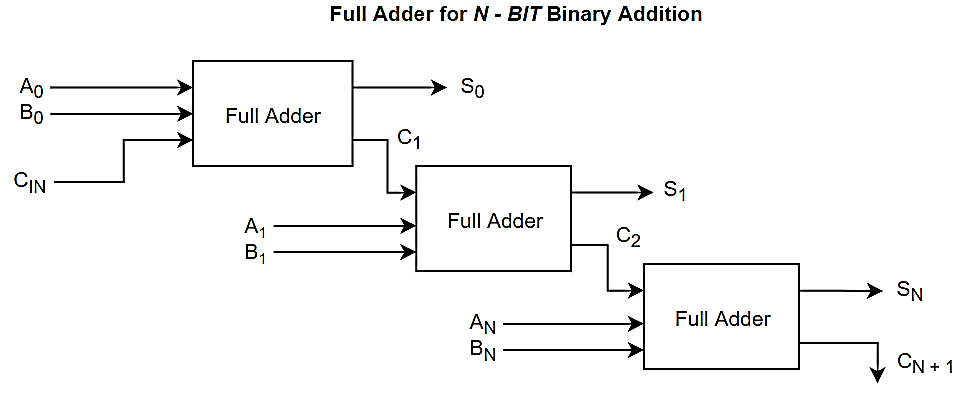


|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **X** | **Y** | **BIN** | **DIFF** | **BOUT** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

1. Now add the subtraction option in your design and show the logic diagram of full adder with subtractor.
2. Can you extend your design to n-bit binary addition? How does input carry propagates through full adder stages for such design and influences the speed? How can you overcome this problem?

**Yes**, this design can be extended to perform n – bit binary addition. An abstract for such a logic through blocks is given below:

**Full Adder for N – Bit Binary Addition**



**Lab Tasks: (3 marks)**

1. Extend your design to 2-bit binary adder and subtractor. Draw the block diagram of the circuit with inputs, outputs and carry.
2. Draw the schematic diagram of the circuit with complete pin configuration, number, each gate input output and carry. Carry out the hardware implementation of your 2-bit adder subtractor and show the results to lab instructor
3. Get the 4-bit binary adder IC from the lab and verify its functionality. Give IC number and pin-layout of the IC.

1. Give the Gate-Level Verilog Code for four-bit adder and show the results on Simulation. Your code should contain following modules:

**half adder**

**full adder** (by instantiating **half adder**)

**4\_bit\_ binary\_ adder** (by instantiating **full adder**)

**test bench\_ 4\_bit\_binary\_adder** (for **4\_bit\_ binary\_ adder**)

Verilog Code:

Waveform/Output: