Decrement Beyond 0x00

# Iteration 1

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 2

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 3

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 4

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 5

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 6

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 7

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |

# Iteration 8

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| Control Status Register | **I** | **T** | **H** | **S** | **V** | **N** | **Z** | **C** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Alterations |  |  |  |  |  |  |  |  |
| Reason for alterations |  |  |  |  |  |  |  |  |