**Department of Electrical Engineering and   
Computer Science**

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**Semester:** 5th **Section:** BEE 12C

**EE-313:** **Electronic Circuit Design**

Lab 3: Cascode Amplifier

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# Common Emitter Amplifier

## Objectives

* To perform DC analysis and calculate gain
* Implement it on hardware and verify calculations

## Equipment

Hardware

* Discrete elements
* Breadboard
* BJTs

Software

* *PSpice*



## Introduction

This lab provides an evaluation of the Cascode amplifier.

The cascode is a two-stage amplifier comprising a common emitter stage feeding into a common base stage. Compared to a single amplifier stage, this combination may have one or more of the following characteristics: output impedance, higher gain or higher bandwidth.

The cascode is often constructed from two transistors (BJTs or FETs), with one operating as a common emitter or common source and the other as a common base or common gate.

## Lab Instructions

All questions should be answered precisely to get maximum credit. Lab report must ensure following items:

* Lab objectives
* Results (Graphs/Tables) duly commented and discussed
* Conclusion

# Lab Tasks

Theoretical Calculations

### Circuit

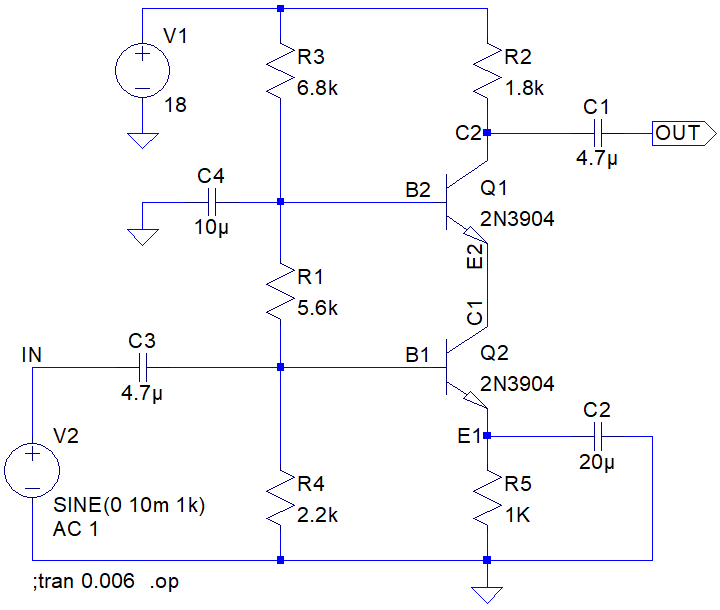


Figure 4.1.1.a: Cascode Amplifier

### Results

1. **DC Bias Voltages**

**VB1** (calculated) = 2.724 V **VB2** (calculated) = 9.622 V

**VC1** (calculated) = 8.923 V **VC2** (calculated) = 14.41 V

**VE1** (calculated) = 2.024 V **VE2** (calculated) = 8.922 V

1. **DC Bias Emitter Currents**

**IE1** (calculated) = 2.02 mA **IE2** (calculated) = 2.02 mA

## Simulation

### Operating Point Analysis

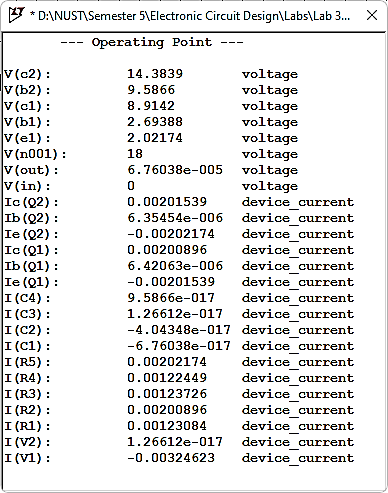


Figure 4.2.1.a Bias Point Simulation

### Transient Analysis

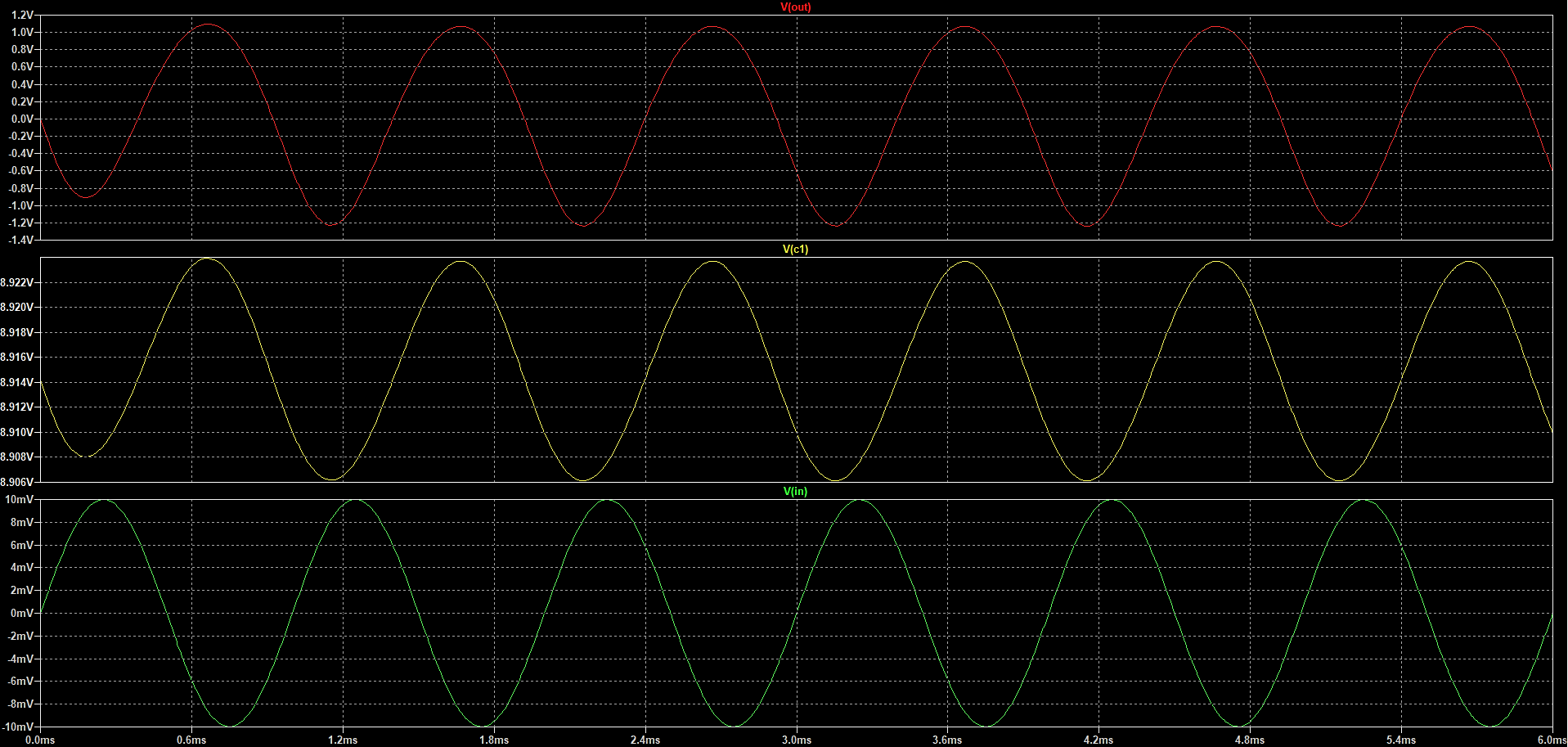


Figure 4.2.2.a Waveforms

### Results

1. **DC Bias Voltages**

**VB1** (simulated) = 2.693 V **VB2** (simulated) = 9.586 V

**VC1** (simulated) = 8.914 V **VC2** (simulated) = 14.38 V

**VE1** (simulated) = 2.021 V **VE2** (simulated) = 8.914 V

1. **DC Bias Emitter Currents**

**IE1** (simulated) = 2.01 mA **IE2** (simulated) = 2.01 mA

1. **AC Voltage Gain of Q1 and Q2**

**AV1** (simulated) = 0.850 V/V **AV2** (simulated) = 136.7 V/V

## Implementation

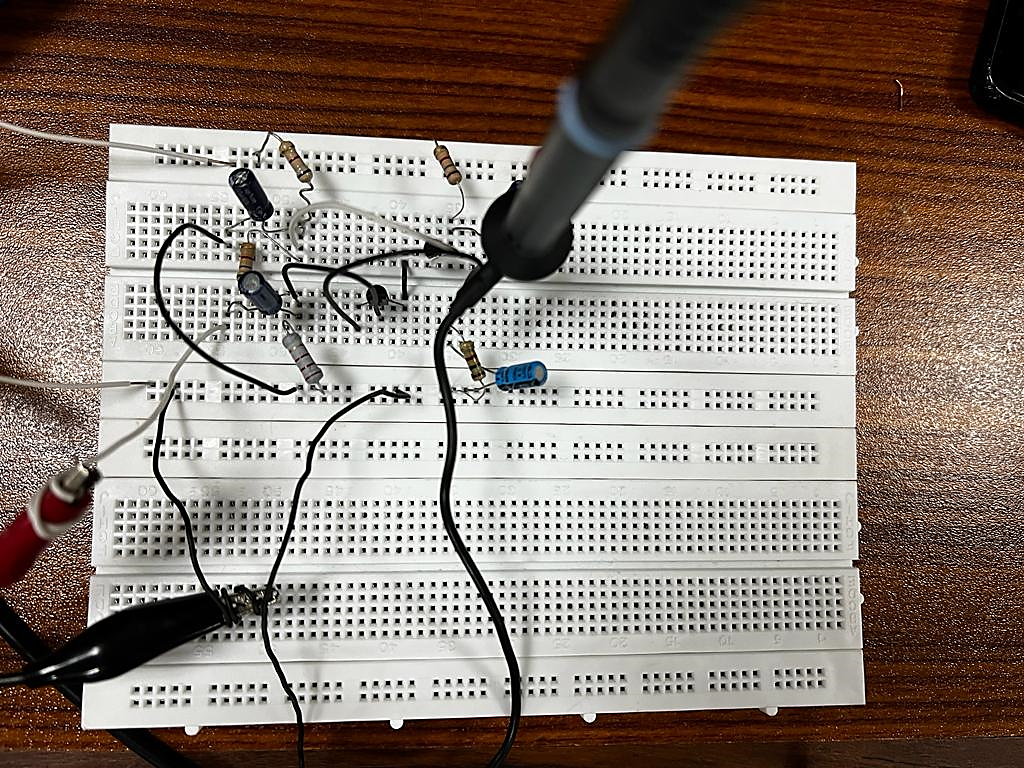


Figure 4.2.3.a Circuit Implementation

### Output Waveform

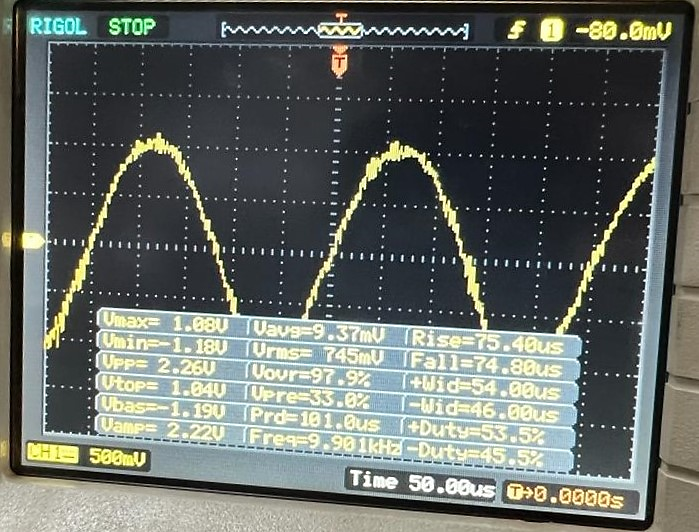


Figure 4.3.1.a Oscilloscope Output

### Results

1. **BJT Voltages (P-P)**

**Vi** (measured) = 19.99 mV

**VO1** (measured) = 16 mV **VO2** (measured) = 2.26 V

1. **AC Voltage Gain**

**AV1** (measured) = 0.842 V/V **AV2** (measured) = 141.25 V/V

**AV-Total** (measured) = 118.93 V/V

# Conclusion

After performing this lab, we have extended our knowledge of amplifiers to a phenomenon known as cascading. We recorded its advantages; a better overall stability is achieved by making one transistor of the cascoded arrangement focus on the operating bandwidth, and the other on the voltage gain. Unlike a single stage amplifier, that always has trade-offs between the gain and bandwidth, we can relatively easily increase the output impedance (RO) of our system and achieve a higher gain by cascoding. Lastly, we verified the theoretical and simulation results with that of the practical implementation and found minimal error margin.