**Department of Electrical Engineering and   
Computer Science**

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**Semester:** 5th **Section:** BEE 12C

**EE-313:** **Electronic Circuit Design**

Lab 9: Differential Pair with Active Load

Group Members

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Reg. No** | **Report**  **Marks** | **Viva**  **Marks** | **Total**  **Marks** |
|  |  | **10 Marks** | **5 Marks** | **15 Marks** |
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# Differential Amplifier

## Objectives

* To design a BJT differential amplifier

## Equipment

Hardware

* Discrete elements
* Breadboard
* BJTs

Software

* PSpice



## Introduction

The differential amplifier, or differential pair, is an essential building block in all integrated amplifiers. In general, the input stage of any analog integrated circuit with more than one input consists of a differential pair or differential amplifier. The basic differential pair circuit consists of two-matched transistors *Q*3 and *Q*4 their emitters are joined together and biased a constant current source.

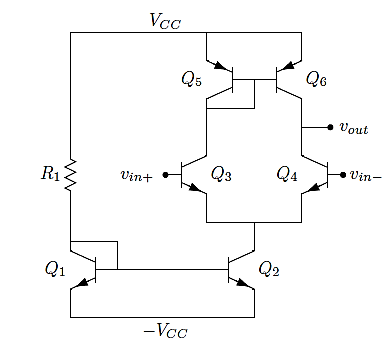
## Lab Instructions

All questions should be answered precisely to get maximum credit. Lab report must ensure following items:

* Lab objectives
* Results (Graphs/Tables) duly commented and discussed
* Conclusion

# Lab Tasks

## Calculation



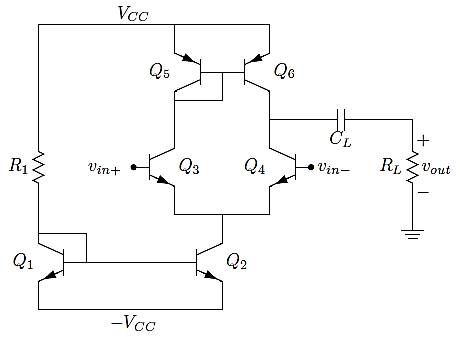
Figure

1. Consider the circuit, shown in Figure 1, in PSPICE using 2N3904 transistors for the NPN BJTs and 2N3906 for PNP. Use R1 = 10 kΩ, R2 = R3 = 5.6 kΩ, and VCC = 9 V.
2. Calculate the Differential mode gain of the amplifier shown in figure 1 with values given above. (Assume VBE = 0.7V)

**Gain:** 2000 V/V

1. Now consider the circuit given in Figure 2. Calculate the differential mode gain of the circuit given in Figure 2. Use R1 = 10 kΩ and VCC = 9 V.

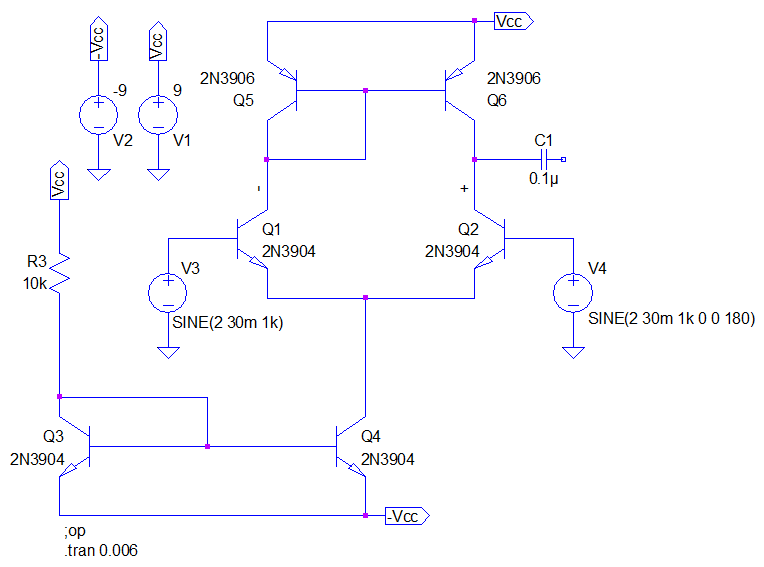
**Gain:** 171.4 V/V



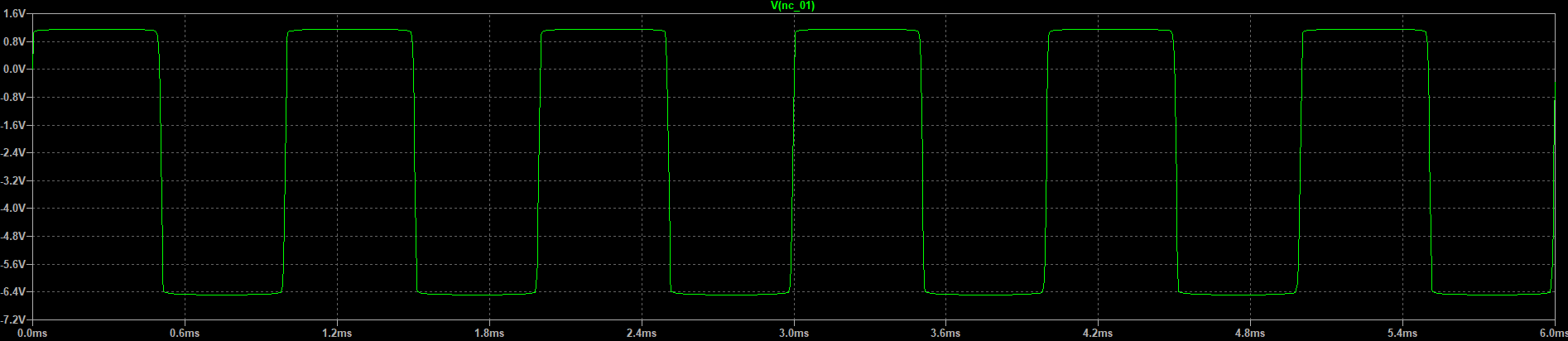
Figure

## Simulation

Construct the circuit in the following figure using 2N3904 transistors for the NPN BJTs and 2N3906 transistors for the PNP BJTs. Use R1 = 10 kΩ and VCC = 9 V.



Apply a 30 mV amplitude, 1 kHz sine wave to vin+ and ground vin−. Use the level marker to display the output waveform at VOUT and sketch the result.



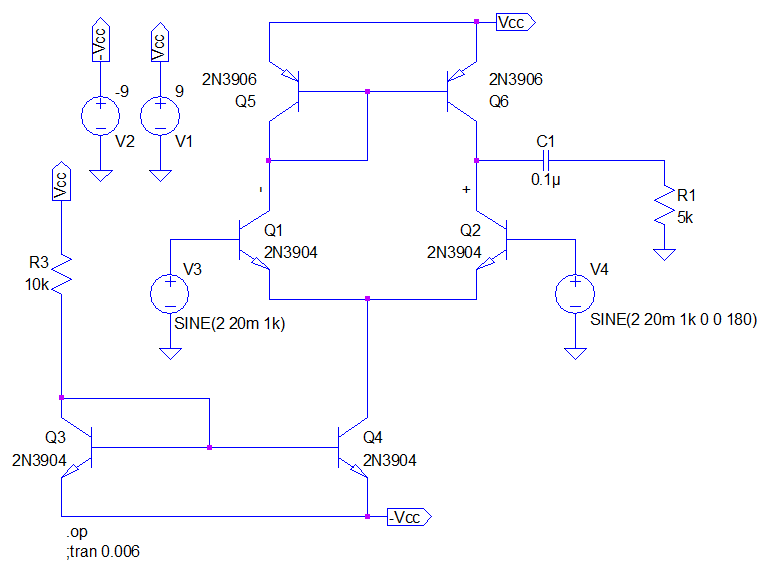
1. Why isn’t the output sinusoidal?

**Answer:** The output is not sinusoidal as it is clipping due to exceeding supply voltage VCC.

1. We’d like to reduce ROUT by loading the amplifier with a small resistor. Attach a load to the amplifier as shown in Figure 2. Use CL = 0.1 µF and RL = 5 kΩ.
2. Calculate the differential gain for the amplifier with the new load resistance.

**Gain:** 79.28 V/V

1. Apply a 20 mV amplitude, 1 kHz sine wave to vin+ and ground VIN-. Use the level marker to display VIN+ and VOUT. Sketch VOUT.





1. What is the measured differential gain of the circuit?

**Gain:** 110.8 V/V

1. How does this compare with your calculations?

**Answer:** Error between simulated and calculated gain

The large mismatch between the simulated and calculated gain arises due to the signal clipping in simulation; an input differential signal of 0.05 mV reduces the error to 1.7%.

1. Does the gain match the differential gain you measured for resistive load differential amplifier? Should it?

**Answer:** The open-loop gain does not match the gain obtained with R­L = 5k Ω. It shouldn’t, as the open-loop gain is obtained by gm times the output resistance of transistors which are ideally infinite or practically very large while the gain with load is less since the load appears in parallel with the output resistances.

# Conclusion

In this lab we learnt about the core concepts of differential amplifiers with active load. We correlated the theoretical concepts with simulations and practical hardware. We learnt about the gain factor and how active load affects the gain of differential amplifier. The differential amplifier, or differential pair, is an essential building block in all integrated amplifiers. In general, the input stage of any analog integrated circuit with more than one input consists of a differential pair or differential amplifier.