FAKULTI TEKNOLOGI & KEJURUTERAANELEKTRONIK & KOMPUTER UNIVERSITI TEKNIKAL MALAYSIA MELAKA

TECHNOLOGY SKILL AND DEVELOPMENT IN ELECTRONIC AUTOMATION II

BERL 1214	SEMESTER 2	SESI 2023/2024

PROJECT: Design a Synchronous Abnormal Counter

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DATE	5 JUN 2024
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	2.
EXAMINER'S COMMENT(S)	TOTAL MARKS

1. INTRODUCTION

In digital electronics, counters are sequential circuits that advance through a specific set of states upon receiving clock pulses. They are widely used in digital systems such as timers, frequency dividers, and digital controllers.

A **synchronous counter** is a type of counter in which all flip-flops are triggered by the same clock signal, ensuring simultaneous state changes. Unlike normal binary or decade counters that follow a natural binary sequence, an **abnormal counter** (also called a non-sequential or arbitrary counter) follows a custom or irregular sequence of states defined by the designer.

In this project, a **synchronous abnormal counter** is designed to follow the sequence:

F → E → C → A → 3 → 2 → 1 → F

Each letter or number represents a unique state encoded in binary form. The design uses **JK flip-flops** to achieve synchronous operation and includes logic to recover automatically if the counter enters an invalid state.

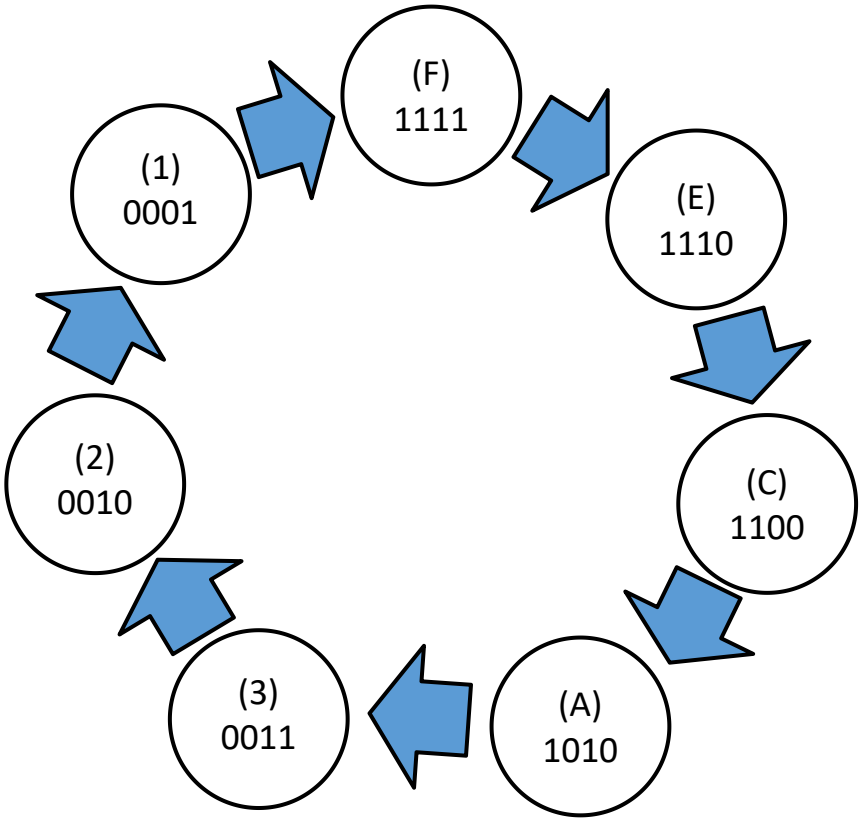
2. OBJECTIVE

To design and implement a **synchronous abnormal counter** that cycles through the sequence :

F → E → C → A → 3 → 2 → 1 → F,

using D flip-flops and combinational logic, with automatic recovery from invalid states.

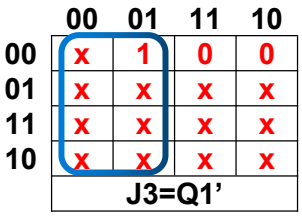
3. STATE DIAGRAM



4. STATE AND EXCITATION TABLE

PRESENT STATE					NEXT STATE					FLIP-FLOP INPUTS								
	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0		J3	K3		J2	K2		J1	K1		J0	K0
F	1	1	1	1	1	1	1	0		X	0		X	0		X	0		X	1
E	1	1	1	0	1	1	0	0		X	0		X	0		X	1		0	X
C	1	1	0	0	1	0	1	0		X	0		X	1		1	X		0	X
A	1	0	1	0	0	0	1	1		X	1		0	X		X	0		1	X
3	0	0	1	1	0	0	1	0		0	X		0	X		X	0		X	1
2	0	0	1	0	0	0	0	1		0	X		0	X		X	1		1	X
1	0	0	0	1	1	1	1	1		1	X		1	X		1	X		X	0

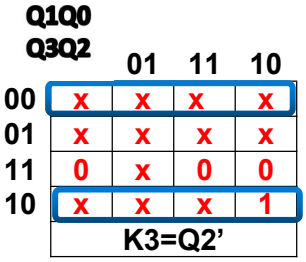
5. KARNAUGH MAP



	00	01	11	10
00	x	1	0	0
01	x	x	x	x
11	x	x	x	x
10	x	x	x	x

J3=Q1'

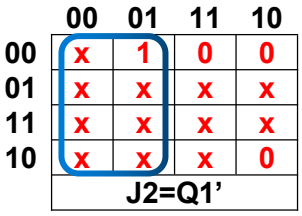
J3



Q1Q0 / Q3Q2	01	11	10
00	x	x	x
01	x	x	x
11	0	x	0
10	x	x	1

K3=Q2'

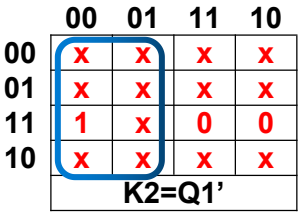
K3



	00	01	11	10
00	x	1	0	0
01	x	x	x	x
11	x	x	x	x
10	x	x	x	0

J2=Q1'

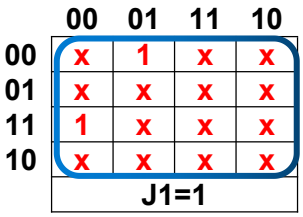
J2



	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	1	x	0	0
10	x	x	x	x

K2=Q1'

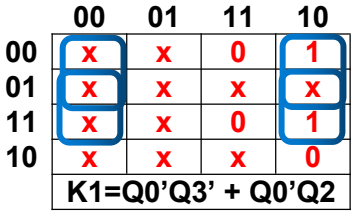
K2



	00	01	11	10
00	x	1	x	x
01	x	x	x	x
11	1	x	x	x
10	x	x	x	x

J1=1

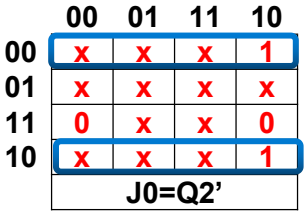
J1



	00	01	11	10
00	x	x	0	1
01	x	x	x	x
11	x	x	0	1
10	x	x	x	0

K1=Q0'Q3' + Q0'Q2

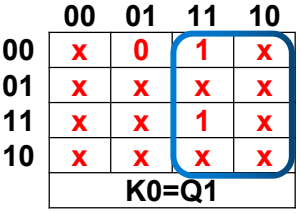
K1



	00	01	11	10
00	x	x	x	1
01	x	x	x	x
11	0	x	x	0
10	x	x	x	1

J0=Q2'

J0

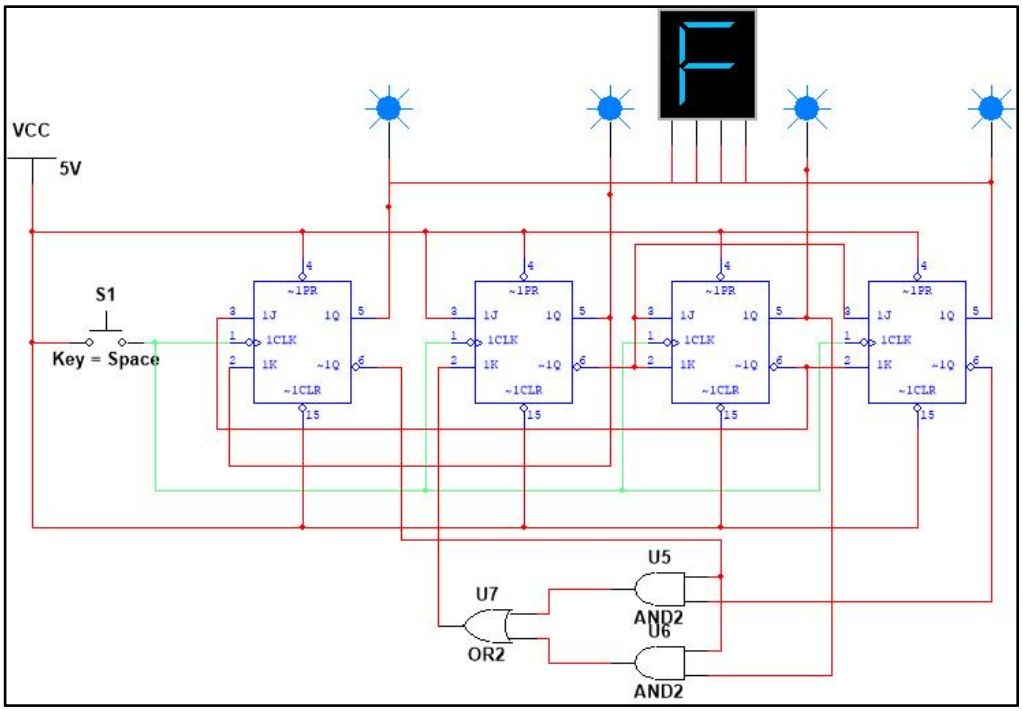


	00	01	11	10
00	x	0	1	x
01	x	x	x	x
11	x	x	1	x
10	x	x	x	x

K0=Q1

K0

6. COUNTER IMPLEMENTATION



7. CONCLUSION

In conclusion,Designing a synchronous counter to produce the sequence (F, E, C, A, 3, 2, 1) involves:

Identifying the Sequence: Define the binary values for each state.

State Transition Diagram: Create a diagram showing the progression from one state to the next.

State Table: Map current states to next states.

Determine Flip-Flop Inputs: Find the required inputs for JK flip-flops to transition between states.

Simplify Logic: Use Karnaugh maps to simplify the boolean expressions for flip-flop inputs.

Design the Circuit: Build the circuit using JK flip-flops and logic gates based on the simplified expressions. This method ensures the counter follows the desired sequence accurately and efficiently.