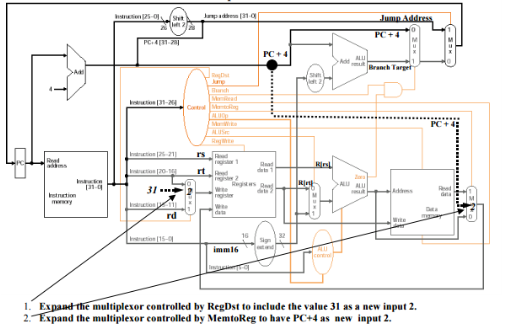
1. This project is a single cycle Mips Processor. It consist of (17 )modules:
2. Program Counter
3. Instruction Memory
4. Register File
5. ALU
6. Data Memory
7. Adders
8. Control unit
9. Shift left unit
10. Alu control unit
11. Sign Extender unit
12. Multiplexer 2x1
13. Multiplexer 3x1
14. Language used Verilog , Active -HDL
15. BOUNCE: Assembler using “python”
16. 

Supporting :**Arithmetic:** add, addi

**Load/Store:** lw, sw

**Logic:** sll, and, andi, nor

**Control flow:** beq, jal, jr

**Comparison:** slt

1. The project was split into modules, uploaded on github. you can review the project on github.