```
1   `timescale 1ns / 1ps
2
3   ////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   20:07:54 04/09/2024
8   // Design Name:   USR
9   // Module Name:   C:/Users/hp/OneDrive/Desktop/Group 5/USR/USR_tb.v
10  // Project Name:  USR
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: USR
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  ////////////////////////////////////////////////////////////////////////////////
24
25  module USR_tb;
26
27     // Inputs
28     reg clr;
29     reg clk;
30     reg left_in;
31     reg right_in;
32     reg [1:0] sel;
33     reg [3:0] par_in;
34
35     // Outputs
36     wire [3:0] out;
37
38     // Instantiate the Unit Under Test (UUT)
39     USR uut (
40        .clr(clr),
41        .clk(clk),
42        .left_in(left_in),
43        .right_in(right_in),
44        .sel(sel),
45        .par_in(par_in),
46        .out(out)
47     );
48
49     initial begin
50        // Initialize Inputs
51        clr = 0;
52        clk = 0;
53        left_in = 0;
54        right_in = 0;
55        sel = 0;
56        par_in = 0;
57
```

```
58          // Wait 100 ns for global reset to finish
59          #10;
60
61          // Add stimulus here
62          clr = 1'b1;
63          #10;
64          //out = 4'b000;
65          //#100;
66          clr = 1'b0;
67          #40;
68
69          right_in = 1'b1;
70          sel = 2'b01;
71          #40;
72
73          left_in = 1'b0;
74          sel = 2'b10;
75          #40;
76          par_in = 4'b1010;
77          sel = 2'b11;
78      end
79          always clk = #5 ~clk;
80  endmodule
81
82
```