```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date:    19:58:58 04/09/2024
7  // Design Name:
8  // Module Name:    USR
9  // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21 module USR(clr, clk, left_in,right_in, sel, par_in, out);
22
23    input clr, clk, left_in, right_in;
24    input [1:0] sel;
25    input [3:0]par_in;
26
27 output reg [3:0]out;
28
29 //behavioural modeling style
30
31    always@(posedge clk)
32
33       begin
34       if (clr)
35       out = 4'b0000;
36       else
37       begin
38          case(sel)
39             2'b00: out = out; //no change
40             2'b01: out = {right_in, out[3:1]}; // right shift
41             2'b10: out = {out[2:0], left_in}; //left shift
42             2'b11: out = par_in; //parellel load
43          endcase
44       end
45    end
46 endmodule
47
```