CSA Proj Phase 2

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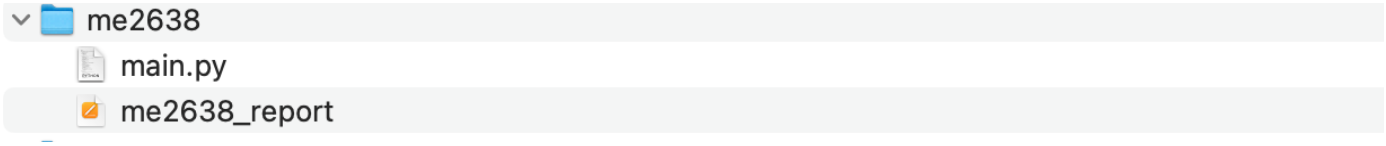
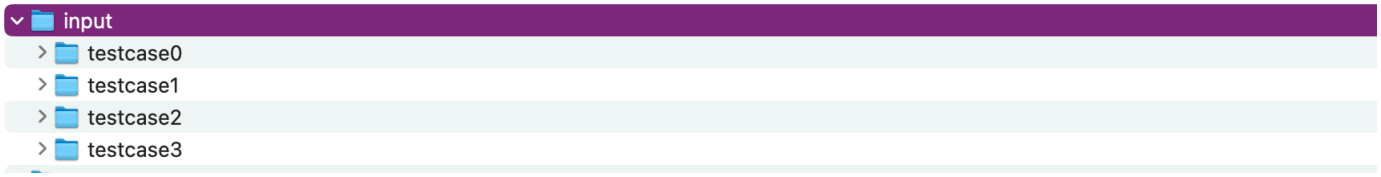
ME2638

- The complete code is stored inside the folder Me2638 named as main.py.
- The language used is python.
- To run the code, just the following structure of files should be followed and no other external libraries are to be installed.



- Inside me2638 the main.py is present and inside Input , the testcases are present as shown below.



- Terminal ss of running the code for different test cases.

```
muki@10-18-245-113 Project_CSA %  /usr/bin/env /usr/local/bin/python3 /Users/muki/.vscode/extensions/ms-python.python-2023.22.0/pythonFiles/lib/python/debugpy/adapter/.
./../debugpy/launcher 52411 -- /Users/muki/Documents/Project_CSA/me2638/main.py
IO Directory: /Users/muki/Documents/Project_CSA/input/testcase3
IO Directory: /Users/muki/Documents/Project_CSA/input/testcase2
IO Directory: /Users/muki/Documents/Project_CSA/input/testcase0
IO Directory: /Users/muki/Documents/Project_CSA/input/testcase1
muki@10-18-245-113 Project_CSA %
```

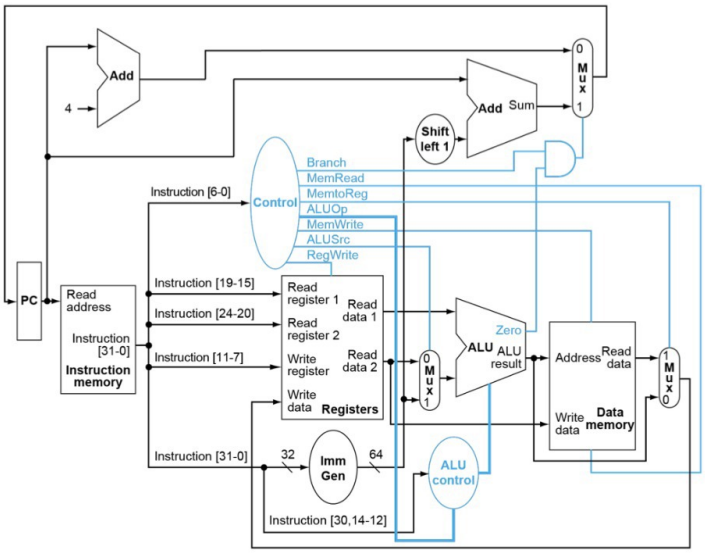
To run the program,

Go to the project folder in terminal and follow the commands given below,

- Run the command python net_id/main.py

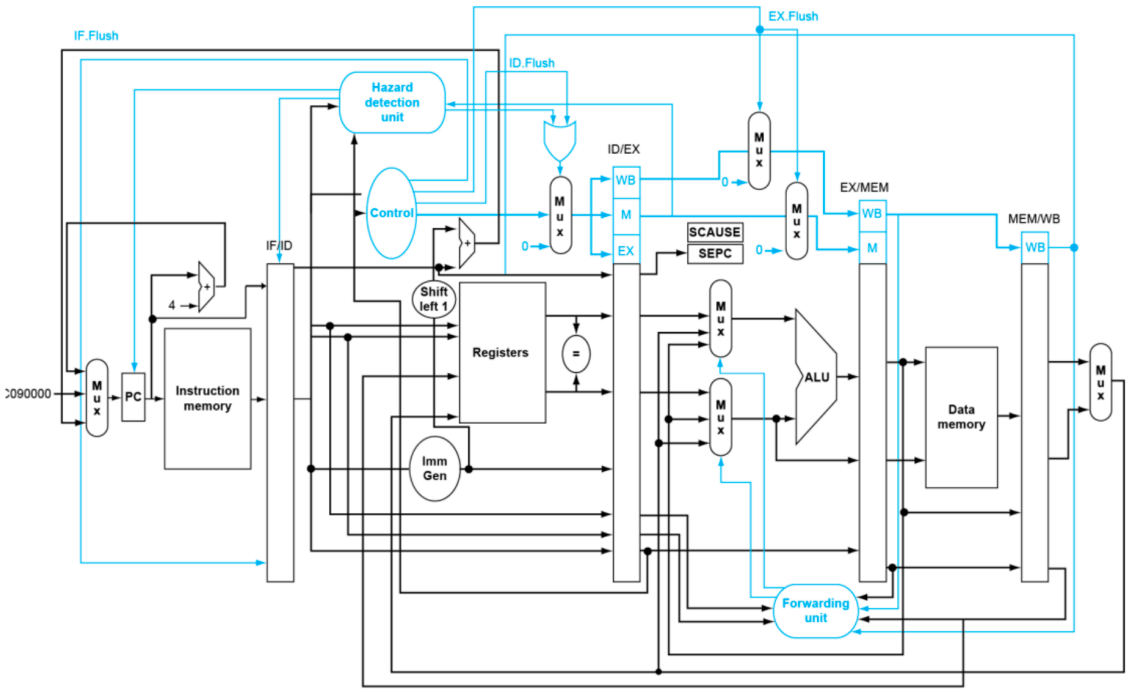
Here, the net_id is the folder where main.py file is present.

1)Draw the schematic for a single-stage processor and fill in your code to run the simulator.



(i.e) From lecture slides

2) Draw the schematic for a five stage processor and fill in your code in the provided file to run the simulator.



b) The final code is available in me2638/main.py.

3) Measure and report average CPI, Total execution cycles, and Instructions per cycle by adding performance monitors to your code. Make sure you output these values to a file.

Testcase 0:

Single Stage Core Performance Metrics

Total execution cycles = 6

Average CPI = 1.2

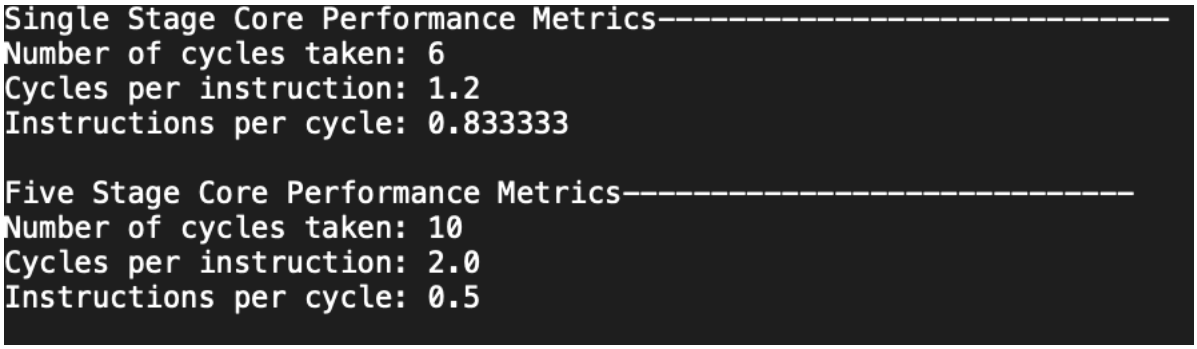
Instructions per cycle = 0.833333

Five Stage Core Performance Metrics----------

Number of cycles taken: 10

Cycles per instruction: 2.0

Instructions per cycle: 0.5



Testcase 1:

Single Stage Core Performance Metrics

Total execution cycles = 40

Average CPI = 1.02564

Instructions per cycle = 0.975001

Five Stage Core Performance Metrics----------

Number of cycles taken: 46

Cycles per instruction: 1.17949

Instructions per cycle: 0.847824

```
Single Stage Core Performance Metrics----------
Number of cycles taken: 40
Cycles per instruction: 1.02564
Instructions per cycle: 0.975001

Five Stage Core Performance Metrics----------
Number of cycles taken: 46
Cycles per instruction: 1.17949
Instructions per cycle: 0.847824
```

Testcase 2:

Single Stage Core Performance Metrics

Total execution cycles = 7

Average CPI = 1.75

Instructions per cycle = 0.571429

Five Stage Core Performance Metrics----------

Number of cycles taken: 10

Cycles per instruction: 2.5

Instructions per cycle: 0.4

```
Single Stage Core Performance Metrics----------
Number of cycles taken: 7
Cycles per instruction: 1.75
Instructions per cycle: 0.571429

Five Stage Core Performance Metrics----------
Number of cycles taken: 10
Cycles per instruction: 2.5
Instructions per cycle: 0.4
```

Testcase 3:

Single Stage Core Performance Metrics

Total execution cycles = 28

Average CPI = 2.54545

Instructions per cycle = 0.392858

Five Stage Core Performance Metrics----------

Number of cycles taken: 38

Cycles per instruction: 3.45455

Instructions per cycle: 0.289473

```
Single Stage Core Performance Metrics------------------------------
Number of cycles taken: 28
Cycles per instruction: 2.54545
Instructions per cycle: 0.392858

Five Stage Core Performance Metrics------------------------------
Number of cycles taken: 38
Cycles per instruction: 3.45455
Instructions per cycle: 0.289473
```

4) What optimizations or features can be added to improve performance? (Extra credit)

The following optimizations or features can be added to improve performance in a processor:

- Resource constraints result in structural hazards which occur when several processes must be carried out sequentially rather than concurrently. Restrictions on memory or register file ports during multi-cycle processes may be the cause of these. This can be resolved by increasing the processor's resources, speeding up the circuitry, or improving the pipelining procedure.

- By increasing the number of pipeline steps, or the depth of pipelining, processor performance can be enhanced. As a result, each stage's processing of logic will be reduced, improving clock rate and throughput in the process.

- One major factor affecting processor performance decrease is branch misprediction latency. This problem can be resolved by substituting arithmetic or lookup operations for the branch instructions, which will avoid adding control flow hazards.

- Achieving nearly perfect balance among the five stages to alleviate time constraints arising from the slowest phase.

- Minimizing the necessary overhead between stages for the storage and retrieval of essential data.

5) Compare the results from both the single stage and the five stage pipelined processor implementations and explain why one is better than the other.

METRIC	SINGLE STAGE PROCESSOR	MULTI STAE PROCESSOR
Execution time	Higher Execution Time.	Lower Execution time.
throughput	Low throughput	High Throughput
Hazards	No hazards will occur.	Control, data or structural hazards may occur.
Cycles	Low total no of cycles	High total no of cycles
CPI and IPC	Low CPI, High IPC	High CPI, low IPC
Execution	One instruction per cycle is executed	Multiple instruction are executed parallelly in a single cycle.

Advantages of a single-stage processor compared to a five-stage pipelined processor:

a) A single-stage processor eliminates structural, control, or data hazards, as there is no resource conflict or inaccurate memory access.

b) There is no need for overhead to store and access data between stages.

Advantages of a five-stage pipelined processor compared to a single-stage processor:

a) The presence of five pipeline stages reduces the amount of logic processed, leading to an improved clock rate and increased processor throughput.

b) In a single-stage processor, the cycle time is determined by the total time required to process each instruction sequentially. If there are m instructions, each taking n seconds, the total processing time is (m * n) seconds. However, in a five-stage processor, the cycle time is influenced by the slowest stage, approximately (m * n)/5, as there are 5 stages. Consequently, even considering the slowest stage as (m * n)/5 seconds, it is faster than the single-stage processor.

For example, in testcase 1:

Assuming the execution time of a single-stage processor is n seconds, in a five-stage processor with 5 stages, the time taken for execution is n/5 seconds.

Metric	Singlestage processor	Multistage processor
Execution time	40*n seconds	46 * n seconds
Instruction(approx)	40	31
Cycles	40	46
IPC	0.9750009	0.847824
CPI	1.02564	1.17949