Unit - 2

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Transistor

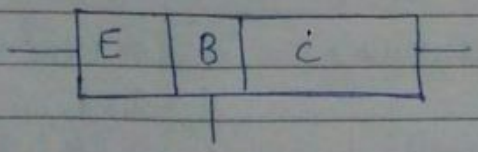
- **Unipolar Junction Transistor** (current only due to majority carriers)
  - → Field Effect Transistor (FET)
  - → Junction field Effect Transistor (JFET)
  - → Metal Oxide Semiconductor field Effect Transistor (MOSFET)
- **Bipolar Junction Transistor**
  - npn
  - pnp

Transistor is a three terminal device
→ Base : lightly doped
→ Emitter : Heavily doped
→ Collector : Moderately doped

Collector area > Emitter area > Base area
BJT has 2 depletion regions:
One b/w emitter & base ; Another b/w base & collector

★ For both npn & pnp transistors, $I_E = I_B + I_C$

∵ I_B is very small, I_E & I_C are nearly equal, however $I_E > I_C$



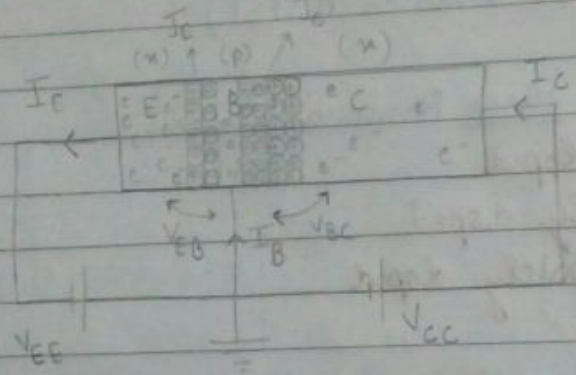
★ A transistor is a semiconductor device used to amplify or switch electronic signals & electrical power
It can be used to both conduct & modulate electric current or voltage

BJT → Transferred resistance transistor

Bipolar — both e^- & holes contribute to current

Junction — 2 junctions are formed J_E & J_C

Region	Emitter-base junction	Collector-base junction	Application
Active	Forward biased	Reverse biased	Amplifier
Cut-off	Reverse biased	Reverse biased	off-switch
Saturation	Forward biased	Forward biased	On-switch
Inverse Active	Reverse biased	Forward biased	—



★ width of BE depletion region < width of CB depletion region (because emitter is heavily doped)

Working of npn

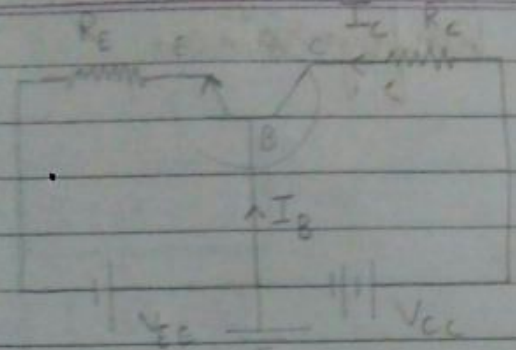
in active mode, $J_E \rightarrow$ F.B & $J_C \rightarrow$ R.B.

J_E ⟨low resistance⟩ $V_i = I \times R_i$ (R_i very small) → small input voltage

J_C ⟨∞ resistance⟩ $V_o = I \times R_o$ (R_o very high) → high output voltage

emitter current → e^- from emitter cross the junc & recombine with holes in the base. Base is very thin & lightly doped so most of the e^- will pass to the collector side & then to the +ve terminal of external dc source. This constitutes collector current

to constitute base current

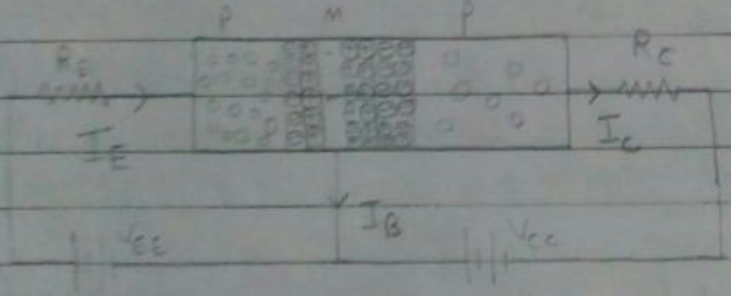


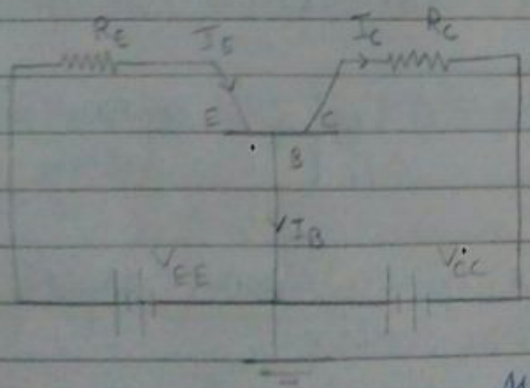
$$I_E = I_B + I_C$$

★ e^- are majority carriers.

Collector current is larger than base current

Working of pnp (in Active region)





$J_E \rightarrow$ F.B

$J_C \rightarrow$ R.B

Holes in emitter flow towards base (Emitter current)

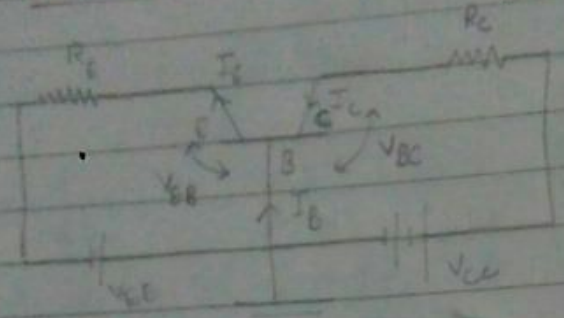
Very few holes combine with e^- in base (Base current)

Most holes pass to the collector & then to -ve terminal of external dc source (collector current)

$$I_E = I_B + I_C$$

★ Holes are majority carriers

Common Base configuration



$$I_E = I_B + I_C$$

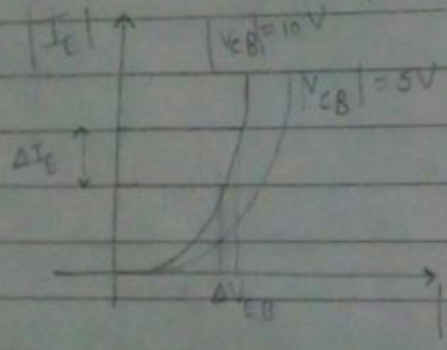
$$\alpha = \frac{I_C}{I_E} \quad [\alpha < 1]$$

$$\alpha \approx 0.96 - 0.99$$

α → current Amplification factor

Input Characteristics :-

Graph b/w input current I_E & input voltage V_{EB} at constant output voltage V_{CB}



$I_E = I_B + I_C$

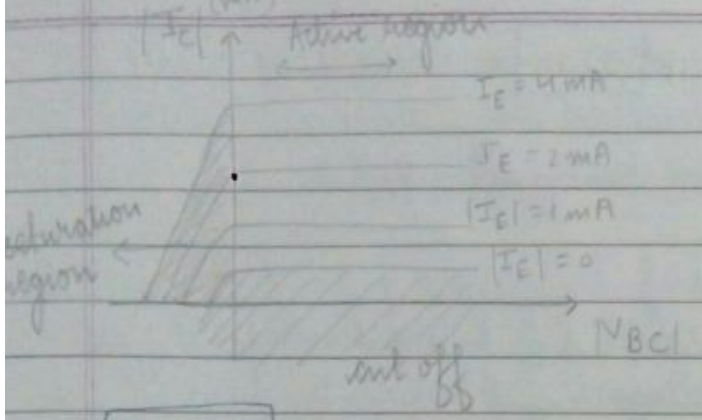
if V_{CB} ↑, I_C ↑ hence I_E ↑

Dynamic Input resistance, $r_i = \frac{\Delta V_{BE}}{\Delta I_E}$ ⟨ for constant output voltage ⟩

After the cut-in voltage, emitter current ↑ rapidly for small ↑ in emitter base voltage.
Thus, input resistance is very small.

Output Characteristics

Graph b/w output current I_C & output voltage V_{BC} at constant input current I_E.



The output characteristic has 3 basic regions:
→ Active
→ cut off
→ Saturation

ACTIVE:
$J_E \rightarrow$ F.B & $J_C \rightarrow$ R.B.

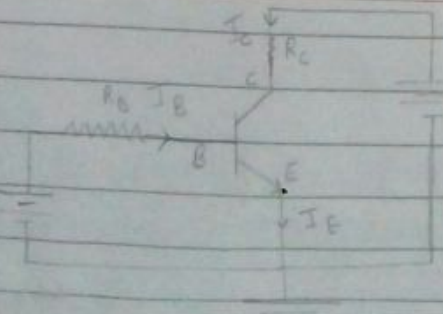
★ collector current is approximately equal to emitter current & transistor works as an amplifier
collector current is almost constant
dynamic output resistance, $r_o = \frac{\Delta V_{CB}}{\Delta I_C}$
Output resistance is very high

★ collector current is almost independent of collector - base voltage V_{CB}

SATURATION: J_E & J_C are F.B.
collector current is independent of ~~I_C~~ V_{BC}

CUT-OFF: J_E & J_C are R.B.

Common Emitter Configuration



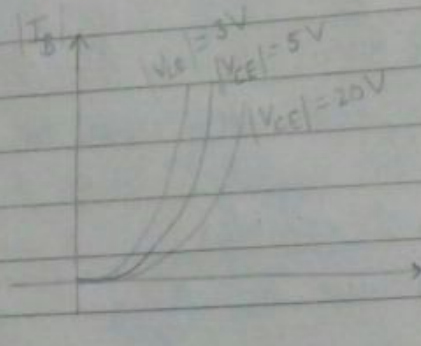
$I_E = I_B + I_C$

Current Amplification factor $\boxed{\beta = \frac{I_C}{I_B}}$ $\boxed{\beta > 1}$

DC Analysis → $\beta_{dc} = \frac{I_C}{I_B} = h_{fe}$

INPUT CHARACTERISTICS:

Graph b/w input current I_B & input voltage V_{EB} at constant output voltage V_{CE}



$I_B = I_E - I_C$

so if $V_{CE} \uparrow$, $I_C \uparrow$ & $I_B \downarrow$

Dynamic input resistance, $\boxed{R_i = \frac{\Delta V_{BE}}{\Delta I_B}}$ at constant V_{CE}

OUTPUT CHARACTERISTICS:

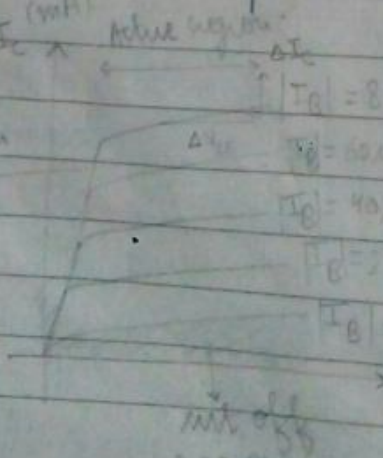
Graph between output current I_C & output voltage V_{CB} at constant input current I_B.

V_{BB} → fixed to V

& $V_{CC} = 0$

→ J_E → F.B. & J_C → F.B

→ Transistor is in saturation region & acts as closed switch



Change in collector emitter voltage causes little change in collector current for constant base current I_B

∴ Output dynamic resistance is high

$$\left[R_o = \frac{\Delta V_{CE}}{\Delta I_C} \right] \text{ for constant } I_B$$

Output characteristics consist of 3 regions:

① ACTIVE REGION

$J_E \rightarrow$ F.B. $J_C \rightarrow$ R.B.

② SATURATION REGION

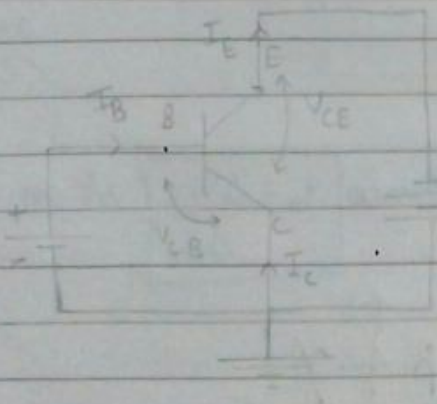
$J_E \rightarrow$ F.B. $J_C \rightarrow$ F.B.

The saturation value of V_{CE} usually ranges b/w 0.1 V to 0.3 V.

③ CUT-OFF REGION:

J_E & J_C are R.B Region below $I_B = 0$

Common Collector Configuration



Input is applied b/w base & collector

INPUT CHARACTERISTICS: Graph b/w input current I_B & input voltage V_{CB} at constant output voltage V_{CE}

Current Amplification factor $\left[\gamma = \frac{I_C}{I_B} \right]$

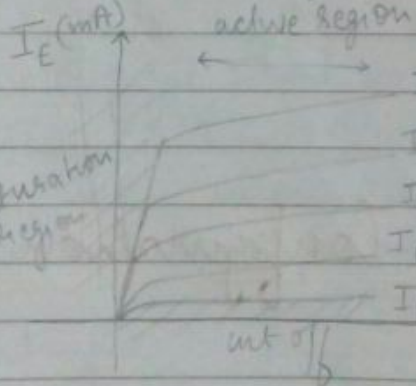
$V_{CE} = V_{CB} + V_{BE}$

★ For fixed V_{CE}, as V_{CB} ↑ width of depletion region ↑ I_C ↑ & due to this the effective base width ↓ & I_B ↓

For fixed V_{CB}, as V_{CE} ↑ or V_{BE} ↑, I_B ↑ because more & more e^- are pushed by the emitter terminal

Dynamic input resistance, $r_i = \frac{\Delta V_{CB}}{\Delta I_B}$ (for constant V_{CE})

OUTPUT CHARACTERISTICS: Graph b/w output current I_E & output voltage V_{CE} at constant input current I_B



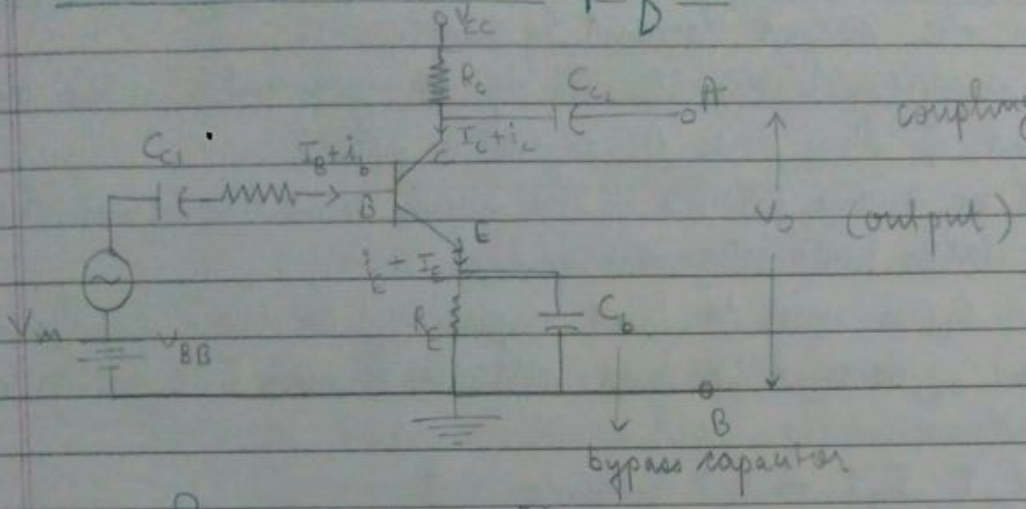
$I_E \approx I_C$
∴ Output graphs are same. (CE & CC)

Dynamic output resistance, $r_o = \frac{\Delta V_{CE}}{\Delta I_E}$ (at constant I_B)

★ Relationship b/w α, β & γ:

★ $\beta = \frac{\alpha}{1-\alpha}$ ★ $\gamma = 1 + \beta$

Common Emitter Amplifier



V_{BB} & V_{cc} are biasing (DC) voltages. They bias the transistor in such a manner that $I_E \rightarrow$ F.B. & $I_c \rightarrow$ R.B.

$I_b + i_b$ → due to AC voltage (V_{in})

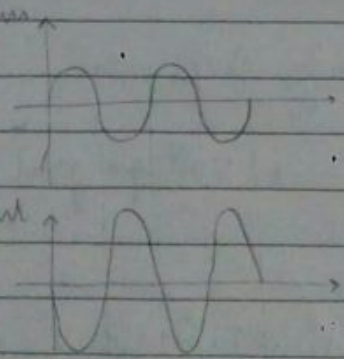
As $v_{in} \uparrow$, $i_b \uparrow \rightarrow i_c \uparrow$ [as $i_c = \beta i_B$ & $\beta > 1$]

$\therefore |i_c R_c| \uparrow = |V_o|$

I_E becomes more F.B. $\quad V_o = -i_c R_c = -\beta I_B R_c$

★

★ In common emitter amplifier, input & output are 180° out of phase



DC signals are just for biasing. Amplification of ac signal takes place.

★ Common Emitter is the only configuration in which input & output are 180° out of phase [applying KVL]

R_E is used to control the current so it cannot be removed

★ Coupling capacitor : It is used to link only the AC signal from one circuit element to another
The capacitor blocks the DC signal from entering the next element & thus only AC signal is passed.
→ Used in audio circuits as the speech is an AC signal when user talks into the microphone
★ C_{c1} is used to link input V_{in} to the base terminal
★ C_{c2} is used to link collector terminal to the output

As $V_m \uparrow$, $I_B \uparrow \rightarrow I_C \uparrow$ & hence $I_E \uparrow$
∴ There is a significant drop over resistor R_E $\{R_E \cdot I_E\}$ which in turn reduces the output across AB
★ So a bypass capacitor is connected in parallel to provide a lower impedance path to current. So majority of the current flows through the bypass capacitor C_1
Drop across R_E is very less & significant output is obtained

$$\boxed{\Delta i_B = \frac{\Delta V_{in}}{R_B}}$$

$$\boxed{\beta \Delta i_B = \Delta i_c = \beta \frac{\Delta V_{in}}{R_B}}$$

$$\Delta V_o = -\Delta i_c R_C = -\beta \frac{R_C}{R_B} \Delta V_{in}$$

$$\boxed{\frac{\Delta V_o}{\Delta V_{in}} = -\beta \frac{R_C}{R_B}} \rightarrow \text{voltage gain } A_v$$

Single Stage Amplifier : Single V_{in} is amplified to get

★ Gain of n^{th} stage amplifier : β^n

FET

JFET

MOSFET (Metal Oxide semiconductor Field Effect Transistor)

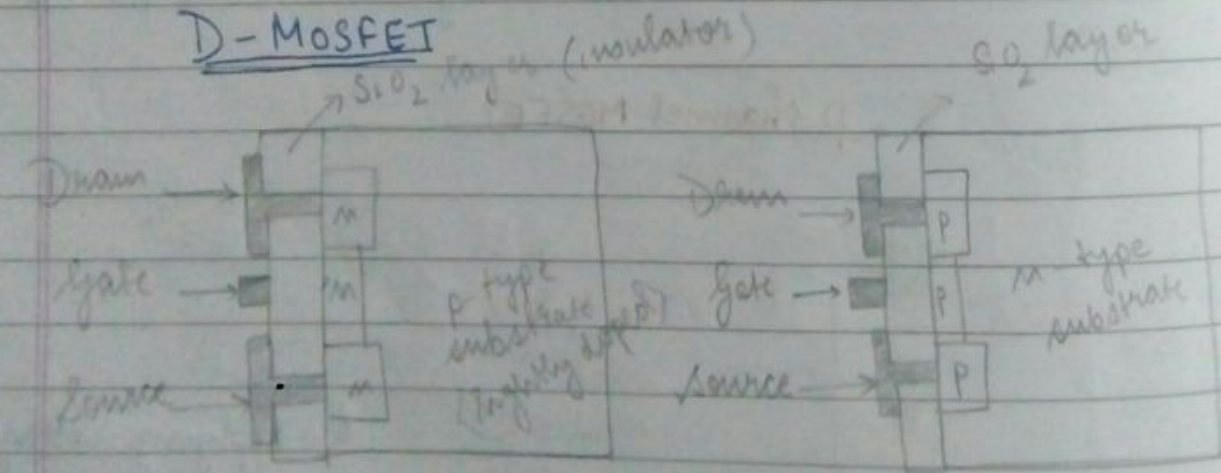
D-MOSFET (Depletion MOSFET)

E-MOSFET (Enhancement MOSFET)

or Insulated Gate Field Effect Transistor (IG-FET)

Gate does not have direct connection with channel.

D-MOSFET



n channel

p channel

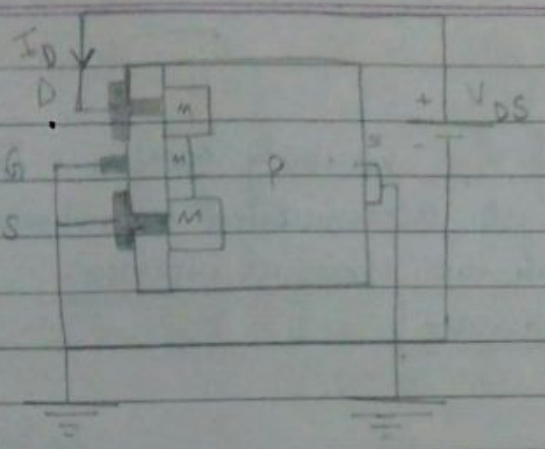
In n channel, p type
contribute in curre

★ Case-II : $V_{GS} <$

Due to negative
leave the channe
holes & combine
Hence, no of e
∴ I_D decreases

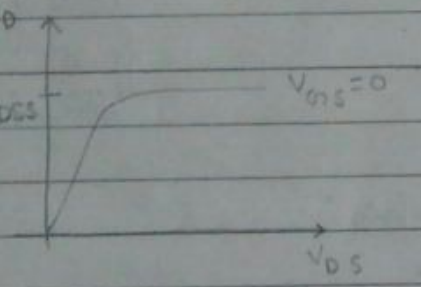
I_D ↑

★ FETs are known as unipolar because current flows only due to one type of charge carriers.



! On ↑ V_{DD}, e^- flow ↑

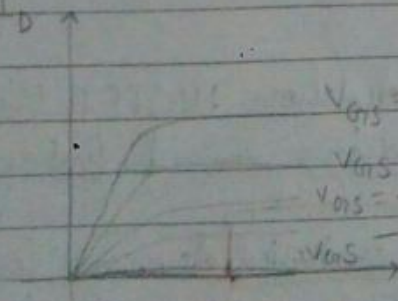
★ Case - I: $V_{GS}=0$



In n channel, p type substrate is very lightly doped & does not contribute in current flow.

★ Case - II: $V_{GS}<0$

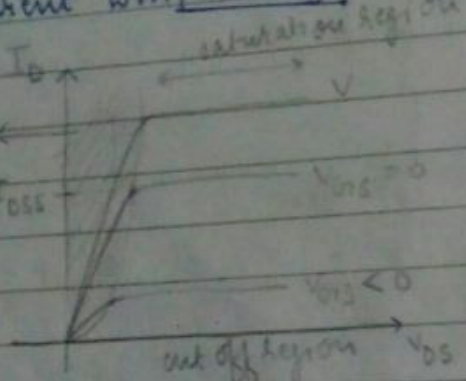
Due to negative polarity of gate, the e^- will get repelled & leave the channel & go into the substrate leaving behind holes & combine with holes in the p type substrate.
Hence, no of e available in the channel will decrease.
∴ I_D decreases



★ V_{GS} for which I_D is zero is known as pinch off voltage
$V_{GS}=V_p$

* Case III : $V_{GS} > 0$

Due to +ve polarity of V_{GS}, minority carriers → ~~holes~~ e^- from p type substrate will get accumulated in n channel.
Hence, the no of e^- in the channel increases.
∴ I_D current will increase



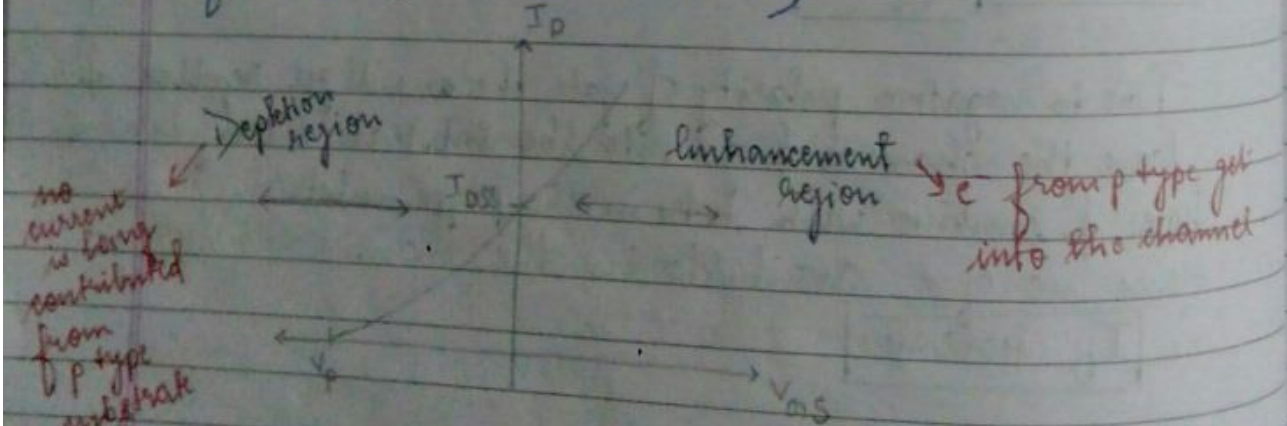
* Ohmic region (or linear region) is the locus of the points taken just before the current is saturating.

Transfer Characteristics :

input voltage → V_{GS}

output current → I_D

* Relationship b/w V_{GS} & I_D will give Transfer Characteristics of MOSFET (n channel - D MOSFET)



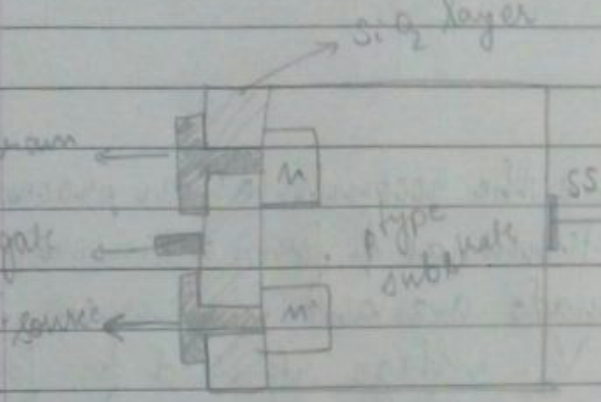
* In depletion MOSFET, there are 2 regions: Depletion region & Enhancement region

* FETs are voltage controlled devices. Controlling by changing the input voltage V_{GS}
V_{GS} is controlling the output current I_D.

Current eqⁿ for n channel D-MOSFET:

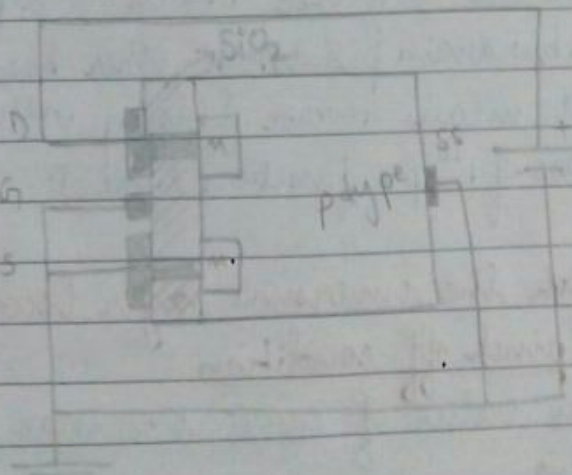
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

E-MOSFET:



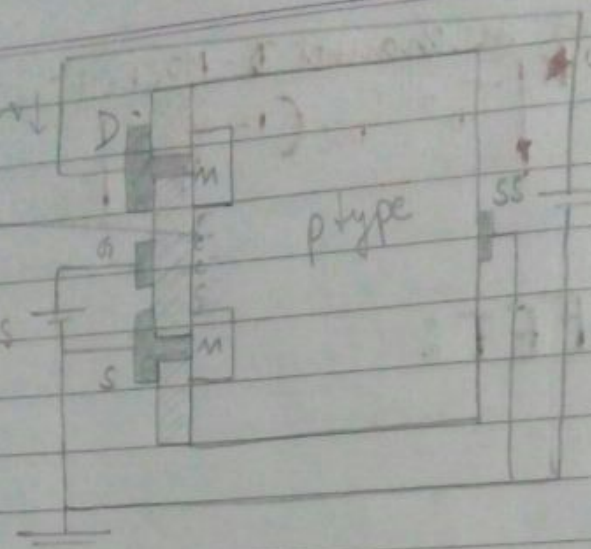
i) $V_{GS} = 0$

There is no path for current to flow as there is no channel available. (circuit is not complete)



ii) $V_{GS} > 0$

Due to +ve polarity of battery, holes in substrate get repelled & the e⁻ get attracted. Due to insulator, e⁻ cannot cross so they accumulate & form a visual channel



As V_{GS} is ↑ the e^- overcome the recombination process & get attracted by the +ve terminal & form an inversion layer ∴ ★ A channel is made available for current to flow

★ The minimum value of V_{GS} voltage required for forming a channel is known as Threshold Voltage (V_T)

After $V_{GS} = V_T$, V_{DS} battery is connected.

Two pn junctions are formed n channel & p substrate

★ Both pn junctions are reverse biased & depletion layer is formed → b/w drain & substrate, other b/w source & substrate

As V_{DS} is increased, it means reverse biasing voltage is ↑

∴ Depletion region in case of 1st pn junction diode ↑.

(max)

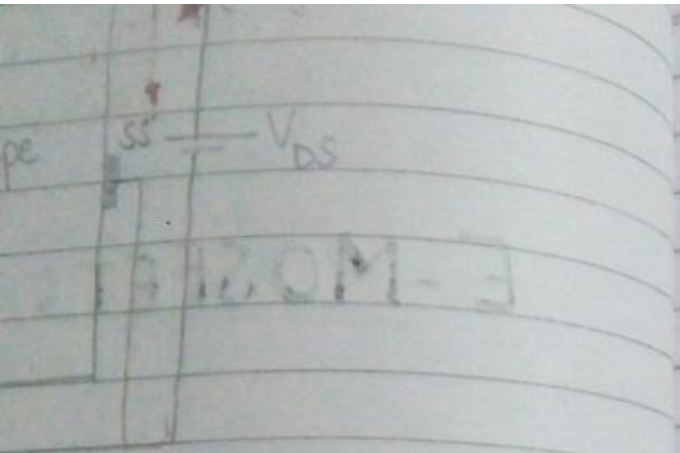
★ Value of V_{DS} for which the inversion layer becomes very narrow is known as ★ pinch off condition

At pinch off condition, value of current is max or we can say it is saturating

$$V_G - V_D = V_{GS} - V_{DS}$$

As V_D ↑, voltage b/w gate & drain ↓

Pinch off: ★ $\boxed{V_{DS(sat)} = V_{GS} - V_T}$



he recombination process
inal & form an inversion
available for current to flow
voltage required for forming
hold Voltage (V_T)
connected.

ned n channel & p substrate
verse biased & depletion
substrate, other b/w source & substra
verse biasing voltage is ↑

→ Channel is created at V_T ⟨Threshold voltage⟩

★ Beyond V_{DS} ⟨or pinch off⟩, the ~~of~~ inversion layer is detached ⟨or loses contact⟩ with upper n channel. The 2 n channel won't remain connected by inversion layer.

★ But current will still flow as V_{GS} is suffucent & e⁻ have gained enough K.E. to move from 1 n region to another & in this case current will become constant.

★ $I_D = K(V_{GS} - V_T)^2$

↓ device constant

★ MOSFETs are <u>voltage controlled resistors</u>.

★ In Ohmic region ⟨or linear region⟩ MOSFET can be used as Voltage controlled resistor.

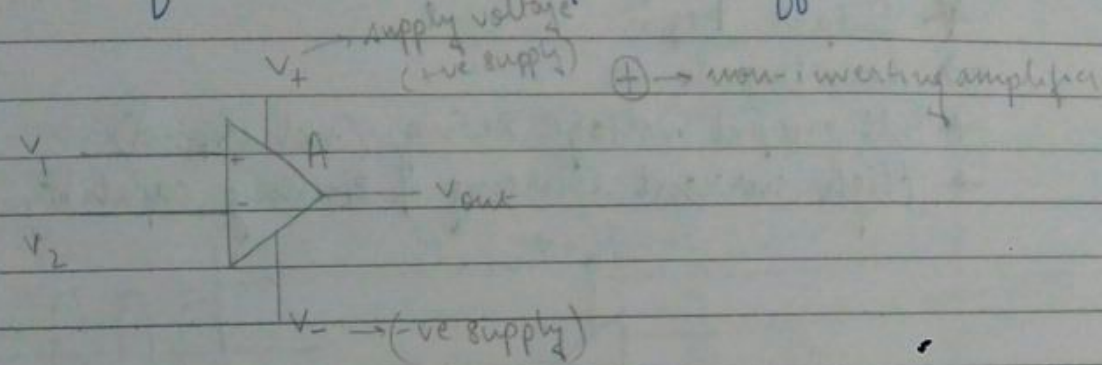
→ <u>V_{GS}</u> controls the <u>inversion layer</u>. It controls the amount of charge carriers in the inversion layers.

MOSFET → Common Drain, Common Source, Common Gate } configurations

ideally, op-amp → ∞ input resistance device
input current → 0

Operational Amplifier

can be used for add^n, subt^n, integeration, differentiation



2 input → V_1 & V_2 (1 inverting, 1 non inverting)
2 supply → V_+ & V_- (1 inverting, 1 non inverting)
1 Output → V_{out} ★
A → open loop gain (no feedback is taken → no output component is given to input
Effective input: $V_1 - V_2$

Operational or Differential Amplifier
↓ (diff b/w V_1 & V_2)

$$V_{out} = A(V_1 - V_2)$$

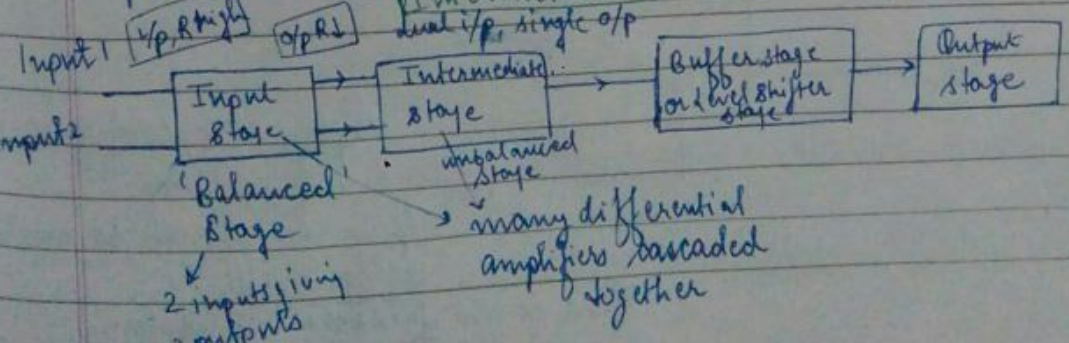
if V_2 is grounded: $V_{out} = AV_1$ → non inverted

if V_1 is grounded: $V_{out} = -AV_2$ → inverted

★ If input is given on +ve terminal, output will be in phase (not inverted)

If input is given on −ve terminal, output will be 180° out of phase (inverted)

Internal Block Schematic of op amp



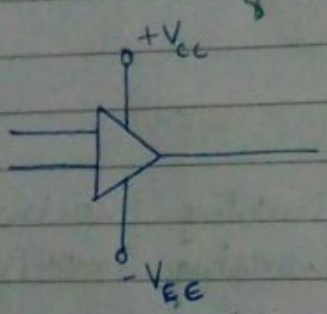
★ In stage 1 & 2, Dc level is rising as capacitors are not attached.

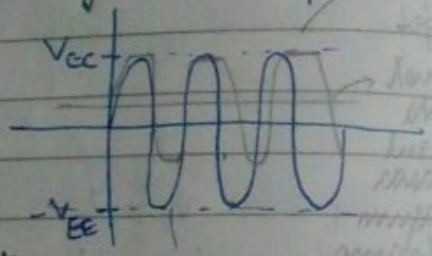
★ Output Reg:

→ Low impedance

→ Full output voltage swing (not clipped)

→ High current sourcing & sinking capability





★ Output voltage is going to lie b/w V_{cc} & $-V_{EE}$

a Push pull complementary Amplifier

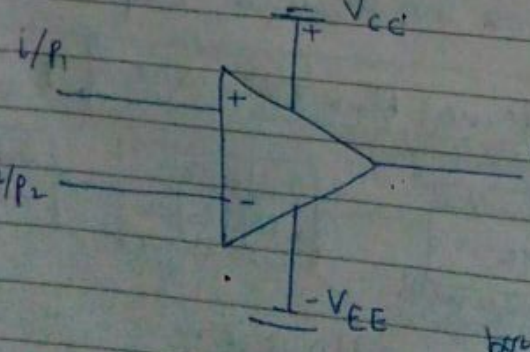
→ Push pull Transistors are used in output stage.

→ First op-amps were created using vacuum tubes.

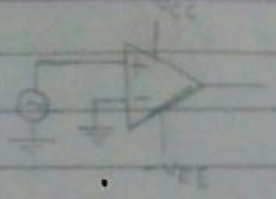
→ Nowadays, op-amps use BJTs, MOSFETs cascaded together

★ Gain of op amp → 10^5 or 10^6

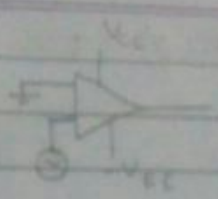
Input Stage → Differential Amplifiers
Intermediate Stage → Multistage Cascaded Amplifiers
Buffer Stage → Buffers



Open loop configuration of op-amp
o/p is not taken to input as feedback.
There is no feedback mechanism.



Non inverted output



Inverted output

★

$$V_o \propto (V_1 - V_2) \rightarrow \boxed{V_o = A_d (V_1 - V_2)}$$

A_d → differential gain / open loop gain

$V_1 - V_2 = V_d$ → differential voltage

$$\rightarrow \boxed{V_o = A_d V_d}$$

Common Mode Gain ⟨A_c⟩

if $V_1 = V_2 \rightarrow V_o = 0$ → ideally

$\frac{V_1 + V_2}{2} \propto V_o$

★

$$\rightarrow \boxed{V_o = A_c \left\{ \frac{V_1 + V_2}{2} \right\}} \rightarrow \boxed{V_o = A_c V_c}$$

★

Practically, $\boxed{V_o = A_d V_d + A_c V_c}$, common mode voltage

In ideal scenario, $A_c V_c = 0$

∴ Ideally, $\boxed{V_o = A_d V_d}$

★ Common Mode Rejection Ratio ⟨CMRR⟩

The ability of an op amp to reject a common mode signal is expressed as a ratio known as CMRR (ρ)

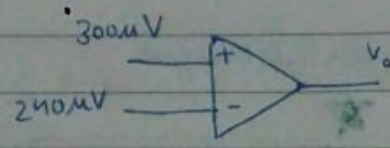
★ $\text{CMRR} \langle \rho \rangle = \left| \frac{A_d}{A_c} \right|$

Ideally, CMRR should be infinite because ideally A_c should be zero

★ CMRR is expressed in decibels ⟨dB⟩

$$CMRR(\rho) = 20 \log_{10}\left|\frac{A_d}{A_c}\right| \quad \text{in dB}$$

Q.



$A_d = 5000$

$CMRR = 10^5$

$V_o = A_d V_d + A_c V_c$

$= 5000\,(60)\times 10^{-6} +$

→ $CMRR(\rho) = 20 \log\left|\frac{A_D}{A_C}\right|$ { ∵ CMRR is not given in dB

→ $10^5 = 20 \cdot \left|\frac{A_D}{A_C}\right|$

$A_c = \frac{5000}{10^5}$

→ $V_o = 5000(60)\times 10^{-6} + 5000 \times 10^{-5}\left(\frac{240+300}{2}\right)$

$= 300.0135\,mV$

Ideal op amp characteristics :

(i) Open loop gain (A_{OL}) → ideally it should be ∞.

(ii) I/p impedance (R_{in}) → equivalent resistance which is measured at either of the 2 input terminals with the other terminal grounded

★ Ideally, R_{in} should be ∞.

(iii) O/p impedance (R_o) → equivalent resistance measured b/w output terminal of op amp & ground.

★ Ideally, R_o should be 0.

$\langle V_{ios} \rangle$

v) Input offset voltage : Even when both the input terminals are grounded, a small voltage occurs at the output.

★ V_{ios} should ideally be zero. (due to noise)

To make this zero, small -ve voltage is provided at one of the terminals.

vi) Input Bias current $\langle I_b \rangle$

Ideally, since i/p impedance is ∞, there should be no current flowing into the i/p terminals.
Practically, very small currents flow.

I_{b1} → Terminal 1 I_{b2} → Terminal 2

★

→ Bias current, $I_b = \frac{I_{b1} + I_{b2}}{2}$

Ideally, I_b should be zero

vii) Output offset voltage : Voltage existing at the output when inputs are zero due to input offset voltage & input bias current $\langle V_{oos} \rangle$ (Ideally, V_{oos} should be zero) ★

viii) Slew Rate : Max rate of change of output voltage with time ★

$S = \left. \frac{dV_o}{dt} \right|_{max}$ ★ Ideally ∞

unit : V/μs
voltage / microsecond.

(iii) ★ Power Supply Rejection Ratio $\langle PSRR \rangle$:

The ratio of change in input offset voltage due to change in supply voltage producing it. Keeping other power supply voltage constant ★

$PSRR = \frac{\Delta V_{ios}}{\Delta V}$

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or $PSRR = \frac{\Delta V_{IOS}}{\Delta V_{EE}}$ | V_{CC} constant

Ideally, PSRR should be zero

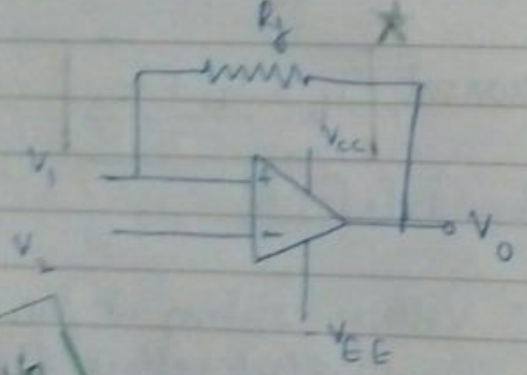
(11) Ideally, bandwidth should be ∞.

Virtual ground concept :

Ideal Behaviour: $I_{b_1} = I_{b_2} = 0$

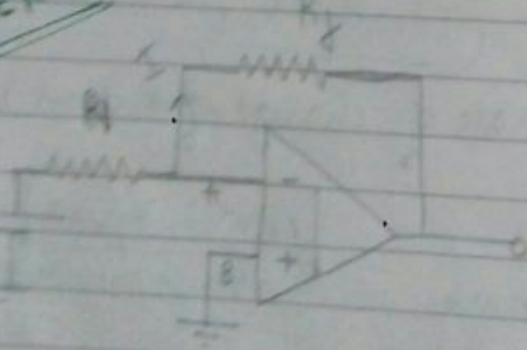
If any one of the input is grounded, then other is also virtually grounded

& both are virtually short



Closed Loop System

INVERTING AMPLIFIER



Feedback or Closed Loop System

→ o/p would be inverted as input is given on inverting terminal

→ $I_2 = 0$ { $\because R_2 \to \infty$ ideally }

→ $V_E = 0$ { $\because$ pt B is grounded }

By virtual ground concept, $V_A = 0$

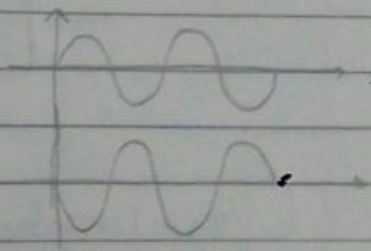
$I = \frac{V_{in} - V_A}{R_1}$ {input side}

$I = \frac{V_A - V_o}{R_f}$ {output side}

$V_A = 0$ [$\because V_B = 0$, by virtual ground concept]

Equating both:

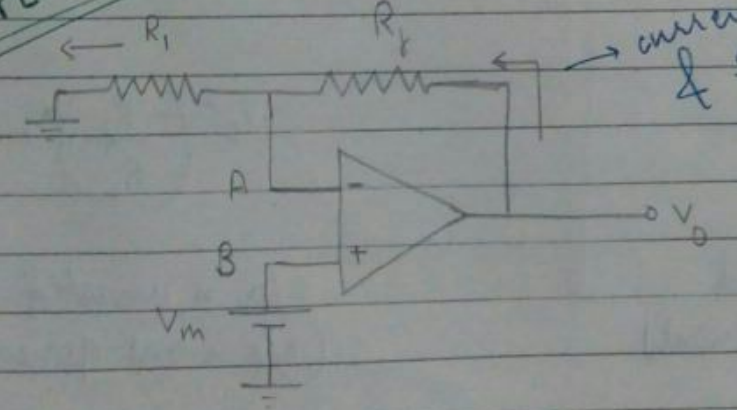
$$\frac{V_{in}}{R_1} = \frac{-V_o}{R_f}$$



$$\rightarrow \boxed{V_o = \left(\frac{-R_f}{R_1}\right) V_{in}}$$

↓ Amplification factor

NON-INVERTING AMPLIFIER



→ current direction is this because $I_b = 0$ & feedback from output is going here.

→ o/p would be non inverted as input is given on non inverting terminal

→ $V_B = V_{in}$

$V_A = V_B$ {By virtual ground or virtual short concept}

$$\rightarrow \boxed{V_A = V_B = V_{in}}$$

$I = \frac{V_o - V_A}{R_f} = \frac{V_o - V_{in}}{R_f}$ {output side}

$I = \frac{V_A - 0}{R_1} = \frac{V_A}{R_1} = \frac{V_{in}}{R_1}$ {input side}

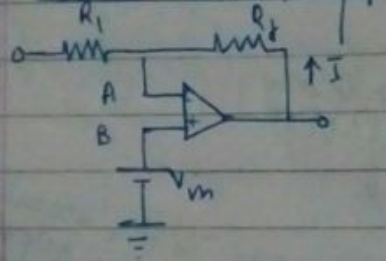
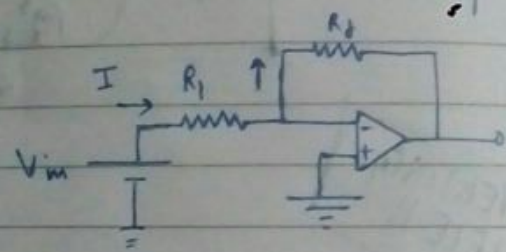
equating both:

$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{R_f} = V_{in}\left\{\frac{1}{R_1} + \frac{1}{R_f}\right\}$$

★

$$\boxed{V_o = \left(\frac{R_1 + R_f}{R_1}\right) V_{in}}$$

	Non-Inverting	Inverting
①		
②	$V_o = \left(\frac{R_1 + R_f}{R_1}\right) V_{in}$	$V_o = \left(-\frac{R_f}{R_1}\right) V_{in}$
③	o/p is non inverted (o/p is in phase with input)	o/p is inverted (o/p is out of phase, 180° shift)
④	Voltage gain always greater than one $\left\{1 + \frac{R_f}{R_1}\right\}$	voltage gain can be adjusted equal to, less than or more than 1. $\left\{\frac{R_f}{R_1}\right\}$

Ex: An op-amp is used in non inverting mode with $R_1 = 1\,K\Omega$; $R_f = 15\,K\Omega$, $V_{cc} = \pm 15V$. Calculate voltage for (i) $V_{in} = 150\,mV$ (ii) $V_{in} = 2\,V$

(i) $V_o = 2.4\,V$ for inverting : $V_o = -2.25\,V$

(ii) for inverting : $-15\,V$ (saturated output)

$\{0.9\,(-15)\}$

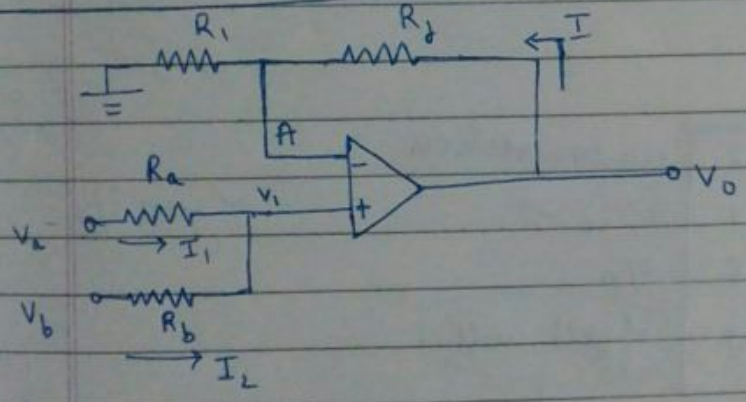
Ex 2. $R_1 = 1K\Omega$, $R_f = 12K\Omega$, $V_{cc} = \pm 15V$. Take output voltage when : (i) $V_{in} = 250mV$ (non-inverted)

(ii) $V_{in} = 3V$

(i) $V_o = (1+12) \times 250 \times 10^{-3} = 13 \times 25 \times 10^{-2} = 3.25$

(ii) $V_o = 13 \times 3 = 39\,V \rightarrow$ not possible

$V_o = 15V$ (saturated o/p)



$V_a = 2V$

$V_b = 4V$

$R_a = R_b = 1K\Omega$

& $R_f = 3K\Omega$

$R_1 = 1K\Omega$

$$I_1 = \frac{V_a - V_1}{R_a}$$

$$I_2 = \frac{V_b - V_1}{R_b}$$

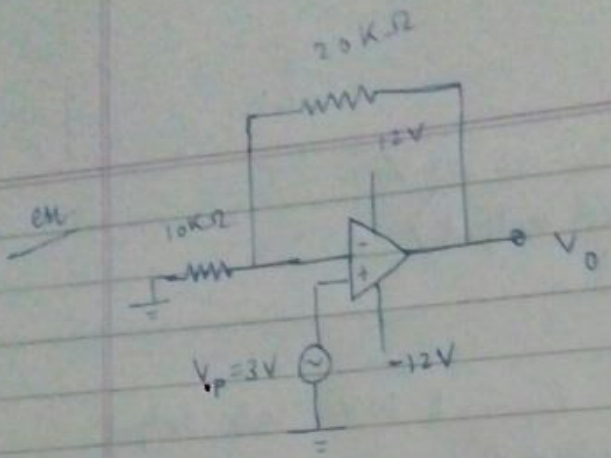
$\rightarrow I_1 + I_2 = 0 \rightarrow \frac{V_a - V_1}{R_a} + \frac{V_b - V_1}{R_b} = 0$

$$V_1 = \frac{V_a R_b + V_b R_a}{R_a + R_b}$$

$$= \frac{(2+4) \times 10^3}{2 \times 10^3} = 3\,V$$

$\rightarrow V_A = 3V$

$$\frac{V_o - V_A}{R_1} = \frac{V_A - 0}{R_1} \rightarrow \frac{V_o - 3}{3} = \frac{3}{1} \rightarrow \boxed{V_o = 12V}$$

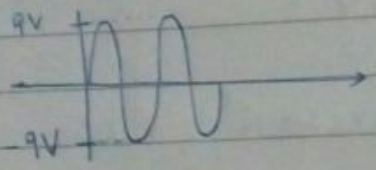


$$V_0 = \left(1 + \frac{R_f}{R_1}\right) V_m$$

$$= \left(1 + \frac{20}{10}\right) \times V_m$$

$$= 3 \times V_m$$

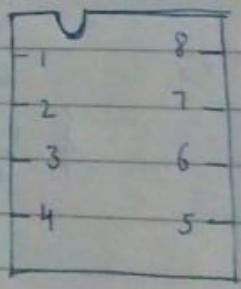
V_{pp} = 18V (peak to peak)



example of op amp:

IC-741 → 8 pin IC

I/O



✓ → 4 i/p

used to set input offset bias

7 pins are used, 1 is not used, 2 offset nulls

	Ideally	Practically
A_{OL}	∞	2×10^5
R_{out}	0	75Ω
R_{in}	∞	2MΩ
I_{bias}	0	20nA
V_{IOS}	0	2mV
Bandwidth	∞	1MHz
CMRR(p)	∞	

	Ideally	Practically
Slew rate	∞	0.5 V/μs
I_b	0	30 mA
PSRR	0	30 μV/V