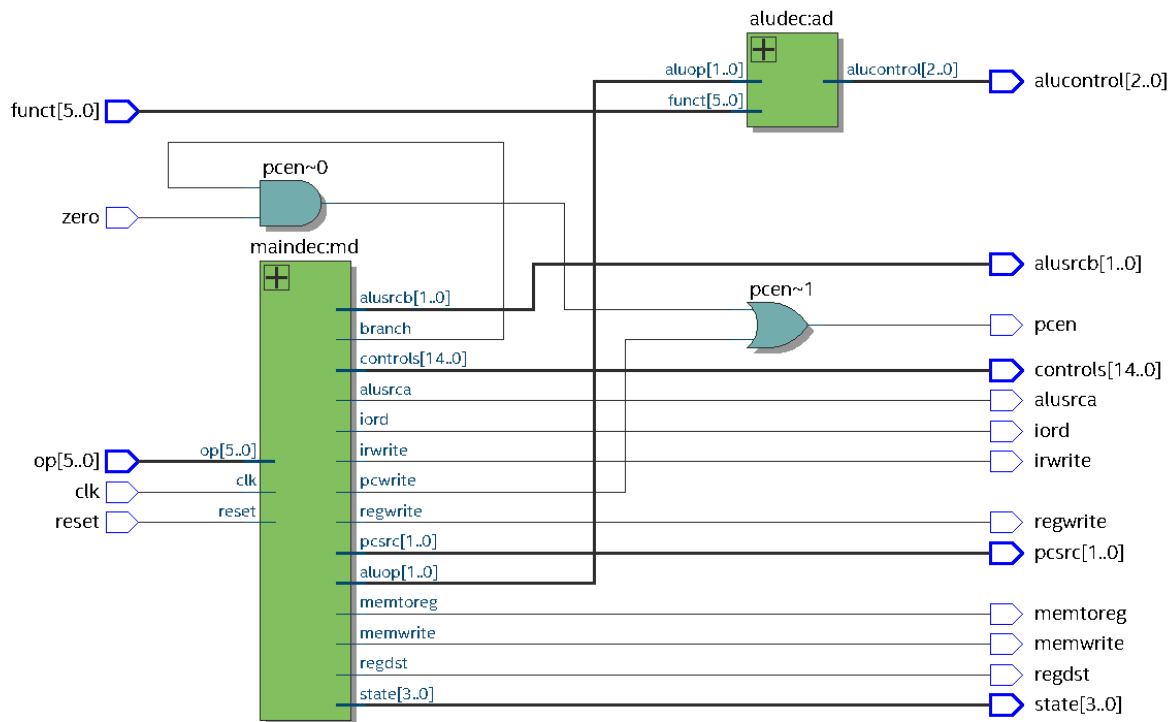
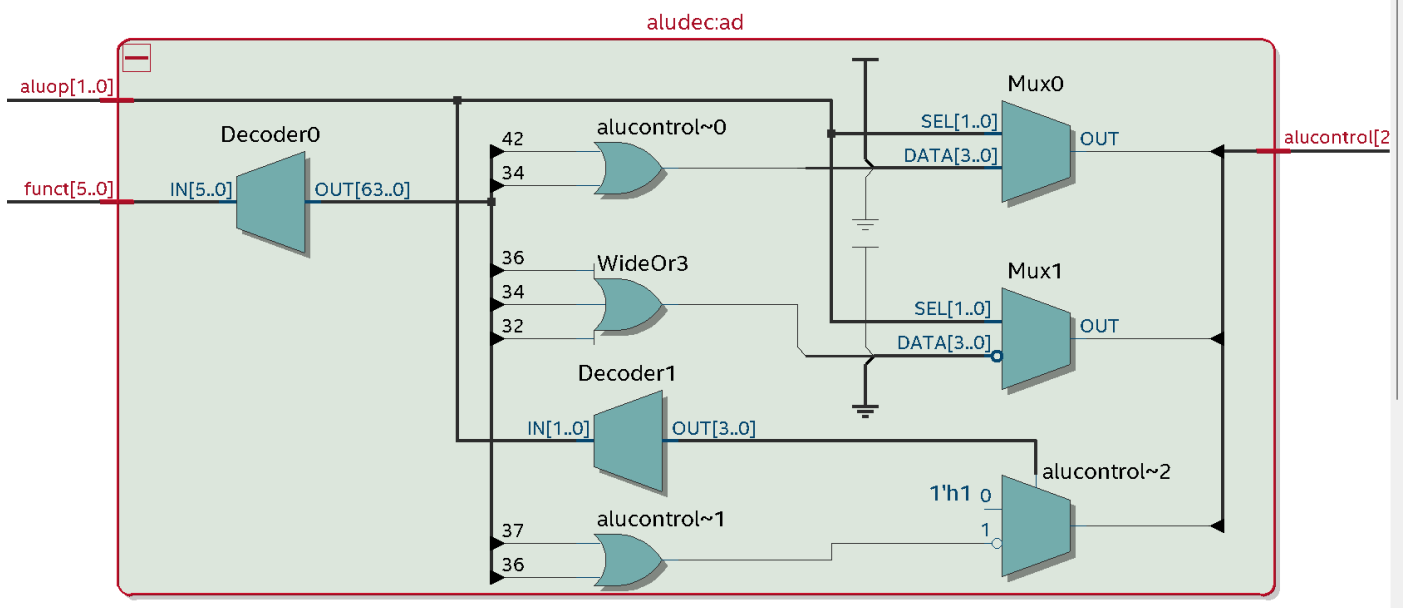


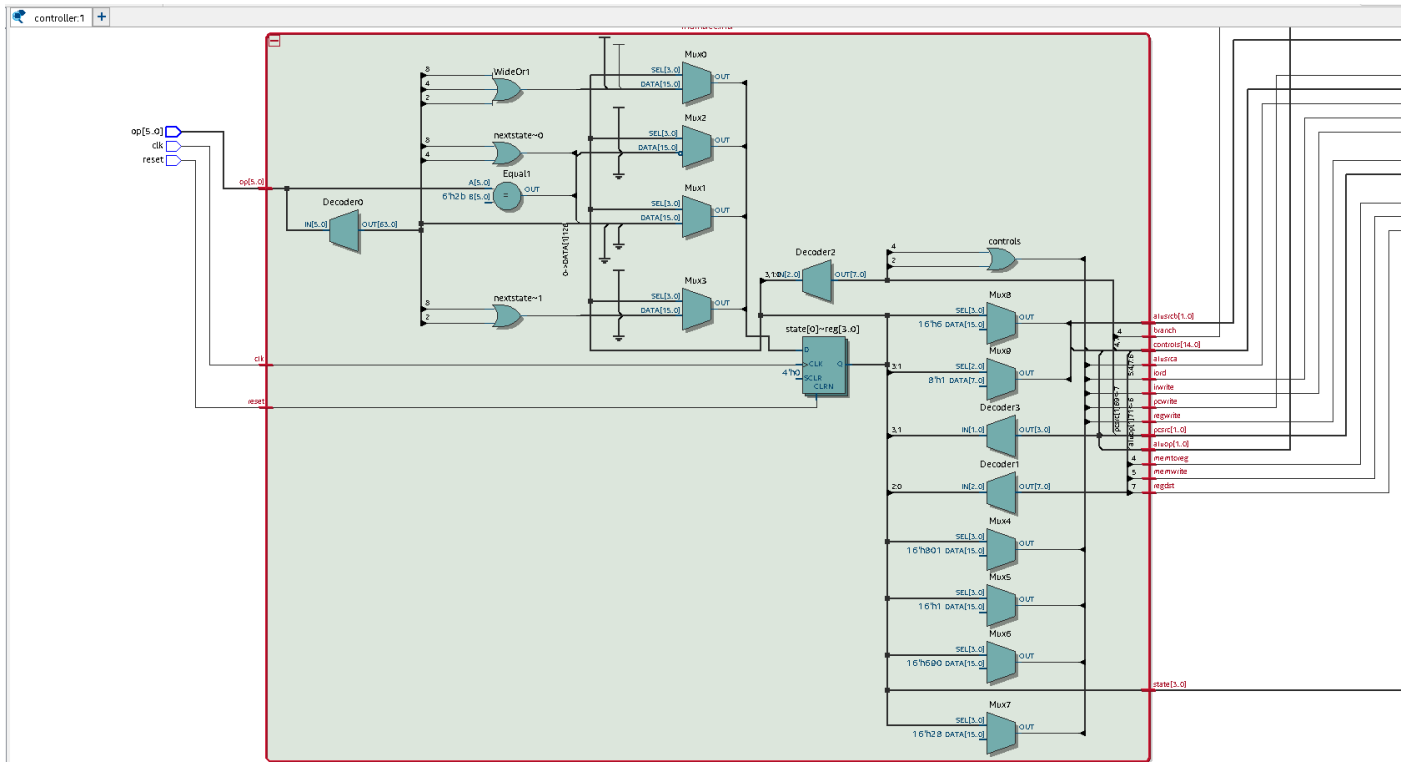
→ RTL PART-A



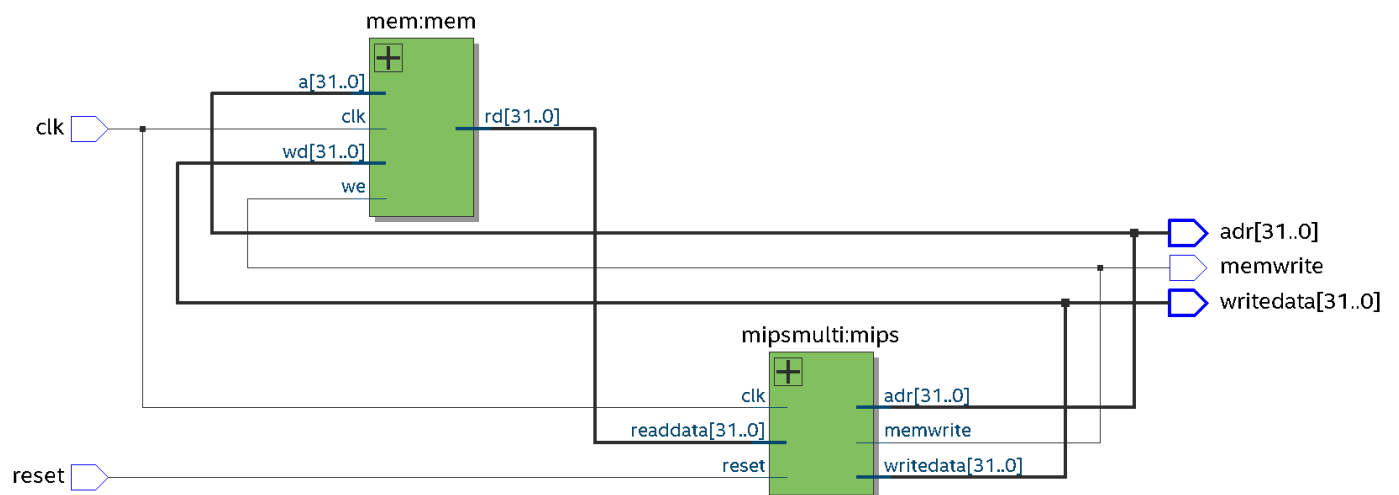
→ ALU-Decoder



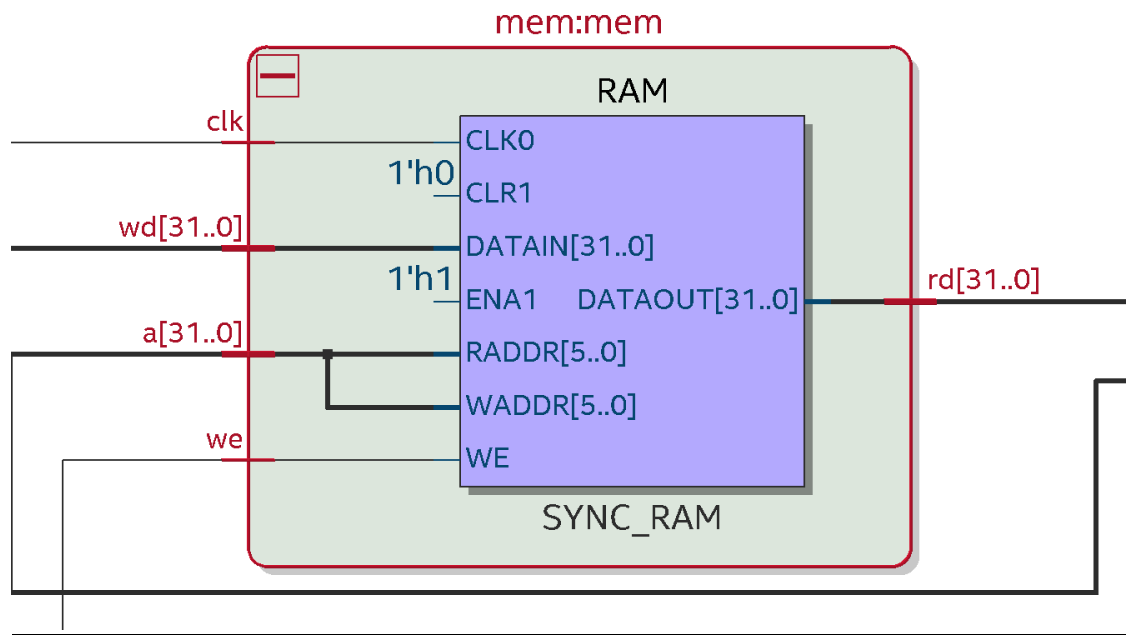
→ Main Decoder



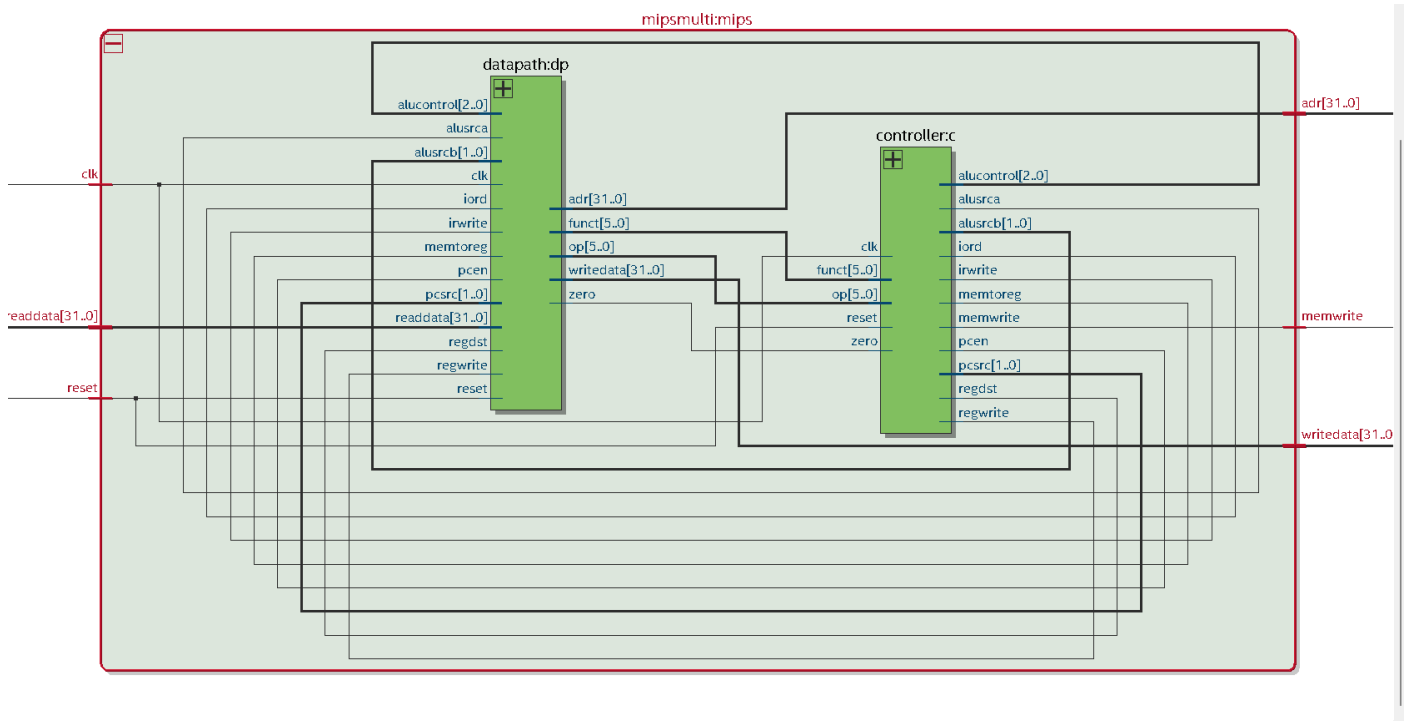
→ RTL PART-B



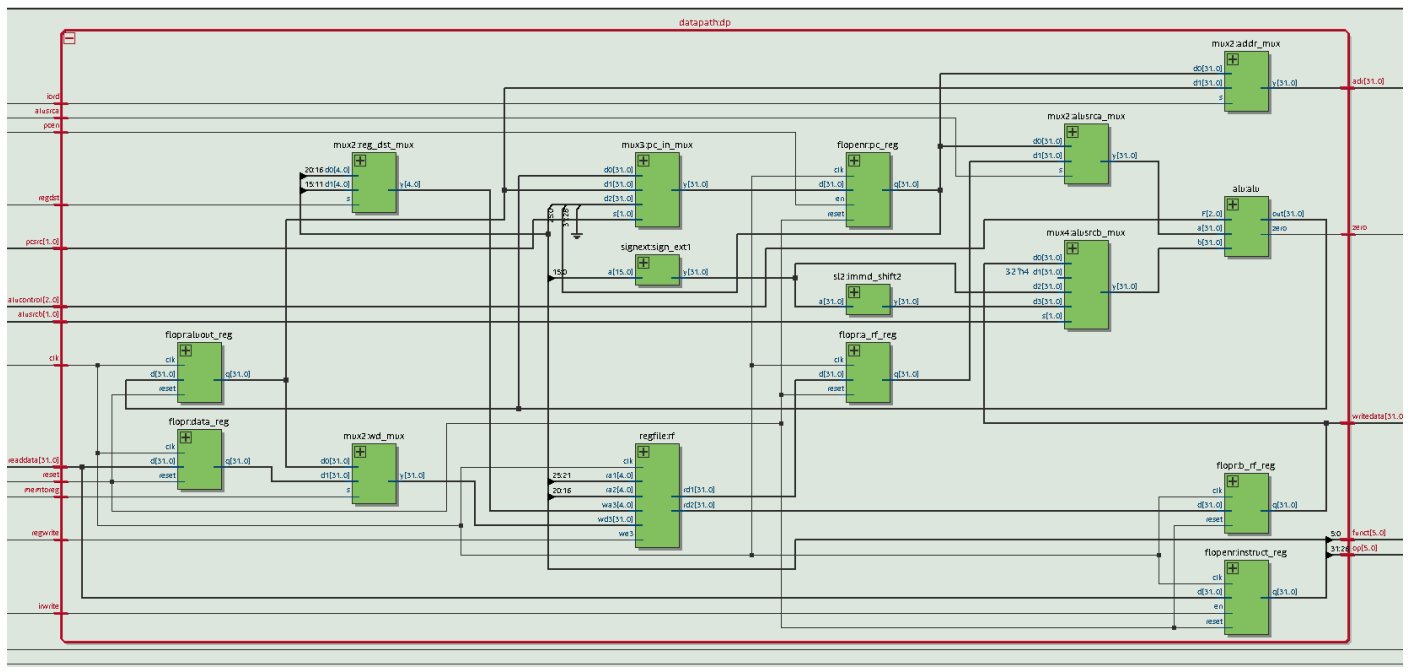
- MIPS MEMORY.



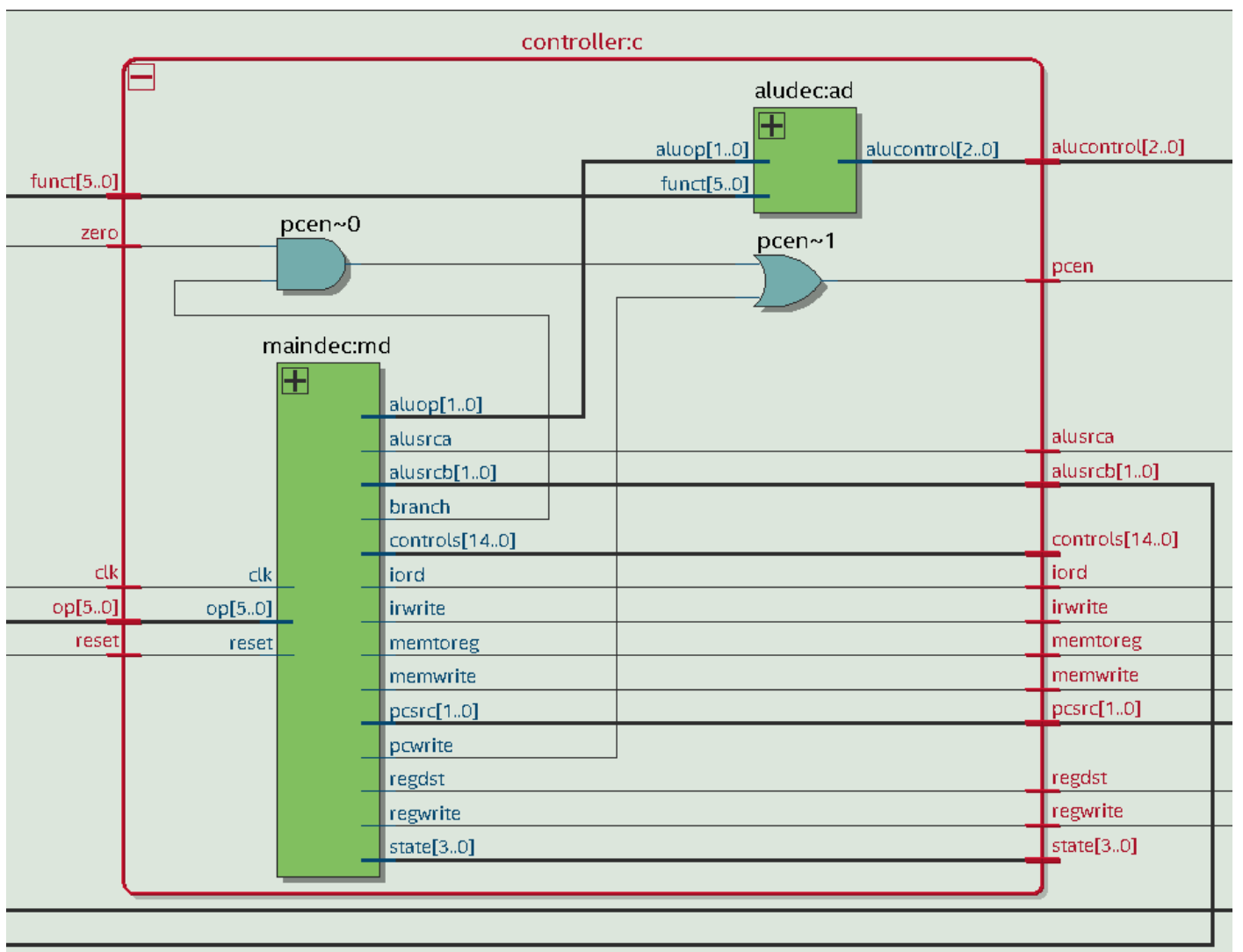
- MIPS.



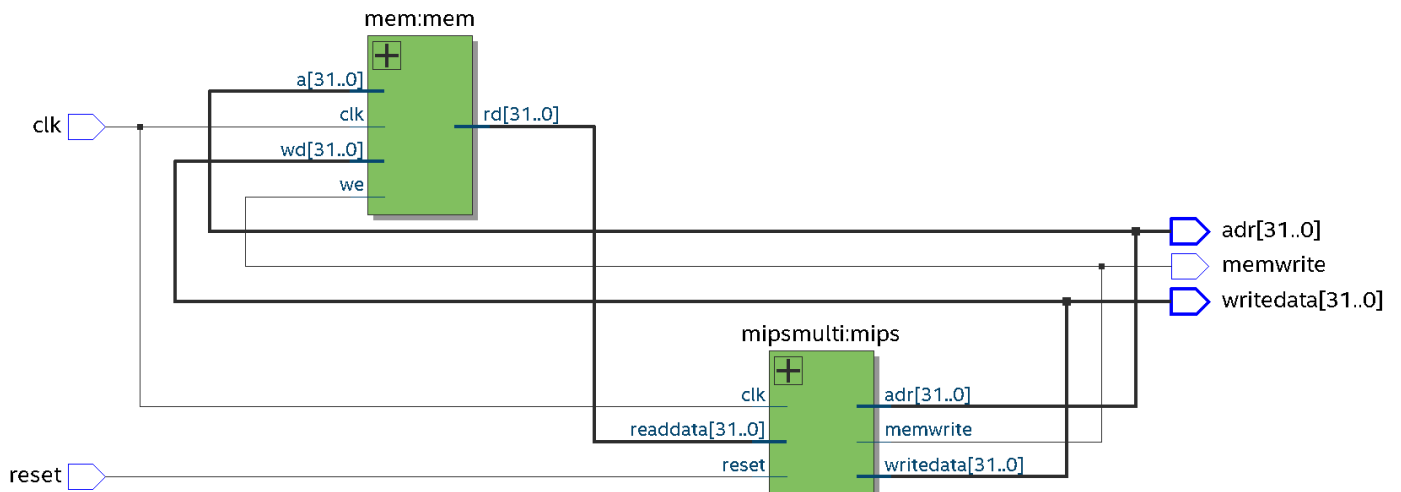
→ MIPS DATAPATH:



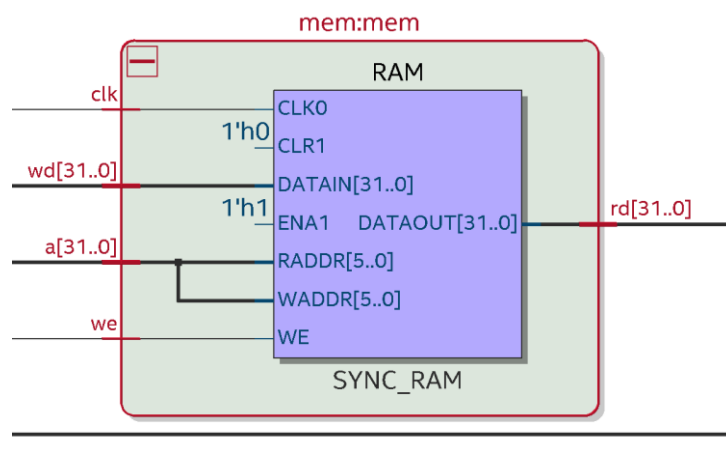
→ MIPS Controller



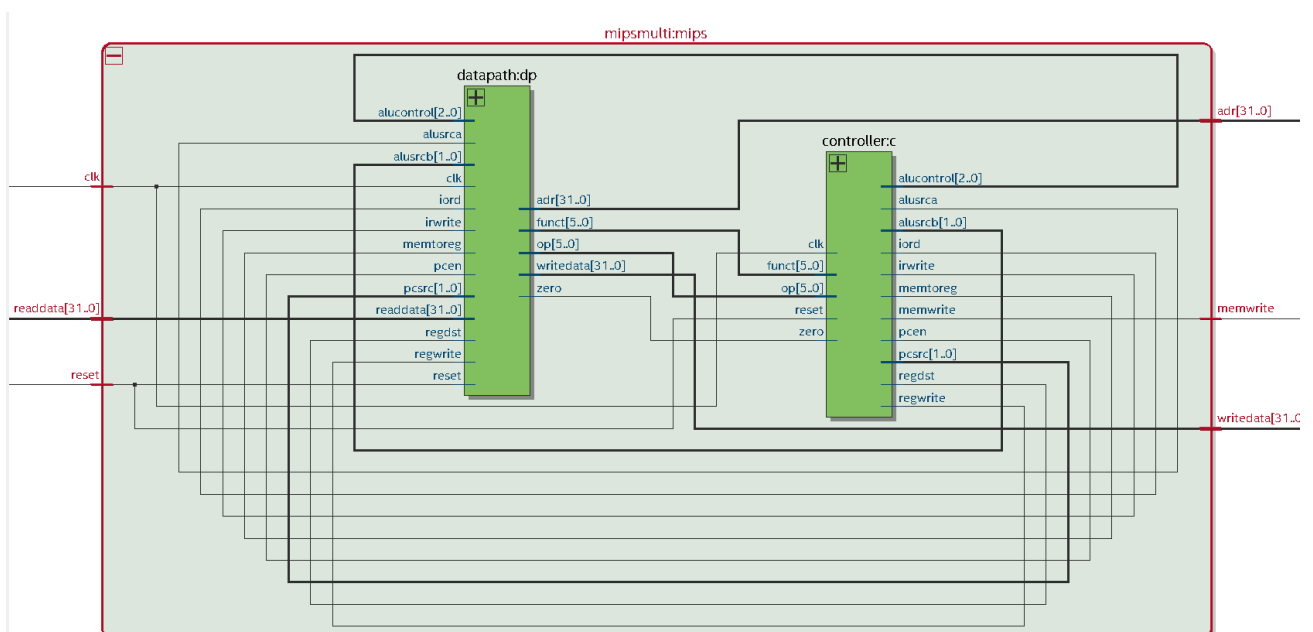
→ RTL PART C:-



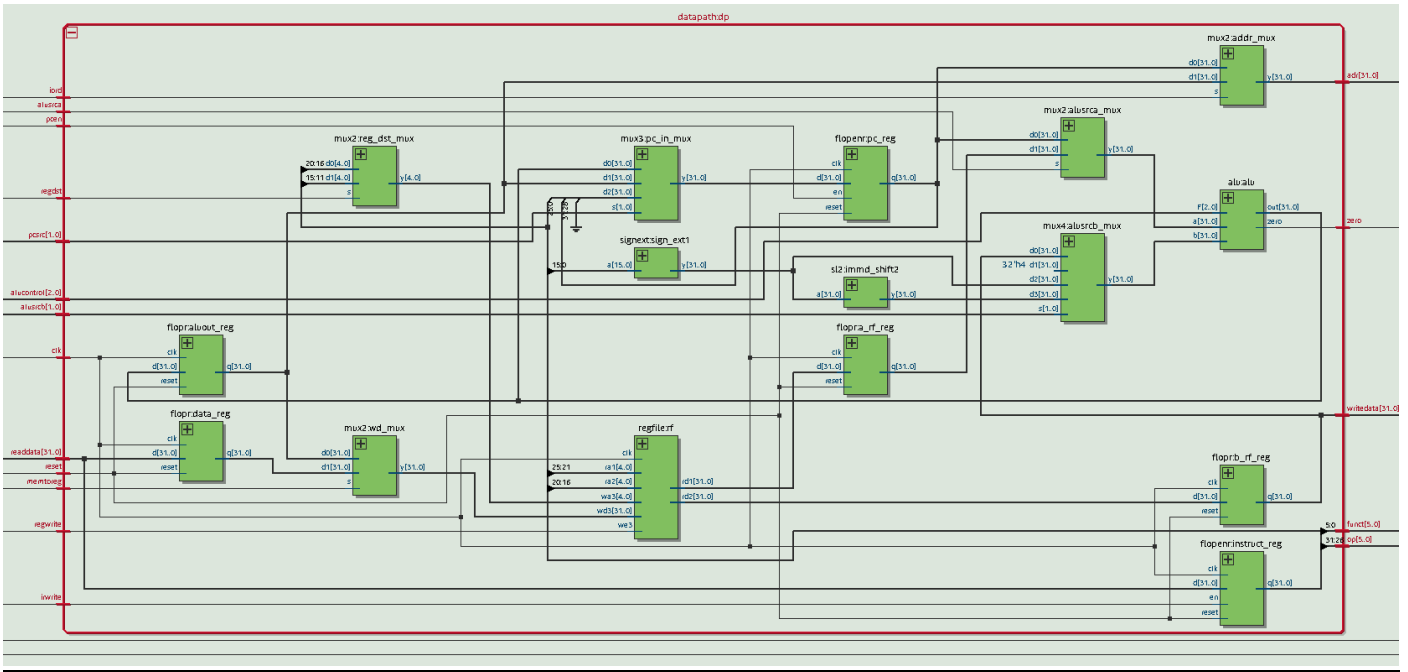
- MIPS MEMORY.



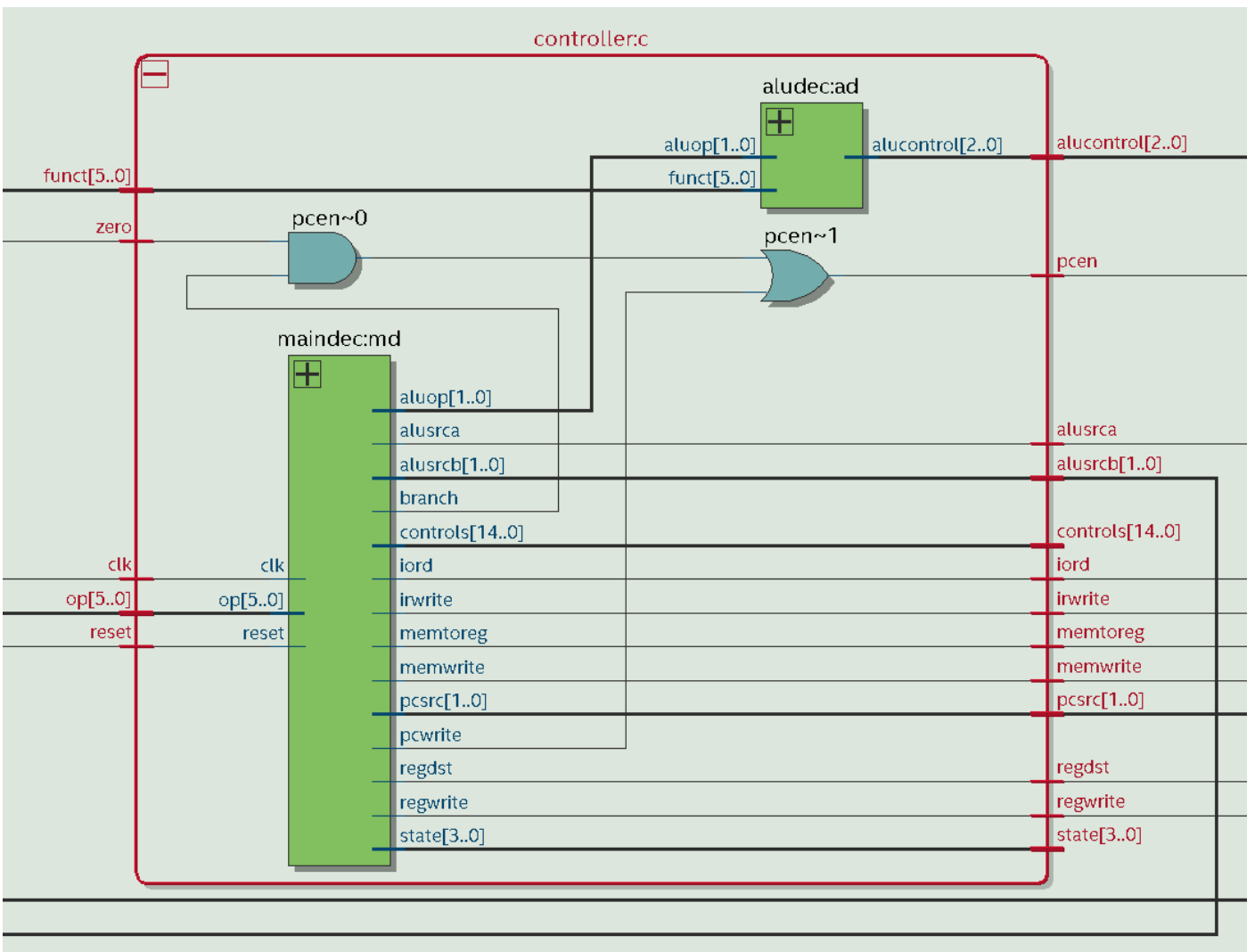
- MIPS.



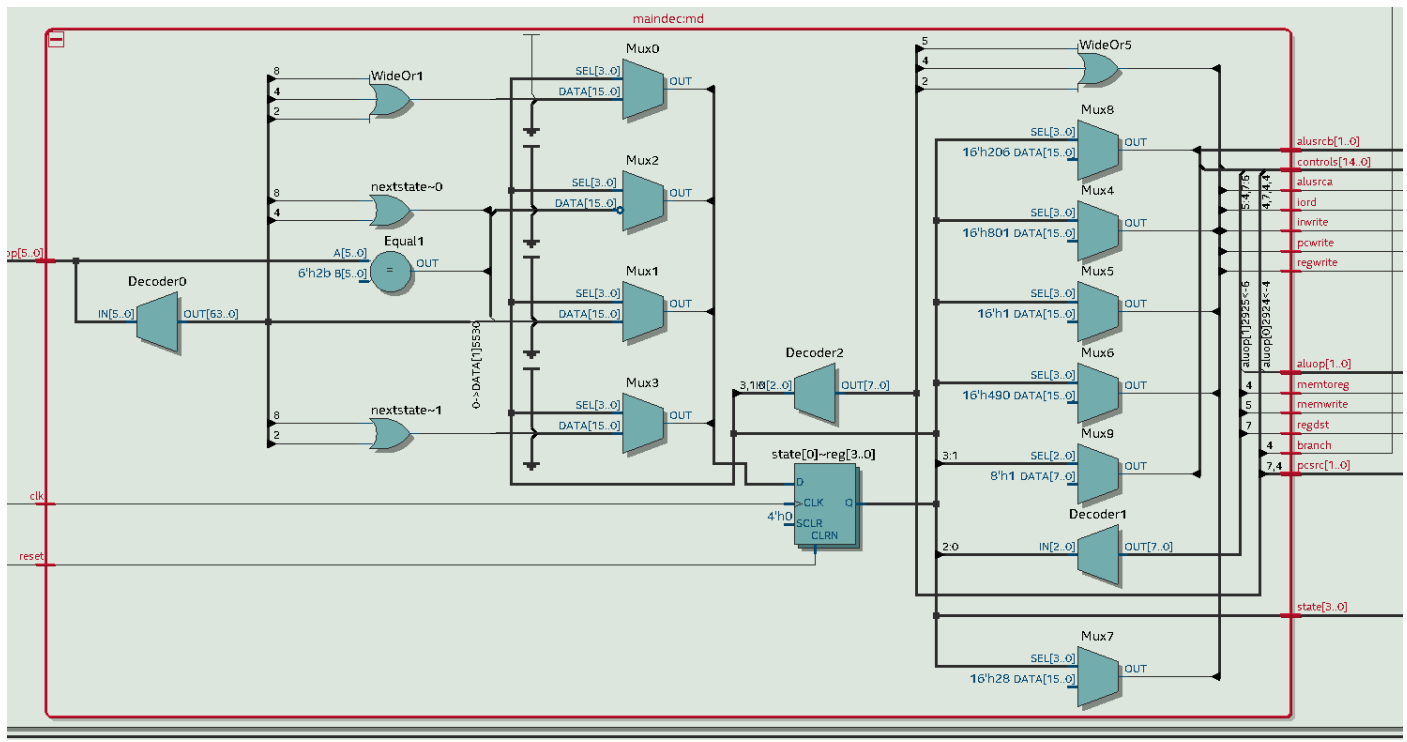
→ MIPS DATAPATH:



→ MIPS Controller



→ Main Decoder:



→ ALU Decoder:

