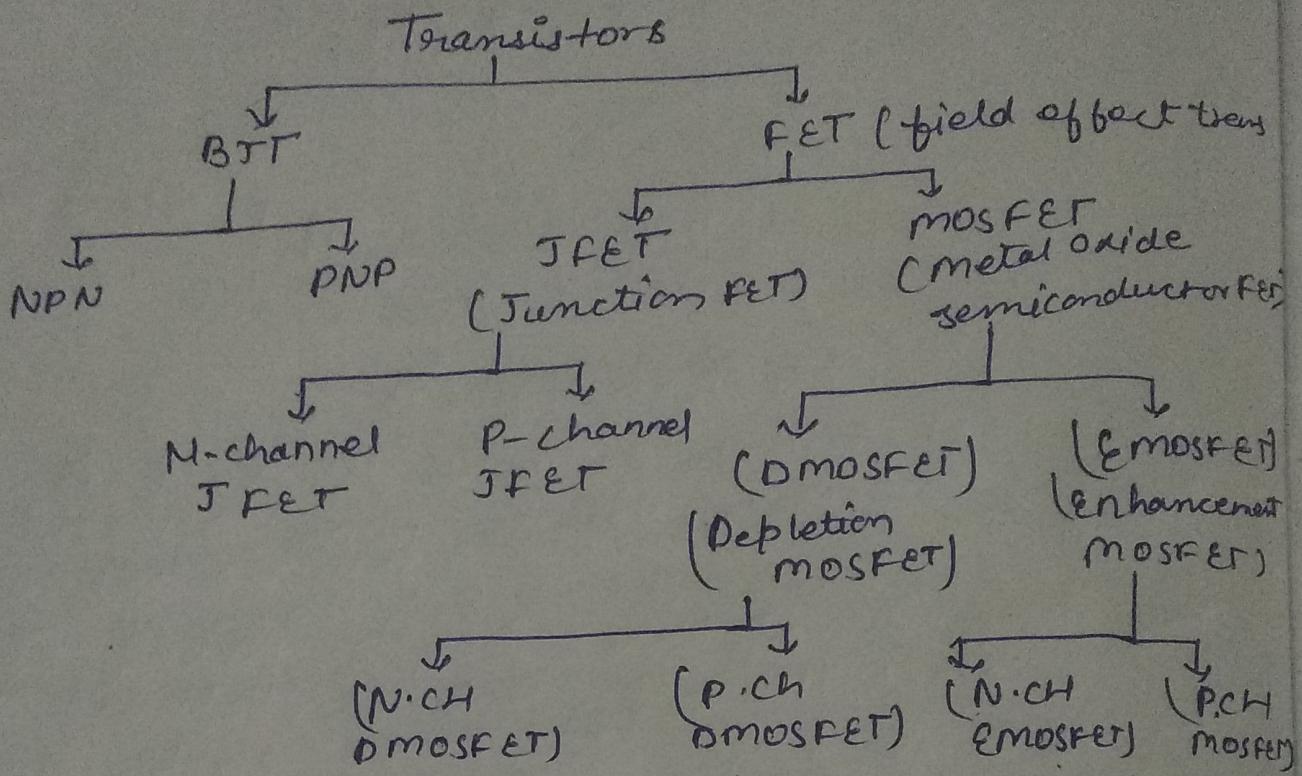


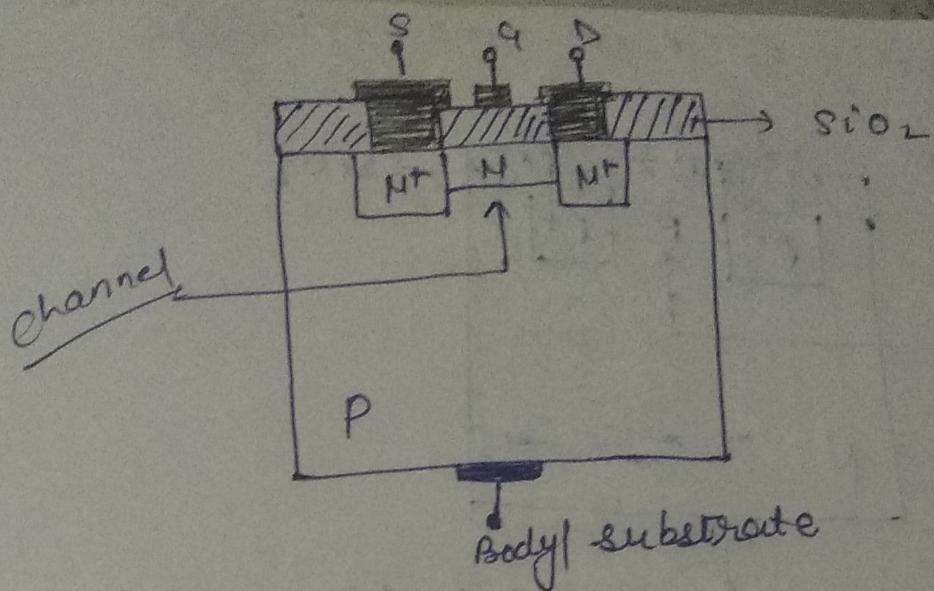
Unit - 3 MOSFET



MOSFET (IGFET) → A mosfet differs from a JFET in the sense that its gate terminal is electrically insulated from its channel. For this reason a mosfet is also called as insulated gate FET.

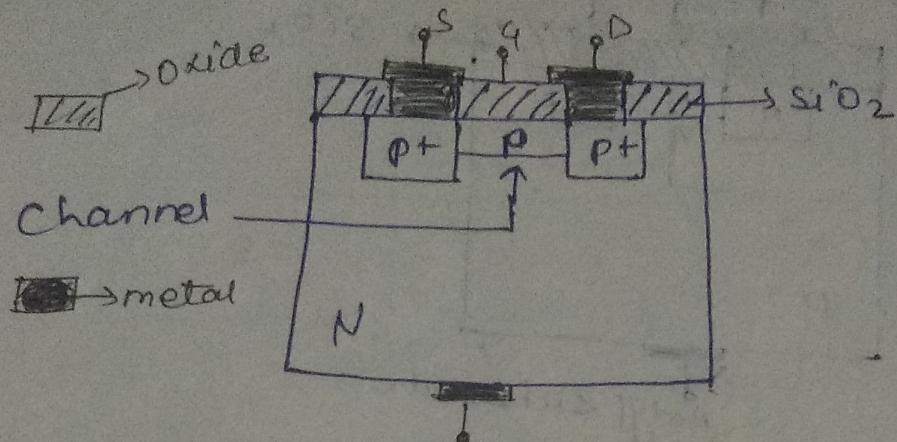
- Due to insulation of gate its input impedance is extremely high.
- mosfet are of two type :
 - i) DMOSFET (Depletion mosfet)
 - ii) EMOSFET (enhance mosfet)

Construction of N-CH-DMOSFET



- A block of P-type silicon form a substrate / body which provide support to the device.
- To heavily doped n-type region are created in this P-substrate.
- B/w two N+ region there is lightly doped n-type region which makes channel.
- A thin layer of silicon di-oxide is deposited along the surface.
- Metal contact at two N+ region form source and drain of the device.
- metal deposited on SiO₂ layer opposite two channel form gate terminal.
- * while going from the gate to the channel become across metal oxide and semiconductor in the sequence. That why we name it has MOSFET.

Construction of P-N-P MOSFET.

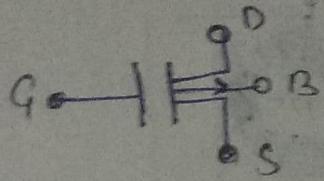


Body / substrate

- A block of n-type silicon from a substrate / body which provide support to the device.
- To heavily doped p-type region are created in this N-substrate.
- Between two P^+ regions there is lightly doped n-type region which make channel.
- A thin layer of silicon dioxide is deposited along the surface.
- Metal contact at two P^+ region form source and drain of the device.
- Metal deposited on SiO_2 layer opposite two channel form gate terminal.
- While going from the gate two channel become across metal oxide and semiconductor in the sequence that why we has ~~the~~ name it has MOSFET.

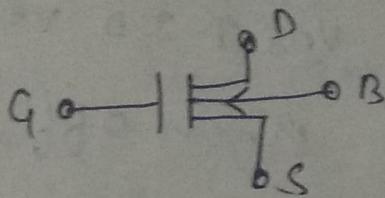
Circuit symbol

①



P-CH-D MOSFET

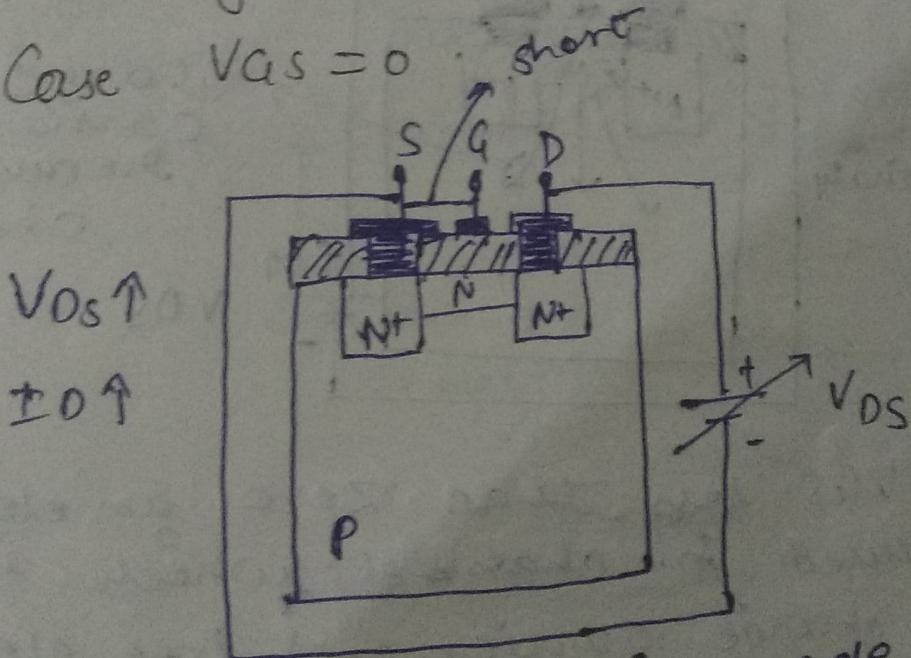
②



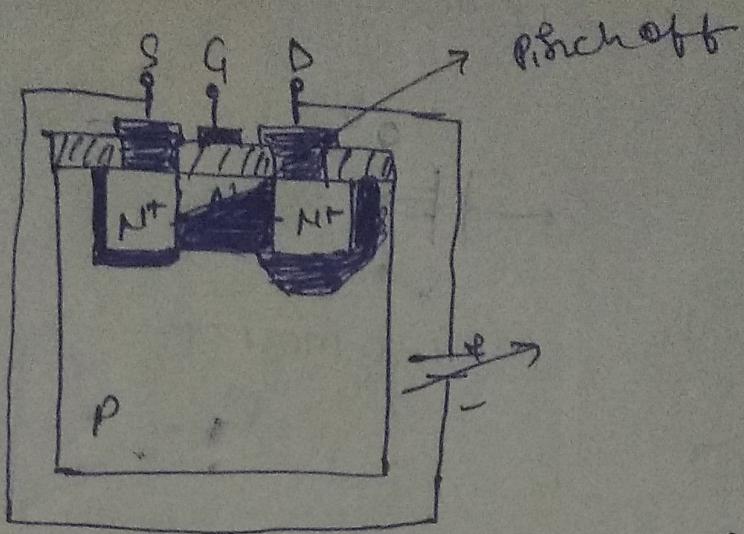
N-CH-D MOSFET

** Working of N-CH-D MOSFET

i) Case $V_{GS} = 0$: short

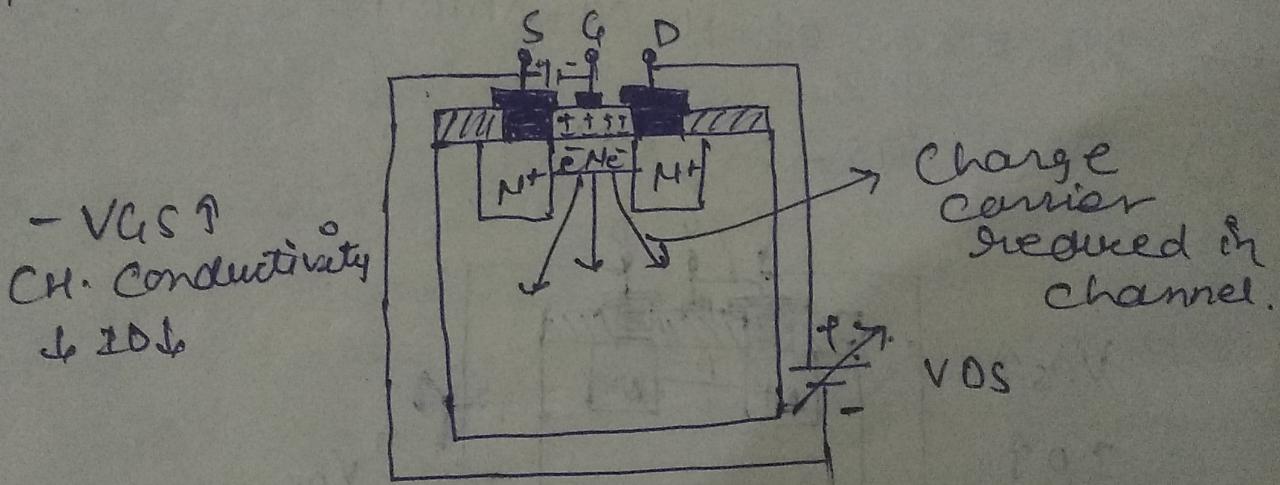


When the gate is made shorted with source ($V_{GS}=0$) On increasing V_{DS} I_D increases linearly but as V_{DS} reaches to pinch off voltage the current became constant.



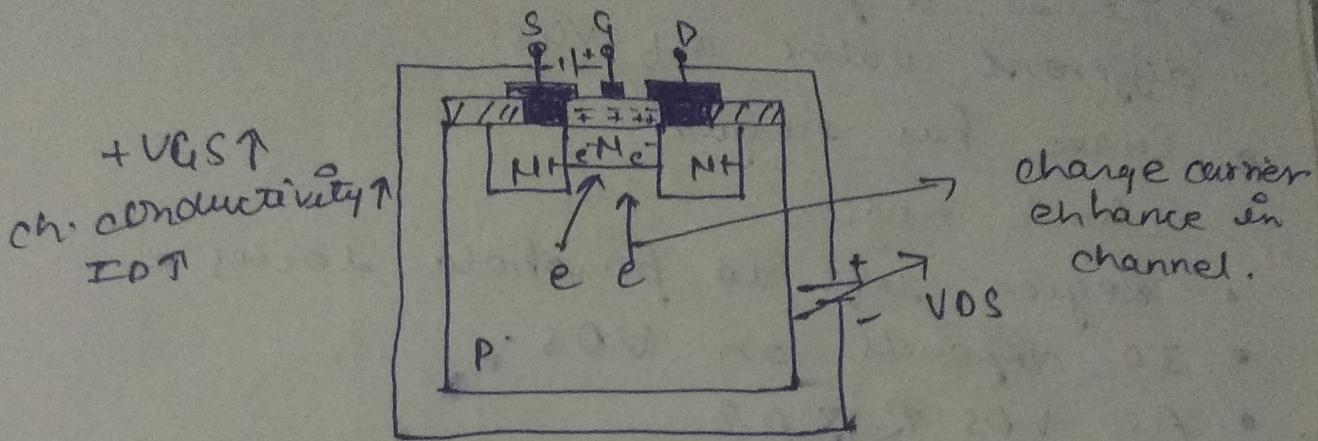
Beyond V_P if $V_{OS} \uparrow \pm I_D$ remain constant
 $V_{OS} = V_P$ Pinch off potential.

2.) Case $V_{GS} < 0$



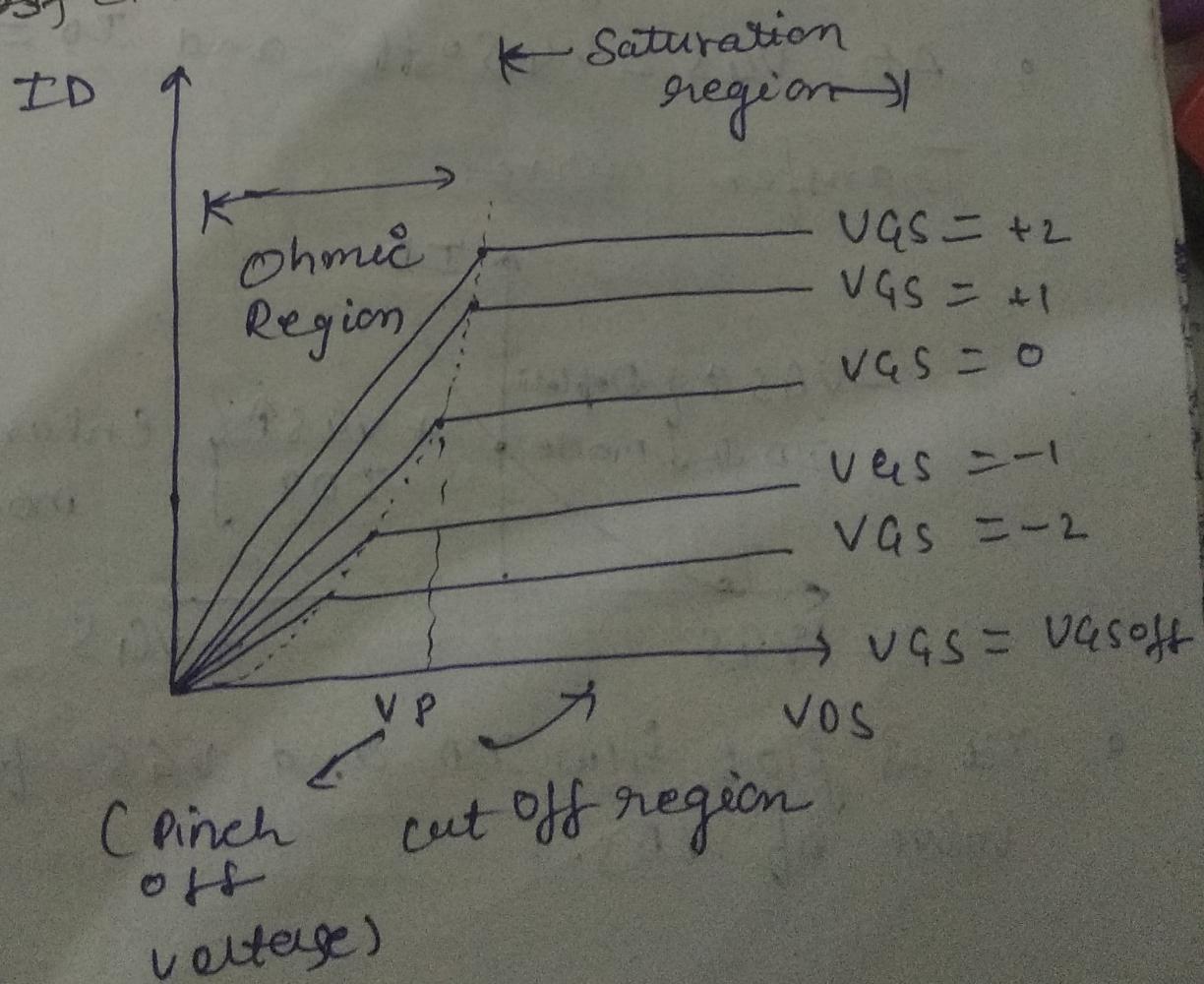
When V_{GS} less than zero an electric field is induced in channel which repel majority charge carrier (e^-) free electron away from channel thus reduced conductivity of the channel so I_D decreases.

3.7 Case $V_{GS} > 0$



When V_{GS} greater than zero electric field attract electron into channel from substrate which increases conductivity of the channel and as a result I_D increase.

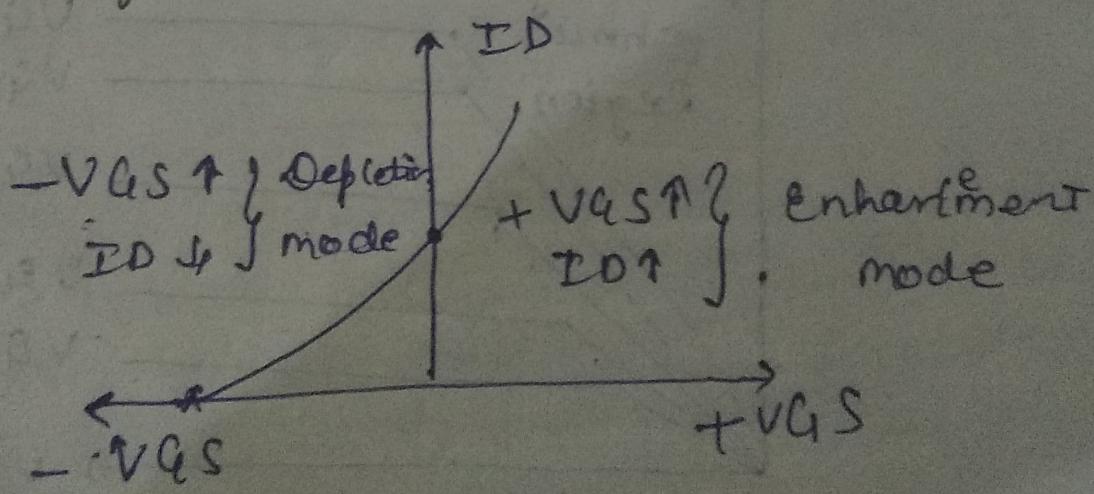
Output characteristic curve for Nch DMOSFET.



- It is a plot b/w V_{DS} and I_D for different value of V_{GS} .
 - Curve has region
 - Ohmic region
 - Region left to parabola locus.
 - I_D depends on V_{DS} .
 - As $V_{DS} \uparrow I_D \uparrow$
- Saturation region -

- Region right to parabola locus.
- I_D is independent of V_{DS} and depend on V_{GS} .
- Cut off region
- At $V_{GS} = V_{GS\text{off}}$ and $I_D = 0$

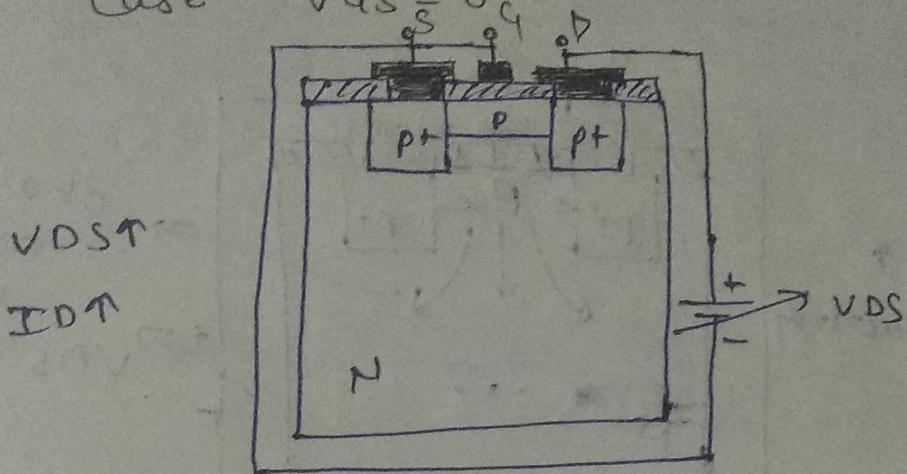
Transfer curve.



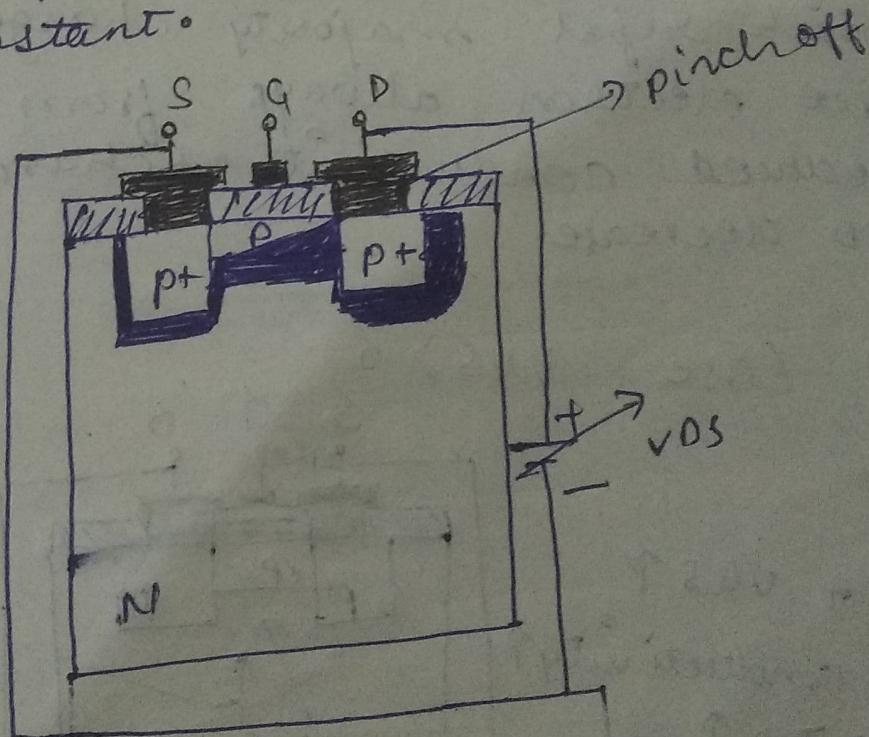
- It is plot b/w I_D and V_{GS} for constant value of V_{DS} .

* * On Working of P-CH-DMOSFET

i) Case $V_{GS} = 0V$

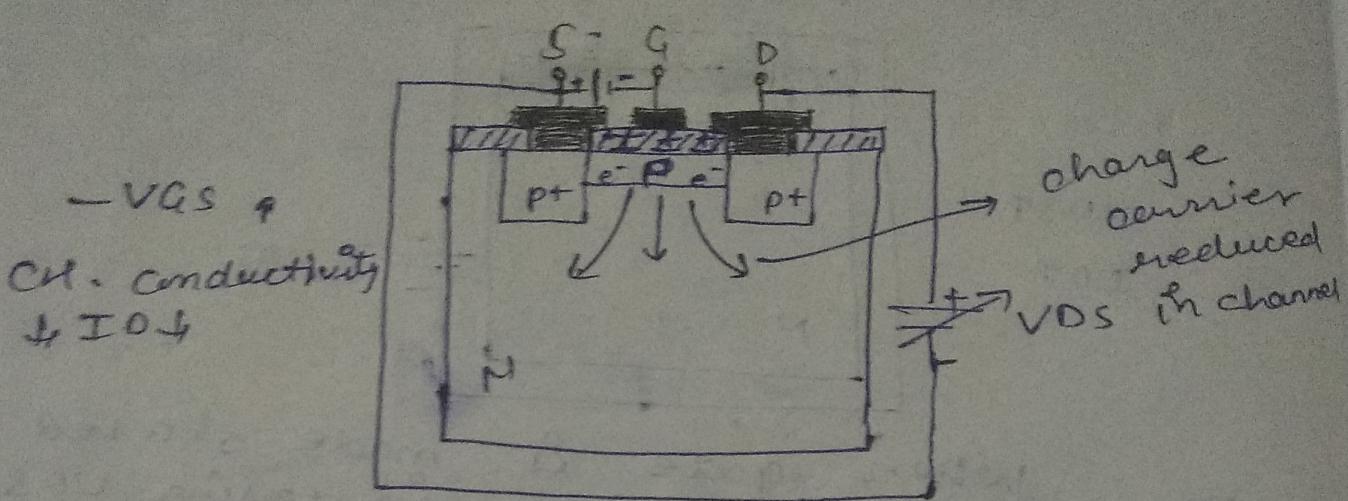


When gate is made shorted with source ($V_{GS}=0$) on increasing V_{DS} I_D increasing linearly but as V_{DS} reach to pinch off voltage the current become constant.



Beyond V_P if $V_{DS} \uparrow I_D$
remain constant $V_{DS} = V_P$ pinch
off potential.

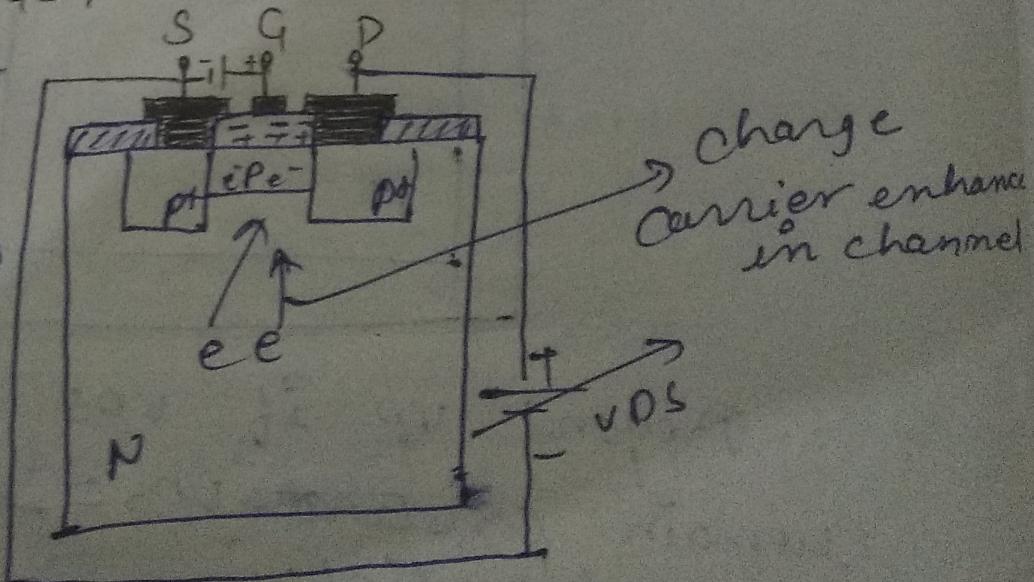
2.7 Case $V_{GS} < 0$



when V_{GS} less than zero an electric field is induced in channel which repel majority charge carrier e^- free electron always from channel thus reduced conductivity of channel so I_D decrease.

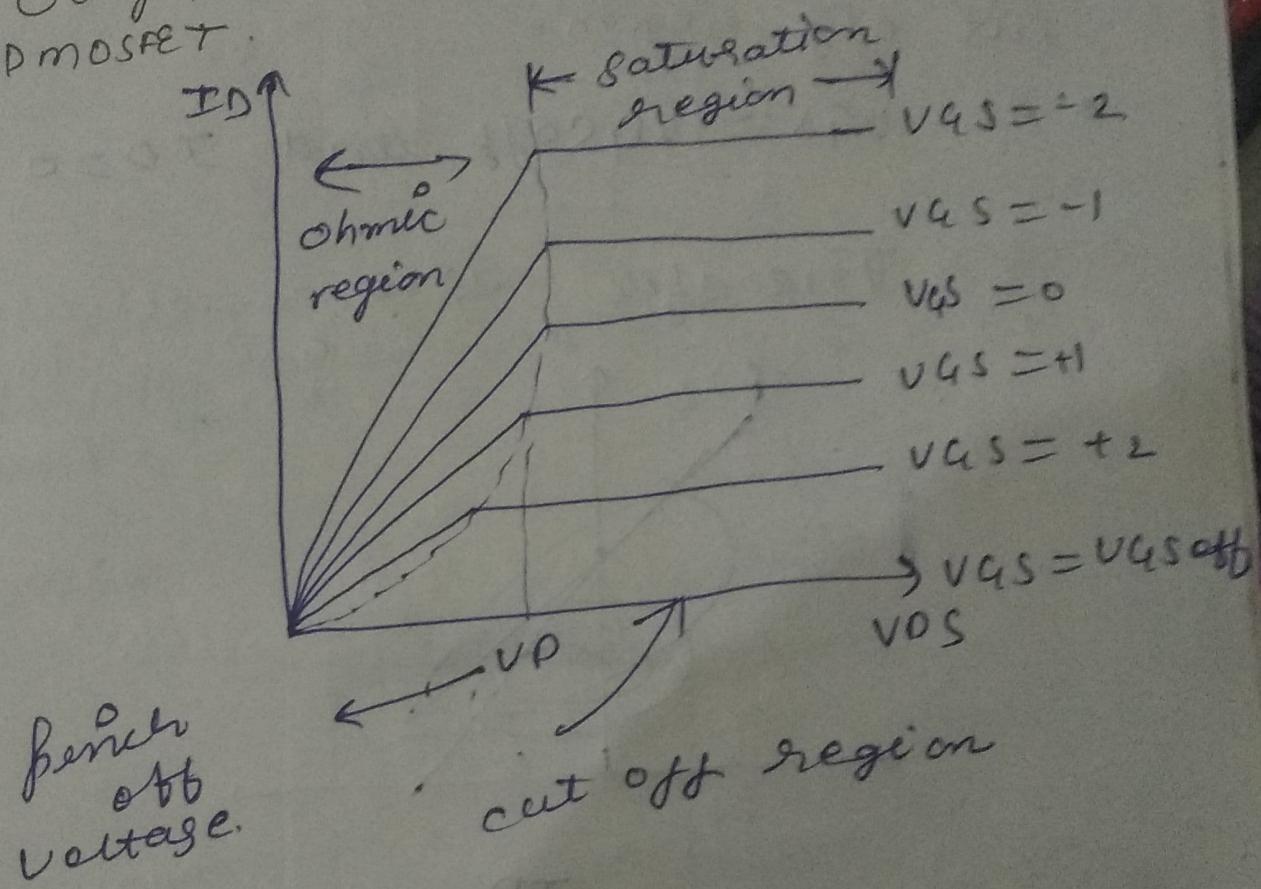
3.7 Case $V_{GS} > 0$

$+ V_{GS} \uparrow$
CH conductivity \uparrow
 $I_D \uparrow$



When V_{GS} is greater than zero electric field attract electron into channel from substrate which increase conductivity of the channel and as a result I_D increases.

Output characteristic for P-CH DMOSFET.



- It is plot b/w V_{DS} and I_D for different value of V_{GS}
- Curve has region.

- Ohmic region.
- Region left to parabola locs.
- I_D depends on V_{DS} .
- As $V_{DS} \uparrow I_D \uparrow$

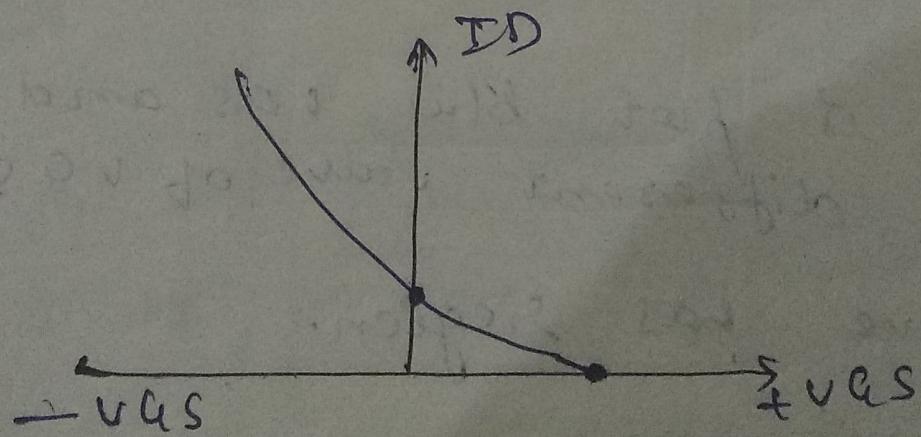
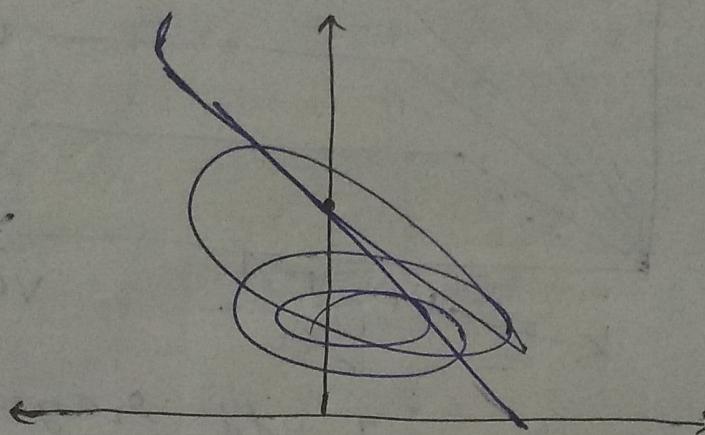
Saturation region \rightarrow

- Region right to parabola region.
- I_D is independent of V_{OS} and depend on V_{GS} .

Cut off region -

- At $V_{GS} = V_{GS\text{off}}$ and $I_D = 0$

Transfer curve

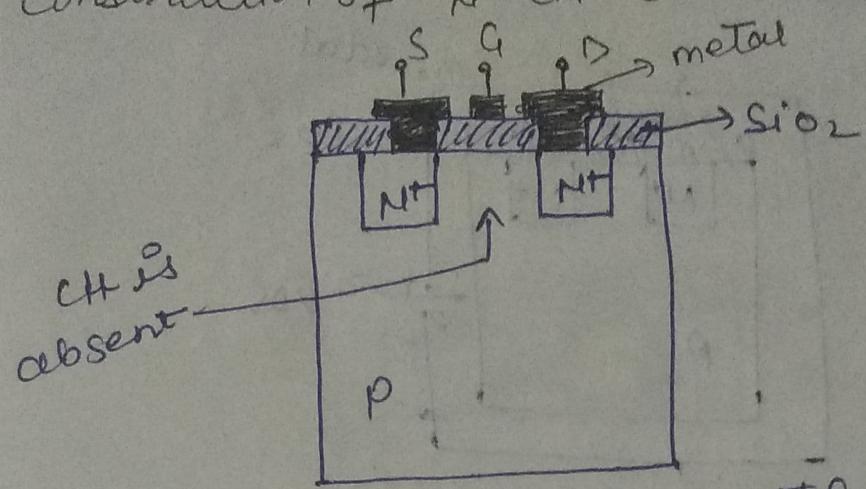


- It is plot b/w I_D and V_{GS} for constant value of V_{OS} .



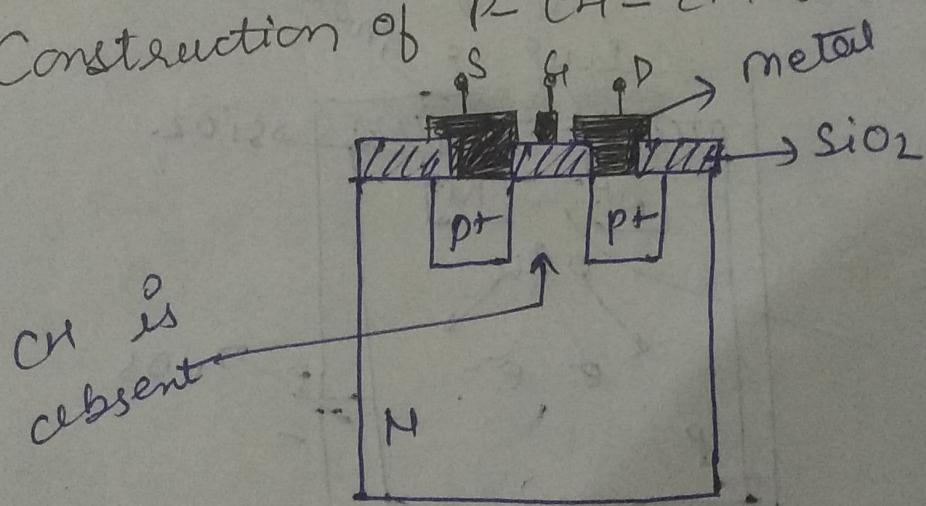
Enhancement MOSFET →

Construction of N-CH-EMOSFET →



- Construction similar to N-CH DMOSFET
the only difference is here CH is physically absent.

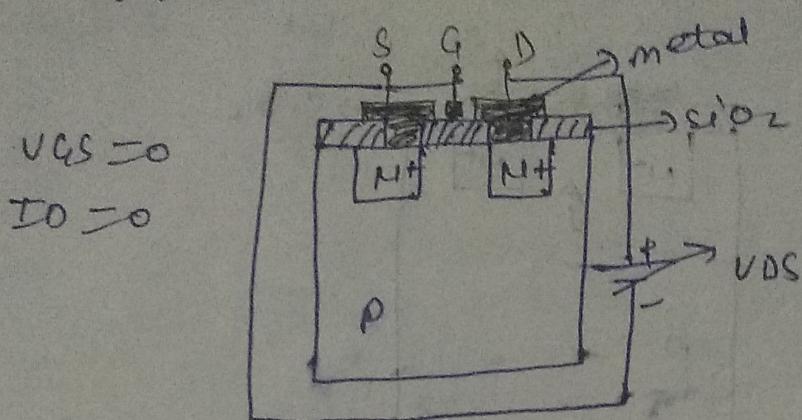
Construction of P-CH-EMOSFET →



- Construction similar to P-CH DMOSFET
the only difference is that here CH is physically absent.

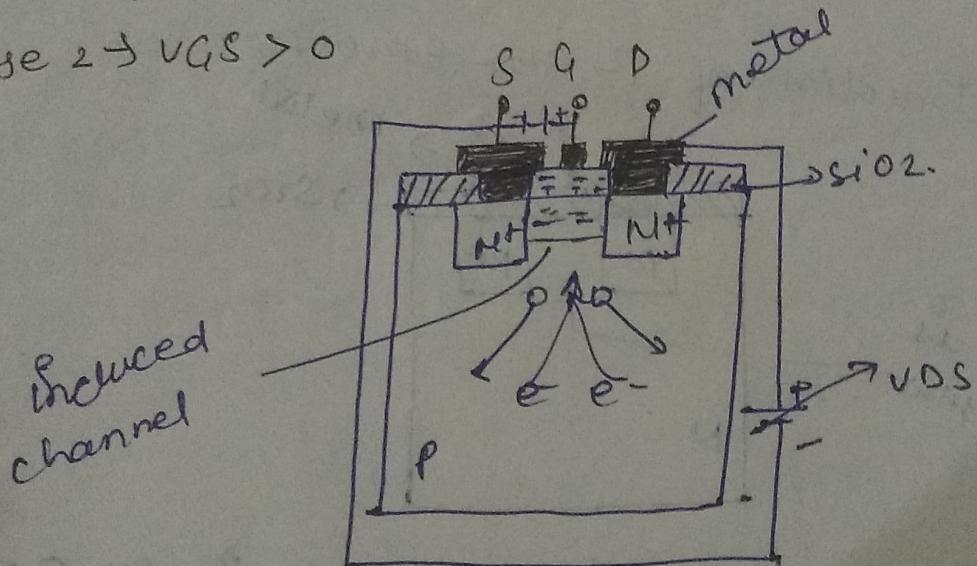
Working of N-CH MOSFET \rightarrow

Case 1) $V_{GS} = 0$



If $V_{GS} = 0$ and positive voltage is applied b/w drain and source then due to absent of N-type channel I_D will be zero.

Case 2 $\rightarrow V_{GS} > 0$



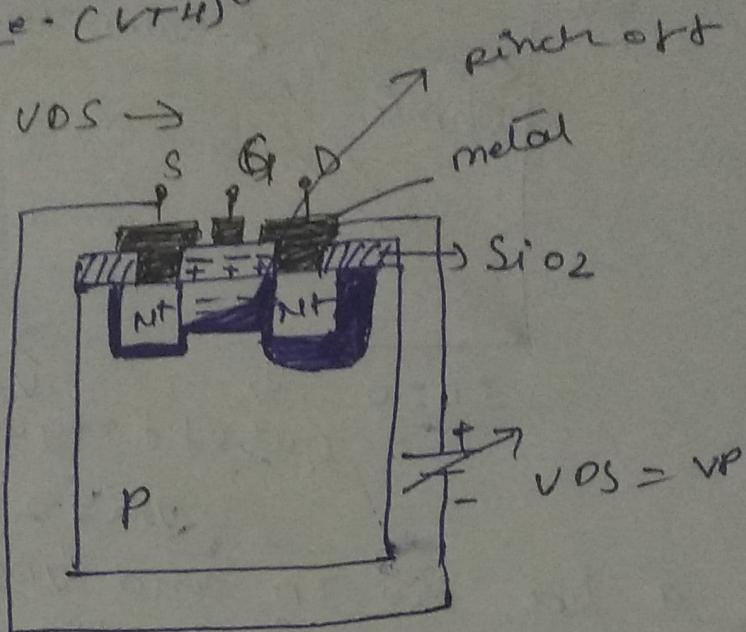
When V_{GS} is +ve, positive terminal of gate will repel hole present in p-type substrate and attract electron towards gate terminal and gather near the surface of SiO₂ layers.

As V_{GS} increases electron concentration increases to such amount that it creates n-type channel which connects N+ region.

Now drain current start flowing through the induced channel.

Note - The minimum value of V_{DS} at which conduction begins is known as threshold hold voltage - (V_{TH})

Case 3 → Effect of V_{DS} →

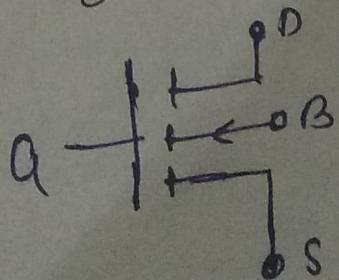


If $V_{GS} > V_{TH}$
then $V_{DS} \uparrow I_D \uparrow$ (Before pinch off)

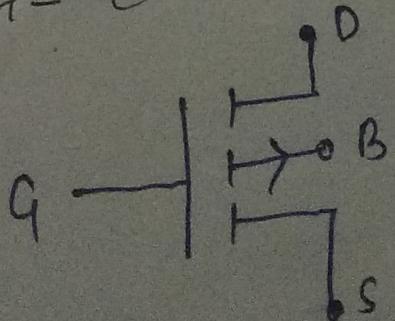
$I_D = \text{constant}$ (after $V_{DS} = V_P$).

Circuit symbol -

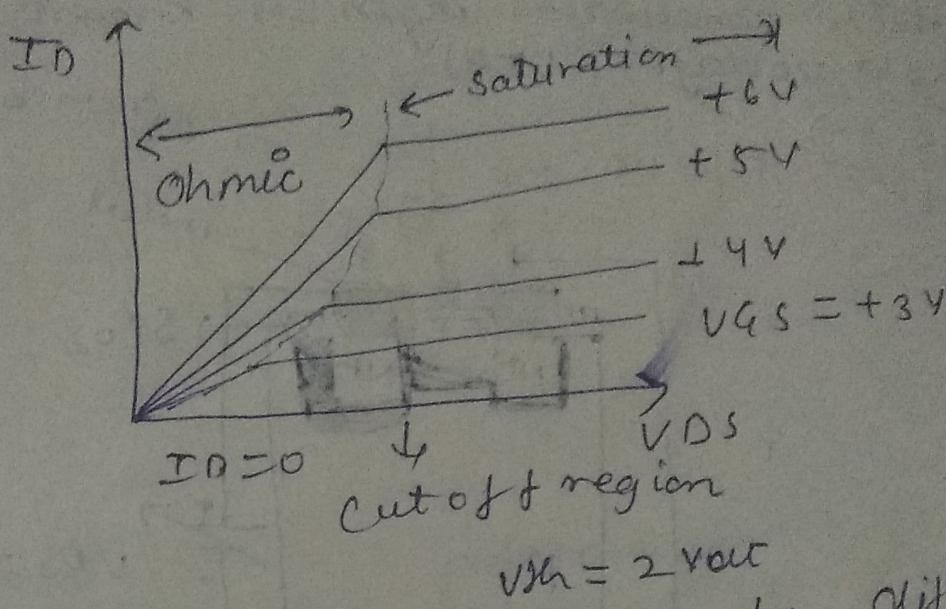
① N-CH- ϵ MOSFET



② P-CH- ϵ MOSFET



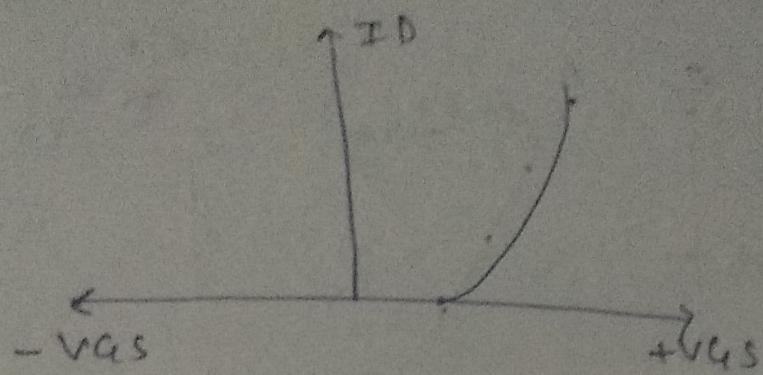
O/P curve / drain characteristic curve for
N-CH-EMOSFET



Its a plot b/w ID and V_{DS} for difference value of V_{GS} here $ID \neq 0$ for $V_{GS} \leq V_{TH}$ for all values of V_{DS} .

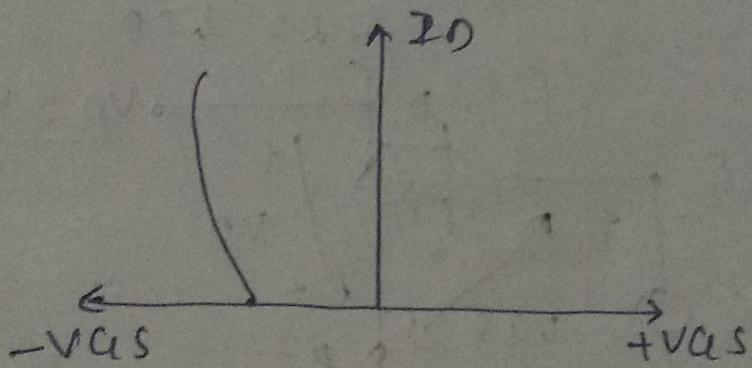
- For V_{GS} set at different positive value ($V_{GS} > V_{TH}$) the drain characteristic are similar to those of N-CH-DMOSFET.
- Curve has \triangleright region.

* Transfer curve of N-CH-EMOSFET



It's a flat b/w I_D and V_{GS} after threshold voltage I_D increases non linear.
 For V_{GS} less than equal to V_{th} , $I_D = 0$,
 $(V_{GS} \leq V_{th}), I_D = 0$

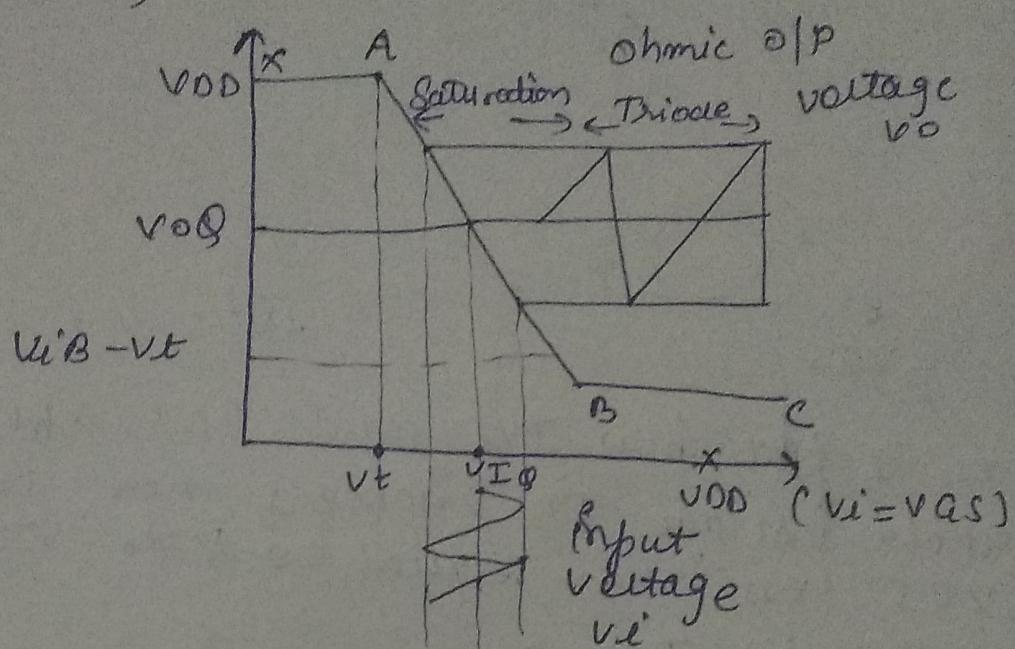
Transfer curve P-CH EMOSFET



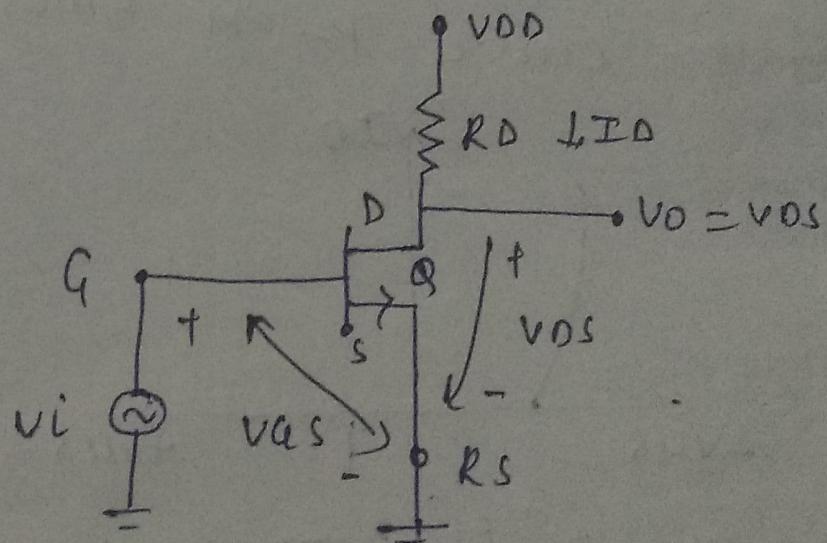
It's a flat b/w I_D and V_{GS} after fresh
 hold voltage I_D increases non linear.
 For V_{GS} less than, V_{th} $I_D = 0$, $V_{GS} \leq V_{th}$
 equal to

** ITB

MOSFET as an amplifier / switch / transfer
curve →



$$V_O = V_{OS} = V_D = V_{DD} - I_{ORD} R_D$$



In the amplifier circuit MOSFET is operate saturation region and for switch operated in cut off and ohmic regions

From Circuit

$$\boxed{V_O = V_{DD} - I_{ORD} R_D}$$

Circuit Operations

- Cut off region $\rightarrow (XA)$
 $V_i < V_t$

For $V_i < V_t$ the transistor will be cut off $I_D = 0$ and output voltage.

$$V_i < V_t, I_D = 0, V_{DS} = V_{DD} = V_0$$

- Saturation $\rightarrow (AB)$

As V_i exceeds V_0 the transistor term on $I_D \uparrow V_{DS}$

Saturation region operation continues until V_0 decreases to point that is below V_i (Input voltage) by V_t volt.

At this point MOSFET enters into ohmic region.

- Ohmic region $\rightarrow (BC)$

After point B ohmic region starts in this region output voltage decreases slowly and we get a point C where $V_i \leq V_{DD}$.

Voltage and current relation for MOSFET.

- 1.) (Cut off)

$$(V_i \leq V_t)$$

$$V_0 = V_{DD}$$

$$I_D = 0$$

- 2.) Saturation ($V_i > V_t$)

$$I_D = \frac{1}{2} \mu n C_o x \frac{W}{L} \left(\frac{V_{GS}}{V_t} - 1 \right)^2$$

$$V_0 = V_{DS} = V_{DD} - I_D R_D$$

$$V_0 = V_{DS} = V_{DD} - R_D \left(\frac{1}{2} \mu n C_o x \frac{W}{L} (V_{GS} - V_t)^2 \right)$$

Voltage gain

$$\Delta V \approx \frac{\partial V_o}{\partial V_{GS}}$$

$$\frac{\partial V_o}{\partial V_{GS}} = \left(V_{DD} - 2V_T \right) \text{mhos} \cdot \frac{W}{L} (V_{GS} - V_t)^2$$

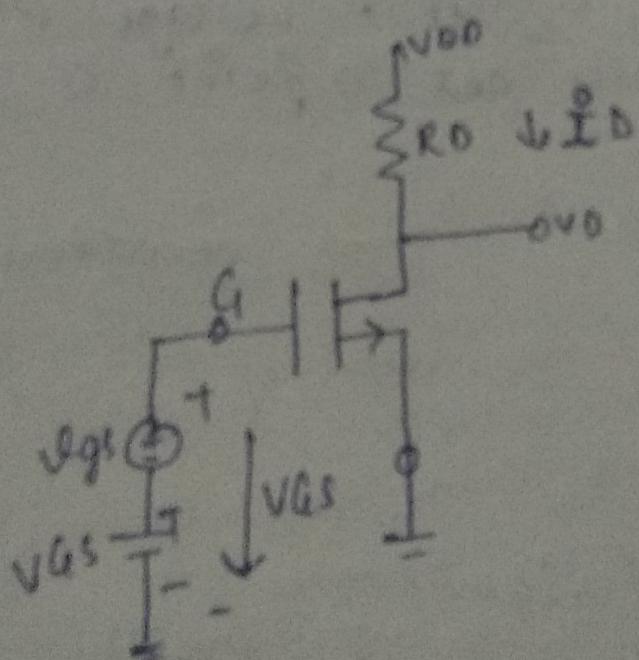
$$\Delta V \approx \frac{\partial V_o}{\partial V_{GS}} = -2 \times \frac{1}{L} \text{mhos} \cdot \frac{W}{L} (V_{GS} - V_t)^2$$

$$\boxed{\Delta V = -R_{OSS} \times \frac{W}{L} (V_{GS} - V_t)}$$

$$R_{OSS} = R_o$$

$$V_{GS} - V_t = V_{AS}$$

Small signal operation for MOSFET



$$\begin{aligned} I_D &\approx \text{dc} \\ i_d &= \text{ac} \\ I_D &= \text{ac} + \text{dc} \end{aligned}$$

$$\boxed{g_m = \frac{i_d}{v_{GS}}}$$

Dc bias point
 $v_{AS} = V_G - V_S$

$$I_D = \frac{1}{2} K_n \frac{W}{L} (V_{AS} - V_t)^2$$

$$V_{OS} = V_{DD} - I_D R_D$$

Calculation for signal current (i_d) $\underline{v_a(ac)}$

$$V_D = V_{DS} = V_{DD} - i_D R_D$$

$$i_D = \frac{1}{2} k n' \frac{\omega}{L} (V_{GS} - V_t)^2$$

$$V_{GS} = \underbrace{V_{GS}}_{ac+dc} + \underbrace{v_{gs}}_{de} + \underbrace{v_{gs}}_{dc}$$

$$i_D = \frac{1}{2} k n' \frac{\omega}{L} ((V_{GS} - v_{ds} + v_{gs})^2)$$

$$i_D = \frac{1}{2} k n' \frac{\omega}{L} ((V_{GS} - V_t) + v_{gs})^2$$

$$i_D = \frac{1}{2} k n' \frac{\omega}{L} (V_{GS} - V_t)^2 + k n' \frac{\omega}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} k n' \frac{\omega v_{gs}^2}{L}$$

$$i_D = \frac{1}{2} k n' \frac{\omega}{L} (V_{GS} - V_t)^2 + k n' \frac{\omega}{L} (V_{GS} - V_t) v_{gs}$$

$$\boxed{i_d = k n' \frac{\omega}{L} (V_{GS} - V_t) v_{gs}}$$

$$g_m = \frac{i_d}{v_{gs}} = k n' \frac{\omega}{L} (V_{GS} - V_t)$$

$$\boxed{g_m = k n' \frac{\omega}{L} V_{DD} = g_m}$$

Voltage gain for AC signal - $\left\{ \frac{i_d}{v_{gs}} \right\}$

$$V_D = V_{DS} = V_{DD} - R_D i_D$$

$$V_D = V_{DD} - R_D (I_D + i_d)$$

$$[V_O + v_{ed}] = V_D = \underbrace{V_{DD} - R_D I_D}_{V_D = dc} - \underbrace{\frac{R_D i_d}{ac}}$$

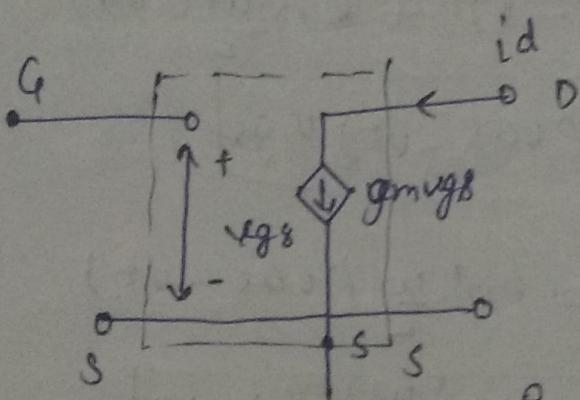
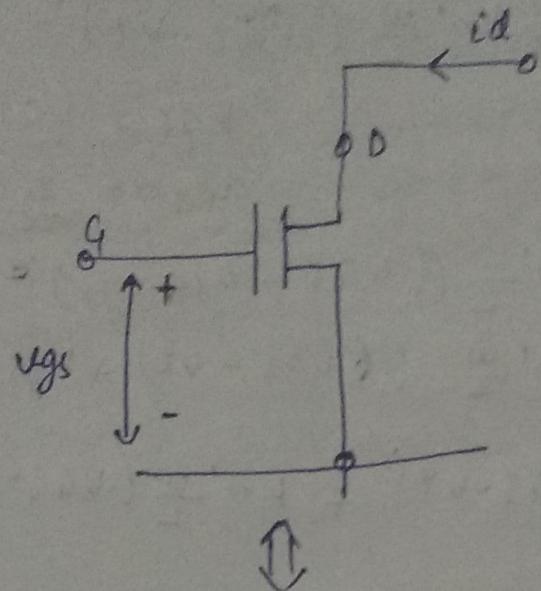
$$v_{ed} = -R_D i_d$$

$$v_{ed} = -R_D g_m v_{gs}$$

$$\boxed{\frac{v_{ed}}{v_{gs}} = AV = -R_D g_m}$$

AC gain

small signal model for MOSFET \rightarrow (n) model



For low frequency signal capacitors are replaced by short circuit and all the dc voltage sources are replaced by zero.

MOSFET behaves as a voltage control current source it accept a signal ~~signal~~ vgs b/w gate and source .

vgs b/w gate and source a provide a current $gm vgs$ and drain terminal.

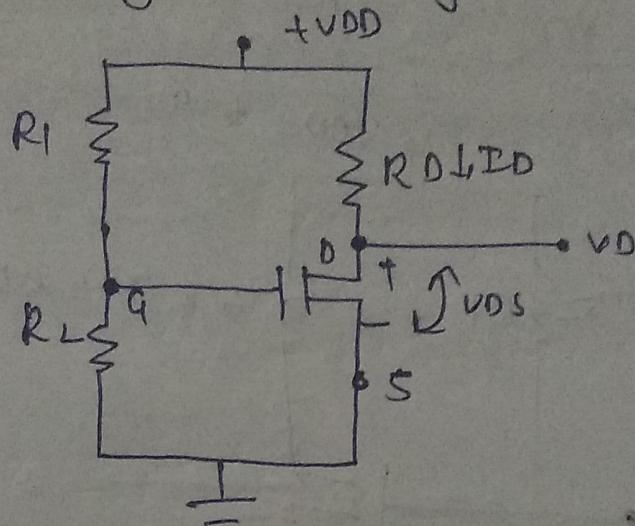
\therefore At the output side a current source

G_{MUGS} has been included.

Input resistance of MOSFET is extremely large so gate terminal is open.

★ DC Biasing of MOSFET -

Cases → Biasing by fixing VGS



$$V_{GS} = V_G - V_S \quad (\because V_G = 0)$$

$$V_{GS} = V_G = \frac{R_L \times V_{DD}}{R_1 + R_L}$$

$$I_D = \frac{1}{2} \underbrace{\mu_{n'c}}_{K_n} \frac{W}{L} (V_{GS} - V_t)^2$$

$$V_D = V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = V_D - V_S$$

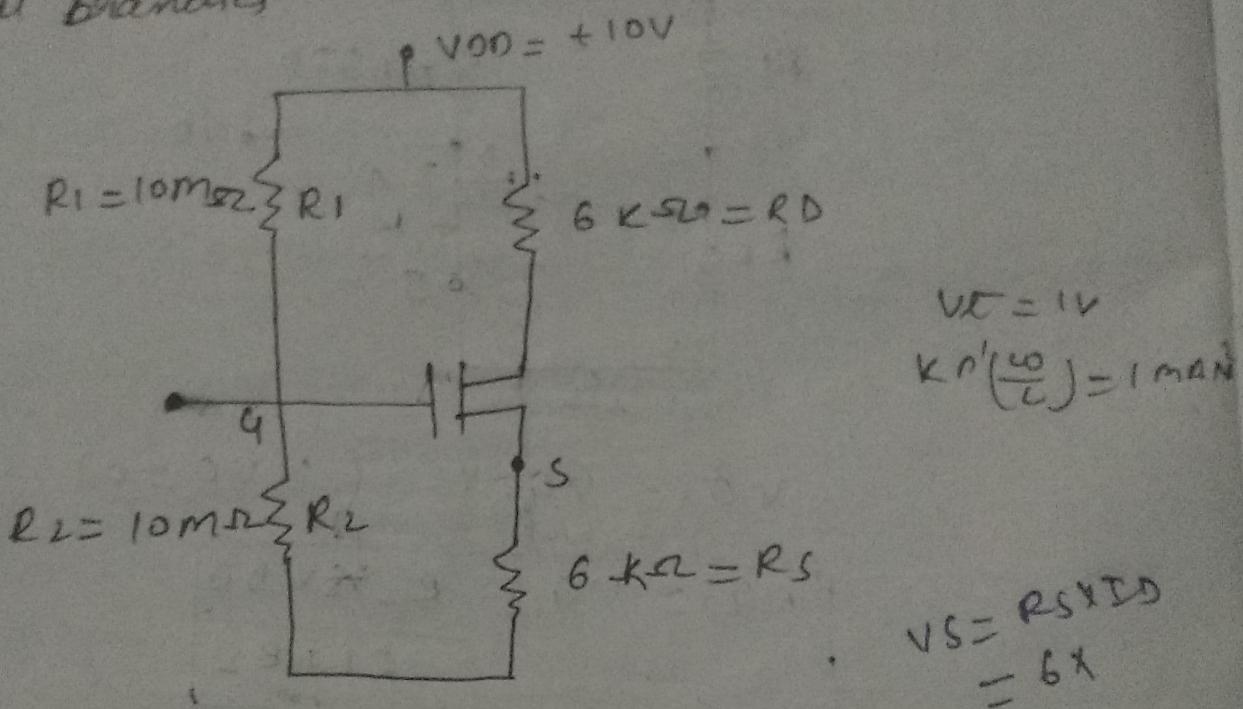
★ if R_S is connected at source

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - R_S I_D$$

Q.1 For given circuit determine the voltage at all nodes and the current through all branches.



$$\textcircled{1} \quad V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$V_G = \frac{10 \times 10}{10 + 10} = \frac{10}{20} = 5V$$

$$\textcircled{2} \quad V_{GS} = V_G - V_S$$

$$V_{GS} = 5 - 6 I_D$$

$$I_D = \frac{1}{2} \cdot 4 \cos \frac{\pi}{6} (V_{GS} - V_t)^2$$

$$I_D = \frac{1}{2} \times 1 (5 - 6I_D - 1)^2$$

$$I_D = \frac{1}{2} (4 - 6I_D)^2$$

$$I_D = \frac{1}{2} \times (16 + 36I_D^2 - 48I_D)$$

$$I_D = (0 + 18I_D^2 - 24I_D)$$

$$18I_D^2 - 24I_D + 0 = 0$$

$$I_{D1} = 0.89 \text{ mA}$$

$$I_{D2} = 0.5 \text{ mA}$$

$$\textcircled{4} \quad V_{GS} = 5 - 6 + 0.5 \times 10^{-3} = 2 \text{ V}$$

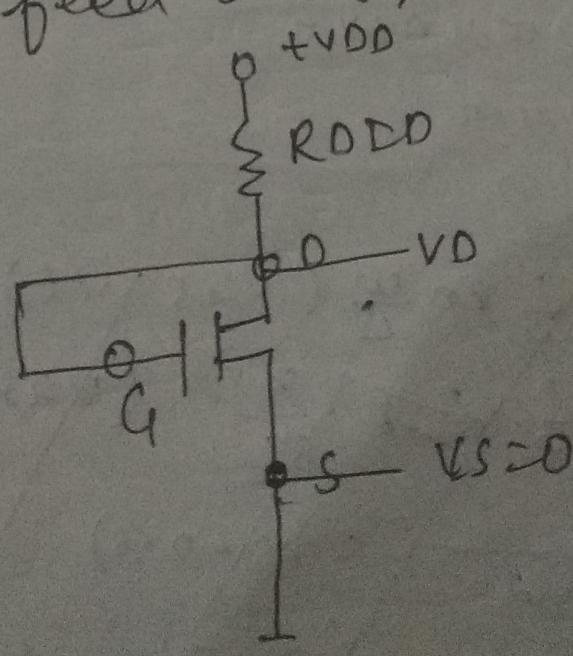
$$\textcircled{5} \quad V_S = R_S \times I_D = 6 \times 10^3 \times 0.5 \times 10^{-3} = +3 \text{ V}$$

$$\textcircled{6} \quad V_D = V_{DD} - R_D I_D = 7 \text{ V out}$$

$$= 10 - 6 \times 0.5$$

$$= 10 - 3 = \underline{\underline{7 \text{ V out}}}$$

\textcircled{2} Biasing by feed back \rightarrow

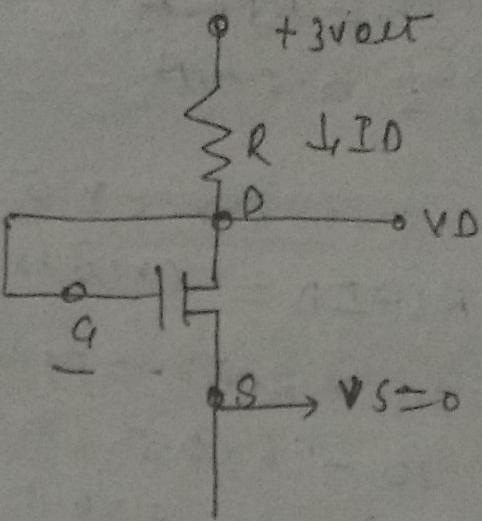


Here $V_S = 0$
 $\vec{V_{GS}} = \vec{V_{DS}} = V_D - R_D I_D$

$$\boxed{\begin{aligned} V_G &= V_D \\ \therefore V_S &= 0 \end{aligned}}$$

$$\boxed{I_D = \frac{1}{2} k n' \frac{w}{L} (V_{GS} - V_t)^2}$$

Q2



$$V_D = ?$$

$$R = ?$$

$$I_D = 0.04 \mu A$$

$$V_t = 0.6 V$$

$$\mu n \text{Con} = 200 \mu A/V^2$$

$$L = 0.8 \mu m$$

$$w = 4 \mu m$$

~~$$I_D = \frac{1}{2} k n' \frac{w}{L} (V_{GS} - V_t)^2$$~~

~~$$8 \times \frac{1}{2} \times \frac{200}{0.8} \times \frac{4 \times 10^{-6}}{10^{-6}} (V_{GS} - 0.6)$$~~

~~$$8 \times \frac{1}{2} \times \frac{200}{0.8} (V_{GS} - 0.6)$$~~

~~$$16 \times 5 (V_{GS} - 0.6)$$~~

$$I_D = \frac{1}{2} \mu n C_{ox} \times \frac{W}{L} (V_{GS} - V_t)$$

$$8 \text{ mA} = \frac{1}{2} \times 200 \times \frac{4}{0.8} (V_{GS} - 0.6) \text{ V}$$

$$(V_{GS} - V_t) = 0.4$$

$$V_{GS} = 0.4 + V_t$$

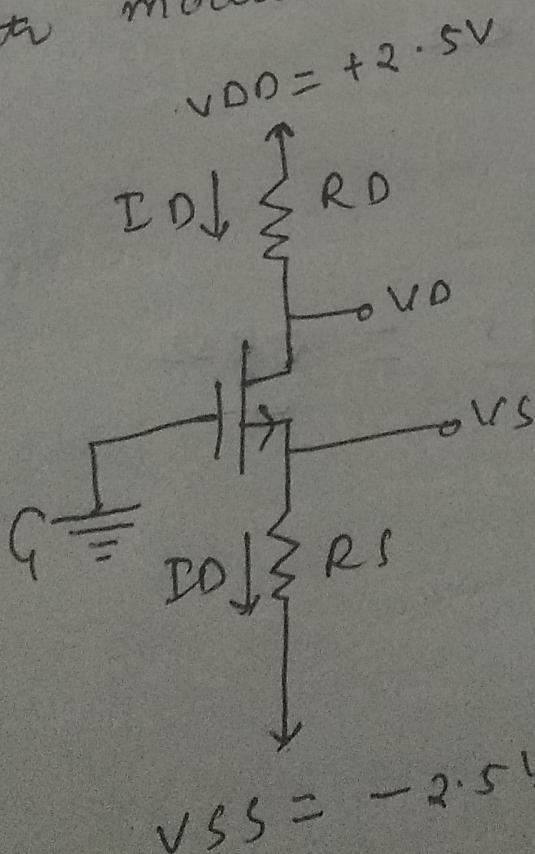
$$V_{GS} = 0.4 + 0.6$$

$$\boxed{V_{GS} = 1.0}$$

$$\boxed{V_D = V_G = V_{GS} = 1.0 \text{ V}}$$

$$R = \frac{V_{DD} - V_D}{I_D} = 25 \text{ k}\Omega$$

Q.3 Design the circuit so that the transistor operates at $I_D = 0.4 \text{ mA}$ and $V_D = 0.5 \text{ V}$. The NMOS transistor has $V_r = 0.7 \text{ V}$, $\mu n C_{ox} = 100 \mu \text{A/V}^2$, $L_F = 1 \mu\text{m}$ and $W = 32 \mu\text{m}$. Neglect the channel length modulation effect (i.e. assume that $\lambda = 0$)



Soln

$$I_D = \frac{1}{2} \mu n \cos \frac{\omega}{L} (V_{GS} - V_T)^2$$

$$V_{GS} - V_T = V_{OV}, I_D = 0.4mA \approx 400mA$$

$$\text{den const} = 100mA/V^2$$

$$\frac{\omega}{L} = \frac{32}{1}$$

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

$$\boxed{V_{OV} = 0.54}$$

$$\begin{aligned} V_{GS} &= V_T + V_{OV} = 0.75 + 0.5 \\ &= 1.2V \end{aligned}$$

$$\begin{aligned} R_S &= \frac{V_{GS} - V_{SS}}{I_D} \\ &= \frac{-1.2 - (-2.5)}{0.4} \\ &= 3.25k\Omega \end{aligned}$$

$$\begin{aligned} R_D &= \frac{V_{OD} - V_O}{I_D} \\ &= \frac{2.5 - 0.5}{0.4} = 5k\Omega \end{aligned}$$