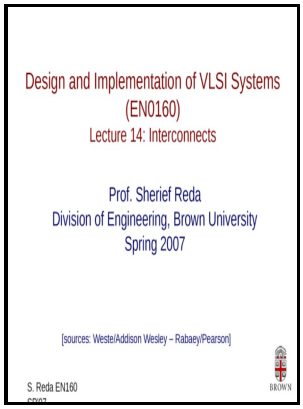
Interconnects in VLSI design

Kluwer Academic Publishers - Addressing Electromigration and IR Drop Within VLSI Interconnect Downscaling



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VLSI System Design

We propose an efficient static current calculation technique.

Interconnects in VLSI Design

Do you like to take this exhaustive path when there is an easy way out? Combined with a pruning technique, it is integrated into a reliability verification flow to be tested on a SoC design.

NPTEL :: Electronics & Communication Engineering

The whole domain of computing ushered into a new dawn of electronic miniaturization with the advent of semiconductor transistor by Bardeen 1947-48 and then the Bipolar Transistor by Shockley 1949 in the Bell Laboratory. Thus, for short wires, with thickness kept constant, the resistance remains same. You can access features of these design engines to identify the wear-out failures in interconnects without much difficulty.

Tapering interconnect topology for high speed vlsi design

Objective This course is designed for students who are interested in understanding the issues in designing high performance VLSI chips in gigahertz frequencies using deep submicron CMOS technology and potential techniques to ensure such designs are successful in meeting the design goal.

VLSI technology: An overview

A sort of block diagram is decided upon with the number of inputs, outputs and timing decided upon without any details of the internal structure. It has to be a tradeoff between market requirements, the available technology and the economical viability of the design. A notable characteristic of this technique is that current calculations are based on ramp input signals, a more realistic signal than a step input.

Interconnect Scaling trends

Moreover, an advanced gate model is applied to this technique; thus the current it yields is more accurate than that using a switch-resistor model.

Current calculation on VLSI signal interconnects — University of Illinois Urbana

On the other hand, for long wires, where the length of wire is independent of scaling, only thickness and width of the wire scales down.

EE660 Advanced Topics in VLSI Design

The number of metal layers and the interconnects be it global and local also tend to get messy at such nano levels. The major parameters considered at this level are performance, functionality, physical dimensions, fabrication technology and design techniques.

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