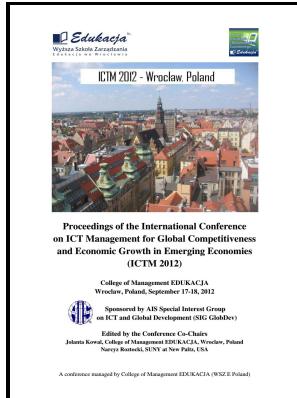


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Cache and pipeline sensitive fixed priority scheduling for preemptive real-time systems. Software and Compilers for Embedded Systems: 8th International Workshop, SCOPES 2004, Amsterdam, The Netherlands, September 2-3, 2004.

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Adding instruction cache effect to schedulability analysis of preemptive real-time systems. IEEE Micro, 30 5 :66—75, 2010.

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We first present the challenges and static analysis techniques for independent programs with respect to different cache features. Journal of Systems Architecture — Embedded Systems Design, 54 1-2 :265—286, 2008. Selfish-lru: Preemption-aware caching for predictability and performance.

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Schloss Dagstuhl — Leibniz-Zentrum für Informatik. Initially, the workshop was referred to as the International Workshop on Code Generation for Embedded Systems.

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