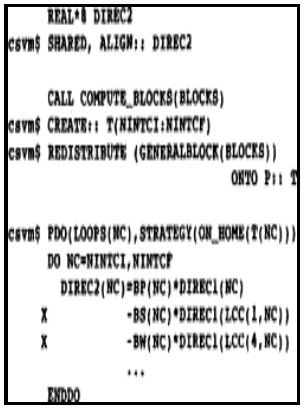
Shared virtual memory accomodating hetergeneity

CSRI, University of Toronto - Shared Virtual Memory for Heterogeneous Embedded Systems on Chip



Description: -
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Virtual storage -- Computer science.Shared virtual memory accomodating hetergeneity
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Technical r/port CSRI -- 220Shared virtual memory accomodating hetergeneity
Notes: Includes bibliographical references.
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Analysis and modeling of collaborative execution strategies for heterogeneous CPU

We show that the general trend is that kernel duplication improves performance until the memory bandwidth saturates. This enables application portability, flexibility, and ease of data structure implementation.

Similar but different: virtual memory CD8 T cells as a memory

At the same time, programmability is also improving with High Level Synthesis tools e.

Architectural support for virtual memory in GPUs

In these systems, any application that wants to share data between CPU and GPU will need to copy it from CPU memory to graphics memory at a significant cost of latency and power. The CPU and GPU on a typical applications processor occupy a significant proportion of die area and applying these resources efficiently across multiple applications can improve the end user experience.

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These charts approximate elapsed time on the horizontal axis, and address space on the vertical axis.

Inferring Kaveri's Shared Virtual Memory Implementation

To allow SVM buffers to be freed after completion of enqueued commands, the specification supplies a command to enqueue a free operation: clEnqueueSVMFree.

Architectural support for virtual memory in GPUs

We show that introducing cache-parallel address translation does pose challenges, but that modest optimizations can buy back much of this lost

performance. For instance, if the size of the allocated memory is less than or equal to the cache size, we would expect the entire array to fit in the cache and every access to hit in the cache, experiencing only the cache hit latency.

HERO Documentation

Adding Hardware Coherency to the GPU While processor clusters have implemented cache coherency protocols for many years, this is a new area for GPUs. HSA is set of standards from the which provides transparent support for multiple compute platforms.

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This means the GPU caches must be cleaned with cache maintenance operations after processing completes. Ubal, in , 2016 9. The MYO module implements a software coherence mechanism to ensure any data is properly updated when modified by either the processor or coprocessor.

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