Lateral superjunction power MOSFETs.

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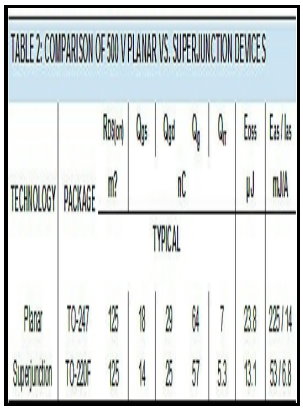

TABLE 2: COMPARISON OF 500 V PLANAR VS. SUPERJUNCTION DEVICES

TECHNOLOGY	PACKAGE	$R_{DS(on)}$ mΩ	Q_{gs} nC	Q_{gd} nC	Q_g nC	Q_{rr} nC	E_{oss} µJ	E_{AS} / I_{AS} mJ/A
				TYPICAL				
Planar	TO-247	125	18	29	64	7	23.8	225/14
Superjunction	TO-220F	125	14	25	57	5.3	13.1	50/6.8

Description: -
-Lateral superjunction power MOSFETs.
-
Canadian theses = -- Thèses canadiennesLateral superjunction power MOSFETs.
Notes: Thesis (M.A.Sc.) -- University of Toronto, 2001.
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Tags: #Extended #Trench #Gate #Superjunction #Lateral #Power #MOSFET #for #Ultra

Lateral Superjunction Power MOSFET

The semiconductor device described in 11, wherein each of the virtually L-shaped columns comprises a continuous pattern with a pair of columns separated at a middle point and oriented perpendicularly to each other, and an auxiliary column located near and outside a point where the paired columns meet. Right now, the temperature dependency is not considered but will be added in a future work. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

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Typically, the Q gd of a MOSFET can be used for estimating the V DS voltage rise and fall times during switching. Gate electrodes G 1 to G 4 may also be located adjacent sources S 1 to S 4 respectively and are connected to their respective gate electrodes such as gate electrode 50. Kinzer Srikant Sridevan Current Assignee The listed assignees may be inaccurate.

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Be careful, if you disable it, you will not be able to share the content anymore. Then, as shown in FIG.

Exicon Lateral MOSFETS

A semiconductor device which includes: a a semiconductor chip having a first main surface with a source electrode of a power MOSFET thereon and a second main surface with a drain electrode of the power MOSFET thereon; b a virtually rectangular cell region provided almost in the center of the first main surface and a cell peripheral region surrounding it; c a first-conductivity type drift region provided in virtually whole surfaces of the cell region and the cell peripheral region on the first main surface of the semiconductor chip; d a first super junction structure provided in the drift region on a virtually whole surface of the cell region, having a first orientation; e a second and a third super junction structure provided in the drift region of the cell peripheral region on both sides of the cell region in a direction perpendicular to the first orientation of the first super junction structure, having almost the same length and orientation as the first super junction structure; and f a fourth and a fifth super junction structure provided in the drift region of the cell peripheral region except portions containing the second and third super junction structures and peripheral corner regions, having an orientation almost perpendicular to the first super junction structure; and g virtually L-shaped columns each interconnecting a pair of columns configuring the second to fifth super junction structures in each peripheral corner region, wherein the first to fifth

super junction structures are of a trench epitaxial buried type. In the conduction mode of operation, and with the application of a bias to gate electrode 50 and the grounding of source 43 relative to substrate 12, an N type channel is formed between source regions 41 and base 40. Im Vergleich zu bestehenden Simulationsmodellen des Herstellers verspricht das vorgestellte Modell eine bessere Konvergenz, ein besseres Hochfrequenzverhalten und eine schnellere Simulationszeit.

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However, their performance is greatly handicapped by the limitation of fabrication process technology.

Power MOSFET Basics: Understanding superjunction technology

The solid lines are the equipotential lines and the dashed lines are the depletion Fig.

MDmesh: 20 Years of Superjunction STPOWER™ MOSFETs, A Story About Innovation

The semiconductor device described above in 3, wherein each of the virtually L-shaped columns forms a pattern with a pair of columns separated at a middle point and oriented perpendicularly to each other. Semiconductor device and method of forming the same 2006-03-13 2007-09-20 Fairchild Semiconductor Corporation Periphery design for charge balance power devices 2006-06-15 2007-12-20 Fuji Electric Holdings Co.

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