

High-level VLSI synthesis

Kluwer Academic Publishers - High

Description: -

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Self-Help

Self-Help / Success

Success

Goal (Psychology)

Śāraṇādāsa, -- 15th cent.*

Dover (N.H.) -- Appropriations and expenditures -- Periodicals.

Carbon monoxide -- Environmental aspects -- United States

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Integrated circuits -- Very large scale integration -- Computer-aided design. High-level VLSI synthesis

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Textes littéraires français -- 478.

Journal of biosocial science. Supplements -- 4

Working paper -- SWP 16/95.

Working paper / Cranfield School of Management -- SWP 16/95

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Kluwer international series in engineering and computer science.

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VLSI, computer architecture, and digital signal processing

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The Kluwer international series in engineering and computer science Tags: #High

;High-level VLSI synthesis

Notes: Includes bibliographical references and index.

This edition was published in 1991



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data-flow and control-flow graphs.

RTL Design and Integration Course

Authors and Affiliations Cite this paper as: Nepomnyashchiy O. On the one hand, it should provide separating an initial algorithm representation from a target hardware architecture; on the other hand, it should make possible translating the initial algorithm representation into the RTL-level with simultaneous verification.

High

Incremental Optimization: In this step there are various techniques which are applied to optimize the design in terms of area, timing, power and fix DRC violations.

[PDF] A Framework for High

Selection of concrete computing control strategy defines by the developer. This removes the problem with varied designer styles for the different blocks in the design and suboptimal designs.

[PDF] A Framework for High

Cell degradation Some technology libraries contain cell degradation tables. This course discusses good amount of LINT rules and guidelines, which will enable audience to gain good design practices and perform LINTING if needed.

Unlike existing HLS methods, the proposed methodology allows us to develop an initial description of the VLSI algorithm with the maximal parallelism. Then, the initial algorithm is translated into

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