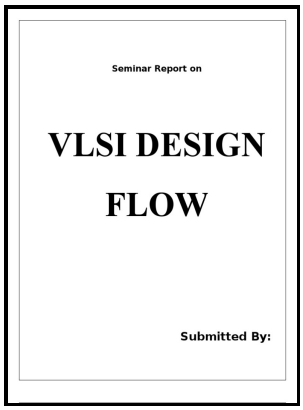
High-performance ASIC design - using synthesizable domino logic in an ASIC flow

Cambridge University Press - ASIC Design Course



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Notes: Includes bibliographical references and index.
This edition was published in 2008

Filesize: 55.61 MB

Tags: #Low #voltage #dual #mode #logic: #Model #analysis #and #parameter #extraction

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Since the inputs to the cell have finite rise and fall times, this means that during the transition period both the PMOS and the NMOS transistors are weakly on. The output voltage of a static and domino buffer as the input switches from low to high.

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The drive 1× size is determined by layout and the likely load encountered by a cell driving a single fan-out placed close to the cell. Hold failures are more dangerous as they can lead to functional failures across all testing conditions and must be avoided at all costs. The acquisition brings together two industry leaders with complementary product portfolios and customers.

High Performance ASIC Design : Using Synthesizable Domino Logic in an ASIC Flow (Hardcover)

The third approach to implement a correct design is to make sure that every domino cell is only clocked when stable input values are present at the input of the domino cells.

Design and Analysing the Various Parameters of CMOS Circuit's under Bi

This is shown in Figure 3.

High Performance ASIC Design : Razak Hossain : 9780521873345

This contention between the two transistors increases the input voltage level at which the cell switches. While the clocking scheme tries to avoid this circumstance, it may still occur, and hence, all cells need to be verified against this failure mechanism.

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The standard approach to designing edge-triggered flip-flops has been as master—slave latches. Thus, while each cell has greater drive strength than the preceding one, it is also driving a larger capacitive load.

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Another technique that can be used to speed up a function is applicable if it consists of a number of serial functions, which can then be replaced by a set of speculative parallel operations.

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If, however, the address comes earlier than the data, the address path can be enabled allowing for a faster write. This has not happened, as many digital designs have specific needs that cannot be achieved by using standard ASIC techniques.

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