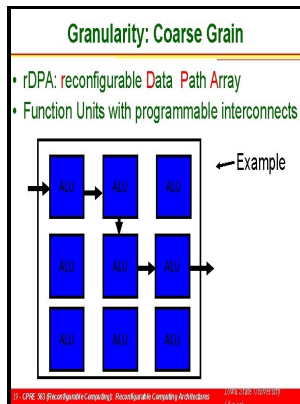# Array architecture for reconfigurable datapaths

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Notes: Thesis (M.A.Sc.)--University of Toronto, 1993.
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COARSE GRAIN RECONFIGURABLE ARCHITECTURES POLYMORPHISM IN SILICON CORES

The US has a center for high-performance reconfigurable computing CHREC. The bubblesort works with a linear chain of 'scan-max' operators producing a new sorted data word every 240 ns. In an affinity graph, nodes represent operations and edges represent affinity values.

CiteSeerX — An Array Architecture for Reconfigurable Datapath

It was not a commercial success, but was promising enough that the inventor of the , FPGA bought the technology and hired the Algotronix staff. It is extendible to arbitrarily large arrays and dynamically in-circuit reconfigurable.

Reconfigurable Computing Architectures

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COARSE GRAIN RECONFIGURABLE ARCHITECTURES POLYMORPHISM IN SILICON CORES

These works may not be reposted without the explicit permission of the copyright holder. Furthermore it consists of the x- and the y-address, the address of the DPU's configuration memory, and the data for this memory. Therefore it is possible to connect the outputs of the east south array boundary with the west north one, to build a torus.

CiteSeerX — A Dynamically Reconfigurable Wavefront Array Architecture for Evaluation of Expressions

In many cases it is useful to be able to swap out one or several of these subcomponents while the FPGA is still operating. This means that the operation will be evaluated when the required operands are available.

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