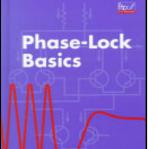
# Phase-lock basics

# John Wiley - Phase Locked Loops

Description: -

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-Phase-lock basics

Notes: Includes index.

This edition was published in 2007



Filesize: 38.85 MB

Tags: #Phase

### \* Understanding Phase

The impact of TDC resolution on PLL performance can be seen by examining a linearized model of the PLL as shown in Figure 12. The thermometer code bits are added together to form the overall TDC output.

#### Phase

Like the lock range, it too is centered on the free running frequency. Then the DC output voltage of the comparator will be a function of the phase difference between the two inputs. The loop filter removes the unwanted high-frequency components of the error signals.

#### Phase Locked Loop (PLL)

Author: Carlos Quemada Publisher: Artech House ISBN: 1596933844 Size: 35. The macimum frequency of the VCO is 500 KHz.

#### Phase

It consists of a Simulink library called the Xilinx Blockset, and software to Xtreme DSP Development translate a Simulink model into a Kit-II powered by a Virtex-II FPGA chip from Xilinx. It can demodulate FM signals with very high accuracy and reliability, or it can detect signals buried in noise, but it can't do both in a single configuration, because the two tasks require very different setups and assumptions.

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