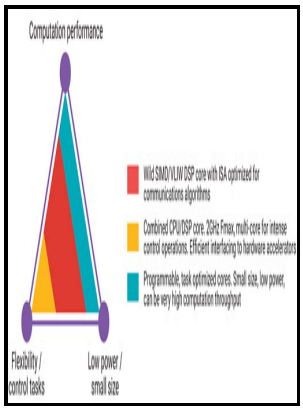
Branch prediction strategies for low power microprocessor design.

Universityof Manchester - 2



Description: -
-Branch prediction strategies for low power microprocessor design.
-Branch prediction strategies for low power microprocessor design.
Notes: Manchester thesis (M.Sc.), Department of Computer Science.
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Tags: #Techniques #to #Improve #Performance #Beyond #Pipelining: #Superpipelining, #Superscalar, #and #VLIW

Power

Out-of-order issue and retire can require extensive amounts of logic consuming extra power. And when the second half of A finishes, the CPU can start on both the second half of B and the first half of C. So a single 10-issue core would actually be both larger and slower than two 5-issue cores, and our dream of a 20-issue SMT design isn't really viable due to circuit-design limitations.

Techniques to Improve Performance Beyond Pipelining: Superpipelining, Superscalar, and VLIW

For other types of software, such as compilers and database systems, the speedup is generally much smaller, perhaps even nothing at all.

Architecture and Implementation of the ARM Cortex

. Bi-mode appears to be more successful than agree in that it's seen wider use.

Dynamic Branch Prediction

Branch target prediction attempts to guess the target of a taken conditional or unconditional jump before it is computed by decoding and executing the instruction itself.

A General Low

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The data cache, on the other hand, is usually set-associative to some degree, but often not overly so, to minimize the all-important load latency.

This next-line predictor handles as well as branch direction prediction.

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