

SOI design - analog, memory and digital techniques

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Description: -

- Silicon-on-insulator technology.

Semiconductors -- Design and construction. SOI design - analog, memory and digital techniques

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Appropriate company and government clearances MUST be obtained prior to submission. A plot of drain current vs.

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A scheme to achieve a substrate tie in PD-SOI is shown in figure 2.

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Sufficient vertical diffusion of a tank for a pMOS structure requires the tank to be diffused well below the deepest possible junction of the source and drain. If a high resistivity substrate is chosen, SOA is particularly good for integrated inductors. Variants on this device exist that allow standoff in both directions.

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Exact body voltage characteristics vary over temperature and supply voltage, since diode leakage is strongly temperature and voltage dependent.

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The AC component of body voltage is determined by capacitive coupling during switching, in particular the gate to body coupling C_{gd} and drain to body coupling C_{db} .

Silicon on insulator

A layout option for this is shown in figure 2. This exists when a stacked transistor body is connected to supply rail, resulting in large reverse bias with respect to source.

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IEEE Transactions on Electron Devices.

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The test chip has a measured access time of 25 ns with a read cycle time of 70 ns.

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