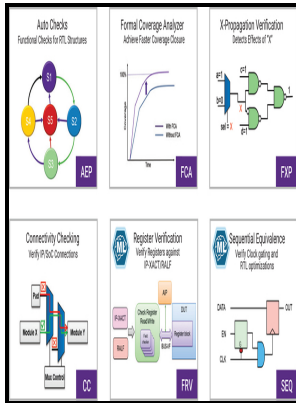# Power optimization and synthesis at behavioral and system levels using formal methods

Kluwer - Behavioral Synthesis

Description: -
-
Integrated circuits -- Very large scale integration -- Computer-aided design.
Low voltage integrated circuits -- Computer-aided design.Power optimization and synthesis at behavioral and system levels using formal methods
-Power optimization and synthesis at behavioral and system levels using formal methods
Notes: Includes bibliographical references (p. [157]-163) and index.
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Methods and tools for high and system level synthesis

In Merom, Intel's Core Duo microprocessor, we integrated Formal Verification FV with Dynamic Verification DV such that FV was also practiced by non-FV experts and replaced some traditional, simulation-based verification activities. The genetic algorithm optimization process efficiently generates tight lower bounds of the peak power dissipation for a given integrated circuit design. The drawbacks of this scheme are: 1.

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Our vacuity detection tool, VaqTree, uses these methods to detect vacuous variables, decreasing the total number of model-checking runs required to detect all sources of vacuity. However, the practical impact of low-level circuit, physical EDA solutions for power management has not been great.

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The resulting network, commonly referred to as a netlist, comprises a detailed specification defining the integrated circuit, typically in terms of a particular fabrication technology e.

Formal Methods and Toolsuites for CPS Security, Safety and Verification

Audience members will respond with open mic, confronting or supporting the panelists and giving their own brief views of the future. The results are shown in Table 1. Thus, using behavioral synthesis did not save as much effort as designing at a higher level of abstraction promised.

Related Books

- Raiders of the Western & Atlantic
- Development of Stansted Airport.
- Breve diccionario político
- DDT story
- Düyûn-ı Umûmiyeden İstanbul (Erkek) Lisesine