Microcomputer interfacing with the 8255 PPI chip

H. W. Sams - What is 8255 Programmable Peripheral Interface (PPI)? Definition, Architecture, Pin Diagram and Modes of Operation of 8255

Description: -

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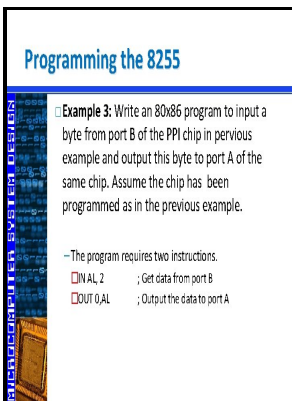Blacksburg continuing education seriesMicrocomputer interfacing with the 8255 PPI chip

Notes: Includes index.

This edition was published in 1979

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Interfacing of 8085 with 8255 Programmable Peripheral Interface

We call them as Port A, Port B, Port C upper, and Port C lower, respectively. A 0 and A 1: These are basically used to select the desired port among all the ports of the 8255 and it do so by forming conjunction with RD and WR.

Description of 8255 PPI

This feature reduces software requirement in control-based applications. Port B can work in either mode or in mode 1 of input-output mode. Port B can be programmed in mode 0 and 1.

Interfacing of 8051 with 8255 Programmable Peripheral Interface

Architecture of 8255 PPI The figure below represents the architectural representation of 8255 PPI: Let us understand the operation performed by each unit separately. All ports are set as input ports by default after reset.

8255 Programmable Peripheral Interface Chip

Larsen MICROCOMPUTER INTERFACING WITH THE 8255 PPI CHIP ISBN: 0-672-21614-0 Authors: Paul F.

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The other mode of 8255 i. Operational modes of Ports are described later. Brush up your concepts on.

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