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Prathima Agrawal

Elkin Garcia, Daniel Orozco and Guang R.

Proceedings

In addition, the long wires can be pipelined and thus do not affect the clock-cycle time and performance of individual processors in a CMP. This will be discussed in the next chapter.

El Gamal's Research Group at stanford University

In Proceedings of the 15th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPOPP 2010, pages 127—136, January 2010. Globecom'96, pp 2018-2027, Nov 18-22, 1996. Freiburg: Institute of Electrical and Electronics Engineers IEEE , 2002, p.

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Using gals architecture to reduce the impact of long wire delay on fpga performance. Message Passing on Data-Parallel Architectures.

A New Algorithm of Mobile Node Localization Based on RSSI

In ERS04: The International Conference on Engineering of Reconfigurable Systems and Algorithms, pages 213—217, Las Vegas, Nevada, June 2004. However, until recently supply voltage has scaled with technology, but power densities continued to increase. Even if one can create a

device with that current ratio, another problem arises.

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