

Automatic parallelization - new approaches to code generation, data distribution, and performance prediction

Vieweg - Autotuning for Automatic Parallelization on Heterogeneous Systems

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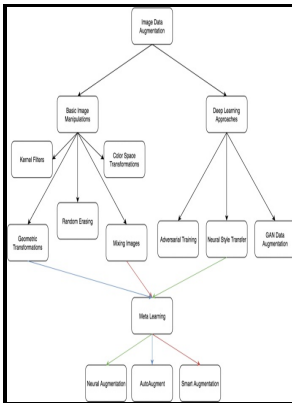
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In this method, it is proved that the parallelization can be done on binary level without array index or symbolic information. The code Generator will insert special constructs in the code that will be read during execution by the scheduler. The resulting contexts are often explicitly represented as a sequence of call sites and hence bulky.

Recent Publications of J. (Ram) Ramanujam

Programs requiring one-dimensional versus multi-dimensional time schedules are all handled with the same algorithm.

Autotuning for Automatic Parallelization on Heterogeneous Systems

C program, or even by disassembling executable code. In contrast, our approach uses ILP, including DOACROSS loop parallelism.

A novel compiler support for automatic parallelization on multicore systems

The first direction is the validation on manycore architecture similar to the one implemented in FPGA with 16 cores or more. . Although there are more than 8 cores e.

An Automatic Instruction

The target hint indicates at which cache levels it is profitable to retain data, allowing to improve cache replacement decisions at run time.

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