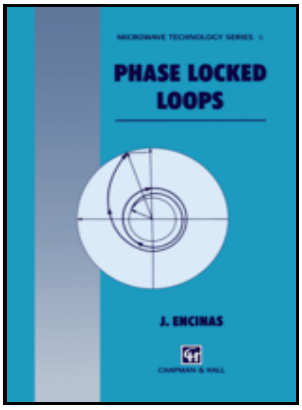
Phase-lock basics

John Wiley - Phase Locked Loops, block diagram,working,operation,Design,Applications



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Phase Locked Loops

In this test program, we have set a very low PLL loop filter cutoff frequency of 0. The value of C2 must be large enough to eliminate the variations in demodulated output and stabilize the VCO frequency.

Phase Locked Loop (PLL)

We will continue to explore PLL functionality and applications in future articles. If ϕ in t is varied slowly such that the denominator of the transfer function is still close to ω n 2, H s remains close to unity, showing that the output phase follows the input phase, which is the natural PLL definition as a tracking system.

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The locking action is made possible by , i.

Phase

A typical low-pass filter introduces some phase shift, and this has implications for feedback loop stability.

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If the VCO frequency, f o, differs from the input reference signal frequency, the phase detector sees this as a phase shift. It comprises of a logic exclusive OR circuit.

Phase Locked Loop (PLL)

In general, any noise input following the phase detector contributes to the output noise.

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