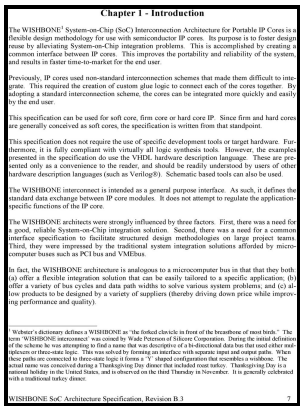
Proposed standard backplane bus specification for advanced microcomputer systems

IEEE - PICMG



Chapter 1 - Introduction

The WISHBONE[1] System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores is a flexible design methodology for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating System-on-Chip integration problems. This is accomplished by creating a common interface between IP cores. This improves the portability and reliability of the system, and results in faster time-to-market for the end user.

Previously, IP cores used non-standard interconnection schemes that made them difficult to integrate. This required the creation of custom glue logic to connect each of the cores together. By adopting a standard interconnection scheme, the cores can be integrated more quickly and easily by the end user.

This specification can be used for soft core, firm core or hard core IP. Since firm and hard cores are generally conceived as soft cores, the specification is written from that standpoint.

This specification does not require the use of specific development tools or target hardware. Furthermore, it is fully compliant with virtually all logic synthesis tools. However, the examples presented in the specification do use the VHDL hardware description language. These are presented only as a convenience to the reader, and should be readily understood by users of other hardware description languages (such as Verilog®). Schematic based tools can also be used.

The WISHBONE interconnect is intended as a general purpose interface. As such, it defines the standard data exchange between IP core modules. It does not attempt to regulate the application-specific functions of the IP core.

The WISHBONE architects were strongly influenced by three factors. First, there was a need for a good, reliable System-on-Chip integration solution. Second, there was a need for a common interface specification to facilitate structured design methodologies on large project teams. Third, they were impressed by the traditional system integration solutions afforded by microcomputer buses such as PCI bus and VMEbus.

In fact, the WISHBONE architecture is analogous to a microcomputer bus in that that they both (a) offer a flexible integration solution that can be easily tailored to a specific application, (b) offer a variety of bus cycles and data path widths to solve various system problems, and (c) allow products to be designed by a variety of suppliers (thereby driving down price while improving performance and quality).

[1] Webster's dictionary defines a WISHBONE as "the forked clavicle in front of the breastbone of most birds." The term 'WISHBONE interconnect' was coined by Wade Peterson of Silicore Corporation. During the initial definition of the scheme he was attempting to find a name that was descriptive of a bi-directional data bus that used either multiplexers or three-state logic. This was solved by forming an interface with separate input and output paths. When these paths are connected to three-state logic it forms a 'Y' shaped configuration that resembles a wishbone. The actual name was conceived during a Thanksgiving Day dinner that included roast turkey. Thanksgiving Day is a national holiday in the United States, and is observed on the third Thursday in November. It is generally celebrated with a traditional turkey dinner.

WISHBONE SoC Architecture Specification, Revision B.3 7

Description: -
-proposed standard backplane bus specification for advanced microcomputer systems
-
FUTUREBUS draft proposed standard -- P896.1
Draft -- 6.2proposed standard backplane bus specification for advanced microcomputer systems
Notes: Cover title:Specifications for advanced microcomputer backplane buses.
This edition was published in 1983

Tags: #PICMG

NuBus

This specification does not include the complete set of tests for a PCI Express System. Leaving all boxes unchecked will not limit the search criteria for this question; products with all attribute options will be returned as matches. Complete System Only: To maintain quality and integrity, this product is sold only as a completely-assembled system including 1 CPU, 1 DIMM, 20 HDDs.

Backplane Architectures Proliferate

The new class code will allow for system software to identify a controller as being attached to serial ATA devices and serial attached SCSI devices. These higher layers are not part of this standard.

Futurebus

The discussions are confined to copper cabling and their connector requirements to meet the PCI Express signaling needs at 5. ANSI Ratified VPX: Gbit Ethernet Control Plane Signal Mapping This standard supplements the VITA 46 base specification with the definition for the Gbit Ethernet signals as mapped to a VITA 46 connector. It is expected that XMC.

VPX

This interface allows the crate, including power supply, fan tray and bin temperature sensors, to be controlled and monitored remotely using either Ethernet or CAN-bus. If the information in this document contradicts IEEE 1386 or IEEE 1386. This was apparently part of an unapproved NuBus standard.

Standard specification for proposed microcomputer system backplanes P896/D2

ANSI Ratified VPX: VMEbus Signal Mapping This standard supplements the VITA 46 base specification with the definition for the VMEbus signals as mapped to a VITA 46 connector. ANSI Ratified Environments, Design and Construction, Safety, and Quality for Plug-In Units This

standard defines the unique Environments, Design and Construction, Safety, and Quality for Plug-In Module requirements related to products meant to align with the applications defined in IPC J-STD-001, Class 3. The new document will also consolidate Extended Capability definitions from the PCIe Base spec and various other PCIe specs.

5049P

This standard provides an alternative connector to the one specified in the VITA 46. Most buses up to this point conformed to the signalling and data standards of the machine they were plugged into being big or for instance.

Related Books

- Shenzhen wen bo lun cong.
- Report on Roman camp.
- Ciudad de los Césares - un estudio de teopolítica.
- Hākadhā kādū lil-Islām wa-zawwarū al-tārīkh
- Principî generali del diritto nellordine giuridico contemporaneo - 1837-1942