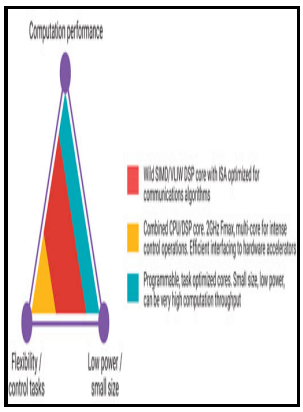
Parallel algorithms and architectures for DSP applications

Kluwer Academic Publishers - Parallel Algorithms and Architectures for DSP Applications



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Parallel algorithms and architectures for DSP applications (1991 edition)

As an example, suppose you write an efficient FIR filter program using 100 coefficients. For instance, in the SHARC DSPs, each of the two DAGs can control eight circular buffers.

Parallel Algorithms and Architectures for DSP Applications

These perfor mance requirements can be achieved by employing parallel processing at all levels.

Architecture of the Digital Signal Processor

At the top of the diagram are two blocks labeled Data Address Generator DAG , one for each of the two memories. The Super Harvard architecture takes advantage of this situation by including an instruction cache in the CPU.

Parallel Architectures For Iterative Image Restoration

Catalogue Persistent Identifier APA Citation Bayoumi, Magdy A. Most present day DSPs use this dual bus architecture.

Parallel Architectures For Iterative Image Restoration

Thakkar SequentComputerSystems The aim of the workshop was to bring together researchers working on cache coherence protocols for shared-memory multiprocessors with various.

Architecture of the Digital Signal Processor

The overriding goal is to move the data in, perform the math, and move the data out before the next sample is available.

Parallel Algorithms and Architectures for DSP Applications

The communication between the two channels has to be minimized. For instance, we might place the filter coefficients in program memory, while keeping the input signal in data memory. In simpler microprocessors this task is handled as an inherent part of the program sequencer, and is quite transparent to the programmer.

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