

HDL chip design - a practical guide for designing, synthesizing, and simulating ASICs and FPGAs using VHDL or Verilog

Doone Publications - HDL Chip Design : A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs Using VHDL or Verilog by Douglas J. Smith (1996, Hardcover) for sale online

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4
5 entity signed_adder is
6 port
7 (
8   aclr : in std_logic;
9   clk  : in std_logic;
10  a    : in std_logic_vector;
11  b    : in std_logic_vector;
12  q    : out std_logic_vector
13 );
14 end signed_adder;
15
16 architecture signed_adder_arch of signed_adder is
17   signal q_s : signed(a'high+1 downto 0); -- extra bit wide
18
19 begin -- architecture
20   assert(a'length >= b'length)
21     report "Port A must be the longer vector if different sizes!"
22     severity FAILURE;
23   q <= std_logic_vector(q_s);
24
25   adding_proc:
26   process (aclr, clk)
27   begin
28     if (aclr = '1') then
29       q_s <= (others => '0');
30     elsif rising_edge(clk) then
31       q_s <= ('0' & signed(a)) + ('0' & signed(b));
32     end if; -- clk '0
33   end process;
34
35 end signed_adder_arch;

```

Description: -

- Verilog (Computer hardware description language)

VHDL (Computer hardware description language)

Logic design -- Data processing.

Field programmable gate arrays -- Computer-aided design.

Application specific integrated circuits -- Computer-aided

design.HDL chip design - a practical guide for designing, synthesizing,

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Notes: Includes index.

This edition was published in 1996



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Since then, we have published 1+ million words of real-user reviews, 2+ million words of content from our experts and helped millions of webmasters around the world find their perfect web hosting provider, whether it is for a personal website, blog or small business. Verilog was originally developed with gate-level modeling in mind and has good constructs for modeling at this level for ASIC and FPGA library-cell primitives. Well, everyone has their own reason ought to check out some books , By Douglas J.

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An HDL is declarative to facilitate the abstract description of hardware behavior for specification. This is a great reference.

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This statement assumes the exclusion of the Verilog compiler directive language for simulation and of the PLI. VHDL can be used to describe any type of circuitry and is frequently used in the design, simulation, and testing of processors, CPUs, mother boards, , , and many other types of digital circuitry. Standard-cell devices are not configured with a basic-cell architecture, and no components are prefabricated on the silicon chip.

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An HDL looks a bit like a programming language, but has a different purpose. However, it does mean VHDL models are often more verbose and the code is often longer than its Verilog equivalent. The inputs are specified within a structure called an entity, and the self-contained logic is defined

in an architecture.

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As a result, you must be careful in writing both the compilation order of code for a single file and the compilation order for multiple files. Compared with VHDL, Verilog data types are simple, easy to use, and geared toward modeling hardware structure as opposed to abstract hardware modeling. Designers base the choice of which HDL to use not solely on technical capability, but also on personal preferences, EDA-tool availability and commercial, business, and marketing issues.

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. There are many advantages of adopting a top-down design methodology. You should carefully consider the choice of which data types to use, especially with enumerated abstract data types.

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Manufacturers define hard macros in terms of cell primitives. However, extensions are sometimes necessary to achieve desired results. A model with a signal whose type is one of the net-data types has a corresponding electrical wire in the implied modeled circuit.

Get Started with VHDL Programming: Design Your Own Hardware

The advantage of FPGAs is that they are quick and easy to program, or customize.

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