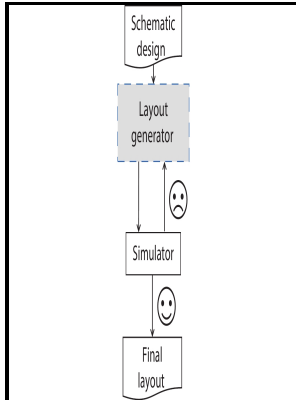


High-performance ASIC design - using synthesizable domino logic in an ASIC flow

Cambridge University Press - Low voltage dual mode logic: Model analysis and parameter extraction



Description: -

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Notes: Includes bibliographical references and index.

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ASIC Design Course

The Xilinx team is one of the strongest in the industry and we are thrilled to welcome them to the AMD family. The Dual Model Logic DML family, which was recently introduced by our group for sub-threshold operation, provides an alternative design methodology to the existing low power digital design techniques.

High Performance ASIC Design : Razak Hossain : 9780521873345

An alternate scenario may occur where parallel transistors in a standard cell switch simultaneously, leading to a smaller delay time than under characterization conditions where only a single input is assumed to change. After the course, the participants were benefitted very much. The full adder works on bits from the same binary position in the numbers being added together.

High Performance ASIC Design: Using Synthesizable Domino Logic in an ASIC Flow

Sometimes these paths cannot be further pipelined, since they have feedback requirements which require the full computational cycle to be completed every clock period. For example, in a domino AND3 gate all three inputs must be on at the same time for the internal node of the cell to be discharged and the output of the cell to rise.

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In some cases, the internal nodes may remain at 0 due to the input signals remaining low.

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