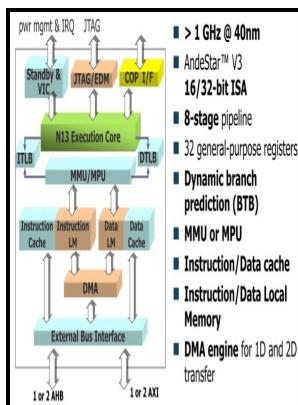# Branch prediction strategies for low power microprocessor design.

Universityof Manchester - A General Low

Description: -
-Branch prediction strategies for low power microprocessor design.
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Notes: Manchester thesis (M.Sc.), Department of Computer Science.
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Tags: #Dynamic #Branch #Prediction

A General Low

Since all mispredicts and exceptions have been resolved in the ARM integer unit, once an instruction has been issued to the NEON media engine it must be completed as it cannot generate exceptions. A 300 MHz Pentium II was also about the same speed for many things, yet it was about half that speed for floating-point code such as scientific number crunching.

Branch prediction

A case for partially TAgged GEometric history length branch prediction. For those programs, the key problem is the memory system, and yet another wall, the memory wall which we'll get to later. This type of situation is called thrashing, since the cache is not achieving anything and is simply getting in the way — despite obvious temporal locality and reuse of data, the cache is unable to exploit the locality offered by this particular access pattern due to limitations of its simplistic mapping between memory locations and cache lines.

Power

SPECint95 SPECfp95 195 MHz MIPS R10000 11.

Dynamic Branch Prediction

Write back, write through, and write-allocate policies are followed according to page table settings. Intel has been the most interesting of all to watch.

A General Low

Scaling of technology allowed the implementation of faster and larger circuits on silicon, permitting a sophisticated and powerful set of features to be integrated into CPU.

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