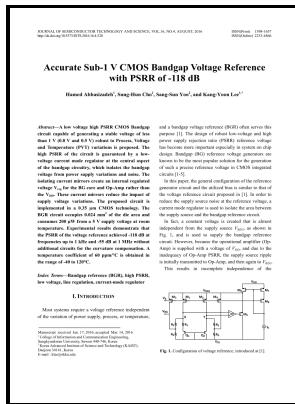


# A 1 V low power CMOS process

## National Library of Canada - A 1 V Low



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-A 1 V low power CMOS process

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Notes: Thesis (M.Sc.) -- University of Toronto, 1998.

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## A 1 V Low

In the literature, for Zigbee receivers using cascode LNAs, a number of techniques such as gain-boosting, derivative superposition technique and forward body bias have been proposed individually for improving the gain, linearity and reducing the power dissipation of the LNA respectively. The minimum noise figure is 3.

## A 1.2V low power CMOS front end for bluetooth

KW - LNA KW - CMOS KW - Ultra wide-band U2 - 10. In Proceedings of IEEE International Conference on Electronics, Circuits and Systems ICECS , pp.

## A 1

This thesis deals with the optimization of the MOSFET device structure as a means of providing 1V low power circuits in a submicron CMOS VLSI technology. The Frontend achieves a voltage gain of 37 dB, 7.

## A 1.2V low power CMOS front end for bluetooth

In this paper we present a direct and simple approach towards the LNA noise performance.... This will only be true however, if the threshold voltage can be scaled down proportionately to the supply voltage without increasing the standby current which otherwise increases due to subthreshold leakage.

## A 1.2V Low Power CMOS Front End for Bluetooth

A high gain and high linearity current-reused CMOS LNA using modified derivative superposition technique with bulk-bias control.

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