Timing and Delays:

→ The procedure for generating delays using a micro processor based system can be described step wise as shown:

(1). Determine the exact required delay.

(2) Select the instructions for delay loop

(3) Find out the no. of clock states each of required for execution of the selected delay loop instructions.
Further, find out the no. of clock states (n) to execute the loop once by adding all the individual instructions clock states.

(4) Find out the period of the clock frequency at which the microprocessor is running. (T).

(5) Find out the time required to execute the loop once ($n \times T$ seconds)

(6) Count value for the required delay (T_d) is obtained as count $N = \frac{\text{Required delay } (T_d)}{n \times T}$

Ex:- Write a program to generate a delay of 100 ms using an 8086 system, that runs on 10 MHz frequency.

Sol Required delay T_d = 100 ms.

Instruction selected	T-States
MOV CX, COUNT	4
DEC CX	2
NOP	3
JNZ label	16

∴ No. of T. states for execution of loop once
= 2 + 3 + 16 = 21.

∴ time required for execution of loop once = $21 \times \frac{1}{10\,MHz} = 2.1\,\mu s$

∴ count $N = \frac{T_d}{n \times T} = \frac{100 \times 10^{-3}}{2.1 \times 10^{-6}}$

= 47619.

∴ count $N = (47619)_{10} = (BA03H)$

The ALP to generate this delay is

```
PROC    DELAY LOCAL
ASSUME  CS : CODEP
CODEP   SEGMENT
        MOV CX, BA03H ; load count register
WAIT:   DEC CX
        NOP
        JNZ WAIT
        RET
DELAY   ENDP
```

The exact delay obtained using the above routine is

$$T_d(\text{exact}) = 0.1 \times 4 + (2+3) * 47679 \times 0.1 + 16 \times 47618 \times 0.1 + 4 \times 0.1 + 8 \times 0.1$$

$$\cong 1.00\text{ms}.$$

Note: If zero condition is satisfied JNZ takes 4 T-states otherwise it takes 16 T-states. Also MOV CX, BA03H, RET execute only once during the execution of loop.

6:- Use the ALP of previous program to design a delay of ten minutes.

Required time delay T_d = 10 minutes = 600 sec.

Instruction Selected	T-states
MOV BX, COUNT1	4
MOV CX, COUNT2	4
DEC CX	2
DEC BX	2
JNZ label	16 / 3
NOP	8
RET	

clock freq = 10 MHz $\Rightarrow T = \frac{1}{10\text{MHz}} = 0.1\,\mu s$

There will be two nested counter loops for decrementing the two counting registers. Let the first loop has a count FFFF.

Count 2 = FFFFH.

```
PROC    DELAY LOCAL

        ASSUME CS: CODE

CODE    SEGMENT

        MOV BX, COUNT1

BBB :   MOV CX, COUNT2 ; load count 2=FFFFH

CCC :   NOP

        DEC CX

        JNZ CCC

        DEC BX

        JNZ BBB

        RET

DELAY   ENDP

CODE    ENDS

        END
```

Inner loop requires:

$$T_1 = 0.1 \times 4 + (2+3+16) \times 65535 \times 0.1$$

$$= 0.137605 \text{ seconds.}$$

outer loop requires $T_2 = 0.137605 + (16+2) \times 10^{-6} \times 0.1$

for one iteration $= 0.1376068$ second.

Required delay $= T_d = 10 \times 60 \text{ sec} = 600 \text{ sec.}$

$$\therefore \text{COUNT1} = \frac{T_d}{T_2} = \frac{600}{0.1376068} = 4359.58.$$

$$= (4360)_{10}$$

$$= (1107)_H.$$