

# DMA CONTROLLER 8257

## Features:

It is a 4-channel DMA.

- So 4 I/O devices can be interfaced to DMA

- It is designed by Intel

- Each channel have 16-bit address and 14 bit counter

- It provides chip priority resolver that resolves priority of channels in fixed or rotating mode.

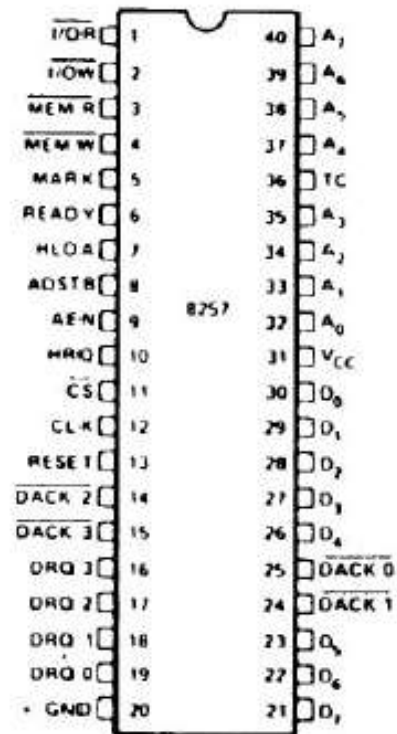
- It provide on chip channel inhibit logic.

- It generates a TC signal to indicate the peripheral that the programmed number of data bytes have been transferred.
- It generates MARK signal to indicate the peripheral that 128 bytes have been transferred.
- It requires single phase clock.

The maximum frequency is 3Mhz and minimum frequency is 250 Hz.

- It execute 3 DMA cycles
  - 1.DMA read
  - 2.DMA write
  - 3.DMA verify.
- It provide AEN signal that can be used to isolate CPU and other devices from the system bus.
- It is operate in two modes.
  - 1.Master Mode
  - 2.Slave Mode

# Pin Diagram of DMA controller



# Description of pin diagram

- D0-D7:
- it is a bidirectional ,tri state ,Buffered ,Multiplexed data (D0-D7)and (A8-A15).
- In the slave mode it is a bidirectional (Data is moving).
- In the Master mode it is a unidirectional (Address is moving).

- IOR:

- It is active low ,tristate ,buffered ,Bidirectional lines.
- In the slave mode it function as a input line. IOR signal is generated by microprocessor to read the contents 8257 registers.
- In the master mode it function as a output line. IOR signal is generated by 8257 during write cycle

- IOW:
- It is active low ,tristate ,buffered ,Bidirectional control lines.
- In the slave mode it function as a input line. IOR signal is generated by microprocessor to write the contents 8257 registers.
- In the master mode it function as a output line. IOR signal is generated by 8257 during read cycle

### CLK:

- It is the input line ,connected with TTL clock generator.
- This signal is ignored in slave mode.

### RESET:

- Used to clear mode set registers and status registers

### A0-A3:

These are the tristate, buffer, bidirectional address lines.

In slave mode ,these lines are used as address inputs lines and internally decoded to access the internal registers.

In master mode, these lines are used as address outputs lines,A0-A3 bits of memory address on the lines.



## CS:

- It is active low, Chip select input line.
- In the slave mode, it is used to select the chip.
- In the master mode, it is ignored.

## A4-A7:

These are the tristate, buffer, output address lines.

In slave mode ,these lines are used as address outputs lines.

In master mode, these lines are used as address outputs lines,A0-A3 bits of memory address on the lines.

## READY:

- It is an asynchronous input line.
- In master mode,
- When ready is high it receives the signal.
- When ready is low, it adds wait state between S1 and S3
- In slave mode, this signal is ignored.

## HRQ:

- It is used to receive the hold request signal from the output device.

### HLDA:

- It is acknowledgment signal from microprocessor.

### MEMR:

- It is active low ,tristate ,Buffered control output line.
- In slave mode, it is tristated.
- In master mode ,it activated during DMA read cycle.

### MEMW:

- It is active low ,tristate ,Buffered control input line.
- In slave mode, it is tristated.
- In master mode ,it activated during DMA write cycle.

### AEN (Address enable):

- It is a control output line.
- In master mode ,it is high
- In slave mode ,it is low
- Used it isolate the system address ,data ,and control lines.

### ADSTB: (Address Strobe)

- It is a control output line.
- Used to split data and address line.
- It is working in master mode only.
- In slave mode it is ignore.

## TC (Terminal Count):

- It is a status of output line.
- It is activated in master mode only.
- It is high ,it selected the peripheral.
- It is low ,it free and looking for a new peripheral.

## MARK:

- It is a modulo 128 MARK output line.
- It is activated in master mode only.
- It goes high ,after transferring every 128 bytes of data block.

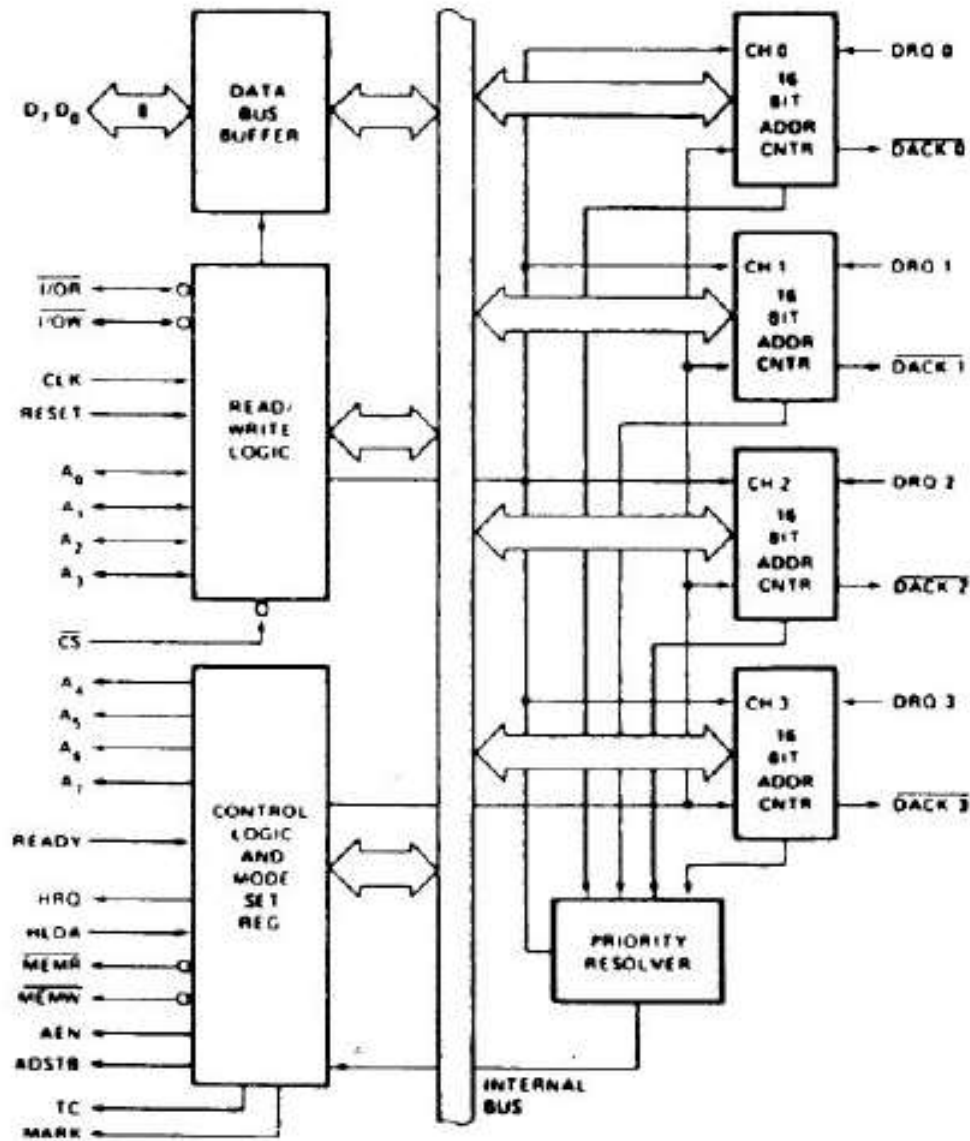
### DRQ0-DRQ3(DMA Request):

- These are the asynchronous peripheral request input signal.
- The request signals is generated by external peripheral device.

### DACK0-DACK3:

- These are the active low DMA acknowledge output lines.
- Low level indicate that ,peripheral is selected for giving the information (DMA cycle).
- In master mode it is used for chip select.

# 8257 BLOCK DIAGRAM



# Description

- It containing Five main Blocks.
  1. Data bus buffer
  2. Read/Control logic
  3. Control logic block
  4. Priority resolver
  5. DMA channels.



## DATA BUS BUFFER:

- It contains tristate, 8 bit bi-directional buffer.
- Slave mode, it transfers data between microprocessor and internal data bus.
- Master mode, the outputs A8-A15 bits of memory address on data lines (Unidirectional).

## READ/CONTROL LOGIC:

- It controls all internal Read/Write operation.
- Slave mode, it accepts address bits and control signal from microprocessor.
- Master mode, it generates address bits and control signal.

## Control logic block:

- It contains ,
  1. Control logic
  2. Mode set register and
  3. Status Register.

## CONTROL LOGIC:

- Master mode ,It control the sequence of DMA operation during all DMA cycles.
- It generates address and control signals.
- It increments 16 bit address and decrement 14 bit counter registers.
- It activate a HRQ signal on DMA channel Request.
- Slave ,mode it is disabled.

## MODE SET REGISTERS:

- It is a write only registers.
- It is used to set the operating modes.
- This registers is programmed after initialization of DMA channel.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
AL	TCS	EW	RP	EN <sub>3</sub>	EN <sub>2</sub>	EN <sub>1</sub>	EN <sub>0</sub>

- AL=1=Auto load mode

AL=0=Rotating mode

- TCS=1=Stop after TC (Disable Channel)

- TCS=0=Start after TC (Enable Channel)

- EW=1=Extended write mode

- EW=0=normal mode.

- RP=1=Rotating priority

- RP=0=Fixed priority.

- $EN_3=1$ =Enable DMA CH-3
- $EN_3=0$ =Disable DMA CH-3
  
- $EN_2=1$ =Enable DMA CH-2
- $EN_2=0$ =Disable DMA CH-2
  
- $EN_1=1$ =Enable DMA CH-1
- $EN_1=0$ =Disable DMA CH-1
  
- $EN_0=1$ =Enable DMA CH-0
- $EN_0=0$ =Disable DMA CH-0

## STATUS REGISTERS:

- It is read only registers.
- It is tell the status of DMA channels
- TC status bits are set when TC signal is activated for that channel.
- Update flag is not affected during read operation.
- The UP bit is set during update cycle . It is cleared after completion of update cycle.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	UP	TC <sub>3</sub>	TC <sub>2</sub>	TC <sub>1</sub>	TC <sub>0</sub>

- UP=Update flag
- UP=1=8257 executing update cycle
- UP=0=8257 executing DMA cycle

- TC<sub>3</sub>=1=TC activated CH-3
- TC<sub>3</sub>=0=TC deactivated CH-3

- TC<sub>2</sub>=1=TC activated CH-2
- TC<sub>2</sub>=0=TC deactivated CH-2

- $TC_1=1$ =TC activated CH-1
- $TC_1=0$ =TC deactivated CH-1
- $TC_0=1$ =TC activated CH-0
- $TC_0=0$ =TC deactivated CH-0
- The address of status register is  $A_3A_2A_1A_0=1000$ .

### FIRST/LAST FLIP FLOP:

- 8257 have 8bit data line and 16 bit address line.
- 8085 it is getting 8-bit data in simultaneously.
- 8085 can not access 16-bit address in simultaneously.



- A0-A3 lines are used to distinguish between registers ,but they are not distinguish lower and higher address.
- It is reset by external RESET signal.
- It is also reset by whenever mode set register is loaded.
- So program initialization with a dummy (00 H).
- FF=1=Higher byte of address
- FF=0=Lower byte of address.

# Modes of Operation

- Rotating priority Mode:
- The priority of the channels has a circular sequence.
- Fixed Priority Rotating Mode:
- The priority is fixed.
- TC Stop Mode
- Auto Load mode
- Extended Write mode