# The 8085 Machine cycles and Bus timings:

→ The 8085 microprocessor is designed to execute 74 different types of instructions.

→ Each instruction has two parts:
opcode and operands.

The opcode is a command such as ADD and the operation is an object to be operated on, such as a byte or the contents of a register.

→ Some instructions are 1-byte and some are multi-byte.

To execute an instruction, 8085 needs to perform various operations such as memory read/write and I/O Read/write.

There is no direct relationship between the no. of bytes of an instruction and the no. of operations 8085 has to perform.

→ All instructions are divided into few basic machine cycles and these machine cycles are divided into precise system clock periods.

→ Basically microprocessor external communication functions can be divided into three categories:

(1) Memory Read and Write
(2) I/O Read and write
(3) Request Acknowledge.

These functions are further divided into various operations (machine cycles) as shown below which involve: opcode fetch, memory read, memory write, I/O read, I/O write, Interrupt acknowledge, Halt, Hold, Reset.

These machine cycles are further divided into T-States.

→ We will understand the first three operations

- → opcode fetch
- → memory read
- → memory write

} machine cycles

→ We will examine the signals on various buses in relation to system clock.

Opcode fetch Machine Cycle:

→ This is the first operation in any instruction.

Ex:- Illustrate the steps and timing diagram of data flow when the instruction code 0100 1111 (4FH → MOV C, A), stored in location 2005H is being fetched.

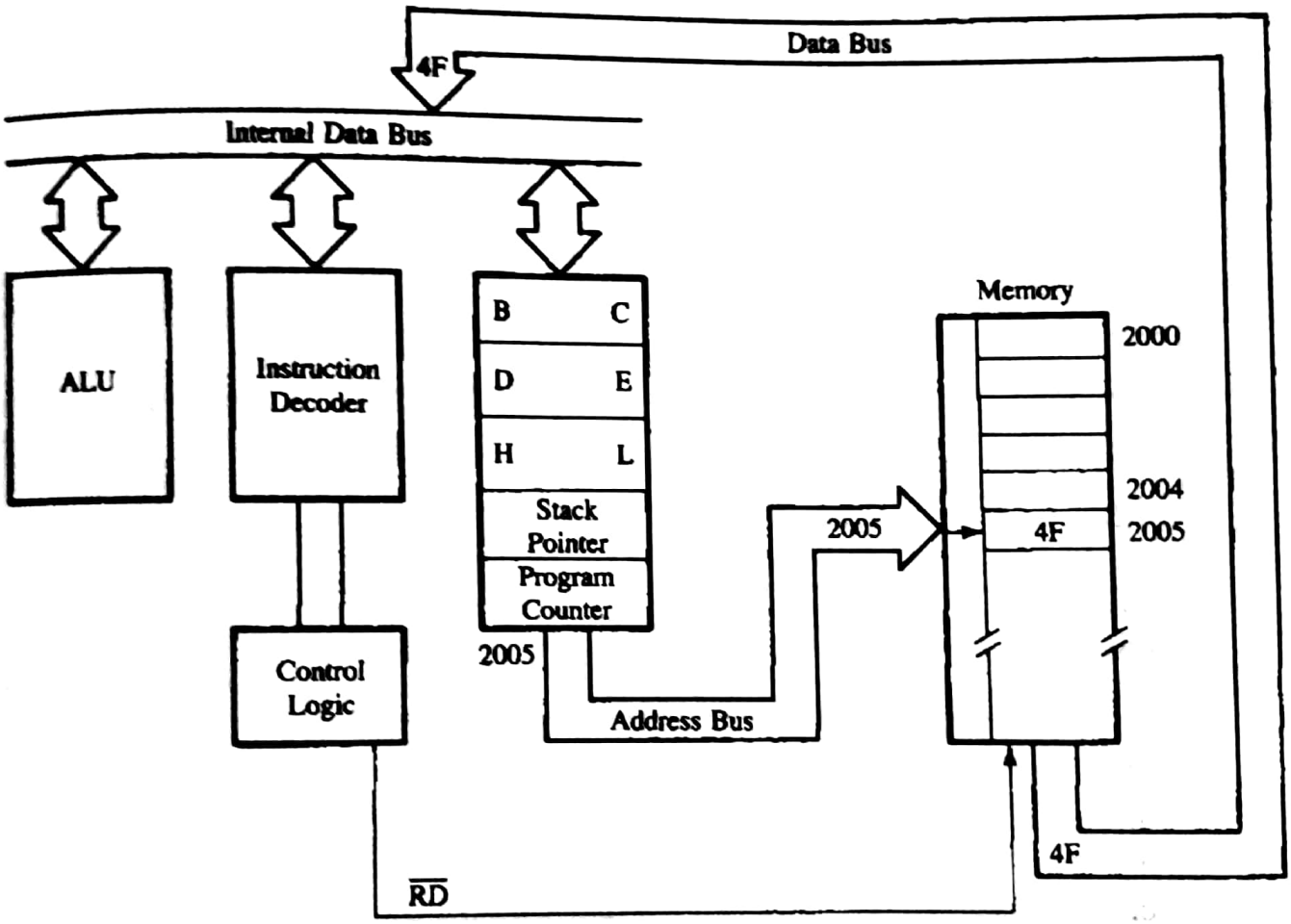


**FIGURE 4.2**
**Data Flow from Memory to the MPU**

The steps involved are

(1) The microprocessor places the 16 bit memory address from PC on the address bus

(2) The control unit sends the control signal $\overline{RD}$ to enable the memory chip

(3) The byte from memory location is placed on data bus.

(4) The byte is placed in the instruction decoder of the microprocessor and the task is carried out according to the instruction.

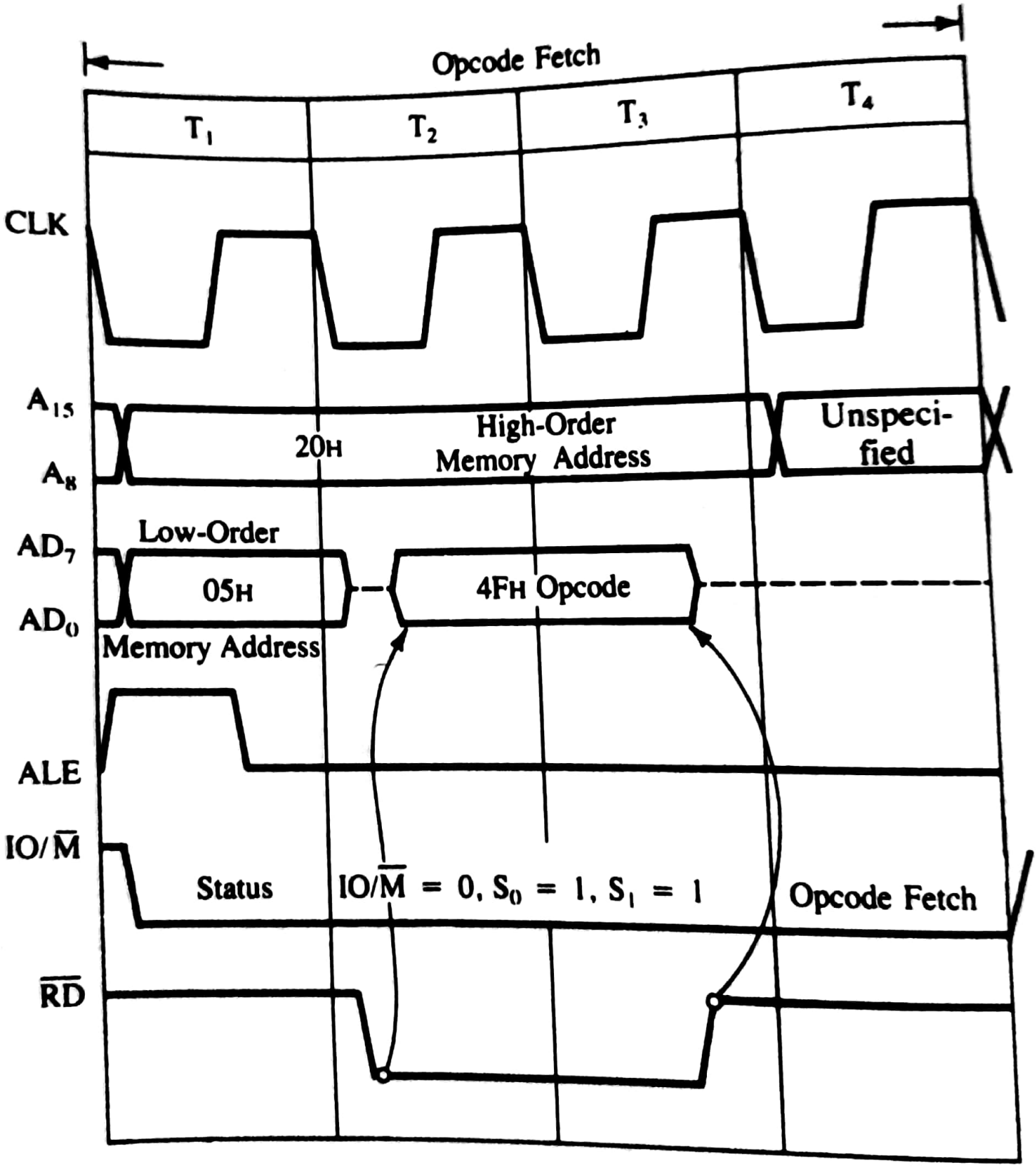


**FIGURE 4.3**
Timing: Transfer of Byte from Memory to MPU

Thus opcode fetch cycle is called the $M_1$ cycle and has four T-states. 8085 uses first three T states ($T_1 - T_3$) to fetch the code and $T_4$ to decode and execute the opcode.

→ In 8085 instruction set, some instructions have opcodes with six T-states.

## Memory Read Machine Cycle:

To understand the Memory read machine cycle, we need to examine the execution of a 2 byte or 3 byte instruction because in a 1 byte instruction, the machine code is an opcode; therefore, the operation is always an opcode fetch.

The execution of a 2 byte instruction is explained next:

Ex:- Two machine codes 00 11 1110 (3EH) and 00 11 0010 (32H) — are stored in memory locations 2000H and 2001H respectively.

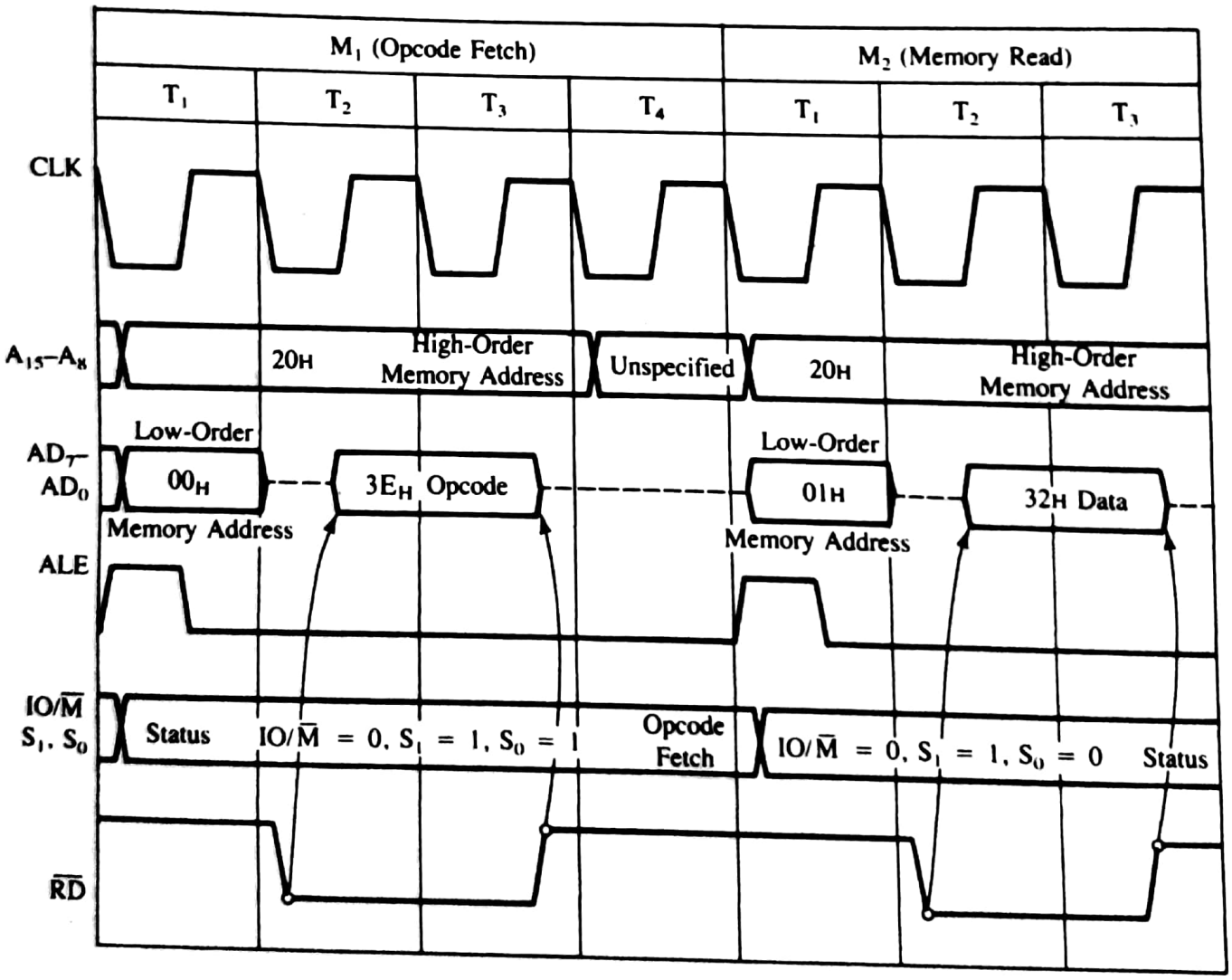


**FIGURE 4.10**
8085 Timing for Execution of the Instruction MVI A,32H

The execution times of the memory Read machine cycle and the instruction cycle are calculated as follows :

→ clock frequency $f = 2MHz$

→ T-state = clock period = $\frac{1}{f} = 0.5\,\mu s$

→ Execution time for opcode fetch

$= (4T) \times 0.5\,\mu s = 2\,\mu s$

→ Execution time for memory read

$= (3T) \times 0.5\,\mu s = 1.5\,\mu s$

→ Execution time for instruction : $7T \times 0.5$

$= 3.5\,\mu s.$

Explain the machine cycles of the following 3-byte instruction when it is executed.

| Opcode | Operand | Bytes | Machine Cycles | T-States | Operation |
|---|---|---|---|---|---|
| STA | 2065H | 3 | 4 | 13 | This instruction stores (writes) the contents of the accumulator in memory location 2065H |

The machine codes are stored in memory locations 2010H, 2011H, and 2012H as follows: the 16-bit address of the operand must be entered in reverse order, the low-order byte first, followed by the high-order byte.

| Memory Address | Machine Code | | |
|---|---|---|---|
| 2010 | 0011 | 0010 → 32H | Opcode |
| 2011 | 0110 | 0101 → 65H | Low-order address |
| 2012 | 0010 | 0000 → 20H | High-order address |

1. In the first machine cycle, the 8085 places the address 2010H on the address bus and fetches the opcode 32H.
2. The second machine cycle is Memory Read. The processor places the address 2011H and gets the low-order byte 65H.
3. The third machine cycle is also Memory Read; the 8085 gets the high-order byte 20H from memory location 2012H.
4. The last machine cycle is Memory Write. The 8085 places the address 2065H on the address bus, identifies the operation as Memory Write ($IO/\overline{M} = 0$, $S_1 = 0$, and $S_0 = 1$). It places the contents of the accumulator on the data bus $AD_7$–$AD_0$ and asserts the $\overline{WR}$ signal. During the last T-state, the contents of the data bus are placed in memory location 2065H.