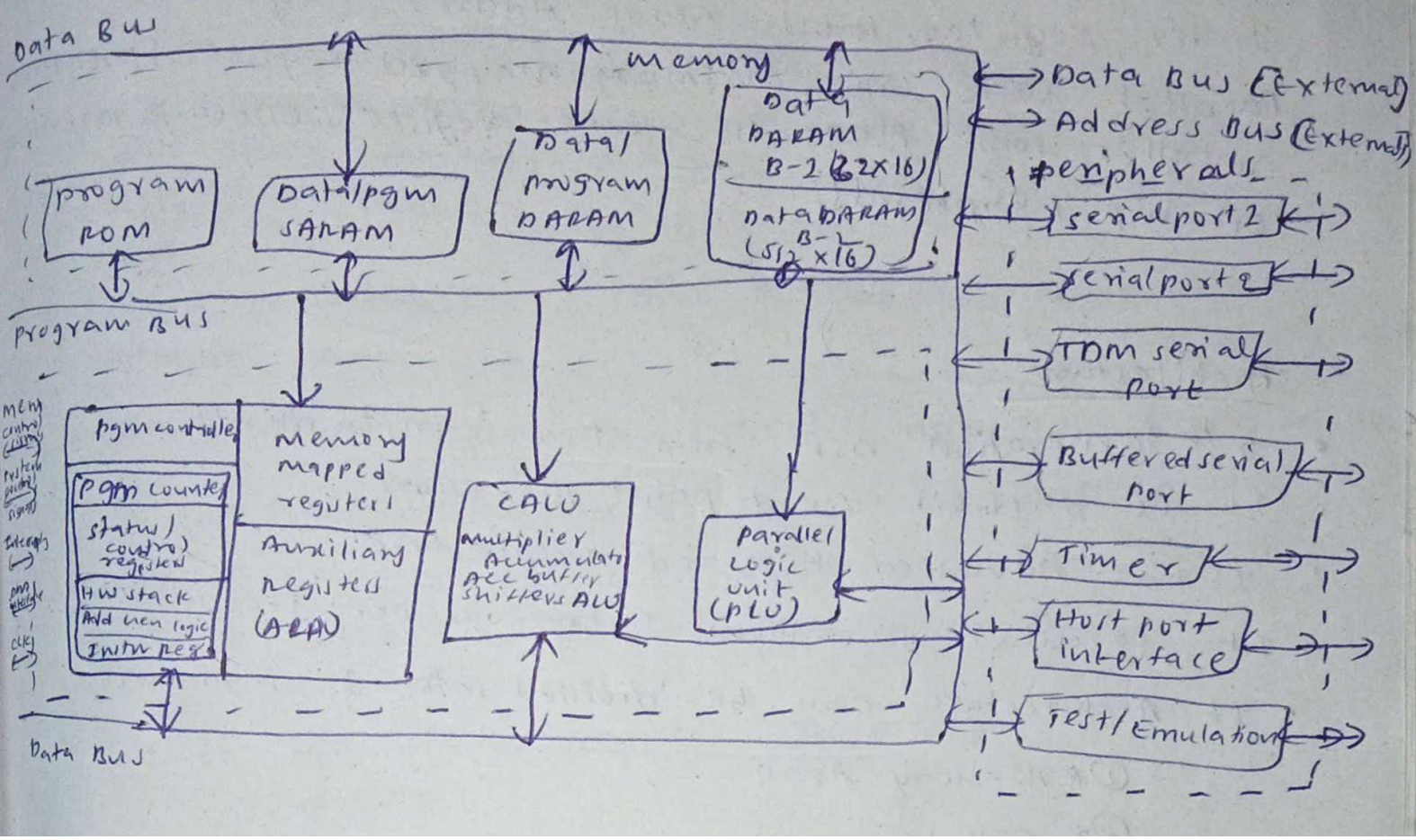
UNIT-5

-) TMS320C5X:

Architecture:



• UNIT-5: DSP PROCESSORS:

• Architecture of TMS320C5X: Introduction, Bus structure, central ALU, Auxiliary register ALU, Index register, Block Move Address register, Parallel logic unit, memory mapped registers, program controller, some flags in status-registers, on-chip memory on-chip peripherals.

• Architecture:

• 5th generation DSP from Texas instruments.
• It is a 16-bit fixed point processors
• It has Advanced Harvard Architecture
• It executes 50 million Instructions per second (MIPS)
• It Architecture can be divided into 3 segments:-
  ① * Memory Area
  ② * CPU
  ③ * Peripherals
• It consists of programmable timer & PLL
  - IEEE standard JTAG ports
  - DMA Interface
  - 5V/3V operation for low power dissipation & power down modes.
• It is a single ~~instruction~~ cycle with 20-50ns speed.

① Memory organisation: / on-chip memory:- used to store data permanently.
  ④ - It consists of program ROM of 2K to 32K words
  ③ - It contains DARAM, which consists of 3 Blocks: B0, B1, B2
  ② - It has SARAM with size of 1K to 9K word.
  → External devices has no acess to PROM.
  → - stands for single Acess RAM.
  - we can store either data/program/both.
  → Double/Dual acess RAM
  • "B0": can store either data/program.
    - Has memory of 512x16 RAM
  • "B1": only data is stored
    • Has memory of 512x16
  • "B2": only data is stored
    • size is 301x16

  } total size is = 1056 words

External memory:

→ It has 64K×16 bit external program memory
→ It can store " " " data memory
→ Has " " " IO Address space.

- 32 K global data memory space: It can share data with other peripherals within system.

② CPU: - contains following 5 parts:-

① program controller contains all devices that decodes instruction and CPU execution.

- can execute three concurrent instructions simultaneously.
- It contains PC, registers, HW stack, ADL, IR.
  - PC is a 16 bit counter, contains address of instruction to be executed next.
  - 16 bit status registers, They are:-
    * ST0
    * ST1
    * PMST: processor mode status register
    * CBCR: circular Buffer control register
  - Hardware stack has 16×16 size.
  - ADL generates addresses based on instructions.
  - IR stores instructions

③ Memory mapped registers:

The c5x has 96 registers mapped into page '0' of the data memory space. This memory mapped register space contains various controls and status registers including those for CPU, serial port, timer & software wait generators.

Additionally, the 1st 16 I/O port locations are mapped into this data memory space, allowing them to be accessed either as data memory using single word instruction or as I/O locations with two-word instruction.

③ Auxiliary register arithmetic unit (ARAU):

C5x consists of a register file containing eight auxiliary registers (AR0-AR7) each of 16-bit length, a 3-bit auxiliary register pointer (ARP) and an unsigned 16 bit ALU. The auxiliary register file is connected to the auxiliary register arithmetic unit

④ parallel logic unit (PLU):

PLU is another logic unit that executes logic operations on data without affecting the contents of the accumulator. The multiplier bit in a status/control register (or) any memory location can be directly set, clear, test (or) toggled by the PLU. After executing the logical operation, PLU writes the result of the operation to the same memory location from which the first Operand was fetched.

⑤ central Arithmetic logic unit (CALU):-

- CPU uses CALU to perform 2's complement arithmetic. It consists of the following:
  1. parallel multiplier (16x16 bit)
  2. Accumulator (32 bit)
  3. Accumulator buffer (ACCB) (32 bit)
  4. product register (PREG)
  5. shifters
  6. ALU (32 bit)

- All 32 bit signed/unsigned multiplication operations can be performed in parallel multiplier within one machine cycle.
- All multiply instructions except the MPYU instruction perform a signed multiply operation in the multiplier.
- one of the operand to the multiplier is from 16-bit temporary register (TREG0) and the second input is from the program bus/data bus.
- The product register (PREG) holds the product.

The 32 bit ALU along with 16-bit accumulator carries out arithmetic and logic operations executing most of them in one machine cycle.

- Here, the accumulator provides one of the inputs to the ALU, whereas the PREG, accumulation buffer / scaling shifter output provides second input. The results of of operations are stored in accumulator.

- Scaling shifter has a 16-bit input connected to the data bus and a 32-bit output connected to ALU. The scaling shifters produce a left shift of 0 to 16 bits on i/p data.

- A 5-bit register (TREG1) specifies number of bits by which the scaling shifter should shift (or) shift count is specified by a constant embedded in instruction word.

③ peripherals:-

All C5X DSPs have same CPU structure; however, they have different on-chip peripherals connected to their CPUs.

- A TMS320C50 dsp processor contains following on-chip peripherals:-

* clock generator:-
* Hardware timer:-
* software programmable wait stage generators:-
* General purpose I/O pins
* parallel I/O ports
* serial port Interface
* Buffered serial port
* TDM serial port
* Host port interface
* User maskable interrupts

BUS structure:

- seperate program and data buses in advance Harvard architecture of c5x maximize the processing power and provide a high degree of parallelism.
- Many DSP applications are accomplished using single cycle multiply / accumulate instruction with a data move option.
- The c5x included the control mechanism to manage interrupts, repeated operations and functions calling.
- The c5x architecture has 4 buses:-
  - program bus (PB)
  - program address read bus (PRB)
  - Data read bus (DB)
  - Data read address bus (DRB)
- The (PB) program Bus carries the instruction code & immediate operands from program memory to CPU.
- The program address bus provides address to program memory space for both read & write.
- The data read bus interconnects various elements of CPU to data memory space.
- The Data read address bus provides address to acess data memory space.

→ Addressing modes:-

- TMS320c5x processor supports 6 types of addressing modes:
  1. Immediate:
  2. Absolute

① operand is specified in instruction directly.
- It can be 3,5, 7, 8/9-bit length called as short operand.
- ~~The~~ requires only one memory location.
- It can also be 16 bit length called "long word".
- ~~The~~ requires 2 memory locations which are consecutive

ex: LD # 20, DP
= RPT # 0FFFFh

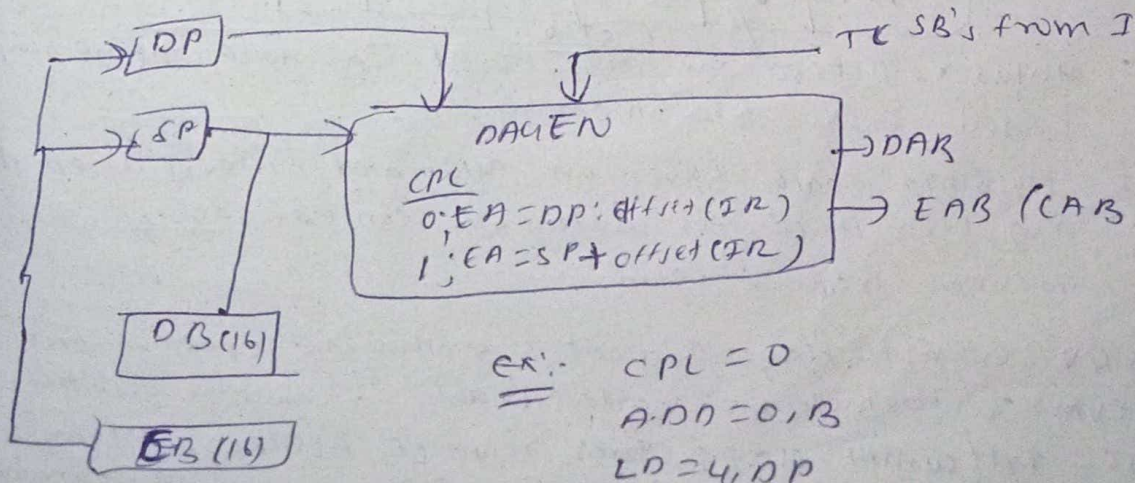
② Absolute AM: (~~direct memory addressing~~)
- Address of operand is specified in instruction directly

ex: MVKD 1000h, *AR3
= MVPD 2000h, *AR5
LD @1000h, A

③ Accumulator addressing:
- Assign the accumulator contents as address in instruction and the address is used to transfer the data b/w mem→mem.
- ~~Read & write~~ READA & WRITEA are used to transfer data.

ex:
- READA *AR2
↓
used to transfer word from program mem to data mem.
- WRITEA *AR3
↓
From data mem to program memory

④ Direct AM: DP ← [9-bits | 7-bits] → IR
- 16 bit address is generated using DAGenerator.

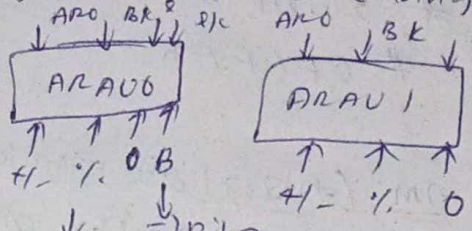


ex: CPL = 0
ADD = 0, B
LD = 4, DP

⑤ Indirect AM:-

- Data is accessed indirectly by means of Auxiliary registers
- There are 8-16 bit Auxilary registers (AR0 → AR7)
- we use this AM when we want to acess data items of certain no. of steps.
- values of Auxilary register can be changed using

*ARAU0
*ARAU1



=) Bit reversed addressing mode
=) circular addressing mode

Ex: *AR3+0

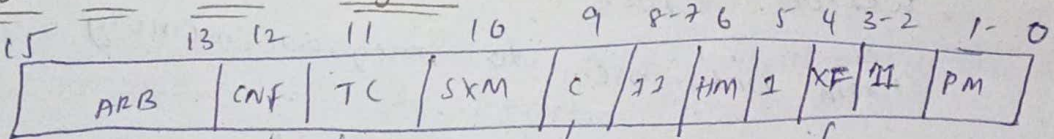
*+AR3(40h)

⑥ circular addressing mode:-

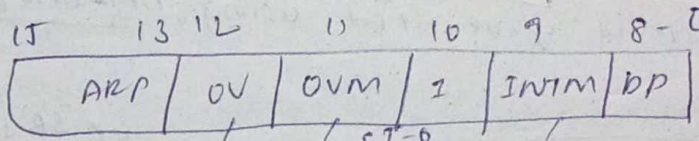
It is one of the specialized addressing modes available for signal processing applications in that of circular addressing.

In most real time signals processing applications, like filtering, input is an infinite stream of data samples. These are windowed and used in filtering applications

* Flags in status Register:-



* ST1-Bit assaignment *



- status registers can be stored in data mememory & loaded from data memory.
- ST0 & ST1 each have an associated 1-level deep shadow register stack for automatic context-saving when an interrupt trap is taken.

* OV : overflow flag : Indicates arithmetic operation overflow in ALU.
* OVM : Overflow mode bit : enables/disables accumulator overflow saturation mode
* TC : Test/control flag : Stores result of ALU/PLU. Determines if conditional branch, call & return instructions

- ARB holds previous value contained in ARP.
- CNF enables on-chip dual access RAM B0
  CNF = 0 => DARAM in data memory
  CNF = 1 => DARAM in ~~data~~ program memory
- SXM: sign extension mode bit: Enables/disables sign extension of an arithmetic operation
- C: carry bit: result is carry/not
- HM: Hold mode bit: determine whether CPU stops/continues execution
- XF: external Flag: Determines level of XF output pin.
- PM: product shift mode bits: Determines product shifter modes & shift value for PREG o/p
- ARP: Auxilliary register pointer:- selects AR to be used in indirect addressing
- INTM: Interrupt mode:- Globally masks/enables all interrupts