


Operands: w bits

True sum w/ bits

Discard carry: \sim bits
进位 \nwarrow

• standard Addition Function

Ignores carry output

• Implements Modular Arithmetic

$$s = \text{UAdd}_w(u, v) = u + v \bmod 2^w.$$

Integer Addition

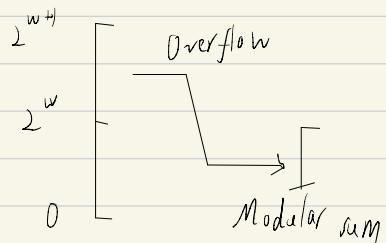
- ① 4-bit integers u, v
- ② compute true sum $\text{Add}_4(u, v)$
- ③ Values increase linearly with u and v .
- ④ forms planar surface.

Wraps Around:

If true sum $\geq 2^w$.

At most once.

True sum:



TAdd and UAdd have Identical Bit-Level Behavior.

- Signed v.s. unsigned addition in C:

int s, t, u, v;

s = int(unsigned(u) + unsigned(v));

t = u+v

will give s == t

e.g. 1.

$$\begin{array}{r} \text{1101} & - 3 \\ \underline{+ 0101} & \\ \text{X} \textcircled{0} \text{010} & 5 \\ \text{---} & 2 \end{array}$$

A handwritten binary addition diagram. The top row has '1101' above a minus sign and '3' below it. The bottom row has '0101' above a plus sign. A red circle highlights the first column from the right where a '0' is written over a '1'. A red arrow points from this circled '0' down to the carry line, which is labeled '2' at its end.

e.g. 2.

$$\begin{array}{r} 0111 & 7 \\ 0101 & 5 \\ \hline 1100 & -4 \end{array}$$

A handwritten binary addition diagram. The top row has '0111' above a '7'. The bottom row has '0101' above a '5'. The result row has '1100' above a minus sign and '4' below it. The diagram shows standard binary addition without any circled digits or arrows.

TAdd Overflow

Functionality.

- (i) True sum requires $w+1$ bits
- (ii) Drop off MSB (most significant bit)
- (iii) Treat remaining bits as 2's comp. integer.

Visualizing 2's complement Addition.

(I) Values

- (i) 4-bit two's comp.
- (ii) Range from -8 to +7.

(II) Wraps Around.

- (i) If $\text{sum} \geq 2^{w-1}$
 - Becomes negative
 - At most once
- (ii) If $\text{sum} < -2^{w-1}$
 - Becomes positive
 - At most once

Multiplication.

(I) Goal: computing Product of w -bit numbers x, y .
Either signed or unsigned.

(II) But, exact results can be bigger than w bits:

(i) Unsigned: up to 2^w bits

$$\cdot \text{Result range: } 0 \leq x * y \leq (2^w - 1)^2 = 2^{2w} - 2^{w+1} + 1$$

(ii) Two's complement min (negative): Up to 2^{w-1} bits

$$\cdot \text{Result range: } x * y \leq (-2^{w-1}) * (2^{w-1} - 1) = -2^{2w-2} + 2^{w-1}$$

(iii) Two's complement max (positive): Up to 2^w bits, but only for $(T_{Minw})^2$.

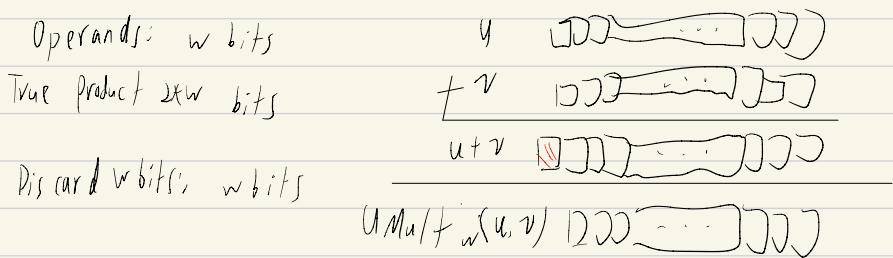
$$\cdot \text{Result range: } x * y \leq (-2^{w-1})^2 = 2^{2w-2}.$$

so, maintaining exact results...

(i) would need to keep expanding word size with each product computed

(ii) is done in software, if needed.

• e.g. by "arbitrary precision" arithmetic packages.



(i) Standard Multiplication Function:
 (ii) Ignores high order w bits,

(II) Implements Modular Arithmetic

$$\text{UMult}_w(u, v) = u \cdot v \bmod 2^w.$$

e.g.

$$\begin{array}{r} 3 * 5 \\ = 15 \end{array} \quad \text{OK}$$

$$\begin{array}{r} 5 * 5 \\ = 0(1010) \\ \begin{array}{l} 2^4 2^3 2^2 \\ = 9 \text{ (rather than 25)} \end{array} \end{array}$$

discard

Signed Multiplication in C.

Operands: w bits

standard multiplication Function:

- (i) ignores high order w bits
- (ii) some of which are different for signed vs.

unsigned multiplication

- (iii) lower bits are the same.

4 bits

5 times

101	
101	
101	
101	

101
0100
= $(2^3) + 2^0 = \text{minus } 7$

discard ←

Power-of- b multiply with shift

(ii) Operations:

(i) $a \ll b$ gives $a \times 2^b$

Both signed and unsigned.

Operands: w bits.

historically, shift operation is much faster than multiplication operation.

Unsigned Power-of-2 divide with shift.

I Quotient of Unsigned by Power of 2.

(i) $u \gg k$ gives $[u/2^k]$

(ii) Uses logical shift. (filled with 0) (NOT arith. shift filled with 1)

unsigned case:

$$\begin{array}{c} 0|10 \\ 00|1 \\ 000| \end{array} \quad \begin{array}{c} (6)_{10} \\ 6 \gg 1 \\ 6 \gg 2 \end{array} \quad \begin{array}{c} (3)_{10} \\ (1)_{10} \end{array}$$

signed case:

$$\begin{array}{c} 10|0 \\ 010| \\ 110| \end{array} \quad \begin{array}{c} (-6) \\ (-6 \gg 1) \\ (-6 \gg 2) \end{array} \quad \begin{array}{c} (-3) \\ (-3) \\ (-2) \end{array} \quad \text{(arith. shift)}$$

division still much slower than right-shift.

So, compiler does it with shifting and tweaking (like $\lceil \rceil$ things around it ...)

$X \rightarrow -X$ step(i); complement step(i); increment

$$\begin{array}{r} \text{flip} + \begin{array}{r} 1010 \\ 010 \\ + 000 \end{array} \mid \quad - 6 \\ \hline 0110 \end{array} \quad \begin{array}{r} \text{+} \quad \begin{array}{r} 0110 \\ 100 \\ + 000 \end{array} \\ \hline 1010 \end{array}$$

>> Java logical shift
>> C arithmetic shift.

check } error-so/n.c
} error-soln1.c.

Byte - Oriented Memory Organization.

00000000

FF FF FF FF



(I) Programs refer to data by address.

(i) Conceptually, envision it as a very large array of bytes

(ii) In reality, it's not, but can think of it that way.

(II) An address is like an index into that array.

and a pointer variable stores an address

(III) Note: system provides private address spaces to each "program"

(i) Think of a process as a program being executed

(ii) So, a program can clobber its own data but not that

of others.

↳ clobbering: To overwrite, usu. unintentionally; "I walked off the end of the array and clobbered the stack."

Machine Words.

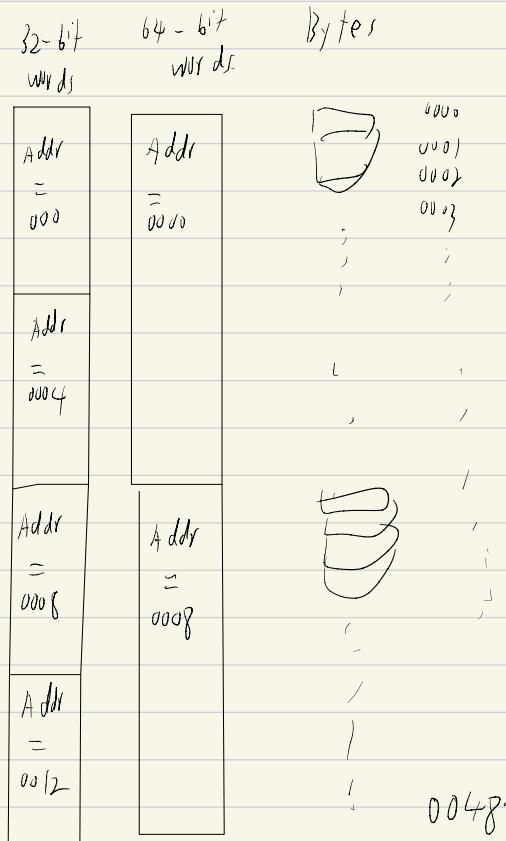
It refers to the number of bits processed by a computer's CPU in one go.

- (i) Any given number has a "Word Size": (these days, typically 32 bits or 64 bits)
- (ii) Nominal size of integer-valued data and of address.
- (iii) Until recently, most machines use 32 bits (4 bytes) as word size.
 - Limits addresses to 4GB (2^{32} bytes)
- (iv) Increasingly, machines have 64-bit word size:
 - Potentially, could have 18 PB (petabytes) of addressable memory
 - That's 18.4×10^{15}
- (v) Machines still support multiple data formats:
 - Fractions or multiples of word size.
 - Always integral number of bytes.

It's compiler and computer together who decide the word size in a certain program.

Word-Oriented Memory Organization.

- (i) Addresser Specify Byte Locations.
- (ii) Address of first byte in word.
- (iii) Addresses of successive words differ by 4 (32-bit) or 8 (64-bit).



Byte Ordering:

(I) So, how are the bytes within a multi-byte word ordered in memory?

(II) Conventions:

- (i) Big Endian: Sun, PPC Mac, Internet. Least significant byte has highest address.
- Least Endian: x86, ARM processors running Android, Least significant byte has lowest address

Byte Ordering Example:

(I) Example

- (ii) Variable x has 4-byte value of $0x01234567$
- (iii) Address given by $\&x$ is $0x100$

BigEndian:

$0x100\ 0x101\ 0x102\ 0x103$



LittleEndian:

$0x100\ 0x101\ 0x102\ 0x103$



Examining Data Representations.

Code to print Byte Representation of Data.

See -

casting.c

You can't directly copy a pointer from another -

Representing strings.

(I) strings in C.

- (i) Represented by array of characters
- (ii) Each character encoded in ASCII format.
- (iii) Std. 7-bit encoding of character set
- (iv) character "0" has code 0x30.
 - Digit i has code $0x30 + i$
- (v) string should be null-terminated.
- (vi) Final character = 0

(II) compatibility

- (i) Byte ordering not an issue.

T_{\min} FALSE

$$x < 0 \Rightarrow ((x \& 2) < 0)$$

$ux > 0$ TRUE

$$x \& 1 == 1 \Rightarrow (x < s_0) < 0.$$

(TRUE)

$ux > -1$ Always false

It will be cast into U_{\max}

$$x > y \Leftrightarrow -x < -y$$

If $T_{\min} = y$ Then...

$x * x >= 0$ FALSE.

$x > 0 \& y > 0 \Rightarrow x + y > 0$ FALSE

$x >= 0 \Rightarrow -x <= 0$ TRUE.

$x <= 0 \Rightarrow -x >= 0$ FALSE

$$\begin{aligned} |T_{\min}| - |T_{\max}| &\leq 1 \\ (|x| - |x|) &> 3 \leq -1 \\ \begin{cases} x = 0 & \text{FALSE} \\ \text{otherwise} & \text{TRUE.} \end{cases} \end{aligned}$$