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A dynamic current mode design approach of 2/3 prescaler for phase locked loop application

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Abstract
Though Current Mode Logic has excellent features like higher switching speed and reduced crosstalk due to small output swing, there exists numerous flaws such as static power dissipation, non-suitable for power-down modes and comparably higher design complexity of load resistors. To address the aforementioned worries, this article incorporates a dynamic current mode design approach having active load and controlled current source to configure an improved (2/3) dual modulus prescaler. Simulation results of the proposed circuit using Cadence Virtuoso platform for 90 nm CMOS at 1.2 V supply depict a power consumption of 2.517 mW when driven by a high frequency of 2 GHz. The phase noise and output noise are found to be − 147.001 dBc/Hz and − 181.7 dB at 1 MHz offset while it reads a self-oscillation frequency of 5 GHz. The variation tolerance of the design is proved via 5% skew-based simulation at all corners; whereas the correct functionality at 28 nm UMC justifies its scalability.

Keywords Current mode logic · Frequency divider · Prescaler · High speed

1 Introduction

Low power and high frequency operation play an important role in modern communication circuit, where frequency translation or prescaler device is broadly used in the design of phase-locked loops (PLLs) and clock and data recovery modules. There have been various techniques to design a prescaler circuit such as current mode logic (CML), dynamic logic divider, TSPC and ILFD, which operates at higher input frequency with wider range [1–3]. However, the design of divide-by-2/3 at higher input frequency is a tough task. To obtain the two distinct division ratios, a module with D-flip flop embedded with additional logic gates has been implemented only to find a reduced operating frequency and large power dissipation. Also, the fact of adding gated elements introduces some delay. To overcome such demerits we have, in this paper proposed a prescaler circuit with dynamic current mode D-Flip flop to sustain distinct divisions at higher frequency burning lowest possible power. This dynamic design eliminates static power dissipation and obtains better performance. The highlights of this article are:

(a) A dynamic design approach of 2/3 prescaler circuit for low power and higher frequency of operation.
(b) Higher sensitivity range of 2.4–10 GHz with a self-oscillation frequency of 5 GHz.
(c) Quick response time along with a reduced phase noise of − 147.0 dBc/Hz.
(d) A variation tolerant circuit as tested at five different corners to see the least variation between 'no skew' and '5% skew' condition.
(e) A scalable design as observed for lower technology nodes like 28 nm UMC.

This paper is further organized as below: Sect. 2 briefs the prior arts and it is summarized in Table 1. Section 3 consists of our proposed architecture, results and

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Table 1 Summary of a few recent works

References	Year	Design methodology	Merit	Demerit	Uses & applications
Stephan Henzler et al. [1]	2008	CMOS logic-based frequency dividers	Power efficient high speed	Maximum area consumption	Low-power IQ-transceivers
Zhiming et al. [2]	2010	TSPC CMOS technology	High operational frequency	Trade off exist between the power and speed	Frequency synthesizers
X.P. Yu [3]	2010	Multi-phase quasi-differential	Low power consumption	It occupies more areas	Low power applications such as Bluetooth. and Zigbee
S. Ramakrishnan et al. [5]	2008	Dynamic CML technique	Reduces in leakage current	It can only operates up to 250 MHz	4-bit carry look ahead adder, ripple adder
Chi-Sheng Lin [6]	2011	Programmable frequency divider	It operates in Full modulus range	Less operating frequency	Applicable in advanced processor
Andrea Ghilioni [7]	2013	Dynamic latches based frequency divider	Inductor-less mm-wave dividers which reduces the power	Less bandwidth is reported	mm Wave applications
Wenjian Jiang [8]	2016	Triple-modulus prescaler	Less number of transistors	Low operational speed	Divide-by-6/7/8 prescaler
Self-Calibration Techniques [9]	2017	Self-calibration techniques	Increased locking range and increase the speed	It occupies more areas	Millimetre wave radar transmission
Sheng-Lyang Jang [10]	2017	Injection-locked frequency divider	Work in wide range of frequency	It's only divide by four and it is more complex	Used in harmonic mixer & resonator
Gautam R. Gangasani [11]	2019	Multi-phase injection-locked	Automatic calibration	Increased in phase noise	Frequency synthesizer

discussion. Section 4 highlights the comparison of this work with literature. Validation of design in lower technology node is demonstrated in Sect. 5. Section 6 concludes the paper.

2 Background and prior arts

Figure 1a shows the block diagram of 2/3 dual-modulus prescaler circuit consisting of two D flip-flops and two NOR gates [4]. It is steered by Modulus Control (MC) input such that it divides frequency by 2 when MC = 1, otherwise it divides frequency by 3. The literature have witnessed many different efforts of designing prescaler circuits. To operate in higher frequency range, a technique was proposed in [1] using fundamental CMOS; but it consumes larger die area [2]. A multiphase quasi-differential technique was employed in [3] to attain a better trade-off exist between the power and speed. The work in [6] offered a programmable division of frequency operating in full modulus range with significantly low switching frequency. A triple modulus scalar was implemented to reduce the number of transistor count with low operational speed [8], which was addressed using a self-calibration technique as it helps to widen the locking range giving away larger area and it can be used in the application of mm wave radar transmission [9].A injection locked frequency divider was presented in [9] to operate in wide range of frequency; but it can only divide by 4 and was typically used in the application of mixer and resonator [10]. To mitigate this problem of divide factor, a multiphase injection locked architecture was configured with

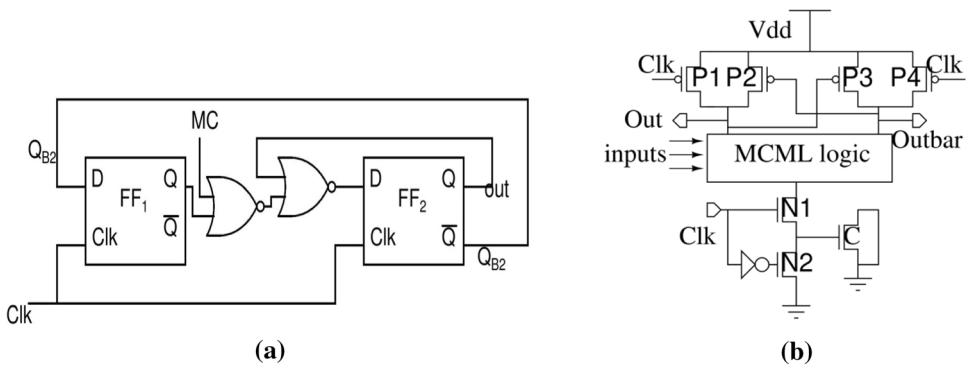

Fig. 1 **a** Basic 2/3 prescaler module **b** configuration of dynamic CML

automatic calibration technique having a penalty in higher phase noise and it was applicable in frequency synthesizer applications [11].

To eliminate the power dissipation issues and maintain the operating speed, dynamic current mode logic (DyCML) has come into existence and its schematic is drawn in Fig. 1b [12], which is made of an MCML based logic evaluation unit, a precharge module (P1, P4, N2), a current source with dynamic behavior (N1, C), and a latch module to hold logic after evaluation (P3, P2). When the clock is low (Logic 0), the output nodes get charged to V_{DD} through the pre-charge transistors being turned ON and the saturation of transistor N2 refers the capacitor to discharge to Gnd. As transistor N1 remains OFF, no dc path between power rails is allowed. When clock is high, the transistors N2, P1 and P4 move to cut-off state, whereas transistor N1 turns ON allowing current to flow from the pre-charged output nodes to the capacitor (C). Both the paths offer different impedances based on the inputs and logic function. Hence, either of the output nodes rolls down faster than the other node. The cross-connected transistors (P2 and P3) guide to hurry up the evaluation and maintain the logic levels.

In [5], a novel approach of improved Dynamic CML was discussed to attain a low power dissipation by turning the circuits into standby mode; but its operation was limited to 250 MHz as operating frequency. Another approach of dynamic latch-based frequency divider was highlighted in [7], which reduces power consumption, but works in less bandwidth. A few of the recent works are summarized in Table 1.

3 Proposed architecture and its simulation

Figure 2 displays the design of proposed dynamic MCML based dual-modulus 2/3 pre-scaler circuit to serve as frequency divider and Table 2 highlights the transistor sizes. Figure 3 refers to its physical layout in 90 nm CMOS. The dynamic configuration reduces the power burn and also helps to operate in better switching frequency. This architecture comprises of two Dynamic D flip flop and two dynamic NOR gates to reduce the load and fan-out of OUT_{BAR} of second D-FF in conventional design. The working principle (refer Fig. 1a) is discussed in two different following cases:

Case-1 When the control input MC = 1, it switches N17 and N18 transistor of NOR gate-1 to cut-off and saturation respectively to drive its output to a constant logic 0. This actually disconnects DFF-1 from operation and helps NOR gate-2 to work as an inverter. As a consequence, the output of DFF-2 gets inverted and is fed to input of DFF-1. Hence, the circuit appears to be a T Flip flop and works as divided by 2.

Case-2 When a low logic level hits the Modulus control input (MC = 0), N18 transistor switches to cut-off and N17 moves to saturation only to make the NOR gate-1 to behave as an inverter. This makes the output of first DFF to get inverted before hitting the NOR gate-2, which is waiting with the output of DFF-2 at the second input. This critical delay of signal through two NOR gates help the circuit to act as a divide-by-3 unit.

3.1 Transient analysis

The simulation is carried out with a maximum input frequency (f_{in}) of 10 GHz having V_{DD} = 1.2 V and the obtained output frequencies are 5 GHz and 3.33 GHz respectively in dual mode of operation. But, here Fig. 4a and b refer to the transient analysis of the circuit with f_{in} = 2 GHz to showcase divide-by-2 and divide-by-3 mode respectively.

3.2 Power and noise analysis

The Table 3 represents the study of power and noise metrics at all the extreme process corners with 'no skew' and '5% skew' to check the variation tolerance of our proposed circuit. The power dissipation, Phase noise (PN) and output noise (ON) in no-skew condition are found to differ from 5% process skew condition by 3.98%, 0.06% and 0.22% respectively in Nominal–Nominal Corner during the divide by 2 operation mode.

A Monte Carlo simulation of our proposed circuit is performed with 500 statistical run to check its variation following 3σ process. The histogram plot of power consumption, PN and ON are depicted in Fig. 5a, b and c respectively. It is noted that the minimum-to-maximum values of these parameters are 2.392 to 2.579 mW, − 149.664 to − 147.597 dBc/Hz and − 186.87 to − 177.49 dB respectively. The plot of PN and ON due to varying frequency is shown in Fig. 6a and b respectively for both pre layout and post layout study.

3.3 Frequency sensitivity analysis

The behaviour of a clock divider is correctly studied by its frequency sensitivity plot, where the input power in (dBm) is plotted as a function of given input frequency for the divider to lock. Figure 7a displays the sensitivity plot of proposed dual modulus (2/3) prescalar circuit and it has a very wide frequency band ranging from 2.4 to 8 GHz with a self-oscillation frequency of 5 GHz, which is suitable to be used in the application of frequency synthesizer. The

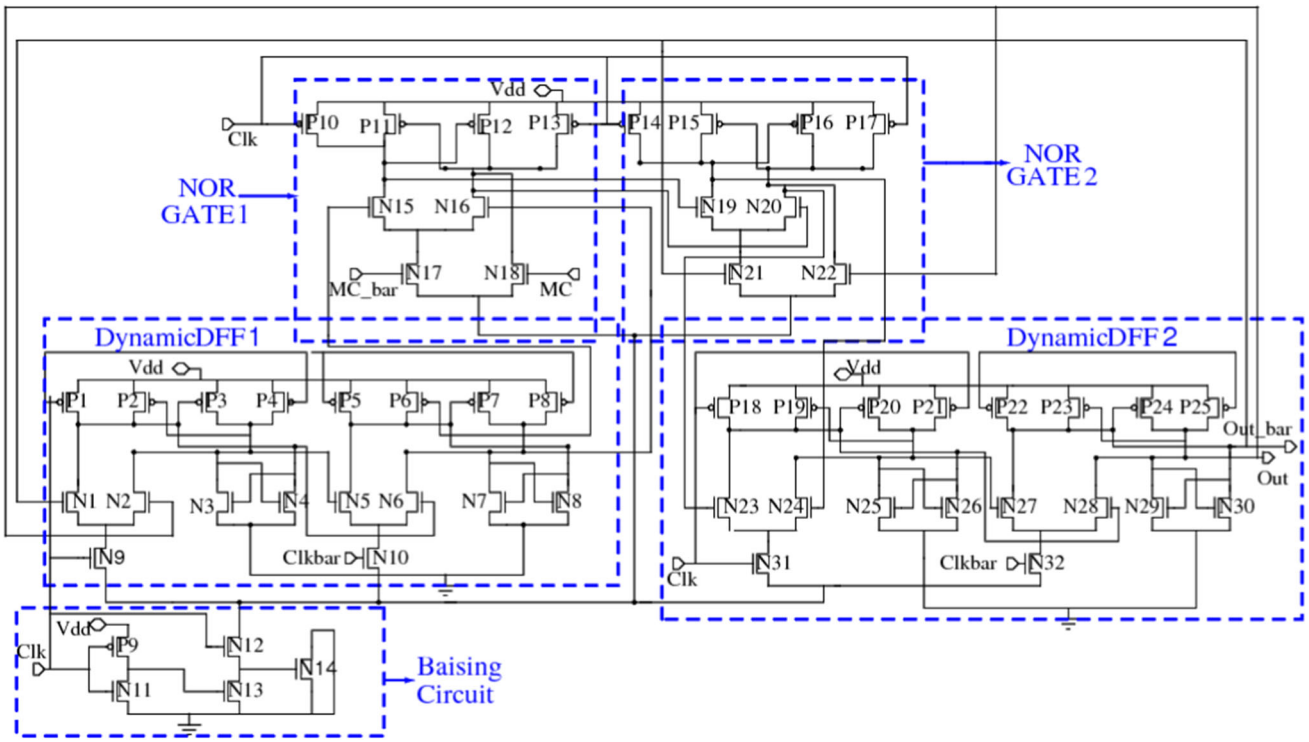

Fig. 2 Proposed Prescaler module Schematic @ 90 nm CMOS

Table 2 Sizes of transistor used

Biasing circuit					
Transistor No.	Width (um)	Length (um)	Transistor No.	Width (um)	Length (um)
P9, N11	0.12	0.1	N12-N14	0.4	0.1
DFF1					
P1-P7	1.4	0.1	N1-N7	3.0	0.1
N9	4.5	0.1	N10	4.5	0.1
NOR Gate 1					
P10-P13	1.4	0.1	N15-18	3.0	0.1
NOR Gate 2					
P14-P17	1.4	0.1	N19-N22	3.0	0.1
DFF2					
P18-P25	1.4	0.1	N23-N30	3.0	0.1
N31	4.5	0.1	N32	4.5	0.1

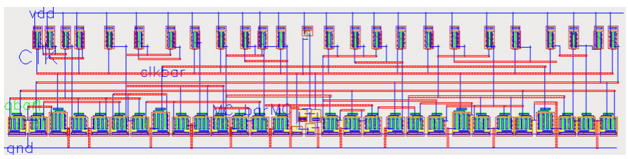

Fig. 3 Prescaler Layout @ 90 nm (59.633 μm × 13.225 μm)

said behaviour is studied at different V_{DD} as shown in Fig. 7b and it is observed that the self-oscillation frequency significantly increases with the rise in supply voltage.

3.4 Study of average power and maximum operating frequency

The average power of the circuit is studied by varying the input frequency and from Fig. 8a it's clear that power rises linearly with input frequency and a variation of 2.3 mW to 4.2 mW is noted with frequency ranges from 1 to 10 GHz. Figure 8b denotes the maximum operating frequency of the circuit at different supply voltages.

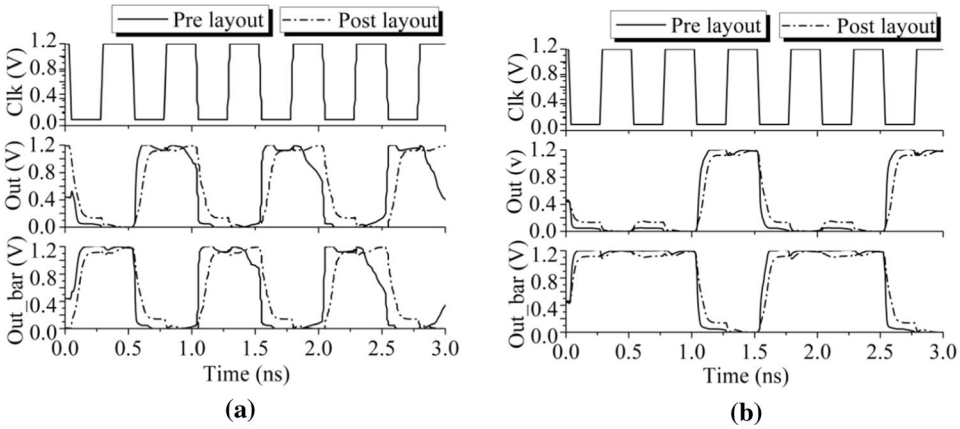

Fig. 4 Transient of the proposed design **a** Divide by 2 **b** Divide by 3

Table 3 Metrics at different Process Corners @ f_{in} = 2 GHz

Process corner	No Skew			5% processSkew					
	Average power (mW)	Phase noise (dBc/Hz)	Output noise (dB)	Average power (mW)		Phase noise (dBc/Hz)		Output noise (dB)	
				Mean	Standard deviation	Mean	Standard deviation	Mean	Standard deviation
TT	2.51	− 147.0	− 181.7	2.41	0.794	− 146.9	0.286	− 182.1	0.011
FF	2.98	− 148.9	− 181.7	2.84	0.981	− 148.9	0.276	− 182.2	0.098
FS	2.02	− 144.7	− 181.8	1.89	0.673	− 144.6	0.323	− 183.2	0.015
SF	2.97	− 148.1	− 181.6	2.89	0.996	− 148.0	0.260	− 177.4	0.005
SS	2.00	− 144.2	− 181.5	1.87	0.653	− 144.1	0.296	− 181.8	0.008

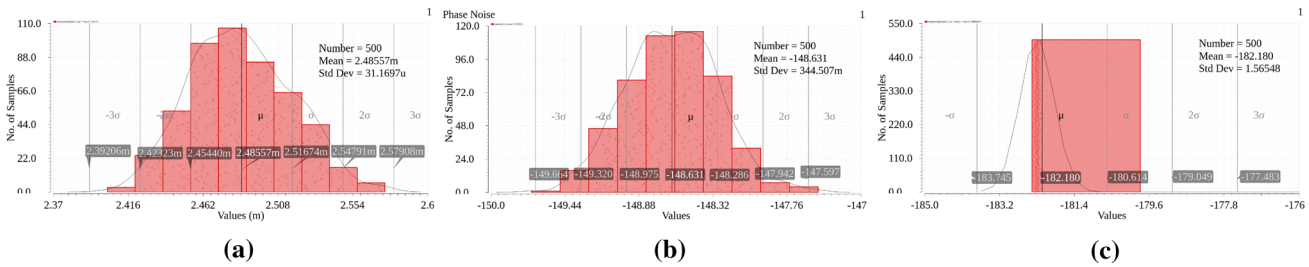

Fig. 5 Histogram plot of **a** average power **b** phase noise **c** output noise when MC = 1

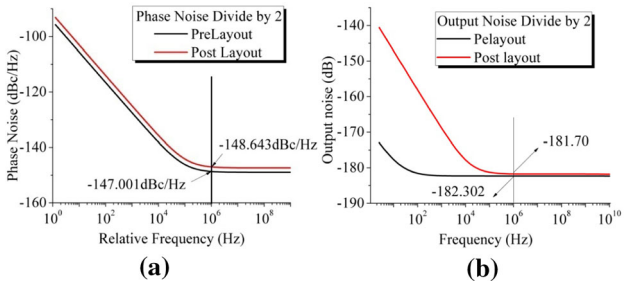

Fig. 6 During MC = 1 **a** phase noise **b** output noise

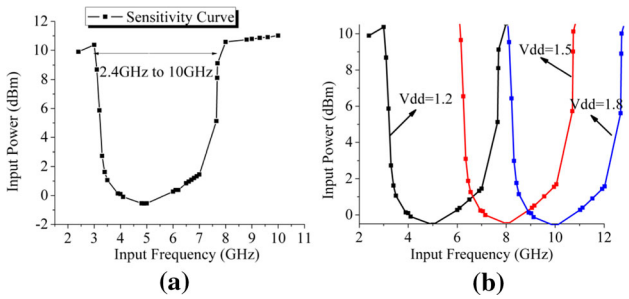

Fig. 7 **a** Input sensitivity plot **b** sensitivity plot versus V_{DD}

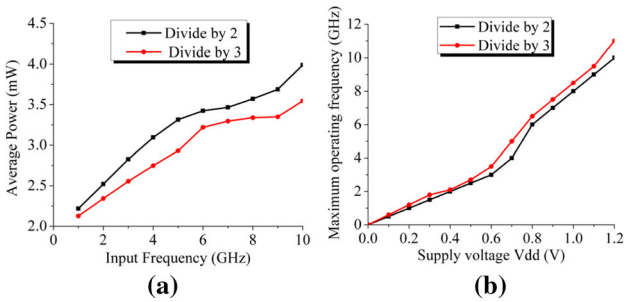

Fig. 8 **a** Average power versus input frequency **b** maximum operating frequency versus supply voltage

Table 5 Validation at 28 nm UMC @ f_{in} = 4 GHz

Parameters	Value
Technology	28 nm
Average power	2.8578 mW
Supply voltage	1 V
Phase noise offset @1 MHz	− 152.437
Output noise offset @1 MHz	− 183.208
Division factor	2/3
Operating frequency range	1.5–8.5 GHz
Self-oscillation frequency	4 GHz

4 Comparison analysis

Table 4 demonstrates the comparison of proposed work with the other well-known recent works in which it is clearly noticed that this work has least power consumption even after working at as high as 10 GHz of switching frequency. Phase noise is found to be better than the others; whereas the die area occupancy and self-oscillation frequency are moderate.

5 Validation at 28 nm technology

The scale down of technology offers many different adverse effects in an IC design for which it is always imperative to test the functionality of any newly built logic in lower CMOS nodes. In this paper, we have designed and tested the proposed prescaler for 28 nmUMC technology at a supply voltage of 1 V. The circuit is found well functional and observed performance metrics are expressed in Table 5. As the technology and supply voltage both got scaled down the obtained power dissipation reduces immensely as evident by comparing with Fig. 8a. Also, both phase noise and output noise are noted to curb down in lower process nodes thereby justifying the worth of the design.

6 Conclusion

A variation aware dynamic current mode configuration of 2/3 prescaler circuit is unveiled in this article by embedding two dynamic D-FF and two dynamic NOR module. The circuit arrangement cuts down the short circuit power dissipation, which allows it to express comparably lower power dissipation even when operated at as high as 10 GHz input. The design is validated at lower process nodes with better performance in metrics like power dissipation, phase noise and output noise by maintaining the frequency band of operation. This 2/3 division ratio can be used further extended to divide any integral number of N/N + 1 with a

Table 4 Comparison with prior arts

Parameters	[13]	[14]	[15]	[16]	[17]	[18]	[19]	This work
Technology (nm)	90	130	90	180	250	180	90	90
Supply (V)	1.2	1.3	1.2	1.8	2.5	1.8	2	1.2
Locking range (GHz)	9.2	4.6	7.1	3	1.75	0.99	4.6	2 (Max 10)
Phase noise @ 1 MHz (dBc/Hz)	− 140	− 72	− 132	− 93.5	− 81	− 85.2	− 90	− 147.0
Power (mW)	17.8	57	28.8	112	287.5	35.7	12.9	2.51
Division factor	Divide by 4 and 8	Divide by 2	Divide by 6	2/3	Multimodulus divider	Divide by 32	Divide by 2 and 5	2/3
Technique used	Regenerative Freq. Divider	LC-ILFD	ILFD	Distributed switches	BiCMOS	ILFM	Current reuse	Dynamic Logic
Self-oscillation frequency (GHz)	8	20	7.1	–	0.125	0.35	5	5.0
Required area (mm^2)	0.72	0.87	0.6984	1.628	0.560	0.8064	0.4992	1.160

high speed operation thereby making it eligible in frequency synthesizer and phase locked loop application.

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Data availability The authors confirm that all data are included within the manuscript.

Declarations

Conflict of interest The authors declare that there is no conflict of interest regarding the publication of this work.

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