**EXPERIMENT1 ( 18CS30009 & 18CS10048 )**

**PART 1**

**Aim**: To efficiently implement a logic circuit using only 2 input NAND and NOR gates represented by a random binary tree with the properties:

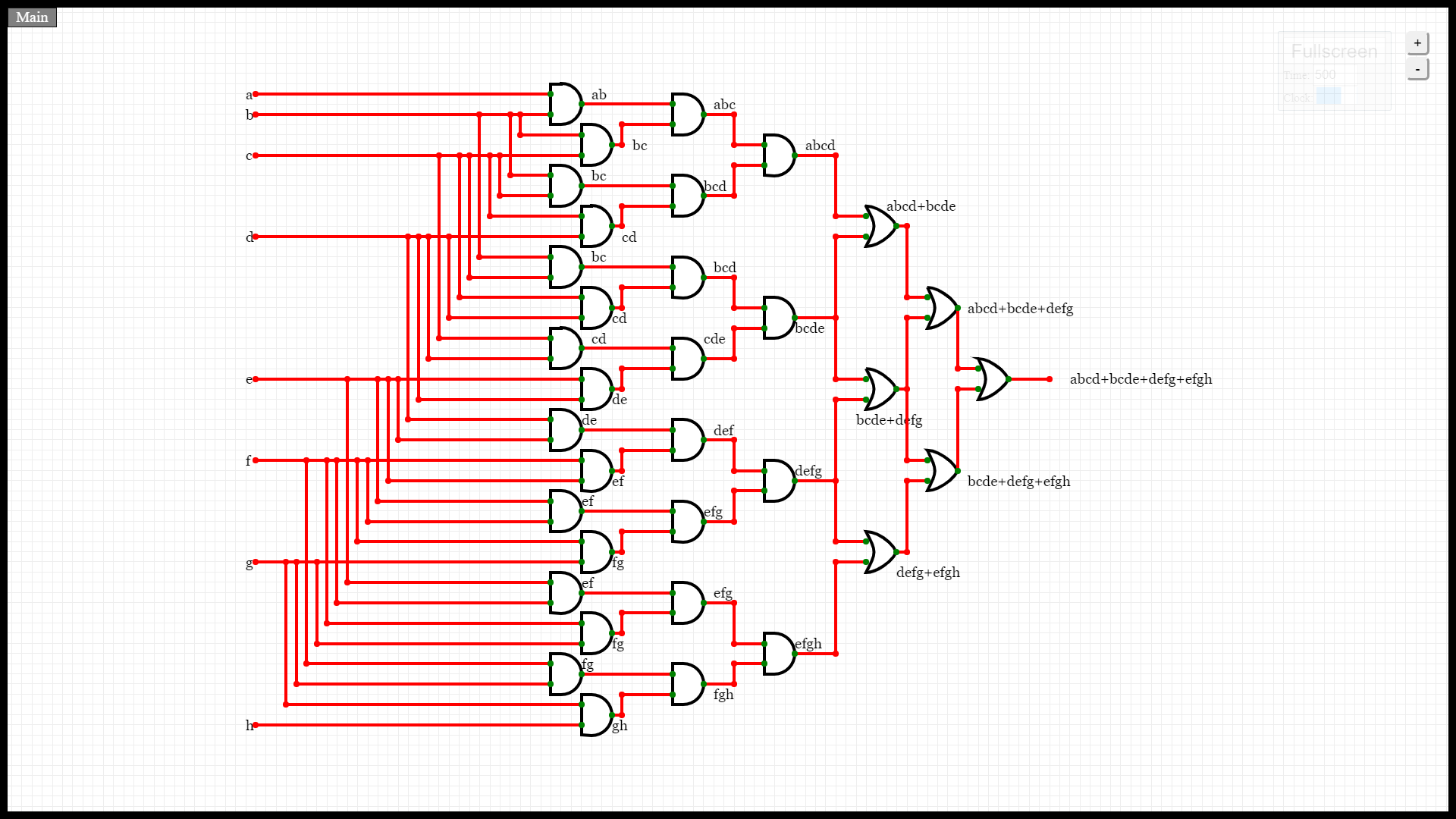
(i) The upper blue tree will have at least 6 internal nodes in which each node is the OR of the children nodes

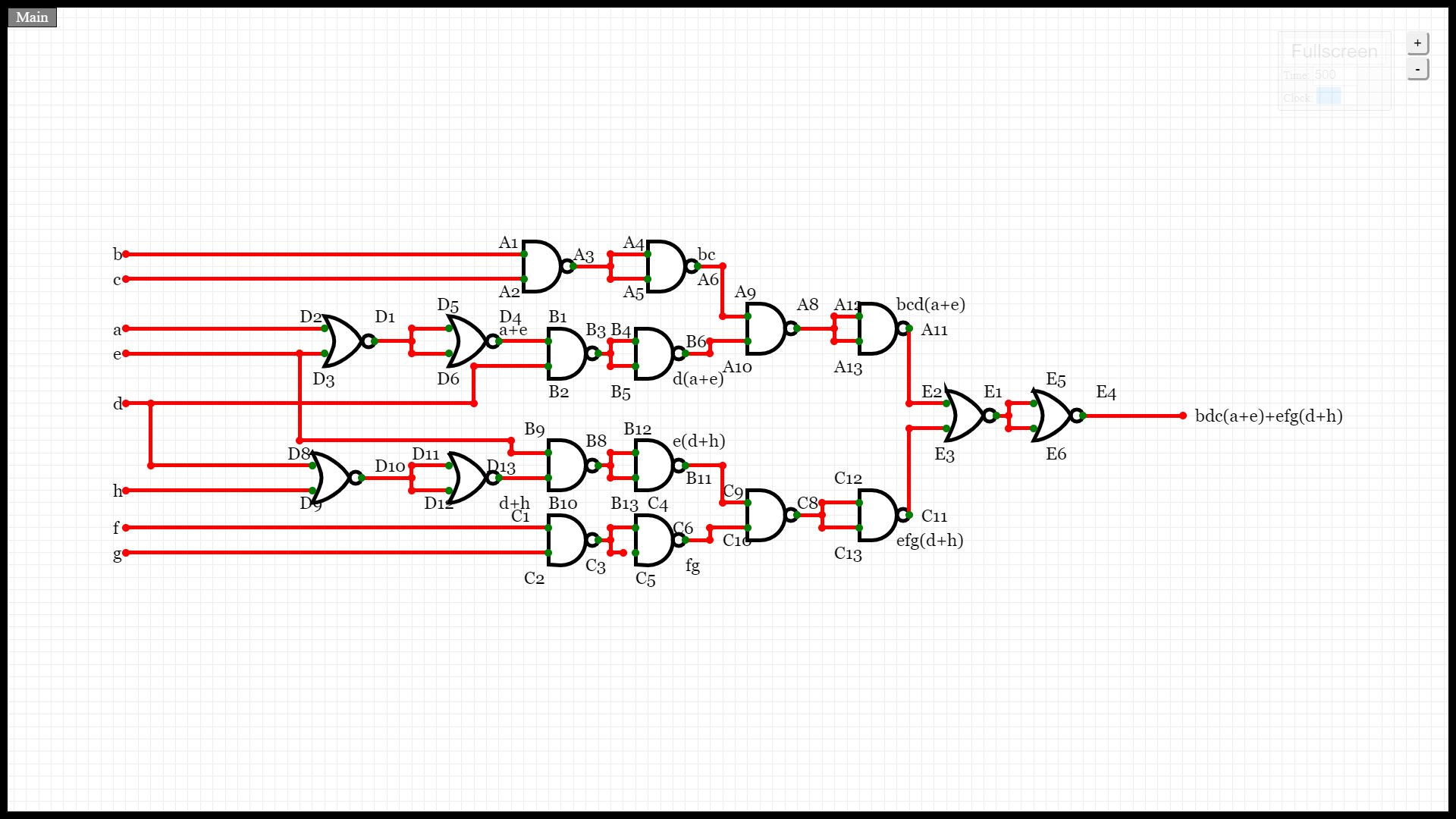
(ii) The lower tree will have at least 24 internal nodes in which each node is the AND of the children nodes.

**Apparatus Required**: (i)IC 74LS00(x3), (ii)IC 74LS02(x2)

**Theory:** The random tree which we used is shown in the figure with the AND gate as the red node and the OR gate as the blue node as specified in the problem statement. The final SOP form of the output is **abcd+bcde+defg+efgh** as can be seen from the tree. The SOP form can be written as **bcd(a+e)+efg(d+h)** which is then implemented using NAND and NOR gates.

**Tree:**



**Circuit Diagram:** 

**Result:** The efficient implementation of the circuit required 12 NAND gates and 6 NOR gates. Thus we required 3 IC 74LS00 and 2 IC 74LS02. The circuit cannot be optimized further.

**Discussion:** The AND and OR gates have been implemented from the NAND and NOR gates as shown.

