**EXPERIMENT1 ( 18CS30009 & 18CS10048 )**

**PART 2**

**Aim**: To construct a 3-bit to 8-bit encoder as indicated in the table below using only NAND and NOR gates.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUT | | |  | OUTPUT | | | | | | |
| x | y | z |  | a | b | c | d | e | f | g |
| 0 | 0 | 0 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 |  | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 |  | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 |  | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 |  | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 |  | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Apparatus Required**: (i) IC 74LS00(x2), (ii) IC 74LS02(x2)

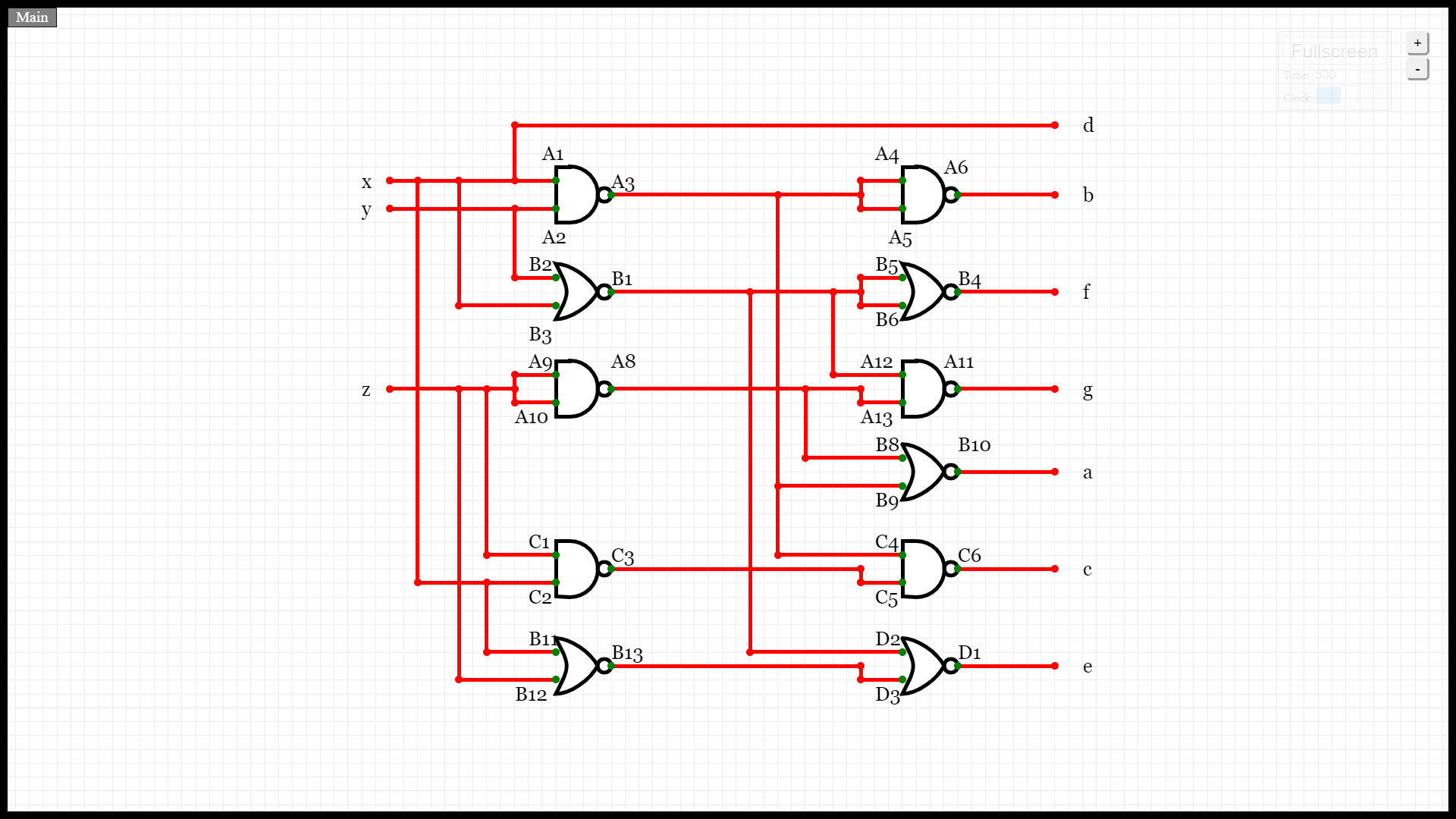
**Theory**: The encoded bits can be formulated in SOP form as follows:

a = **x\*y\*z** b = x\*y + x\*y\*z = **x\*y** c = x\*y + x\*z + x\*y\*z = **x\*y + x\*z** d = **x** e = y\*z + x + x\*z + x\*y + x\*y\*z = **x + y\*z** f = y + y\*z + x + x\*z + x\*y + x\*y\*z = **x+y** g = z + y + x + y\*z + x\*z + x\*y + x\*y\*z = **x+y+z**

If the implementation is done naively then it will require 16 or more logic gates. But we reduced it to 11 gates by efficiently constructing the circuit as shown in the circuit diagram.

**Circuit Diagram:**

**A,C : 74LS00 B,D : 74LS02**



**Result:** The efficient implementation of the circuit required 6 NAND gates and 5 NOR gates. Thus we required 2 IC 74LS00 and 2 IC 74LS02.

**Discussion:**

NAND and NOR are called universal gates because using them we can implement any of the 4 basic logic gates.

(i) Implementation of the 3 basic gates using NAND gate

(a) NOT: x’ = (1\*x)’

(b) AND: x\*y = (1\*(x\*y)’)’

(c) OR: x+y = ( ( (1\*x)’ ) \* ( (1\*y)’ ) )’

(ii) Implementation of the 3 basic gates using NOR gate

(a) NOT: x’ = (0+x)’

(b) AND: x\*y = ( (0+x)’ + (0+y)’ )’

(c) OR: x+y = (0+(x+y)’)’

Efficient construction of logic circuits is necessary for reducing the space occupied, the power loss and the complexity of the circuit. Each IC was fabricated with 3 such gates which further helped in reducing the space.