EE101

Tutorial 1 and Tutorial 2 (16-AUG-2013 and 20-AUG-2013) Solutions

1. This problem has been done in class assuming ideal diodes. Here, we want you to redo the calculations when the diode is not ideal, i.e. has a forward voltage drop of 0.7 volts.

For **$0 \le V_i \le 2.7$ V** BOTH D1 and D2 are OFF as they are reverse biased **$V_O = V_i$**

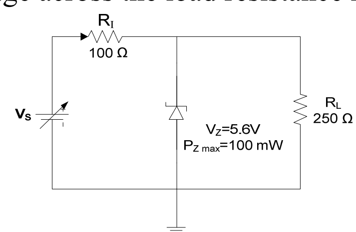
For **$V_i > 2.7$ V** D2 is OFF but D1 turns ON $i_{R1} = \frac{V_i - (2+0.7)}{R1 + R2} = \frac{V_i - 2.7}{20}$ mA

$$V_O = i_{R1} R_2 + 2.7 = \left(\frac{V_i - 2.7}{20}\right) 10 + 2.7 \qquad \mathbf{V_O = 0.5 V_i + 1.35}$$

For **$-4.7 \le V_i \le 0$ V** BOTH D1 and D2 are OFF as they are reverse biased **$V_O = V_i$**

For **$V_i < -4.7$ V** D2 is ON but D1 stays OFF **$V_O = -4.7$ V**

2. (a) For the circuit shown below, what is the maximum value of the source voltage V_S for which the voltage across the load resistance R_L can be maintained at 5.6V?



Since $P_Z = V_Z I_Z$ where I_Z is the current through the zener diode, we have $I_{Z, MAX} = 100/5.6 = 17.86$ mA

Since $I_{RL} = 5.6/0.250 = 22.4$ mA, we have $I_{RI\,MAX} = I_{Z\,MAX} + I_{RL} = 17.86 + 22.4 = 40.26$ mA

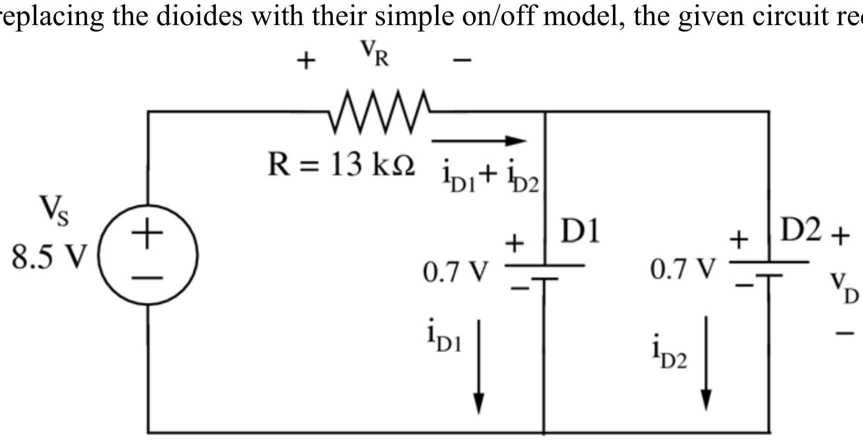
Therefore, $\mathbf{V_{S\,MAX} = I_{RI\,MAX} R_I + V_Z = 40.26*0.1 + 5.6 = 9.63\ V}$

(b) If the Zener diode is such that a minimum current of 1 mA is required for the Zener action to take place, what is the minimum source voltage V_S that can be used?

When the zener diode is drawing minimum current, we have $I_{RI\,MIN} = 1 + I_{RL} = 23.4$ mA

Therefore, $\mathbf{V_{S\,MIN} = I_{RI\,MIN} R_I + V_Z = 23.4*0.1 + 5.6 = 7.94\ V}$

3. On replacing the dioides with their simple on/off model, the given circuit reduces to as below:



Now, as the diodes are in parallel, the volatage across each of the diode would be

$$v_D = 0.7\ V$$

The voltage drop across the resistor (R) be

$$v_R = V_S - v_D = 8.5 - 0.7 = 7.8\ V$$

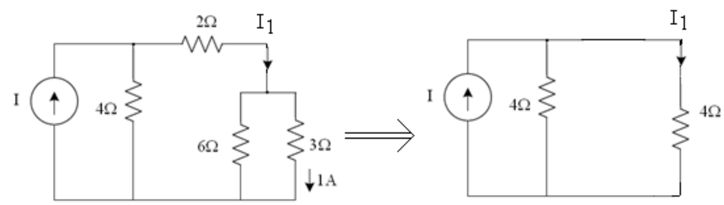
The total diode current (= resistor current) be

$$i_{D1} + i_{D2} = i_R = v_R / R = 7.8/13\text{k}\Omega = 0.6\text{ mA}$$

Note that in the simple on/off model, the forward resistance of diode is assume to be zero so we cannot find the individual diode current for diodes connected in parallel.

4. Considering the division of current, $1 = \frac{6}{6+3} I_1 \qquad \therefore I_1 = \frac{3}{2}\text{A}$

Further, the circuit can be simplified as,

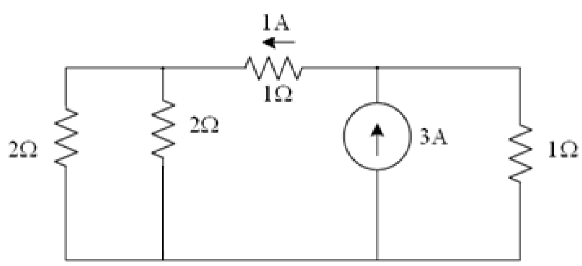


Therefore, $I = 2I_1 = 3\text{ A}$

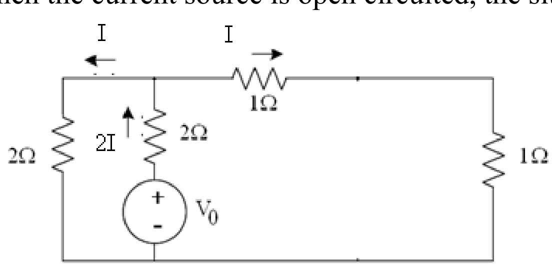
Power dissipated in 4 ohm register, P = ((I/2)^2)*4 = 9 watt

5. We apply superposition.

When the voltage source is short circuited, a current of 1 A as shown flows $\left(3 \times \frac{1}{(2 \| 2+1)+1} = 1\text{ A}\right)$.



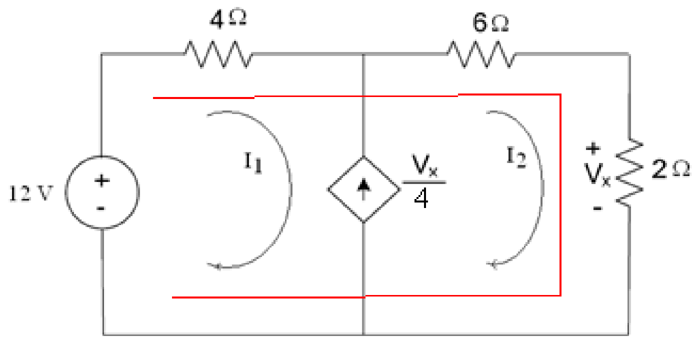
When the current source is open circuited, the situation is shown in the figure below



When both the sources are present, if the net current in the 1 Ohm resistance is to be 1 A as stated in the problem, I has to be 2 A.

Therefore, applying KVL in the figure above, $V_0 = 2\text{x}4+2\text{x}2=12$ V

6. Since we have common current source between the meshes, we apply the concept of super-mesh as shown



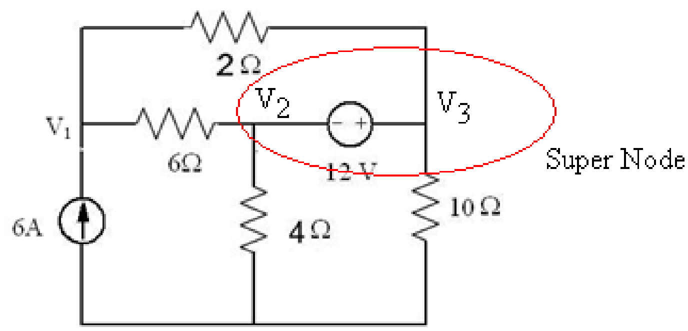
Applying KVL, $12\text{-}4I_1\text{-}6I_2\text{-}V_x = 0$

We also have $V_x = 2I_2$ and $I_2\text{-}I_1 = \frac{V_x}{4}$

Reducing further, $12 = 4I_1 + 8I_2$ and $2I_2\text{-}4I_1 = 0$

Solving the above equations, $I_1 = \frac{3}{5}$ A and $I_2 = \frac{6}{5}$ A

7. Since the voltage source appear between two nodes, we form a super node



The equations are as follows:

$V_2 - V_3 = -12$

At the node 1 (where node voltage is V_1),

$$\frac{V_1 - V_2}{6} + \frac{V_1 - V_3}{2} = 6$$

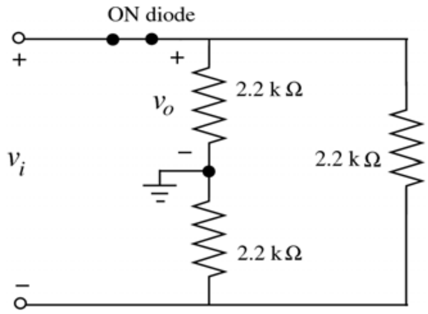
At super node

$$\frac{V_2 - V_1}{6} + \frac{V_2}{4} + \frac{V_3}{10} + \frac{V_3 - V_1}{2} = 0$$

Eliminating V_3 we get,

$4V_1 - 4V_2 = 72$ and $40V_1 - 61V_2 = 432$. Solving for V_1, we get $V_1 = 666/21 = 31.714$ V

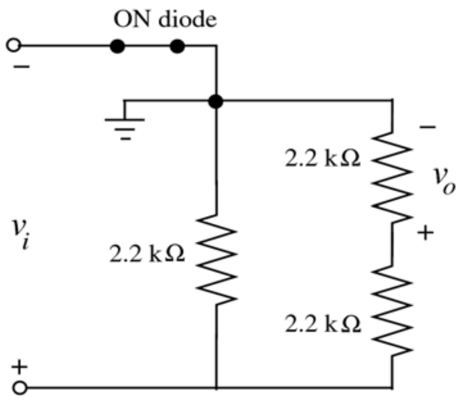
8. For positive half-cycle of v_i, the given circuit could be redrawn as



On applying the voltage devider rule, we have

$$v_{o_{max}} = \frac{2.2k\Omega \times v_{i_{max}}}{2.2k\Omega + 2.2k\Omega} = \frac{v_{i_{max}}}{2}$$
$$= \frac{100}{2} = 50V$$

For negative half-cycle of v_i, the given circuit could be redrawn as



Again applying the voltage divider rule, we have

$$v_{o_{max}} = \frac{2.2k\Omega \times v_{i_{max}}}{2.2k\Omega + 2.2k\Omega} = 50V$$

Note the polarity of v_o across 2.2 kΩ resistor acting as load is the same for both the positive and negative cycles of the input waveform.

Thus the output voltage v_o be a full-wave rectified ersion of the input waveform but with peak value V_m of 50 V.

For the full-wave rectified waveform, the dc voltage $V_{dc} = 0.636\ V_m = 0.636(50) = 31.8V$