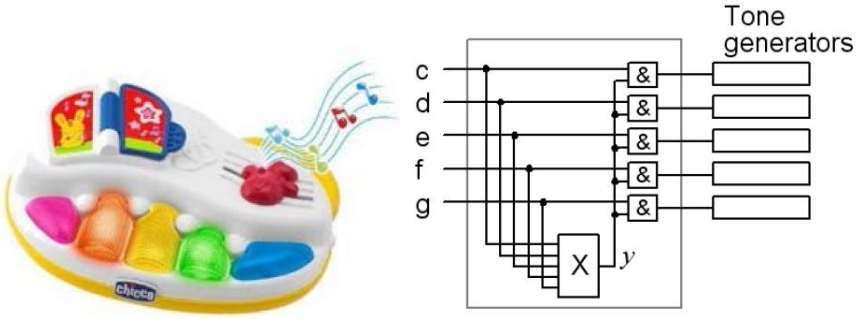
Session: 2017-18 **EE101: Electrical Sciences** **Max. Marks: 10**

Long Assignment-1

(Due Date: 15/09/17)

Q1. The toy piano for young children can be very disturbing as it produces a highly inharmonious sound when multiple keys are pressed simultaneously. You must therefore construct a "dissonance-lock" representing the block X in the figure below. The lock X should allow sounding on individual keys, but if multiple keys are pressed simultaneously, then only nice sounding cords (i.e., combinations of keys c, e and g) should sound and the rest should be quite. Thus sound should be produced only if (1) exactly one of the keys c, d, e, f, g is pressed, (2) any possible combination of keys c, e, g is pressed. All other combinations produce no sound.



Note: The blocks with symbol '&' in the given circuit denote the AND gates.

a) Set up the truth table for $y = f(\text{c, d, e, f, g})$ or draw Karnaugh map directly. Can you find a case where the value of y does not matter? If so then use that as a don't care. **[1]**

b) Using don't cares, obtain the minimized SOP expression for y. **[1]**

c) Realize the minimized expression for y using 4-input NOR gates only. **[1]**

Q2. A 2-bit counter can be designed either to count "up" (i.e., producing count sequence 00, 01, 10, 11, 00, …) or to count "down" (i.e., producing count sequence as 11, 10, 01, 00, 11 …). Consider a 2-bit counter being realized using three flip-flops such that apart from the common clock input it has two additional inputs "up" and "down". Out of three flip-flops one stores whether or not the counter should currently be counting up or down, i.e., the "up" input makes the clock start counting up and the "down" input makes the clock counting down. (The "up" or "down" input will be held at 1 for at least a clock cycle, and it does not matter what happens *while* it's being held at 1.)

Draw the logic diagram of the above described "up-down" counter. **[2]**

(**Hint:** By XORing with 1, the output of a flip-flop can be inverted.)

Q3. In the circuit shown in Fig.1, $\mathbf{i_C = 20e^{j(40t+30°)}\ A}$. Express $\mathbf{V_S}$ as a complex forcing function. **[2.5]**

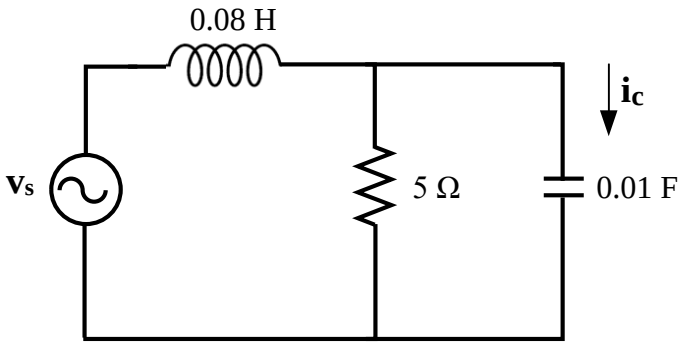


Fig.1

Q4. Find $\mathbf{V_x}$ in the circuit shown in Fig.2. **[2.5]**

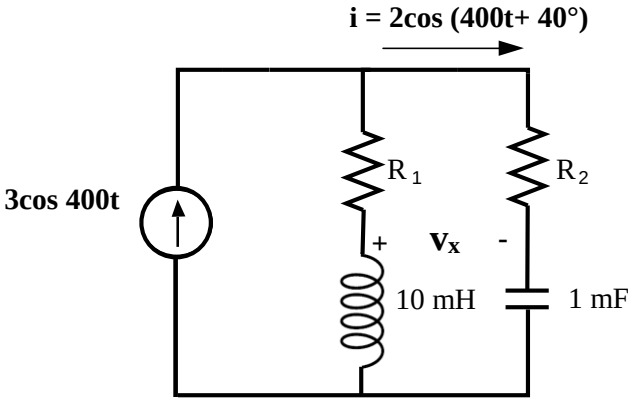


Fig.2