Department of Electronics and Electrical Engineering
Indian Institute of Technology Guwahati

End-Semester Examination **EE101: Electrical Sciences**

Date: 19.11.2012 **Time: 1:00PM – 4:00PM** **Maximum Marks: 50**

Important Instructions:

1. This exam consists of six questions on two pages and all questions have to be answered.
2. Start a new Question on a fresh page and answer all parts of a question together.
3. Credit for each question is shown in square bracket.
4. Index all pages (excluding the cover page and overleaf instruction page) with page numbers 1, 2, 3,..etc. and continue this numbering order across all the Supplementary Sheets.

1. The **BCD** number $B_3\ B_2\ B_1\ B_0$ is given as input to a logic circuit to generate an output **Y** which is **1** only when the bits add up to a number greater than or equal to **TWO**; otherwise, the output is **0**.

(a) Give the Truth Table for **Y** in terms of $B_3\ B_2\ B_1\ B_0$ **[1]**
(b) Write the Standard Sum-of-Product (SSOP) expression for **Y** **[1]**
(c) Draw the Karnaugh Map for **Y** **[1]**
(d) Use the Karnaugh Map to obtain a simpler expression for **Y** **[2]**
(e) Give a circuit **using only NAND gates** to realize this function. **[2]**
Assume that NAND gates with two, four or six inputs are available for use for (e).
(f) Give a circuit using only **2-input NAND gates** to realize this function. **[2]**
Note: For **(e)** and **(f)**, assume that inverted values of the bits are also available, if needed.

2. Design a 3-bit counter (i.e. $Q_2\ Q_1\ Q_0$) counting in the **Gray Code** sequence 000, 001, 011, 010, 110, 111, 101, 100, 000.. using negative edge-triggered D flip-flops. The counter is allowed to start in a random state when power is first applied but thereafter must count in the Gray Code sequence for every negative edge of the applied clock signal.

(a) Give the truth tables for the input of each flip-flop, i.e. D_2, D_1, D_0. **[3x1]**
(b) Using Karnaugh Maps, derive the logic expressions for the input of each flip-flop **[3x1.5]**
(c) Using **only NAND gates**, give the three circuits that will generate the required inputs to be given to each of the three D flip-flops. Assume that the D flip-flops used provide both Q and $\overline{Q}$ outputs that you can directly use in your circuits. **[3x0.5]**

3. The circuit shown in Figure1 has R_1=10 KΩ, R_2=2 KΩ, R_3=100 KΩ and R_{gain}=20 KΩ. Find the voltages at the points **A, B, C, D, E and F** and the output voltage V_{out} in terms of the input voltages V_1 and V_2. **[7]**

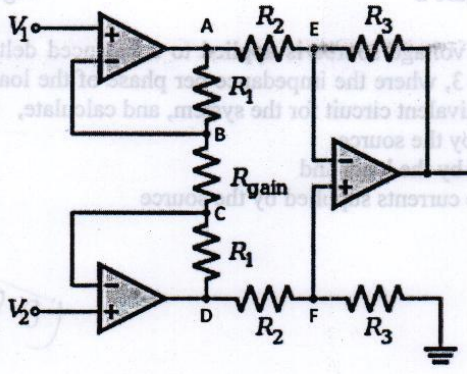

Figure 1

4. A 440 V, 50 Hz, Y connected, 3-phase induction motor has negligible stator impedance and a rotor impedance of (0.9+*j*02.7) Ω/phase at standstill referred to the stator. The motor runs at 960 rpm at full load.

(i) How many poles does the machine have? **[1]**
(ii) Determine the synchronous speed and find the percent slip at full load. **[1]**
(iii) Determine the effective rotor resistance and emulated load resistance at full load condition. **[1]**
(iv) Draw the equivalent circuit and calculate the air-gap power at full load, and **[3]**
(v) Determine the developed torque at full load. **[2]**

5. (a) The resistances and leakage reactances of a 25 kVA, 50 Hz, 2400/240 V transformer are:

$R_1 = 0.65\ \Omega$, $R_2 = 0.0065\ \Omega$,
$X_1 = 7.0\ \Omega$, $X_2 = 0.07\ \Omega$,

where subscript 1 denotes the 2400-V winding and subscript 2 denotes the 240-V winding.

(i) Ignoring the shunt components, draw the equivalent circuit of the transformer referred to the high voltage side and label the parameters in numerical values. **[1.5]**
(ii) When the transformer delivers its rated kVA at 0.8 pf lagging to a load on the low voltage side with 240 V across the load, find the input voltage at the high voltage terminals. **[2]**
(iii) If the power factor of the load in part (ii) above were 0.8 leading, what would be the input voltage? **[1.5]**

(b) A coil of 150 turns is wound on an iron ring of square cross-section and carries a current of 2 A. The inner radius of the ring is 10 cm and the outer radius is 12 cm. The relative permeability of the iron ring is 1500. Assuming no saturation in the core, determine (a) the reluctance of the ring, (b) the flux density in the ring, and (c) the inductance of the coil. **[1.5+1+1.5]**

6. (a) Use mesh analysis to the circuit shown in Figure 2 to find the node voltages v_1, v_2, and v_3. **[4]**

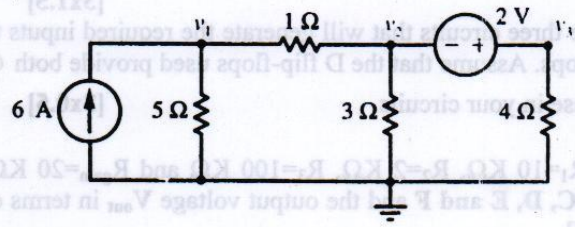

Figure 2

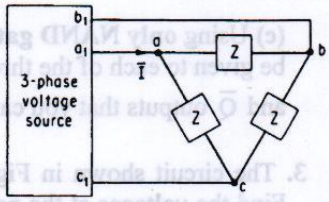

Figure 3

(b) A balanced 220 V, 3-phase voltage source is applied to a balanced delta connected 3-phase load as shown in Figure 3, where the impedance per phase of the load is Z= 10+*j*20 Ω. Draw the one star phase equivalent circuit for the system, and calculate,

(i) the line current supplied by the source, **[2]**
(ii) the total power absorbed by the load, and **[1]**
(iii) the sum of the three line currents supplied by the source **[1]**