Department of Electronics and Electrical Engineering

Indian Institute of Technology Guwahati

Lab Manual

EE 102

Session: 2017-2018/ II semester

http://172.16.28.65/ee102/

Expt. No.	Title of Experiments
E1	**FAMILIARIZATION WITH THE LABORATORY EQUIPMENTS**
E2	**Circuit Theorems** OBJECTIVE: Verification of superposition theorem, Thevenin's theorem and maximum power transfer theorem
E3	**RLC Circuits** OBJECTIVE: To find the step response of RC and RL circuits and RLC series circuit resonance
E4	**DIODE CIRCUITS** OBJECTIVES: Design and analysis of half wave rectifier and clipping circuits
E5	**POWER SUPPLY** OBJECTIVES: Design and analysis of full-wave rectifier and zener regulator
E6	**Study of Common-emitter Amplifier** OBJECTIVES: 1. To carry out an approximate DC and AC-analysis of the given CE amplifier. 2. To determine the voltage gain, the "maximum undistorted peak-to-peak output voltage swing" (MUOVS) and the maximum input voltage for undistorted output. 3. To study the effect of emitter bypass capacitor on voltage gain.
E7	**OPERATIONAL AMPLIFIER** OBJECTIVE: Realization of amplifier circuits with Op-Amp
E8	**VOLTAGE TO FREQUENCY CONVERTER** OBJECTIVE: Designing a voltage to frequency converter

Day	**Monday**		**Tuesday**		**Wednesday**		**Thursday**		**Friday**	
Session	**FNS**	**ANS**	**FNS**	**ANS**	**FNS**	**ANS**	**FNS**	**ANS**	**FNS**	**ANS**
Lab Hours	**0900-1200**	**1400-1700**	**0900-1200**	**1400-1700**	**0900-1200**	**1400-1700**	**0900-1200**	**1400-1700**	**0900-1200**	**1400-1700**
Expt. No./Lab Group	**L2**	**L7**	**L5**	**L10**	**L3**	**L8**	**L1**	**L6**	**L4**	**L9**
E1	29 Jan		23 Jan		24 Jan		**18 Jan**		19 Jan	
E2	5 Feb		30 Jan		31 Jan		1 Feb		**25 Jan (Thurs)**	
E3	12 Feb		**6 Feb**		7 Feb		8 Feb		9 Feb	
E4	17 Feb **(Sat)**		**13 Feb**		14 Feb		15 Feb		16 Feb	
E5	**19 Feb**		20 Feb		21 Feb		22 Feb		23 Feb	
Mid-Sem Lab Quiz	**24/02/2018 (Saturday: 1000-1300) Based on Expt. 1-4 (L1-L4)**									
E6	**5 March**		6 March		7 March		8 March		16 March	
E6	**12 March**		13 March		14 March		15 March		17 March **(Sat)**	
E7	**19 March**		20 March		21 March		22 March		23 March	
E8	**2 April**		3 April		4 April		5 April		6 April	
Makeup Lab	**9 April**		10 April		11 April		12 April		13 April	
End-Sem Exam	16 April		17 April		18 April		19 April		20 April	

INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
Department of Electronics & Electrical Engineering
EE102: Basic Electronics Laboratory

EXPT. No. 1: FAMILIARIZATION WITH THE LABORATORY EQUIPMENTS

1. Making Groups: Grouping will be done on the first day of lab and each group will consist of 2 members.

2. Suggested sitting arrangement for Groups: The position of each group is marked on the experiment desks. Each group has to occupy the respective place.

3. Announcements: There will be 8 experiments.

(a) Lab. Evaluation is group-wise. [Lab Quiz & End sem evaluation on individual basis]

(b) The marks for different experiments done during assigned laboratories hours are given below: Marks for the lab performance will be given on the same day of experiments while marks for the lab report will be given on the next lab day.

E1 - 50 marks	(Lab reports (10) + lab performance (40))
E2 - 60 marks	(Lab reports (12) + lab performance (48))
E3 - 60 marks	(Lab reports (12) + lab performance (48))
E4 - 70 marks	(Lab reports (14) + lab performance (56))
E5 - 70 marks	(Lab reports (14) + lab performance (56))
E6 - 80 marks	(Lab reports (16) + lab performance (64))
E7 - 80 marks	(Lab reports (16) + lab performance (64))
E8 - 80 marks	(Lab reports (16) + lab performance (64))

8 experiments carry (1 x 50 + 2 x 60 + 2 x 70 + 3 x 80)/10 = 55 marks

Mid semester (Lab Quiz) = 15 marks

End semester = 30 marks

Total = 100 marks

4. Lab report submission: (a) one common lab report for each experiment should be submitted by each group. Lab report submission must be on next lab day. Lab reports should be hand written on A4 size paper.

(b) If one of the group members is absent for a particular experiment, his/her name should not be included in the lab report.

(c) No marks will be given for makeup lab

(d) Lab reports should not be copied from anywhere, if found zero marks will be awarded.

5. Any act of indiscipline will lead you to debar from the lab forever.

6. Announcement to be made by the instructor/TA

a. Switch on your function generator & Oscilloscope. Then, you proceed for demonstration

b. Four TAs should divide the groups to demonstrate waveforms on the scope. Please demonstrate the calibration of the scope by showing the built-in square wave of 1 KHz in the scope (APLAB only 0.2V, scientific 0.2V and 2V).

c. The measurement of signal from function generator is to be carried out by the students. If the displayed value on the function generator if different from the value obtained through CRO reading, it should be mentioned accordingly in the lab report.

EXERCISE

Perform the following exercise and write the observations on the sheet given for this purpose. Show your result to the TA/instructor and get the observations signed. Submit it in the next lab session along with the answers to the questions given at the end.

Set a function generator to output a triangular waveform of 2.3 kHz. Connect the output of the function generator to Channel 2 of an oscilloscope. Adjust appropriate knobs of the oscilloscope to get a stable display of the triangular wave. Measure the period of the waveform by counting the number of divisions per cycle on the time axis (x-axis) of the display and calculate the frequency of the waveform. Write the observations below

Time scale =

Number of divisions =

Period=

Frequency =

With the oscilloscope connected, adjust the knobs of the function generator to obtain a square wave of frequency 5 kHz and amplitude 5 Vp-p by doing measurement on the oscilloscope screen (ignore the indicator on the function generator). Write the following parameters you have set on the oscilloscope.

Selected time scale =

Required number of divisions on x-axis =

Selected amplitude scale =

Required number of divisions on y-axis =

Q1. Write the values of the resistances (in Ω, kΩ, or MΩ) provided to you in the box using colour codes.

a)

b)

c)

d)

Q2. What is the value of a capacitor on which 104K is written?

Answer the following questions on a separate sheet and attach it to this sheet.

Q3. Write the colour code used to specify the value of a resistance.

Q4. How cathode and anode are generally indicated on a diode?

Q5. What does the notch on a transistor indicate?

Q6. Draw a circuit diagram to generate a variable voltage from 0 to 5 V using a potentiometer and a fixed power supply of 5 V.

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EXPT. NO 2 : Circuit Theorems

OBJECTIVE: Verification of superposition theorem, Thevenin's theorem and maximum power transfer theorem

MATERIALS REQUIRED

- Breadboard
- Equipment : Multioutput DC Power Supply, Oscilloscope
- Components : Resistances: One 10 Ω, One 560 Ω, Three 1 kΩ, Three 2.2 kΩ, One 3.9 kΩ, One 4.7 kΩ

PRECAUTIONS AND GUIDELINES

1. Make sure the ground terminals of the oscilloscope probes and power supplies are connected together in the circuit.

2. While switching on the set-up, switch on the oscilloscope first, followed by the power supply.

Pre-experiment observation

Part A: For the circuit shown in Fig. 1, find the voltage V_C across resistance R for the cases listed in Table 1. Assume V_1 = 12 V, V_2 = 5 V and zero source resistances. Also repeat the same for V_1 = 15 V and V_2 = 5 V.

Part B: Calculate the Thevenin's voltage and resistance a seen into terminals A-B of the circuit given in Fig 2.

Part C: For the circuit in Fig 2, find the value of R_L for which maximum power transfer would take place and also find the value of maximum power transferred.

Part A: SUPERPOSITION THEOREM

The response of any circuit variable in a multi-source linear memoryless circuit containing 'n' independent sources can be obtained by adding the responses of the same circuit variable in 'n' single-source circuit with i^{th} independent source active and all the remaining independent sources deactivated.

1. Assemble the circuit shown in Fig. 1. Use 0-32V and 5V sources of the multi-output DC power supply for realizing voltage sources V_1 and V_2 in the circuit.

2. For the safety of resistors, do not apply more than 20 V from 0-32V source for the experiment purpose.

3. Verify the superposition theorem for the voltage V_C developed across the resistance R due to voltage sources V_1 and V_2.

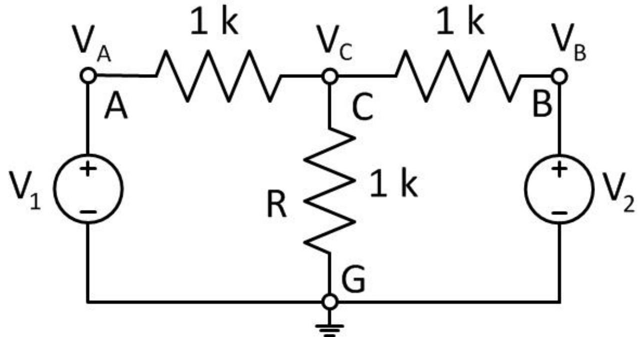

Fig. 1

Take the measurements listed in Table 1. Verify that voltage V_C for Case I is the sum of voltages obtained in Case II and III.

Case	Circuit modification required	V_1 (V)	V_2 (V)	V_A (V)	V_B (V)	V_C (V)
I	Both sources connected	12	5			
II	V_2 removed from circuit and port B-G shorted	12	0			
III	V_1 removed from circuit and port A-G shorted	0	5			

Table. 1

Repeat the experiment for V_1 = 15 V while keeping V_2 = 5 V.

4. Comment on the possible cause if the superposition theorem is not verified exactly.

Part B: THEVENIN'S THEOREM

Any linear electrical network with voltage and current sources and resistances can be replaced at terminals A-B by an equivalent voltage source V_{th} in series connection with an equivalent resistance R_{th}.

- ***This equivalent voltage V_{th} is the voltage obtained at terminals A-B of the network with terminals A-B open circuited.***
- ***This equivalent resistance R_{th} is the resistance obtained at terminals A-B of the network with all its current sources open circuited and all its voltage sources short circuited.***

1. Assemble the circuit as shown in Fig. 2. Find the Thevenin's equivalent as seen into terminals A-B.

2. To find Thevenin's equivalent voltage V_{th}, remove load R_L and measure the open circuit voltage cross terminals A-B (V_{oc}) with help of CRO.

3. To find Thevenin's equivalent resistance R_{th}, first determine the current through the terminals A-B when shorted. As we cannot directly measure current using CRO so connect a small resistance 10 Ω across A-B terminals and measure the voltage drop $V_{10\Omega}$ .Now the R_{th} can be computed as $R_{th} = 10 \times (V_{oc} / V_{10\Omega})$ Ω.

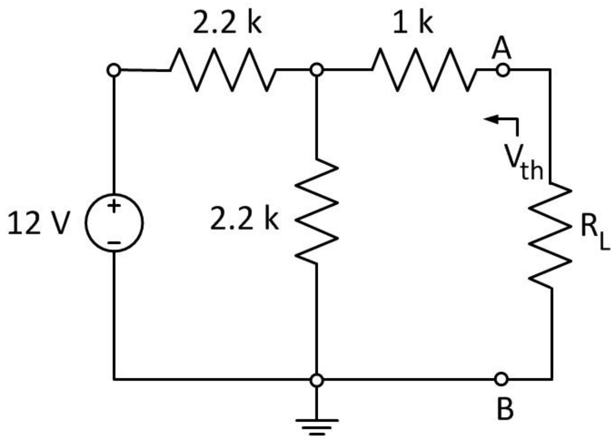

Fig. 2

4. Give comment for any difference observed among the values obtained by following the above procedure and the theoretically computed ones.

Part C: MAXIMUM POWER TRANSFER THEOREM

The power delivered by a linear time invariant memoryless circuit containing independent DC sources is a maximum when the value of the load is equal to the Thevenin's equivalent resistance seen by it.

1. Re-assemble the circuit as shown in Fig. 2. Now the objective is to verify the maximum power transfer theorem for the load R_L connected across terminals A-B. The power transferred to a load is product of voltage drop across it and the current flowing through it.

2. To measure the current through load R_L using CRO, a small resistance10 Ω is connected in series as shown in Fig. 3 and measure the voltage drop across terminals C-B (Ch2). The voltage drop across terminals A-B is to be approximated for the voltage drop across the load R_L.

3. Find out the power for varying values of the load R_L as suggested in Table 2.

4. Note the value of the load resistance for which the power turns out to be the maximum among the load resistance values considered. Compare it with the Thevenin's equivalent resistance determined in Part B.

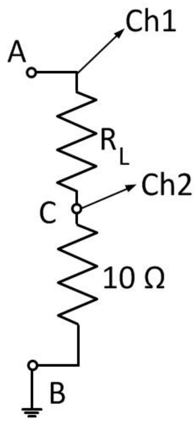

Fig.3

R_L (Ω)	V_A (V) to Ch1	V_C (V) to Ch2	I_{RL} (= V_C / 10Ω)	Power (Watt)
560				
1 k				
2.2 k				
3.9 k				
4.7 k				

Table. 2

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EXPT. NO 3 : RLC Circuits

OBJECTIVE: To find the step response of RC and RL circuits and RLC series circuit resonance

MATERIALS REQUIRED

- Breadboard
- Equipment : Function Generator, Oscilloscope
- Components : Resistors: One 1 k Ω, One 4.7 kΩ; Inductor: 0.1 H; Capacitors: One 0.1 μF, One 1 μF

PRECAUTIONS AND GUIDELINES

1. Make sure the ground terminals of the oscilloscope probes and function generator are connected together.

2. While switching on the set-up, switch on the oscilloscope first, followed by the function generator.

Pre-experiment observation

Part A: Calculate the value of the time constant for RC circuit given in Fig. 1.
Part B: Calculate the value of the time constant for RL circuit given in Fig. 2.
Part C: Find the value of the resonant frequency for RLC circuit given in Fig. 3 using the formula

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Part A: STEP RESPONSE OF RC CIRCUIT

When a step input V_S is applied to an RC circuit with no charge on capacitor, the capacitor starts charging towards V_S with time 't'. The instantaneous voltage across capacitor is given by $V_C(t) = V_S(1-\exp(-t/RC))$. The time required by the capacitor to charge up to 63% of full charge voltage is called the time-constant 'τ' of RC circuit and is given by $\tau = RC$.

1. Assemble the circuit shown in Fig. 1. Connect Ch1 and Ch2 probes of CRO to node A and node B, respectively. Use the dc coupling mode of CRO for this part of the experiment.

2. Apply a **unipolar** square wave input (5 V; 0.1 kHz) from the function generator.

3. Observe the voltages at node A and node B in CRO and measure the time-constant 'τ' by noting the time taken by the capacitor to rise to 63% of its maximum charge voltage.

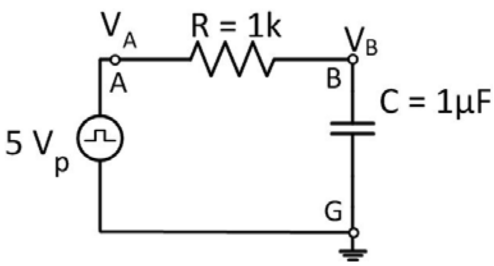

Fig. 1

4. Now increase the frequency of the input signal and note the frequency 'f' for which the capacitor just gets charged up to maximum possible voltage. Find the ratio of T/τ, where $T = 1/f$.

Part B: STEP RESPONSE OF RL CIRCUIT

When a step input V_S is applied to an RL circuit with inductor having no stored energy, initially the current through it is zero but increases towards the maximum value of V_S/R with time 't'. The instantaneous value of current through inductor is given by $I_L(t) = (V_S/R)(1-\exp(-Rt/L))$. The time required by the voltage across inductor to drop to 37% of maximum voltage or the voltage across resistor to rise up to 63% of maximum voltage is called the time-constant 'τ' of RL circuit and is given by $\tau = L/R$.

1. Assemble the circuit shown in Fig. 2. Connect Ch1 and Ch2 probes of CRO to node A and node B, respectively. Keep using the dc coupling mode of the CRO.

2. Apply a unipolar square wave input (5 V; 0.5 kHz).

3. Observe the voltages at node A and node B in CRO and measure the time-constant 'τ' by noting the time taken by the voltage drop across resistor to rise to 63% of its maximum value.

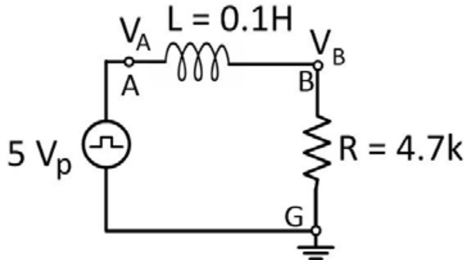

Fig. 2

Part C: RESONANCE IN SERIES RLC CIRCUIT

The resonance in a series RLC circuit is a state where the current drawn from the source is in phase with the voltage applied. This occurs at a particular frequency which is called the resonant frequency. At resonance, the reactance of the inductor and that of the capacitor cancel each other so the RLC circuit offers minimum impedance and hence the current through the circuit is maximized.

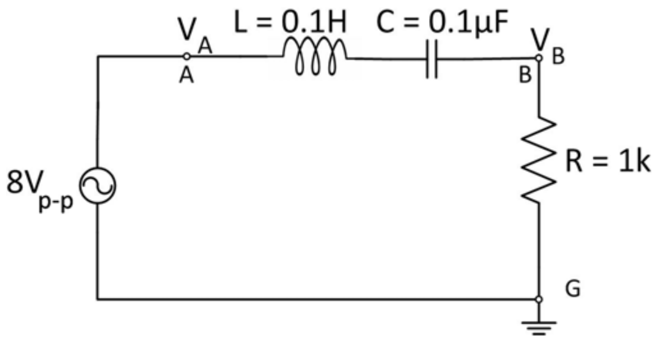

Fig. 3

1. Assemble the circuit as shown in Fig. 3. Apply a sinusoidal input (8 Vp-p) to the circuit.

2. Using CRO measure the applied input across terminals A-G in Ch1 and the current through RLC circuit through the voltage drop across terminals B-G in Ch2.

3. Vary the frequency of the function generator as suggested below and measure the peak-to-peak amplitude of voltage across terminals B-G (Ch2) which proportional to the current in the circuit.
   Estimate the coarse resonant frequency of the RLC circuit from these measurements.

Frequency (in KHz)	Voltage across B-G
0.1	
0.5	
1.0	
1.5	
2.0	
4.0	
10.0	

4. To refine the estimate of resonant frequency, set the function generator again to the coarse estimate of the resonant frequency and now observe the phase difference between the applied input voltage (Ch1) and the circuit current (Ch2). Finely varying the frequency of the function generator till voltages in Ch1 and Ch2 get phase synchronized. The frequency at which synchronization is achieved is a precise estimate of the resonant frequency of the RLC circuit. Compare that with theoretically computed value.

5. In the same setup, reset input frequency to 0.1 kHz and observe the amount and the nature of the phase difference between Ch1 and Ch2.

6. Repeat step 5 for input frequency of 10 kHz instead of 0.1 kHz.

7. Comment on the cause of the observations made in step 5 and 6, if any. Also draw the phasor diagram of voltages across all three components at resonant frequency using given nominal value of components.

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EXPT. No. 4 : DIODE CIRCUITS

OBJECTIVES : Design and analysis of half wave rectifier and clipping circuits.

MATERIALS REQUIRED

- Breadboard
- Equipment : Function Generator, Oscilloscope
- Components :
  - Diode : One: Type 1N4007 (Diode voltage drop V_D = 0.7V)
  - Zener Diode : One: (Zener voltage V_Z = 3.9 V)
  - Resistance : Four: 56 Ω, 1 kΩ, 2.2 kΩ, 4.7 kΩ
  - Capacitor : One: 22 µF.

GENERAL GUIDELINES / PREQUATIONS

1. Connect the capacitor with correct polarity. The capacitor being of electrolytic type, it is polarized, and will be damaged if connected with incorrect polarity. Similarly, confirm the polarity of the diodes before connecting.
2. Keep ground terminals of oscilloscope probes and function generator output connected together throughout the experiment.
3. In an oscilloscope, for higher precision, increase vertical sensitivity (i.e. lower value of volt/div), especially while measuring small amplitude levels (e.g. ripple voltage). You may need to switch to ac coupling while doing so.

PART A : HALF - WAVE RECTIFIER WITHOUT FILTER

1. Set the function generator to obtain 10 V peak-to-peak sine wave at 500 Hz frequency. Do not connect any circuit to the function generator. Keep dc offset equal to 0. Observe the function generator output on the oscilloscope and verify sine wave generation.
2. Set up the circuit as shown in Fig. 1(a) without the capacitor C, taking R_L = 2.2 kΩ.
3. Now, connect the function generator to the circuit at points F_1 & F_2 as shown in Fig. 1(a).
4. Display V_i and V_o simultaneously on the oscilloscope. ***Sketch*** V_i and V_o one below the other with identical time and amplitude axes.

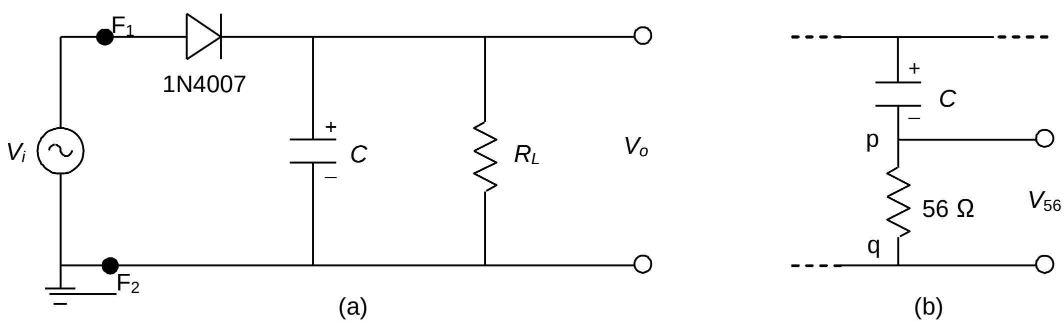

Fig. 1 Half-wave rectifier.

PART B : HALF - WAVE RECTIFIER WITH CAPACITOR FILTER

1. Now connect a capacitor C = 22 µF in the circuit with correct polarity as shown in Fig. 1(a).
2. Display V_i and V_o simultaneously on the oscilloscope. ***Sketch*** V_i and V_o overlapping, with the same time and amplitude axes.
3. ***Measure*** peak-to-peak ripple voltage on oscilloscope by enlarging V_o to the maximum extent. You may have to put the input coupling in ac mode while doing this measurement. See the guidelines given at the end. Repeat steps 2 and 3 for R_L = 1 kΩ and 4.7 kΩ. ***Comment*** on the output waveforms and ripple voltages.
4. Connect a 56Ω resistance in series with C of Fig. 1(a) as shown in Fig. 1(b). The points across this 56Ω resistor are marked as **p** and **q.**

Please note that: The resistance 56Ω is chosen small enough not to affect the overall performance of the circuit and at the same time to ensure an appreciable voltage across it. This voltage represents the current flowing through the capacitor.

5. Display and ***sketch*** V_o and V_{56} (i.e. voltage across 56Ω between 'p' and 'q') one below the other with identical time axes. Mark the ground reference line.

Q. 1 : Why is I_C ($=V_{56}$ / 56), the current through the capacitor, negative for some portion of a cycle? Estimate I_{surge} (positive peak of I_C).

PART C : CLIPPING CIRCUIT - POSITIVE CLIPPER

1. Connect the circuit as shown in Fig. 2 with R = 2.2 kΩ.
2. Set the function generator to get 20 V peak-to-peak sine wave at 500 Hz frequency. Observe the function generator output on the oscilloscope and verify sine wave generation.
3. Connect the function generator output to the circuit as shown in Fig. 2.
4. Display and ***sketch*** V_i and V_o one below the other with identical time and amplitude axes.
5. Superimpose the two waveforms V_i and V_o and observe.
6. Set the oscilloscope in X-Y mode (V_i to Ch2 : X-input and V_o to Ch1 : Y-input) and ***sketch*** V_o versus V_i with equal x and y scales. Label the graph and ticks on the axes.

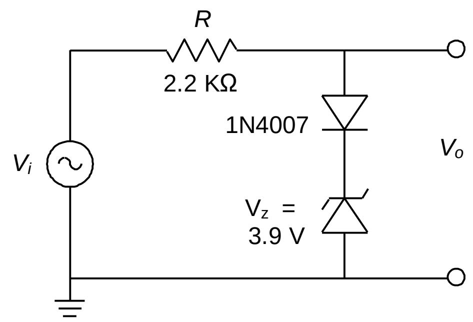

Fig. 2 Positive clipper

Q. 2 : Draw the circuit diagrams for : (a) –ve clipper

(b) +ve and –ve clipper

<u>**Pre observation reading:**</u>

(a) Draw the expected waveforms at – (i) Step no. 4 of PART A,

(ii) Step no. 2 of PART B and

(iii) Step no. 4 of PART C.

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EXPT. No. 5 : POWER SUPPLY

OBJECTIVES : Design and analysis of full-wave rectifier and zener regulator.

MATERIALS REQUIRED

- Breadboard
- Equipment : Oscilloscope
- Components :
    - Transformer : One: 230 V to 12–0–12 V
    - Diode : Two: Type 1N4007 (Forward voltage drop V_F = 0.7V)
    - Zener Diode : One: (Zener voltage V_Z = 6.2 V)
    - Resistance : Three: 220 Ω, 560 Ω, 1 kΩ
    - Capacitor : One: 100 μF.

GENERAL GUIDELINES

1. Switch on the mains supply to the transformer only after you have made all other connections (in order to avoid electric shock).
2. Also, while making any changes in the circuit, switch off the mains supply to the transformer.
3. Connect the capacitor with correct polarity. The capacitor being of electrolytic type, it is polarized, and will be damaged if connected with incorrect polarity. Similarly, confirm the polarity of the diodes before connecting.
4. Use "*line*" as the source of triggering in the oscilloscope. Put the oscilloscope in *CHOP* mode.

PART A : Unregulated Power Supply : Using center tapped Transformer and Full - Wave Rectifier (FWR)

i) Full-wave rectifier (FWR)

1. Set up the circuit as shown in Fig. 1 without the capacitor *C*. The transformer TX has rating of 230 V to 12-0-12 V,1 A. Take R_L = 1 kΩ. Connect transformer primary to the mains and switch on the mains. Display the secondary voltages V_{AG} and V_{BG} (V_{AG} to Ch-1, V_{BG} to Ch-2) on the oscilloscope. Make sure that both the "probe grounds" are connected to the circuit ground. Sketch the waveforms overlapping, with the same time and amplitude axes. They should be 180° out of phase.
2. Display and sketch the full-wave rectified output V_o across R_L. Measure the peak voltages in both halves.

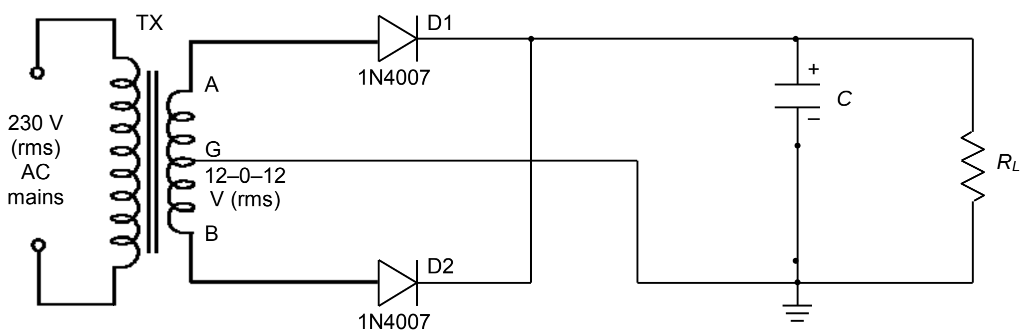

Fig. 1 Power supply using a centre tapped transformer and full-wave rectifier.

Q. 1 : If the peak amplitudes are not equal, what could be the reason?

3. Now connect *C* = 100 μF as shown in Fig. 1. Sketch V_o and measure V_r (peak-to- peak ripple voltage). Set the oscilloscope channel to *AC coupling* and increase vertical sensitivity (decrease V/div) while measuring V_r.

ii) Comparison with half-wave rectifier (HWR)

1. Remove diode D2. The circuit is now a HWR with C-filter.
2. Compare V_r values in FWR and HWR.

Q. 2 : What are the ripple frequencies in FWR and HWR?

PART B : Regulated Power Supply : FULL - WAVE RECTIFIER WITH ZENER REGULATOR

1. Connect a zener diode D_Z with series resistance R = 560 Ω as shown in Fig. 2. The voltage across D_Z will now be the desired (regulated) output voltage V_{oR} which will supply current I_L to the external load R_L .
2. With $R_L = \infty$, using the oscilloscope measure $V_{o\ max}$, the maximum of V_o (the unregulated DC along with ripple) & V_r (peak to peak ripple) at point 1 (unregulated output). Similarly obtain $V_{oR\ max}$, the maximum of V_{oR} (the regulated DC along with ripple) & V_{rR} at point 1 (regulated output). You will find V_{rR} to be very small, hence you may have to increase the oscilloscope sensitivity suitably.

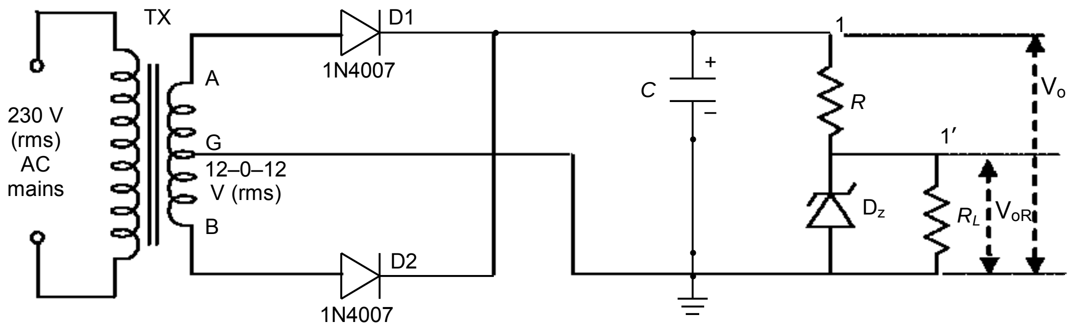

Fig. 2 Regulated Power Supply with zener diode.

3. Calculate : $V_{o\ av} = V_{o\ max} - V_r\ / 2$, and $V_{oR\ av} = V_{oR\ max} - V_{rR}\ / 2 \approx V_{oR\ max}$. You will notice that the average regulated voltage $V_{oR\ av} \approx V_{oR\ max}$ (almost equal since V_{rR} is very small).
4. Compute I_R, I_Z, and I_L (all average values), and the power dissipations : $P_Z = V_Z\ I_Z$, ($V_Z = V_{oR\ av}$), and $P_R = V_R\ I_R$, (V_R = voltage across R = $V_{o\ av} - V_{oR\ av}$).
5. Repeat step 2 and 3 for R_L = 1 kΩ and 220 Ω. Enter the measured and calculated values in a tabular form as shown below :

R_L	$V_{o\ max}$	V_r	$V_{oR\ max}$	V_{rR}	$V_{o\ av}$	$V_{oR\ av}$	I_R	I_L	I_Z	P_Z	P_R	%Reg
∞												
1 kΩ												
220 Ω												

% Regulation is defined as :

% Reg = $[\ \{\ (V_{oR\ av})_{\text{NO-LOAD}} - (V_{oR\ av})_{\text{LOADED}}\ \}\ /\ (V_{oR,av})_{\text{NO-LOAD}}\ ] \times 100$

Q. 4 : Do you observe poor regulation for some I_L? Why does it occur?

Q. 5 : What is the maximum load current the zener regulator (under test) can supply? Given that $I_{Z\ min}$ = 5 mA and the maximum power dissipation in the zener is ½ W.

Q. 6 : How would you modify the circuit to provide an even higher I_L? What is this maximum value?

Q. 7 : What are the wattage ratings of the resistances you will use in the modified circuit for the maximum I_L value obtained in Q.6? (Standard wattage ratings : ¼ W, ½ W, 1 W, 2 W, 5 W etc.)

Q. 8 : Have you used the correct wattage resistances for the circuit under test?

INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

DEPARTMENT OF ELECTRONICS & ELECTRICAL ENGINEERING

EE102 : BASIC ELECTRONICS LABORATORY

Expt. No. 6 Study of Common-emitter Amplifier

OBJECTIVES :

1. To carry out an approximate DC and AC-analysis of the given CE amplifier.
2. To determine the voltage gain, the "maximum undistorted peak-to-peak output voltage swing" (MUOVS) and the maximum input voltage for undistorted output.
3. To study the effect of emitter bypass capacitor on voltage gain.

MATERIALS REQUIRED

- Breadboard
- Equipment and parts : Multi-output Power Supply, Function Generator, Oscilloscope, Digital Multimeter.

Transistor	: One- NPN type 2N2222A.
Resistor	: Five - 470 Ω, 1K Ω, 2.2 K Ω, 22 K Ω, 100K Ω.
Variable resistor	: One - 1KΩ Pot. (Potentiometer).
Capacitor	: Three - 10 μ F, 10 μ F, 22 μ F

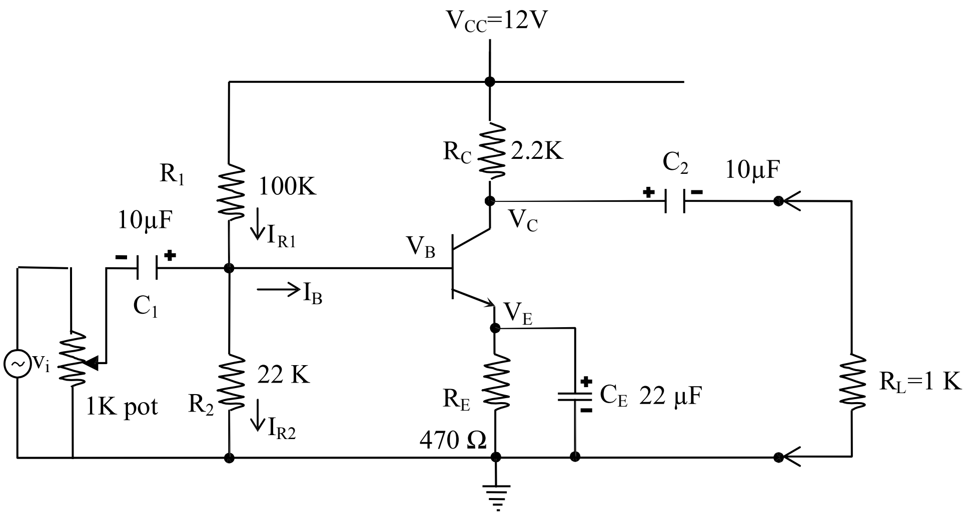

Fig. 1 : Common-emitter amplifier

Important: You are expected to complete Part-I at home and come to the Lab with a neat report showing all calculations. You will be allowed to continue with the rest of the experiment only after the instructor has checked the report.

Part-I. Pre-experiment preparation

Approximate DC and AC-analysis:

Carry out an approximate DC-analysis by using the values given in Fig. 1 and by making use of the following assumptions:

(a) $I_{R1}, I_{R2} >> I_B$, so that $I_{R1} \approx I_{R2}$

(b) $V_{BE} \approx 0.65$ V

Under these assumptions, you should be able to estimate the

- DC quantities (quiescent values) $V_B, V_E, V_C, I_E (\approx I_C)$

- Voltage gain $A_V = -\frac{\beta R_C}{r_b} = -\frac{R_C}{r_b/\beta} \approx -\frac{R_C}{r_e} = -\frac{R_C}{V_T / I_E}$

$$= -\frac{R_C\ I_E}{V_T} \approx -\frac{R_C\ I_C}{V_T} \qquad \textbf{(1)}$$

where $V_T = \frac{kT}{q}$: the thermal voltage ; k= Boltzmann's constant = 1.38 x 10^{-23} J/K,

q = 1.6 x 10^{-19} Coulomb, T is temperature in ^{o}Kelvin.

Take $V_T \approx 25mV$ (at a room temp of 20^{o} C)

In (4.1), we have used the approximation $r_b = (\beta + 1)r_e \approx \beta r_e$

Note: The approximation does not require the knowledge of β

- MUOVS = 2 * Min{V_{CC} –V_C, V_C –V_E }

Q: (connecting an electrolytic capacitor) How do you decide that the + terminal of C_1 should be connected to the R_1–R_2 node and the – terminal to the source v_i ? Likewise, for C_2 and C_E..

2.1 Experimental determination of the quiescent voltages and currents:

a) Before assembling the circuit, measure the actual values of the resistors by means of a Digital Multi Meter (DMM). [Remember you are using resistors with 10% tolerance]. The actual values are to be used in determining the currents.

b) Now assemble the circuit, apply V_{CC} and note the following:
   - measure V_{BE} using DMM; it should be around 0.6 ~ 0.7 V indicating that BE-junction is forward biased.
   - Measure V_C and check if $V_E < V_C < V_{CC}$. A value of V_C midway between V_E and V_{CC} is preferable (**Q: Why is such a value preferable?**).

If your measurements agree, you are along the right path.

c) Now measure V_B , V_E , V_C and V_{CC} ; then using the measured resistance values, determine I_B, I_E, I_C and hence β (β=I_C/I_B).

d) Compare the experimentally determined values of the currents and voltages with those you obtained through approximate analysis.

e) Compare the experimentally determined value of β with the approximate value stated in the manual or given by the Lab Instructor.

f) Compute A_V (Equation 1) using the experimentally determined values of R_C and I_C. Use V_T=25mV.

2.2 Voltage gain without load resistance R_L :

- Disconnect C_2.
- Adjust FG to get approximately 10-20 mV peak-to-peak sinusoid at 1 kHz (display in Ch-I). Apply this voltage at amplifier input (v_i).
- Display collector voltage in Ch-II of CRO(use DC-coupling). Note the 180^{o} phase difference between the input and the output. Adjust v_{in} amplitude to get a convenient value for peak-to-peak collector voltage $v_{C,PP}$ (say 2 V). Use appropriate vertical sensitivity (V/div). Note the corresponding $v_{i,PP}$ (mV). Experimentally obtained voltage gain is therefore:

$$A_V = \frac{-v_{C,PP}}{v_{i,PP}}$$

- Compare this value with the computed values obtained in step 2.1(f). Also compare this value with the value estimated in your pre-reading assignment.

3. Maximum undistorted output voltage swing (MUOVS)

- Increase v_i slowly till you observe a slight flattening of v_C waveform at its peaks (either positive peaks or negative peaks). The peak-to-peak value of the output signal (just at the onset of distortion/clipping) is the MUOVS. Measure the corresponding $v_{i,\,PP}$, the peak-to-peak input voltage.

  This information is useful in an amplifier: it tells the user that the input should not exceed this value for faithful amplification of the signal, else distortions sets in.
- Now increase v_i beyond this point and observe the output waveform. The sinusoid gets increasingly flattened and becomes more like a square wave.
  (overdriving an amplifier leads to heavy distortion)

  [!! Square-wave from a sine-wave]

4. Voltage-gain with load resistance R_L :

The output of an amplifier normally drives a load resistance R_L which may represent an actual load like an ear-phone or a loudspeaker, or the input impedance of another state of amplifier.

- Connect R_L (see circuit) to the collector through the coupling capacitor C_2 (C_2 blocks the DC voltage at the collector and allows only the AC i.e. the signal component to pass through).
- Measure A_V with R_L connected. (you would observe a reduced A_v since $R_{C,eff} = R_C \| R_L$).

5. Effect of C_E on A_v :

- Get back to the conditions in Part 2.2 i.e. v_i at 1 kHz, its amplitude adjusted to get $v_{C,PP} \approx$ 2V .
- Now, remove C_E (with ckt. powered) and note the drastic reduction in $v_{C,PP}$. You have to change to appropriate V/div in your CRO. Determine the gain of the CE amplifier with unbypassed R_E.
- Compare your observation with the theoretical value

$$A_v = -\frac{\alpha R_C}{(R_E + r_e)} \approx -\frac{R_C}{R_E} \qquad \textbf{(2)}$$

- Display and sketch v_i and v_E waveforms. Note the amplitudes and the phase-relationship between them.
- Display and sketch v_E and v_C. Note the amplitudes and the phase relationship. Please note that you are in DC coupling mode of the CRO. Please ensure that when you pressed the ground options in CH1 and CH2, both the horizontal traces (of CH1 and CH2) are coinciding. Also ensure that the V/div of CH1 is equal to V/div of CH2.
- Increase v_i gradually and observe how v_E and v_C change. Continue to increase v_i till you observe the +ve peak of v_E (almost) touching the negative peak of v_C. When this occurs, we say that the BJT has gone into saturation ($v_{CE} \approx 0$).

Q: What do you observe if v_i is increased beyond this point ?

INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

Department of Electronics & Electrical Engineering

EE102: Basic Electronics Laboratory

EXPT. No. 7 : OPERATIONAL AMPLIFIER

OBJECTIVE : Realization of amplifier circuits with Op-Amp (Operational Amplifier).

MATERIALS REQUIRED

- Breadboard
- Equipment : Multioutput DC Power Supply, Function Generator, Oscilloscope.
- Components
  - Op-Amp : One: LM741.
  - Resistance : Five: 1 kΩ (1 no), 10 kΩ (1 no), 12 kΩ (2 nos), 100 kΩ (1 no).

PRECAUTIONS AND GUIDELINES

1. The op-amp generally works on split power supply (e.g. ±12 V). Both positive and negative power supplies must be present whenever op-amp is powered. The range of power supply is from ±12 V to ±15 V. Do not forget to connect the common terminal of the power supply to the *ground* on the breadboard.
2. Connecting only one side of power supply or interchanging positive and negative power supplies damages the op-amp.
3. For connecting power supply, you have to follow the procedure as given below.
   a. Disconnect the power supply to op-amps.
   b. Switch on the power supply.
   c. Set the output voltage as required (e.g. ±12 V).
   d. Switch off the power supply.
   e. Connect the power supply to op-amps.
   f. Switch on the power supply.
4. For any IC, never exceed the input voltage beyond the power supply limits.
5. Use the horizontal strips of the breadboard for power supply. Tap the power supply for each IC from these supply lines.
6. Keep ground terminals of the oscilloscope probes and function generator output, and power supply common connected together throughout the experiment.

Pre-experiment Reading:

Obtain theoretical values of V_o / V_i for step 5 of Part A. Do this for Part B also.

PART A : INVERTING AMPLIFIER

1. Assemble the circuit shown in Fig. 1 with R_1 = 10 kΩ and R_2 = 1 kΩ. Make sure the power supply ground is connected to the circuit ground.

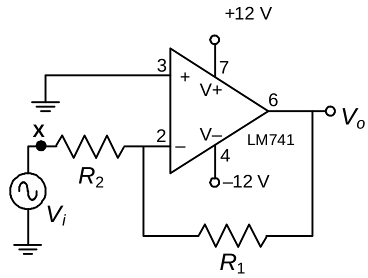

Fig. 1 Inverting amplifier

2. Apply 200 mVp-p, 1 kHz sine wave at V_i from the function generator and see the output.
3. Observe V_o and V_i, and determine voltage gain $A = V_o / V_i$. Also obtain A for V_i = 100 mVp-p and 300 mVp-p.
4. Change R_1 & R_2 to 100 kΩ & 10 kΩ and determine A for V_i = 100 mVp-p, 200 mVp-p and 300 mVp-p.
5. Now apply a fraction of the voltage V_i (keeping V_i at 200 mVp-p) to the point 'X' through the potential divider circuit as shown in Fig. 2 and note the values of V_o for

(i) $$R_1/R_2 = \frac{100\,\text{k}\Omega}{10\,\text{k}\Omega}$$ and

(ii) $$R_1/R_2 = \frac{10\,\text{k}\Omega}{1\,\text{k}\Omega}$$

Compute V_o / V_i for (i) and (ii).

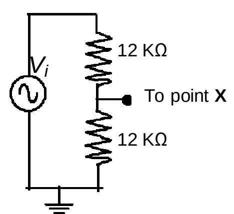

Fig. 2 Voltage Divider

PART B : NON-INVERTING AMPLIFIER

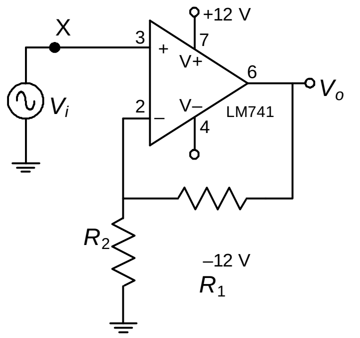

Fig. 3 Non-inverting amplifier

1) Assemble the circuit shown in Fig. 3 with R_1 = 10 kΩ and R_2 = 1 kΩ. Make sure the power supply ground is connected to the circuit ground.

2) Apply 200 mVp-p, 1 kHz sine wave at V_i from the function generator and see the output.

3) Observe V_o and V_i, and determine voltage gain $A = V_o / V_i$. Also obtain A for V_i = 100 mVp-p and 300 mVp-p.

4) Change R_1 & R_2 to 100 kΩ & 10 kΩ and determine A for V_i = 100 mVp-p, 200 mVp-p and 300 mVp-p.

5) Now apply a fraction of the voltage V_i (keeping V_i at 200 mVp-p) to the point 'X' through the potential divider circuit as shown in Fig. 2 and note the values of V_o for

(i) $R_1 / R_2 = \dfrac{100\,\text{k}\Omega}{10\,\text{k}\Omega}$ and

(ii) $R_1 / R_2 = \dfrac{10\,\text{k}\Omega}{1\,\text{k}\Omega}$

Compute V_o / V_i for (i) and (ii).

Q1. For a source with high internal impedance which configuration (inverting or non-inverting) will be suitable for designing a good amplifier?

PART C : NON-INVERTING HIGH PASS FILTER

The circuit given below is a non-inverting amplifier with the RC circuit at the non-inverting terminal of the OPAMP acting as a frequency dependent voltage divider. Cut-off frequency of this RC arrangement is given as

$$\boldsymbol{f_c = \frac{1}{2\pi RC}}$$

Using this formula, find the theoretical value of cut-off frequency.

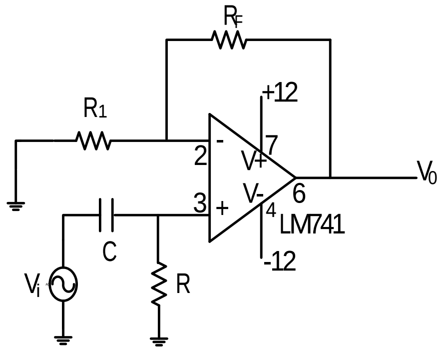

Fig. 4 Non-inverting high pass filter

1) Assemble the circuit shown in Fig. 4 with R_1 = 10 kΩ, R_2 = 100kΩ, R=1 kΩ and C=0.1µF. Make surethe power supply ground is connected to thecircuit ground.
2) Connect channel 1 of CRO to the input and channel 2 to the output of the circuit.
3) Apply 200 mVp-p at the input. Vary the frequency below and above the calculated cut-off frequency.
4) Observe corresponding V_o and V_i, and determine voltage gain $A = V_o / V_i$
5) Plot gain vs frequency graph and mark the cut-off frequency.

Note: Cut-off frequency is the frequency where gain falls below 70.7 % of the flat-band gain.

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EXPT. No. 8 : VOLTAGE TO FREQUENCY CONVERTER

OBJECTIVE: Designing a voltage to frequency converter.

MATERIALS REQUIRED

- Breadboard
- Equipment : Multioutput DC Power Supply, Oscilloscope.
- Components : Op-Amp : Two LM741.
  : Transistor : One 2N2222A
  : Diode : one 6.2V zener diode.
  : Resistance: One 330Ω, One 1kΩ, two 2.2KΩ, one 3.9KΩ, one 5.6KΩ, two 10 kΩ, three 100 kΩ.
  : Capacitor : One 0.01 µF.

PRECAUTIONS AND GUIDELINES

1. The op-amp generally works on split power supply (e.g. ±12 V). Both positive and negative power supplies must be present whenever op-amp is powered. The range of power supply is from ±12 V to ±15 V. Do not forget to connect the common terminal of the power supply to the *ground* on the breadboard.
2. Connecting only one side of power supply or interchanging positive and negative power supplies damages the op-amp.
3. While switching on the set-up, switch on the oscilloscope first, then the power supply to the circuit, and finally the function generator. When switching off, follow the sequence in reverse order.
4. For any IC, never exceed the input voltage beyond the power supply limits.
5. Keep ground terminals of the oscilloscope probes and function generator output, and power supply common connected together throughout the experiment.

The circuit shown in Fig. 1 is of Voltage to Frequency converter

Working Principle: Initially, the capacitor C gets charged at constant rate of (**V_i / R_3**) amp. The output voltage **V_a** at point '**a**' drops linearly till this voltage is not less than the voltage **V_b** at point '**b**' which is approx. at about -5.0V. Note that, the comparator output voltage **V_C** is at approx. -12V when **V_a** is greater than -5.0V and the transistor is in 'off' state.

When the negatively increasing voltage **V_a** becomes less than -5.0V, the comparator output **V_c** goes to approx. +12V. The transistor gets 'on' and hence the emitter voltage (also voltage at comparator '+' input) of the transistor is about at zero voltage. The transistor is in saturated state. The capacitor starts discharging. The discharging continues and **V_a** increases positively, till **V_a** becomes greater than zero voltage. The comparator output **V_C** becomes about -12V and the transistor becomes 'off'. This charging and discharging process repeats again and again. Note that the discharging duration is same for any input voltage **V_i** and it should be much smaller than the charging time, which depends on the input voltage **V_i**.

Pre-experiment Reading:

(a) Draw the waveforms at (i) V_a (ii) V_b and (iii) V_c
(b) Compute the charging time of the capacitor.
(c) Compute the discharging time of the capacitor.
(Assume V_i= 4V for above)

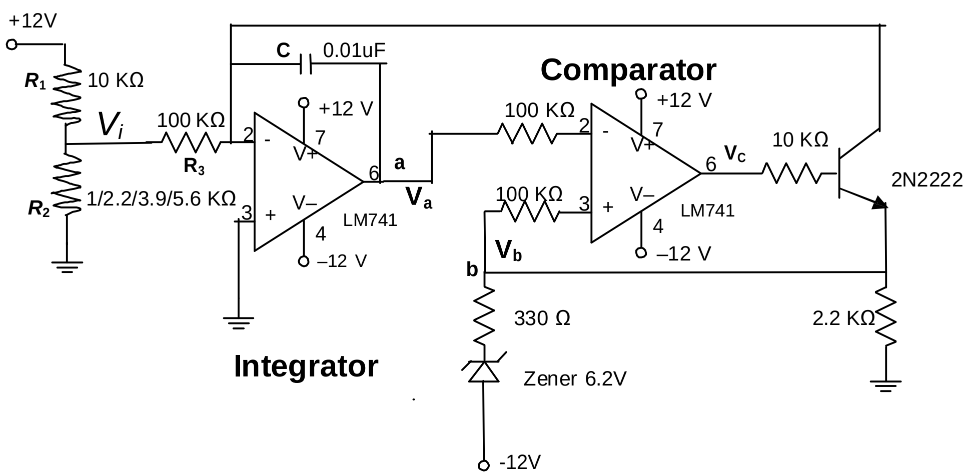

Fig. 1

OBSERVATIONS:

1. Connect the circuit as shown in Fig. 1 with R_1 = 10 kΩ, and R_2 = 1 kΩ. Make sure the power supply ground is connected to the circuit ground.

2. Observe the waveform $\mathbf{V_a}$ at point '**a**' for

   (a) for R_2 = 1 KΩ

   (b) for R_2 = 2.2 KΩ

   (c) for R_2 = 3.9KΩ

   (d) for R_2 = 5.6 KΩ

3. Similarly, observe the waveform V_b at point 'b' for all V_i as in step 2.

4. Remove the zener diode and replace it by a resistance so that V_b is approx. at -5.0V and observe V_b (both frequency and pulsewidth).
