

EE 311- VLSI Laboratory

FIR Low Pass Filter

Cut-off frequency = 14 Hz

Project Report



Introduction

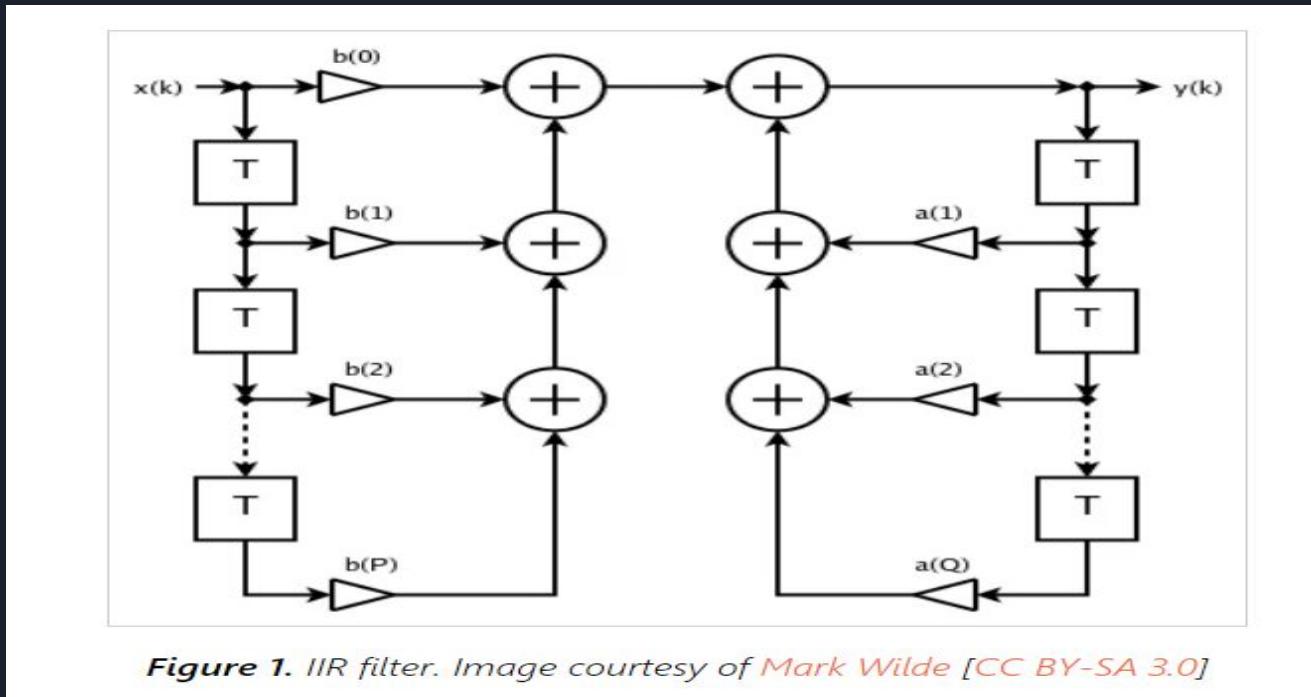
Analog and Digital Filters

In another aspect, filters can be constructed in two ways: digital and analog.

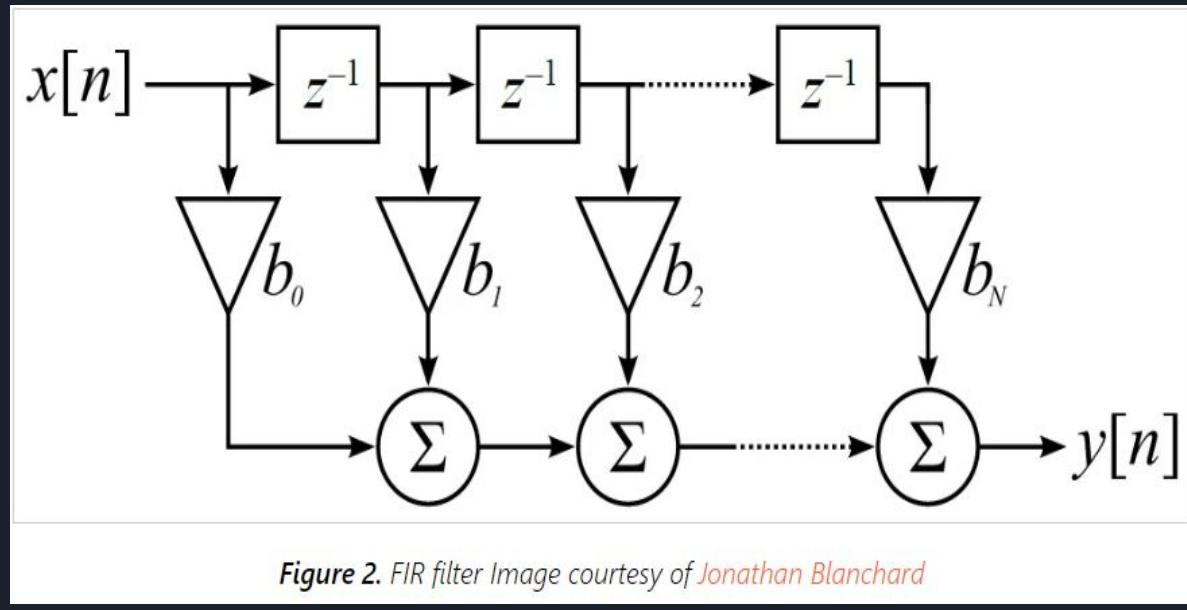
In an analog circuit, passive filters are a ladder of inductors and capacitors or resistors. Active analog filters can be a structure that exploits amplifiers or resonators. Their value can be determined simply by using tables or applications already created for designing analog filters.

Digital filters can be created with two methods, IIR and FIR. IIR (infinite impulse response) filters are the types of filters in which the output depends on the inputs and previous outputs.

IIR Filter



FIR Filter



- Moving average is a filter that averages N points of previous inputs and makes an output with them.

$$y[n] = \frac{1}{N} \sum_{i=0}^N x_{n-i}$$

- Therefore it is a FIR filter with N coefficients of 1/N.

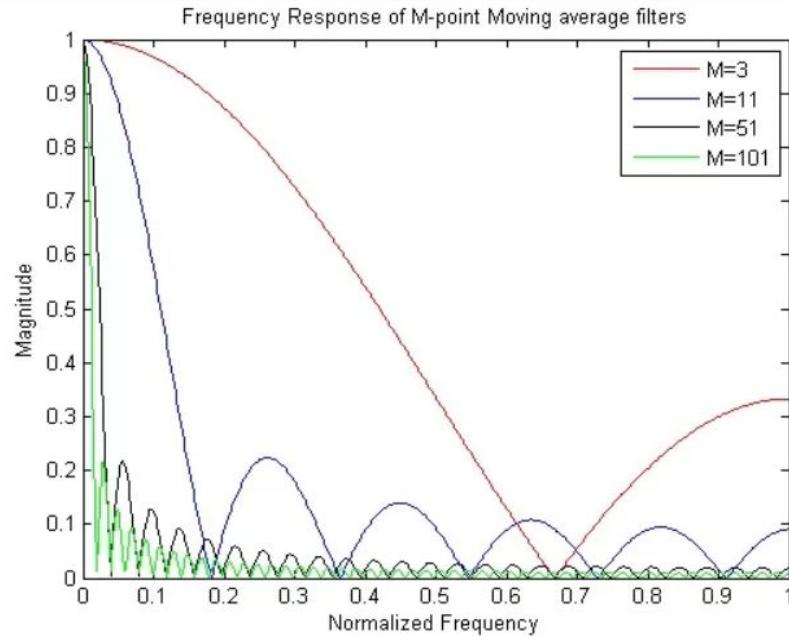


Figure 3. Frequency response of moving average

$$\pmb{y}[\pmb{n}] = \frac{\pmb{1}}{N}\sum_{i=0}^N\pmb{x}_{\pmb{n}-i}$$

$$h[n] = \frac{1}{N} \sum_{k=0}^{N-1} \delta[n-k]$$

$$\begin{aligned}H(\omega) &= \frac{1}{N} \frac{e^{-j\omega N/2}}{e^{-j\omega/2}} \frac{j2\sin\left(\frac{\omega N}{2}\right)}{j2\sin\left(\frac{\omega}{2}\right)} \\&= \frac{1}{N} \frac{e^{-j\omega N/2}}{e^{-j\omega/2}} \frac{\sin\left(\frac{\omega N}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}\end{aligned}$$



Cut-off Frequency

And cut-off frequency can be estimated as:

$$F_{co} = \frac{0.442947}{\sqrt{N^2 - 1}}$$

- For our case, $F_s = 250\text{Hz}$.
- That gives us the value of $N = 8$.

Code

```
1 module fir_filter (input sample_clock, input reset, input [19:0] input_sample1, output reg [19:0] output_sample1,output reg [23:0] finsummation2);
2
3 parameter N = 8; //Specify the number of taps
4
5 reg [19:0] delayholder[N-1:0];//for holding previous N-1 values and current value
6 reg [23:0] finsummation; //It will store the mean of N entries
7 //reg [19:0] finsummation2;
8 //reg div_en=1'b0;
9
10
11 integer z;
12
13 always @(posedge sample_clock or posedge reset)
14 begin
15 if(reset)
16 begin
17 // If reset then all values are set as zero
18 output_sample1 = 0;
19 for (z=0; z<N; z=z+1)
20 begin
21 delayholder[z] = 0;
22 end
23 end
24
25 else
26 begin
27 for (z=N-1; z>0; z=z-1)
28 begin
29 delayholder[z] = delayholder[z-1]; //shifting values
30 end
31 delayholder[0] = input_sample1; // current value stored
32 end
33
34 finsummation = 0;//initialisation
35 for (z=0; z<N; z=z+1)
36 begin
37 finsummation = finsummation + delayholder[z];//Sum calculation
38 end
39 finsummation2=finsummation;
40 finsummation=finsummation>>1;//Division by 2
41 finsummation=finsummation>>1;//Division by 2
42 finsummation=finsummation>>1;//Division by 2
43 //Now mean of 8 values stored in finsummation
44 output_sample1 = finsummation;
45 end
46 endmodule
```

Test Bench

```
1  `timescale 1ps/1fs
2  module test2;
3  reg sample_clock,reset;
4  reg [19:0] input_sample1;
5  wire [19:0] output_sample1;
6  wire [23:0] finsummation2;
7
8  //assign out2=output_sample1-3000;
9
10 fir_filter myfilter(sample_clock, reset,input_sample1,output_sample1,finsummation2);
11
12 initial sample_clock=1'b0;
13 always #1 sample_clock<=~sample_clock;
14
15
16 initial
17 begin
18     // $dumpfile("test2.vcd");
19     // $dumpvars(0, test2);
20     $monitor("%d ",output_sample1/*,output_sample1/*,finsummation2/*,out2*/);
21 end
22
23 /* #3 reset=1'b0; input_sample1=1;
24    #2 input_sample1=2;      //out2=output_sample1/8;
25    #2 input_sample1=3;      //out2=output_sample1/8;
26    #2 input_sample1=4;      //out2=output_sample1/8;
27    #2 input_sample1=5;      //out2=output_sample1/8;
28    #2 input_sample1=6;      //out2=output_sample1/8;
29    #2 input_sample1=7;      //out2=output_sample1/8;
30    #2 input_sample1=8;      //out2=output_sample1/8;
```

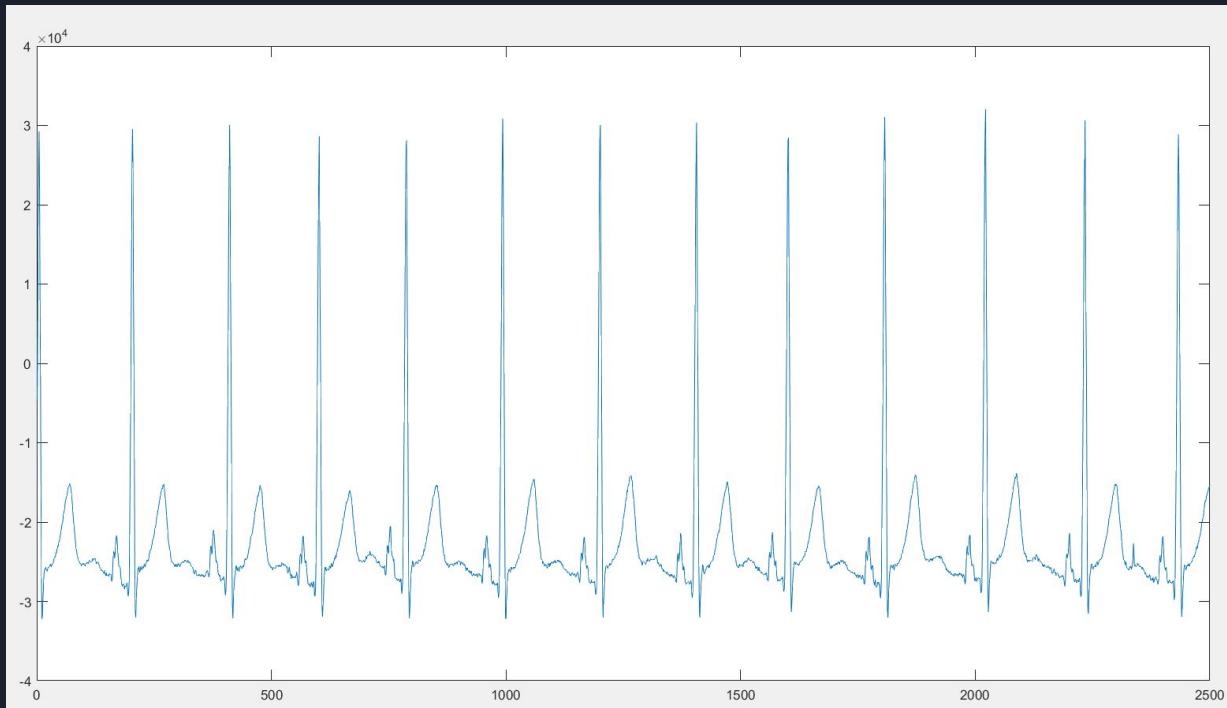
```
36 #:2 input_sample1=15; //out2=output_sample1//;
37 /*
38 #1 reset='b0'; input_sample1=45541;
39
40 #:2 input_sample1 = 55391;
41 #:2 input_sample1 = 67301;
42 #:2 input_sample1 = 74611;
43 #:2 input_sample1 = 79211;
44 #:2 input_sample1 = 71929;
45 #:2 input_sample1 = 57987;
46 #:2 input_sample1 = 48448;
47 #:2 input_sample1 = 34506;
48 #:2 input_sample1 = 22962;
49 #:2 input_sample1 = 17797;
50 #:2 input_sample1 = 18136;
51 #:2 input_sample1 = 20055;
52 #:2 input_sample1 = 21325;
53 #:2 input_sample1 = 22793;
54 #:2 input_sample1 = 23865;
55 #:2 input_sample1 = 24007;
56 #:2 input_sample1 = 24148;
57 #:2 input_sample1 = 24289;
```

- Sampling frequency = 250Hz
- No of samples taken = 2500

```
2536 #:2 input_sample1 = 34252;
2537 #:2 input_sample1 = 34562;
2538 #:2 input_sample1 = 34647;
2539 #1 $finish;
2540 end
2541 endmodule
2542
```

Input

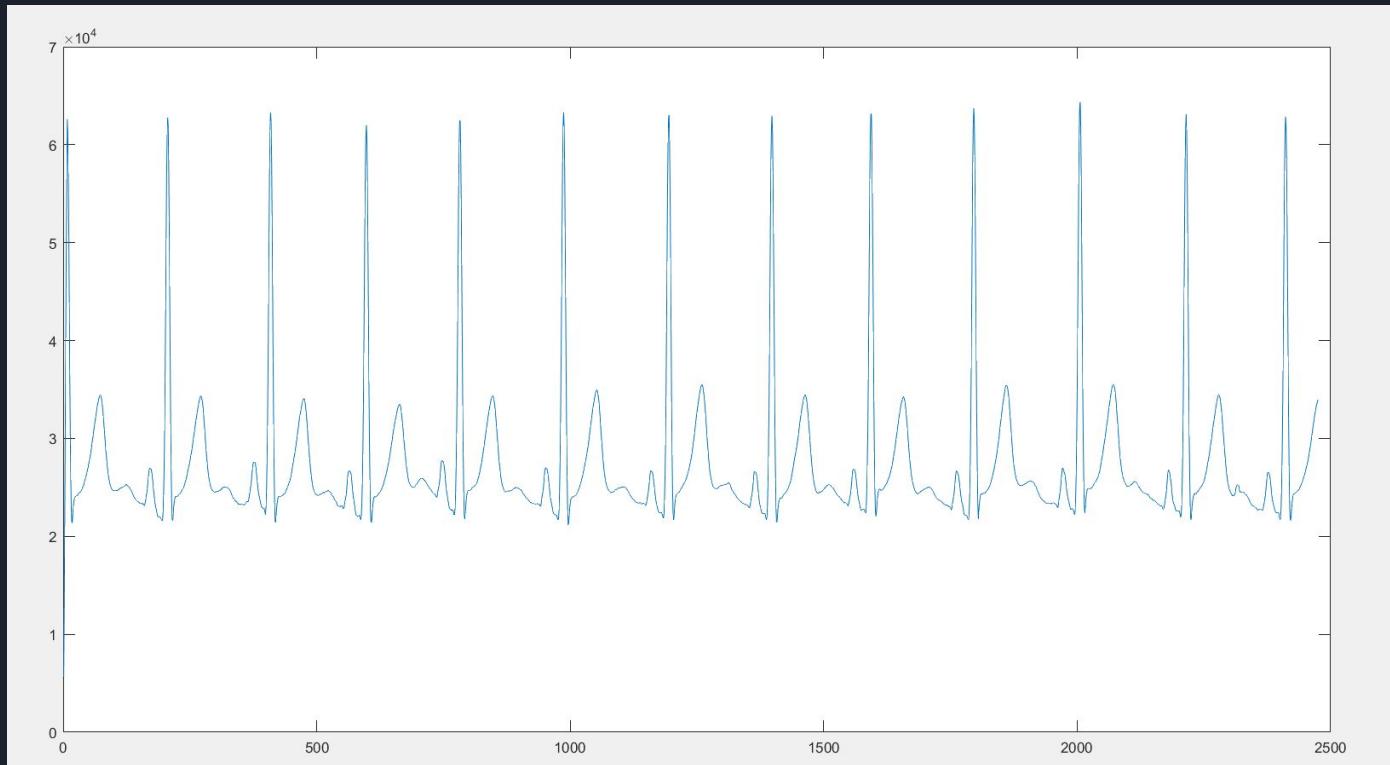
- Input ECG was given through test bench.
- Source of ECG data-Physio Bank ATM



Plot of input made using MATLAB

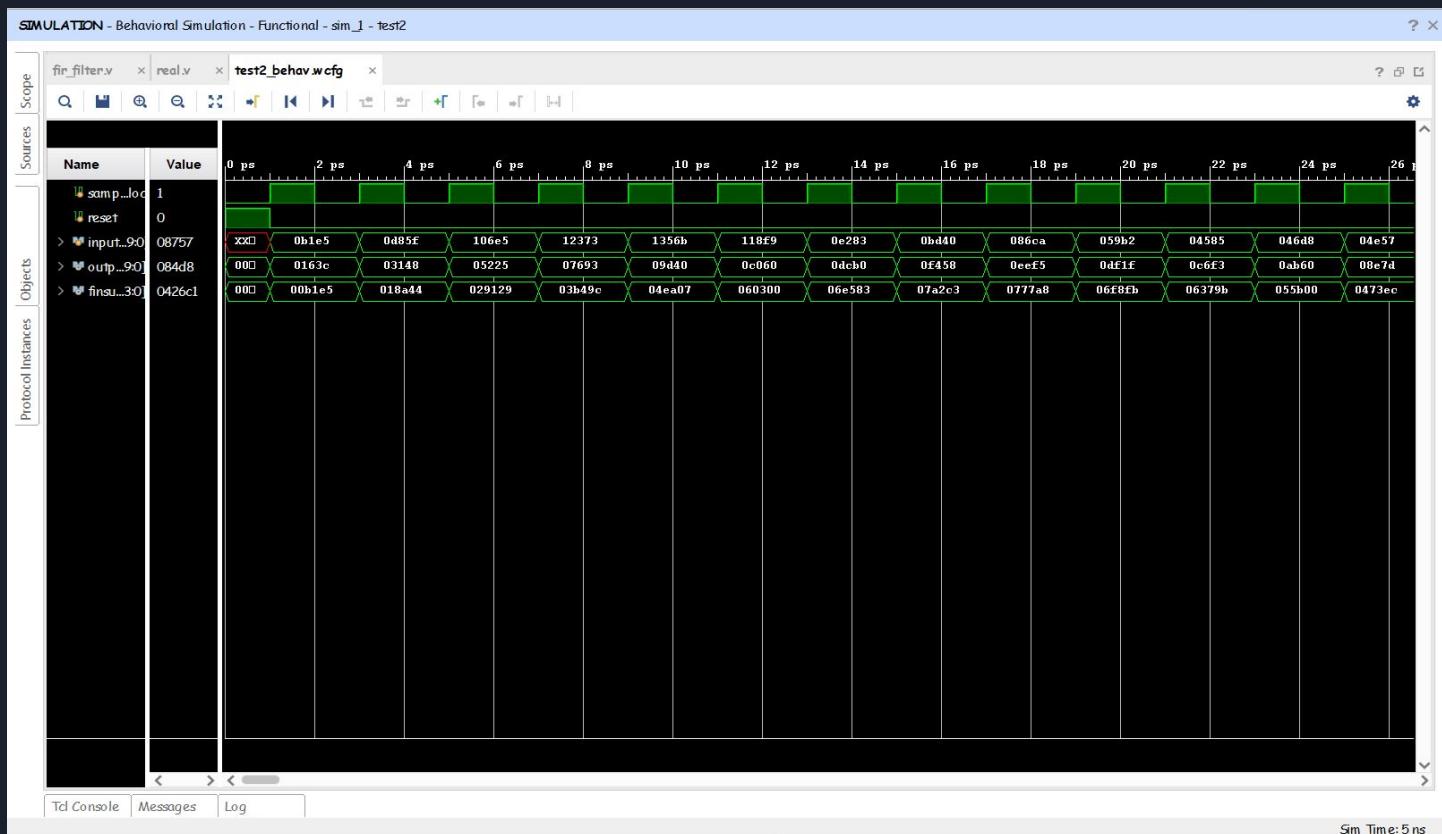
Output

- Output data points were printed on console and were converted to a text file.
- They were plotted using MATLAB

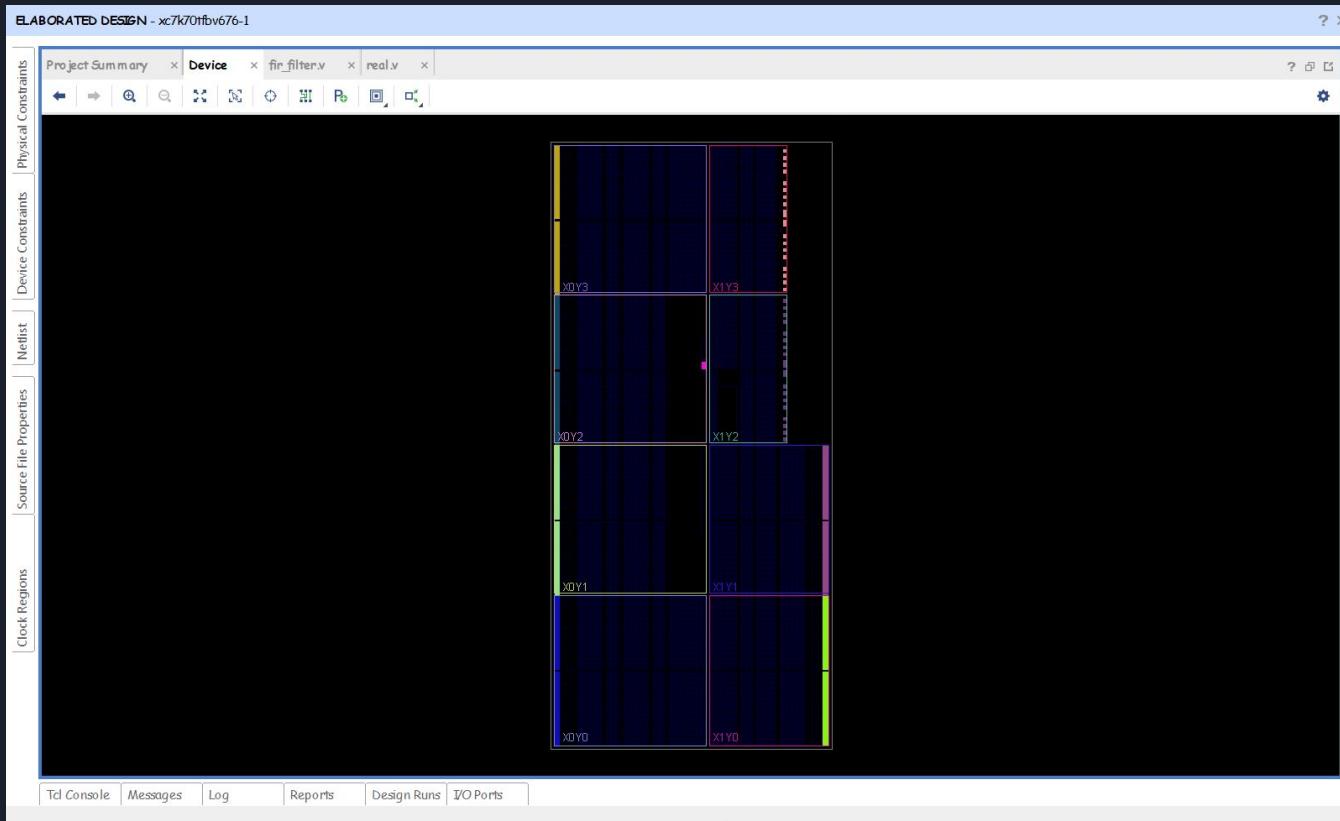


Plot of Output filtered ECG Signal, Cut-off freq = 14 Hz

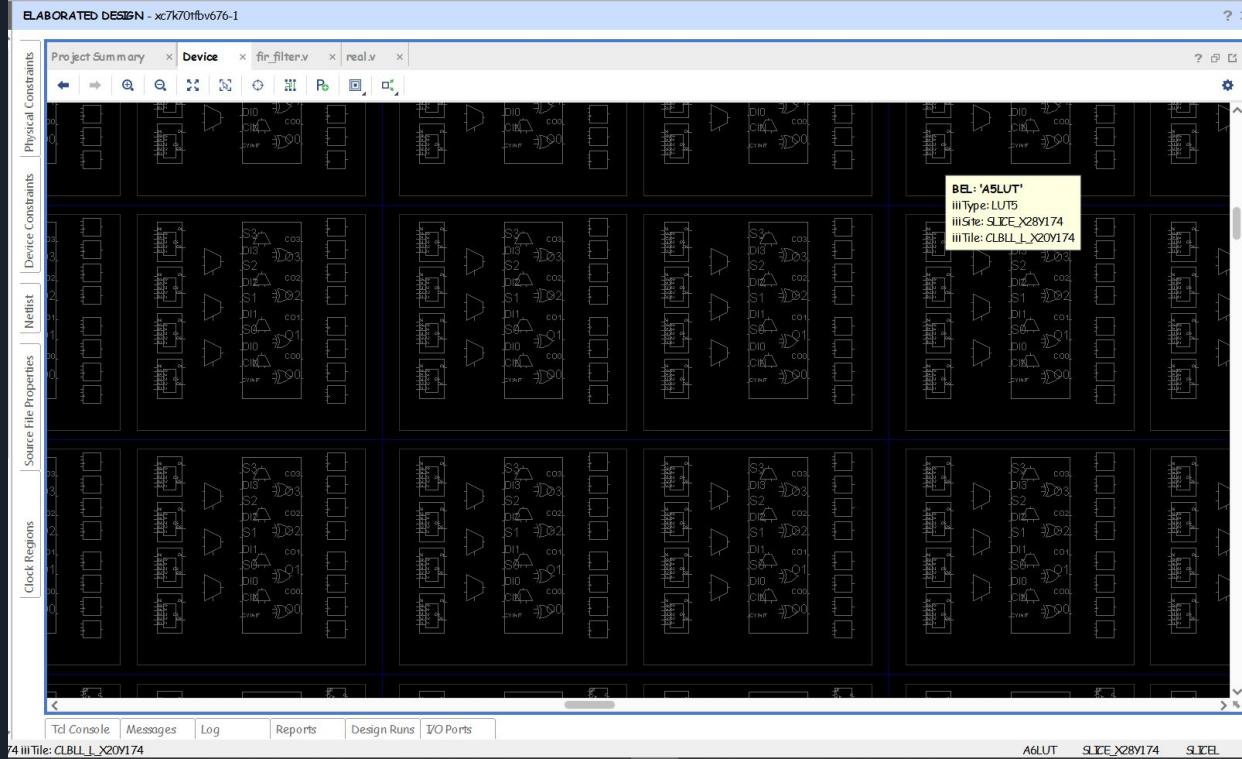
Simulation Results



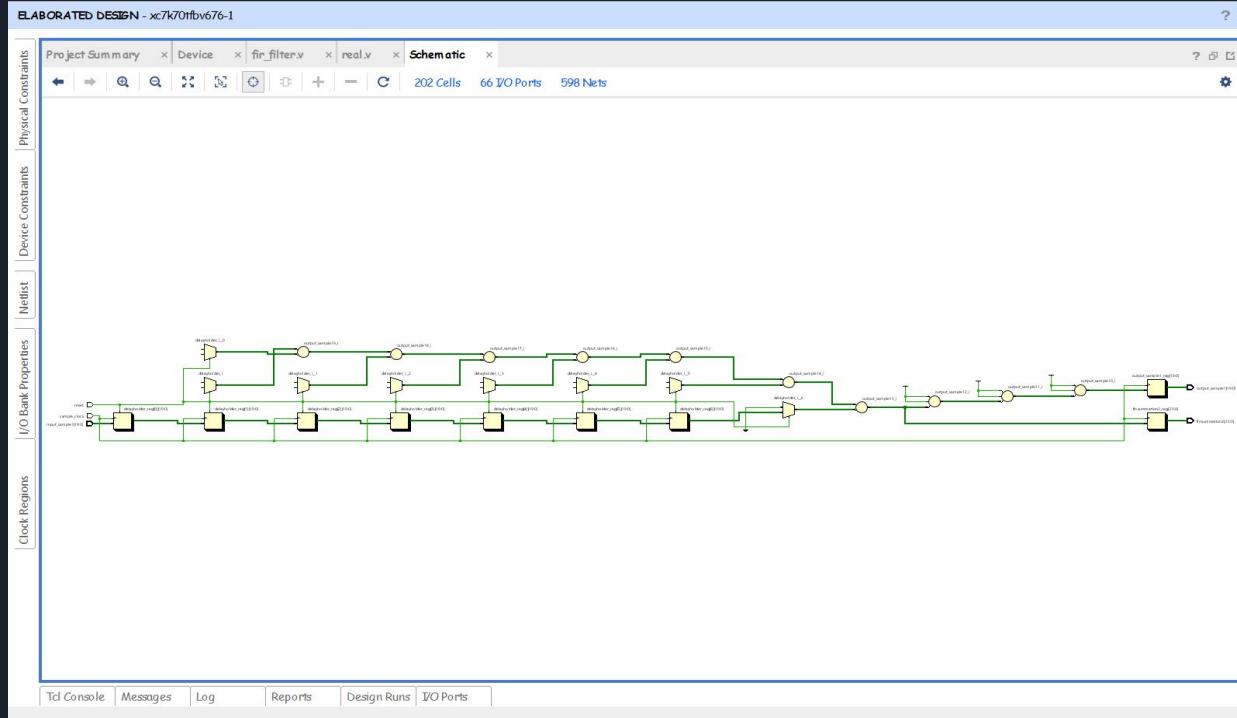
Elaborated Design



Zoomed View

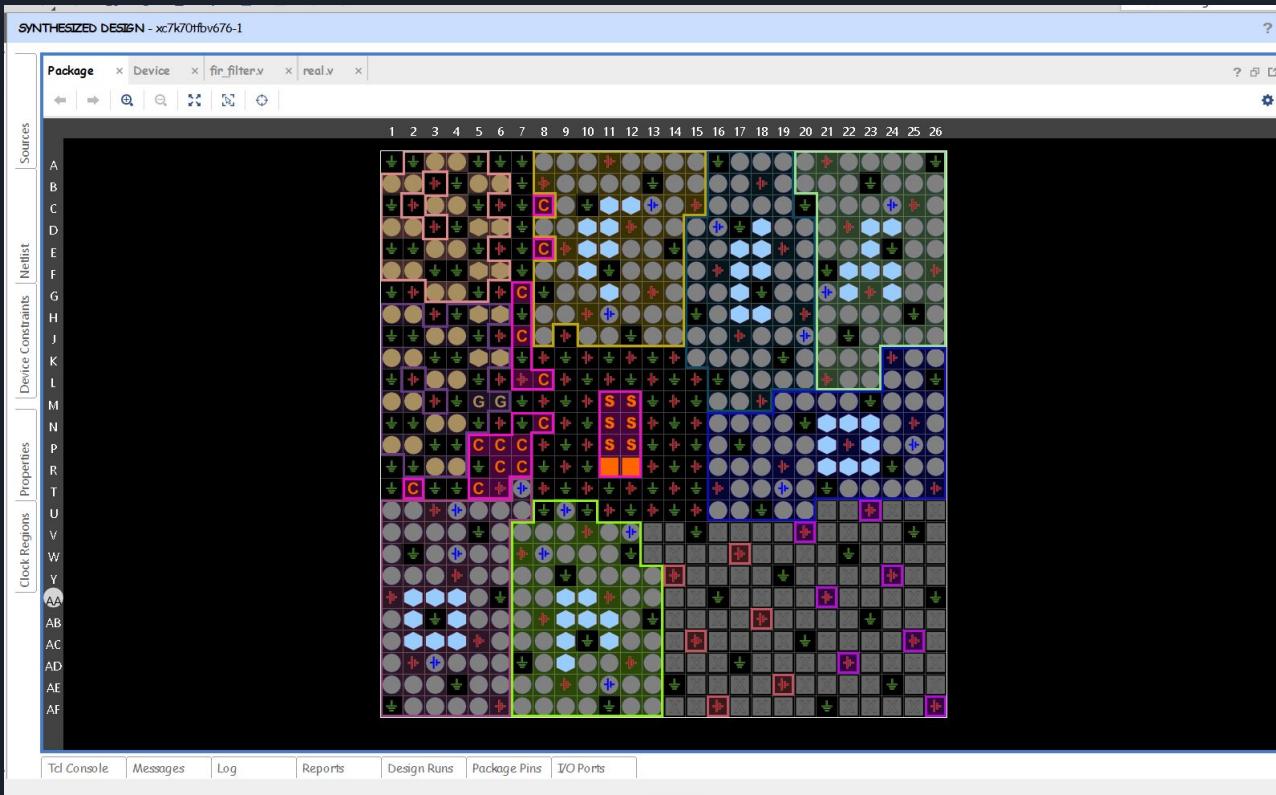


RTL Analysis Schematic



Detailed schematic pdf file location -
project_4\project_4.srcts\RTLA
nalysisSchematic.pdf

Synthesized Design



Post Synthesis Design Timing Summary

SYNTHESIZED DESIGN - xc7k70tfbv676-1

Timing

Constraint Set Properties

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

> Check Timing (275)

 Intro-Clock Paths

 Inter-Clock Paths

 Other Path Groups

 User Ignored Paths

> Unconstrained Paths

Clock Regions

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): inf	Worst Hold Slack (WHS): inf	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: NA
Total Number of Endpoints: 168	Total Number of Endpoints: 168	Total Number of Endpoints: NA

There are no user specified timing constraints.

Timing Summary - timing_1

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports

Post Synthesis Utilization

SYNTHESIZED DESIGN - xc7k70tfbv676-1

Utilization

Hierarchy

Name	Slice LUTs (41000)	Slice Registers (82000)	Bonded IOB (300)	BUFGC ^ TRL
N fir_filter	30	66	66	1

Constraint Set Properties

Clock Regions

Memory

DSP

IO and GT Specific

 Bonded IOB (22%)

Clocking

 BUFGCTRL (3%)

Specific Feature

Primitives

Black Boxes

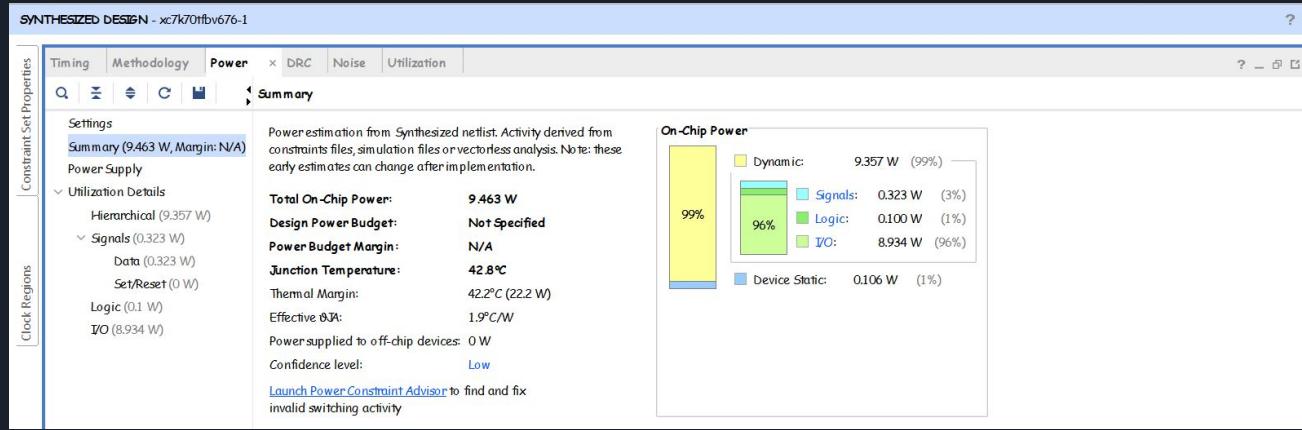
Instantiated Netlists

utilization_1

Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports

The screenshot shows the Utilization report for a synthesized design. The main pane displays a table of resource usage for a component named 'fir_filter'. The table includes columns for Slice LUTs, Slice Registers, Bonded IOBs, and BUFGC TRL. The 'fir_filter' component uses 30 Slice LUTs, 66 Slice Registers, 66 Bonded IOBs, and 1 BUFGC TRL. The left sidebar lists various categories of resources, such as Slice Logic, Memory, DSP, and IO, with their respective utilization percentages. The bottom navigation bar includes links for Tcl Console, Messages, Log, Reports, Design Runs, Package Pins, and I/O Ports.

Post Synthesis Power



SYNTHESIZED DESIGN - xc7k70tfbv676-1

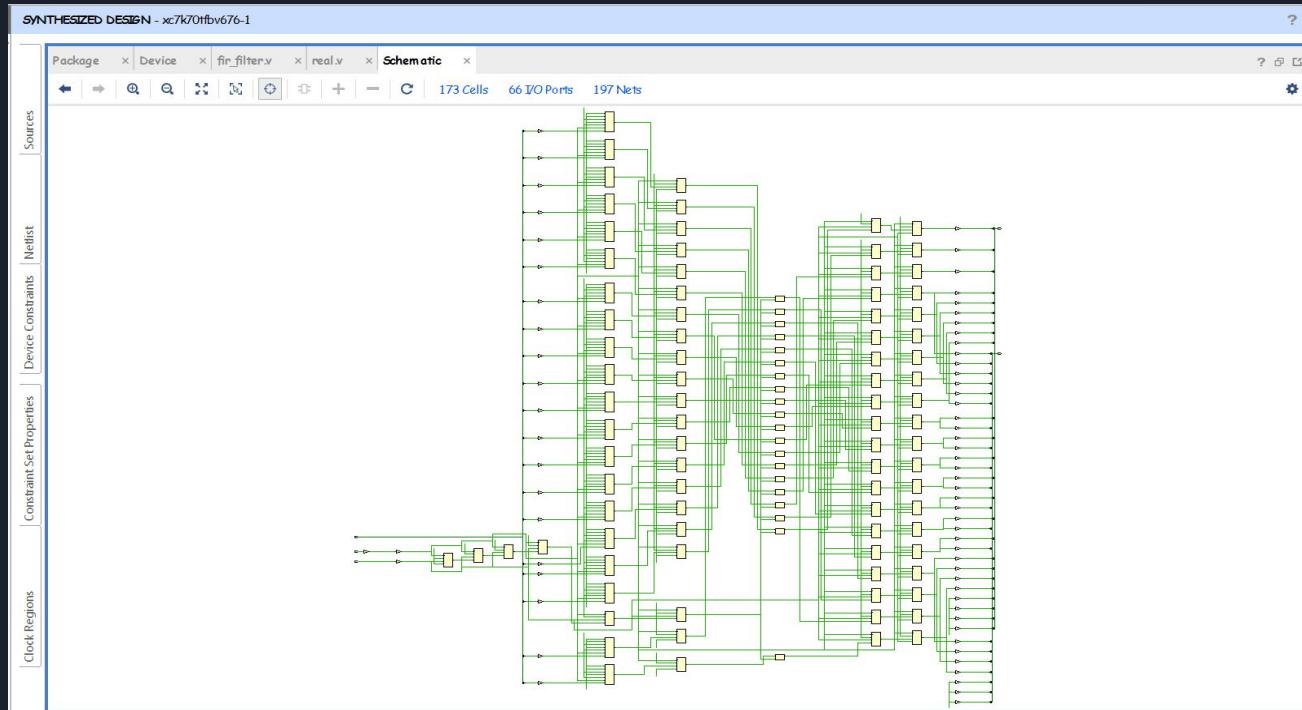
Timing Methodology Power DRC Noise Utilization

I/O

Settings
Summary (9.463 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (9.357 W)
 Signals (0.323 W)
 Data (0.323 W)
 Set/Reset (0 W)
 Logic (0.1 W)
 I/O (8.934 W)

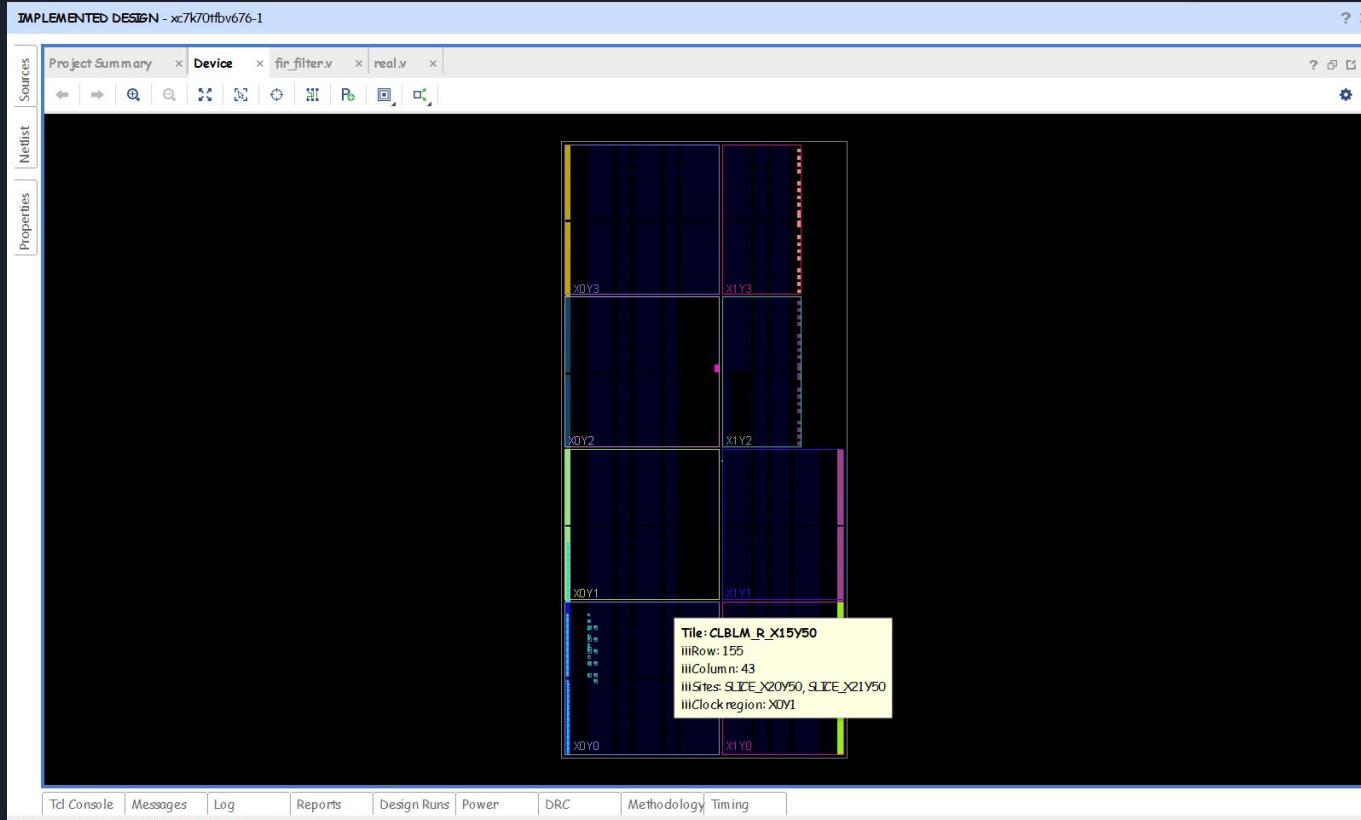
Utilization	Name	I/O Type	I/O Standard	Drive Strength	Input Pins	Output Pins	Bidir Pins	I/O LOGIC SERDES	I/O DELAY
8.934 W (94% of total)	fir_filter	N/A	LVCMS18	12.000	0	24	0	No	Off
4.75 W (50% of total)	finsummation2	N/A	LVCMS18	12.000	0	20	0	No	Off
4.037 W (43% of total)	output_sample1	N/A	LVCMS18	N/A	20	0	0	No	Off
0.14 W (1% of total)	input_sample1	N/A	LVCMS18	N/A	1	0	0	No	Off
0.007 W (< 1% of total)	sample_clock	N/A	LVCMS18	N/A	1	0	0	No	Off
0 W	reset	N/A	LVCMS18	N/A	1	0	0	No	Off

Synthesized Design Schematic

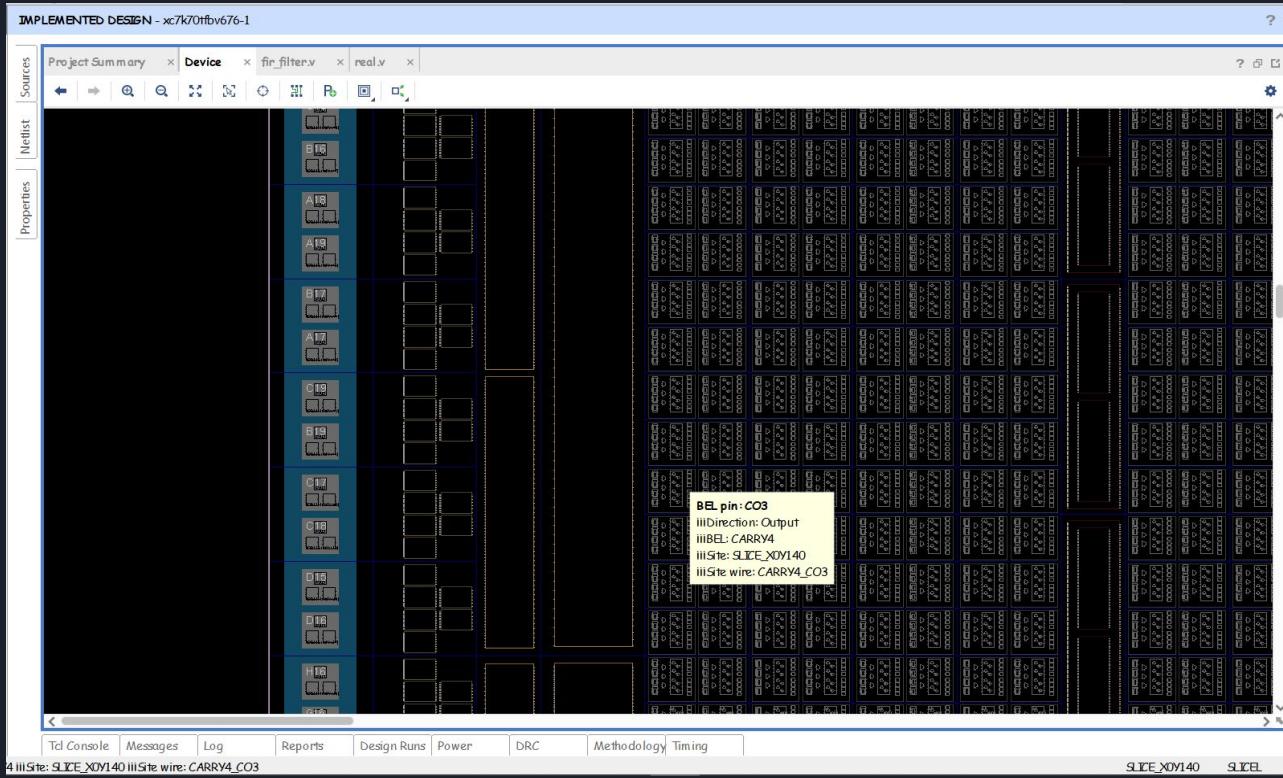


Detailed schematic pdf file location -
project_4\project_4.srcts\postSynthesisSchematic.pdf

Implemented Design



Zoomed View



Post Implementation Timing

IMPLEMENTED DESIGN - xc7k0tfbv676-1

Tcl Console Messages Log Reports Design Runs Power DRC Methodology **Timing** ×

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

> Check Timing (326)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

User Ignored Paths

> Unconstrained Paths

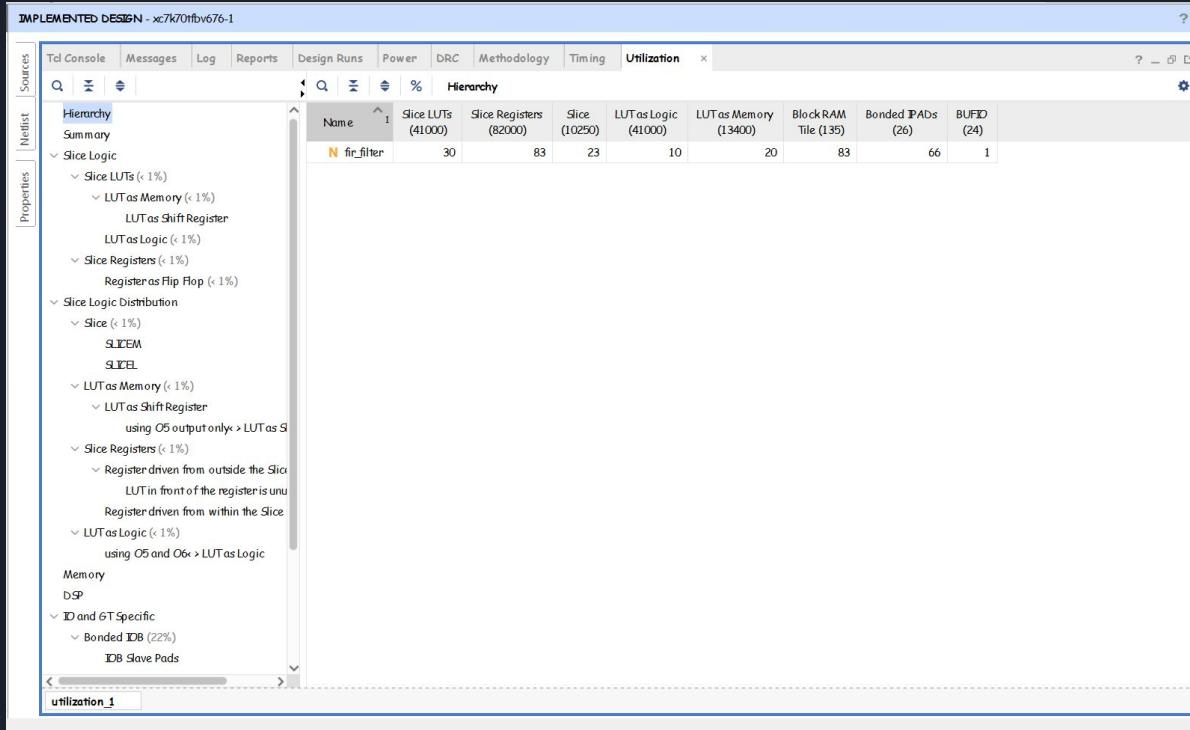
Setup Hold Pulse Width

Worst Negative Slack (WNS): inf	Worst Hold Slack (WHS): inf	Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: NA
Total Number of Endpoints: 202	Total Number of Endpoints: 202	Total Number of Endpoints: NA

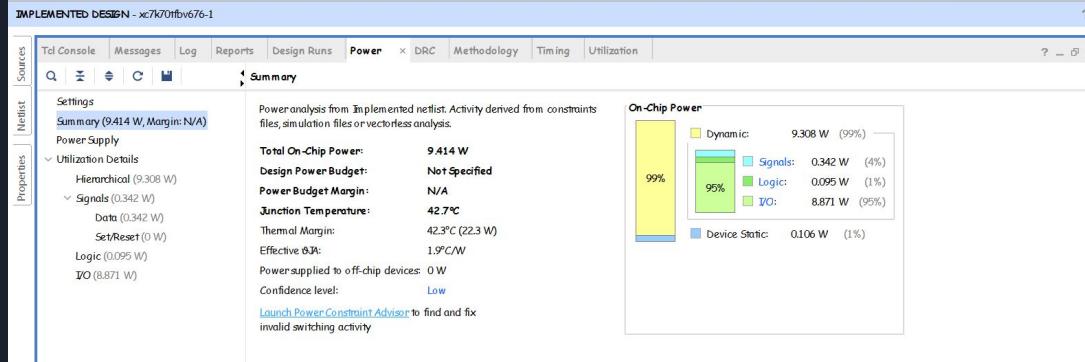
There are no user specified timing constraints.

Timing Summary - impl_J (saved) × Timing Summary - timing_1 ×

Post Implementation Utilization



Post Implementation Power



IMPLEMENTED DESIGN - xc7k0fbv676-1

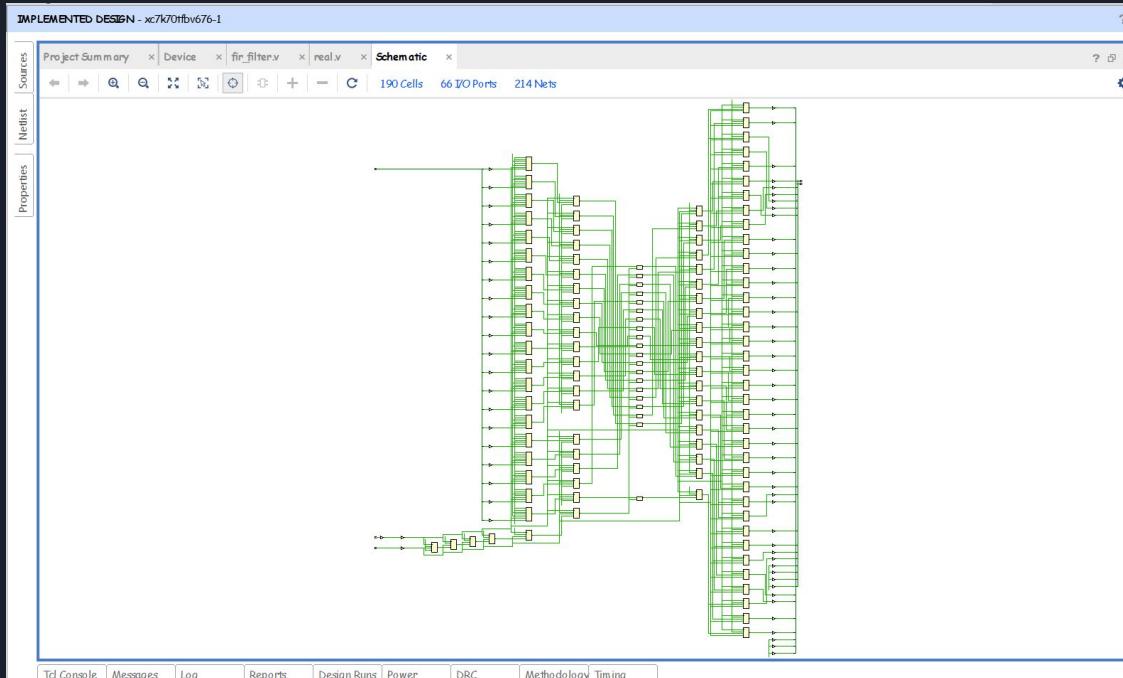
Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization

I/O

Utilization

Name	I/O Type	I/O Standard	Drive Strength	Input Pins	Output Pins	Bidir Pins	ID LOGIC SERDES	ID DE
N_fifofilter	HR	LVCMSI8	12.000	0	24	0	No	Off
finsumation2	HR	LVCMSI8	12.000	0	20	0	No	Off
output_sample1	HR	LVCMSI8	N/A	20	0	0	No	Off
input_sample1	HR	LVCMSI8	N/A	1	0	0	No	Off
sample_clock	HR	LVCMSI8	N/A	1	0	0	No	Off
reset	HR	LVCMSI8	N/A	1	0	0	No	Off

Post Implementation Schematic



Detailed schematic pdf file location -
project_4\project_4.srcts\postImplementationSchematic.pdf

PROJECT SUMMARY:

PROJECT MANAGER - project_4

Sources | Properties | Project Summary | fir_filter.v | ? X

Overview | Dashboard

Synthesis

Status: ✓ Complete
Messages: 4 warnings
Part: xc7k70tfb676-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None

Implementation

Status: ✓ Complete
Messages: 6 warnings
Part: xc7k70tfb676-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None

DRC Violations

Summary: 2 critical warnings
1 warning
[Implemented DRC Report](#)

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
[Implemented Timing Report](#)

Utilization

Post-Synthesis | Post-Implementation

Graph | Table

Utilization (%)

Power

Summary | On-Chip

Total On-Chip Power: 9.414 W
Junction Temperature: 42.7 °C
Thermal Margin: 42.3 °C (22.3 W)
Effective QJA: 1.9 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
[Implemented Power Report](#)

Tcl Console | Messages | Log | Reports | Design Runs



Thank You