**SCHOOL OF MANAGEMENT SCIENCES, LUCKNOW**

**Question Bank**

**Course: B. Tech.** **Branch: CSE, IOT, AIDS, AIML**

**Subject Name: Computer Organization & Architecture** **Subject Code: BCS 302**

**Short Answer type questions:**

1. What is bus arbitration and bus structure?
2. Name the type of buses used in computer Architecture.
3. What are the functions of a processor?
4. List and define the main structural components of a computer.
5. Explain computer organization and architecture.
6. Differentiate between Daisy Chaining and Centralized parallel arbitration.
7. Describe different types of control signals and it's usage.
8. Write short notes on:
    a. Flip-Flops
    b. Multiplexers
9. What do you understand by register stack and memory stack?
10. Describe the need of computer architecture.
11. Explain the need of IEEE Standard for Floating point numbers.
12. Write the advantages of Booth's algorithm.
13. Explain logic operators.
14. Discuss need of biasing with reference to floating point representation.
15. Register A holds the binary values 10011101.What is the register value after arithmetic shift right? Starting from the initial number 10011101, determine the register value after arithmetic shift left.
16. Perform addition and subtraction on the following signed numbers:
    a. (-11) + (+10)
    b. (-13) - (+12)
    c. (+12) + (-10)
    d. (+12) - (+10)
17. What is an instruction format? Write the different types of instruction formats.
18. Categorize the following instructions:
    a. JUMP 2000
    b. MOVR1, 2085
    c. INCR 4
    d. CMPR0, R1
19. What is a control memory and control word?
20. Explain Micro-program sequencer.
21. Explain different phases of instruction cycle.

22. Explain the meaning of parallelism and pipelining.
23. Write the differences between RISC and CISC.
24. What do you understand by micro-operations?
25. Differentiate between Interrupt and Sub-program.
26. Define the parameters used for the evaluation of performance of a processor.
27. List the differences between static RAM and dynamic RAM.
28. Differentiate between spatial locality and temporal locality.
29. Explain multilevel cache organization.
30. Explain the terms address space and memory space.
31. Explain HIT ratio and MISS ratio in cache memory.
32. A computer uses RAM chips with capacity of 1024 * 8. Calculate the number of chips required to provide a memory capacity of 16 KB.
33. Define associative memory. Also list its advantages and disadvantages.
34. List the functions performed by Input-Output interface.
35. Explain the terms Burst mode and Cycle Stealing mode.
36. Define vectored interrupt and non-vectored interrupt.
37. Write a short note on I/O interface.
38. Differentiate between isolated I/O and memory mapped I/O.
39. What is an interrupt? List the types of interrupts.
40. Discuss drawbacks of programmed and interrupt-driven I/O.

**Long Answer type questions:**

1. List the different types of addressing modes. Explain any five with suitable examples.
2. What do you mean by processor organization? Explain various types of processor organization.
3. What is an effective address? How it is calculated in different types of addressing modes? Explain.
4. Differentiate between Vonn Neumann and Harvard Architecture.
5. Define bus arbitration. Explain various methods of bus arbitration.
6. Discuss stack organization. Explain register stack and memory stack.
7. Explain bus architecture and multiple bus organization in detail.
8. A digital computer has common bus system for 16 registers of 16 bits each. The bus is constructed with multiplexers. Calculate the size of multiplexer and total number of multiplexers needed.
9. Explain 4-bit carry look ahead adder with diagram.
10. Represent the following decimal number in IEEE Standard Floating Point format in a single precision representation method:
    a. (2345.175)
    b. (-138.2235)
11. Using Booth's Algorithm perform the multiplication on the following signed binary

numbers:

a. (-13) * (-13)
b. (+21) *(-18)

12. Explain 2-bit by 2-bit array multiplier. Elaborate with diagram.

13. Explain the flowchart for division algorithm of restoring and non-restoring method for signed numbers.

14. Draw flowchart for instruction cycle of computer and explain the instruction execution sequence.

15. What is a sub-program? Explain its characteristics and its working.
16. Suppose every instruction is one word long, as well as every address. Calculate the number of memory accesses required in the following instructions:
    ADD, R1, R2, R3; (Register Addressing Mode)
    ADD, R1, R2, (R3); (Direct Addressing Mode)
    ADD, R1, R2, @R3; (Memory Indirect Addressing Mode)
17. Differentiate between horizontal and vertical micro-programmed control unit. Also explain the internal description of hardwired control unit.
18. Define the terms:
    a. Parallelism
    b. Micro-program
    c. HALT instruction
    d. Micro-instructions
19. What is micro-operation? Write the micro-operations for the sub-cycles of instruction cycle.
20. Describe the usage of RISC pipeline and explain the different stages required in the pipeline.
21. Write the micro-operations for the following instructions:
    I1: ADD R1, R3; [R1 = R1 + R3]
    I2: ADD R1, (R3); [R1 = R1 + (R3)]
22. Explain the concept of pipelining and types of pipelining.
23. Identify the number of Read After Write, Write After Read and Write After write hazards in the following program segment:
    I1: R0 = R1 + R2
    I2: R1 = R2 + R3
    I3: R2 = R3 * R0
    I4: R1 = R4 * R2
    I5: R0 = R5 / R6
    I6: R4 = R0 / R1
24. Illustrate the general model of control unit and write the functions of control unit.
25. Explain the different types of instructions in a categorical manner.
26. A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address

instructions, then, calculate number of one-address instructions that can be formulated.

27. Consider a hypothetical control unit which supports 512 control words memory. There are 32 branch instructions to control branch logic. There are 78 control signals and 8 flags present in the hardware. What will be the size of control word and control memory while using vertical micro-programmed control unit?
28. A hypothetical computer supports 286 instructions. Each instruction takes 15 cycles to complete the execution. CPU uses the vertical micro programmed control unit. Also the hardware contains 264 control signals and 20 flags with 23 branch logic conditions. What will be the size of CAR and CDR registers?
29. Write a program to evaluate arithmetic expression
    X = (A-B) * (((C – D * E )/F)/G)
    By using (i) Three address instructions, (ii) Two address instructions, (iii) One address instructions, (iv) Zero address instructions
30. Define the ways of writing policy into cache memory. Also explain cache coherence.
31. Write short notes on
    a. Magnetic disk
    b. Magnetic tape
    c. Optical disk
32. Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost.
33. Compare different mapping techniques used in cache memory and their relative merits and demerits.
34. Discuss primary and secondary memories in detail. Show their classification.
35. Explain the concept of virtual memory. Discuss memory mapping table for mapping virtual address into physical address.
36. Calculate the page fault for a given string with the help of FIFO and LRU page replacement algorithm.
    Size of Frame: 4
    String: 1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 3, 7, 6, 3, 2, 1, 2, 3, 6
37. Discuss 2D RAM and 2.5D RAM with suitable diagram.
38. Consuder a cache (M1) and memory (M2) hierarchy with following characteristics:
    M1: 16K word, 50ns Access Time,
    M2: 1M word, 400 ns Access Time
    Assume 8-word cache block and set size 256 words with set associative mapping.
    (i) Calculate the effective memory access time with cache hit rstio = 0.95.
    (ii) Show and explain mapping between M1 and M2.
39. Consider a cache (initially empty) with 4 cache lines & the following main memory block references: 4, 5, 7, 12, 4, 5, 13, 4, 5, 7
    Identify the hit ratio using (i) FIFO (ii) LRU (iii) Direct mapping (iv) 2-way set associative using LRU.
40. Elaborate disk structure and its working with a schematic diagram.
41. Discuss the different methods of asynchronous data transfer. Explain in detail.
42. Explain different modes of data transfer.
43. Elaborate the working of a DMA controller module with a neat and clean diagram.
44. Draw the block diagram of CPU-IOP communication and explain.

45. Draw the design of Input-Output interface. Also explain the functions of I/O interface.
46. Define interrupt. Also discuss different types of interrupts.
47. Explain the procedure of working of interrupt. Also explain the types of approaches to service the interrupt.
48. Consider 1mbps I/O device which is interfaced to the CPU in a cycle stealing mode of DMA. Whenever 16B data is available in the buffer, then, it is transferred to the main memory. The latency of MM is 8 microseconds. Calculate the CPU time consumed for the DMA operation.
49. Explain the various configurations of DMA.
50. Differentiate between
    a. Strobe control and handshaking asynchronous data transfer
    b. Processor and IOP
    c. Synchronous and Asynchronous transmission